MCU_ABC

U1A

WKUP		PA0	23
		PA1	24
	GBC_RX	PA2	25
	GBC_TX	PA3	26
DCMI_HREF		PA4	29
		PA5	30
DCMI_PCLK		PA6	31
DCMI_RESET		PA7	32
DCMI_XCLK		PA8	67
	USART1_TX	PA9	68
	USART1_RX	PA10	69
	USB_D-	PA11	70
	USB_D+	PA12	71
	SWDIO	PA13	72
	SWDCLK	PA14	76
KEY0		PA15	77
	T_SCK	PB0	35
	T_PEN	PB1	36
	BOOT1	PB2	37
	T_MOSI	PB3	89
		PB4	90
	LCD_BL	PB5	91
DCMI_D5		PB6	92
DCMI_VSYNC		PB7	93
DCMI_D6		PB8	95
DCMI_D7		PB9	96
DCMI_SCL	IIC_SCL	PB10	47
DCMI_SDA	IIC_SDA	PB11	48
	SPI2_CS	PB12	51
	SPI2_SCK	PB13	52
	SPI2_MISO	PB14	53
	SPI2_MOSI	PB15	54
		PC0	15
		PC1	16
	GBC_KEY	PC2	17
	GBC_LED	PC3	18
DCMI_PWDN		PC4	33
	T_CS	PC5	34
DCMI_D0		PC6	63
DCMI_D1		PC7	64
DCMI_D2	SDIO_D0	PC8	65
DCMI_D3	SDIO_D1	PC9	66
	SDIO_D2	PC10	78
DCMI_D4	SDIO_D3	PC11	79
	SDIO_CLK	PC12	80
		PC13	7

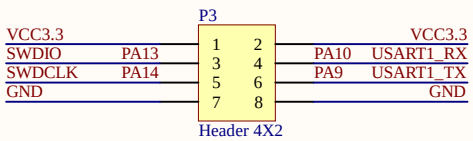
PA0/USART2_CTS/UART4_TX/ETH_MII_CRS/TIM2_CH1_ETR/TIM5_CH1/TIM8_ETR/ADC123_IN0/WKUP
PA1/USART2_RTS/UART4_RX/ETH_RMII_REF_CLK/ETH_MII_RX_CLK/TIM5_CH2/TIM2_CH2/ADC123_IN1
PA2/USART2_TX/TIM5_CH3/TIM9_CH1/TIM2_CH3/ETH_MDIO/ADC123_IN2
PA3/USART2_RX/TIM5_CH4/TIM9_CH2/TIM2_CH4/OTG_HS_ULPI_D0/ETH_MII_COL/ADC123_IN3
PA4/SPI1_NSS/SPI3_NSS/USART2_CK/DCMI_HSYNC/OTG_HS_SOF/I2S3_WS/ADC12_IN4/DAC_OUT1
PA5/SPI1_SCK/OTG_HS_ULPI_CK/TIM2_CH1_ETR/TIM8_CH1N/ADC12_IN5/DAC_OUT2
PA6/SPI1_MISO/TIM8_BKIN/TIM13_CH1/DCMI_PIXCLK/TIM3_CH1/TIM1_BKIN/ADC12_IN6
PA7/SPI1_MOSI/TIM8_CH1N/TIM14_CH1/TIM3_CH2/ETH_MII_RX_DV/TIM1_CH1N/ETH_RMII_CRS_DV/ADC12_IN7
PA8/MCO1/USART1_CK/TIM1_CH1/I2C3_SCL/OTG_FS_SOF
PA9/USART1_TX/TIM1_CH2/I2C3_SMBA/DCMI_D0/OTG_FS_VBUS
PA10/USART1_RX/TIM1_CH3/OTG_FS_ID/DCMI_D1
PA11/USART1_CTS/CAN1_RX/TIM1_CH4/OTG_FS_DM
PA12/USART1_RTS/CAN1_TX/TIM1_ETR/OTG_FS_DP
PA13/JTMS-SWDIO
PA14/JTCK-SWCLK
PA15/JTDI/SPI3_NSS/I2S3_WS/TIM2_CH1_ETR/SPI1_NSS

PB0/TIM3_CH3/TIM8_CH2N/OTG_HS_ULPI_D1/ETH_MII_RXD2/TIM1_CH2N/ADC12_IN8
PB1/TIM3_CH4/TIM8_CH3N/OTG_HS_ULPI_D2/ETH_MII_RXD3/TIM1_CH3N/ADC12_IN9
PB2/BOOT1
PB3/JTDO/TRACESWO/SPI3_SCK/I2S3_CK/TIM2_CH2/SPI1_SCK
PB4/NJTRST/SPI3_MISO/TIM3_CH1/SPI1_MISO/I2S3ext_SD
PB5/I2C1_SMBA/CAN2_RX/OTG_HS_ULPI_D7/ETH_PPS_OUT/TIM3_CH2/SPI1_MOSI/SPI3_MOSI/DCMI_D10/I2S3_SD
PB6/I2C1_SCL/TIM4_CH1/CAN2_TX/DCMI_D5/USART1_TX
PB7/I2C1_SDA/FSMC_NL/DCMI_VSYNC/USART1_RX/TIM4_CH2
PB8/TIM4_CH3/SDIO_D4/TIM10_CH1/DCMI_D6/ETH_MII_TXD3/I2C1_SCL/CAN1_RX
PB9/SPI2_NSS/I2S2_WS/TIM4_CH4/TIM11_CH1/SDIO_D5/DCMI_D7/I2C1_SDA/CAN1_TX
PB10/SPI2_SCK/I2S2_CK/I2C2_SCL/USART3_TX/OTG_HS_ULPI_D3/ETH_MII_RX_ER/TIM2_CH3
PB11/I2C2_SDA/USART3_RX/OTG_HS_ULPI_D4/ETH_RMII_TX_EN/ETH_MII_TX_EN/TIM2_CH4
PB12/SPI2_NSS/I2S2_WS/I2C2_SMBA/USART3_CK/TIM1_BKIN/CAN2_RX/OTG_HS_ULPI_D5/ETH_RMII_TXD0/ETH_MII_TXD0/OTG_HS_ID
PB13/SPI2_SCK/I2S2_CK/USART3_CTS/TIM1_CH1N/CAN2_TX/OTG_HS_ULPI_D6/ETH_RMII_TXD1/ETH_MII_TXD1/OTG_HS_VBUS
PB14/SPI2_MISO/TIM1_CH2N/TIM12_CH1/OTG_HS_DM/USART3_RTS/TIM8_CH2N/I2S2ext_SD
PB15/SPI2_MOSI/I2S2_SD/TIM1_CH3N/TIM8_CH3N/TIM12_CH2/OTG_HS_DP/RTC_REFIN

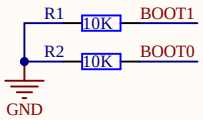
PC0/OTG_HS_ULPI_STP/ADC123_IN10
PC1/ETH_MDC/ADC123_IN11
PC2/SPI2_MISO/OTG_HS_ULPI_DIR/ETH_MII_TXD2/I2S2ext_SD/ADC123_IN12
PC3/SPI2_MOSI/I2S2_SD/OTG_HS_ULPI_NXT/ETH_MII_TX_CLK/ADC123_IN13
PC4/ETH_RMII_RX_D0/ETH_MII_RX_D0/ADC12_IN14
PC5/ETH_RMII_RX_D1/ETH_MII_RX_D1/ADC12_IN15
PC6/I2S2_MCK/TIM8_CH1/SDIO_D6/USART6_TX/DCMI_D0/TIM3_CH1
PC7/I2S3_MCK/TIM8_CH2/SDIO_D7/USART6_RX/DCMI_D1/TIM3_CH2
PC8/TIM8_CH3/SDIO_D0/TIM3_CH3/USART6_CK/DCMI_D2
PC9/I2S_CKIN/MCO2/TIM8_CH4/SDIO_D1//I2C3_SDA/DCMI_D3/TIM3_CH4
PC10/SPI3_SCK/I2S3_CK/UART4_TX/SDIO_D2/DCMI_D8/USART3_TX
PC11/UART4_RX/SPI3_MISO/SDIO_D3/DCMI_D4/USART3_RX/I2S3ext_SD
PC12/UART5_TX/SDIO_CK/DCMI_D9/SPI3_MOSI/I2S3_SD/USART3_CK
PC13/RTC_OUT/RTC_TAMP1/RTC_TS

STM32F407VGT6

SWD & USART1



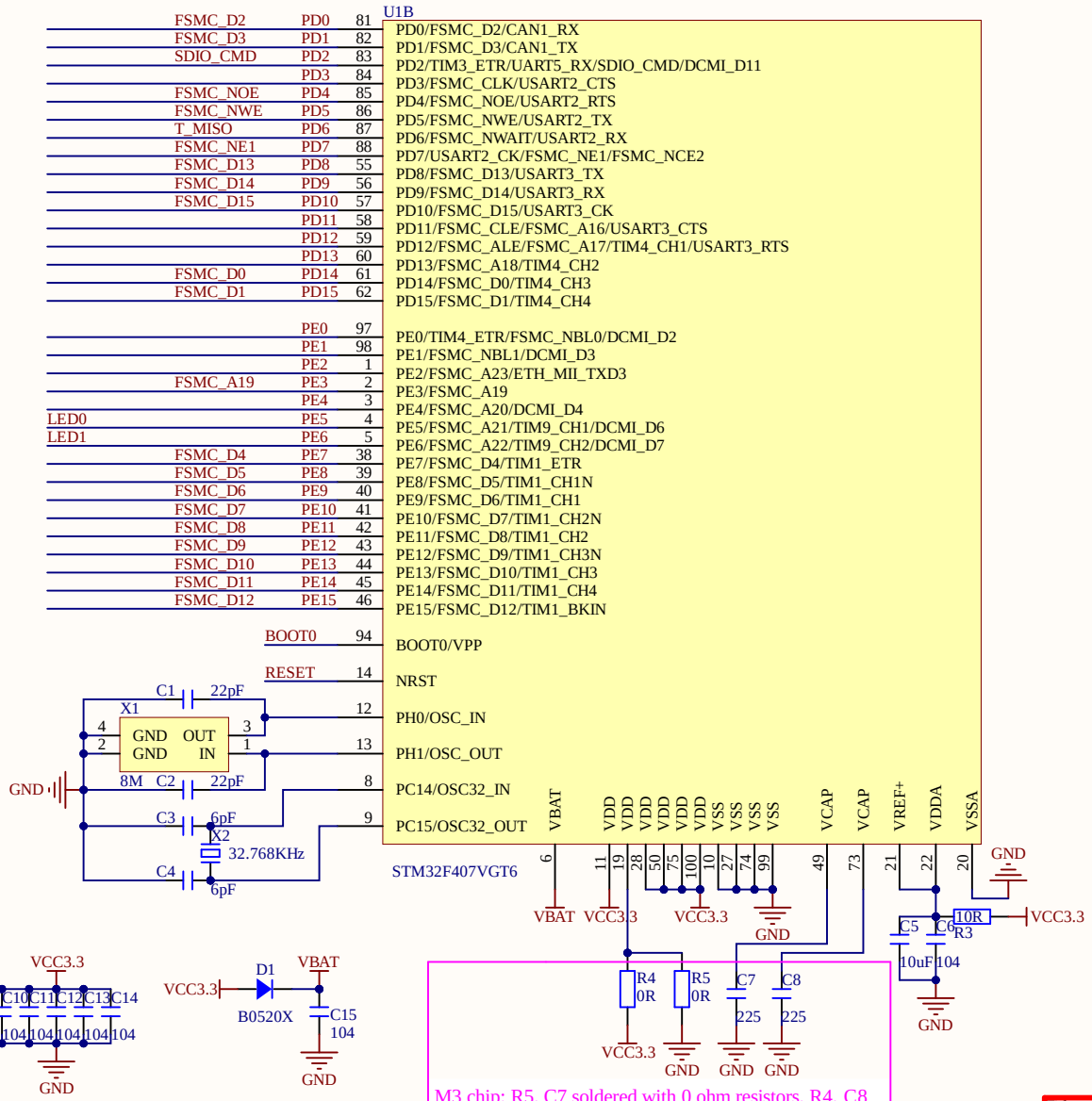
BOOT



Title: M100Z-M3&4.PrjPcb	
Author: *	Size: A2
Date: 2024/5/15	File: M100Z-M3&4_CPU_ABC.SchDoc
Revision: *	Version: *

正点原子

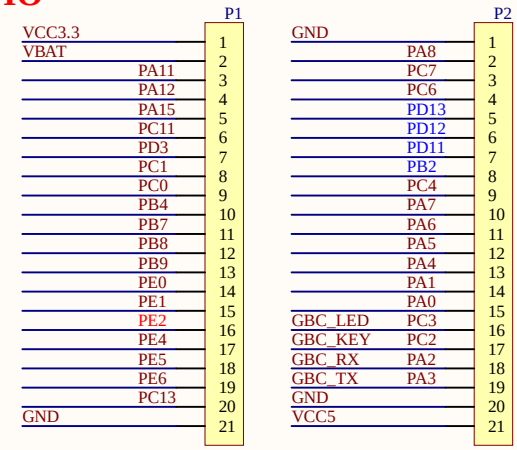
MCU_DE



Title: M100Z-M3&4.PrjPcb	
Author: *	Size: A2
Date: 2024/5/15	File: M100Z-M3&4_CPU_DE.SchDoc
Revision: *	Version: *

正点原子

IO



Blue section IO ports:

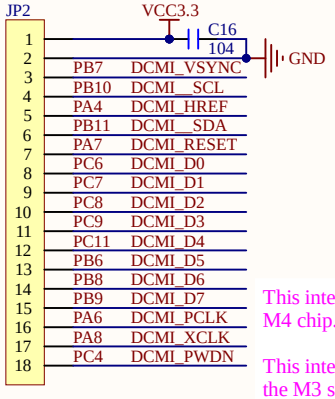
There are differences between M7 and M3/4!
Full compatibility cannot be achieved!

For compatibility, please use other IO ports.

If compatibility is not considered, then all IO ports can be used normally.

PE2 is used as QSPI data line on M7, so it is generally not used as IO on M7. However, on M3/4, it can be used as a general-purpose IO.

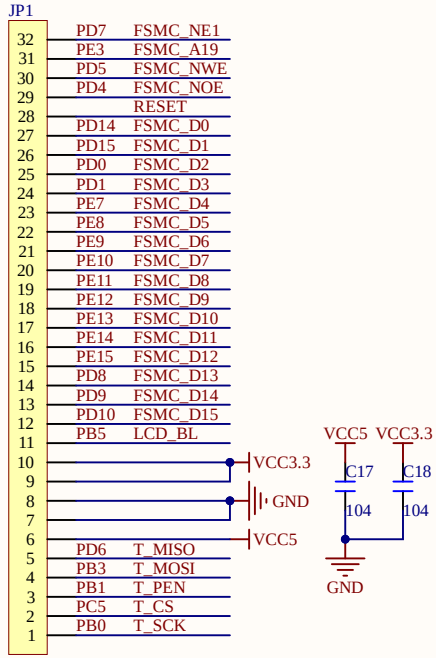
CAMERA



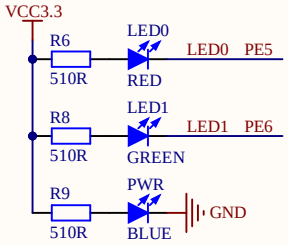
This interface is only valid for the M4 chip.

This interface is not soldered for the M3 series chip.

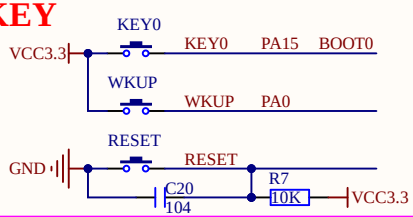
TFTLCD



LED

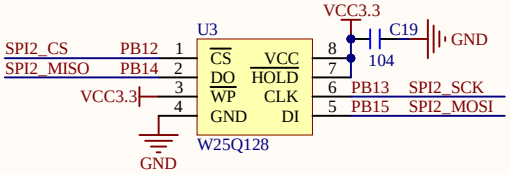


KEY

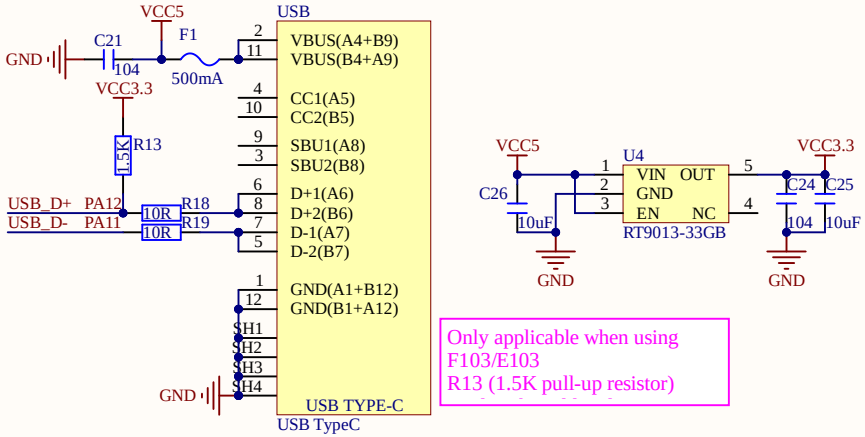


Entering the default BootLoader mode:
First, press and hold KEY0 (BOOT0 = 1)
Then press the reset button on the board and release it.At this point, the MCU will enter Bootloader mode.

FLASH

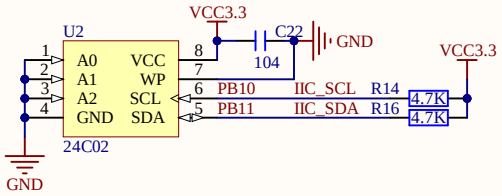


USB & POWER

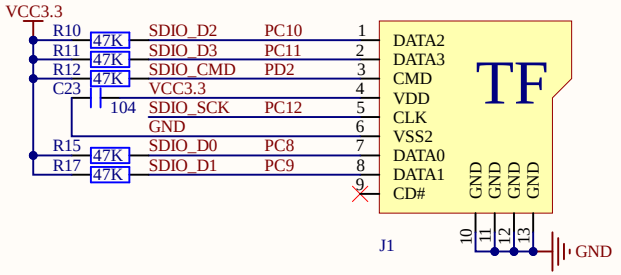


Only applicable when using F103/E103
R13 (1.5K pull-up resistor)

EEPROM

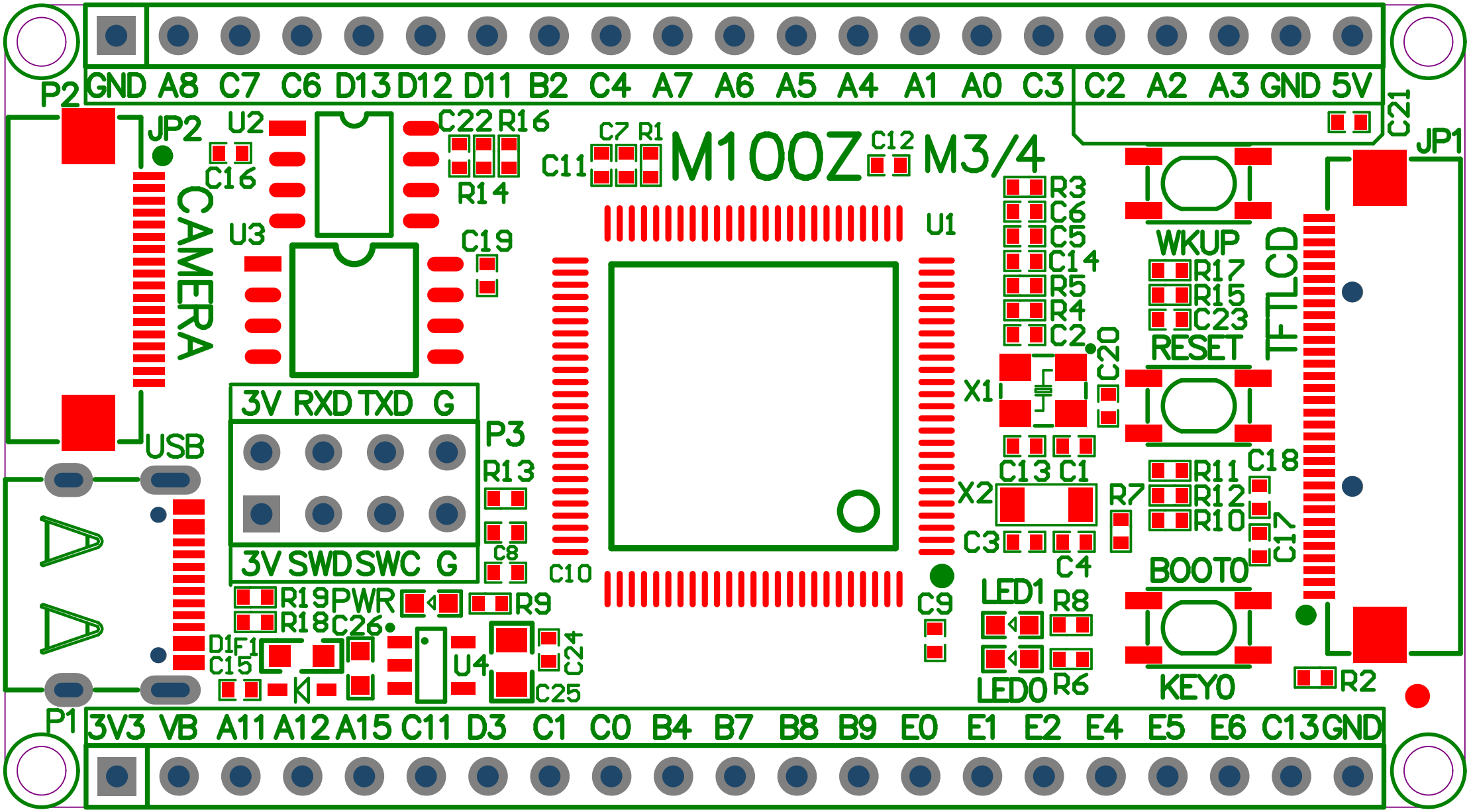


TF CARD



Title: M100Z-M3&4.PrjPcb	
Author: *	Size: A1
Date: 2024/5/15	File: M100Z-M3&4_DEVICE.SchDoc
Revision: *	Version: *

正点原子


P2
GND A8 C7 C6 D13 D12 D11 B2 C4 A7 A6 A5 A4 A1 A0 C3 C2 A2 A3 GND 5V
JP2
CAMERA
U2
C16
C22 R16
R14
U3
C19
C7 R1
C11
M100Z
C12
M3/4
C21
JP1
U1
R3
C6
C5
C14
R5
R4
C2
C20
X1
C13 C1
X2
C3
C4
C10
C9
LED1
R8
LED0
R6
WKUP
R17
R15
C23
RESET
TFTLCD
R11
R12
R10
C18
C17
R7
BOOT0
KEY0
R2
USB
3V RXD TXD G
P3
R13
C8
3V SWD SWC G
R19 PWR
R9
R18 C26
D1 F1
C15
U4
C24
C25
P1
3V3 VB A11 A12 A15 C11 D3 C1 C0 B4 B7 B8 B9 E0 E1 E2 E4 E5 E6 C13 GND