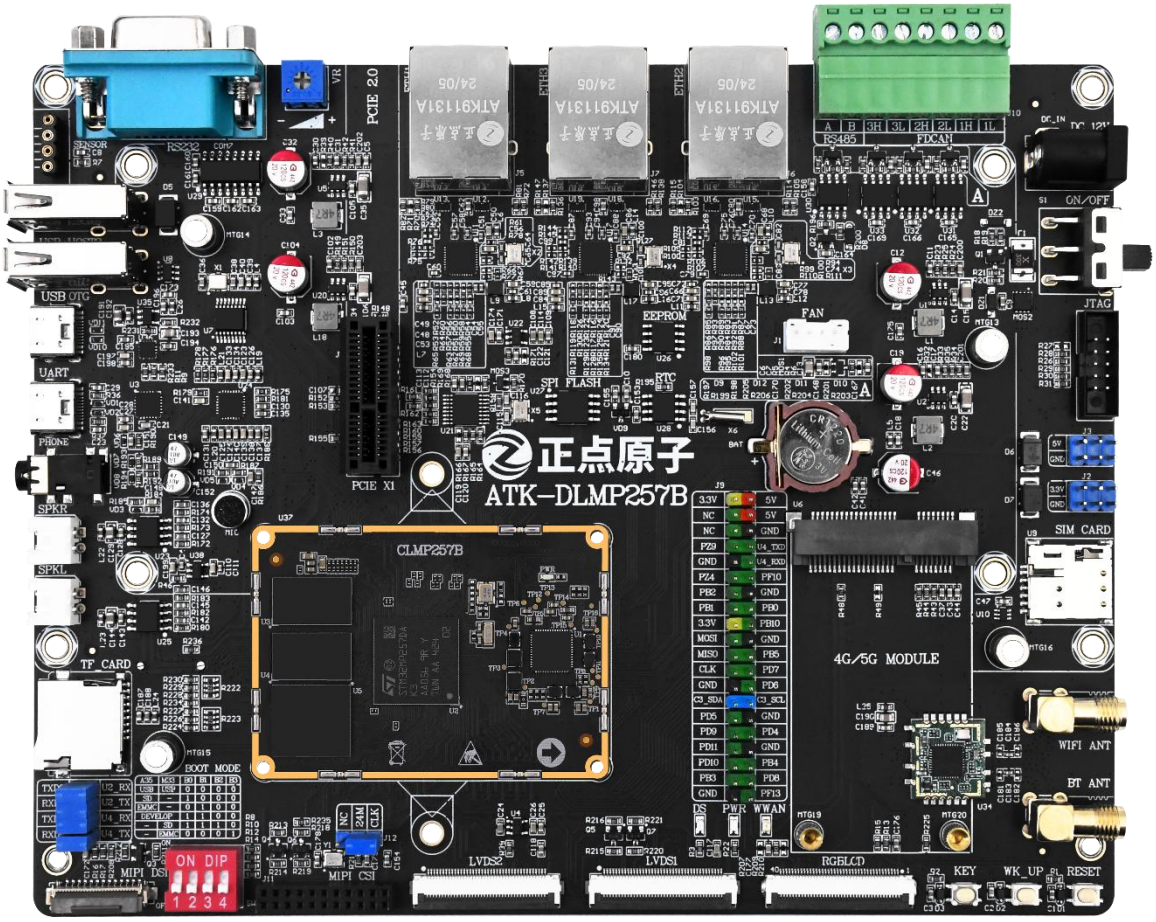
ATK-DLMP257B

Core board usage reference manual

V1.0



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Revision History:

Version	Version Update Notes	Responsible person	Proofreading	Date
V1.0	release officially	ALIENTEK	ALIENTEK	2025.04.01

Catalogue

Introduction

The main content of this document is based on the test results of the ATK-DLMP257B development board bottom board, applicable to B2B core board.

For peripherals for the core board, please refer to the ATK-CLMP257B Core Board Specification. At the same time, the pin reuse on the core board can be referred to the "[ALIENTEK] ATK-CLMP257B Core Board Interface Data Sheet V1.0".

These two PDF documents can be found in the directory structure of the development board CD-ROM: A- Basic Information \6_hardware \ 5_Mechanical_structure_of_core_board. These materials will help you under

Chapter 1. Minimum System Design

1.1 Power Supply Circuit

Three DCDC power chips (SCT2230, labeled U1, U2, U3) and one LDO chip (RT9013-18G, labeled U4) are integrated in the on-board power circuit of the ATK-DLMP257B development board. It is used to buck down the external 12V DC input power supply (DC_IN) and stabilize the output to 5V, 3.3V and 1.8V for the core board and other circuits. At the input end, C9, DZ1 (BZT52B10), R20, R21 and MOS2 together form a anti-reverse protection circuit, which can prevent damage to the development board due to power polarity connection. S1 is the main power switch of the development board, and F1 is the self-healing fuse, which is used to provide overcurrent protection to the input line.

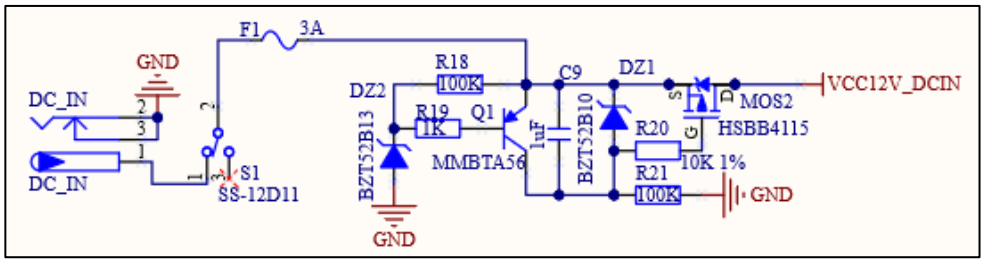


Figure 1 power input circuit

In addition, the development board also provides a 5V power supply (VCC5_USB) to the USB interface. If the R39 is empty solder, then the USB power supply will be independent of the system main power supply, thus reducing interference with the normal startup of the core board during USB plug-ins or load fluctuations.

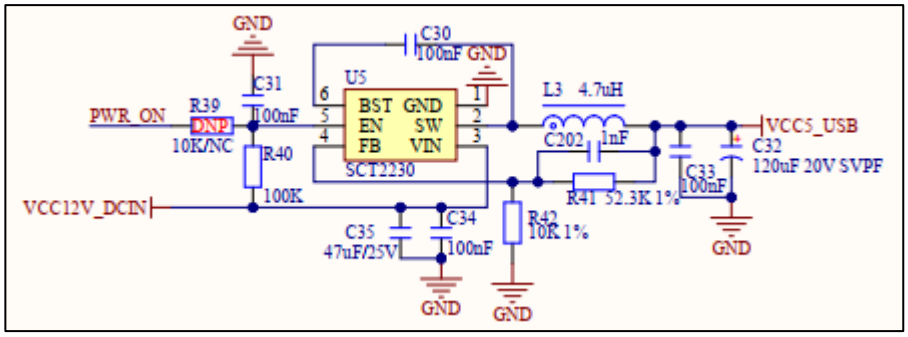


Figure 1.1-1 12V to 5V power supply circuit

The power on process is as follows: First, U1 converts the 12V input voltage to 5V (VCC5) to power the core board. Subsequently, U2 directly steps down the 12V input voltage to 3.3V (VCC3.3), and finally, U4 further steps down the 3.3V voltage to 1.8V (VCC1.8) through voltage regulation to power the LV module.

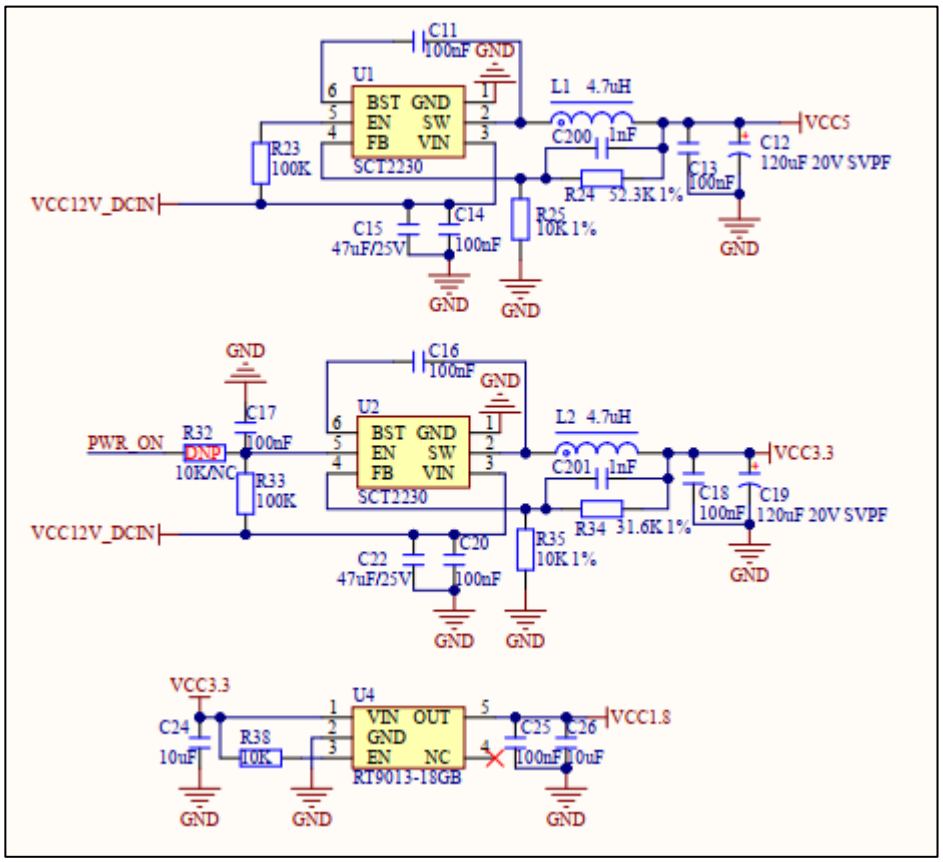
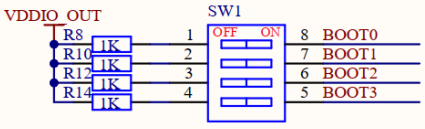


Figure 1.1-2 Power supply circuit

1.2 BOOT configuration circuit

The BOOT mode configuration circuit of ATK-DLMP135 development board is shown in FIG. 4.



BOOT3	BOOT2	BOOT1	BOOT0	A35	M33
0	0	0	0	UART/USB	UART/USB
0	0	0	1	SD-Card	—
0	0	1	0	EMMC	—
0	0	1	1	Development	Development
0	1	0	0	S-NOR	—
0	1	1	1	—	SD-Card
1	0	0	0	—	EMMC
1	0	1	1	—	S-NOR

notice:
0=OFF，0 is floating signal or grounded。
1=ON，1 is signal with pullup or tied to VCC3.3

Figure 4 BOOT boot mode configuration circuit

ATK-DLMP257 development board supports a variety of different startup mode options, you can set the dial switch to choose which mode you want to start from. When designing your own baseboard, it is recommended to keep the EMMC boot and UART/USB boot options so that you can use these common boot modes when needed.

Pay attention to the BOOT pin sequence number order, do not dial the reverse order.

When the core board STM32MP257 processor is in USB boot mode, it is in burn mode, and the system image can be re-burned. According to the software configuration, it can be selected to burn into the EMMC memory chip or SD card. When the processor is in EMMC boot mode, the processor will read the system image firmware stored in the EMMC chip to start operation. When the processor is in the SD card boot mode, the processor will read the system image firmware stored in the SD card to start

and run. When the core board processor is in Development start mode, the processor goes into debug mode.

In addition, as for the BOOT pin pull-up power, it is recommended to refer to this circuit and use the VDDIO_OUT power supply from the core board to power the BOOT pin instead of using other onboard 3.3V power supply. If the other onboard 3.3V power supply is too slow, the processor will fail to read the BOOT boot mode level. This results in the failure to start the system image.

1.3 Reset Circuit

A schematic of the reset circuit of the ATK-DLMP257 development board is shown in FIG. 5. The internal design of the core board uses a low level reset mechanism, so we also use a low level reset way when designing the bottom board circuit. In the schematic diagram, the element labeled "DNP" indicates that no welding is required, but that the pad is reserved for easy debugging.

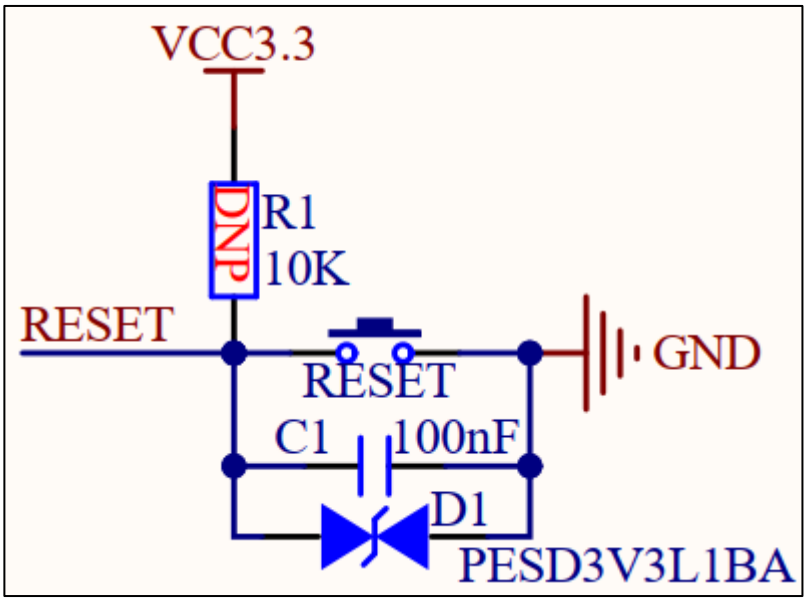


Figure 5 Reset Circuit

1.4 System firmware burning circuit

The ATK-DLMP257 development board uses USB3 of the core board as the USB OTG interface, and the system firmware burning circuit is shown in Figure 6.

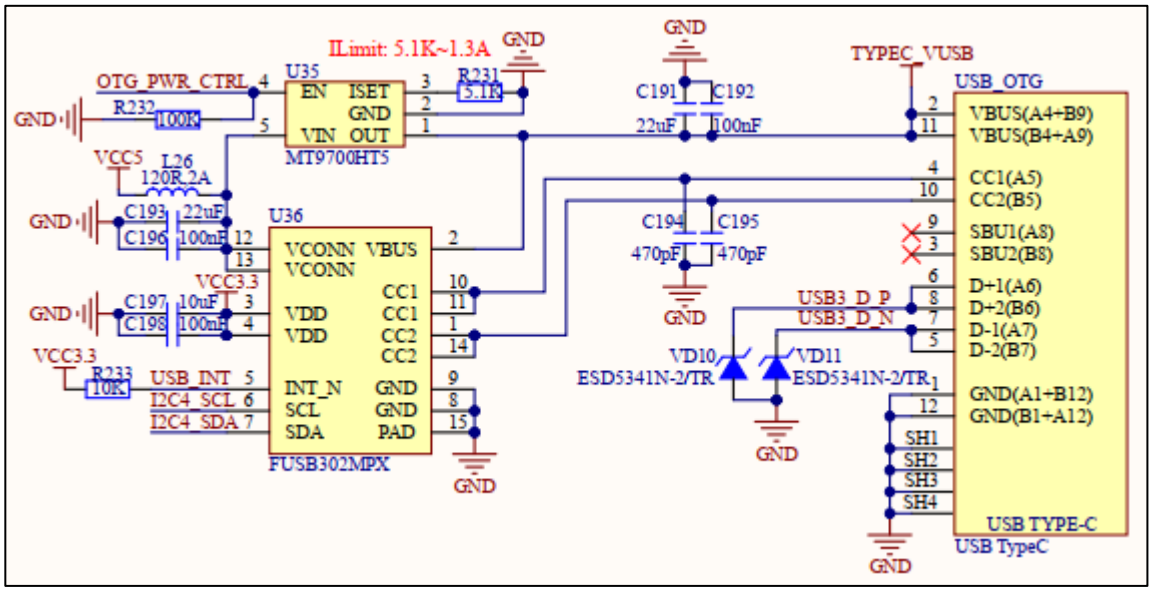


Figure 6 System firmware burn circuit

The USB_OTG circuit can be used both as a USB slave and as a USB host. On the right side of Figure 1.4.1 is the USB_OTG interface (Type-C block), through which system burning and USB OTG testing can be carried out.

USB OTG host Mode: When an external device is connected via USB Type-C, a Type-C OTG adapter is required. This is because the CC pin inside the OTG adapter contains a pull-down resistor that pulls the OTG_ID pin down and pushes the processor into host mode. At this point, the FUSB302MPX will pull the OTG_PWR_CTRL pin high, driving the MT9700HT5's OUT pin to output a 5V voltage, thereby providing 5V power to the external device through the TYPEC_VBUS.

USB OTG Slave mode: When the OTG_ID pin is high, it indicates that OTG is in slave mode. In this state, the FUSB302MPX will pull the OTG_PWR_CTRL pin low, causing the OUT pin of the MT9700HT5 to close, resulting in no voltage output of the TYPEC_VBUS.

1.5 Serial port debugging circuit

The on-board USB serial port on the ATK-DLMP257B development board and the serial port on the core board are realized by connecting to the JP4 socket, see Figure 7 for details.

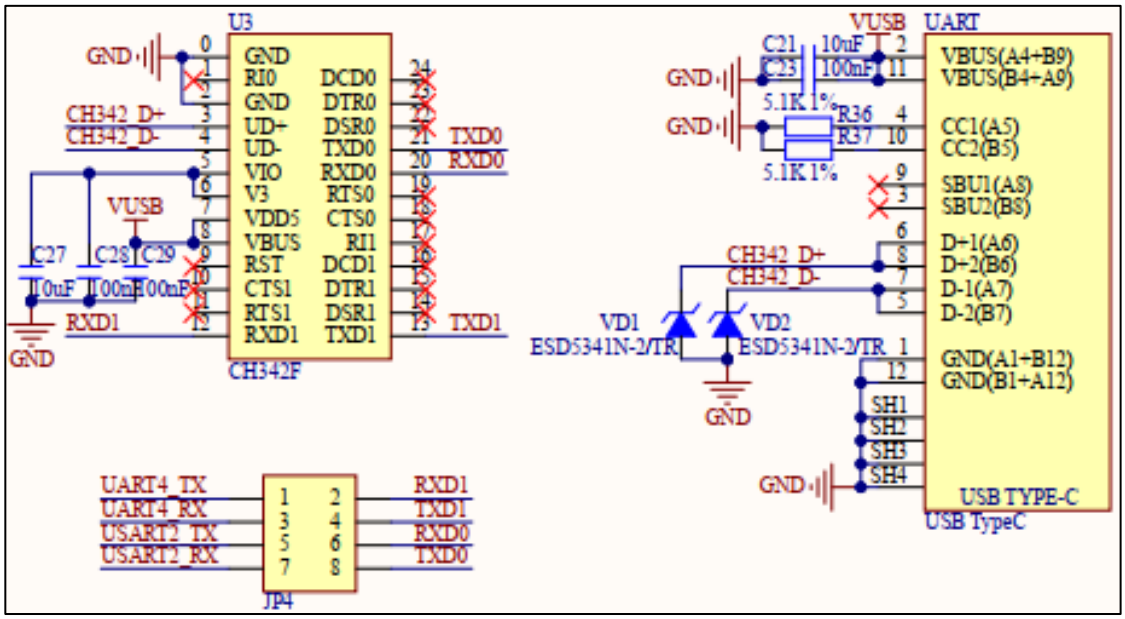


Figure 7 Serial port debugging circuit

The TXD and RXD in the figure are relative to the CH342F chip, which respectively represent the send and receive pins of the USB serial port. UART4_RX, UART4_TX, and USART2_RX, USART2_TX are pins relative to the core board. In the factory system, USART2 is used as the debug serial port of Cortex-M33 core, and UART4 is used as the debug serial port of Cortex-A35 core. By setting the jumper cap, the serial communication between the USB serial port and the core board can be realized.

When the SERIAL debugging assistant is used to connect the development board, the PC side will recognize and display two ports: Serial-A and Serial-B, which correspond to the debugging SERIAL ports of Cortex-A35 core and Cortex-M33 core, respectively, as shown in Figure 8 below.

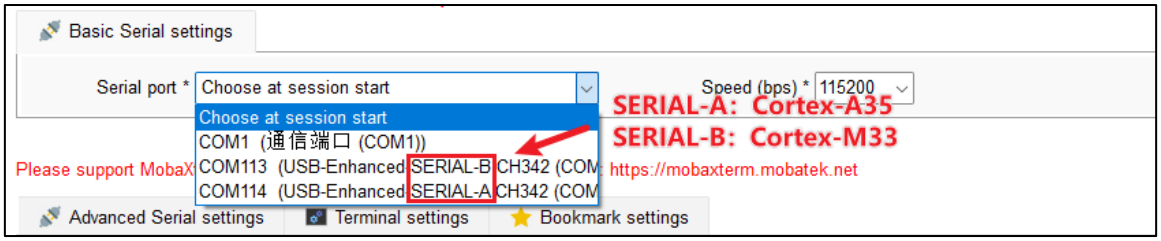


Figure 8 Instructions for connecting serial port

Chapter 2. Power supply voltage on the core board

If your self-designed baseboard does not start, you can check whether the supply voltage on the core board is normal. This method can better determine whether there is a problem with the core board itself or with the baseboard you designed.

2.1 Voltage at each test point of BTB core board

On the BTB core board, the test voltage content of each test point position has been marked next to the point position. You can refer to Table 1 for the voltage situation of each important test point of the core board under normal working condition. This will help you with troubleshooting and problem diagnosis.

Test item	Tests the point position	Voltage value
VDD_CPU	TP1	0.91V
VDD_EMMC	TP6	3.30V
VDD_DDR	TP8	1.20V
VDDA_1V8	TP5	1.80V

Table 1 Voltage at each test point of the core board

BTB core board each test point voltage