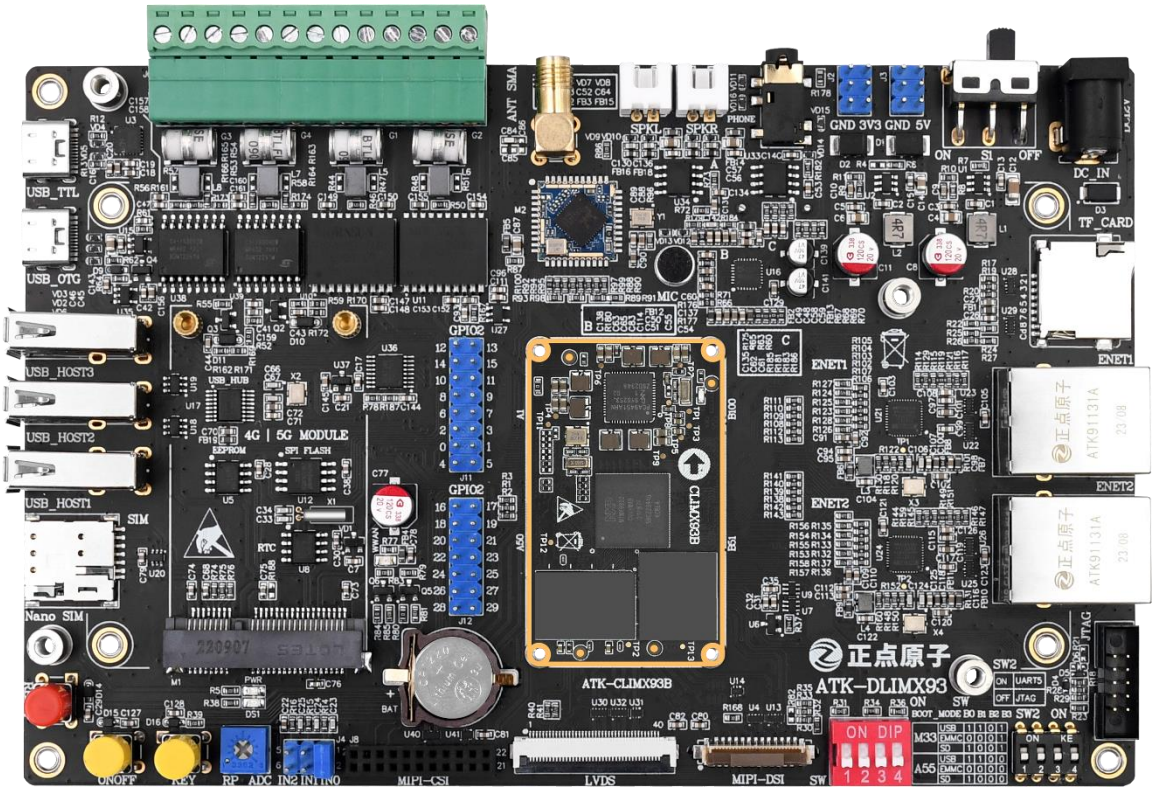
ATK-DLIMX93

Hardware Reference Manual

V1.0



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Version	Version Update Notes	Responsible person	Proofreading	Date
V1.0	release officially	ALIENTEK	ALIENTEK	2024.04.29

Catalogue

Chapter 1. Research on resources of ATK-DLIMX93 development board

At present, ALIENTEK has a number of STM32, I.MXRT, Linux and FPGA development boards. These development boards have consistently ranked first in Taobao sales, and have shipped more than 10W sets. This ATK-DLIMX93 development board is a development board that can run Linux system launched by ALIENTEK, using the form of base board + core board. Next, we introduce the resources of the bottom board and core board of the ATK-DLIMX93 development board, respectively.

1.1 ATK-DLIMX93 development board resources

First, let's take a look at the backplane resource diagram of the ATK-DLIMX93 development board, as shown below:

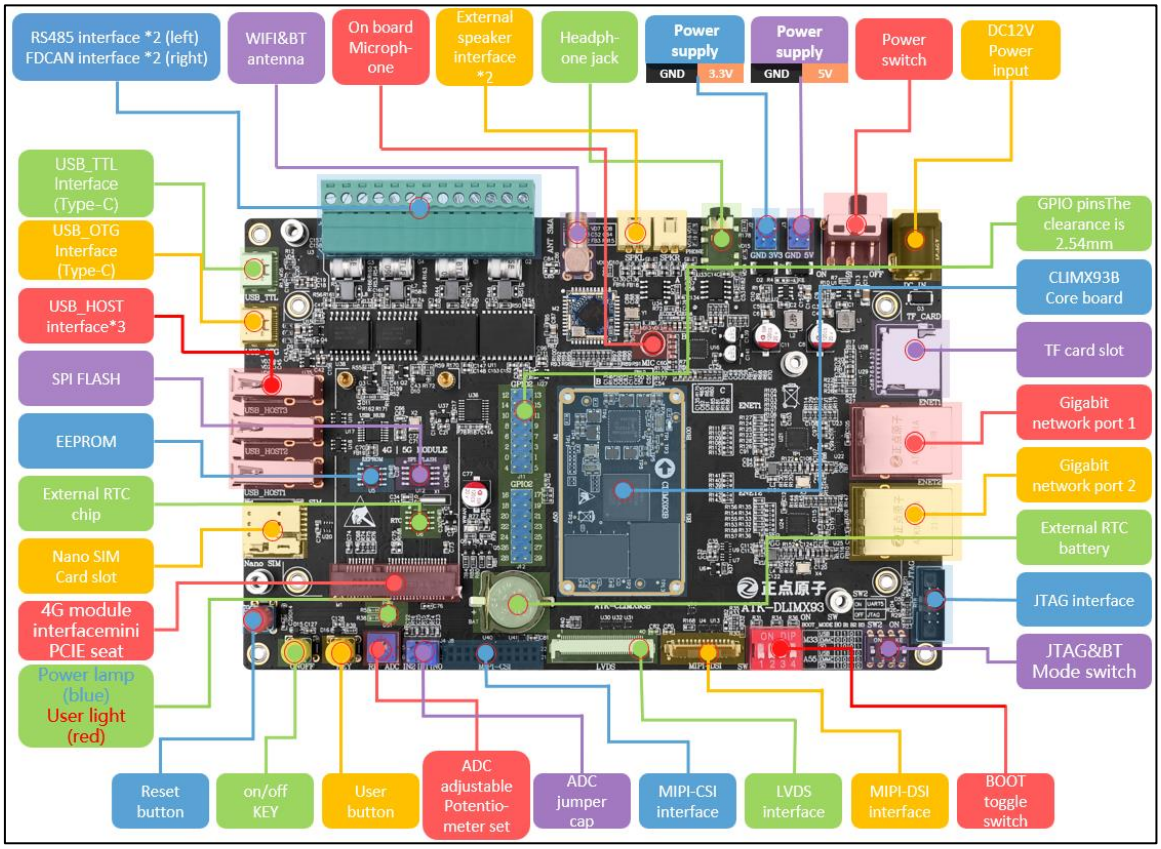


Figure 1.1-1 ATK-DLIMX93 development board resource diagram

As can be seen from the above figure, ATK-DLIMX93 development board is very rich in resources, expanded with a wealth of interfaces and functional modules. The external size of the development board is 170mm*110mm. The design of the board fully considers the humanized design, which is convenient for development and use.

The resources of the ATK-DLIMX93 development board are as follows:

- 1 set of core board connector interface, supporting ATK-CLIMX93B core board
- 1 blue power indicator
- 1 red status indicator

- 1 NOR FLASH chip, 16MB
- 1 EEPROM chip, 8KB
- 1 RTC clock chip
- 1 high performance audio codec chip, ES8388
- 1 way headphone interface, support 4-segment headphone
- 2-way speaker external interface
- 1 electret microphone MIC
- 1 small speaker (back of board)
- 1 WIFI&BT antenna interface
- 1 SDIO WIFI&BT module
- 2-way CAN-FD isolation interface
- 2-way RS485 isolation interface
- 1 USB_TTL debug serial port, Type-C interface Type
- 1 channel USB_OTG interface, Type-C interface Type
- 3-way USB2.0 HOST interface
- 1 Mini PCIE 4G/5G module interface
- 1 way Nano SIM card interface
- 1 adjustable potentiometer for ADC test
- 1 way ADC connection interface
- 1 RTC button battery holder with battery
- 1 channel MIPI-CSI camera interface
- 1 MIPI-DSI screen interface
- 1 LVDS screen interface
- 1 start mode dial switch
- 1 JTAG& Bluetooth serial port switch
- 1 way JTAG debug interface
- 2 10M/100M/1000M Ethernet interface (RJ45)
- 1 TF card interface
- 1 channel DC12V power input interface (recommended input voltage range: DC7~17V)
- 1 power switch, control the whole board power supply
- 1 set of 5V power supply outlet
- 1 set of 3.3V power supply outlet
- 1 reset button
- 1 switch button
- 1 user button
- 1 group of 2×8P 2.54mm spacing row needles, leading to 16 IO
- 1 set of 2×7P 2.54mm spacing row needles, eliciting 14 IO

The features of the ATK-DLIMX93 development board include:

1) Rich interfaces. The development board provides more than ten kinds of standard interfaces, which can conveniently carry out the experiment and development of various peripherals.

2) Flexible design. Adopting the form of core board + bottom board, many resources on the board can be flexibly configured to meet the use of different conditions. The core board brings out all the communication interfaces of i.MX93, including UART, I2C, SPI, CANFD, SDMMC, USB2.0, MIPI-

DSI, MIPI-CSI, LVDS, ADC, Gigabit Ethernet, etc., which is greatly convenient for everyone to expand and use.

3) Abundant resources. The onboard high-performance audio codec chip, gigabit network card, EEPROM memory chip and various interface chips meet a variety of application requirements.

4) Humanized design. Each interface is marked with screen printing, which is clear at a glance; Some commonly used peripherals are marked with large screen printing for easy search; The interface position is designed reasonably and easy to use.

1.2 ATK-CLIMX93B core board resources

Let's look at the ATK-CLIMX93B core board as shown below:

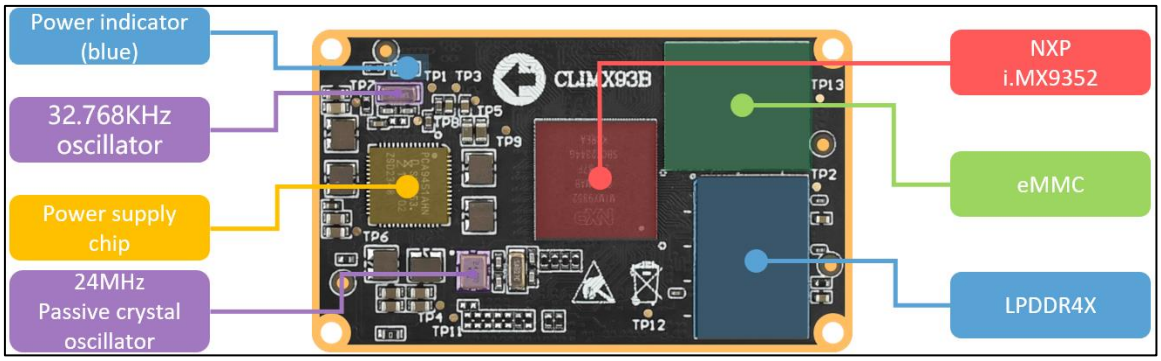


Figure 1.2-1 ATK-CLIMX93B core board

The overall size of the core board is 50mm*30mm, which is very small. It adopts 0.4mm pitch patch board to board connector, and the height of the bottom board BTB connector is 1.5mm, which can be easily applied to various projects.

The on-board resources for the ATK-CLIMX93B core board are as follows:

- CPU: MIMX9352CVVXMAB, dual-core Cortex-A55(1.7GHz), single-core Cortex-M33 (250MHz), FCBGA306 package, 11x11mm.
- Memory LPDDR4X: capacity 1GB (standard).
- Storage EMMC: capacity of 16GB (standard).
- High stability power management PMIC.
- Two 2*50 BTB connector male seats, a total of 200PIN.

Features of the ATK-CLIMX93B core board include:

1) Small size. The core board is only 50mm*30mm in size, easy to use to a variety of projects.

2) Convenient integration. The core board uses two 2*50P BTB connectors, which can be very easily integrated into the customer PCB, easy replacement, convenient maintenance and testing.

3) Abundant resources. LPDDR4X memory and EMMC memory on the core board can meet a variety of application requirements.

4) Stable performance. The core board adopts 8-layer board design, separate layer and power layer, all key signals are wired with equal length, and the layout of components is reasonable. In addition, NXP high stability power management chip PMIC is used to ensure long-term stable and reliable operation of the core board.

5) Humanized design. According to the function of the partition of IO port, convenient wiring.

Chapter 2. Detailed description of ATK-DLIMX93 development board hardware resources

The hardware resources of each part of the ATK-DLIMX93 development board are described in detail below, which is convenient for users to understand the hardware resources of the bottom board in detail, and they are introduced in counterclockwise order:

1. DC12V power input

There is an external power input port (DC_IN) on the development board, and a standard DC power outlet is used. The development board has a DC-DC chip onboard, which is used to provide an efficient and stable 5V power supply to the development board. Because of the DC-DC chip, the power supply range of the development board is very wide, you can easily find a suitable power supply (as long as the output range of DC 7~17V basically can be) to supply power to the development board.

2. Power switch

1 power switch (S1) is onboard the development board. The switch is used to control the power supply of the entire development board. This is a two-stage toggle switch, dial to the left to turn on the power of the development board, the whole board starts to power, and the power indicator light (PWR) is lit. Turn off the power supply of the development board by turning it to the right. The whole development board will be powered off, and the Power Supply Indicator (PWR) will be extinguished.

3. 5V power supply output

The development board has a set of 5V power output pins (2*3) (JP3), which are used to provide 5V power supply to the outside.

Users may be troubled by the lack of 5V power supply when experimenting. With this set of 5V rows, it is very convenient to have a simple 5V power supply.

4. 3.3V power supply output

The development board has a set of 3.3V power output pins (2*3) (JP2) onboard, which is used to provide 3.3V power supply to the outside.

Similarly, while users may be frustrated by the lack of a 3.3V power supply, it is convenient to have a simple 3.3V power supply (maximum current cannot exceed 1000mA) with this 3.3V pin set.

5. Headphone port

The development board has 1 headphone port onboard. The specification of the headphone holder is PJ-342 single pillar band T. The interface can plug in 4 segments of 3.5mm headphone to support recording and playback. When playing, support headphones hot plug; When recording, both headset recording and on-board microphone MIC are supported for recording.

6. Speaker external interface

There are two external speaker interfaces on the development board. One speaker interface SPKR has been connected to a small speaker on the development board to facilitate users to conduct audio playback tests.

7. Speakers (on the back)

An external speaker is mounted on the back of the development board, the speaker model is GSPK2307P-8R1W, and the power is 8Ω and 1W for the user to conduct audio playback test. When the audio chip ES8388 plays audio, the development board supports playing from the speaker and headphones. When the headset is not inserted, the development board automatically plays from the

external speaker; When the headset is inserted, it will automatically switch to the headset to play audio, at which point the speaker will automatically stop playing. The design is consistent with the user's regular use experience.

8. Electret microphone MIC

The development board has an electret microphone, the Recording input port (MIC), which can be used to realize the recording function.

9. SDIO WIFI&BT module

There is a WIFI& Bluetooth module on the development board, which is a SDIO interface and connected to the SD3 interface of i.MX93. The chip used in this module is REALTEK's RTL8723DS, which is a WIFI4+ Bluetooth 4.2 integrated chip, and the WIFI wireless band is 2.4G. WIFI and Bluetooth share a 2.4G antenna, which saves board subspace and facilitates PCB layout and routing.

10. WIFI& Bluetooth antenna

There is a WIFI and Bluetooth antenna interface on the development board, and WIFI and Bluetooth share a 2.4G antenna.

11. FDCAN interface

Development board onboard 2-way FDCAN bus interface (support CAN and CAN-FD), with digital isolation, power isolation, multiple protection. It is connected through 2 ports and external CAN bus, namely CANH and CANL. When CAN is communicating, CANH must be connected to CANH and CANL to CANL, otherwise the communication is not normal.

12. RS485 interface

Development board onboard 2 RS485 bus interface (RS485), with digital isolation, power isolation, multiple protection. It is connected to external RS485 devices through 2 ports. When RS485 communication, must A connect A, B connect B.

13. USB_TTL debugging serial port

The 1 channel USB_TTL debugging serial port on the development board is a USB Type-C interface, which is used to connect the USB to the CH342F chip, so as to realize the function of 1 channel USB to 2 channels serial port, which is used as the system debugging serial port.

14. USB_OTG interface

One USB OTG interface on the development board is USB2.0 Type-C interface. This interface is connected to USB1 bus of i.MX93 processor, which is used to realize OTG function. The development board can be connected to the computer using USB Type-C cable, and the development board acts as a Slave for system burning. You can also use USB OTG cable to connect other USB devices, such as U disk, etc., at this time the development board as the Host.

15. USB HOST interface

The processor i.MX93 has two USB ports. The development board of ALIENTEK ATK-DLIMX93 extends the USB2 of i.MX93 into four USB hosts through the USB HUB chip, one of which is used to connect the 4G/5G module, and the other three are used as USB hosts. Users can connect USB mouse, USB keyboard, U disk and other devices through these three USB HOST interfaces.

16. Mini PCIE 4G/5G interface

There is a Mini PCIE seat on the development board, which is essentially USB protocol and connected to the HUB chip of USB2. This interface can be connected to 4G or 5G modules, such as Gaoxin iot ME3630 4G module, Quectel EC20 4G module, FIBC 5G RedCap FG132 module.

17. Nano SIM card interface

The development board has a Nano SIM card interface onboard, and if 4G/5G modules are needed for wireless data transmission, the Nano SIM card needs to be inserted into this interface.

18. EEPROM

There is an EEPROM memory chip on the development board, the model is AT24C64, the capacity is 8KB, and the IIC interface is used for user storage test.

19. SPI FLASH

There is an SPI NOR FLASH memory chip on the development board, the model is W25Q128, the capacity is 16MB, and the SPI interface is used for user storage test.

20. RTC real-time clock

The development board has 1 RTC real-time clock chip and IIC interface. i.MX93 processor also has a RTC peripheral, but the precision is not high, so the development board has an RTC chip outside for users to test.

21. RTC button battery holder

There is a RTC button battery holder on the development board, which is used to power the RTC real-time clock chip, and can maintain the timing of the RTC clock chip after the power off of the development board.

22. Reset button

The development board is equipped with a RESET button (RESET) for resetting the core board.

23. Switch machine button

There is an on-off button (ONOFF) on the development board. Press the ONOFF button for 5 seconds after the i.MX93 processor is powered on, the processor will enter the shutdown state, and the core board will power off. At this time, press the ONOFF button for 0.5 seconds, and the processor will enter the power on state, and the core board will be powered on again.

24. The user presses the key

There is one input KEY on the development board, which can be used as an ordinary key input by the user.

25. Red status indicator

There is a red status indicator LED on the development board. Users can use this LED to indicate the running status of the processor. When debugging code, using LED lights to indicate the state of the program is a very good debugging aid.

26. Blue power indicator

There is a blue power indicator LED light on the development board. When the 5V power supply of the development board is normal, this light will always be on. If the lamp is not bright, it means that there is a problem with the power supply of the development board (excluding the damage of the LED lamp itself).

27. Adjustable potentiometer

An adjustable potentiometer with 10K resistance on the development board is connected to three ADC pins of i.MX93, which can be used to test ADC voltage acquisition.

28. ADC connection interface

The processor i.MX93 has four special ADC pins, three of which are used to connect the adjustable potentiometer of the development board, and the other one ADC is used for ID identification of the MIPI-DSI LCD screen. When using the adjustable potentiometer, it is necessary to connect the jumper cap to connect the ADC pin to the adjustable potentiometer.

29. MIPI-CSI camera module interface

A MIPI-CSI camera module interface is mounted on the development board, which is used to test i.MX93 image processing and collect images for NPU processor for AI model operation processing. The interface supports the ALIENTEK ATK-MC5645 camera module (OV5645), which can be inserted into this interface, and the lens direction is to the outside.

30. LVDS interface

The development board has a 4-lane LVDS screen interface, which can be connected to the 10.1 inch 1280x800 LVDS capacitive touch screen of ALIENTEK.

31. MIPI-DSI interface

There is a 4-lane MIPI-DSI screen interface on the development board, which can connect the 5.5 inch 720x1280 MIPI capacitive touch screen, 5.5 inch 1080x1920 MIPI capacitive touch screen and 10.1 inch 800x1280 MIPI capacitive touch screen of ALIENTEK.

32. Start mode dial switch

There is a 4x2P red dial switch on the development board to select the processor startup mode, which supports the startup mode from SD card, EMMC and USB. The corresponding dial switch togulation configuration of the startup mode has been marked on the screen print of the development board. Users need to set the dial switch according to their actual needs when using. It should be noted that the processor i.MX93 is a heterocore processor, which supports running Cortex-A55 core and Cortex-M33 core. If you are running Linux system, you only need to set the A55 core boot mode to boot.

33. JTAG& Bluetooth serial port switch

There is a JTAG& Bluetooth serial port switch on the development board, which is used to switch JTAG signal and Bluetooth serial port signal. Because the JTAG pins of i.MX93 processor can be reused into UART5 functions, the development board designs the pins of both of them together, and they cannot be used at the same time, so external switching is needed. The development board connects the JTAG pin of the processor to the JTAG interface by default. When users need to use the Bluetooth function, they need to connect the JTAG pin of the processor to the Bluetooth serial port UART5, and then they need to toggle the switch.

34. JTAG interface

This is a 10P, 2.0mm pitch JTAG interface to connect to the JTAG emulation debugger, typically used to debug Cortex-M33 cores.

35. Gigabit Ethernet interface

The development board has two Gigabit Ethernet interfaces (RJ45), i.MX93 contains two Gigabit Ethernet MAC peripherals, supporting 10M/100M/1000M speed.

36. TF card interface

There is a standard TF card interface (TF_CARD) on the development board, which uses a small TF card interface and is driven by SDIO mode. With this TF card interface, mass data storage requirements can be met.

37. Lead out the IO port

The IO outlet ports J11 and J12 of the development board are adopted 2X8P and 2X7P needle rows respectively, and a total of 30 IO ports are elicited. It should be noted that the IO port is not used independently, and most of them are shared with the pins of the functional circuit on the board. Therefore, when using these IO, users need to check whether there is a conflict with the onboard

function circuit, such as whether there is a pull-up resistance, whether the IO has been connected to other function chips, etc., which will lead to the wrong IO level value and communication failure of external modules. If it is affected, it is necessary to temporarily remove the on-board circuit and chip of the development board.

38. ATK-CLIMX93B core board interface

This is the core board interface above the bottom board of the development board, consisting of two 2*50, 0.4mm spacing of the patch board to board connection seat female seat, a total of 200PIN. It can be used to insert the ATK-CLIMX93B core board, so as to develop and verify the i.MX93 processor.

Chapter 3. ATK-DLIMX93 development board schematic details

The circuit design of each part of the schematic diagram of the bottom board of the development board is explained below for user reference.

It is specially noted here that the hardware circuit of the development board may be updated, optimized and version iterated. If users refer to this circuit for product project development, it is necessary to evaluate whether it meets the project requirements, and perform circuit optimization and protection.

3.1 Core board interface

The development board adopts the form of bottom board + core board. The bottom board of the development board uses 2 2*50 board-to-board connectors to connect with the core board, which is very convenient. The core board interface above the bottom board is defined as shown below:

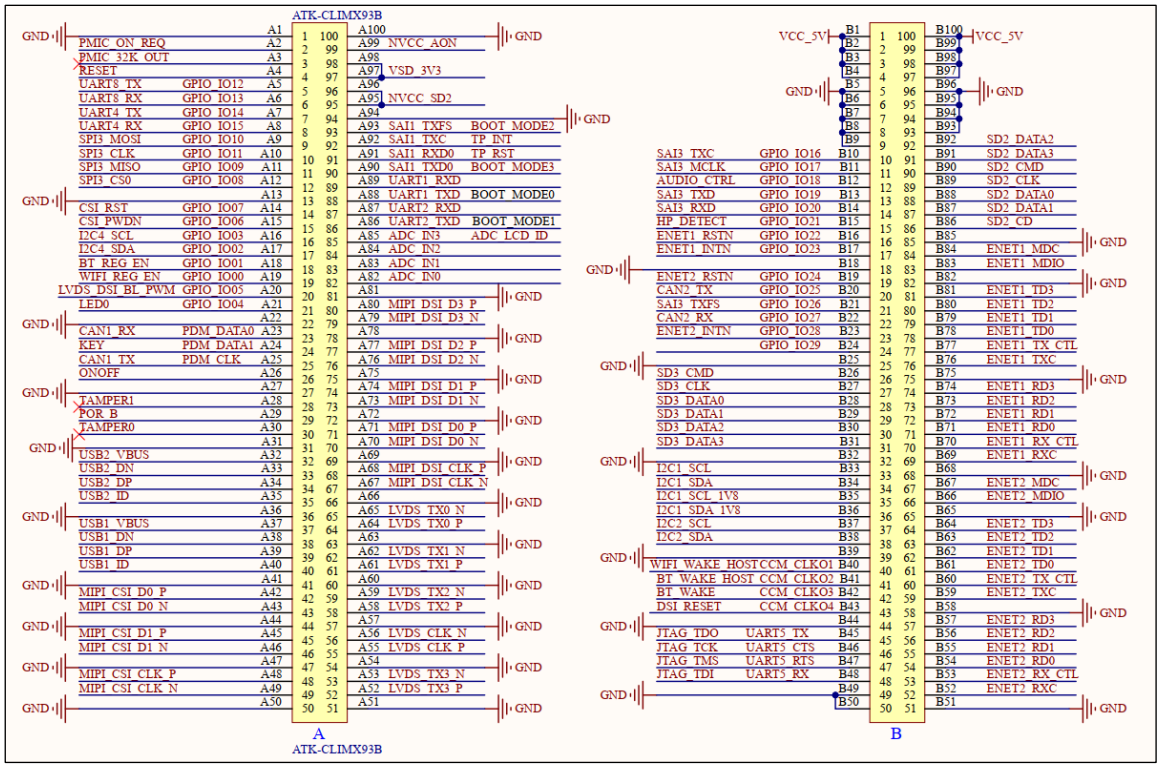


Figure 3.1-1 Base plate docking core plate connection seat definition

A and B in the figure are the connector interface on the base plate, which is composed of two 2*50PIN board-to-board female seats, containing 137 GPIO, 4 other functional pins, 46 GND pins and 13 power pins, forming 200PIN.

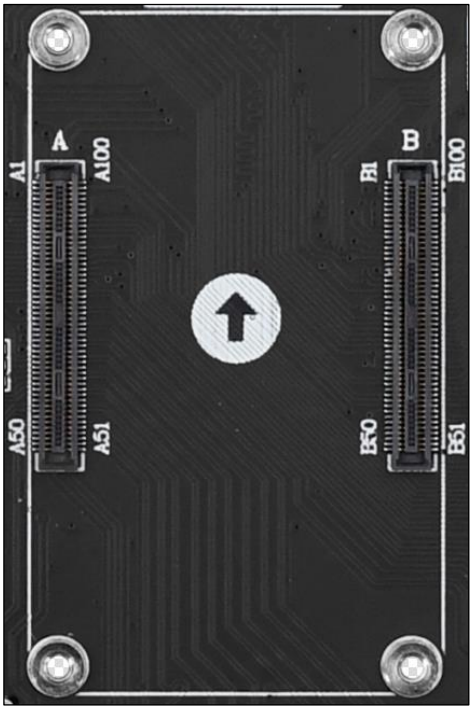


Figure 3.1-2 Physical drawing of base plate adapter interface

When designing the base plate, the user should pay attention to the definition order of the connection seat, and do not connect the opposite direction. For example, pins B1~B4 and B97~B100 in the schematic diagram are eight VCC_5V power input pins that supply the core board; B5 to B9 and B93 to B96 are nine GND pins, and the other pins are the same. The bottom plate has anti-insertion design. When the core board is inserted, the user should pay attention to the direction of the arrow mark in the bottom plate diagram and the direction of the arrow mark of the core board, so as to plug in successfully. In addition, it cannot be removed too forcefully, otherwise it may damage the connection seat.

3.2 DC power supply

The schematic diagram of the on-board power supply part of the development board is as follows:

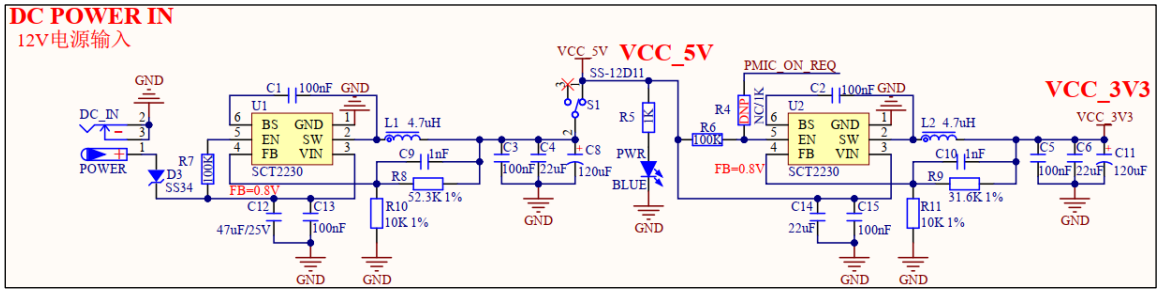


Figure 3.2-1 DC IN power supply

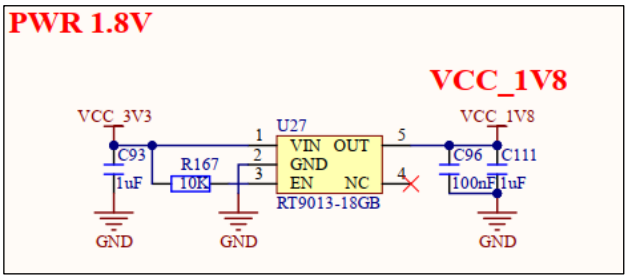


Figure 3.2-2 1.8V power supply

All functional circuits of the development board need 5V, 3.3V and 1.8V power supply. There are totally 2 DCDC power chips in the figure, namely U1 and U2. DC_IN socket is used for external DC12V DC power input, D3 is anti-reverse diode, avoid external DC power polarity is wrong to burn the development board. The DC power supply is converted into 5V power output through the U1 DCDC chip to supply power to the core board and other circuits. S1 is the main power switch of the development board. When the 5V power supply is normal, the blue power indicator light of the development board will light up. U2 is an output 3.3V DCDC chip that provides 3.3V power to the development board.

As a reminder, there are two designs of EN control pin of U2. (1) direct enable control by 5V series 100K resistor; (2) It is controlled by PMIC_ON_REQ pin of the core board, which pulls down 100K resistor on the core board by default. When the processor of the core board is powered on normally, PMIC_ON_REQ pin will automatically pull up to 1.8V (not 3.3V), so as to enable U2 power output of the bottom board. If the user shuts down the processor i.MX93, for example, after long pressing the button ONOFF for 5 seconds, the processor enters the shutdown state, the PMIC_ON_REQ pin will be automatically pulled down to 0V, and the power supply of U2 will be cut off. These two design methods can normally enable the DCDC U2 to output 3.3V, and the design method can be selected on demand.

U27 is an LDO chip with 1.8V power output, which is used to power some peripheral devices that need 1.8V power supply such as ADC and WIFI.

3.3 Power output interface

Development board onboard two sets of power output interface, schematic diagram as shown below:

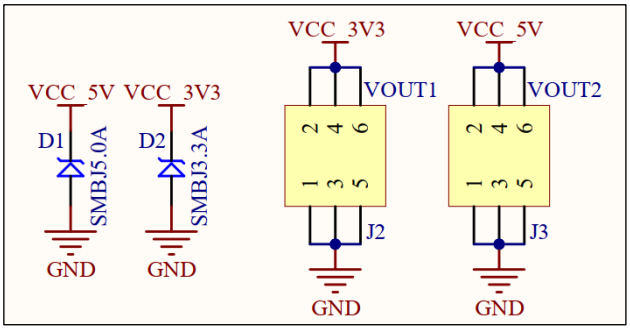


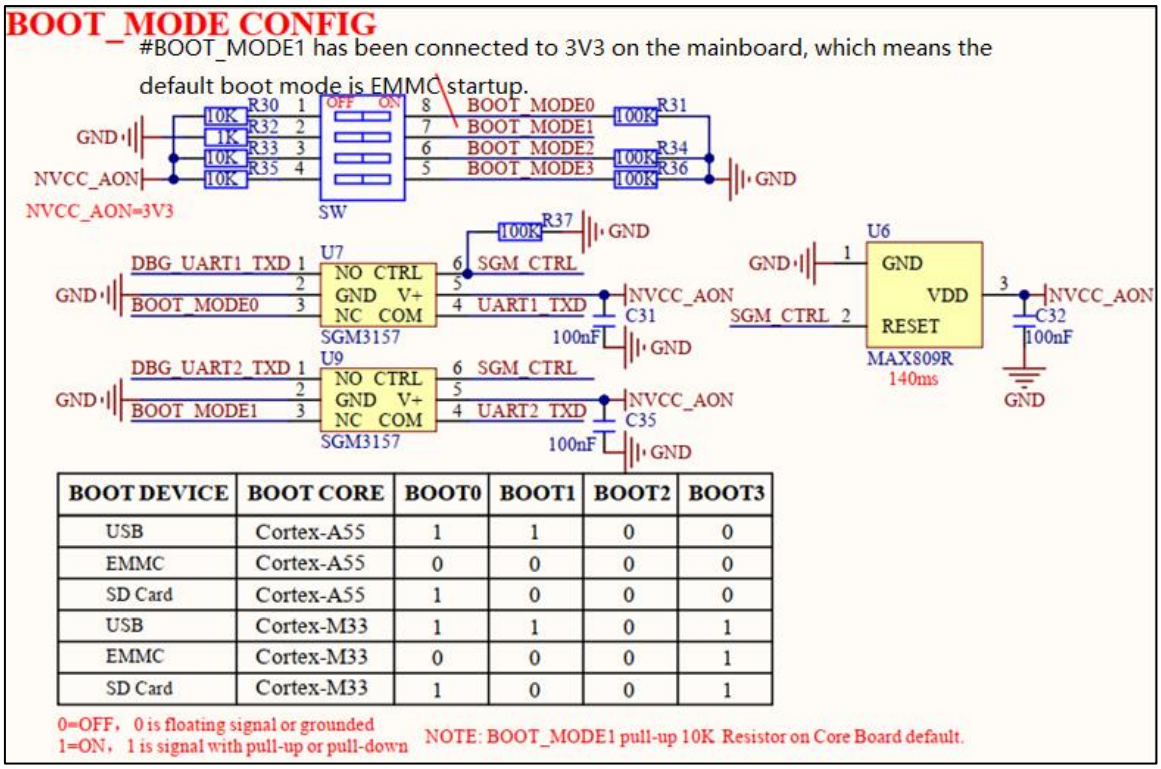
Figure 3.3-1 Power output interface

In the figure, VOUT1 and VOUT2 are 3.3V and 5V power output interfaces respectively, which can provide 3.3V and 5V power to the outside through the development board, so as to facilitate the user's expansion. In the figure, D1 and D2 are TVS tubes, which can effectively avoid damage to the development board when the external power supply/load of VOUT is unstable (especially when the

development board is connected with external inductive loads such as motor/relay/solenoid valve). At the same time, it can also prevent the external power supply from being reversed and damage to the development board to a certain extent.

3.4 Start mode setup interface

ATK-DLIMX93 development board BOOT mode setting interface circuit, the schematic diagram is as follows:



BOOT DEVICE	BOOT CORE	BOOT0	BOOT1	BOOT2	BOOT3
USB	Cortex-A55	1	1	0	0
EMMC	Cortex-A55	0	0	0	0
SD Card	Cortex-A55	1	0	0	0
USB	Cortex-M33	1	1	0	1
EMMC	Cortex-M33	0	0	0	1
SD Card	Cortex-M33	1	0	0	1

Figure 3.4-1 Start mode setup interface

The development board supports starting from a variety of different devices, and you can choose to start from the specified device by setting the dial switch. The core board selects the A55 core EMMC startup mode by default, so the base board supports the following configurations:

Startup mode setting Table 3.4.1

BOOT0	BOOT1	BOOT2	BOOT3	Boot core	Startup mode
1	1	0	0	Cortex-A55	USB startup
0	0	0	0		EMMC startup
1	0	0	0		SD Card startup
1	1	0	1	Cortex-M33	USB startup
0	0	0	1		EMMC startup
1	0	0	1		SD Card startup

The processor i.MX93 is responsible for the configuration of the boot mode by four pins: UART1_TXD (BOOT_MODE0), UART2_TXD (BOOT_MODE1), SAI1_TXFS (BOOT_MODE2), SAI1_TXD0 (BOOT_MODE3). Because the pins UART1_TXD and UART2_TXD involve two functions of system debugging serial port and startup mode, which are in conflict, the analog switch

SGM3157 and reset chip MAX809R are used for time-sharing multiplexing design. After the core board is powered on normally, the NVCC_AON power supply will output 3.3V for SGM3157 and MAX809R. The RESET pin of the MAX809R will then output a high level (the default is low) after a delay of at least 140ms to control the connection channel of the analog switch SGM3157. This feature enables SGM3157 analog switch to connect BOOT_MODE0 with UART1_TXD and BOOT_MODE1 with UART2_TXD at the beginning of power on to realize the setting of boot mode. After 140ms, it will automatically switch and connect to the respective debug serial port pins DBG_UART1_TXD and DBG_UART2_TXD, so as to realize the startup mode and debugging serial port do not affect their respective functions.

3.5 USB_TTL debug serial port (system debugging)

There is a USB_TTL debugging serial port on the development board, Type-C interface Type, the schematic diagram is shown as follows:

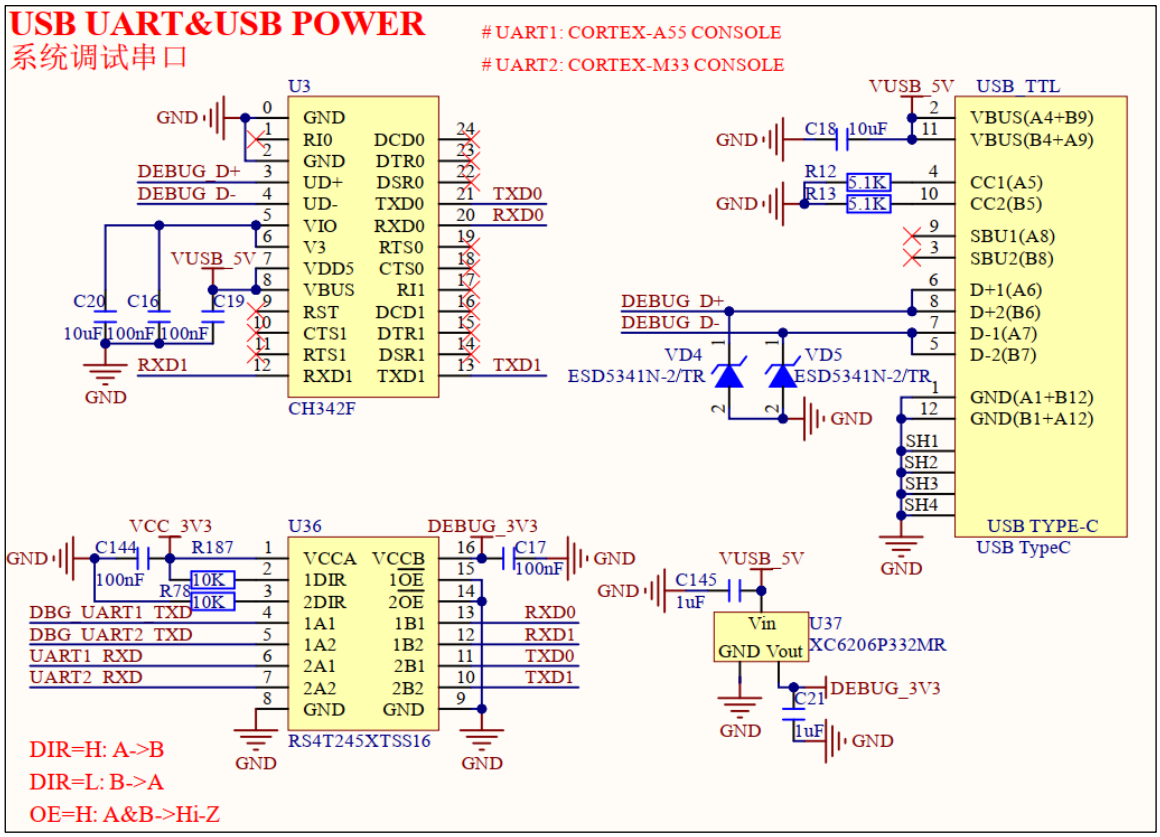


Figure 3.5-1 USB_TTL debug serial port

The processor i.MX93 is a multi-core heterocore processor, including dual-core Cortex-A55 and single-core Cortex-M33, both of which can run independently, so there are two system debugging serial ports: UART1 (debugging A55 core) and UART2 (debugging M33 core). The development board adopts one USB to two TTL serial port scheme, and selects Qinheng CH342F chip to realize communication interface conversion. In the figure, U3 is the CH342F chip, which is independently powered by USB cable. When the USB_TTL interface of the development board is connected to the USB cable, it can directly supply 5V power to the CH342F chip. It should be noted that when the DC12V power supply of the development board is not supplied but the USB cable is still supplied to

the CH342F, the TX pin of the CH342F chip will fill the core board with current by default. Therefore, the RS4T245XTSS16 level conversion chip used in this circuit can act as an isolation chip to prevent IO current filling. The U37 is an LDO chip that uses a USB cable to supply 3.3V power to one side of the RS4T245XTSS16, while the other side of the converter chip is powered by converting 3.3V from a DCDC 5V DC power supply.

3.6 USB_OTG interface (system burn)

The i.MX93 processor supports firmware burning from USB boot mode. There is a USB_OTG interface on the development board, which can not only burn the system firmware, but also access the USB HOST device through the USB OTG cable. This is shown in the figure below.

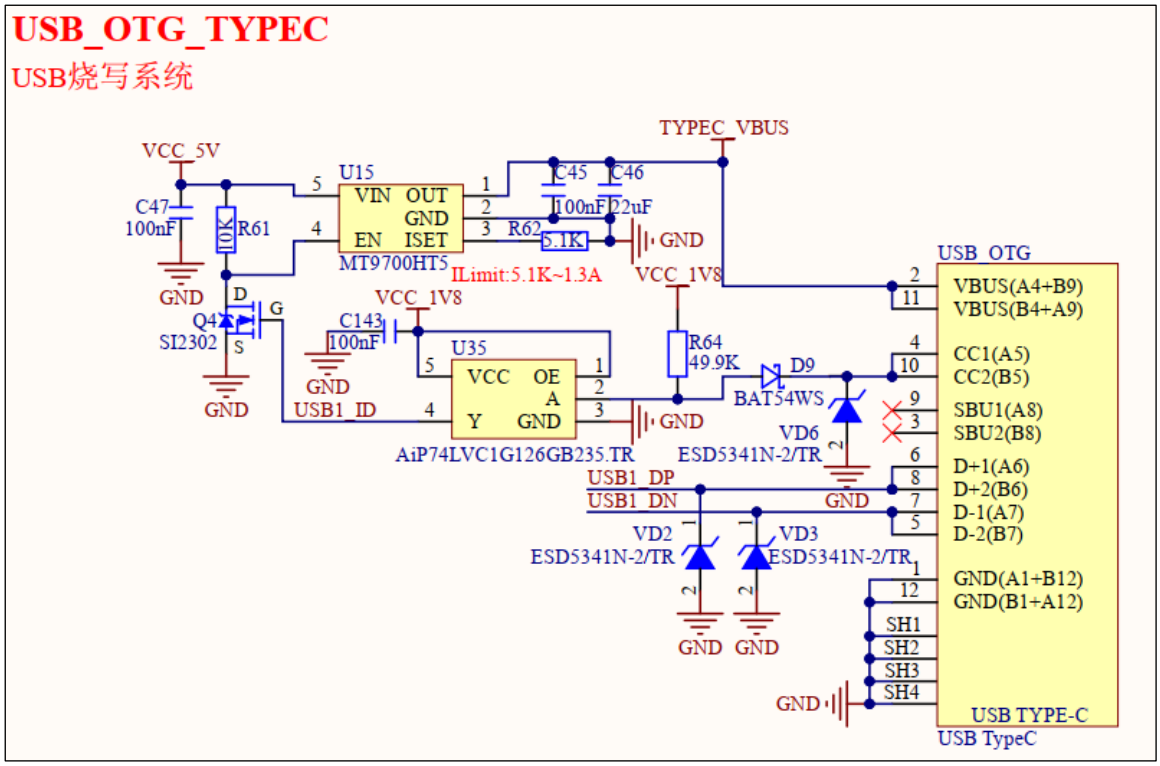


Figure 3.6-1 USB_OTG interface

The USB_OTG circuit can be used as both a USB DEVICE and a USB HOST. The USB_OTG interface on the right of the figure is a USB Type-C block, through which system firmware can be burned and USB OTG test can be carried out. You will also need to purchase a Type-C OTG cable if you need to do USB OTG testing.

The USB1_ID pin in the figure is used to determine the USB master-slave mode of the processor i.MX93. When the USB1_ID pin is high, the processor i.MX93 acts as a USB slave. When USB1_ID pin is low, processor i.MX93 acts as USB host. This circuit indirectly pulls USB1_ID up to 1.8V by default through USB1 bus, which can make the processor i.MX93 enter the USB slave mode, which is used to connect to the PC for system firmware burning. In order to support the USB host mode, a buffer device is added here. When the USB Type-C block is connected to the external OTG adapter and the U disk is connected, the USB1_ID pin level can be pulled down to near 0V, so that the processor enters the USB host mode, and at the same time, the MT9700HT5 power chip provides 5V external power supply. If the user designs the USB interface of the base board without using USB OTG function, that

is, the processor is only used as a USB slave for burning the system, then the buffer and MT9700HT5 power supply can be not added, the USB1_ID can be directly pulled up to 1.8V, and the USB1_VBUS power pin also needs to supply 3.3V.

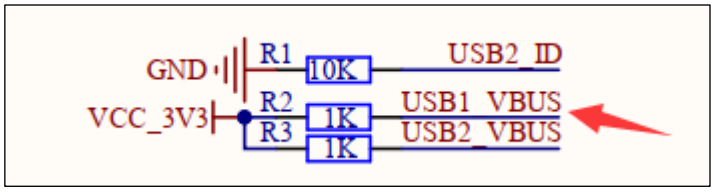


Figure 3.6-2 USB1_VBUS power supply

3.7 The JTAG interface

A 10-pin, 2.0mm pitch JTAG interface is mounted on the development board. The schematic diagram is shown as follows:

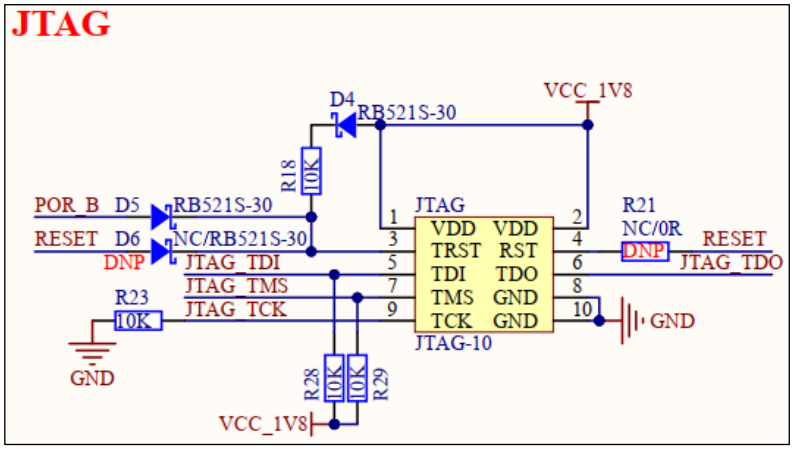


Figure 3.7-1 JTAG interface

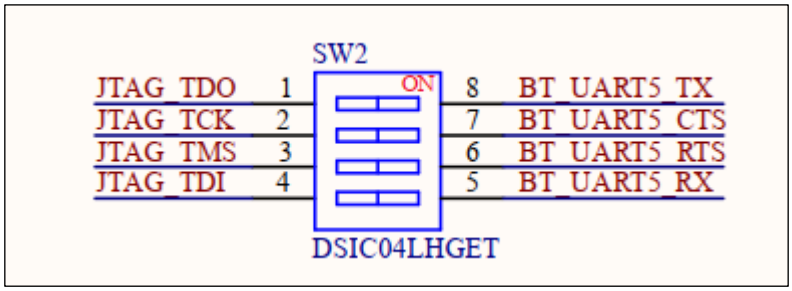


Figure 3.7-2 JTAG and Bluetooth serial port switch

This JTAG interface can be used to debug Cortex-M33 applications. The user selects Cortex-M33 USB mode to start, and can debug the M33 core through the JTAG interface.

Because the JTAG pin of processor i.MX93 can be reused into UART5 serial port function (the IO level is 1.8V), the development board adopts the design of shared pins, note that the two cannot be used at the same time, and it needs to be manually switched by SW2 dial switch. By default, the development board connects four pins JTAG_TDO, JTAG_TCK, JTAG_TMS, and JTAG_TDI to the JTAG holder for M33 debugging purposes. When the user wants to use the Bluetooth function, he needs to dial the SW2 dial switch to connect all the pins to BT_UART5, which can be used as the Bluetooth serial port function when the Cortex-A55 runs the Linux system.

3.8 Leading IO port

The development board leads to 30 IO ports through two needle rows of 2X8P and 2X7P. The schematic diagram is shown as follows:

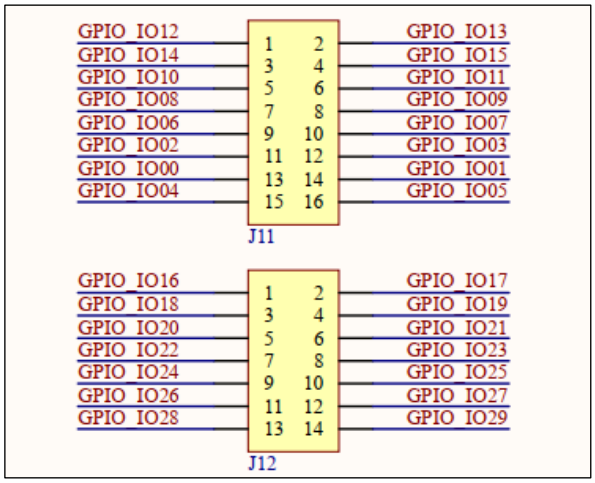


Figure 3.8-1 Leading IO port

According to the wiring convenience of the bottom plate device, it is divided into two needle arrangement groups. These IO ports correspond to the GPIO2 port of i.MX93 processor. Users can use this IO to connect to other modules and do more interesting innovations. Here is a special note, the lead IO port is not used independently, almost all with the development board onboard functional circuit pins shared. Therefore, when using these IO, users need to check the hardware configuration of the bottom board functional circuit for these IO, such as resistance pulling up and down, parallel capacitor, etc., if it affects the use, it needs to be removed manually. When using the specified IO alone, it cannot conflict with the development board function and can not be used at the same time. It needs to change the system reuse function.

3.9 Audio interface

The ES8388 high-performance audio codec chip on the development board can realize audio playback and recording functions. The schematic diagram is as follows:

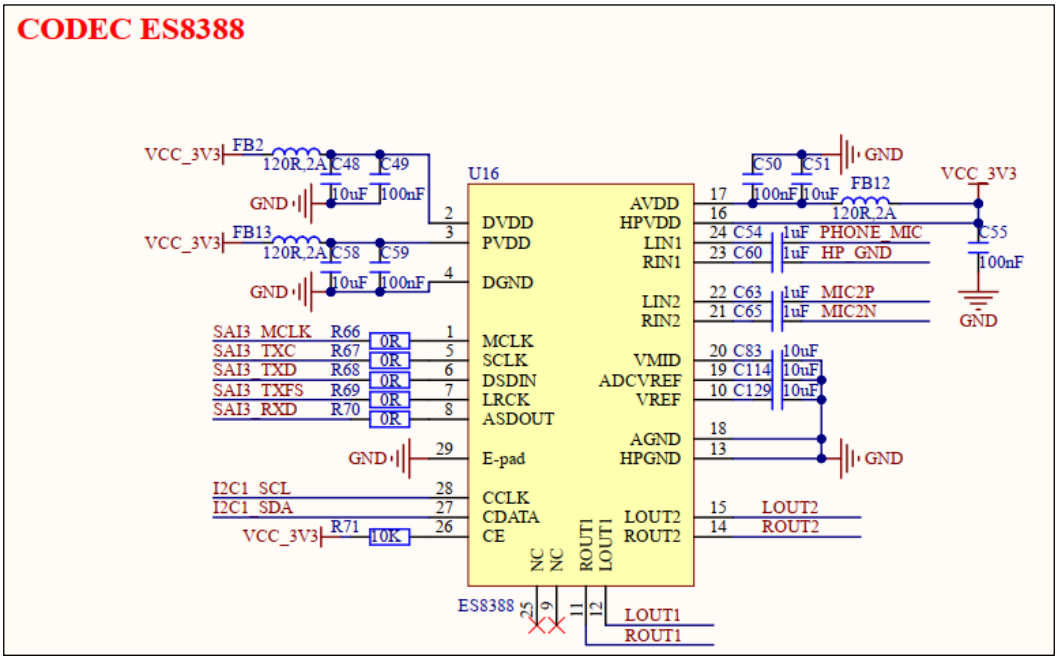


Figure 3.9-1 ES8388 audio codec chip

ES8388 is a stereo audio codec with high performance, low power consumption and low cost. The chip integrates 24 bit high performance ADC and DAC. It is composed of dual-channel ADC, dual-channel DAC, microphone amplifier, headphone amplifier, digital sound effect, analog mixing and gain function. It can be configured through the I2C interface.

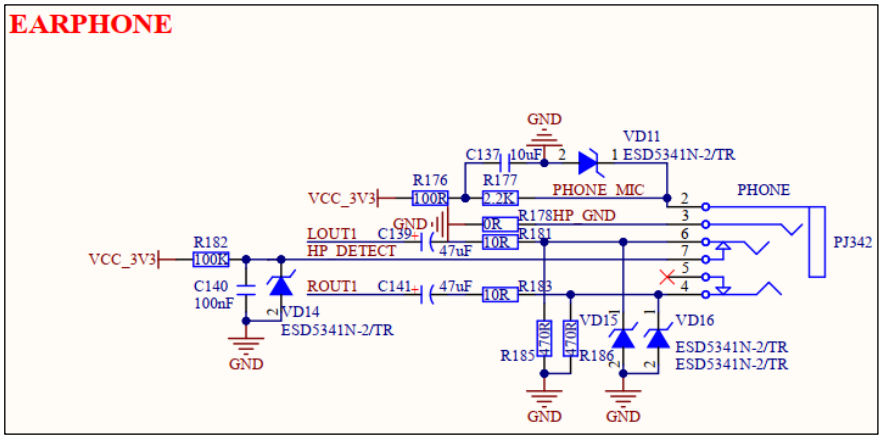


Figure 3.9-2 Headphones playback and recording circuit

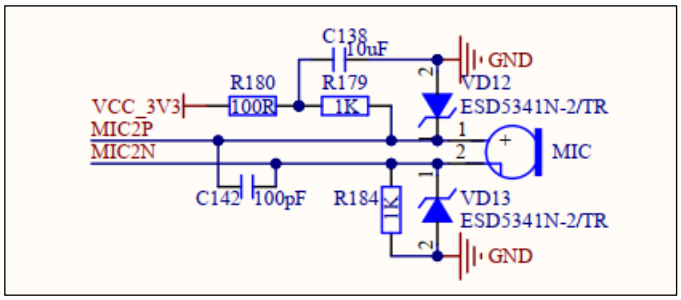


Figure 3.9-3 Electret microphone recording circuit

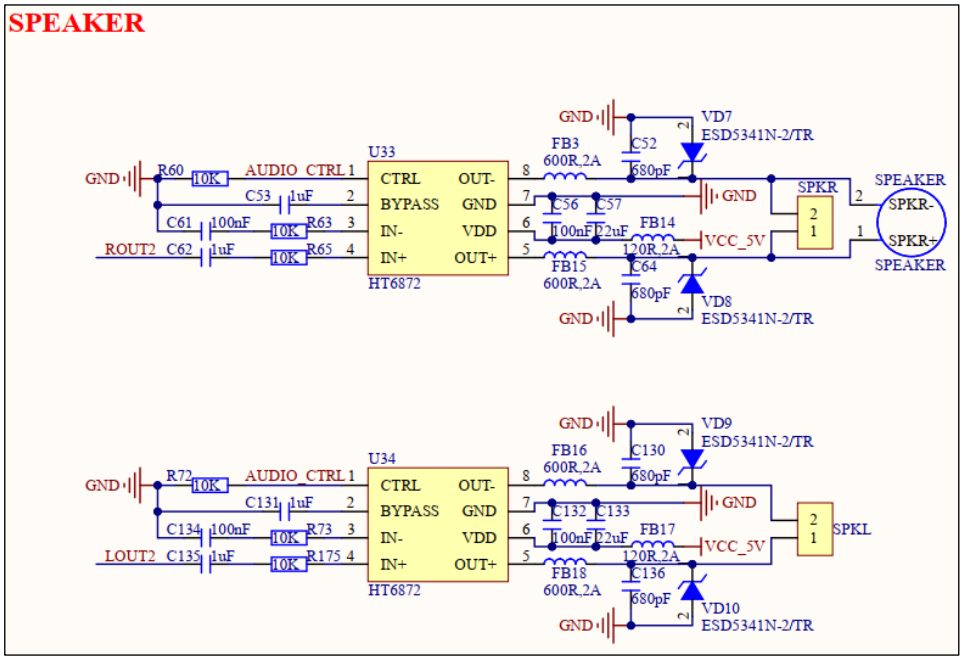


Figure 3.9-4 External power amplifier speaker circuit

Shunxin ES8388 codec chip does not have internal power amplifier function, so it needs external power amplifier chip to play speaker. The development board uses HT6872 mono class D audio power amplifier to drive external speakers. The development board is equipped with an 8Ω1W speaker (on the back), which is connected to the ROUT2 channel of ES8388 through the power amplifier chip HT6872 to provide users with audio testing. At the same time, it also provides two speaker connection terminals of SPKR and SPKL (XH2.54 standard interface) to facilitate users to expand the speaker connection.

In addition to the speaker can play, the development board also supports the headphones to play. The headphones circuit is shown in Figure 3.9.2. When ES8388 plays audio, the development board automatically plays from the external speaker without inserting headphones; When the headset is inserted, it will automatically switch to the headset playback, at which point the speaker will automatically stop playing. The design is consistent with the user's regular use experience. The headphone interface on the development board uses a four-segment 3.5mm headphone interface PJ342, which supports playback, recording and hot swap detection. When designing this interface, users should pay attention to whether the material specifications of the selected headphone holder support 4-segment type. It can also be designed according to the needs of the project.

There are two options for recording, one is the MIC of the headset, and the other is the electret microphone on the development board. Only one of two options can be chosen at the same time. The electret microphone recording circuit is shown in Figure 3.9.3.

3.10 SDIO WIFI& Bluetooth module

There is a SDIO WIFI& Bluetooth module on the development board. The schematic diagram is shown as follows:

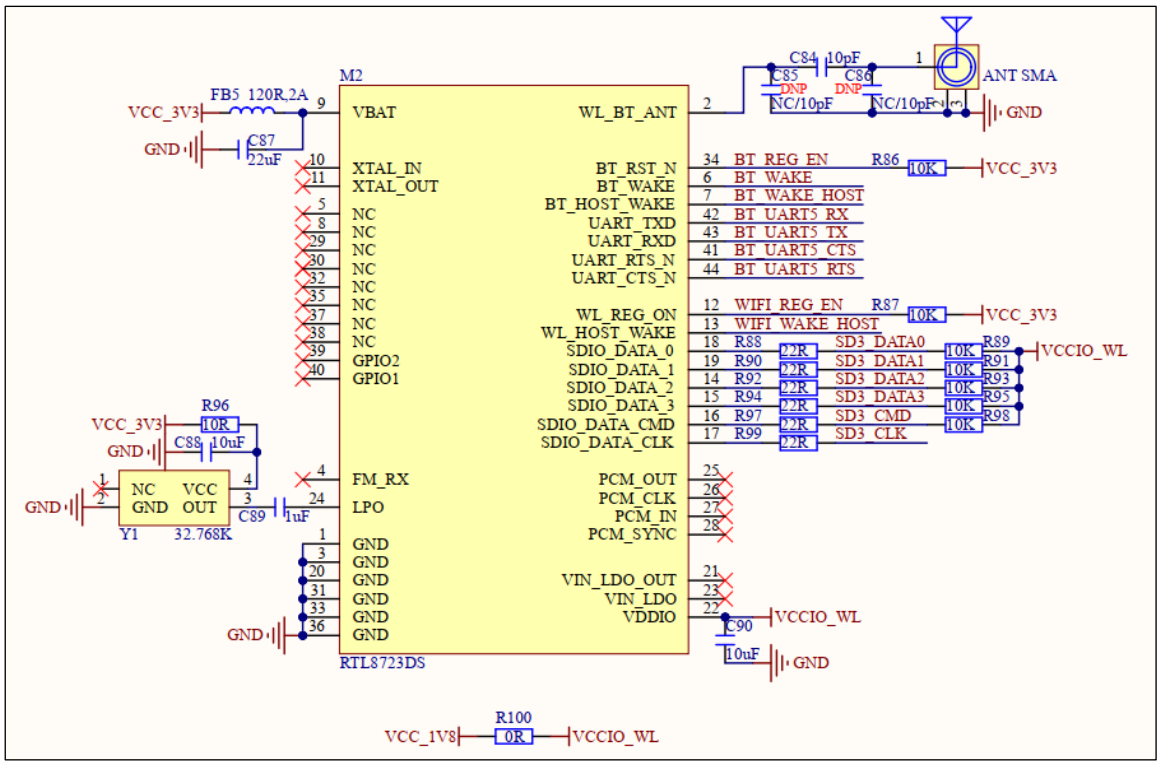


Figure 3.10-1 SDIO WIFI& Bluetooth module

Development board WIFI& Bluetooth module using Realtek RTL8723DS solution, which is a SDIO interface WIFI4 and Bluetooth 4.2 module, wireless band 2.4GHz, connected to the processor i.MX93 SD3 interface.

The Bluetooth function is to send and receive data through the UART5 serial port, which is shared with the JTAG interface pin. Therefore, when users need to use the Bluetooth function, they need to dial all the SW2 dial switches ON the development board to connect to the BT_UART5 serial port signal line of the module.

It should be noted that since the IO level of SD3 bus of processor i.MX93 is 1.8V, the IO power supply of this module should be configured as 1.8V power supply, that is, the VDDIO of pin 22 of the module is 1.8V power supply. According to the RTL8723DS data sheet, 1.8V power domain IO is required for the following pins of this module: BT_WAKE, BT_HOST_WAKE, UART_TXD, UART_RXD, UART_RTS_N, UART_CTS_N, WL_HOST_WAKE, SDIO_DATA_0, SDIO_DATA_1, SDIO_DATA_2, SDIO_DATA_ 3, SDIO_DATA_CMD, SDIO_DATA_CLK. When the user designs the base plate, if some pins choose 3.3V IO, the level conversion is required.

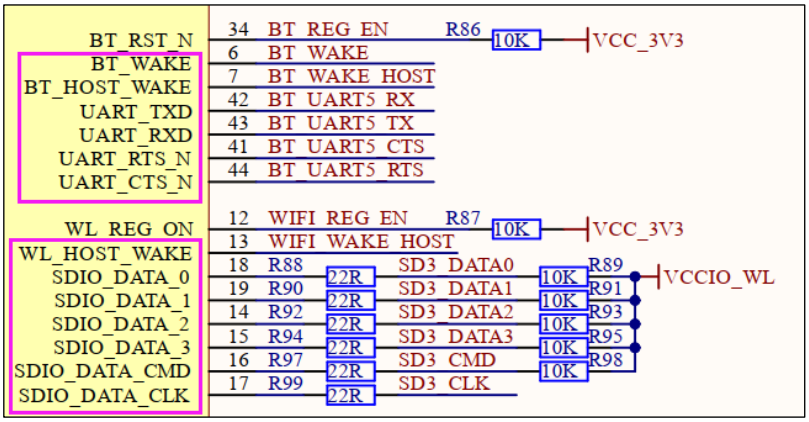


Figure 3.10-2 1.8V power domain IO

3.11 FDCAN interface

The 2-channel FDCAN interface circuit on the development board is shown in the following diagram:

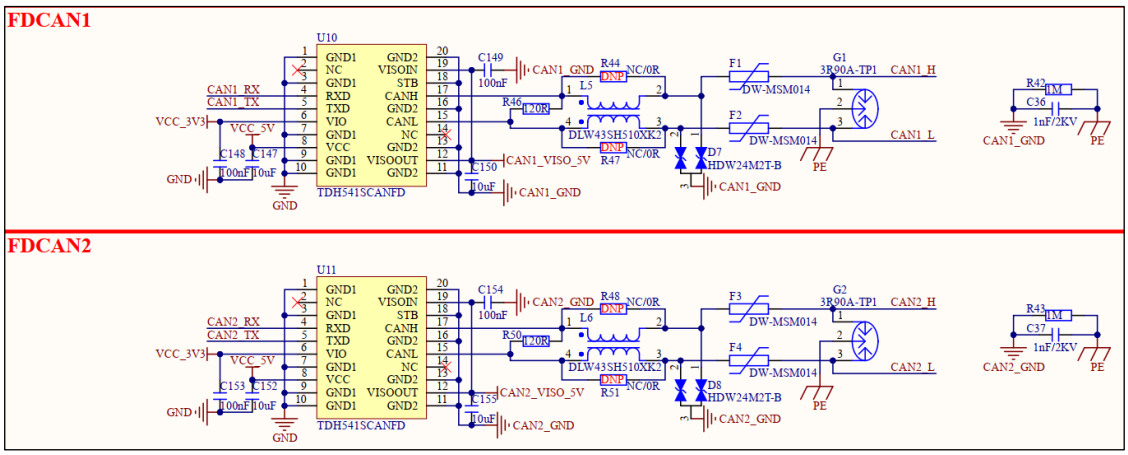


Figure 3.11-1 FDCAN interface circuit

The development board uses isolated CAN transceiver TDH541SCANFD to design CAN interface, supports CAN and CANFD protocol, and the communication rate is up to 5Mbps. The TDH541SCANFD transceiver itself integrates power isolation and digital isolation, and has the characteristics of short circuit protection and over temperature protection, which can protect the inside of the development board from being damaged by external harsh working environment. This circuit adds multiple protective devices to the CAN signal port, which greatly protects the module from damage and ensures the reliability of bus communication. Users need to reliably ground the shielding layer to a single point when using the shielding wire.

3.12 RS485 interface

Development board onboard 2 RS485 interface circuit, schematic diagram as shown below:

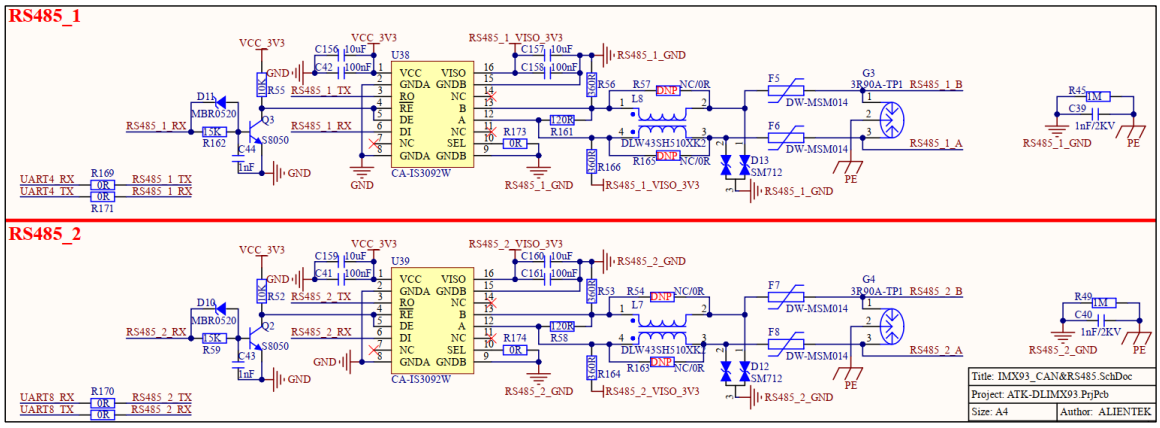


Figure 3.12-1 RS485 interface

The development board uses an isolated half-duplex RS485 transceiver CA-IS3092W for RS485 interface design. The development board uses the CA-IS3092W transceiver of Chipanalog with a communication data rate of 0.5Mbps. It integrates power isolation and digital isolation, and has the characteristics of short circuit protection and thermal shutdown protection, which can protect the inside of the development board from being damaged by external harsh working environment. This circuit adds multiple protective devices to the RS485 signal port, which greatly protects the module from being damaged and ensures the reliability of bus communication. Users need to reliably ground the shielding layer to a single point when using the shielding wire.

The RE and DE pins of the CA-IS3092W transceiver are connected to the UARTx_TX pin through the functional circuit, so that the receiving and sending state of the RS485 transceiver can be automatically controlled through the UARTx_TX pin, and the RS485 can be used completely as a serial port.

3.13 USB HUB interface

There is a USB HUB chip with one expansion and four expansion on the development board, which is used to expand the USB2 of the processor i.MX93 into four USB HOST interfaces (one of which is connected to the 4G module, and the remaining three can be connected to other USB devices). The schematic diagram is shown below:

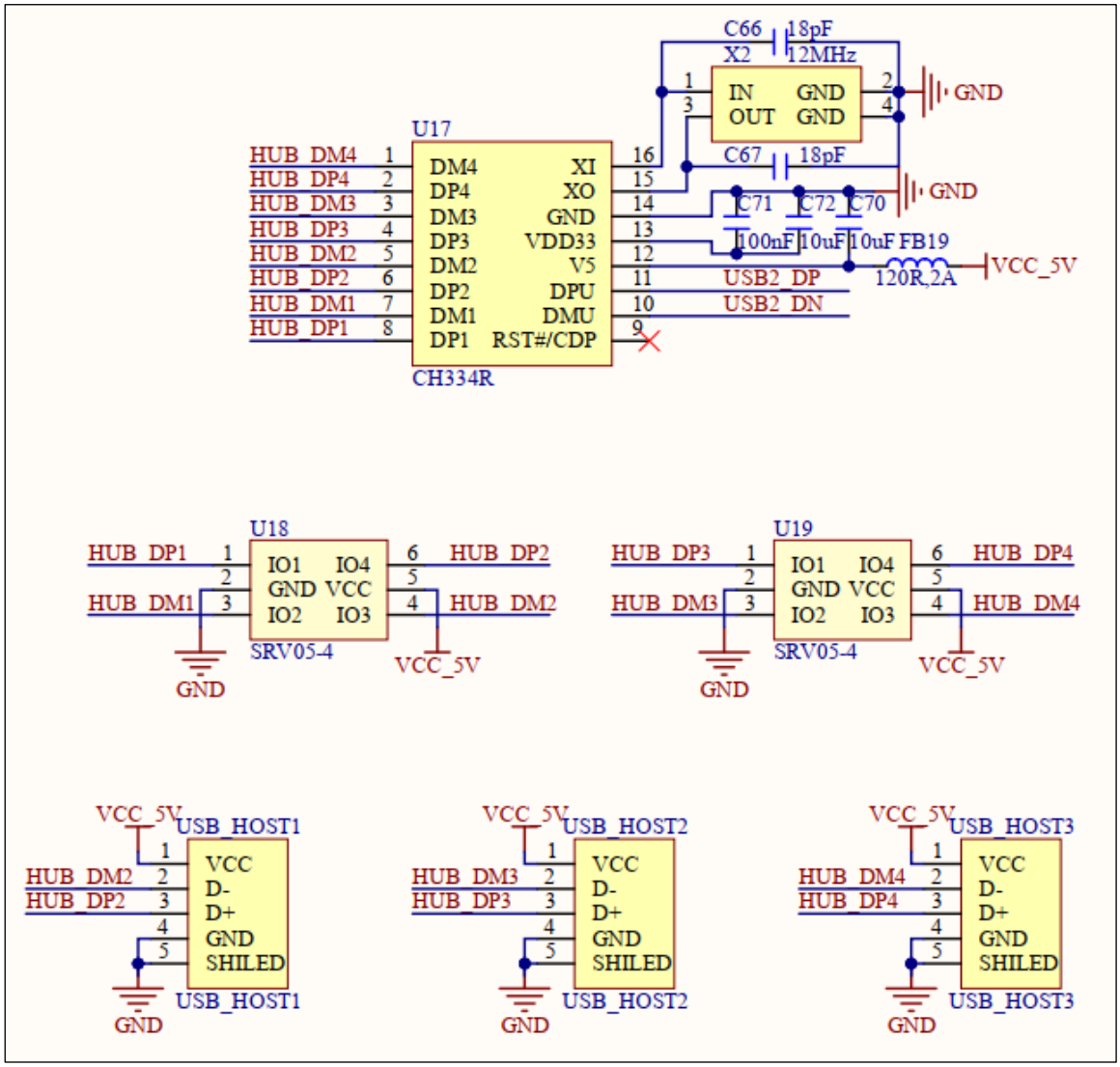


Figure 3.13-1 USB HUB interface

The i.MX93 processor comes with two USB ports, but two USB ports are too few for Linux applications, if we want to connect the mouse, keyboard, USB disk and other devices, then two USB ports are not enough. Therefore, the development board extends the USB2 of i.MX93 out of 4 USB HOST interfaces through the CH334R chip, one of which is connected with the 4G module, so there are 3 USB HOST interfaces provided to users.

3.14 4G module interface

There is a 4G Mini PCIE interface on the development board. The schematic diagram is shown as follows:

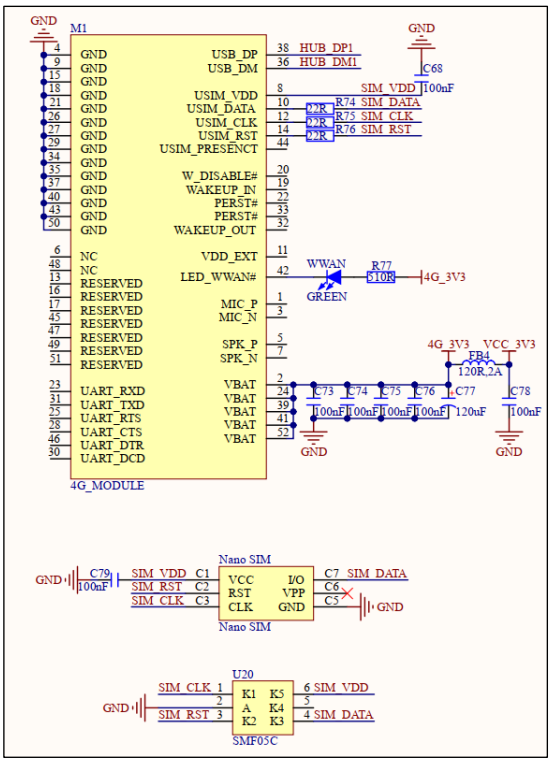


Figure 3.14-1 4G module

M1 is the 4G module connector of Mini PCIE interface, which is used to connect 4G modules of Mini PCIE interface, such as EC20 module. The Nano SIM holder is used to insert the Nano SIM card for use with the 4G module. Although the 4G module uses Mini PCIE interface, the actual USB interface is used. Here, it is connected to a USB HOST interface extended by CH334R.

3.15 Keys (Reset, switch, user)

There are three mechanical buttons on the development board, and the schematic diagram is shown as follows:

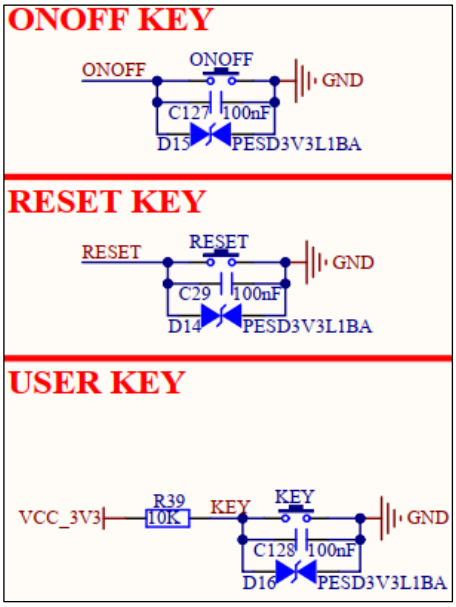


Figure 3.15-1 Input button

The functions of each button are as follows:

1. The ONOFF button is the on/off button of the processor i.MX93. Long press the ONOFF button for 5 seconds, and the processor enters the shutdown state. Press the ONOFF button for 0.5 seconds to turn on the processor. Here again, when the processor enters the shutdown state by long pressing the ONOFF button, the processor will pull the PMIC_ON_REQ pin down to 0V. If the EN pin of the bottom DCDC power chip is enabled by the PMIC_ON_REQ pin, the DCDC power will fail and power off at this time.

2. RESET RESET button is used to reset the core board. Reset signal pin is connected to PMIC_RST_B control pin of PMIC power management chip of the core board, which is used to power up the PMIC again, so that processor, LPDDR4X, EMMC and other core board devices can be powered up again. Reset level is effective for low level.

3. The KEY button is a common input button, which is provided to the user for key input test.

3.16 Adjustable potentiometer

An adjustable potentiometer on the development board is used to complete the ADC voltage acquisition. The schematic diagram is shown as follows:

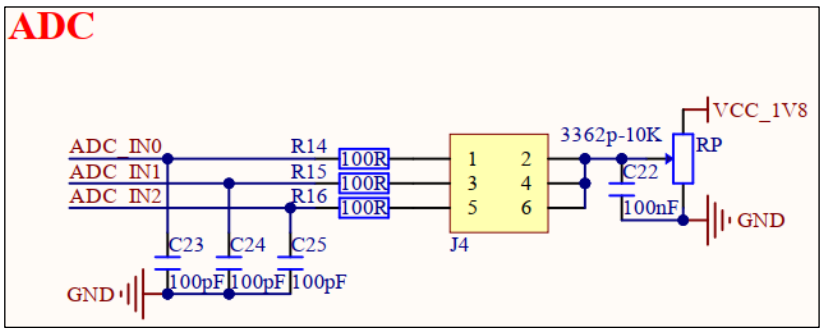


Figure 3.16-1 Adjustable potentiometer

The i.MX93 processor has four ADC-specific pins, and their IO power domain is 1.8V, divided into ADC_IN0 to ADC_IN3. In the figure, RP is an adjustable potentiometer with 10K resistance, which

is drawn to 1.8V power supply. The adjustable resistor is connected to the three ADC channels ADC_IN0, ADC_IN1 and ADC_IN2 through the J4 pin holder, that is, all the three ADC pins can collect the same adjustable potentiometer voltage, and there is a channel ADC_IN3. It is used to identify the ID of the MIPI-DSI screen of the development board, and distinguish the LCD screen with different resolution by collecting different voltage values.

3.17 MIPI-CSI camera interface

A MIPI-CSI camera interface is mounted on the development board, and the camera module supporting MIPI CSI is shown in the following diagram:

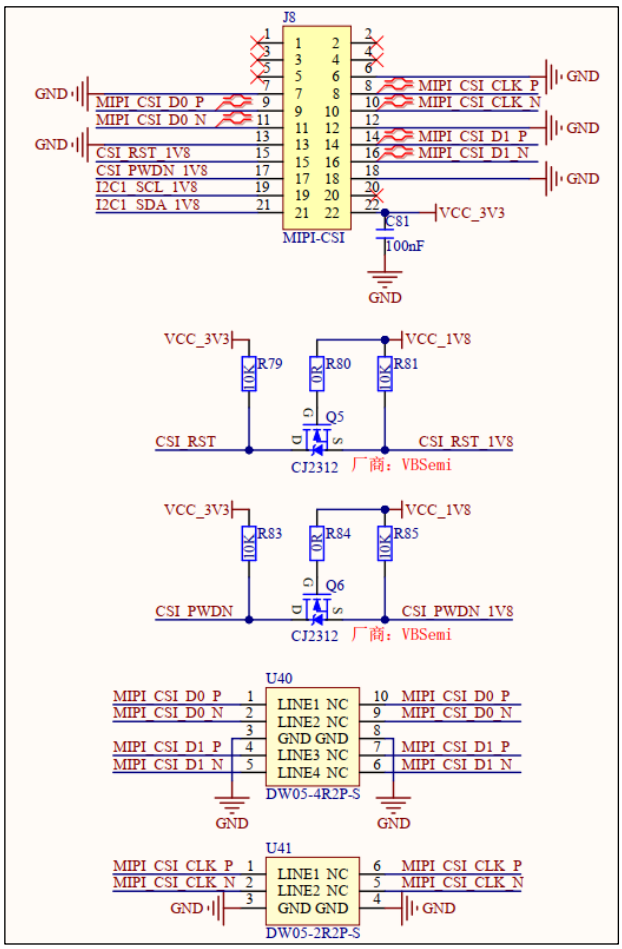


Figure 3.17-1MIPI-CSI camera interface

i.MX93 processor supports 2-lane MIPI CSI-2 camera input signal, including 2 RX data line pairs and 1 RX clock line pairs. Each data line pair supports data rate of 80Mbps -- 1.5Gbps in high speed mode and 10 Mbps in low power mode.This interface has been adapted to support the ALIENTEK ATK-MC5645 camera module (OV5645), in which the four signal pins of CSI_RST, CSI_PWDN, I2C1_SCL and I2C1_SDA are 1.8V IO. If 3.3V IO is selected in the user's design baseboard, the level conversion is required.

3.18 LVDS screen interface

The development board supports LVDS interface screen, the schematic diagram is shown below:

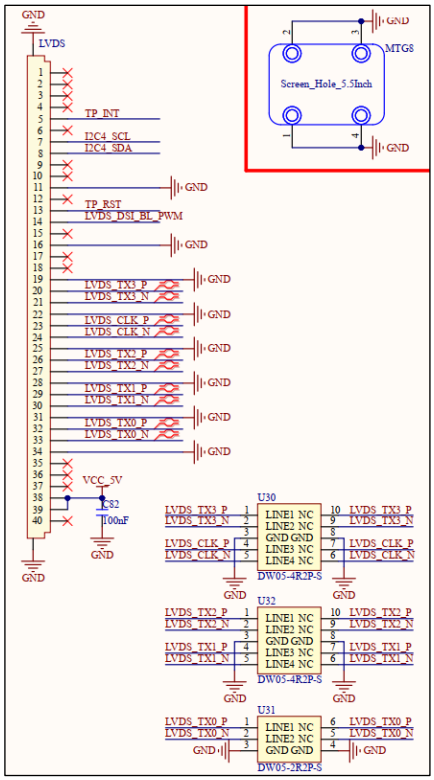


Figure 3.18-1 LVDS screen interface

Processor i.MX93 supports 4-lane LVDS screen display with 1366x768P60 or 1280x800P60 resolution.

The interface has been adapted to a ALIENTEK 10.1 inch 1280*800 LVDS LCD capacitive touch screen, support I2C interface touch. In the figure, TP_INT pin is the interrupt pin of the screen touch chip, TP_RST pin is the power-on and reset enable pin of the screen touch chip, I2C4_SCL and I2C4_SDA are the I2C communication interface of the screen touch chip, which is used for the driver to configure the touch chip, LVDS_DSI_BL_PWM pin is the backlight pin of the screen. Support PWM dimming.

3.19 MIPI-DSI screen interface

The development board supports MIPI-DSI interface screen, the schematic diagram is as follows:

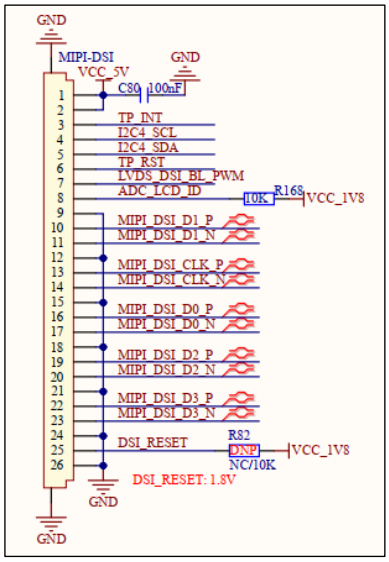


Figure 3.19-1 MIPI-DSI screen interface

The processor i.MX93 supports 4-lane MIPI DSI display with up to 1920x1200 P60 resolution.

The processor i.MX93 has only one LCDIF display controller, which does not support the simultaneous use of LVDS and MIPI DSI interface, that is, it does not support the same display and different display operation, and can only be used alone at the same time.

The interface has been adapted to ALIENTEK 5.5 inch 720*1280, 5.5 inch 1080*1920, 10.1 inch 800*1280 MIPI LCD capacitive touch screen, support I2C interface touch. In the figure, TP_INT pin is the interrupt pin of the screen touch chip, TP_RST pin is the power-on reset enable pin of the screen touch chip, ADC_LCD_ID pin is the ADC acquisition voltage pin to identify the screen ID, I2C4_SCL and I2C4_SDA are the I2C communication interface of the screen touch chip, which is used to configure the touch chip. The LVDS_DSI_BL_PWM pin is the backlight pin of the screen and supports PWM dimming.

Because this interface needs to adapt to MIPI screens with different resolutions of ALIENTEK, this circuit uses ADC_LCD_ID pin for ADC voltage acquisition, and distinguishes different resolutions of screens through different voltage divider configurations of the screen itself, so as to realize screen ID identification function. (Users can refer to the MIPI screen schematic diagram of ALIENTEK with different resolutions to understand this.)

Note that this pin pulls up 10K resistance (accuracy 1%) to 1.8V by default at the interface of the development board. When the development board is not connected to any screen, the voltage sampling value of this ADC pin defaults to about 1.8V. This design will form a parallel connection with the voltage divider resistor of the ALIENTEK MIPI screen itself, thus affecting the screen ID design level. Therefore, the actual ADC voltage sampling value of the screen ID level is subject to this circuit design. When the user designs the bottom board, it is recommended to refer to this circuit design.

3.20 Gigabit Ethernet Interface (RJ45)

Development board onboard 2 Gigabit Ethernet interface (RJ45), the schematic diagram is shown as follows:

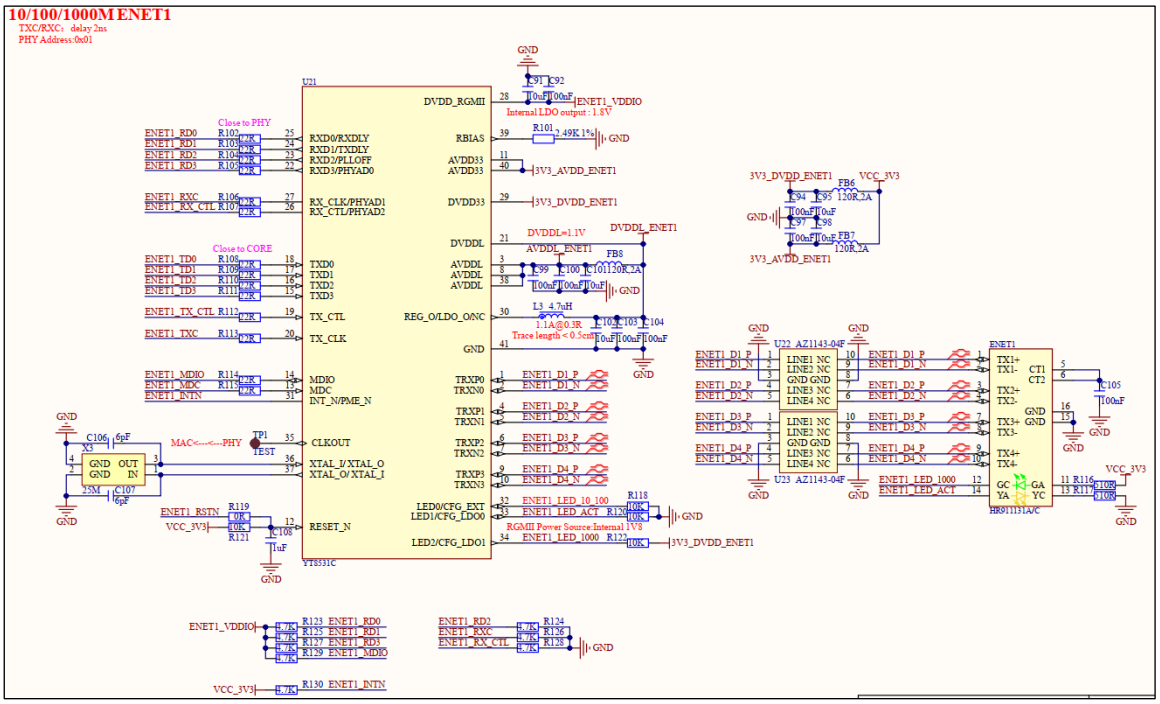


Figure 3.20-1 Gigabit Ethernet interface

i.MX93 processor is equipped with two gigabit network MAC controllers, so it can provide two gigabit Ethernet interfaces.

Here, the example is the schematic diagram of ENET1 network 1, the same is true for ENET2 network 2, pay attention to distinguish the network address, network 1 address is 1, network 2 address is 2.

Since the IO power domain of the network communication TX\RX related pin of the processor i.MX93 is 1.8V, the RGMII voltage of the PHY chip is configured to 1.8V of the PHY built-in LDO output. The ENET1_VDDIO power supply voltage is 1.8V in the figure.

The gigabit network PHY chip model of the development board is Yutai Microelectronics YT8531C, which supports 10/100/1000Mbps rate adaptation. RJ45 connector model HR911131A, built-in network transformer, comes with 2 indicators, designed according to common rules, orange yellow indicator flashing indicates network data transmission, green indicator always on indicates normal network connection. Here, it is recommended to use a four-layer board to design a gigabit network; otherwise, the second-layer board fails to maintain a complete reference plane, which may result in network speeds not reaching near gigabit rates.

3.21 TF card interface

There is a TF card interface on the development board, and the schematic diagram is shown as follows:

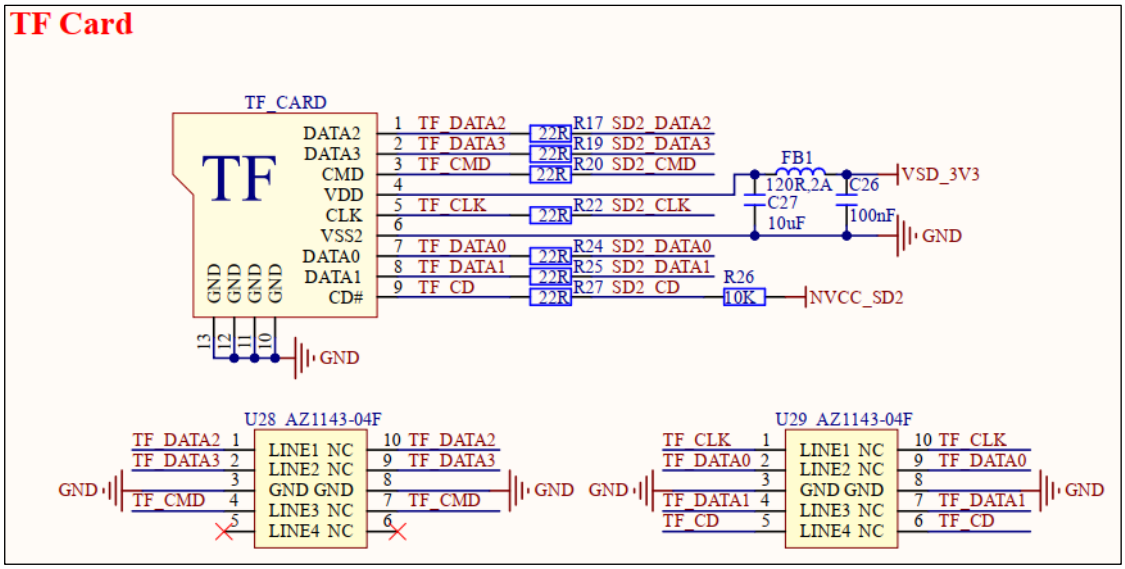


Figure 3.21-1 TF card interface

The processor i.MX93 supports 3-way SD interface, SD3.0 protocol, SD1, SD2 and SD3 respectively. Among them, the SD1 interface is used for the EMMC memory chip of the core board, SD2 is used for this TF card interface, and SD3 is used for the SDIO WIFI module of the development board.

Different types of TF card can use 1.8V or 3.3V IO level to communicate, and 1.8V IO level can support higher speed, so this circuit is compatible to support automatic switching between these two IO levels.

TF_CARD in the figure is the interface of TF card holder, which is driven by 4-wire data line, which is very suitable for the situation that requires high-speed storage. SD2_CD is a hot plug detection pin, power supply VSD_3V3 is fixed to supply 3.3V power supply from the PMIC power management chip on the core board, and SD2 signal line and NVCC_SD2 power level will be determined by the type of TF card inserted by the user. When the user plugs in the high-speed TF card, if the TF card itself supports the working voltage of 1.8V, the SD2 signal line and NVCC_SD2 power level will be switched to 1.8V, otherwise it will be 3.3V.

The TF card level switching is completed by the SD2 interface of i.MX93 processor and the PMIC power chip of the core board, so the user must use SD2 interface when designing the TF card circuit of the bottom board.

3.22 RTC real-time clock

There is a RTC real-time clock chip on the development board. The schematic diagram is shown as follows:

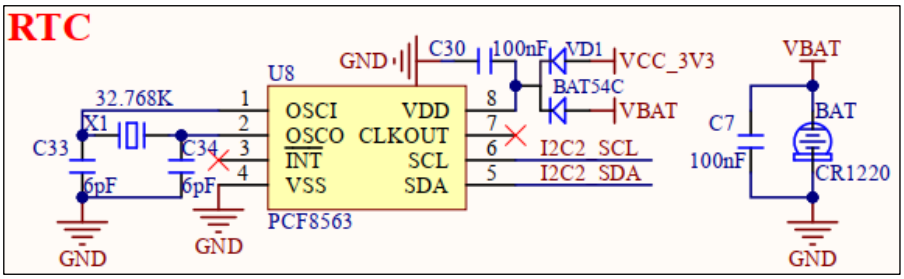


Figure 3.22-1 RTC circuit

The i.MX93 processor has an internal RTC peripheral with a 1.8V power domain that is powered by the PMIC power management chip on the core board. The core board does not lead this internal RTC power domain power supply pin to the baseboard. If the user needs to use the RTC timing function when the whole machine is powered off, it is necessary to use the external RTC chip for timing.

The circuit is designed with PCF8563 RTC chip, which can be compatible with Wuhan Core view RTC chip AT8563.

The VDD power supply of the RTC chip adopts a hybrid power supply mode of button battery CR1220 and on-board 3.3V. When the on-board power supply is 3.3V, the button battery CR1220 does not supply power to the RTC chip. When the onboard power supply is 3.3V, the button battery CR1220 supplies 3V to the RTC chip. In this way, the chip VDD is always powered to ensure RTC timing. If the user needs strict timing accuracy, it is recommended to use better characteristics of the crystal to provide accurate clock.

3.23 EEPROM

There is an EEPROM memory chip on the development board, the model is AT24C64, 8KB, and the I2C interface communication. Users can test and use it according to their own needs. The schematic diagram is shown as follows:

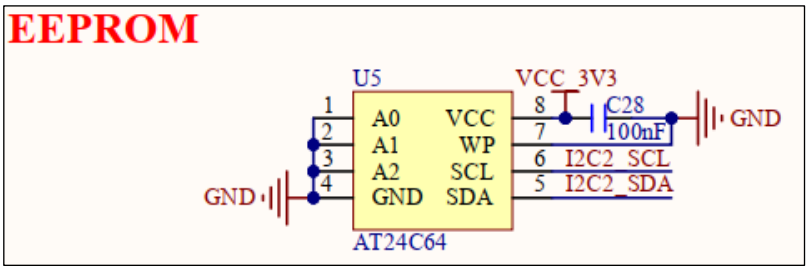


Figure 3.23-1 EEPROM memory

3.24 SPI FLASH

There is an SPI NOR FLASH memory chip on the development board, the model is W25Q128, 16MB, SPI interface communication, users can test according to their own needs, the schematic diagram is shown below:

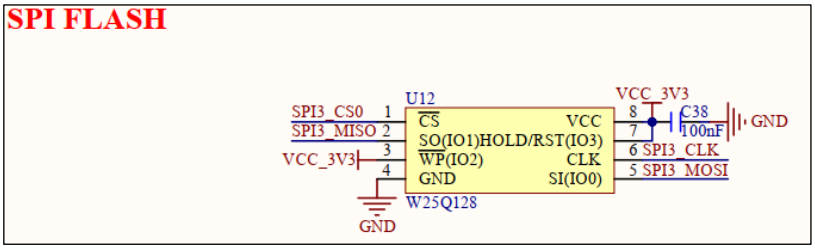


Figure 3.24-1 SPI FLASH storage

3.25 User indicator LED

There is a red status indicator LED on the development board for user control, which is effective at high level. The schematic diagram is shown below:

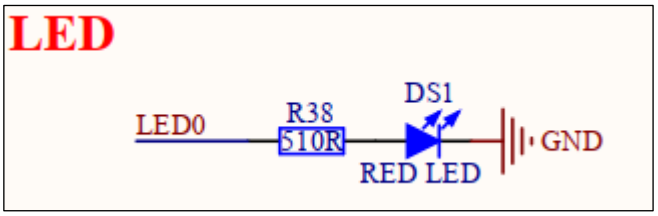


Figure 3.25-1 LED

Chapter 4. Development board use precautions

In order to let users better use the i.MX93 development board, the following introduction of some use precautions, hope that users in the use of more attention to reduce unnecessary problems.

(1) When the user wants to use an IO port for other purposes, please consult the schematic diagram of the development board to check whether the IO port is connected to a peripheral device of the development board and whether it will cause interference to the use. If there is no interference, then use the IO.

(2) When the LCD screen shows a white screen, please check whether the screen is plugged in (unplug and try again), check whether the FPC cable interface contact is damaged, etc.

(3) When the core board needs to be removed from the bottom board, please plug and unplug along the direction marked by the arrow of the core board.

(4) When some peripheral equipment and modules need jumper cap for switching connection, please plug and unplug the jumper cap first before using it.

At this point, the manual hardware platform platform-ALIENTEK i.MX93 development board ATK-DLIMX93 hardware part is introduced, the hardware design scheme for user reference.

If there are any errors in this manual, please contact us for feedback and correction.