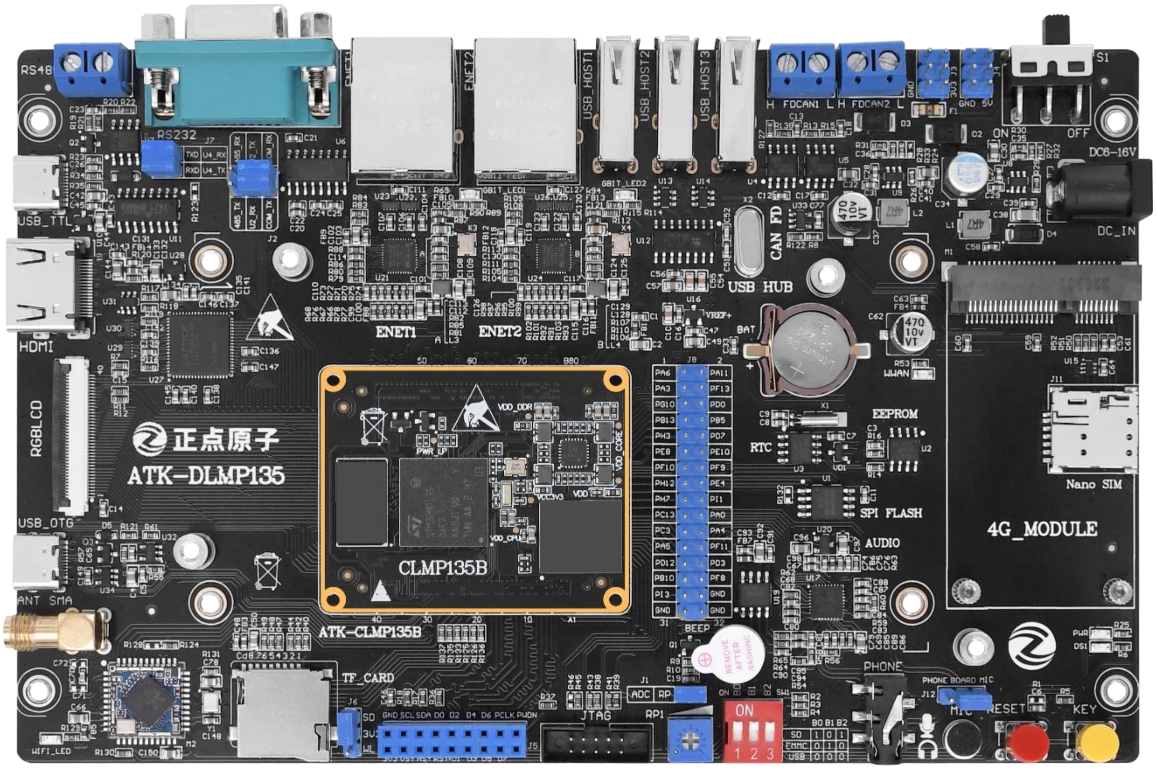
ATK-DLMP135

Hardware Reference Manual

V1.0



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V1.0	release officially	ALIENTEK	ALIENTEK	2023.04.14

Catalogue

Chapter 1. Research on resources of ATK-DLMP135 development board

ALIENTEK currently offers a variety of STM32, I.MXRT, Linux and FPGA development boards. These development boards have consistently ranked as the top sellers on Taobao, with a cumulative shipment of over 100,000 units. This ATK-DLMP135 development board is a development board from ALIENTEK that can run a Linux system. It is designed in the form of a baseboard + coreboard. Now, we will introduce the baseboard and coreboard of the ATK-DLMP135 development board separately.

1.1 Resources of the ATK-DLMP135 Development Board Baseboard

First, let's take a look at the baseboard resource diagram of the ATK-DLMP135 development board, as shown in the following figure:

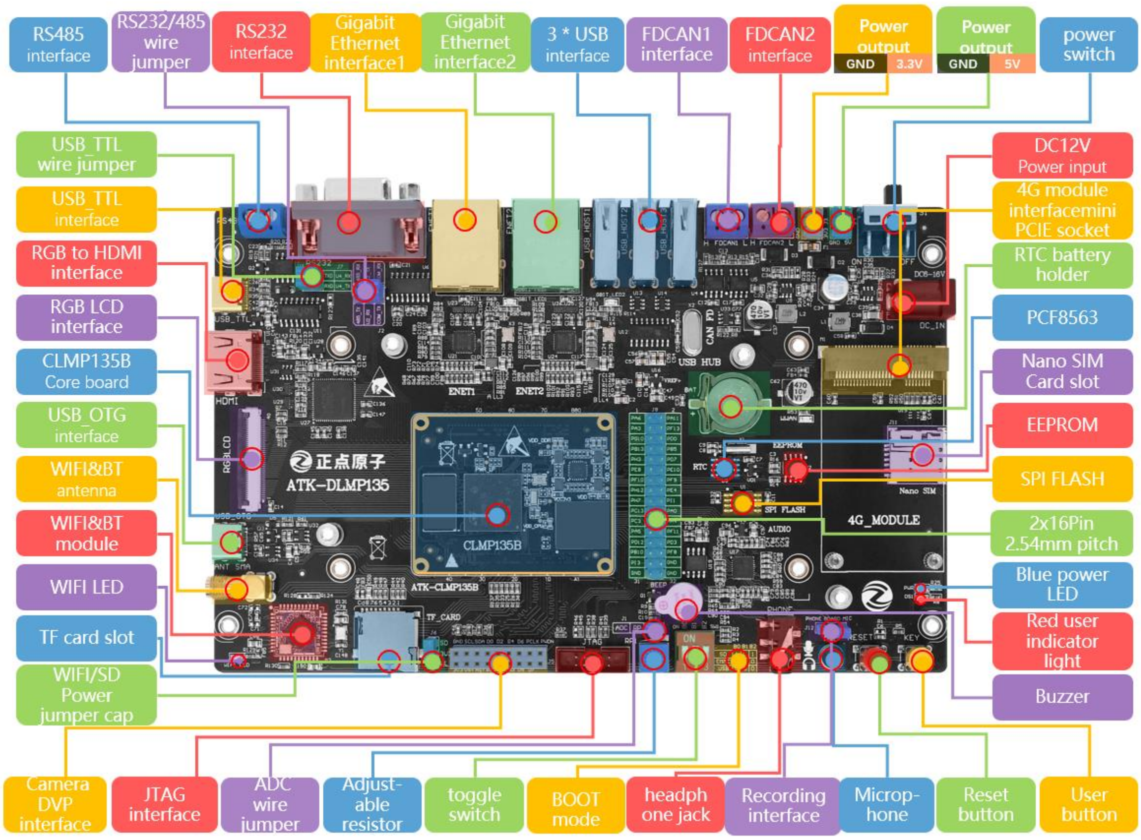


Figure 1-1 The resource diagram of the base board of the ATK-DLMP135 development board

As can be seen from the above picture, the base board resources of the ATK-DLMP135 development board are very abundant, with a wealth of interfaces and functional modules. The size of the development board is 180mm * 115mm, and the design of the board fully considers humanized design, making it convenient for development and use.

The onboard resources of the ALIENTEK ATK-DLMP135 development board base board are as follows:

- 1 core board interface, supporting ATK-CLMP135B core board
- 1 power indicator light (blue)

- 1 status indicator light (red, user can use)
- 1 NOR FLASH chip, W25Q128
- 1 EEPROM chip, AT24C64
- 1 RTC clock chip, PCF8563
- 1 high-performance audio codec chip, CS42L51
- 2 CAN FD interfaces
- 3 USB2.0 HOST interfaces
- 2 10M/100M/1000M Ethernet interfaces (RJ45)
- 1 RS232 serial port (female) interface
- 1 RS485 interface
- 1 RS232/RS485 selection interface
- 1 USB_TTL debugging serial port, Type-C interface type
- 1 serial port connection interface
- 1 RGB to HDMI interface
- 1 RGB LCD screen interface
- 1 USB OTG interface, Type-C interface type
- 1 WIFI&BT antenna interface
- 1 SDIO WIFI&BT module
- 1 TF card interface
- 1 WIFI&TF card power selection interface
- 1 camera module interface
- 1 JTAG debugging interface
- 1 adjustable potentiometer, used for ADC testing
- 1 ADC connection interface
- 1 active buzzer
- 1 startup mode selection configuration interface
- 1 headphone interface, supporting 4-section headphones
- 1 recording head (MIC/microphone)
- 1 small speaker (on the board back)
- 1 recording selection interface
- 1 Mini PCIE 4G module interface
- 1 Nano SIM card interface
- 1 group of 5V power output ports
- 1 group of 3.3V power output ports
- 1 DC12V power input interface (input voltage range: DC6~16V)
- 1 power switch, controlling the power of the entire board
- 1 RTC backup battery seat, with battery
- 1 reset button, can be used to reset MPU and LCD
- 1 user button
- 1 group of 2×16P, 2.54mm pitch pin headers, with 29 IOs, user can use them themselves

The features of the ALIENTEK ATK-DLMP135 development board are as follows:

1) Rich interfaces. The board provides about ten standard interfaces, which can facilitate various peripheral experiments and development.

2) Flexible design. It adopts the core board + base board form, and many resources on the board can be flexibly configured to meet different usage conditions. We have introduced 121 general GPIO pins, as well as 9 other functional pins (USB, NJTRST, VBAT, etc.), 3 VCC_5V pins and 27 GND pins, totaling 160 pins, which greatly facilitates expansion and use.

3) Abundant resources. The board is equipped with a high-performance audio codec chip, gigabit network card, EEPROM storage chip and various interface chips, meeting various application requirements.

4) Humanized design. Each interface has silk-screen marking, making it clear to use; some commonly used peripherals have large silk-screen marking for easy search; the interface position is designed reasonably, making it convenient to use.

1.2 ATK-CLMP135B Core Board Resources

Now let's take a look at the ATK-CLMP135B core board, as shown in the following figure:

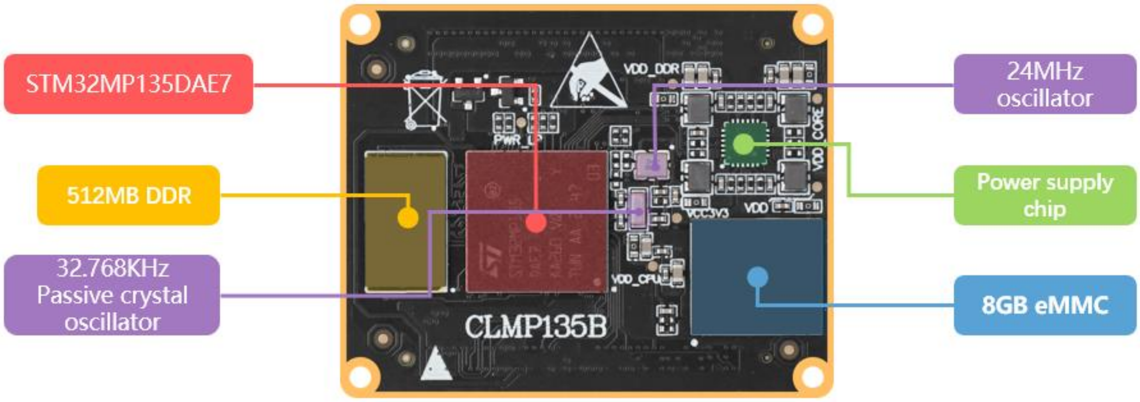


Figure 1-2 ATK-CLMP135B Core Board

The overall size of the core board is 50mm * 40mm, which is very compact. It also adopts surface mount board-to-board connectors, making it easy to be applied in various projects.

The resources onboard the ALIENTEK ATK-CLMP135B core board are as follows:

◆ CPU: STM32MP135DAE7, single-core Cortex-A7, with a main frequency of 1GHz, LFBGA289 package.

◆ External DDR3L: capacity of 512MB, bit width of 16 bits.

◆ EMMC: capacity of 8GB.

◆ Two 2*40 anti-reverse insertion BTB sockets, with a total of 121 GPIOs and 9 other function pins.

The features of the ALIENTEK ATK-CLMP135B core board include:

1) Small size. The core board is only 50mm * 40mm in size, making it convenient to be used in various projects.

2) Easy integration. The core board uses 160P BTB connection sockets, which can be very conveniently integrated onto the customer's PCB, with simple replacement and convenient maintenance and testing.

3) Rich resources. The core board has onboard: 512MB DDR3L, 8GB EMMC memory, which can meet various application requirements.

4) Stable performance. The core board adopts an 8-layer board design, with separate layers for power supply and critical signals, and equal-length wiring for key signals, ensuring stable and reliable operation.

5) Humanized design. The IO pins are divided by function and led out, making wiring convenient.

Chapter 2. Resource Description for the ATK-DLMP135 Development Board

The resource description section will divide these development boards into two parts for explanation: hardware resource description and software resource description.

2.1 ATK-DLMP135 Development Board Hardware Resource Description

Here, we will first provide a detailed introduction to each part of the ATK-DLMP135 development board. We will introduce them in a counterclockwise order:

1. DC12V Power Input

This is an external power input port (DC_IN) on the development board, using a standard DC power socket. The development board is equipped with a DC-DC chip, which is used to provide an efficient and stable 5V power supply to the development board. Due to the use of the DC-DC chip, the power supply range of the development board is very wide. You can easily find a suitable power supply (as long as the output range is within the basic range of DC6 to 16V) to power the development board. In cases where power consumption is relatively high, such as when using 4.3-inch screen/7-inch screen/network port/HDMI/4G and other peripherals, it is recommended to use an external power supply to provide sufficient current for the development board to use.

2. Power Switch

This is the built-in power switch (S1) on the development board. This switch is used to control the power supply of the entire development board. It is a two-section toggle switch. When turned to the left, the power supply of the development board is turned on, and the power indicator light (PWR) lights up. When turned to the right, the power supply of the development board is turned off, and the entire development board will be powered off. The power indicator light (PWR) will go out accordingly.

3. 5V Power Output

This is a set of 5V power output pins (2*3) (JP4) on the development board. These pins are used to provide 5V power to the outside.

During experiments, you might be frustrated by the lack of 5V power. With this set of 5V pins, you can conveniently have a simple 5V power supply.

4. 3.3V Power Output

This is a set of 3.3V power output pins (2*3) (JP3) on the development board. These pins are used to provide 3.3V power to the outside.

Similarly, during experiments, you might be frustrated by the lack of 3.3V power. With the ATK-DLMP135 development board, you can conveniently have a simple 3.3V power supply (with a maximum current not exceeding 1000mA).

5. 2-channel FDCAN interface

This is the FDCAN bus interface (supporting CAN and CAN FD) built into the development board (it supports CAN and CAN FD). It is connected to the external CAN bus through 2 ports, namely CANH and CANL. During CAN communication, CANH must be connected to CANH and CANL to CANL, otherwise the communication will not be normal!

6. 3-channel USB HOST interface

The STMicroelectronics STM32MP135 has two USB interfaces. The ALIENTEK ATK-DLMP135 development board expands the USB1 interface of the STM32MP135 into 4 USB HOST interfaces through the USB HUB chip. One of these interfaces is used to connect the 4G module, and the other 3 are used as USB HOST interfaces. Users can connect USB mice, USB keyboards, USB drives and other devices through these 3 USB HOST interfaces.

7. 2-channel Gigabit Ethernet interface (RJ45)

This is the 2-channel Gigabit Ethernet interface built into the development board. The STM32MP135 has 2 Gigabit Ethernet MAC peripherals inside. It supports 10M/100M/1000M rates.

8. RS232 interface (female)

This is an RS232 interface (RS232) built into the development board. It is connected to an external serial port through a standard DB9 female connector. Through this interface, we can connect a computer or other devices with a serial port to achieve serial communication.

9. RS485 interface

This is an RS485 bus interface (RS485) built into the development board. It is connected to external RS485 devices through two ports. During RS485 communication, A must be connected to A and B to B.

10. RS232/RS485 selection interface

This is an RS232/RS485 selection interface (J2) built into the development board. Since RS485 is basically a half-duplex serial port, to save I/O, we share the same serial port for both RS232 and RS485. Through J2, we can set whether to use RS232 or RS485 at the moment. This design has another advantage. That is, our development board can act as a TTL serial port to RS232 conversion and also as a TTL serial port to RS485 conversion. (Note, the TTL high level here is 3.3V)

11. USB_TTL Debug Serial Port

This is a USB Type-C interface (USB_TTL) built into the development board, used for USB connection to the CH340C chip, thereby achieving USB to serial conversion and serving as the system debugging serial port.

12. USB_TTL Connection Interface

This is the interface for connecting the USB serial port to the serial port 4 of STM32MP135 (J7). The labels TXD and RXD are the two data ports for USB to serial conversion (for CH340C), while U4_TX (TXD) and U4_RX (RXD) are the two data ports of the serial port 4 of STM32MP135. They can be connected together by using the jumper caps, thus enabling the serial communication of STM32MP135.

13. HDMI Interface

This is the HDMI interface built into the development board. The STM32MP135 does not have a native HDMI peripheral. This interface converts the RGB LCD interface of the STM32MP135 into an HDMI interface through the Sil9022A. Therefore, the supported resolution depends on the internal RGB LCD peripheral (LTDC) of the STM32MP135. The highest resolution that LTDC can support is 1366*768.

14. RGB LCD Interface

This is the RGB LCD interface (LCD), which can be connected to various Point Atom's RGB LCD module and supports touch screens. It uses the RGB888 format and can display 16.77 million colors, providing rich color display.

15. USB OTG Interface

This is a USB Type-C interface built into the development board. This interface is connected to the USB2 interface of the STM32MP135 and is used to implement the OTG function. USB Type-C cables can be used to connect the development board to a computer, where the development board acts as a Slave and performs system burning. USB OTG cables can also be used to connect other USB devices, such as USB drives, and in this case, the development board acts as a Host.

The development board has a total of two USB Type-C interfaces. One (USB_TTL) is used for USB to Serial conversion and is connected to the CH340C chip; the other (USB_OTG) is for the internal USB of the STM32MP135.

16. WIFI & Bluetooth Antenna

This is a WIFI and Bluetooth antenna interface. WIFI and Bluetooth share a 2.4G antenna.

17. SDIO WIFI & BT Module

This is a WIFI & Bluetooth module built into the development board, connected to the SDMMC1 interface of the STM32MP135 via the SDIO interface. The chip used in this module is the RTL8723DS from Realtek, which is a WIFI + Bluetooth 4.2 integrated chip. The WIFI operates on the 2.4G frequency band. WIFI and Bluetooth share a single 2.4G antenna, saving board space and facilitating PCB layout and wiring.

18. TF Card Interface

This is a standard TF card interface (TF_CARD) built into the development board, using a small TF card interface and driven by the SDMMC method. With this TF card interface, the demand for large-capacity data storage can be met.

19. WIFI/TF Card Power Selection Interface

This is the power selection interface for WIFI/TF card. The SDIO WIFI module and the TF card share the same set of SDMMC1 communication lines. They cannot be used simultaneously, so a switch is needed. Here, a power selection method is adopted for power supply switching, making it convenient to use. When the power is supplied to the WIFI module, a blue WIFI_LED power indicator light will illuminate.

20. Camera Module Interface

This is a camera module interface (CAMERA) built into the development board, supporting the Point Grey camera module (needs to be self-provided). Align and insert it into this slot.

21. JTAG Interface

This is a 10P, 2.0mm spacing JTAG interface that can be connected to the STlink debugger.

22. Adjustable Potentiometer

This is a 10K adjustable potentiometer that is connected to the ADC pin of ST32MP135 and can be used to learn the ADC acquisition of STM32MP135.

23. ADC Connection Interface

When using the adjustable potentiometer, a jumper cap needs to be connected to allow the ADC pin to be connected to the adjustable potentiometer; when not using the adjustable potentiometer, the jumper cap can be disconnected, and the pin can be used for other functions.

24. Boot (BOOT) DIP Switch

STM32MP135 supports multiple boot methods, such as SD card, eMMC, NAND, QSPI FLASH, and USB, which are all controlled through the BOOT switch (corresponding to the BOOT0~2 pins on the STM32MP135). To boot from a certain device, the boot DIP switch must be set first. The Pointronic ATK-DLMP135 development board uses a 3P DIP switch to select the boot method, supporting boot methods from SD card, eMMC, USB, etc. The operation mode of the DIP switch corresponding to the boot method is already printed on the development board's silk screen. Users can set the DIP switch according to their actual needs.

25. Beeper

This is an onboard beeper, an active one, so it only requires power supply and can be controlled by the control pin for sound control.

26. Headphone Interface

This is the onboard headphone interface of the development board. This interface can accommodate a 4-section 3.5mm headphone, supporting recording and playback. When the CS42L51 is playing back, you can insert a headphone into this interface. The speaker amplifier and the onboard microphone share the CS42L51 AOUTB channel, and will simultaneously output audio. If the headphone has a MIC, it can also be used to record using the MIC on the headphone. Before recording, you need to first jump the J12 jumper cap to the left side, which means using the headphone's built-in MIC. If it is connected to the right side, it will use the onboard MIC microphone.

27. MIC (Microphone)

This is the onboard recording input port (MIC) of the development board. This microphone is connected to the MIC input pin of the CS42L51 and can be used to implement the recording function.

28. Recording Selection Interface

The development board has a 4-section headphone socket. This headphone socket supports using the headphone MIC for recording. Both the headphone and the onboard MIC microphone are connected to the MIC pin of the CS42L51. Therefore, only one can be used for recording at a time. Here, you need to adjust the J12 jumper cap to select whether to use the headphone MIC for recording or the onboard MIC microphone. If the jumper cap is connected to the left side, it will use the headphone MIC. If it is connected to the right side, it will use the onboard MIC microphone.

29. Reset Button

This is the built-in reset button (RESET) on the development board, used to reset the STM32MP135. It also has the function of resetting the LCD, because the reset pin of the LCD module is connected to the reset pin of the STM32MP135. When this button is pressed, both the STM32MP135 and the LCD are reset.

30. User Button KEY

This is a mechanical input button (KEY) built into the development board, which can be used as a regular button input.

31. Red User LED

This is a user LED light built into the development board, red in color. Users can use this LED light. During code debugging, using the LED to indicate the program status is a very good auxiliary debugging method.

32. Blue Power Indicator LED

This is the power indicator LED light of the development board, blue in color. When the board is powered on normally, this light will remain on. If this light is not on, it indicates that there is a problem with the power supply of the development board (excluding the case where the LED light is damaged).

33. Nano SIM Card Interface

This is the Nano SIM card interface on the development board. If you want to use the 4G module, you need to insert the Nano SIM card into this interface.

34. Mini PCIE 4G Interface

This is a Mini PCIE socket built into the development board, but it essentially follows the USB protocol. Through this interface, you can connect the 4G module, such as the ME3630 from Hengxin IoT. After connecting the 4G module, the STM32MP135 development board can achieve 4G internet access functionality. It is a good choice for situations where it is inconvenient to lay network cables or there is no WIFI.

35. Exposed IO Ports

This is the IO exposed port J8 of the development board, using a 2×16 pin header. A total of 29 IO ports are exposed.

36. ATK-CLMP135B Core Board Interface

This is the core board interface on the bottom board of the development board, consisting of 2 pairs of 2*40 surface mount board-to-board connection terminals. It can be used to insert the ALIENTEK ATK-CLMP135B core board, so as to learn the development of the STM32MP135 processor.

37. PCF8563 Real-Time Clock

PCF8563 is a RTC real-time clock chip, an external RTC chip with an IIC interface. The STM32MP135 also has an RTC peripheral inside, but its accuracy is not high. Therefore, the ATK-DLMP135 development board adds an external RTC chip for users to test.

38. Backup Battery Interface

This is the power supply interface for the backup area of STM32MP135, which can be used to provide power to the backup area of STM32MP135. When the external power source is disconnected, it can maintain the operation of the backup area and RTC.

39. EEPROM

This is a board-mounted EEPROM storage chip, model AT24C64, with a capacity of 8KB, IIC interface, for users to store and test.

40. SPI FLASH

This is a board-mounted SPI NOR FLASH storage chip, model W25Q128, with a capacity of 16MB, SPI interface, for users to store and test.

2.2 Software Resource Description of ATK-DLMP135 Development Board

In the previous section, we have provided a detailed introduction to the hardware resources of the ALIENTEK ATK-DLMP135 development board. Now, let's briefly introduce the software resources of the ATK-DLMP135 development board. The software resources are divided into three parts: Linux system software resources, Linux driver routines, and QT development routines. The QT development routines can be found in the dedicated QT tutorial documents. Regarding the Linux system software resources, the following table is provided:

Type	Description	Note
TF-A	Version：2.6	Provide the source code
OP-TEE	Version：3.16	Provide the source code
U-Boot	Version：2021.10	Provide the source code Supports LCD display, supports SD card and eMMC, supports

		network, and supports modification of environmental variables, etc.
Linux kernel	Version：5.15.24	Provide the source code
Root file system rootfs	Provide buildroot and debian as two root file systems and their production methods	Provide tutorials
QT5 root file system	QT version : 5.12.9	Provide tutorials
Cross compiler	arm-buildroot-linux-gnueaihf, version:9.4 arm-none-linux-gnueabihf, version:10.3	Provide softwares
System flashing method	STM32CubeProgrammer and SD card both	Provide tutorials
LCD drive	RGB LCD drive	Provide the source code
Touch	FT5xx6, GT9147 and other capacitive touch screens (available only from ALIENTEK)	Provide the source code
RS485	RS485 drive	Provide the source code
RS232	RS232 drive	Provide the source code
FDCAN	FDCAN drive	Provide the source code
Internet	PHY is YT8531C	Provide the source code
USB HOST	USB HUB is SL2.1A	Provide the source code
USB OTG	USB slave machine and the master machine	Provide the source code
4G wireless	ME3630 4G module	Provide the source code
KEY	GPIO	Provide the source code
LED	GPIO	Provide the source code
Audio	CS42L51	Provide the source code
SDIO WIFI&BT	ALIENTEK RTL8723DS module	Provide the source code
EEPROM(IIC)	AT24C64，IIC interface	Provide the source code
NOR FLASH(SPI)	W25Q128，SPI interface	Provide the source code
TF card/EMMC	SDMMC drive	Provide the source code
Camera	OV5640 drive	Provide the source code
Serial port	UART drive	Provide the source code
PWM backlight	LCD PWM backlight	Provide the source code
Built-in RTC	Internal RTC of STM32MP135	Provide the source code
External RTC	PCF8563 RTC chip	Provide the source code
HDMI	Sil9022A HDMI chip	Provide the source code
ADC	ADC drive	Provide the source code

Table 1.2.2.1 Software Resources of the Linux System on the Development Board

Let's take a look at the embedded Linux driver routines of the ATK-DLMP135 development board, as shown in the following table:

Number	Name	Number	Name
1	chrdevbase	13	irq
2	led	14	blockio
3	newchrled	15	noblockio

4	dtsled	16	asyncnoti
5	gpioled	17	platform
6	beep	18	dtsplatform
7	atomic	19	miscbeep
8	spinlock	20	input
9	semaphore		
10	mutex		
11	key		
12	timer		

Table 1.2.2.2 Linux Driver Examples for ATK-DLMP135 Development Board

Since some peripheral drivers are already integrated into the Linux kernel, we have not written independent drivers for them. We will explain and update these drivers in the corresponding chapters. This concludes the explanation of the software resources for the ALIENTEK ATK-DLMP135 development board. We will continue to update the software resources, so please pay attention to the latest information about the development board.

Chapter 3. Detailed Explanation of the Schematic Diagram of the ATK-DLMP135 Development Board

The following explains the circuit design of each part of the development board schematic diagram for user reference only.

It is particularly noted that the hardware circuit of the development board may be updated and optimized, and version iterations may occur. If users refer to this circuit for product project development, please evaluate by themselves whether it meets the project requirements and carry out circuit optimization, protection, etc.

3.1 The core board interface

The ATK-DLMP135 development board adopts the form of a base board + core board. The base board of the development board uses two 2*40 3710M (male socket) board-to-board connectors to connect with the core board, which is very convenient for plugging and unplugging. The schematic diagram of the core board interface on the base board is shown in the following figure:

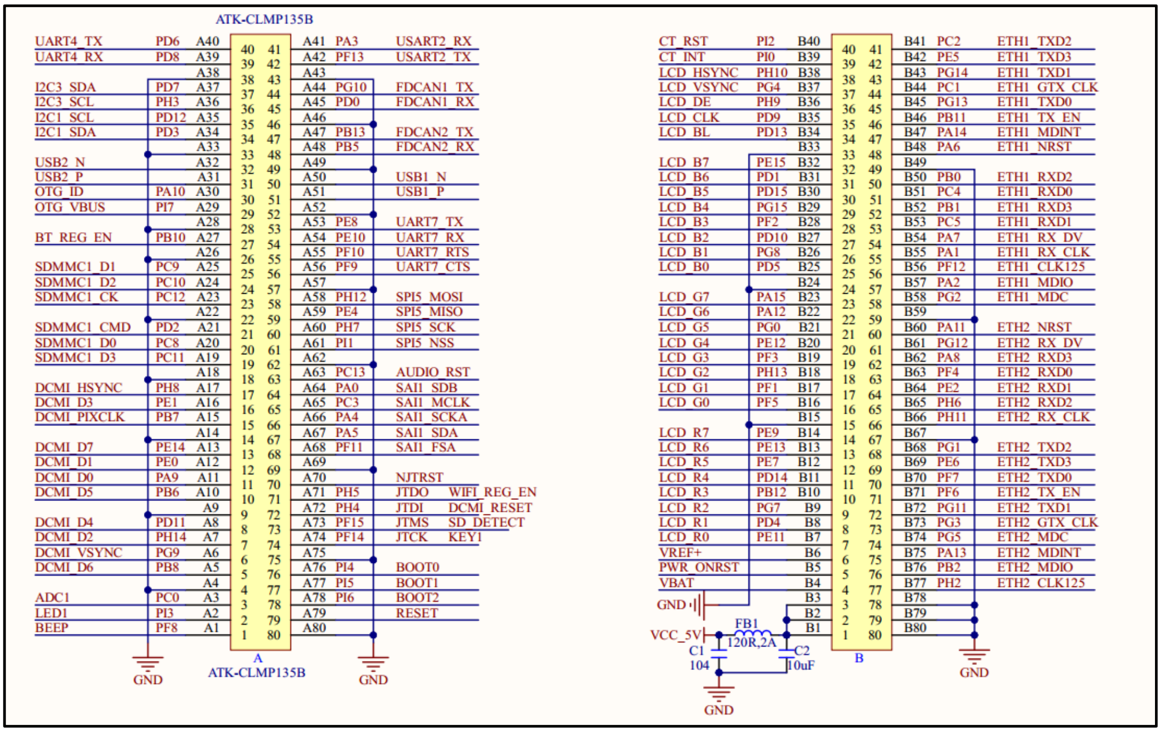


Figure 3-3-1 Schematic diagram of the interface part of the base plate adapter board

In the figure, A and B are the connection seat interfaces on the base plate, consisting of 2 pairs of 2*40PIN 3710M board-to-board male sockets, including 121 GPIOs, 9 other function pins, 27 GND pins and 3 5V power input pins, forming a 160PIN structure.

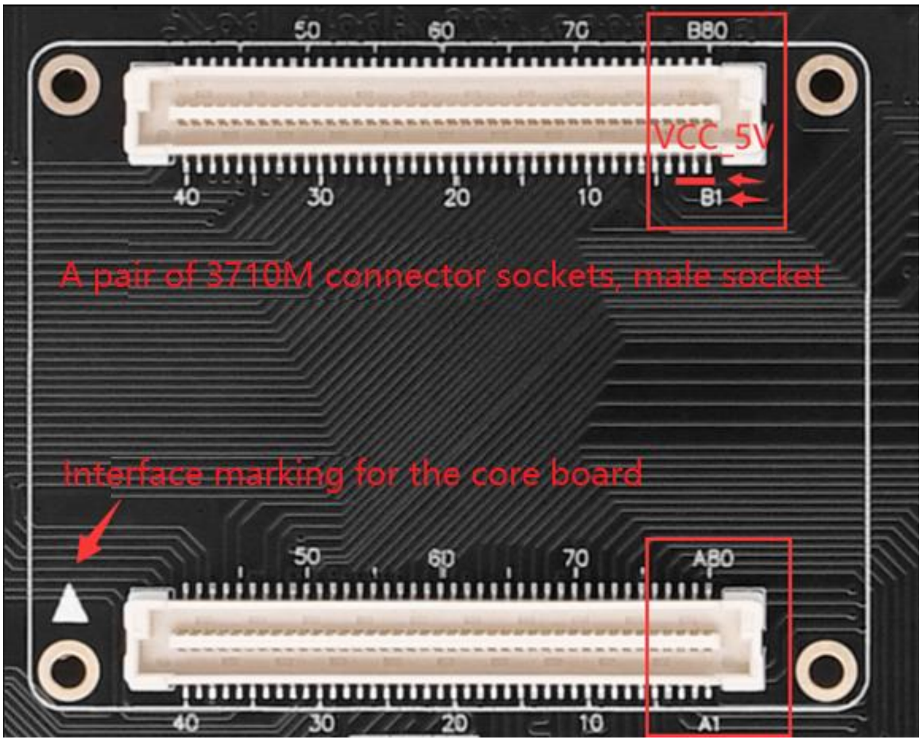


Figure 3-3-2 Physical diagram of the base plate adapter interface

When designing the base plate, users should pay attention to the defined sequence of the connection seats and ensure that the connections are not reversed. In the figure, B1 to B3 pins are the input pins for the 5V power supply VCC_5V, which supplies power to the core board. B78 to B80 are three consecutive GND pins, and other pins follow the same pattern.

3.2 Exposed IO ports

On the base plate of the ATK-DLMP135 development board, 29 IO ports are exposed through a 2x16 pin header group, as shown in the following figure:

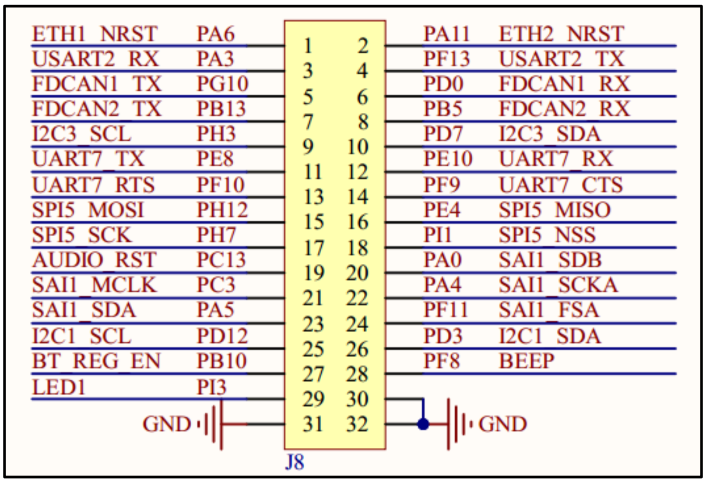


Figure 3-3-3 Exposing the I/O ports

In the figure, J8 is the exposed I/O. There are a total of 29 I/Os, plus 3 GNDs for exposure, forming a 2x16 pin group. You can use these I/Os to connect some other modules for more interesting innovations. Here, it is particularly emphasized that when using a specific I/O alone, it should not conflict with the functions of the development board. Do not use it simultaneously. Changes to the system reuse function are required. Additionally, it is necessary to check the configuration of these I/Os on the baseboard's functional circuit. For example, resistors for pull-up and pull-down, and parallel capacitors have been used. If this affects the use, manual removal is required.

3.3 USB serial port/Serial port 4 selection interface

The USB serial port onboard the ATK-DLMP135 development board and the serial port of the STM32MP135 are connected through J7, as shown in Figure 3.4:

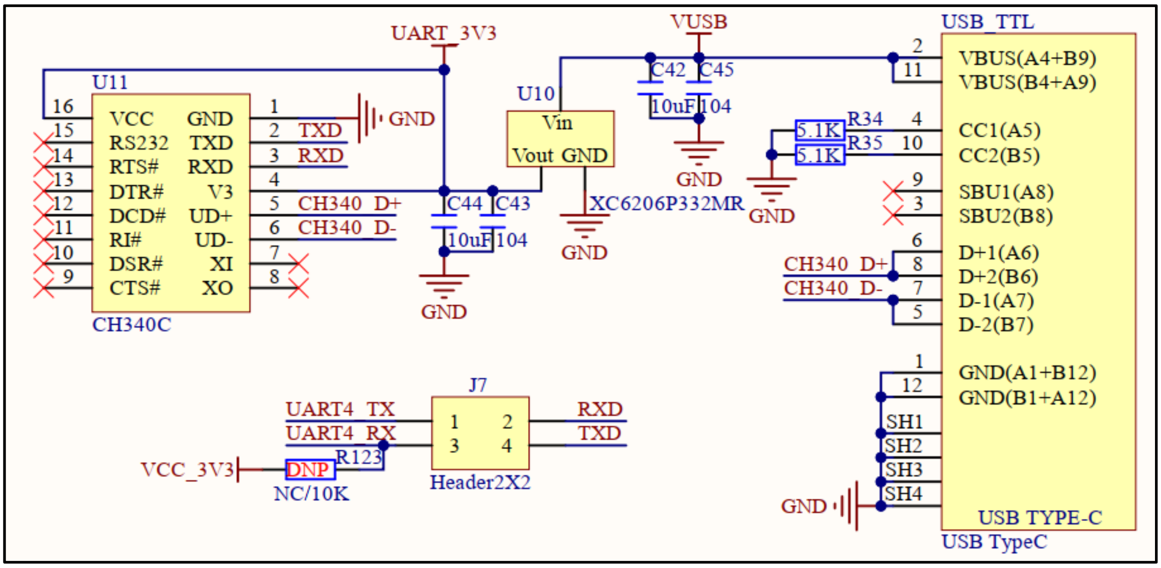


Figure 3-3-4 USB serial port / Serial port 4 selection interface

In the figure, TXD/RXD refer to the sending and receiving pins of the USB serial port, relative to the CH340C. While UART4_RX and UART4_TX are relative to the STM32MP135. By connecting UART4_TX to RXD and UART4_RX to TXD through the jumper cap, serial communication between the USB serial port and the STM32MP135 can be achieved.

3.4 RGB LCD module interface

The ATK-DLMP135 development board is equipped with an RGB LCD interface. The circuit for this part is shown in Figure 3.5:

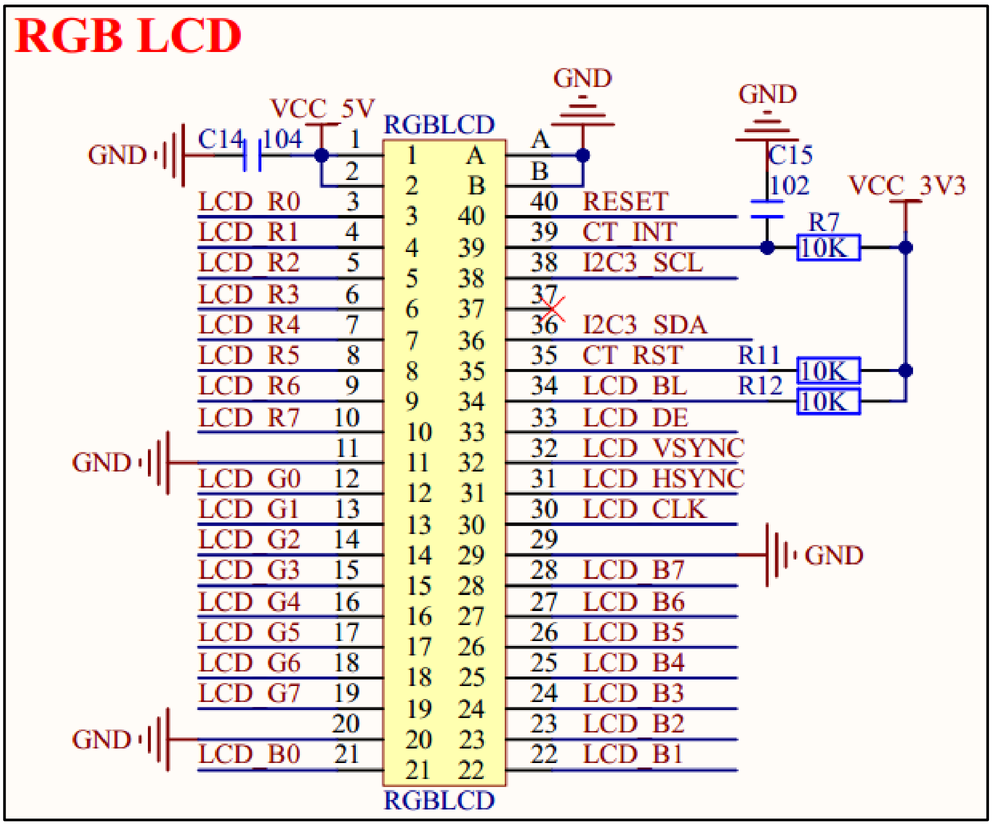


Figure 3-3-5 RGB LCD interface

In the figure, RGBLCD refers to the RGB LCD interface, which adopts the RGB888 data format and supports touch screens (capacitive screens). This interface only supports liquid crystal displays with RGB interfaces (does not support liquid crystal displays with MCU interfaces). Currently, the RGB interface LCD modules from ALIENTEK include: 4.3 inches (ID: 4342, 480*272 and ID: 4384, 800*480), 7 inches (ID: 7084, 800*480 and ID: 7016, 1024*600), and 10 inches (ID: 1018, 1280*800) in various sizes.

The I2C3_SCL and I2C3_SDA in the figure are the two data lines of I2C3, connected to PH3 and PD7 respectively. LCD_BL is the backlight control IO of the LCD, connected to PD13 of STM32MP135, used to control the backlight of the LCD. The LCD reset signal RESET is directly connected to the reset button of the development board and shares the reset circuit with STM32.

3.5 Reset circuit

The reset circuit of the ATK-DLMP135 development board is shown in Figure 3.6:

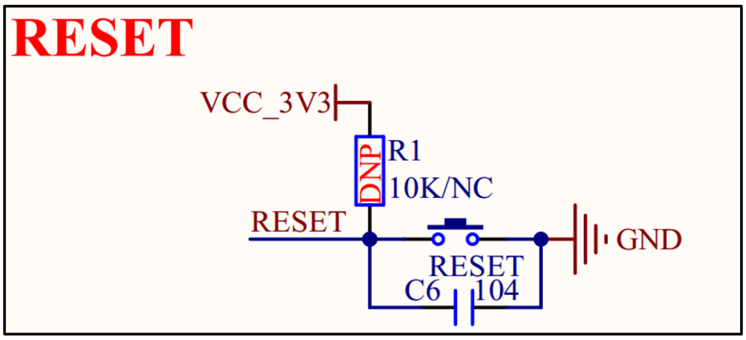
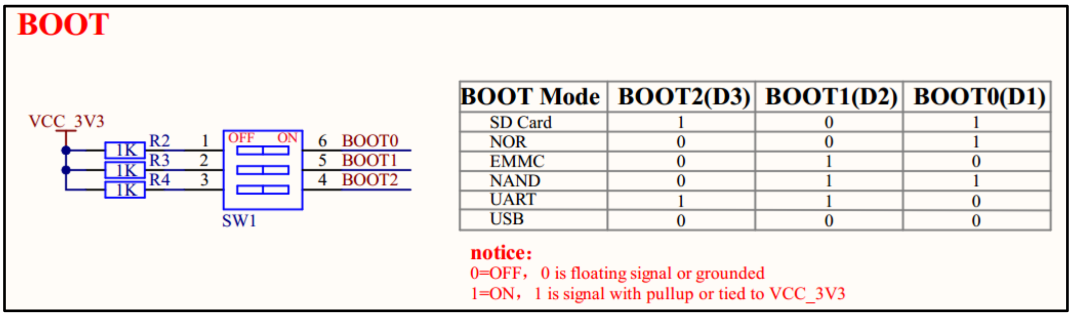


Figure 3-3-6 Reset circuit

Since STM32MP135 is reset by low level, the circuit we designed is also reset by low level.

3.6 Boot mode setting interface

The BOOT boot mode setting interface circuit of the ATK-DLMP135 development board is shown in Figure 3.7:



BOOT Mode	BOOT2(D3)	BOOT1(D2)	BOOT0(D1)
SD Card	1	0	1
NOR	0	0	1
EMMC	0	1	0
NAND	0	1	1
UART	1	1	0
USB	0	0	0

Figure 3-3-7 Boot mode setting interface

The STM32MP135 supports booting from various different devices. By setting the dip switch, the booting from a specific device can be selected. The booting methods are as shown in Table 3.7.1:

BOOT2(D3)	BOOT1(D2)	BOOT0(D1)	Boot mode
1	0	1	SD card boot-up
0	0	1	NOR boot-up
0	1	0	EMMC boot-up
0	1	1	NAND boot-up
1	1	0	USB/UART boot-up
0	0	0	
1	0	0	Development boot (noflash memory boot)

Table 3.7.1 Startup Modes

The ATK-DLMP135 development board on the ALIENTEK ATK-DLMP135 supports USB, SD card, and EMMC startup modes. The STM32MP135 also supports a development startup mode called "Development boot (no flash memory boot)", which can be debugged via the JTAG interface. The ATK-DLMP135 development board also supports this mode.

3.7 VBAT Power Supply Interface

The VBAT power supply circuit of the ATK-DLMP135 development board is shown in Figure 3.8:

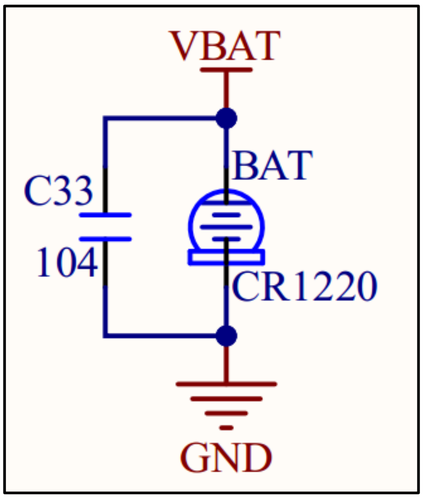


Figure 3-3-8 VBAT power interface

As shown in the above figure, the VBAT is connected to the VBAT pin of the STM32MP135 through the BAT54C on the core board, thereby supplying power to the backup area of the core board. This part of the schematic diagram is on the core board and is shown in Figure 3.9:

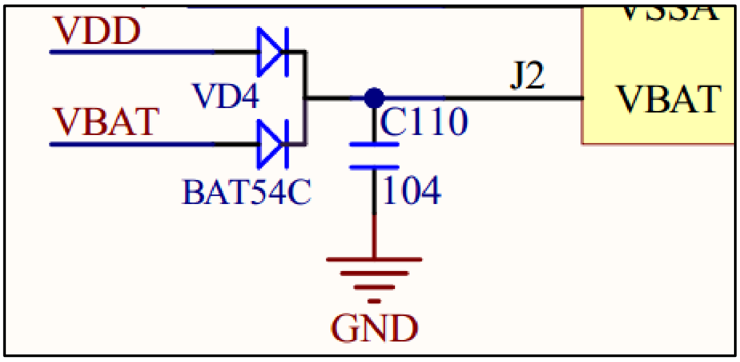


Figure 3-3-9 Core board VBAT power supply schematic

As shown in Figure 3.9, the VBAT pin uses a mixed power supply method of VBAT (connected to the CR1220 battery) and VDD. When there is an external power supply (VDD), the CR1220 does not supply power to VBAT, while when the external power supply is disconnected, it is powered by the CR1220. Thus, VBAT is always powered, ensuring the timing of the RTC.

3.8 RS232 serial port

The ATK-DLMP135 development board is equipped with 1 RS232 interface (female connector), and the circuit schematic is shown in Figure 3.10:

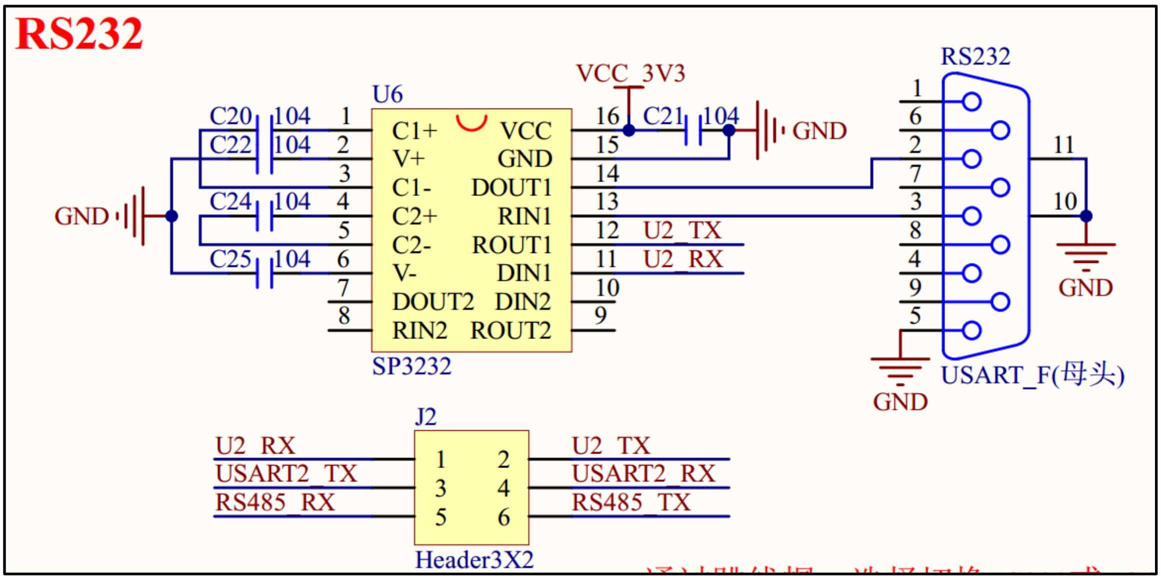


Figure 3-3-10 RS232 serial port and selection interface

Since the RS232 level cannot be directly connected to the STM32MP135, a level conversion chip is required. Here, the SP3232 (or other RS232 level conversion chips) is selected for RS232 level conversion in the schematic diagram. At the same time, the J2 in the figure is used to achieve the selection of RS232 (female connector) / RS485. Therefore, both RS232 (female connector) / RS485 are realized through serial port 2.

3.9 RS485 interface

The RS485 interface circuit on the ATK-DLMP135 development board is shown in Figure 3.11:

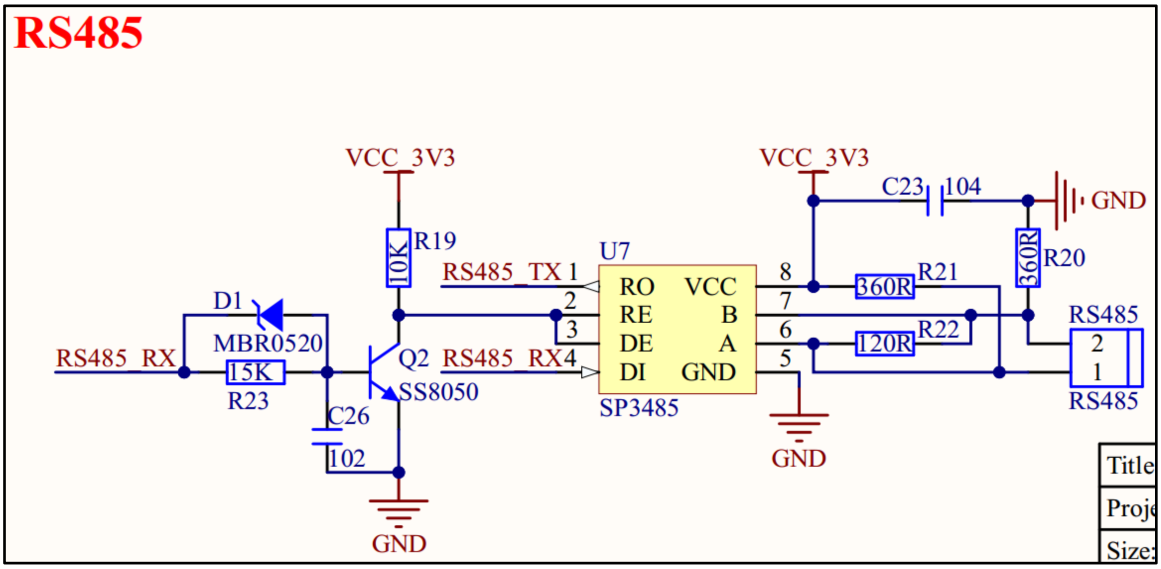


Figure 3-3-11 RS485 interface

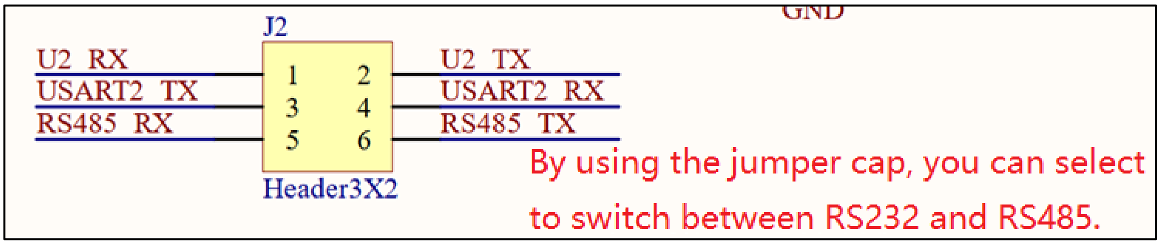


Figure 3-3-12 RS485/RS232 selection interface

The RS485 level cannot be directly connected to the STM32MP135 either; a level conversion chip is still required. In the schematic diagram, the SP3485 (or other RS485 level conversion chips) is selected here for RS485 level conversion. R22 is the termination matching resistor, while R21 and R22 are two bias resistors to ensure that the 485 bus maintains logic 1 in the silent state.

RS485_RX/RS485_TX are connected on J2, and the connection to the STM32MP135 can be selected through J2 jumper. When using RS485, RS485_RX should be connected to the USART2_TX pin, and RS485_TX should be connected to the USART2_RX pin. The RE pin of the SP3485 is connected through a series of circuits to the RS485_RX pin, so that the receiving and sending states of RS485 can be controlled through the RS485_RX pin, completely using RS485 as a serial port.

3.10 FDCAN interface

The ATK-DLMP135 development board is equipped with 2 channels of FDCAN interface circuits, as shown in Figure 3.13:

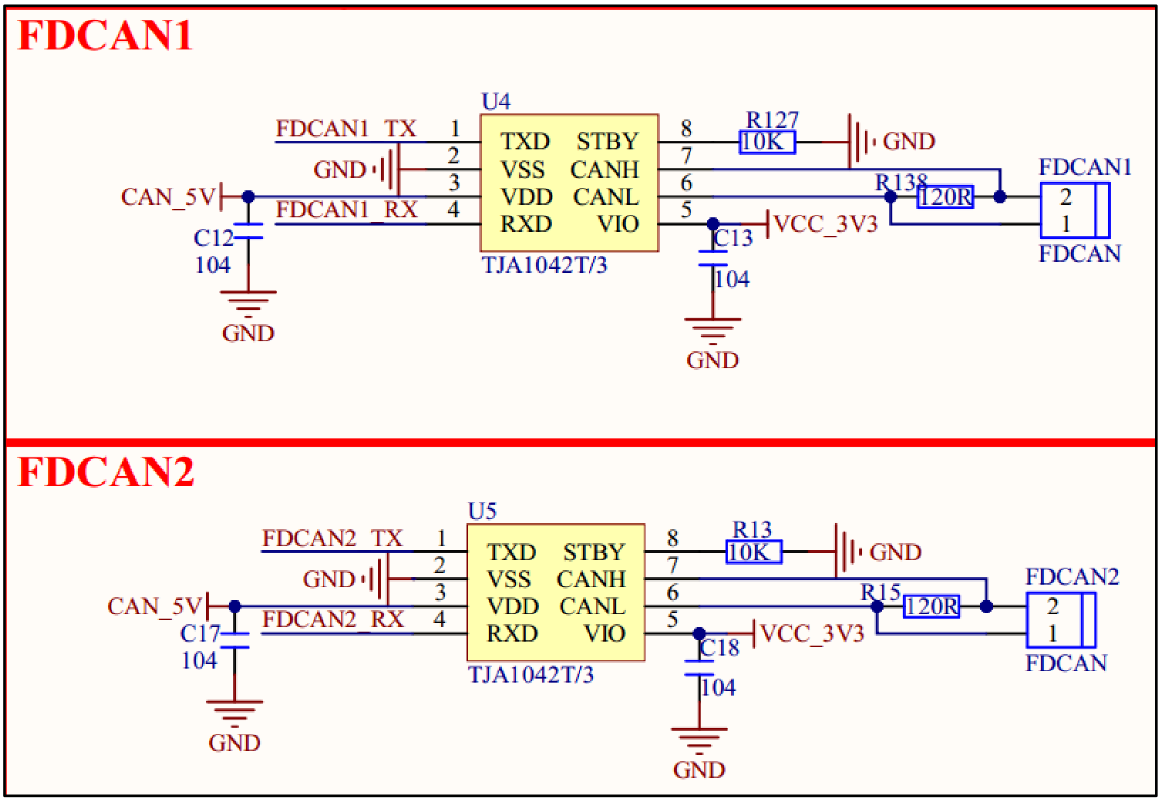


Figure 3-3-13 FD CAN interface circuit

The CAN bus level cannot be directly connected to the STM32MP135 either. A level conversion chip is also required. In the schematic diagram, the TJA1042T (or other CANFD level conversion chips that support CAN and CAN FD protocols) is used for CAN level conversion.

3.11 USB HUB interface

The ATK-DLMP135 development board is equipped with a one-expand-four USB HUB chip, which is used to expand the USB1 of the STM32MP135 to 4 USB HOST interfaces (where one interface is connected to the 4G module, and the remaining 3 interfaces can be connected to other USB devices), as shown in Figure 3.14:

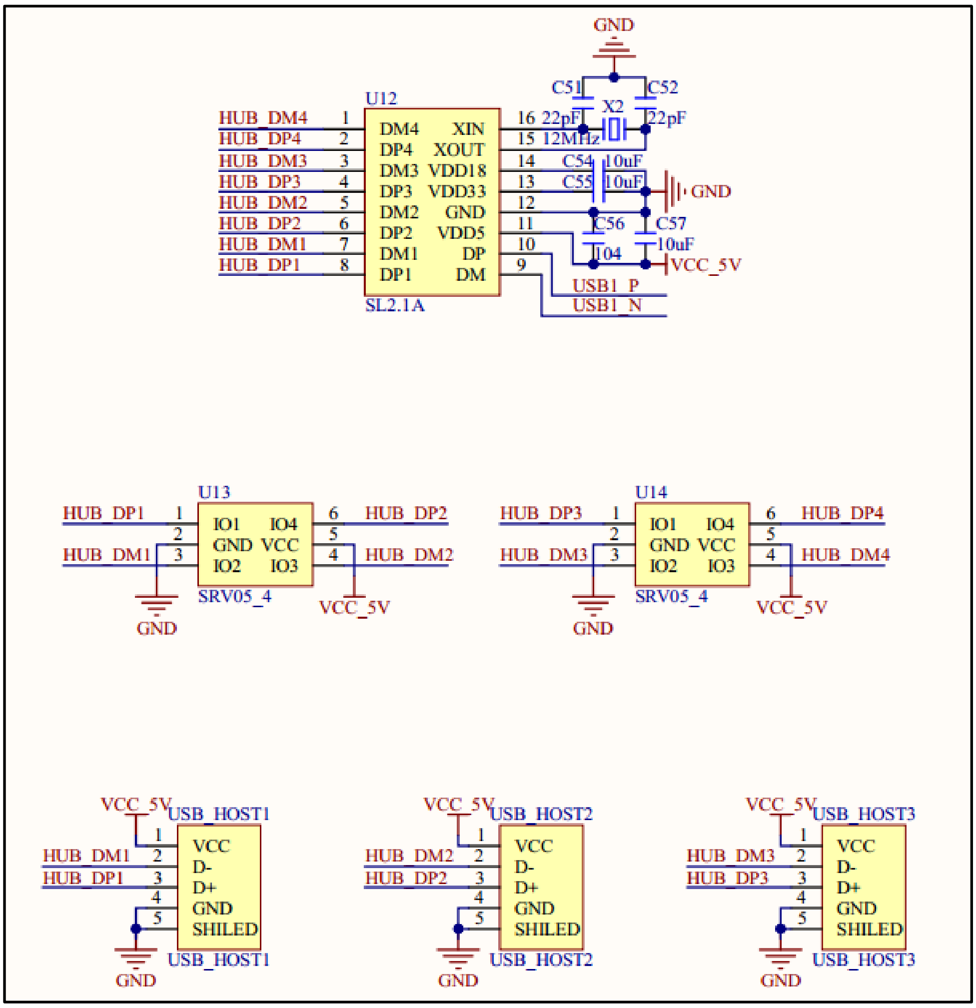


Figure 3-3-14 USB HUB interface circuit

The STM32MP135 has two USB interfaces, but for Linux applications, two USB interfaces are too few. If we want to connect devices such as mice, keyboards, USB drives, etc., the two USB ports are simply not enough. Therefore, the STM32MP135 development board expands the USB1 interface of the STM32MP135 to four USB HOST interfaces through the SL2.1A chip. Among them, one interface is externally connected to a 4G module, so there are three USB HOST interfaces provided to users.

3.12 USB OTG (Type-C) interface

The STM32MP135 also has one USB OTG interface. The USB OTG interface uses the USB2 of the STM32MP135. The USB OTG interface is shown in Figure 3.15:

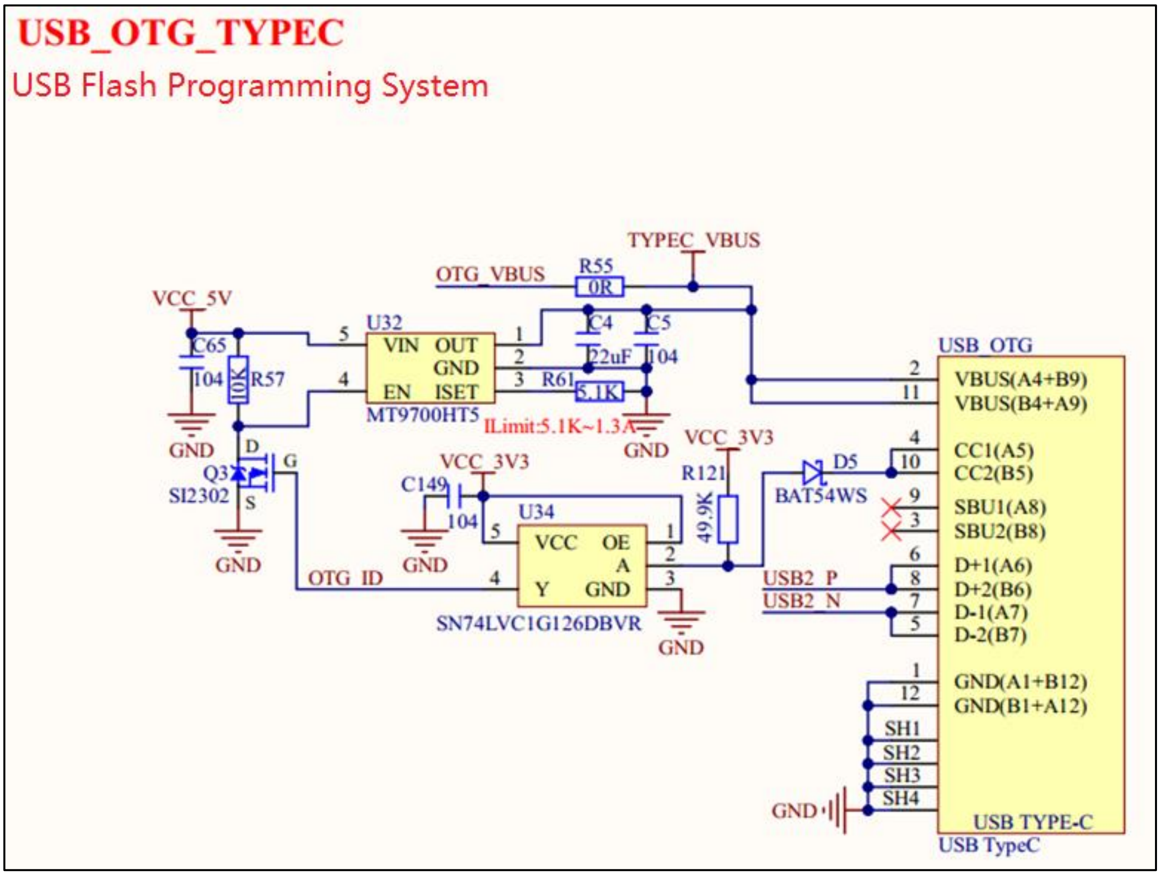


Figure 3-3-15 USB OTG interface

The USB_OTG circuit can function as both a USB slave device and a USB host. The USB_OTG on the right side in Figure 3.15 is the Type-C socket. We use this USB Type-C socket for system programming and USB OTG testing. If you need to conduct USB OTG testing, you will also need to purchase a Type-C OTG cable. The default mode of STM32MP135 is as a slave device. Here, to support the USB host mode, a tri-state buffer device is added. When the OTG adapter is connected to a USB drive, it can pull down the OTG_ID pin, thereby allowing the processor to enter the USB host mode. If the user designs the baseboard USB interface not to use the Type-C interface, then a Micro USB interface can be used instead. In this case, the USB-OTG circuit does not need to add a tri-state buffer.

3.13 EEPROM

The ATK-DLMP135 development board is equipped with an EEPROM storage chip and an I2C interface. Users can test and use it according to their own needs. The circuit for this part is shown in Figure 3.16:

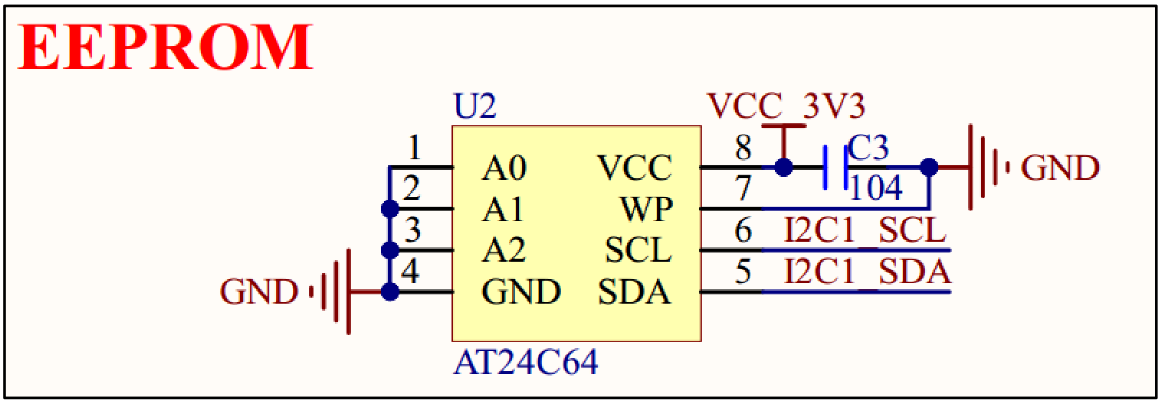


Figure 3-3-16 EEPROM circuit

3.14 SPI FLASH

The ATK-DLMP135 development board is equipped with a NOR FLASH storage chip of model W25Q128, with a SPI interface. Users can test and use it according to their own needs. The circuit is shown in Figure 3.17:

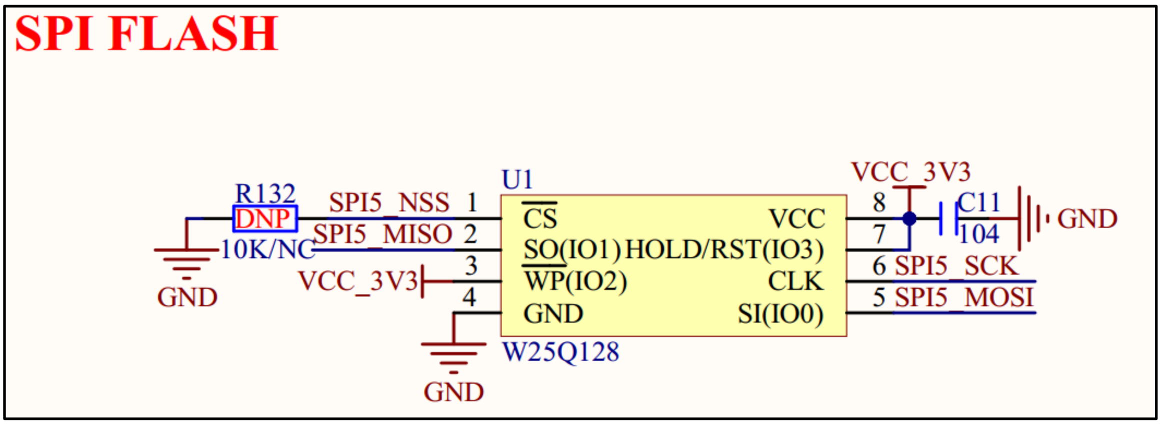


Figure 3-3-17 Six-axis sensor

3.15 LED

The ATK-DLMP135 development board is equipped with one status indicator LED, which is red and is for user control. Its schematic diagram is shown in Figure 3.18:

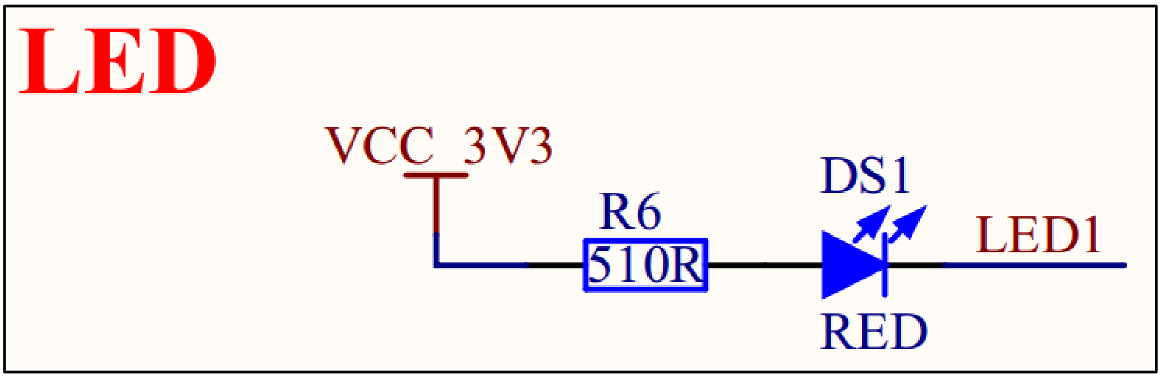


Figure 3-3-18 LED

3.16 KEY

The ATK-DLMP135 development board is equipped with one input key. Its schematic diagram is shown in Figure 3.19:

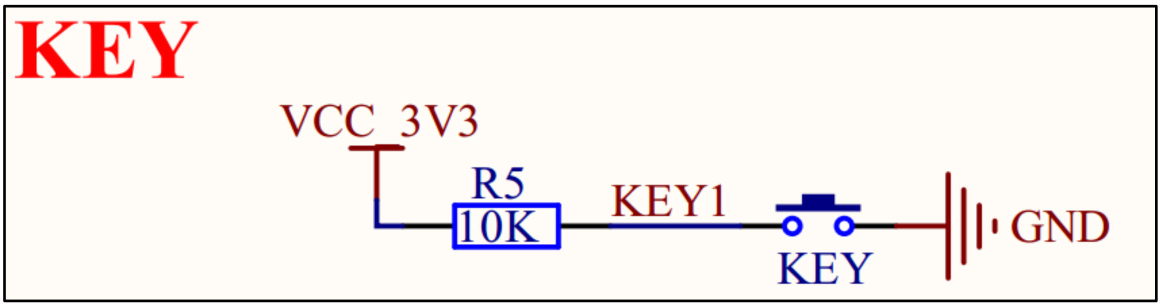


Figure 3-3-19 Input Button

This button can be used as a regular key input and is connected to the PF14 pin of the STM32MP135. This pin shares the JTCK pin. The JTCK pin internally has a 40K pull-down resistor, forming a voltage divider. If the user needs an independent JTAG debugging port, the pull-up resistor of the shared pin can be removed for testing. When designing the product board, other IOs can be used to implement the KEY button function.

3.17 Camera module interface

The ATK-DLMP135 development board is equipped with a camera module interface, which is connected to the hardware camera interface (DCMIPP) of the STM32MP135. Its schematic diagram is shown in Figure 3.20:

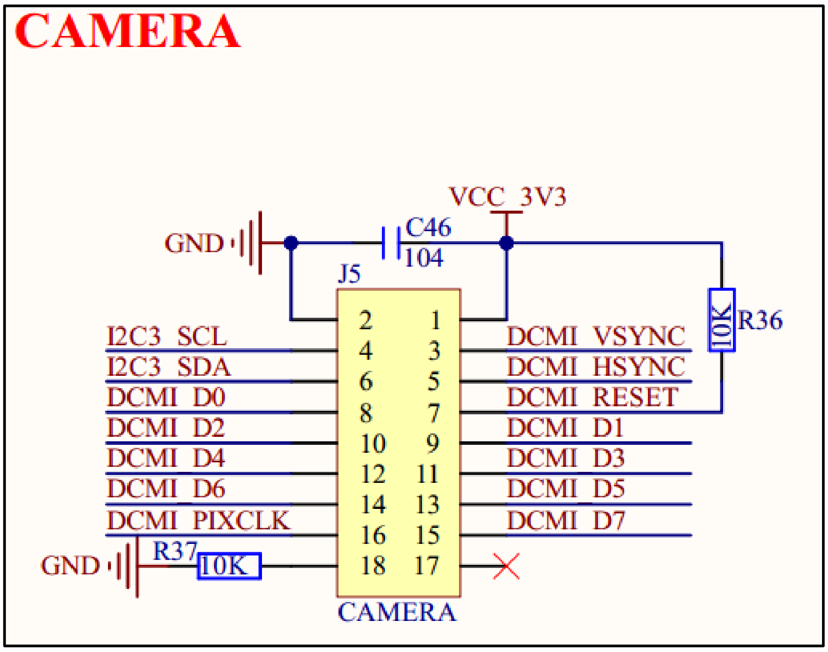


Figure 3-3-20 Camera module interface

The J5 interface in the figure can be used to connect the ALIENTEK camera module. Among them, I2C3_SCL and I2C3_SDA are the SCCB interfaces of the camera, and they are connected to the PH3 and PD7 pins of the STM32MP135. The 18th pin of this J5 interface is the PWDN pin of the

ALIENTEK OV series camera, which is the power-down mode, with a high level being effective. This development board does not use this mode and the default configuration is pull-down. If the user needs it, they can design the baseboard and configure an IO to control it. DCMI_RESET and DCMI_PWDN are two signals that do not belong to the hardware camera interface of the STM32MP135 and can be controlled by ordinary IO.

In addition, the signals such as DCMI_VSYNC/DCMI_HSYNC/DCMI_D0~DCMI_D7/DCMI_PIXCLK are connected to the hardware camera interface DCMIPP of the STM32MP135.

3.18 Active buzzer

The ATK-DLMP135 development board is equipped with an active buzzer. Its schematic diagram is shown in Figure 3.21:

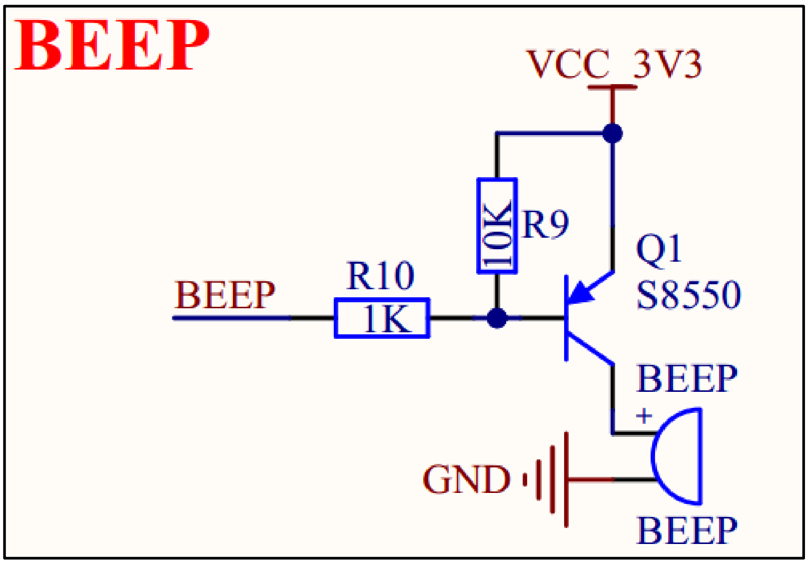


Figure 3-3-21 Active buzzer

An active buzzer refers to a buzzer that has its own oscillation circuit. Once powered on, this buzzer will start oscillating and making sound by itself. On the other hand, an inductive buzzer requires an external driving signal of a certain frequency (2-5 KHz) to produce sound. Here, we choose to use an active buzzer for ease of use.

The BEEP signal is directly connected to the PF8 pin of the STM32MP135. By controlling this pin, the switch of the buzzer can be controlled.

3.19 TF card interface

The ATK-DLMP135 development board is equipped with a TF card (small card) interface. Its schematic diagram is shown in Figure 3.22:

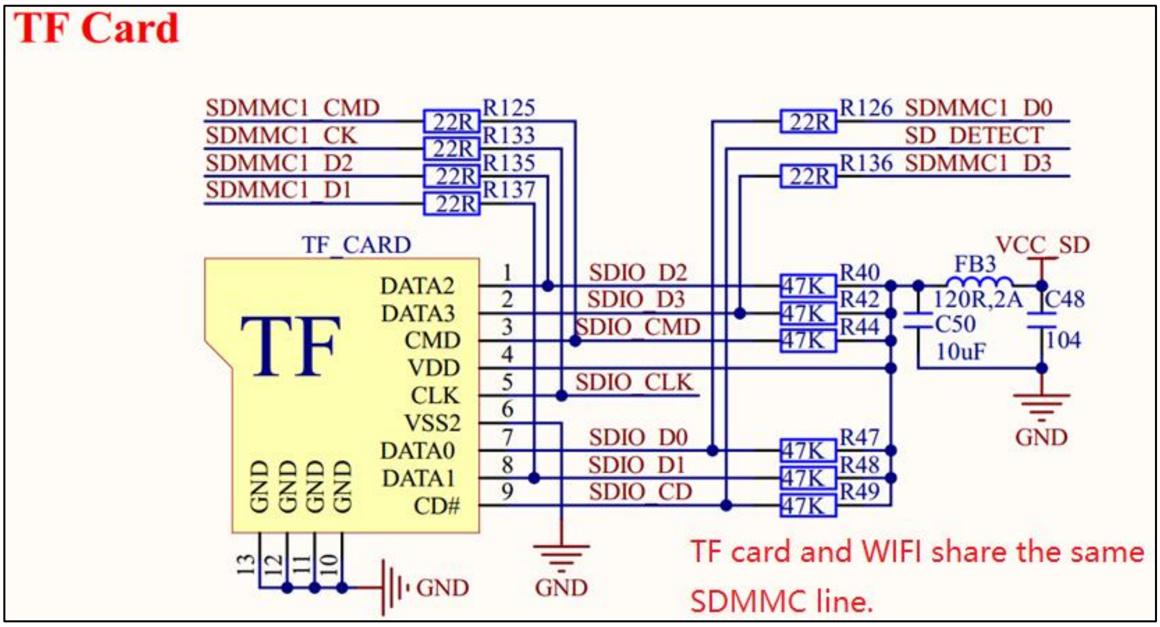


Figure 3-3-22 TF card interface

In the figure, TF_CARD represents the TF card interface. The TF card is driven using the 4-bit SDMMC method, which is very suitable for situations requiring high-speed storage. In the figure: SDMMC1_D0~D3/SDMMC1_CK/SDMMC_CMD are respectively connected to the PC8, PC9, PC10, PC11, PC12 and PD2 pins of the STM32MP135. Since the STM32MP135 only has 2 sets of SDMMC communication interfaces, one set, SDMMC2, is used for the EMMC storage chip on the core board, and the other set is connected to the baseboard. Therefore, the TF card and the SDIO WIFI module share the same SDMMC1 bus, and they cannot work simultaneously. Power switching is required. SD_DETECT is the TF card detection pin, used to detect the insertion and removal process of the TF card, and is connected to the PF15 pin of the STM32MP135.

3.20 SDIO WIFI & Bluetooth module

The ATK-DLMP135 development board is equipped with an SDIO WIFI & Bluetooth module, as shown in Figure 3.23:

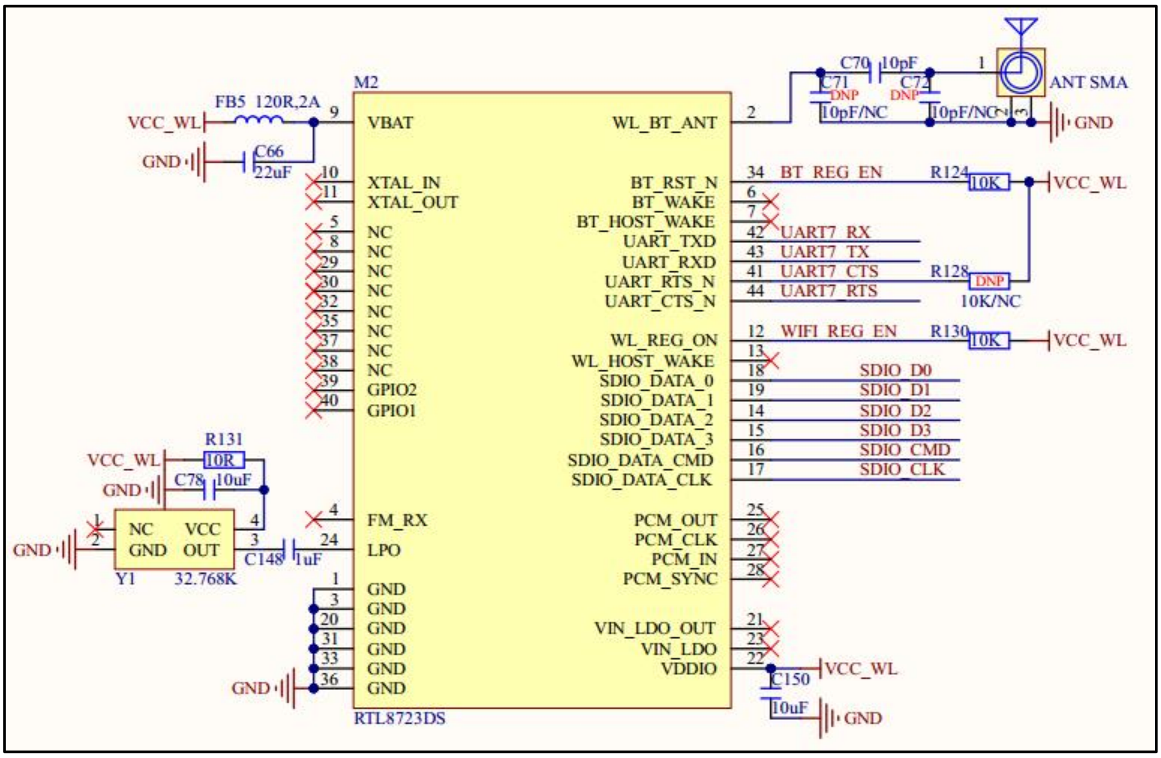


Figure 3-3-23 SDIO WIFI & Bluetooth interface

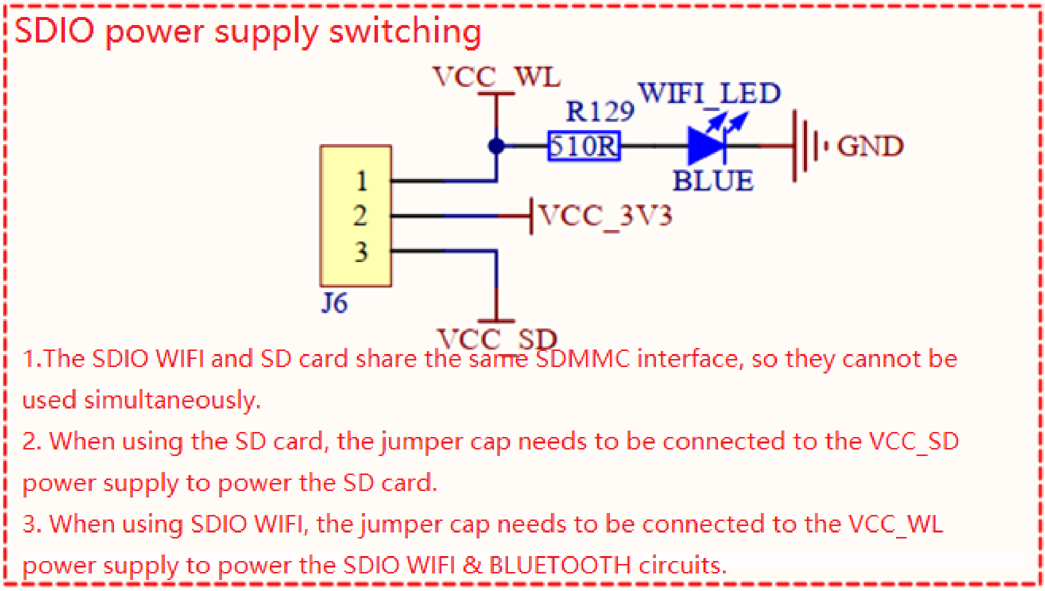


Figure 3-3-24 SDIO WIFI & Bluetooth interface

The WIFI & Bluetooth module uses RTL8723DS, which is an SDIO interface WIFI & Bluetooth module. It is connected to the SDMMC1 interface of STM32MP135 and shares the same set of interfaces with the TF card. Both cannot be used simultaneously. The development board adopts a switching power supply method, allowing users to switch between the TF card function and the WIFI & Bluetooth module.

The Bluetooth part uses the serial port. The UART_TX/UART_RX/UART_CTS/UART_RTS of the module is connected to the UART7 serial port of STM32MP135, and the corresponding pins are

PE8/PE10/PF9/PF10. BT_REG_EN and WIFI_REG_EN these two IOs are connected to the PB10 and PH5 pins of STM32MP137.

Due to the limited number of pins on the MPU, the development board did not use the BT_WAKE/BT_HOST/WAKE/WL_HOST_WAKE pins and the PCM function when trimming the pins. Users can add new controls according to their project requirements and the design specifications of the corresponding WIFI & Bluetooth module manufacturers when designing the baseboard. This circuit is for reference only.

3.21 4G module interface

The ATK-DLMP135 development board is equipped with a 4G Mini PCIE interface, as shown in Figure 3.25:

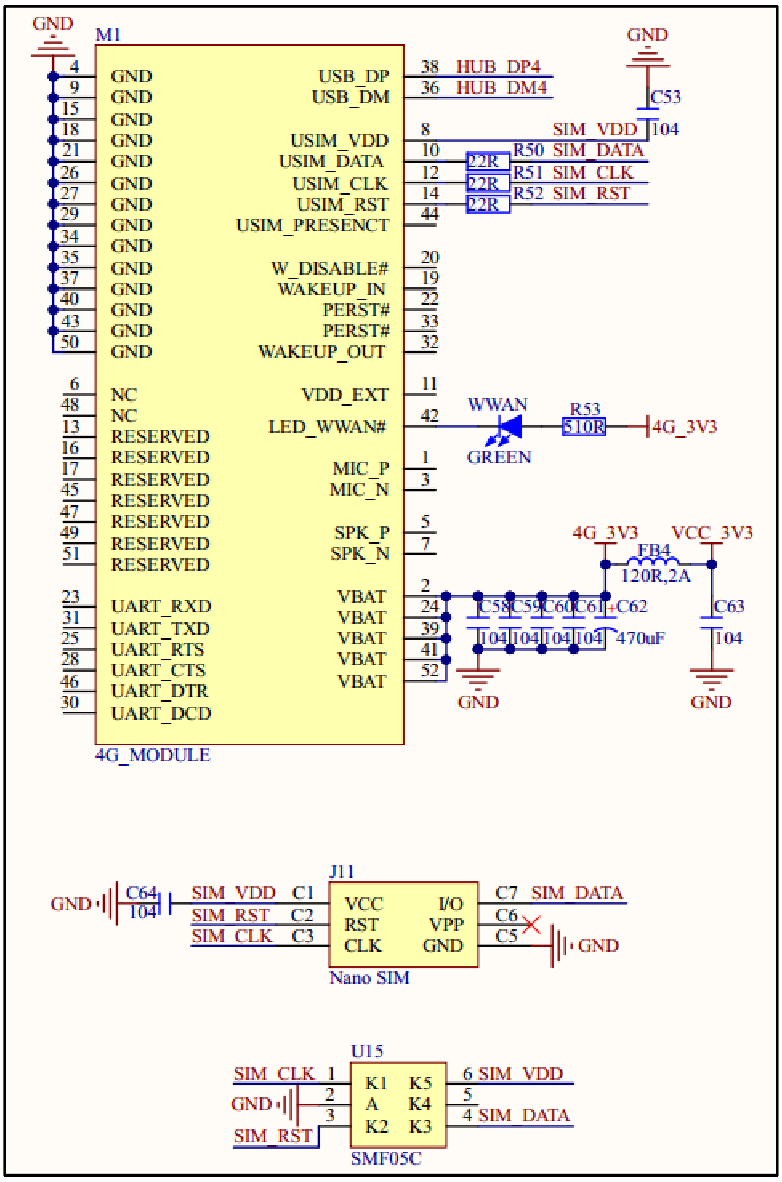


Figure 3-3-25 4G module

M1 is the 4G module socket with Mini PCIE interface, used for connecting the 4G module with Mini PCIE interface, such as the ME3630 module from Gosuncn. J11 is the Nano SIM card socket, used for inserting Nano SIM card. Although the 4G module adopts Mini PCIE interface, it actually uses the USB interface. Here, it is connected to a USB HOST interface expanded by SL2.1.

3.22 Gigabit Ethernet Interface (RJ45)

The ATK-DLMP135 development board is equipped with 2 Gigabit Ethernet interfaces (RJ45), as shown in Figure 3.26:

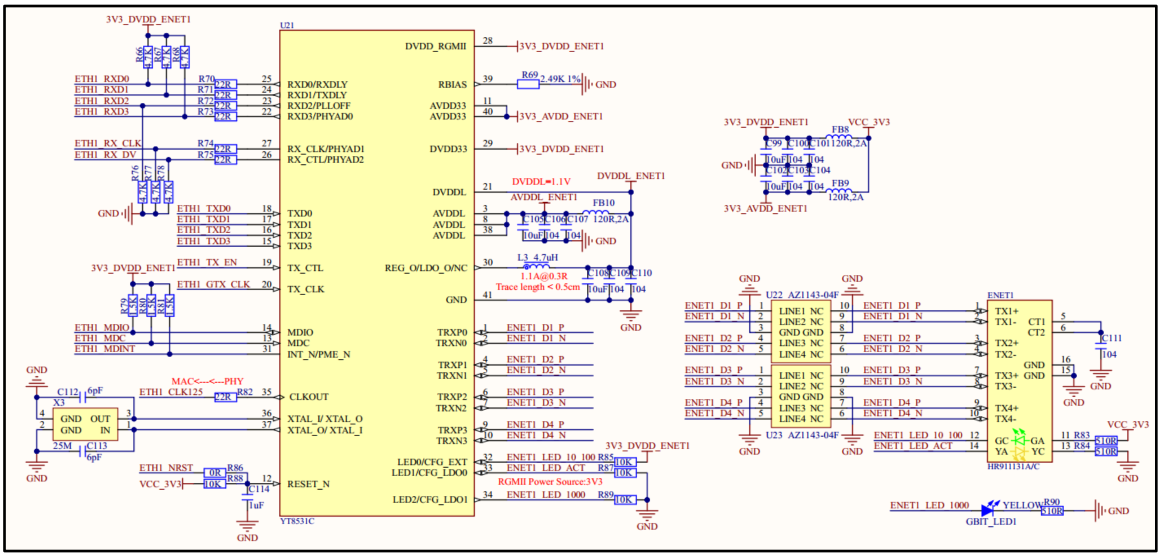


Figure 3-3-26 Gigabit Network Schematic Diagram

The example here is the schematic diagram of the ENET1 network 1. The same applies to ENET2 network 2. Please pay attention to distinguishing the network addresses. The address of network port 1 is 1, and the address of network port 2 is 2. The STM32MP135 has its own two gigabit network MAC controllers, so it can provide two gigabit network ports. The development board selects the network PHY chip model as YT8531C. GBIT_LED1 is a yellow-green LED light, controlled by ENET1_LED_1000. If the network is working at gigabit speed, this LED light will be constantly on. It is recommended to adopt a four-layer circuit board design for the gigabit network; otherwise, the two-layer circuit board fails to maintain a complete reference plane, resulting in the network speed not reaching nearly gigabit rate.

3.23 SAI Audio Codec

The ATK-DLMP135 development board is equipped with the high-performance CS42L51 audio codec chip. Its schematic diagram is shown in Figure 3.27:

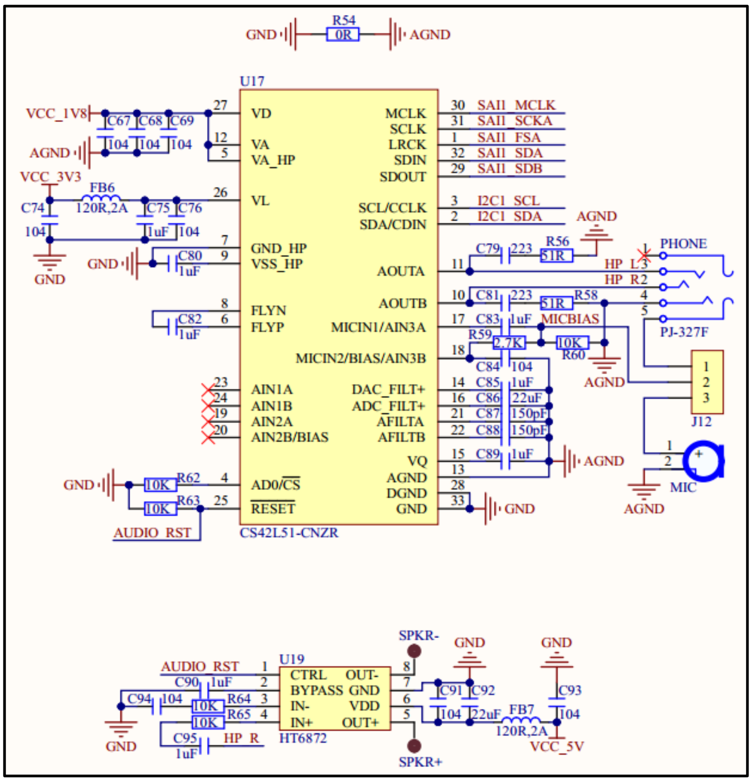


Figure 3-3-27 SAI audio codec chip

The CS42L51 is a low-power, high-performance stereo multimedia digital signal codec. This chip integrates a 24-bit high-performance DAC & ADC internally. Moreover, this chip combines the preamplification of stereo microphones and reduces the necessary external components when used, directly driving headphones (46mW 16Ω @ 1.8V or 88mW 16Ω @ 2.5V).

In Figure 3.27, HT6872 has a single-channel D-class audio power amplifier. Since the CS42L51 does not support speakers, an external speaker driver circuit is required. SPK- and SPK+ are connected to an onboard 8Ω 1W small speaker (on the back of the development board). There are two microphone options: one is the built-in MIC of the headphones, and the other is the onboard microphone. These two can only be chosen from two options, and the selection is made through the J12 jumper cap. PHONE is a four-section 3.5mm headphone output interface that can be used to plug in headphones.

This chip uses the SAI interface to connect with STM32MP135. In the figure: SAI1_MCLK/SAI1_SCKA/SAI2_FSA/SAI1_SDA/SAI1_SDB/ are connected to STM32MP135's: PC3/PA4/PF11/PA5/PA0 respectively.

The CS42L51 requires an I2C interface for configuration. Here, I2C1 of STM32MP135 is used, and I2C1_SCL and I2C1_SDA are connected to the PD12 and PD3 pins of STM32MP135 respectively.

3.24 Power supply

The power supply section onboard the ATK-DLMP135 development board, as shown in the schematic diagram in Figure 3.28:

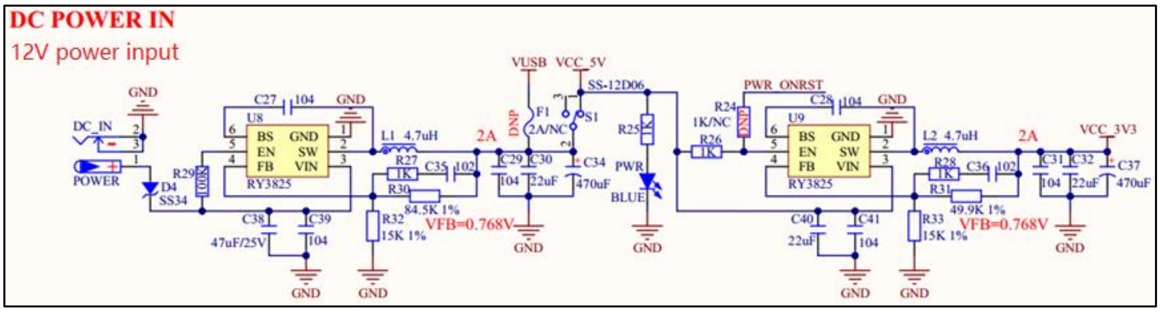


Figure 3-3-28 Power supply

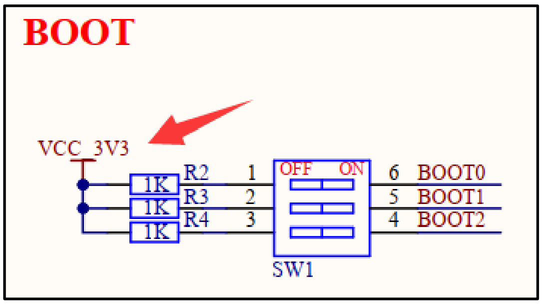


Figure 3-3-29 BOOT startup mode power supply

There are two DCDC power chips in the figure, namely U8 and U9. DC_IN is used for the input of an external DC12V DC power supply, which is converted to a 5V power output by the U8 DCDC chip and supplies power to the core board and other circuits. Among them, D4 is a reverse connection prevention diode, which prevents the development board from being burned out when the polarity of the external DC power supply is incorrect. S1 is the total power switch of the development board, and F1 is a 2A self-recovery fuse, which is used to protect USB. Here, a USB-powered development board is not used. U9 is an output 3.3V DCDC chip, which provides 3.3V power to the development board.

Please note one point here. Since the U9 power chip on the baseboard outputs VCC_3V3 to power the BOOT jumper switch, which involves the selection of the MPU startup mode, the baseboard must establish the output of 3.3V high level (VCC_3V3) by U9 power chip as soon as possible (within 3ms) after the VCC_5V power supply is provided to the core board, so that the MPU can read the corresponding BOOT startup mode to start the system. The development board directly inputs the U9 enable EN pin through R26 resistor to achieve the output of VCC_3V3 from U9 power.

Let me emphasize again, the U9 power chip is a 5V to 3.3V power conversion chip. When selecting the DCDC chip, you must choose a power chip with a soft start time of less than 2ms. Only in this way can the MPU read the correct BOOT startup level after the VCC_5V power supply core board is powered on.

3.25 Power input and output interface

The ATK-DLMP135 development board is equipped with two sets of simple power input and output interfaces. The schematic diagram is shown in Figure 3.30:

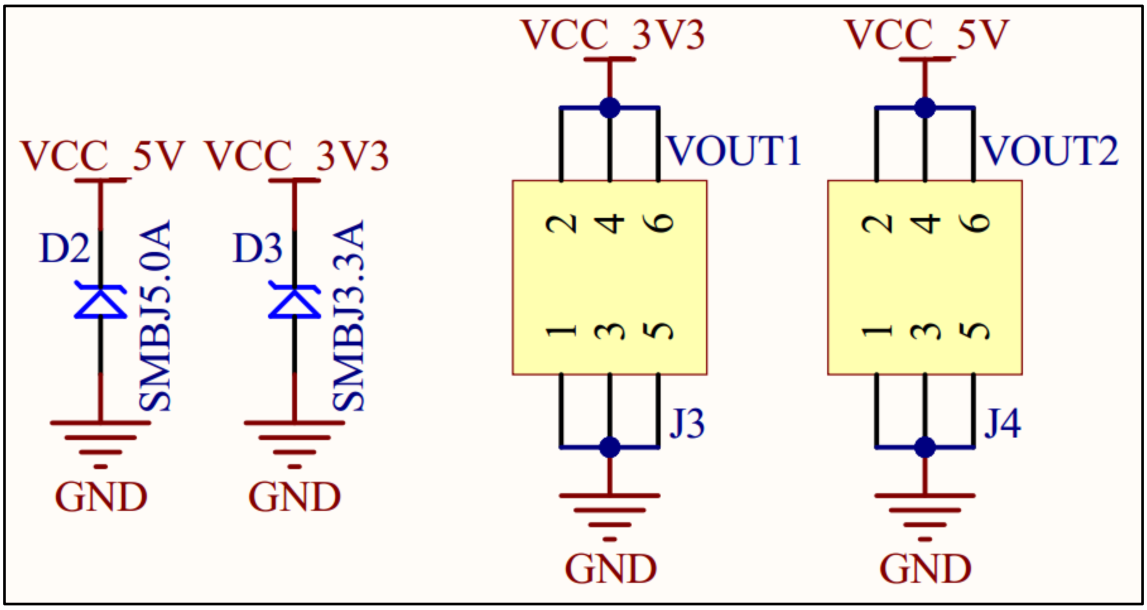


Figure 3-3-30 Power supply

In the figure, VOUT1 and VOUT2 are the input and output interfaces for 3.3V and 5V power supplies respectively. With these two sets of interfaces, we can provide 3.3V and 5V power to the external devices through the development board. Although the power is not very large (maximum 1000mA), it is sufficient for most cases. When you are debugging your own small circuit boards, having these two sets of power supplies is quite convenient.

In the figure, D2 and D3 are TVS diodes, which can effectively prevent damage to the development board when the external power supply/load is unstable (especially when the development board is connected to inductive loads such as motors, relays, or solenoid valves). At the same time, it can also prevent damage to the development board caused by the reverse connection of the external power supply to a certain extent.

3.26 USB serial port (Type-C interface)

The ATK-DLMP135 development board is equipped with a USB serial port. Its schematic diagram is shown in Figure 3.31:

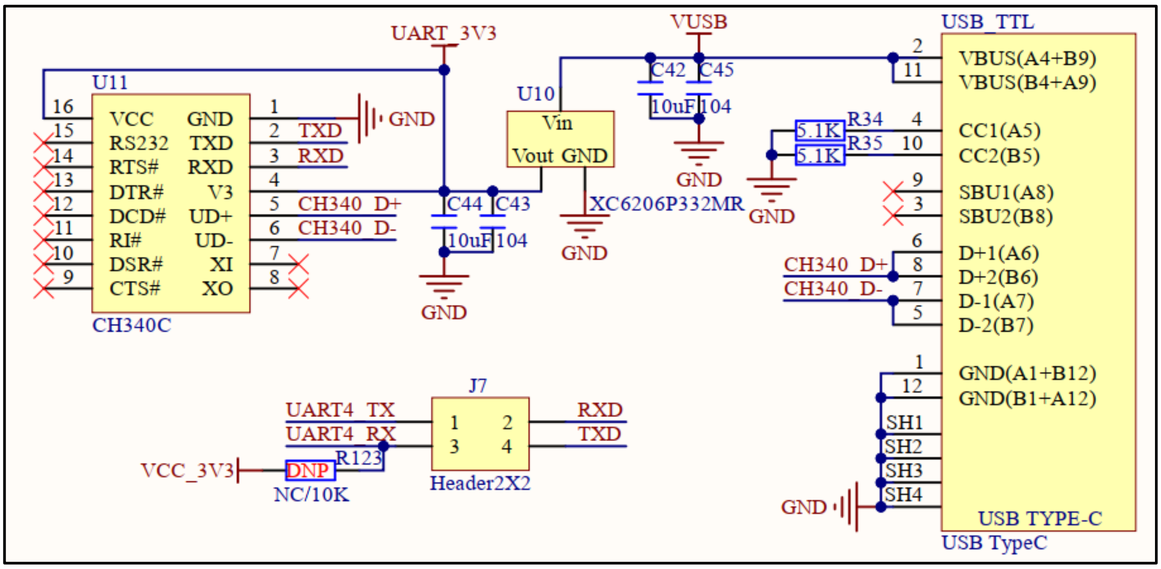


Figure 3-3-31 USB serial port

USB to Serial Port Converter, the development board selected is CH340C. CH340C has an internal crystal, so there is no need to connect an external crystal. As can be seen from the figure, the power supply of CH340C is 3.3V and it is independently powered. U10 is an LDO chip, responsible for providing 3.3V power to CH340C. The power supply of CH340C is not controlled by the power switch of the development board. As long as the USB cable is connected, CH340 will power on. In the figure, RXD/TXD is connected to J7's RXD/TXD, which are the serial port receiving and transmitting pins of the CH340 chip, and can be connected to the serial port 4 of STM32MP135 through the jumper cap.

3.27 JTAG Interface

The ATK-DLMP135 development board is equipped with a 10-pin, 2.0mm pitch JTAG interface. The schematic diagram is shown in Figure 3.32:

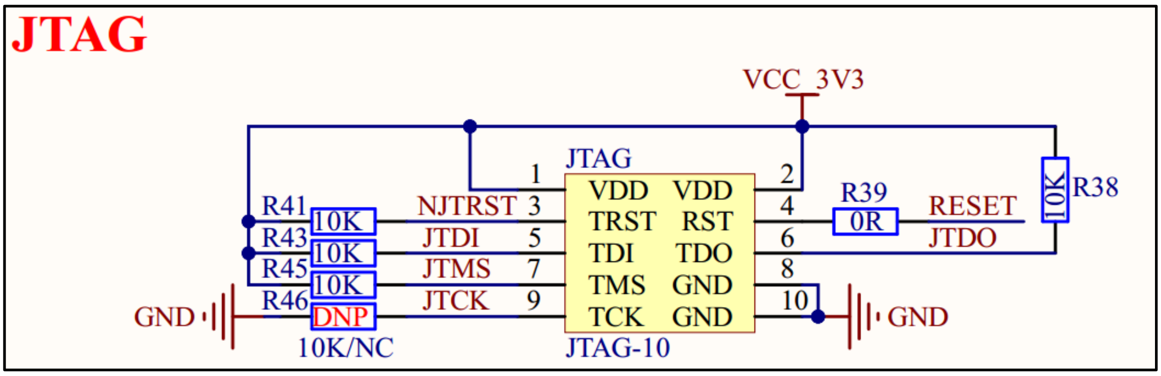


Figure 3-3-32 JTAG interface

The development board uses some of the JTAG pins as regular GPIOs and shares them with other functions. They cannot be used simultaneously. If the user requires a separate JTAG circuit, the JTAG pins can be retained and not shared with other function pins when designing the base board. The JTAG pins have built-in pull-up resistors (30-50K), so external pull-up resistors can be omitted.

When the user needs to use the JTAG interface for debugging, they need to switch the BOOT boot mode B2 to a high level, B1 and B0 to a low level, which is the development boot mode.

3.28 Adjustable resistor

The ATK-DLMP135 development board is equipped with an adjustable resistor, which is used to complete the ADC acquisition experiment. The circuit is shown in Figure 3.33:

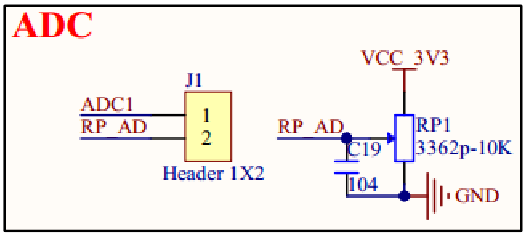


Figure 3-3-33 Adjustable resistor

In Figure 2.33, RP1 is a 10K adjustable resistor, and RP_AD is a tap. It can be connected to ADC1 through J1, and ADC1 is connected to the PC0 pin of STM32MP135, enabling AD acquisition. If the ADC function is not needed, the PC0 pin can be re-used for other functions.

3.29 ADC reference voltage VREF+

The ATK-DLMP135 development board uses an LDO to provide the ADC reference voltage. The circuit is shown in Figure 3.34:

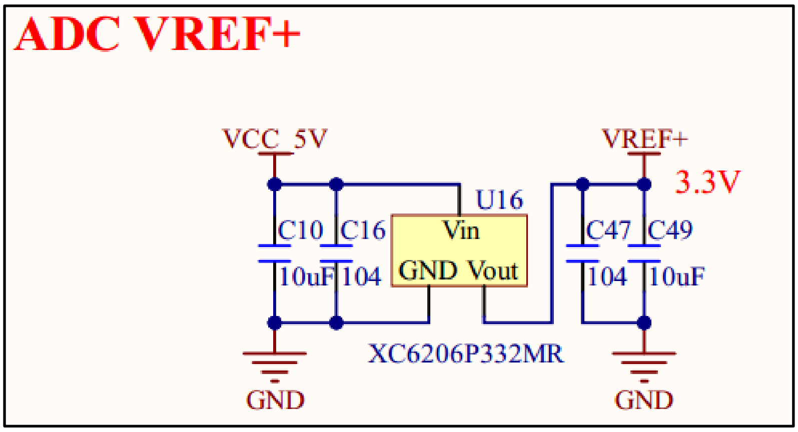


Figure 3-3-34 ADC reference voltage

The LDO model used in the development board is XC6206P332MR, which provides a 3.3V voltage supply to ADC VREF+ for normal use of the ADC function. Users can use other LDOs to provide the ADC VREF+ reference voltage, but note that it should not exceed 3.3V. The VDDA on the core board is 3.3V-powered.

3.30 HDMI interface

The ATK-DLMP135 development board is equipped with an HDMI interface, which is an RGB to HDMI interface and is essentially still an RGB interface. The schematic diagram is shown in Figure 3.35:

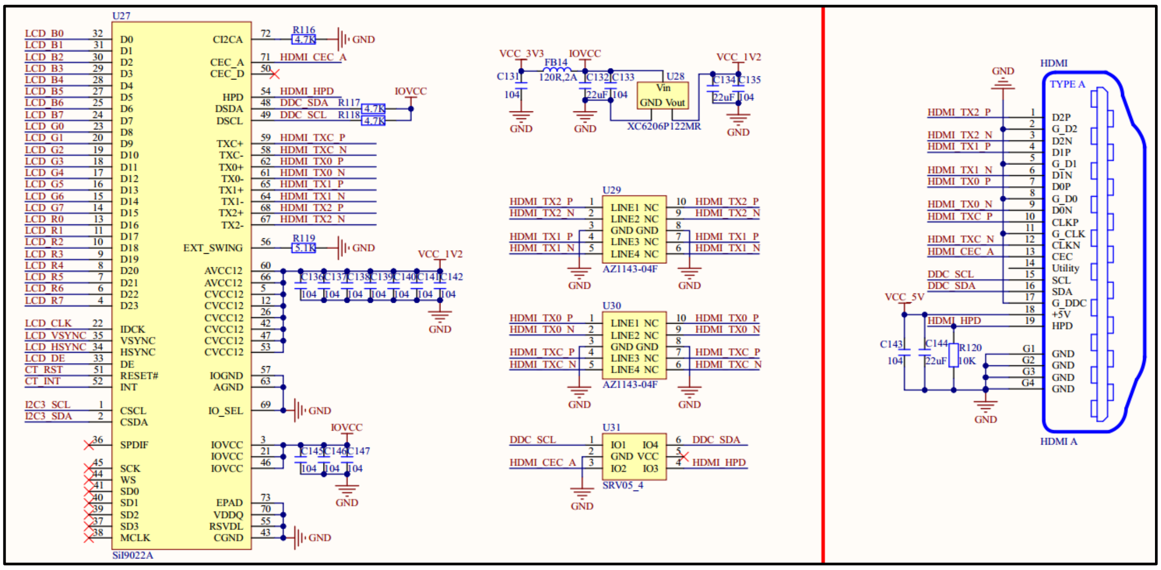


Figure 3-3-35 HDMI schematic diagram

In Figure 3.35, the Sil9022A on the left is an RGB to HDMI chip, and the one on the right is an HDMI socket. Since it is an RGB to HDMI conversion, the RGB screen and HDMI cannot work simultaneously; only one of them can be used at a time.

Chapter 4. ATK-CLMP135B Core Board Schematic Diagram Explanation

4.1 SOC

The ATK-CLMP135B core board, which is provided with the ATK-DLMP135 development board, uses STM32MP135DAE7 as the main control CPU, with a single-core A7, up to 1GHz main frequency. This SOC comes with 32KB of L1 instruction and data Cache, 128KB of L2 Cache, integrates NEON and TrustZone, integrates a double-precision hardware floating-point calculation unit VFPv4, and has 168KB SRAM, 2 advanced timers, 10 general timers, 2 basic timers, 5 low-power timers, 2 watchdogs, 1 FMC interface, 1 QUADSPI interface, 2 ADC peripherals, 1 embedded digital temperature sensor, 1 DFSDM peripheral, 1 DCMIPP interface, 1 RGB LCD controller (LTDC), 1 embedded RTC, 8 UART/USART, 5 SPI, 5 I2C, 2 SAI, 4 SPDIFRX input channels, 2 gigabit network MAC controllers, 2 USB controllers, 2 SDMMC interfaces, 2 FDCAN interfaces, etc.

The schematic diagram of the SOC part is shown in Figures 4.1 to 4.5 (please open the schematic diagram of the development board materials for viewing):

Figure 4-1 Schematic diagram of the SOC section 1

Figure 4-2 Schematic diagram of the SOC section 2

Figure 4-3 Schematic diagram of the SOC section 3

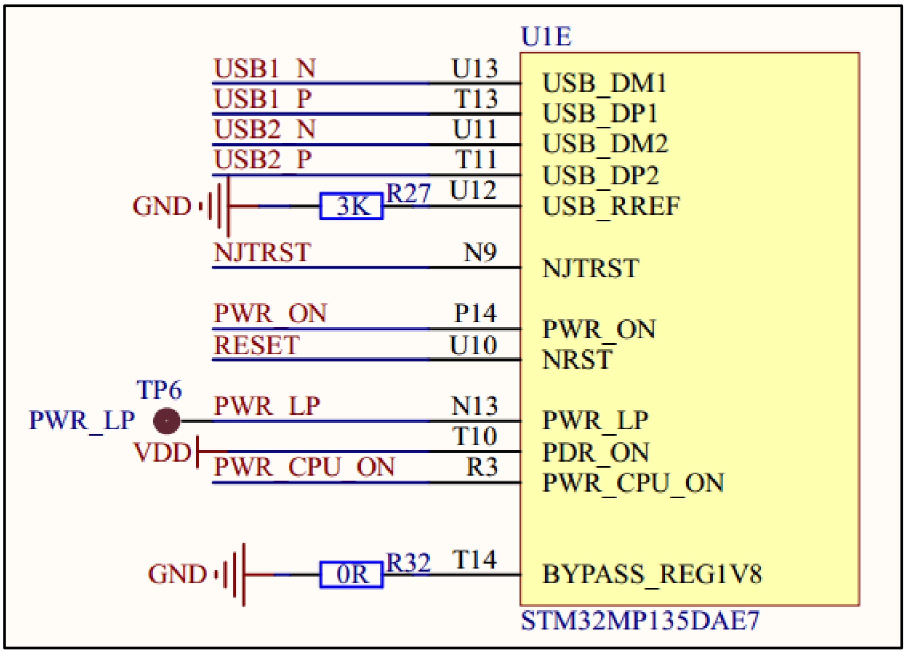


Figure 4-4 Schematic diagram of the SOC section 4

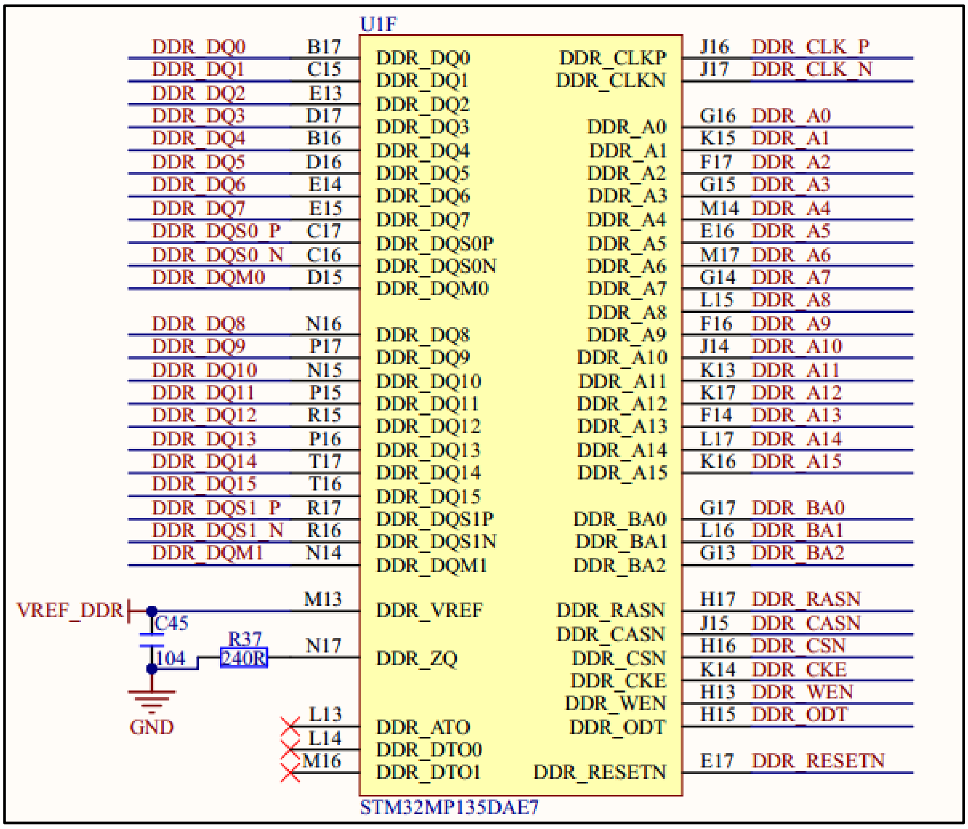


Figure 4-5 Schematic diagram of the SOC section 5

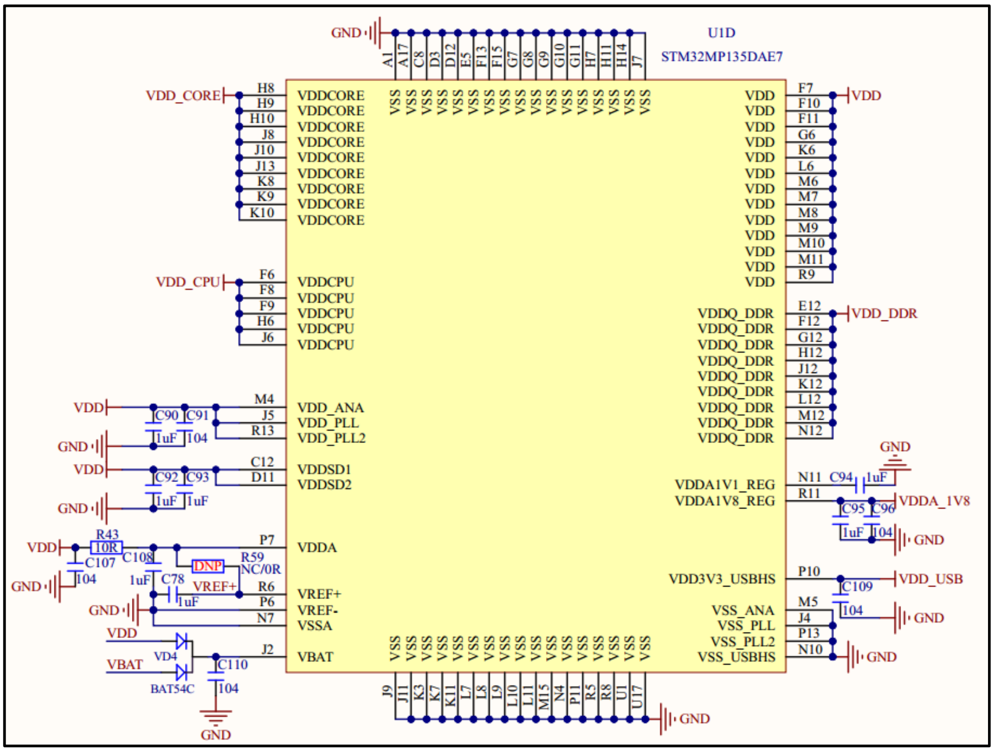


Figure 4-6 Schematic diagram of the SOC section 6

The schematic diagram of the STM32MP135 chip consists of six parts. Let's take a look at the specific contents of each of these six parts one by one:

Figure 4.1: This part of the schematic diagram mainly shows the IO schematic of GPIOA~C in the STM32MP135.

Figure 4.2: This part of the schematic diagram mainly shows the IO schematic of GPIOD~F in the STM32MP135.

Figure 4.3: This part of the schematic diagram mainly shows the IO schematic of GPIOG~I in the STM32MP135.

Figure 4.4: This part of the schematic diagram mainly shows the pins such as USB and power control in the STM32MP135.

Figure 4.5: This part of the schematic diagram is the DDR pins of the STM32MP135.

Figure 4.6: This part of the schematic diagram is the power section of the STM32MP135.

4.2 BTB interface

The ATK-CLMP135B core board uses two 2*40 3710F (female connector) board-to-board connectors to connect with the baseboard (on the bottom surface). The connection is very convenient. The schematic diagram of the baseboard interface on the core board is shown in Figure 4.7:

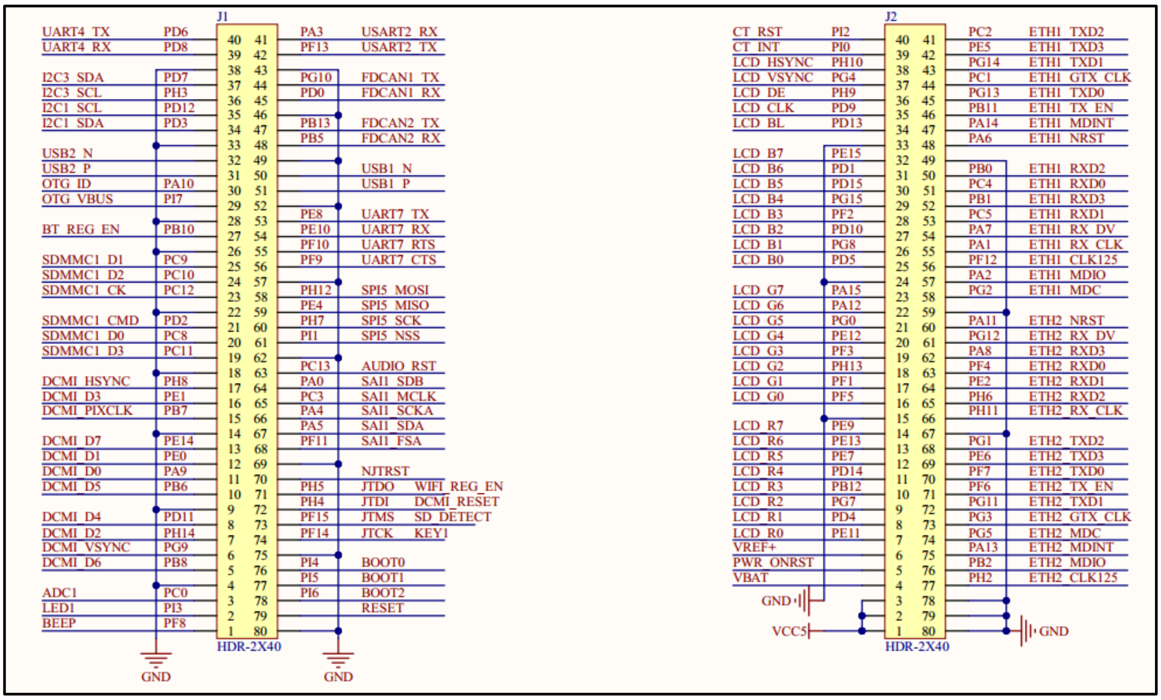


Figure 4-7 Bottom plate interface

In the figure, JP1 and JP2 are two 2*40 board-to-board motherboards (3710F), which are very convenient for connecting to the bottom plate and facilitating the embedding of your own projects. This interface provides a total of 121 I/O ports. Additionally, there are USB, power supply, reset, VREF+ and other signals.

4.3 EMMC

The ATK-CLMP135B core board is equipped with 8GB of EMMC. The circuitry for this part is shown in Figure 4.8:

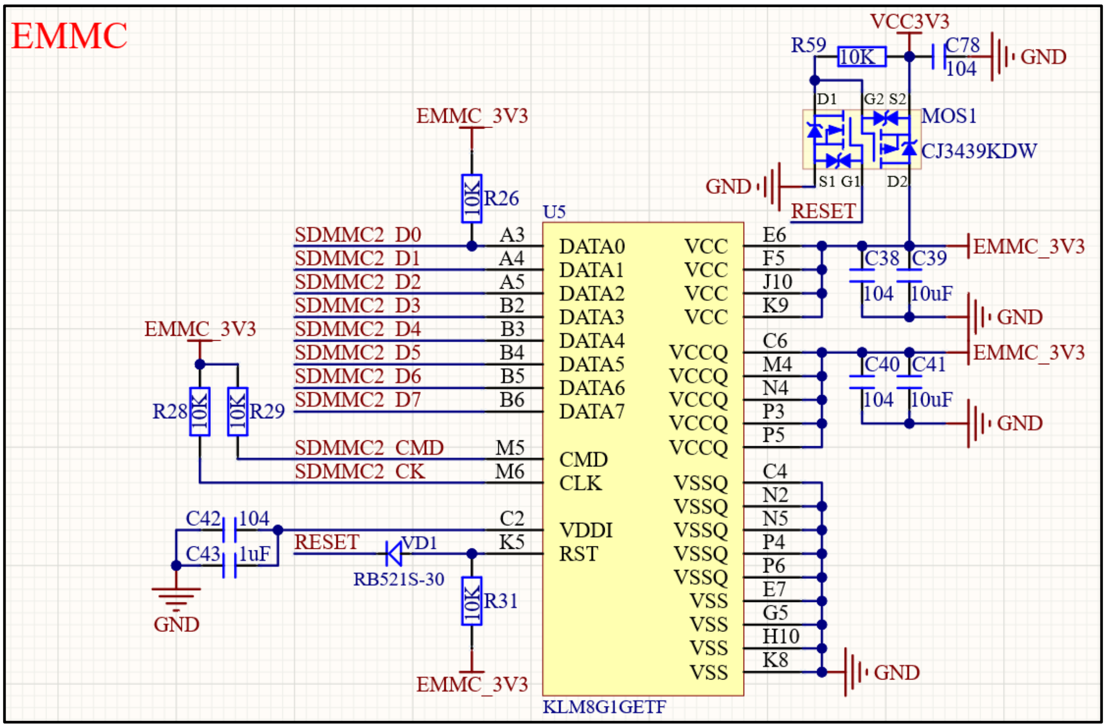


Figure 4-8 EMMC circuit

EMMC is also a type of storage Flash. Compared to NAND Flash, EMMC is simpler to use (similar to SD), has a faster speed, and a higher capacity. Currently, EMMC has gradually replaced NAND Flash, especially in the fields of mobile phones and tablets.

4.4 DDR3L

The ATK-CLMP135B core board is equipped with 512MB DDR3L. The circuitry for this part is shown in Figure 4.9:

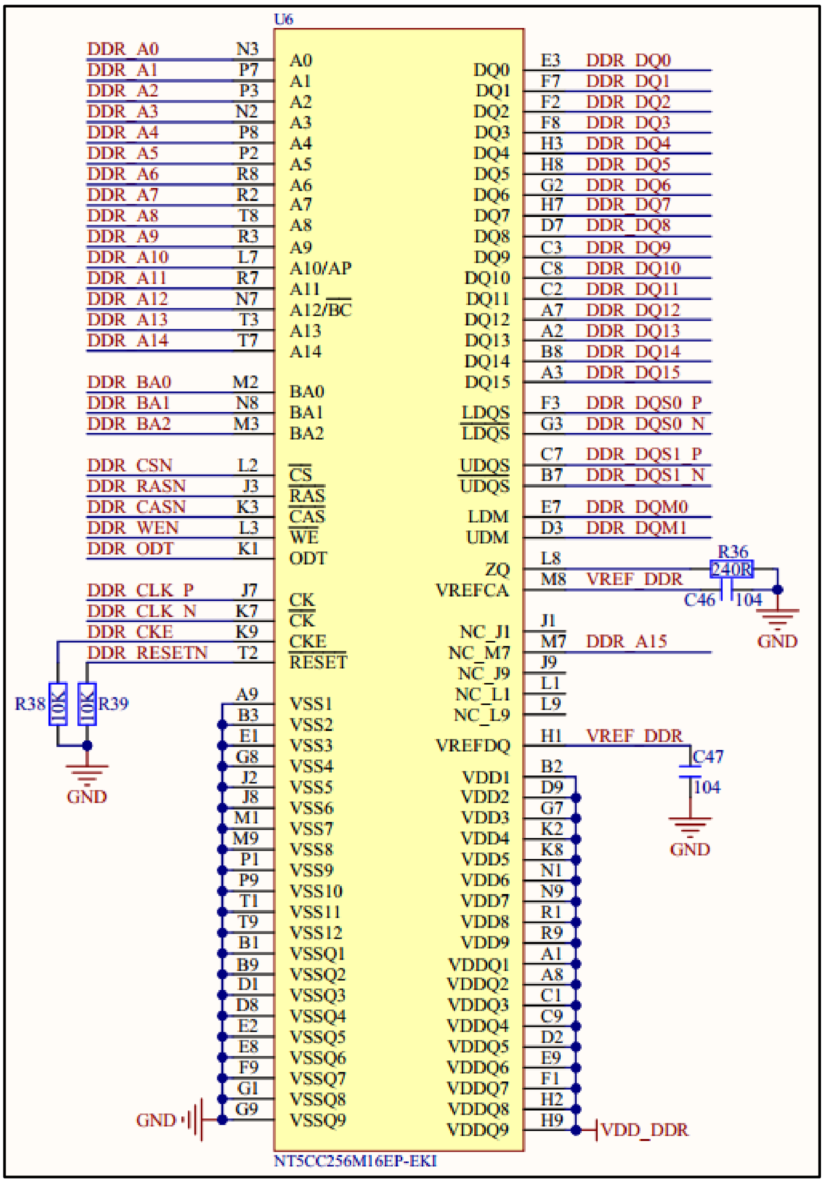


Figure 4-9 DDR3L

4.5 Core board power supply

The power supply for the ATK-CLMP135B core board is mainly divided into 5 parts: VDD power supply, VCC3V3 power supply, VDD_CORE power supply, VDD_DDR power supply, and VDD_CPU power supply. The entire core board power supply is shown in Figure 4.10:

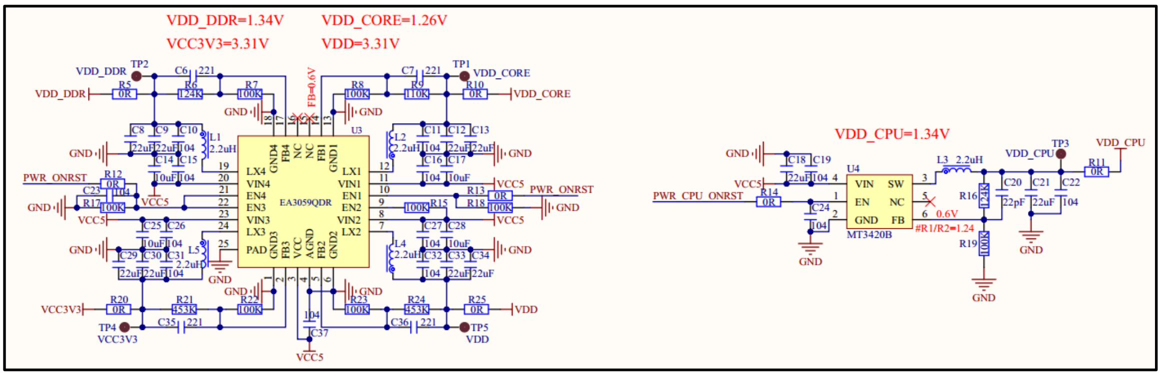


Figure 4-10 Core board power supply

Chapter 5. Development Board Usage Tips

In order to enable everyone to use the ALIENTEK STM32MP135 development board more effectively, we have summarized here some issues that you should pay special attention to when using this development board. Please pay close attention to these issues during use to avoid unnecessary problems.

① When you want to use a certain I/O port for other purposes, please first check the schematic diagram of the development board to see if this I/O port is connected to any peripheral on the development board. If so, whether the signal of this peripheral will cause interference to your use. Make sure there is no interference first, then use this I/O port.

② There are many jumpers on the development board. When using a certain function, please first check if this requires setting the jumper. This can save time.

③ When the LCD display is blank, please first check if the LCD module is properly plugged in (try unplugging and re-plugging). Check if the FPC connector interface is damaged, etc.

④ When you need to remove the adapter board from the base board, please shake it left and right to remove it. Do not shake it too vigorously, otherwise it may damage the socket.

So far, the hardware part of the experimental platform (the ALIENTEK STM32MP135 development board) of this manual has been introduced. Understanding the entire hardware will be very helpful for our subsequent learning, helping to understand the subsequent code， and making it easier to write software. Please read it carefully！ In addition， other materials and tutorials of the ALIENTEK development board can be downloaded from the technical forum. You can frequently go to this forum to obtain updated information.

If there are any errors in the compilation of this manual， please contact for correction.