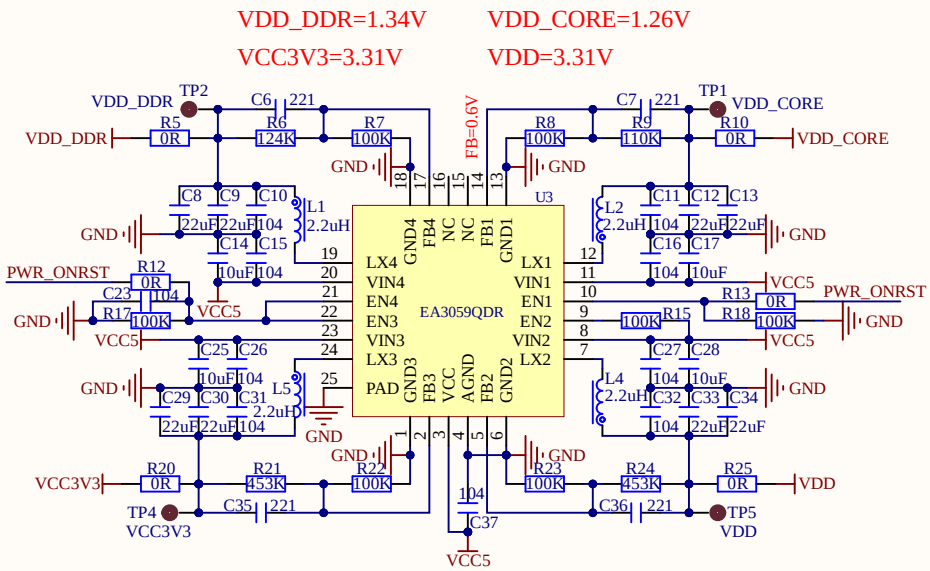
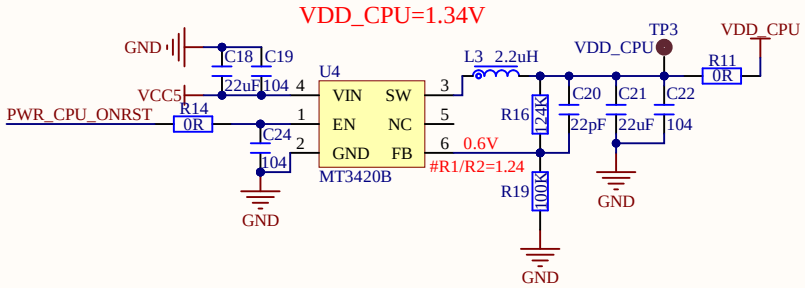




Title: STM32MP135_CORE_POWER.SchDoc		
Project: STM32MP135_CORE.PrjPcb		
Size: A4	Author: ALIENTEK	
Date: 2023/3/31	Version: V1.0	Sheet: 1 of 8

正点原子

Title: STM32MP135_CPU_ABC.SchDoc			
Project: STM32MP135_CORE.PrjPcb			
Size: A4	Author: ALIENTEK		
Date: 2023/3/31	Version: V1.0	Sheet: 2 of 8	

正点原子

U1B

FDCAN1_RX		E4
LCD_B6		D5
SDMMC1_CMD		A15
I2C1_SDA		B1
LCD_R1		E7
LCD_B0		A6
UART4_TX		D2
I2C3_SDA		N3
UART4_RX		C5
LCD_CLK		E8
LCD_B2		A3
DCMI_D4		E2
I2C1_SCL		C6
LCD_BL		J1
LCD_R4		B3
LCD_B5		C7
DCMI_D1		D6
DCMI_D3		B5
ETH2_RXD1		L1
SDMMC2_CK		D13
SPI5_MISO		H5
ETH1_TXD3	R49 22R	T9
ETH2_TXD3	R50 22R	N1
LCD_R5		A5
UART7_TX		A7
LCD_R7		B6
UART7_RX		B8
LCD_R0		D4
LCD_G4		B4
LCD_R6		C4
DCMI_D7		C3
LCD_B7		D8
SDMMC2_D4		C13
LCD_G1		B9
LCD_B3		E9
LCD_G3		B10
ETH2_RXD0		L2
LCD_G0		B2
ETH2_TX_EN	R51 22R	G2
ETH2_TXD0	R52 22R	M1
BEEP		G5
UART7_CTS		G1
UART7_RTS		G3
SAI1_FSA		T6
ETH1_CLK125		T4
USART2_TX		N6
JTCK		P4
JTMS		R10

PD0/SAI1_MCLK_A/SAI1_CK1/FDCAN1_RX/FMC_D2(boot)/FMC_AD2/DCMIPP_D1
PD1/I2C5_SCL/SPI4_MOSI/I2S4_SDO/UART4_TX/QUADSPI_BK1_NCS/LCD_B6/FMC_D3(boot)/FMC_AD3/DCMIPP_D13/LCD_G2
PD2/TRACED4/TIM3_ETR/I2C1_SMBA/SPI3_NSS/I2S3_WS/SAI2_D1/USART3_RX/SDMMC1_CMD(boot)
PD3/TIM2_CH1/TIM2_ETR/USART2_CTS/USART2_NSS/DFSDM1_CKOUT/I2C1_SDA/SAI1_D3/FMC_CLK/DCMIPP_D5
PD4/USART2_RTS/USART2_DE/SPI3_MISO/I2S3_SDI/DFSDM1_CKIN0/QUADSPI_CLK/LCD_R1/FMC_NOE(boot)/LCD_R4/LCD_R6
PD5/QUADSPI_BK1_IO0/FMC_NWE(boot)/LCD_B0/LCD_G4
PD6/TIM16_CH1N/SAI1_D1/SAI1_SD_A/UART4_TX(boot)/DCMIPP_D4/DCMIPP_D0
PD7/MCO1/USART2_CK/I2C2_SCL/I2C3_SDA/SPDIFRX_IN0/ETH1_MII_RX_CLK/ETH1_RGMII_RX_CLK/ETH1_RMII_REF_CLK/QUADSPI_BK1_IO2/FMC_NE1
PD8/USART2_TX/I2S4_WS/USART3_TX/UART4_RX(boot)/DCMIPP_D9/DCMIPP_D3
PD9/TRACECLK/DFSDM1_DATIN3/SDMMC2_CDIR/LCD_B5/FMC_D14(boot)/FMC_AD14/LCD_CLK/LCD_B0
PD10/RTC_REFIN/I2C5_SMBA/SPI4_NSS/I2S4_WS/USART3_CK/LCD_G5/LCD_B7/FMC_D15(boot)/FMC_AD15/DCMIPP_VSYNC/LCD_B2
PD11/LPTIM2_IN2/I2C4_SMBA/USART3_CTS/USART3_NSS/SPDIFRX_IN0/QUADSPI_BK1_IO2/ETH2_RGMII_CLK125/LCD_R7/FMC_CLE(boot)/FMC_A16/UART7_RX/DCMIPP_D4
PD12/LPTIM1_IN1/TIM4_CH1/I2C1_SCL/USART3_RTS/USART3_DE/FMC_ALE(boot)/FMC_A17/DCMIPP_D6
PD13/LPTIM2_ETR/TIM4_CH2/TIM8_CH2/SAI1_CK1/SAI1_MCLK_A/USART1_RX/QUADSPI_BK1_IO3/QUADSPI_BK2_IO2/FMC_A18/LCD_G4
PD14/TIM4_CH3/I2C3_SDA/USART1_RX/UART8_CTS/FMC_D0(boot)/FMC_AD0/DCMIPP_D8/LCD_R4
PD15/USART2_RX/TIM4_CH4/DFSDM1_DATIN2/QUADSPI_BK1_IO3/FMC_D1(boot)/FMC_AD1/LCD_B5

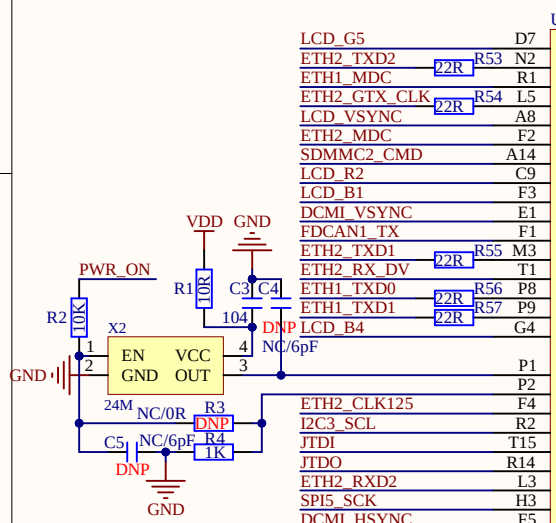
PE0/DCMIPP_D12/UART8_RX(boot)/FDCAN2_RX/LCD_B1/FMC_A11/DCMIPP_D1/LCD_B5
PE1/LPTIM1_IN2/UART8_TX(boot)/LCD_HSYNC/LCD_R4/FMC_NBL1/DCMIPP_D3/DCMIPP_D12
PE2/TRACECLK/TIM2_CH1/TIM2_ETR/I2C4_SCL/SPI5_MOSI/SAI1_FS_B/USART6_RTS/USART6_DE/SPDIFRX_IN1/ETH2_MII_RXD1/ETH2_RGMII_RXD1/ETH2_RMII_RXD1/FMC_A23/LCD_R1
PE3/TRACED11/SAI2_D4/TIM15_BKIN/SPI4_MISO/I2S4_SDI/USART3_RTS/USART3_DE/FDCAN1_RX/SDMMC2_CK(boot)/LCD_R4
PE4/SPI5_MISO/SAI1_D2/DFSDM1_DATIN3/TIM15_CH1N/I2S_CKIN/SAI1_FS_A/UART7_RTS/UART7_DE/UART8_TX/QUADSPI_BK2_NCS/FMC_NCE2/FMC_A25/DCMIPP_D3/LCD_G7
PE5/SAI2_SCK_B/TIM8_CH3/TIM15_CH1/UART4_RX/ETH1_MII_TXD3/ETH1_RGMII_TXD3/FMC_NE1
PE6/MCO2/TIM1_BKIN2/SAI2_SCK_B/TIM15_CH2/I2C3_SMBA/SAI1_SCK_B/UART4_RTS/UART4_DE/ETH2_MII_TXD3/ETH2_RGMII_TXD3/FMC_A22/DCMIPP_D7/LCD_G3
PE7/TIM1_ETR/LPTIM2_IN1/UART5_TX/FMC_D4(boot)/FMC_AD4/LCD_B3/LCD_R5
PE8/TIM1_CH1N/DFSDM1_CKIN2/I2C1_SDA/UART7_TX/FMC_D5(boot)/FMC_AD5
PE9/TIM1_CH1/QUADSPI_BK1_IO1/LCD_HSYNC/FMC_D6(boot)/FMC_AD6/DCMIPP_D7/LCD_R7/HDP3
PE10/TIM1_CH2N/UART7_RX/FDCAN1_TX/FMC_D7(boot)/FMC_AD7
PE11/TIM1_CH2/USART2_CTS/USART2_NSS/SAI1_D2/SPI4_MOSI/I2S4_SDO/SAI1_FS_A/USART6_CK/LCD_R0/ETH2_MII_TX_ER/ETH1_MII_TX_ER/FMC_D8(boot)/FMC_AD8/DCMIPP_D10/LCD_R5
PE12/TIM1_CH3N/SPI4_SCK/I2S4_CK/UART8_RTS/UART8_DE/LCD_VSYNC/LCD_G4/FMC_D9(boot)/FMC_AD9/DCMIPP_D11/LCD_G6/HDP4
PE13/TIM1_CH3/I2C5_SDA/SPI4_MISO/I2S4_SDI/LCD_B1/FMC_D10(boot)/FMC_AD10/DCMIPP_D4/LCD_R6
PE14/TIM1_BKIN/SAI1_D4/UART8_RTS/UART8_DE/QUADSPI_BK1_NCS/QUADSPI_BK2_IO2/FMC_D11(boot)/FMC_AD11/DCMIPP_D7/LCD_G0/TAMP_IN6
PE15/TIM2_ETR/TIM1_BKIN/USART2_CTS/USART2_NSS/I2C4_SCL/FMC_D12(boot)/FMC_AD12/DCMIPP_D10/LCD_B7/HDP7

PF0/TRACED13/DFSDM1_CKOUT/USART3_CK/SDMMC2_D4/FMC_A0/LCD_R6/LCD_G0
PF1/TRACED7/I2C2_SDA/SPI3_MOSI/I2S3_SDO/FMC_A1/LCD_B7/LCD_G1/HDP7
PF2/TRACED1/I2C2_SCL/DFSDM1_CKIN1/USART6_CK/SDMMC2_D0DIR/SDMMC1_D0DIR/FMC_A2/LCD_G4/LCD_B3
PF3/LPTIM2_IN2/I2C5_SDA/SPI4_MISO/I2S4_SDI/SPI3_NSS/I2S3_WS/FMC_A3/LCD_G3
PF4/USART2_RX/ETH2_MII_RXD0/ETH2_RGMII_RXD0/ETH2_RMII_RXD0/FMC_A4/DCMIPP_D4/LCD_B6
PF5/TRACED12/DFSDM1_CKIN0/I2C1_SMBA/LCD_G0/FMC_A5/DCMIPP_D11/LCD_R5
PF6/TIM16_CH1/SPI5_NSS/UART7_RX(boot)/QUADSPI_BK1_IO2/ETH2_MII_TX_EN/ETH2_RGMII_TX_CTL/ETH2_RMII_TX_EN/LCD_R7/LCD_G4
PF7/TIM17_CH1/UART7_TX(boot)/UART4_CTS/ETH1_RGMII_CLK125/ETH2_MII_TXD0/ETH2_RGMII_TXD0/ETH2_RMII_TXD0/FMC_A18/LCD_G2
PF8/TIM16_CH1N/TIM4_CH3/TIM8_CH3/SAI1_SCK_B/USART6_TX/TIM13_CH1/QUADSPI_BK1_IO0(boot)/DCMIPP_D15/LCD_B3/WKUP1
PF9/TIM17_CH1N/TIM1_CH1/DFSDM1_CKIN3/SAI1_D4/UART7_CTS/UART8_RX/TIM14_CH1/QUADSPI_BK1_IO1(boot)/QUADSPI_BK2_IO3/FMC_A9/LCD_B6
PF10/TIM16_BKIN/SAI1_D3/TIM8_BKIN/SPI5_NSS/USART6_RTS/USART6_DE/UART7_RTS/UART7_DE/QUADSPI_CLK(boot)/DCMIPP_HSYNC/LCD_B5/TAMP_IN1
PF11/USART2_TX/SAI1_D2/DFSDM1_CKIN3/SAI1_FS_A/ETH2_MII_RX_ER/ADC1_INP8_INN4/ADC2_INP8_INN4
PF12/SPI1_NSS/I2S1_WS/SAI1_SD_A/UART4_TX/ETH1_MII_TX_ER/ETH1_RGMII_CLK125/ADC1_INP6_INN2
PF13/TIM2_CH1/TIM2_ETR/SAI1_MCLK_B/DFSDM1_DATIN3/USART2_TX/UART5_RX/ADC1_INP11_INN10/ADC2_INP11_INN10
PF14/JTCK/SWCLK
PF15/JTMS/SWDIO

STM32MP135DAE7

Title: STM32MP135_CPU_DEF.SchDoc			
Project: STM32MP135_CORE.PrjPcb			
Size: A4	Author: ALIENTEK		
Date: 2023/3/31	Version: V1.0	Sheet: 3 of 8	

正点原子



U1C

LCD_G5			D7
ETH2_TXD2	22R	R53	N2
ETH1_MDC			R1
ETH2_GTX_CLK	22R	R54	L5
LCD_VSYNC			A8
ETH2_MDC			F2
SDMMC2_CMD			A14
LCD_R2			C9
LCD_B1			F3
DCMI_VSYNC			E1
FDCAN1_TX			F1
ETH2_TXD1	22R	R55	M3
ETH2_RX_DV			T1
ETH1_TXD0	22R	R56	P8
ETH1_TXD1	22R	R57	P9
LCD_B4			G4
			P1
			P2
ETH2_CLK125			F4
I2C3_SCL			R2
JTDI			T15
JTDO			R14
ETH2_RXD2			L3
SPI5_SCK			H3
DCMI_HSYNC			F5
LCD_DE			A9
LCD_HSYNC			E11
ETH2_RX_CLK			H1
SPI5_MOSI			C2
LCD_G2			A10
DCMI_D2			B7
CT_INT			L4
SPI5_NSS			K5
CT_RST			J3
LED1			H2
BOOT0			U14
BOOT1			P12
BOOT2			R12
OTG_VBUS			U16

PG0/FDCAN2_TX/FMC_A10/DCMIPP_PIXCLK/LCD_G5
PG1/LPTIM1_ETR/TIM4_ETR/SAI2_FS_A/I2C2_SMBA/SPI2_MISO/I2S2_SDI/SAI2_D2/FDCAN2_TX/ETH2_MII_TXD2/ETH2_RGMII_TXD2/FMC_NBL0/LCD_G7
PG2/MCO2/TIM8_BKIN/SAI2_MCLK_B/ETH1_MDC/DCMIPP_D1
PG3/TIM8_BKIN2/I2C2_SDA/SAI2_SD_B/FDCAN2_RX/ETH2_RGMII_GTX_CLK/ETH1_MDIO/FMC_A13/DCMIPP_D15/DCMIPP_D12
PG4/TRACED1/TIM1_BKIN2/DFSDM1_CKIN3/USART3_RX/SDMMC2_D123DIR/LCD_VSYNC/FMC_A14/DCMIPP_D8/DCMIPP_D13/HDP1
PG5/TIM17_CH1/ETH2_MDC/LCD_G4/FMC_A15/DCMIPP_VSYNC/DCMIPP_D3
PG6/TRACED3/TIM17_BKIN/TIM5_CH4/SAI2_D1/USART1_RX/SAI2_SD_A/SDMMC2_CMD(boot)/LCD_G0/LCD_DE/LCD_R7/HDP3
PG7/TRACED8/TIM1_ETR/SPI3_MISO/I2S3_SDI/UART7_CTS/SDMMC2_CKIN/LCD_R1/LCD_R5/LCD_R2
PG8/TIM2_CH1/TIM2_ETR/TIM8_ETR/SPI5_MISO/SAI1_MCLK_B/LCD_B1/USART3_RTS/USART3_DE/SPDIFRX_IN2/QUADSPI_BK2_IO2/QUADSPI_BK1_IO3/FMC_NE2/ETH2_CLK/DCMIPP_D6/TAMP_IN4
PG9/DBTRGO/I2C2_SDA/USART6_RX/SPDIFRX_IN3/FDCAN1_RX/FMC_NE2/FMC_NCE(boot)/DCMIPP_VSYNC
PG10/SPI5_SCK/SAI1_SD_B/UART8_CTS/FDCAN1_TX/QUADSPI_BK2_IO1(boot)/FMC_NE3/DCMIPP_D2
PG11/SAI2_D3/I2S2_MCK/USART3_TX/UART4_TX/ETH2_MII_TXD1/ETH2_RGMII_TXD1/ETH2_RMII_TXD1/FMC_A24/DCMIPP_D14/LCD_B2
PG12/LPTIM1_IN1/SAI2_SCK_A/SAI2_CK2/USART6_RTS/USART6_DE/USART3_CTS/ETH2_PHY_INTN/ETH1_PHY_INTN/ETH2_MII_RX_DV/ETH2_RGMII_RX_CTL/ETH2_RMII_CRS_DV
PG13/LPTIM1_OUT/USART6_CTS/USART6_NSS/ETH1_MII_TXD0/ETH1_RGMII_TXD0/ETH1_RMII_TXD0/ADC2_INP6_INN2
PG14/LPTIM1_ETR/SAI2_D1/USART6_TX/SAI2_SD_A/ETH1_MII_TXD1/ETH1_RGMII_TXD1/ETH1_RMII_TXD1
PG15/USART6_CTS/USART6_NSS/UART7_CTS/QUADSPI_BK1_IO1/ETH2_PHY_INTN/LCD_B4/DCMIPP_D10/LCD_B3

PH0-OSC_IN
PH1-OSC_OUT
PH2/LPTIM1_IN2/DCMIPP_D9/LCD_G1/UART7_TX/QUADSPI_BK2_IO0(boot)/ETH2_MII_CRS/ETH1_MII_CRS/FMC_NE4/ETH2_RGMII_CLK125/LCD_B0
PH3/I2C3_SCL/SPI5_MOSI/QUADSPI_BK2_IO1/ETH1_MII_COL/LCD_R5/ETH2_MII_COL/QUADSPI_BK1_IO0/LCD_B4
PH4/JTDI
PH5/JTDO
PH6/TIM12_CH1/USART2_CK/I2C5_SDA/SPI2_SCK/I2S2_CK/QUADSPI_BK1_IO2/ETH1_PHY_INTN/ETH1_MII_RX_ER/ETH2_MII_RXD2/ETH2_RGMII_RXD2/QUADSPI_BK1_NCS
PH7/SAI2_FS_B/I2C3_SDA/SPI5_SCK/QUADSPI_BK2_IO3/ETH2_MII_TX_CLK/ETH1_MII_TX_CLK/QUADSPI_BK1_IO3/LCD_B2
PH8/TRACED9/TIM5_ETR/USART2_RX/I2C3_SDA/LCD_R6/FMC_A8/DCMIPP_HSYNC/LCD_R2/HDP2
PH9/TIM1_CH4/TIM12_CH2/SPI4_SCK/I2S4_CK/DCMIPP_D13/LCD_B5/LCD_DE/FMC_A20/DCMIPP_D9/DCMIPP_D8
PH10/TRACED0/TIM5_CH1/SAI2_D3/DFSDM1_DATIN2/I2S3_MCK/SPI2_MOSI/I2S2_SDO/USART3_CTS/USART3_NSS/SDMMC1_D4/LCD_HSYNC/LCD_R2/HDP0
PH11/SPI5_NSS/TIM5_CH2/SAI2_SD_A/SPI2_NSS/I2S2_WS/I2C4_SCL/USART6_RX/QUADSPI_BK2_IO0/ETH2_MII_RX_CLK/ETH2_RGMII_RX_CLK/ETH2_RMII_REF_CLK/FMC_A12/LCD_G6
PH12/USART2_TX/TIM5_CH3/DFSDM1_CKIN1/I2C3_SCL/SPI5_MOSI/SAI1_SCK_A/QUADSPI_BK2_IO2/SAI1_CK2/ETH1_MII_CRS/FMC_A6/DCMIPP_D3
PH13/TRACED15/USART2_CK/TIM8_CH1N/I2C5_SCL/SPI3_SCK/I2S3_CK/UART4_TX/LCD_G3/LCD_G2
PH14/DFSDM1_DATIN2/I2C3_SDA/DCMIPP_D8/UART4_RX/LCD_B4/DCMIPP_D2/DCMIPP_PIXCLK

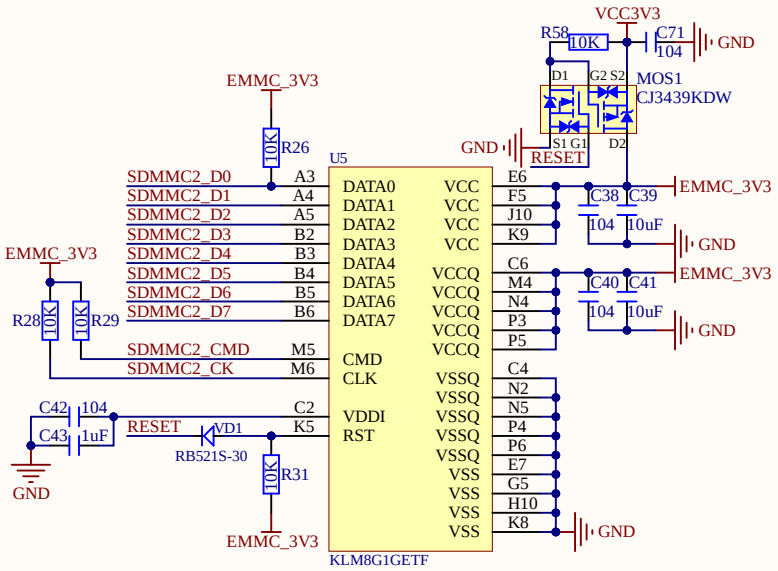
PI0/SPDIFRX_IN0/TAMP_IN8_OUT1
PI1/SPDIFRX_IN1/RTC_OUT2_LSCO/TAMP_IN2_OUT3/WKUP4
PI2/SPDIFRX_IN2/TAMP_IN3_OUT4/WKUP5
PI3/SPDIFRX_IN3/ETH1_MII_RX_ER/TAMP_IN4_OUT5/WKUP2
PI4-BOOT0(BOOT0)
PI5-BOOT1(BOOT1)
PI6-BOOT2(BOOT2)
PI7/OTG_HS_VBUS

STM32MP135DAE7

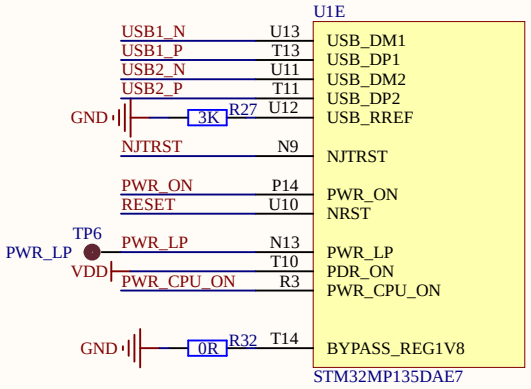
Title: STM32MP135_CPU_GHI.SchDoc			
Project: STM32MP135_CORE.PrjPcb			
Size: A4	Author: ALIENTEK		
Date: 2023/3/31	Version: V1.0	Sheet: 4 of 8	

正点原子

EMMC



USB&PWR_CONTROL



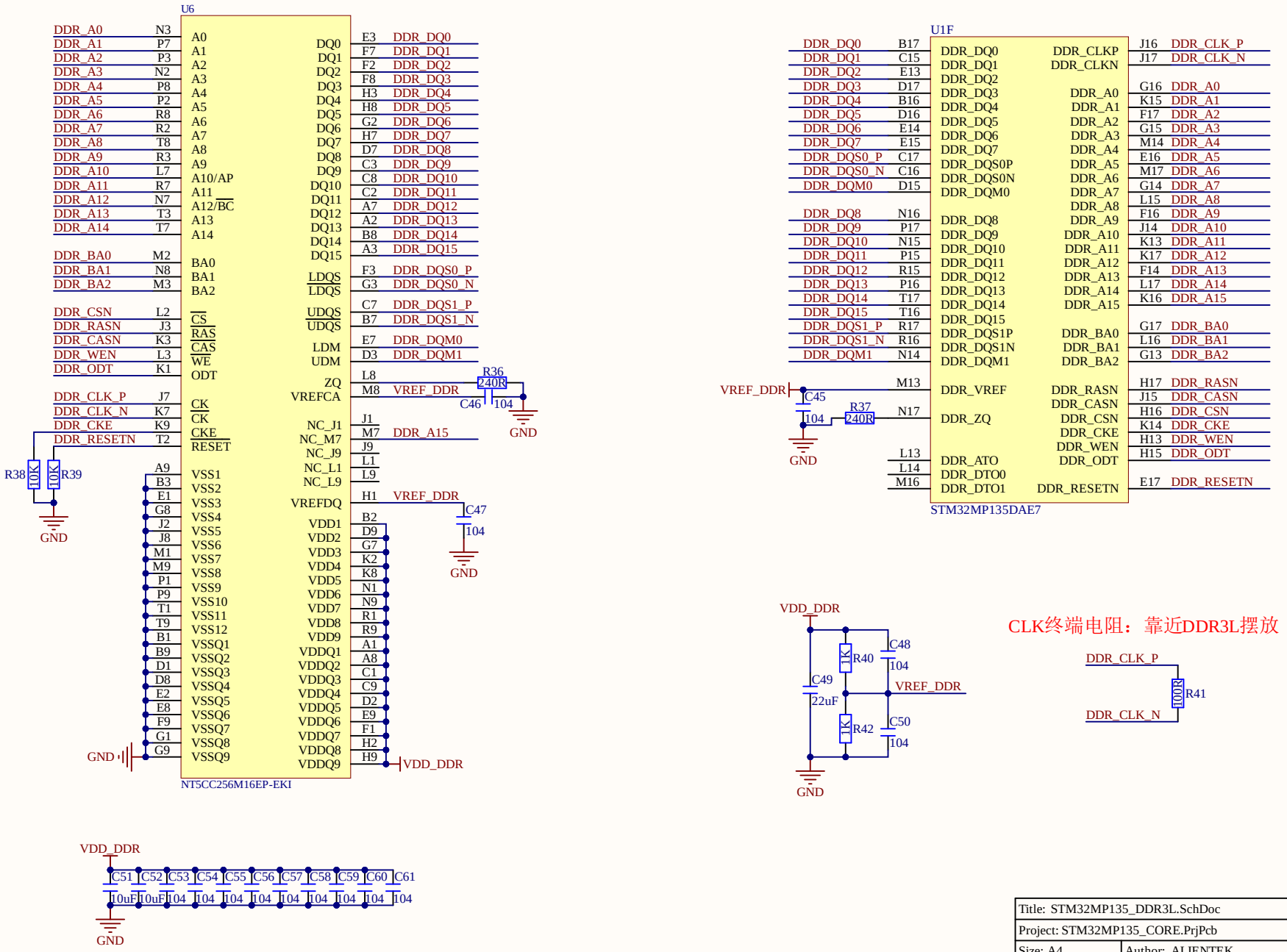
RESET

ESD&FKT

ESD	FKT
ESD	FKT
ESD	FKT

Title: STM32MP135_FLASH&OTHER.SchDoc		
Project: STM32MP135_CORE.PrjPcb		
Size: A4	Author: ALIENTEK	
Date: 2023/3/31	Version: V1.0	Sheet: 5 of 8

正点原子


U6
DDR_A0 N3
DDR_A1 P7
DDR_A2 P3
DDR_A3 N2
DDR_A4 P8
DDR_A5 P2
DDR_A6 R8
DDR_A7 R2
DDR_A8 T8
DDR_A9 R3
DDR_A10 L7
DDR_A11 R7
DDR_A12 N7
DDR_A13 T3
DDR_A14 T7
DDR_BA0 M2
DDR_BA1 N8
DDR_BA2 M3
DDR_CSN L2
DDR_RASN J3
DDR_CASN K3
DDR_WEN L3
DDR_ODT K1
DDR_CLK_P J7
DDR_CLK_N K7
DDR_CKE K9
DDR_RESETN T2
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12/BC A13 A14
BA0 BA1 BA2
CS RAS CAS WE ODT
CK CK CKE RESET
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6 VSS7 VSS8 VSS9 VSS10 VSS11 VSS12 VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5 VSSQ6 VSSQ7 VSSQ8 VSSQ9
A9 B3 E1 G8 J2 J8 M1 M9 P1 P9 T1 T9 B1 B9 D1 D8 E2 E8 F9 G1 G9
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15
E3 F7 F2 F8 H3 H8 G2 H7 D7 C3 C8 C2 A7 A2 B8 A3
DDR_DQ0 DDR_DQ1 DDR_DQ2 DDR_DQ3 DDR_DQ4 DDR_DQ5 DDR_DQ6 DDR_DQ7 DDR_DQ8 DDR_DQ9 DDR_DQ10 DDR_DQ11 DDR_DQ12 DDR_DQ13 DDR_DQ14 DDR_DQ15
LDQS UDQS LDM UDM ZQ VREFCA
F3 G3 C7 B7 E7 D3 L8 M8
DDR_DQS0_P DDR_DQS0_N DDR_DQS1_P DDR_DQS1_N DDR_DQM0 DDR_DQM1 VREF_DDR
LDQS UDQS
NC_J1 NC_M7 NC_J9 NC_L1 NC_L9 VREFDQ
J1 M7 J9 L1 L9 H1
DDR_A15 VREF_DDR
VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDDQ1 VDDQ2 VDDQ3 VDDQ4 VDDQ5 VDDQ6 VDDQ7 VDDQ8 VDDQ9
B2 D9 G7 K2 K8 N1 N9 R1 R9 A1 A8 C1 C9 D2 E9 F1 H2 H9
VDD_DDR
NT5CC256M16EP-EKI
R36 240R
C46 104
R38 10K
R39 10K
C47 104
GND
U1F
DDR_DQ0 B17
DDR_DQ1 C15
DDR_DQ2 E13
DDR_DQ3 D17
DDR_DQ4 B16
DDR_DQ5 D16
DDR_DQ6 E14
DDR_DQ7 E15
DDR_DQS0_P C17
DDR_DQS0_N C16
DDR_DQM0 D15
DDR_DQ8 N16
DDR_DQ9 P17
DDR_DQ10 N15
DDR_DQ11 P15
DDR_DQ12 R15
DDR_DQ13 P16
DDR_DQ14 T17
DDR_DQ15 T16
DDR_DQS1_P R17
DDR_DQS1_N R16
DDR_DQM1 N14
M13
N17
L13 L14 M16
DDR_VREF
DDR_ZQ
DDR_ATO DDR_DTO0 DDR_DTO1
DDR_CLKP DDR_CLKN
DDR_A0 DDR_A1 DDR_A2 DDR_A3 DDR_A4 DDR_A5 DDR_A6 DDR_A7 DDR_A8 DDR_A9 DDR_A10 DDR_A11 DDR_A12 DDR_A13 DDR_A14 DDR_A15
DDR_BA0 DDR_BA1 DDR_BA2
DDR_RASN DDR_CASN DDR_CSN DDR_CKE DDR_WEN DDR_ODT
DDR_RESETN
J16 J17 G16 K15 F17 G15 M14 E16 M17 G14 L15 F16 J14 K13 K17 F14 L17 K16 G17 L16 G13 H17 J15 H16 K14 H13 H15 E17
DDR_CLK_P DDR_CLK_N DDR_A0 DDR_A1 DDR_A2 DDR_A3 DDR_A4 DDR_A5 DDR_A6 DDR_A7 DDR_A8 DDR_A9 DDR_A10 DDR_A11 DDR_A12 DDR_A13 DDR_A14 DDR_A15 DDR_BA0 DDR_BA1 DDR_BA2 DDR_RASN DDR_CASN DDR_CSN DDR_CKE DDR_WEN DDR_ODT DDR_RESETN
STM32MP135DAE7
VREF_DDR
C45 104
R37 240R
GND
VDD_DDR
R40 1K
R42 1K
C48 104
C49 22uF
C50 104
VREF_DDR
GND
CLK终端电阻：靠近DDR3L摆放
DDR_CLK_P
R41 100R
DDR_CLK_N
VDD_DDR
C51 10uF C52 10uF C53 104 C54 104 C55 104 C56 104 C57 104 C58 104 C59 104 C60 104 C61 104
GND
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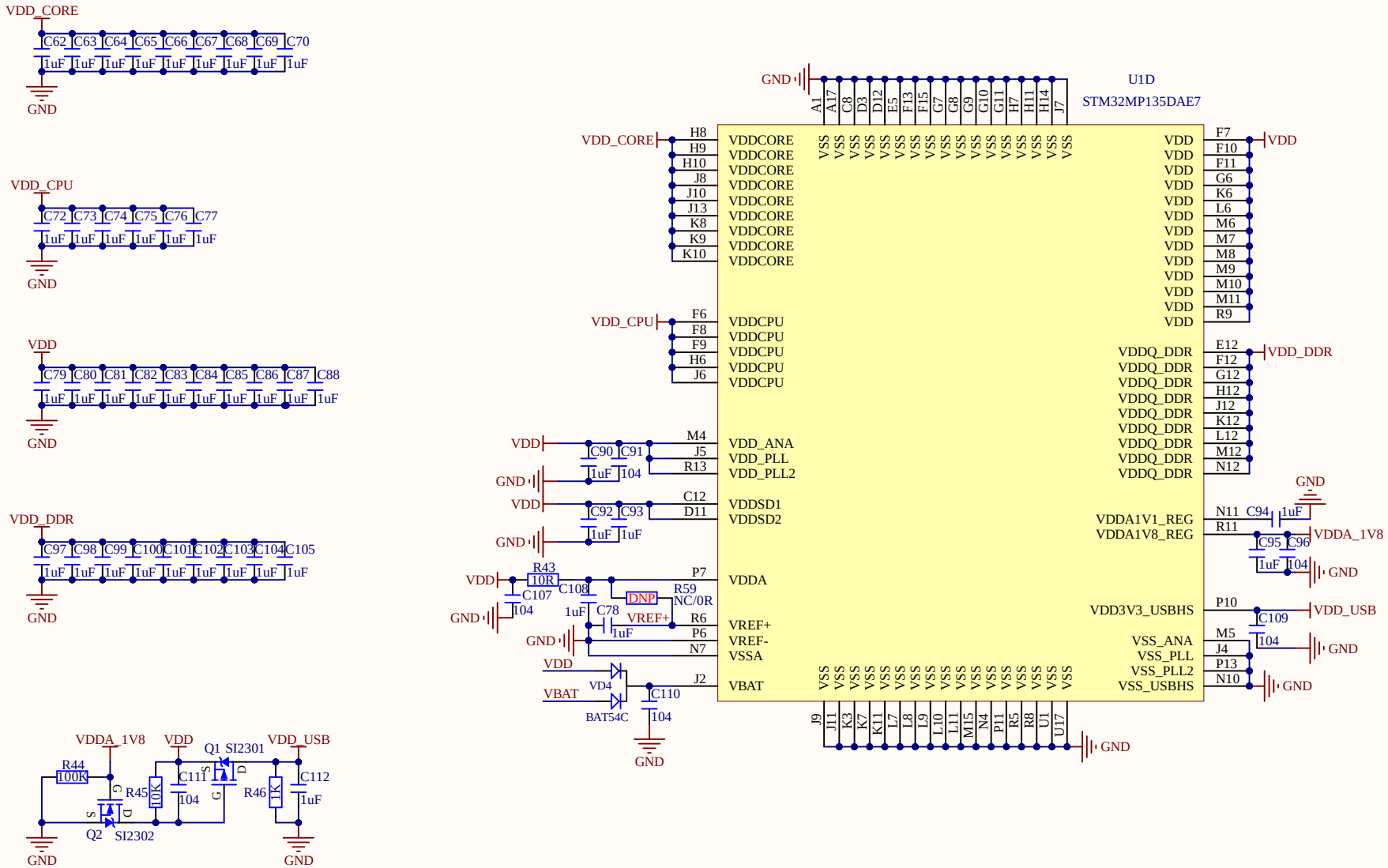
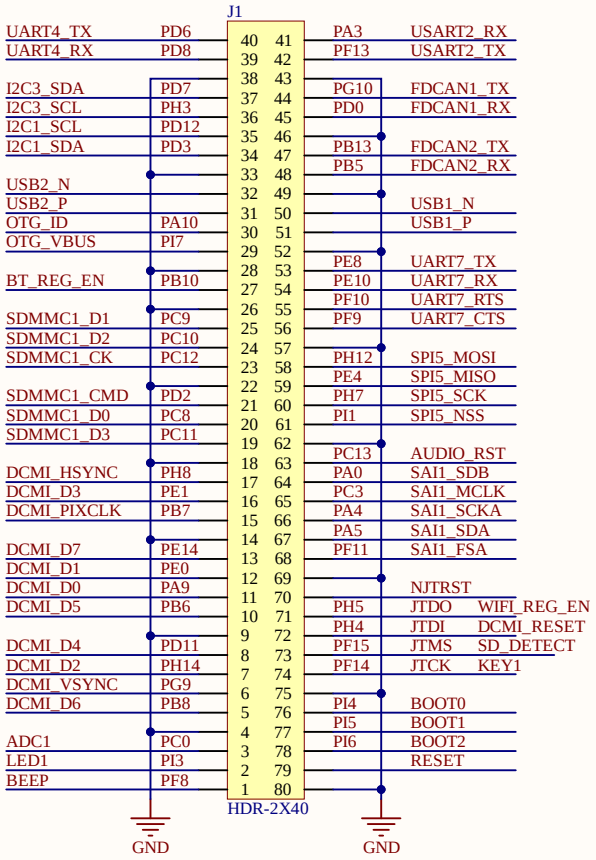
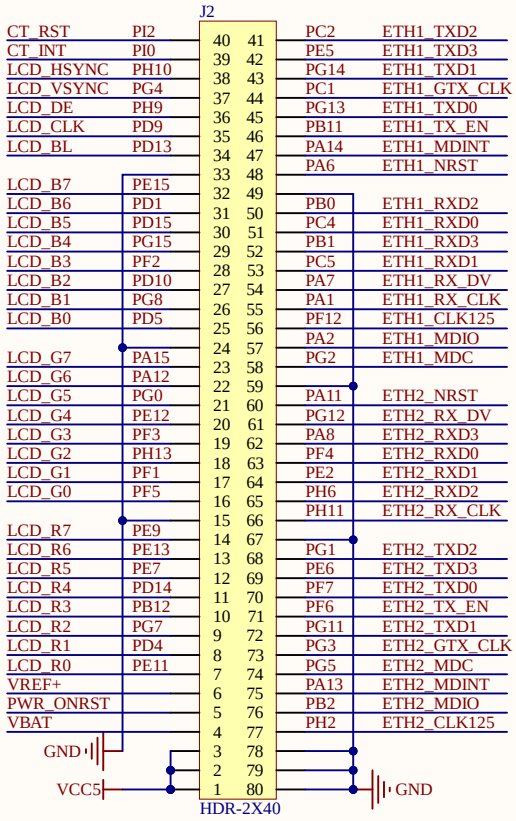
Project: STM32MP135_CORE.PrjPcb
Size: A4
Author: ALIENTEK
Date: 2023/3/31
Version: V1.0
Sheet: 6 of 8
正点原子


VDD_CORE
C62 C63 C64 C65 C66 C67 C68 C69 C70
1uF 1uF 1uF 1uF 1uF 1uF 1uF 1uF 1uF
GND
VDD_CPU
C72 C73 C74 C75 C76 C77
1uF 1uF 1uF 1uF 1uF 1uF
GND
VDD
C79 C80 C81 C82 C83 C84 C85 C86 C87 C88
1uF 1uF 1uF 1uF 1uF 1uF 1uF 1uF 1uF 1uF
GND
VDD_DDR
C97 C98 C99 C100 C101 C102 C103 C104 C105
1uF 1uF 1uF 1uF 1uF 1uF 1uF 1uF 1uF
GND
VDDA_1V8
VDD
VDD_USB
Q1 SI2301
R44 100K
R45 10K
C111 104
R46 1K
C112 1uF
Q2 SI2302
GND
U1D
STM32MP135DAE7
VDD_CORE
VDD_CPU
VDD_DDR
VDD_USB
VDDA_1V8
VDD_ANA
VDD_PLL
VDD_PLL2
VDDSD1
VDDSD2
VDDA
VREF+
VREF-
VSSA
VBAT
VDDCORE
VDDCPU
VDDQ_DDR
VDDA1V1_REG
VDDA1V8_REG
VDD3V3_USBHS
VSS_ANA
VSS_PLL
VSS_PLL2
VSS_USBHS
VSS
VDD
C90 C91 1uF 104
C92 C93 1uF 1uF
R43 10R
C107 104
C108 1uF
R59 DNP NC/0R
C78 1uF
R6
P6
N7
VD4 BAT54C
C110 104
C94 1uF
R11
C95 C96 1uF 104
C109 104
Title: STM32MP135_CPU_POWER.SchDoc
Project: STM32MP135_CORE.PrjPcb
Size: A4
Author: ALIENTEK
Date: 2023/3/31
Version: V1.0
Sheet: 7 of 8
正点原子

PINOUT





Title: STM32MP135_PINOUT.SchDoc		
Project: STM32MP135_CORE.PrjPcb		
Size: A4	Author: ALIENTEK	
Date: 2023/3/31	Version: V1.0	Sheet: 8 of 8

正点原子