

A

B

C

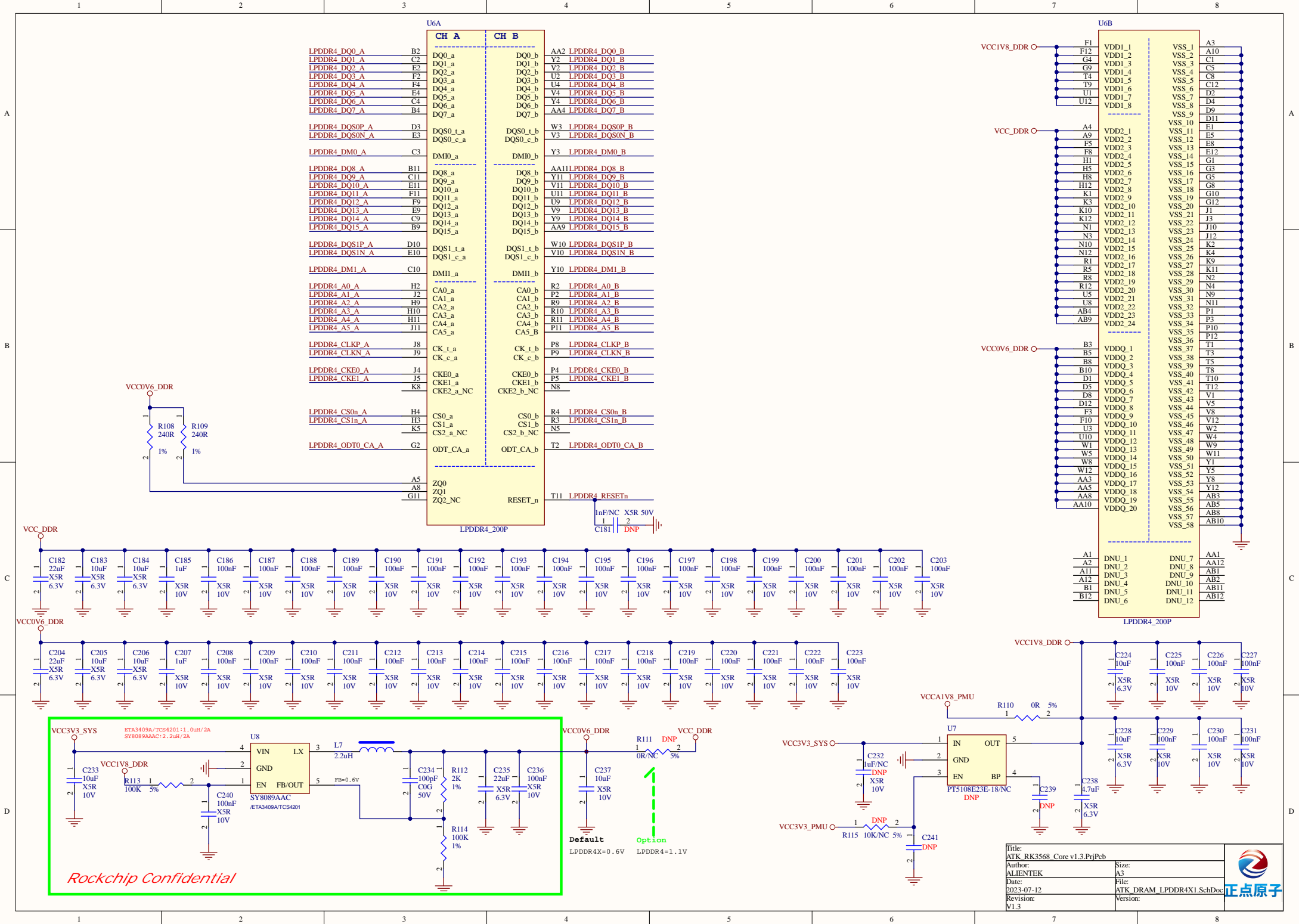
D

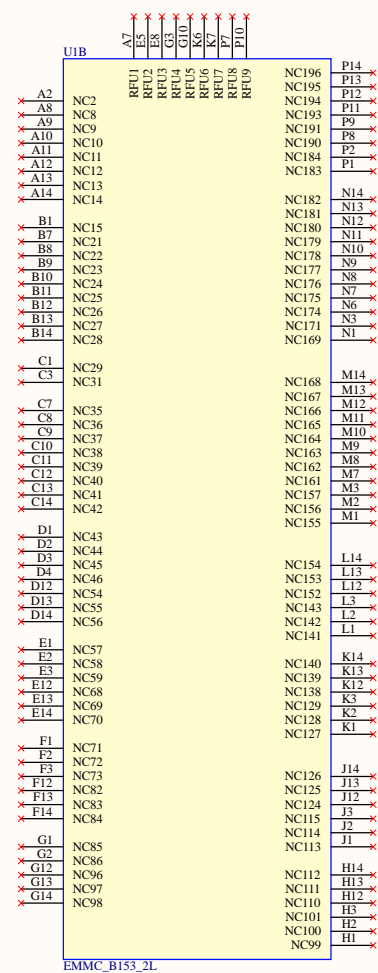
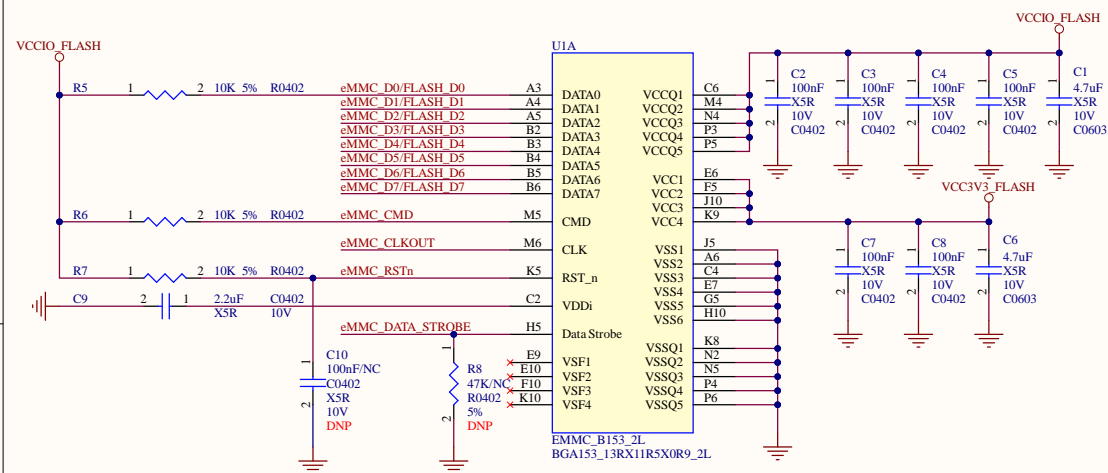
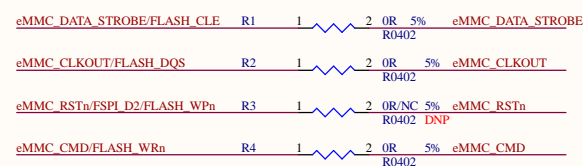
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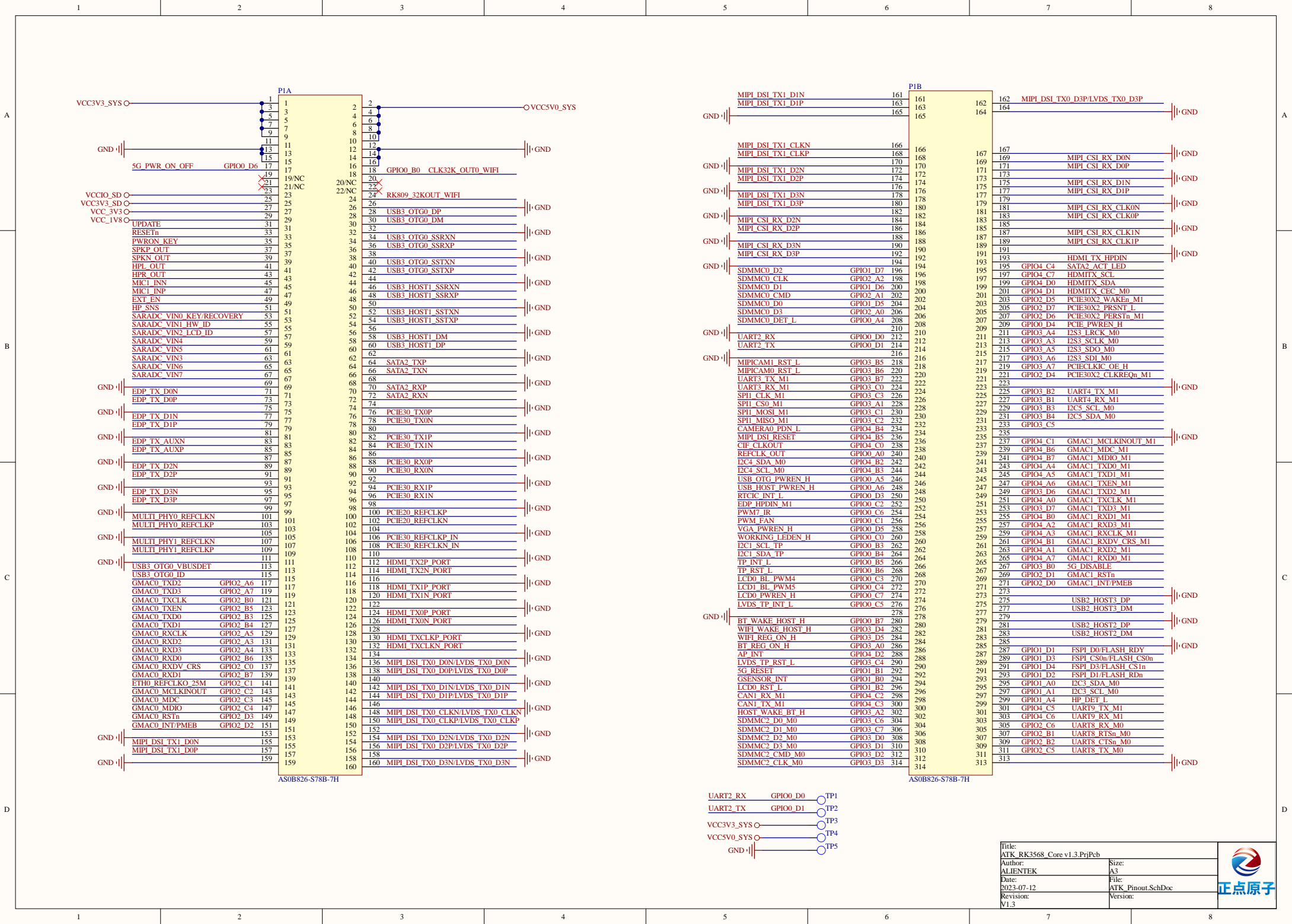
B

C

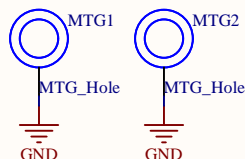
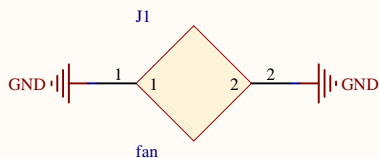
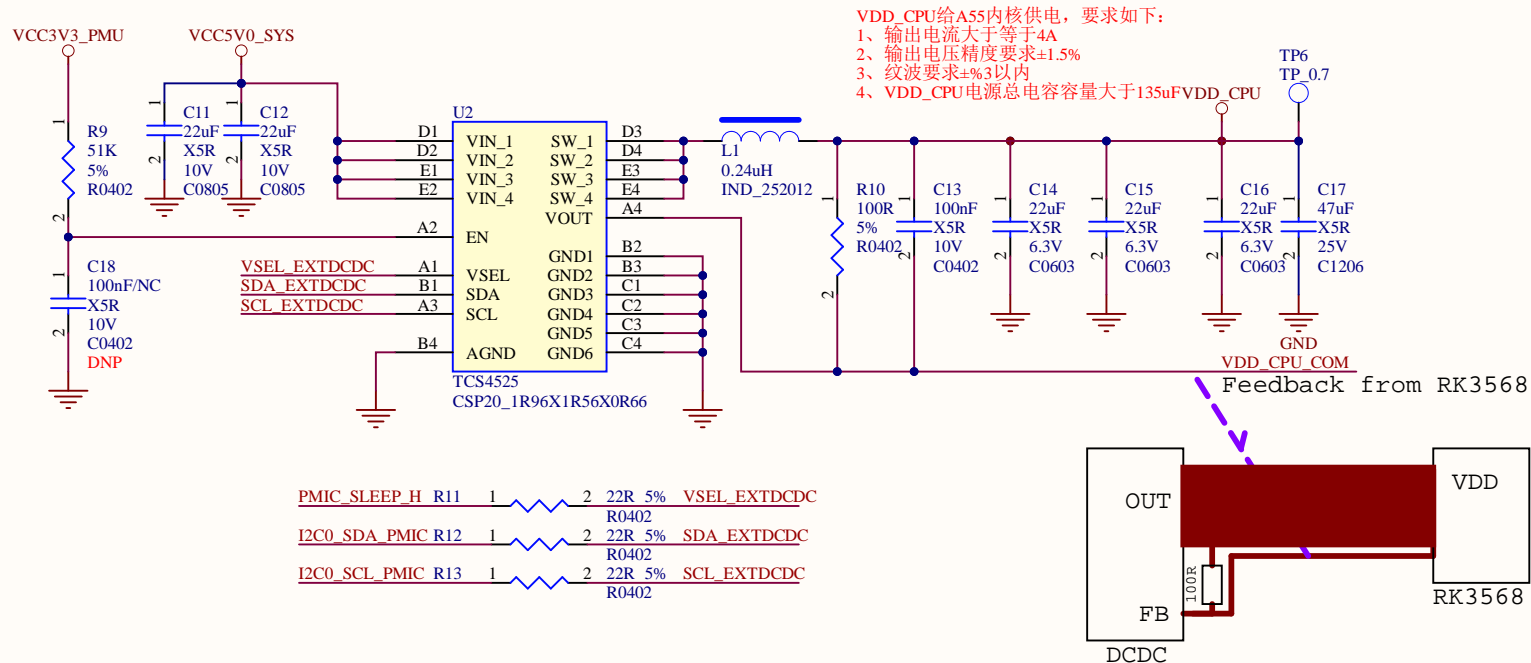
D







VDD_CPU

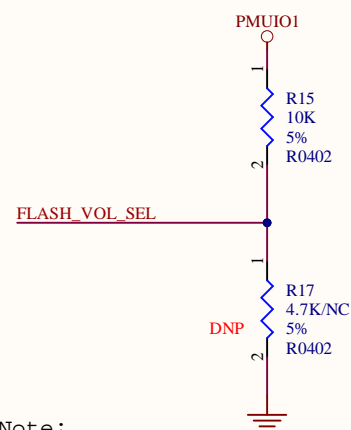
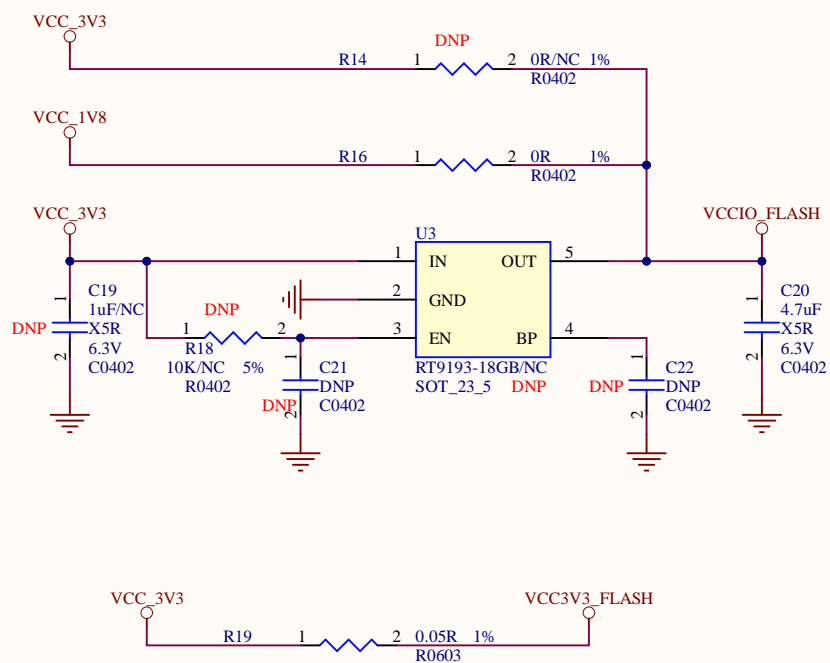


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| | | |
|-----------|-----------------------------|----------------------|
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| Author: | ALIENTEK | G:\AD标准库\字 |
| Date: | 2023-07-12 | 体模板\AD通用 |
| Revision: | V1.3 | 模板标题栏\正 |
| | | 点LOGO竖.png. |
| | | File does not exist. |

Flash Power Manage

| | | |
|------------|--|---|
| | VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH) | FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default |
| eMMC | 1.8V | FLASH_VOL_SEL --> Logic=H |
| Nand flash | Default 3.3V, Adjust according to demand 1.8V | FLASH_VOL_SEL --> Logic=L(Default) |
| SPI flash | Default 3.3V, Adjust according to demand 1.8V | FLASH_VOL_SEL --> Logic=L(Default) |



Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

| | |
|---------------------------------------|---|
| Title: ATK_RK3568_Core v1.3.PrjPcb | Cannot open file G:\AD标准库\字 体模板\AD通用 模板标题栏\正 点\LOGO竖.png. File does not exist. |
| Author: ALIENTEK | Size: A4 |
| Date: 2023-07-12 | File: ATK_Powr_Flash Power Manage.SchDoc |
| Revision: V1.3 | Version: |

RK3568_H(VCCIO1 Domain)

USH

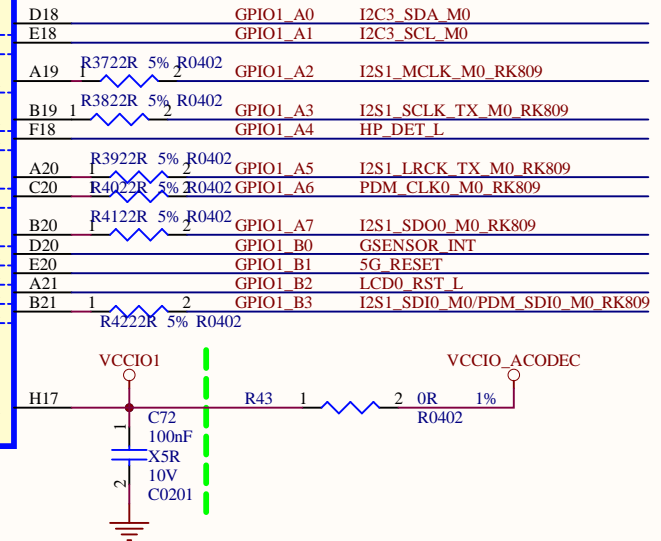
VCCIO1 Domain

Operating Voltage=1.8V/3.3V

| | | | | | | | | | | |
|-----------------|---|---------------|---|-------------|---|---------------------|---|------------------|---|------------|
| I2C3_SDA_M0 | / | UART3_RX_M0 | / | CAN1_RX_M0 | / | AUDIOPWM_LOUT_P | / | ACODEC_ADC_DATA | / | GPIOD_A0_u |
| I2C3_SCL_M0 | / | UART3_TX_M0 | / | CAN1_TX_M0 | / | AUDIOPWM_LOUT_N | / | ACODEC_ADC_CLK | / | GPIOD_A1_u |
| I2S1_MCLK_M0 | / | UART3_RTSn_M0 | / | SCR_CLK | / | PCIE30X1_PERSTn_M2 | / | | / | GPIOD_A2_d |
| I2S1_SCLK_TX_M0 | / | UART3_CTSn_M0 | / | SCR_IO | / | PCIE30X1_WAKEn_M2 | / | ACODEC_DAC_CLK | / | GPIOD_A3_d |
| I2S1_SCLK_RX_M0 | / | UART4_RX_M0 | / | PDM_CLK1_M0 | / | SPDIF_TX_M0 | / | | / | GPIOD_A4_d |
| I2S1_LRCK_TX_M0 | / | UART4_RTSn_M0 | / | SCR_RST | / | PCIE30X1_CLKREQn_M2 | / | ACODEC_DAC_SYNC | / | GPIOD_A5_d |
| I2S1_LRCK_RX_M0 | / | UART4_TX_M0 | / | PDM_CLK0_M0 | / | AUDIOPWM_ROUT_P | / | | / | GPIOD_A6_d |
| I2S1_SDO0_M0 | / | UART4_CTSn_M0 | / | SCR_DET | / | AUDIOPWM_ROUT_N | / | ACODEC_DAC_DATA1 | / | GPIOD_A7_d |
| I2S1_SDO1_M0 | / | I2S1_SDI3_M0 | / | PDM_SDI3_M0 | / | PCIE20_CLKREQn_M2 | / | ACODEC_DAC_DATA0 | / | GPIOD_B0_d |
| I2S1_SDO2_M0 | / | I2S1_SDI2_M0 | / | PDM_SDI2_M0 | / | PCIE20_WAKEn_M2 | / | ACODEC_ADC_SYNC | / | GPIOD_B1_d |
| I2S1_SDO3_M0 | / | I2S1_SDI1_M0 | / | PDM_SDI1_M0 | / | PCIE20_PERSTn_M2 | / | | / | GPIOD_B2_d |
| | | I2S1_SDI0_M0 | / | PDM_SDI0_M0 | / | | / | | / | GPIOD_B3_d |

RK3568-Socket

VCCIO1



Note:

Caps of between dashed green lines and U5 should be placed under the U5 package

Rockchip Confidential

| | | |
|-----------|-----------------------------|----------------------|
| Title: | ATK_RK3568_Core v1.3.PrjPeb | Cannot open file |
| Author: | ALIENTEK | G:\AD标准库\字 |
| Date: | 2023-07-12 | 体模板\AD通用 |
| Revision: | V1.3 | 模板标题栏\正 |
| | | 点\LOGO竖.png |
| | | File does not exist. |

RK3568_F (DDR PHY)

USF

| | | DDR4 | LPDDR4 | DDR3 | LPDDR3 | | DDR4 | LPDDR4 | DDR3 | LPDDR3 | |
|----------------|-----|------------------------------|------------------|------------------|----------------|--|-------------|--------------------|---------------|---------------|------|
| LPDDR4 DQ0_A | F2 | DDR DQ0_A / DDR4_DQ0_A | / LPDDR4_DQ0_A | / DDR3_DQ0 | / LPDDR3_DQ15 | | DDR4_A0 | / LPDDR4_CLKP_B | / DDR3_A9 | / --- | AC0 |
| LPDDR4 DQ1_A | E1 | DDR DQ1_A / DDR4_DQ1_A | / LPDDR4_DQ1_A | / DDR3_DQ1 | / LPDDR3_DQ14 | | DDR4_A1 | / LPDDR4_CLKN_B | / DDR3_A8 | / --- | AC1 |
| LPDDR4 DQ2_A | E2 | DDR DQ2_A / DDR4_DQ2_A | / LPDDR4_DQ2_A | / DDR3_DQ2 | / LPDDR3_DQ13 | | DDR4_A2 | / LPDDR4_A1_A | / DDR3_A7 | / LPDDR3_A6 | AC2 |
| LPDDR4 DQ3_A | D1 | DDR DQ3_A / DDR4_DQ3_A | / LPDDR4_DQ3_A | / DDR3_DQ3 | / LPDDR3_DQ12 | | DDR4_A3 | / LPDDR4_CKE1_A | / DDR3_A3 | / --- | AC3 |
| LPDDR4 DQ4_A | J1 | DDR DQ4_A / DDR4_DQ4_A | / LPDDR4_DQ4_A | / DDR3_DQ4 | / LPDDR3_DQ11 | | DDR4_A4 | / LPDDR4_A3_B | / DDR3_BA1 | / LPDDR3_A3 | AC4 |
| LPDDR4 DQ5_A | J2 | DDR DQ5_A / DDR4_DQ5_A | / LPDDR4_DQ5_A | / DDR3_DQ5 | / LPDDR3_DQ10 | | DDR4_A5 | / LPDDR4_A5_B | / DDR3_A11 | / LPDDR3_A2 | AC5 |
| LPDDR4 DQ6_A | H1 | DDR DQ6_A / DDR4_DQ6_A | / LPDDR4_DQ6_A | / DDR3_DQ6 | / LPDDR3_DQ9 | | DDR4_A6 | / LPDDR4_A1_B | / DDR3_A13 | / LPDDR3_A1 | AC6 |
| LPDDR4 DQ7_A | H4 | DDR DQ7_A / DDR4_DQ7_A | / LPDDR4_DQ7_A | / DDR3_DQ7 | / LPDDR3_DQ8 | | DDR4_A7 | / LPDDR4_ODT0_CA_B | / DDR3_A8 | / --- | AC7 |
| LPDDR4 DM0_A | H5 | DDR DM0_A / DDR4_DM0_A | / LPDDR4_DM0_A | / DDR3_DM0 | / LPDDR3_DM1 | | DDR4_A8 | / LPDDR4_ODT0_CA_A | / DDR3_A6 | / LPDDR3_A9 | AC8 |
| LPDDR4 DQS0P_A | G1 | DDR DQS0P_A / DDR4_DQS0_P_A | / LPDDR4_DQS0P_A | / DDR3_DQS0P | / LPDDR3_DQS1P | | DDR4_A9 | / LPDDR4_CLKN_B | / DDR3_A5 | / --- | AC9 |
| LPDDR4 DQS0N_A | G2 | DDR DQS0N_A / DDR4_DQS0_N_A | / LPDDR4_DQS0N_A | / DDR3_DQS0N | / LPDDR3_DQSIN | | DDR4_A10 | / LPDDR4_CKE0_B | / DDR3_A10 | / --- | AC10 |
| | | | | | | | DDR4_A11 | / LPDDR4_A0_A | / DDR3_A7 | / LPDDR3_A8 | AC11 |
| | | | | | | | DDR4_A12 | / LPDDR4_A3_A | / DDR3_BA2 | / --- | AC12 |
| LPDDR4 DQ8_A | M1 | DDR DQ8_A / DDR4_DQ8_A | / LPDDR4_DQ8_A | / DDR3_DQ8 | / LPDDR3_DQ25 | | DDR4_A13 | / LPDDR4_A0_B | / DDR3_A14 | / LPDDR3_A0 | AC13 |
| LPDDR4 DQ9_A | N2 | DDR DQ9_A / DDR4_DQ9_A | / LPDDR4_DQ9_A | / DDR3_DQ9 | / LPDDR3_DQ24 | | DDR4_A14 | / LPDDR4_A4_A | / DDR3_A15 | / LPDDR3_A5 | AC14 |
| LPDDR4 DQ10_A | L7 | DDR DQ10_A / DDR4_DQ10_A | / LPDDR4_DQ10_A | / DDR3_DQ10 | / LPDDR3_DQ23 | | DDR4_A15 | / LPDDR4_A3_B | / DDR3_A0 | / --- | AC15 |
| LPDDR4 DQ11_A | L6 | DDR DQ11_A / DDR4_DQ11_A | / LPDDR4_DQ11_A | / DDR3_DQ11 | / LPDDR3_DQ22 | | DDR4_A16 | / LPDDR4_A5_A | / DDR3_BA2n | / LPDDR3_A7 | AC16 |
| LPDDR4 DQ12_A | K2 | DDR DQ12_A / DDR4_DQ12_A | / LPDDR4_DQ12_A | / DDR3_DQ12 | / LPDDR3_DQ21 | | DDR4_A17n | / LPDDR4_CKE1_B | / DDR3_CASn | / --- | AC17 |
| LPDDR4 DQ13_A | J6 | DDR DQ13_A / DDR4_DQ13_A | / LPDDR4_DQ13_A | / DDR3_DQ13 | / LPDDR3_DQ20 | | DDR4_BA0 | / LPDDR4_A2_B | / DDR3_A1 | / --- | AC18 |
| LPDDR4 DQ14_A | J7 | DDR DQ14_A / DDR4_DQ14_A | / LPDDR4_DQ14_A | / DDR3_DQ14 | / LPDDR3_DQ19 | | DDR4_BA1 | / LPDDR4_A4_B | / DDR3_A12 | / LPDDR3_A4 | AC19 |
| LPDDR4 DQ15_A | L4 | DDR DQ15_A / DDR4_DQ15_A | / LPDDR4_DQ15_A | / DDR3_DQ15 | / LPDDR3_DQ18 | | DDR4_B0 | / LPDDR4_ODT1_CA_B | / DDR3_WBn | / --- | AC20 |
| LPDDR4 DM1_A | J4 | DDR DM1_A / DDR4_DM1_A | / LPDDR4_DM1_A | / DDR3_DM1 | / LPDDR3_DM3 | | DDR4_B01 | / LPDDR4_ODT1_CA_A | / DDR3_BA0 | / --- | AC21 |
| LPDDR4 DQS1P_A | L2 | DDR DQS1P_A / DDR4_DQS1_P_A | / LPDDR4_DQS1P_A | / DDR3_DQS1P | / LPDDR3_DQS3P | | DDR4_CLKP | / LPDDR4_CLKP_A | / DDR3_CLKP | / LPDDR3_CLKP | AC23 |
| LPDDR4 DQSIN_A | L1 | DDR DQSIN_A / DDR4_DQSIN_A | / LPDDR4_DQSIN_A | / DDR3_DQSIN | / LPDDR3_DQSIN | | DDR4_CLKN | / LPDDR4_CLKN_A | / DDR3_CLKN | / LPDDR3_CLKN | AC24 |
| | | | | | | | DDR4_CS0n | / LPDDR4_CS0n_A | / DDR3_ODT1 | / LPDDR3_ODT0 | AC25 |
| LPDDR4 DQ0_B | B10 | DDR DQ0_B / DDR4_DQ0_B | / LPDDR4_DQ0_B | / DDR3_DQ16 | / LPDDR3_DQ1 | | DDR4_CS1n | / LPDDR4_CS1n_A | / DDR3_CS1n | / LPDDR3_ODT1 | AC26 |
| LPDDR4 DQ1_B | A9 | DDR DQ1_B / DDR4_DQ1_B | / LPDDR4_DQ1_B | / DDR3_DQ17 | / LPDDR3_DQ0 | | DDR4_ODT0 | / LPDDR4_CS1n_B | / DDR3_ODT0 | / LPDDR3_CS1n | AC27 |
| LPDDR4 DQ2_B | D12 | DDR DQ2_B / DDR4_DQ2_B | / LPDDR4_DQ2_B | / DDR3_DQ18 | / LPDDR3_DQ6 | | DDR4_ODT1 | / LPDDR4_CS0n_B | / DDR3_CS0n | / LPDDR3_CS0n | AC28 |
| LPDDR4 DQ3_B | E12 | DDR DQ3_B / DDR4_DQ3_B | / LPDDR4_DQ3_B | / DDR3_DQ19 | / LPDDR3_DQ5 | | DDR4_RESETn | / LPDDR4_RESETn | / DDR3_RESETn | / --- | AC29 |
| LPDDR4 DQ4_B | A12 | DDR DQ4_B / DDR4_DQ4_B | / LPDDR4_DQ4_B | / DDR3_DQ20 | / LPDDR3_DQ4 | | | | | | |
| LPDDR4 DQ5_B | D15 | DDR DQ5_B / DDR4_DQ5_B | / LPDDR4_DQ5_B | / DDR3_DQ21 | / LPDDR3_DQ3 | | | | | | |
| LPDDR4 DQ6_B | E15 | DDR DQ6_B / DDR4_DQ6_B | / LPDDR4_DQ6_B | / DDR3_DQ22 | / LPDDR3_DQ2 | | | | | | |
| LPDDR4 DQ7_B | E14 | DDR DQ7_B / DDR4_DQ7_B | / LPDDR4_DQ7_B | / DDR3_DQ23 | / LPDDR3_DQ1 | | | | | | |
| LPDDR4 DM0_B | D14 | DDR DM0_B / DDR4_DM0_B | / LPDDR4_DM0_B | / DDR3_DM2 | / LPDDR3_DM0 | | | | | | |
| LPDDR4 DQS0P_B | A11 | DDR DQS0P_B / DDR4_DQS0_P_B | / LPDDR4_DQS0P_B | / DDR3_DQS2P | / LPDDR3_DQS0P | | | | | | |
| LPDDR4 DQS0N_B | B11 | DDR DQS0N_B / DDR4_DQS0_N_B | / LPDDR4_DQS0N_B | / DDR3_DQS2N | / LPDDR3_DQS0N | | | | | | |
| | | | | | | | | | | | |
| LPDDR4 DQ8_B | A16 | DDR DQ8_B / DDR4_DQ8_B | / LPDDR4_DQ8_B | / DDR3_DQ24 | / LPDDR3_DQ18 | | | | | | |
| LPDDR4 DQ9_B | B17 | DDR DQ9_B / DDR4_DQ9_B | / LPDDR4_DQ9_B | / DDR3_DQ25 | / LPDDR3_DQ19 | | | | | | |
| LPDDR4 DQ10_B | A17 | DDR DQ10_B / DDR4_DQ10_B | / LPDDR4_DQ10_B | / DDR3_DQ26 | / LPDDR3_DQ22 | | | | | | |
| LPDDR4 DQ11_B | B18 | DDR DQ11_B / DDR4_DQ11_B | / LPDDR4_DQ11_B | / DDR3_DQ27 | / LPDDR3_DQ23 | | | | | | |
| LPDDR4 DQ12_B | B13 | DDR DQ12_B / DDR4_DQ12_B | / LPDDR4_DQ12_B | / DDR3_DQ28 | / LPDDR3_DQ16 | | | | | | |
| LPDDR4 DQ13_B | A13 | DDR DQ13_B / DDR4_DQ13_B | / LPDDR4_DQ13_B | / DDR3_DQ29 | / LPDDR3_DQ17 | | | | | | |
| LPDDR4 DQ14_B | D17 | DDR DQ14_B / DDR4_DQ14_B | / LPDDR4_DQ14_B | / DDR3_DQ30 | / LPDDR3_DQ20 | | | | | | |
| LPDDR4 DQ15_B | B14 | DDR DQ15_B / DDR4_DQ15_B | / LPDDR4_DQ15_B | / DDR3_DQ31 | / LPDDR3_DQ21 | | | | | | |
| LPDDR4 DM1_B | E17 | DDR DM1_B / DDR4_DM1_B | / LPDDR4_DM1_B | / DDR3_DM3 | / LPDDR3_DM2 | | | | | | |
| LPDDR4 DQS1P_B | B15 | DDR DQS1P_B / DDR4_DQS1_P_B | / LPDDR4_DQS1P_B | / DDR3_DQS3P | / LPDDR3_DQS2P | | | | | | |
| LPDDR4 DQSIN_B | A15 | DDR DQSIN_B / DDR4_DQSIN_B | / LPDDR4_DQSIN_B | / DDR3_DQS3N | / LPDDR3_DQS2N | | | | | | |
| | | | | | | | | | | | |
| ✗ P5 | | DDR ECC DQ0 / DDR4_ECC_DQ0 | / --- | / DDR3_ECC_DQ0 | | | | | | | |
| ✗ M4 | | DDR ECC DQ1 / DDR4_ECC_DQ1 | / --- | / DDR3_ECC_DQ1 | | | | | | | |
| ✗ M5 | | DDR ECC DQ2 / DDR4_ECC_DQ2 | / --- | / DDR3_ECC_DQ2 | | | | | | | |
| ✗ R5 | | DDR ECC DQ3 / DDR4_ECC_DQ3 | / --- | / DDR3_ECC_DQ3 | | | | | | | |
| ✗ M7 | | DDR ECC DQ4 / DDR4_ECC_DQ4 | / --- | / DDR3_ECC_DQ4 | | | | | | | |
| ✗ R7 | | DDR ECC DQ5 / DDR4_ECC_DQ5 | / --- | / DDR3_ECC_DQ5 | | | | | | | |
| ✗ P4 | | DDR ECC DQ6 / DDR4_ECC_DQ6 | / --- | / DDR3_ECC_DQ6 | | | | | | | |
| ✗ R4 | | DDR ECC DQ7 / DDR4_ECC_DQ7 | / --- | / DDR3_ECC_DQ7 | | | | | | | |
| | | | | | | | | | | | |
| ✗ P7 | | DDR ECC DM / DDR4_ECC_DM | / --- | / DDR3_ECC_DM | | | | | | | |
| | | | | | | | | | | | |
| ✗ P2 | | DDR ECC DQS / DDR4_ECC_DQS_P | / --- | / DDR3_ECC_DQS_P | | | | | | | |
| ✗ P1 | | DDR ECC DQS / DDR4_ECC_DQS_N | / --- | / DDR3_ECC_DQS_N | | | | | | | |

RK3568-Socket

Note:
Except DDR3, other DQ sequences
can not be swap

DDR3L =1.35V
DDR3 =1.5V
DDR4 =1.2V
LPDDR4 =1.2V
LPDDR4x =1.1V

DDRRPHY_VDDQ_1
DDRRPHY_VDDQ_2
DDRRPHY_VDDQ_3
DDRRPHY_VDDQ_4
DDRRPHY_VDDQ_5
DDRRPHY_VDDQ_6
DDRRPHY_VDDQ_7
DDRRPHY_VDDQ_8

DDR3L =1.35V
DDR3 =1.5V
DDR4 =1.2V
LPDDR3 =1.2V
LPDDR4 =1.1V
LPDDR4x #NAME?

DDRRPHY_VDDQL_1
DDRRPHY_VDDQL_2
DDRRPHY_VDDQL_3
DDRRPHY_VDDQL_4
DDRRPHY_VDDQL_5
DDRRPHY_VDDQL_6

DDR_AVSS

| | |
|-----|------------------|
| B6 | LPDDR4_CLKP_B |
| F5 | |
| B1 | LPDDR4_A1_A |
| F4 | LPDDR4_CKE1_A |
| D9 | LPDDR4_A3_B |
| B7 | LPDDR4_A5_B |
| A7 | LPDDR4_A1_B |
| A8 | LPDDR4_ODT0_CA_B |
| C1 | LPDDR4_ODT0_CA_A |
| A5 | LPDDR4_CLKN_B |
| D6 | LPDDR4_CKE0_B |
| C2 | LPDDR4_A0_A |
| C4 | LPDDR4_A3_A |
| B8 | LPDDR4_A0_B |
| C5 | LPDDR4_A4_A |
| E4 | LPDDR4_A2_A |
| D5 | LPDDR4_A5_A |
| E6 | LPDDR4_CKE1_B |
| E11 | LPDDR4_A2_B |
| E9 | LPDDR4_A4_B |
| F8 | |
| F7 | |
| B3 | LPDDR4_CKE0_A |
| B4 | LPDDR4_CLKP_A |
| A4 | LPDDR4_CLKN_A |
| A2 | LPDDR4_CS0n_A |
| B2 | LPDDR4_CS1n_A |
| E8 | LPDDR4_CS1n_B |
| D8 | LPDDR4_CS0n_B |
| F11 | LPDDR4_RESETn |

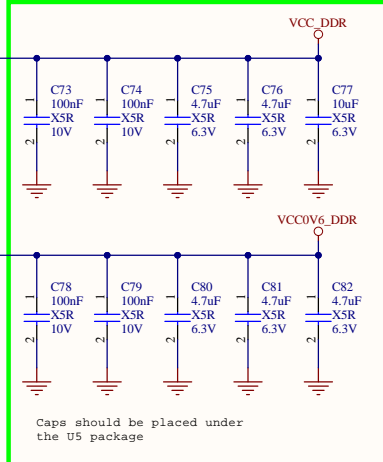
H7 DDR_RZQ R44 1 2 120R 1% OVCC_DDR

P8 DDR_VREFOUT

| | |
|-----|--|
| H9 | |
| H11 | |
| H12 | |
| H14 | |
| H15 | |
| J9 | |
| M9 | |

| | |
|-----|--|
| J11 | |
| J12 | |
| J14 | |
| K10 | |
| L10 | |
| M10 | |

J8



For DDR4/DDR3/LPDDR3 mode,
a 120 ohm +/-1% tolerance external
resistor must be connected between
the DDR_RZQ pin and VDD pin

For LPDDR4/LPDDR4x mode,
a 120 ohm +/-1% tolerance external
resistor must be connected between
the DDR_RZQ pin and DDRPHY_VDDQ pin

RK3568_I(VCCIO2 Domain)

U51

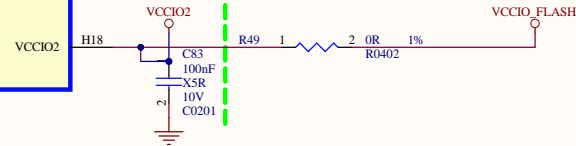
VCCIO2 Domain

Operating Voltage=1.8V/3.3V

| | | | | | |
|------------------|--------------|--------------|-----|----------|-----------------------------|
| EMMC_D0 | / FLASH_D0 | / GPIO1_B4_u | A24 | GPIO1_B4 | eMMC D0/FLASH D0 |
| EMMC_D1 | / FLASH_D1 | / GPIO1_B5_u | C21 | GPIO1_B5 | eMMC D1/FLASH D1 |
| EMMC_D2 | / FLASH_D2 | / GPIO1_B6_u | B24 | GPIO1_B6 | eMMC D2/FLASH D2 |
| EMMC_D3 | / FLASH_D3 | / GPIO1_B7_u | D21 | GPIO1_B7 | eMMC D3/FLASH D3 |
| EMMC_D4 | / FLASH_D4 | / GPIO1_C0_u | A25 | GPIO1_C0 | eMMC D4/FLASH D4 |
| EMMC_D5 | / FLASH_D5 | / GPIO1_C1_u | E21 | GPIO1_C1 | eMMC D5/FLASH D5 |
| EMMC_D6 | / FLASH_D6 | / GPIO1_C2_u | E22 | GPIO1_C2 | eMMC D6/FLASH D6 |
| EMMC_D7 | / FLASH_D7 | / GPIO1_C3_u | B25 | GPIO1_C3 | eMMC D7/FLASH D7 |
| EMMC_CMD | / FLASH_WRn | / GPIO1_C4_u | B22 | GPIO1_C4 | eMMC CMD/FLASH WRn |
| EMMC_CLKOUT | / FSPI_CSIn | / FLASH_DQS | A23 | GPIO1_C5 | eMMC CLKOUT/FLASH DQS |
| EMMC_DATA_STROBE | / FSPI_CSIn | / FLASH_CLE | A26 | GPIO1_C6 | eMMC DATA STROBE/FLASH CLE |
| EMMC_RSTn | / FSPI_D2 | / FLASH_WPn | F20 | GPIO1_C7 | eMMC RSTn/FSPI D2/FLASH WPn |
| FSPI_CLK | / FLASH_ALE | / GPIO1_D0_u | A22 | GPIO1_D0 | FSPI_CLK/FLASH ALE |
| FSPI_D0 | / FLASH_RDY | / GPIO1_D1_u | C24 | GPIO1_D1 | FSPI D0/FLASH RDY |
| FSPI_D1 | / FLASH_RDn | / GPIO1_D2_u | D23 | GPIO1_D2 | FSPI D1/FLASH RDn |
| FSPI_CS0n | / FLASH_CS0n | / GPIO1_D3_u | C23 | GPIO1_D3 | FSPI CS0n/FLASH CS0n |
| FSPI_D3 | / FLASH_CSIn | / GPIO1_D4_u | A27 | GPIO1_D4 | FSPI D3/FLASH CSIn |

Default is determined by Pin
FLASH_VOL_SEL/GPIO0_A7_u:
L:VCCIO2 must supply 3.3V
H:VCCIO2 must supply 1.8V

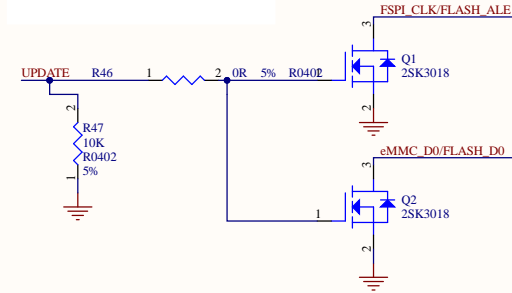
RK3568-Socket



注意，上电和复位的时候：

如果UPDATE为低，因此2SK3018不导通。eMMC_D0/FLASH_D0保持默认电平(高)。

如果UPDATE为高电平，2SK3018导通，eMMC D0/FLASH_D0此时就会接地，为低电平，工作在MASKROM模式，可以烧写系统



RK3568_J(VCCIO3 Domain)

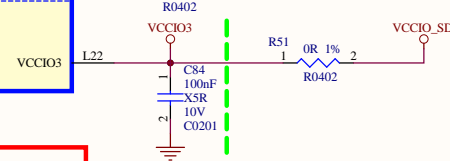
U51

VCCIO3 Domain

Operating Voltage=1.8V/3.3V

| | | | | | | | |
|------------|---------------|-----------------|--------------|--------------|--------------------|-----------|------------|
| SDMMC0_D0 | / UART2_TX_M1 | / UART6_TX_M1 | / PWM8_M1 | / GPIO1_D5_u | J25 | GPIO1_D5 | SDMMC0_D0 |
| SDMMC0_D1 | / UART2_RX_M1 | / UART6_RX_M1 | / PWM9_M1 | / GPIO1_D6_u | J24 | GPIO1_D6 | SDMMC0_D1 |
| SDMMC0_D2 | / ARMATA0_TCK | / UART5_CTSn_M0 | / GPIO1_D7_u | H26 | GPIO1_D7 | SDMMC0_D2 | |
| SDMMC0_D3 | / ARMATA0_TMS | / UART5_RTSn_M0 | / GPIO2_A0_u | J23 | GPIO2_A0 | SDMMC0_D3 | |
| SDMMC0_CMD | / PWM10_M1 | / UART5_RX_M0 | / CAN0_TX_M1 | / GPIO2_A1_u | H27 | GPIO2_A1 | SDMMC0_CMD |
| SDMMC0_CLK | / TEST_CLKOUT | / UART5_TX_M0 | / CAN0_RX_M1 | / GPIO2_A2_d | H28 R50 1 22R 5% 2 | GPIO2_A2 | SDMMC0_CLK |

RK3568-Socket



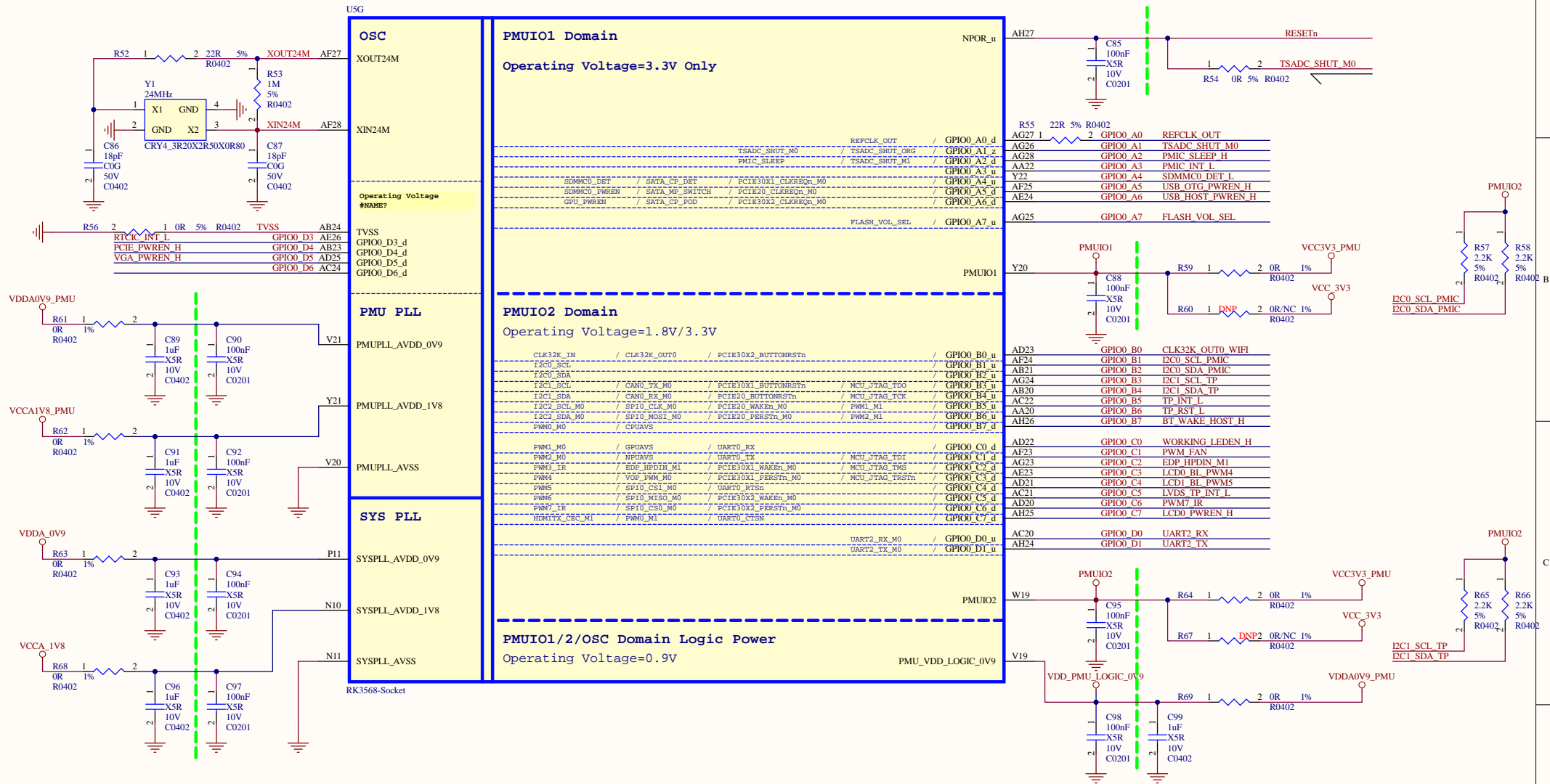
Note:

Caps of between dashed green lines and U5 should be placed under the U5 package

| | |
|-----------|-----------------------------|
| Title: | ATK_RK3568_Core v1.3.PrjPcb |
| Author: | ALIENTEK |
| Date: | 2023-07-12 |
| Revision: | V1.3 |
| Size: | A3 |
| File: | ATK_RK3568_Flash_SD.SchDoc |
| Version: | |



RK3568_G(OSC/PLL/PMUIO1/2)



The schematic diagram illustrates the power plane for the RK3568-Socket, showing various power rails and decoupling capacitors. The diagram is divided into several sections by a vertical green dashed line.

Left Section (RK3568-Socket):

- VDD_CPU:** Includes pins J15, K15, K16, K17, K18, L15, L16, L17, L18, and M17. The rail is labeled **VDD_CPU_COM** at pin M15.
- VDD_LOGIC:** Includes pins L12, M12, N13, N16, P13, P16, R12, R16, T12, and T16. The rail is labeled **VDD_LOGIC** at pin M12.
- VDD_GPU:** Includes pins R13, T13, U11, U12, and U13. The rail is labeled **VDD_GPU** at pin R13.
- VDD_NPU:** Includes pins M19, N19, P18, P19, and P20. The rail is labeled **VDD_NPU** at pin M19.

Right Section (U5D):

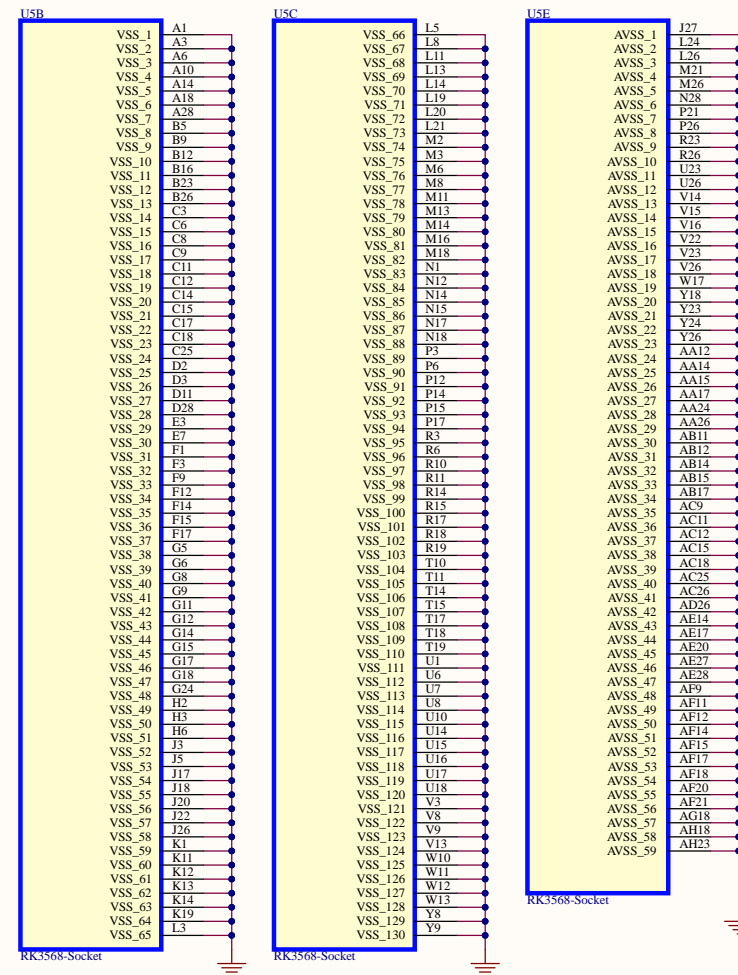
- VDD_CPU:** Includes pins C103, C104, C109, and C111. The rail is labeled **VDD_CPU** at pin C103.
- VDD_LOGIC:** Includes pins C110, C111, C115, and C116. The rail is labeled **VDD_LOGIC** at pin C110.
- VDD_GPU:** Includes pins C112, C113, C114, C115, and C116. The rail is labeled **VDD_GPU** at pin C112.
- VDD_NPU:** Includes pins C117, C118, C119, and C120. The rail is labeled **VDD_NPU** at pin C117.


Decoupling Capacitors:

- C100, C101, C102:** 100nF, 1uF, and 10uF capacitors, respectively, connected to ground.
- C103, C104, C109, C111:** 22uF capacitors, connected to ground.
- C110, C112, C113, C114, C115, C116:** 22uF capacitors, connected to ground.
- C117, C118, C119, C120:** 22uF capacitors, connected to ground.

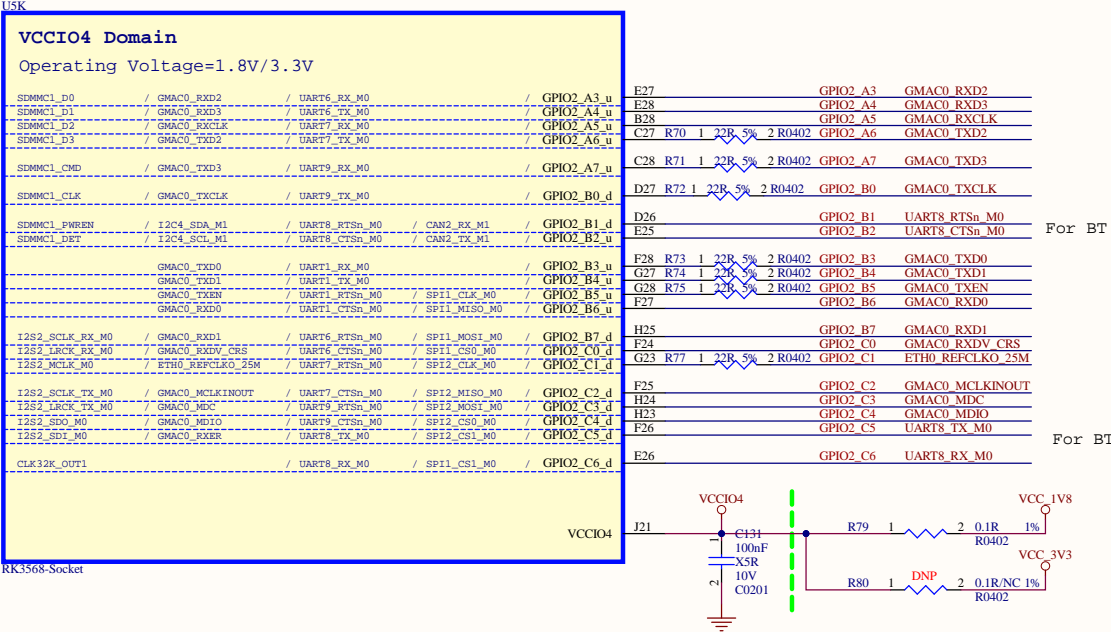
Notes:

- Caps should be placed under the U5 package** (referring to the VDD_CPU and VDD_LOGIC rails).
- Caps should be placed close to the U5 package** (referring to the VDD_GPU and VDD_NPU rails).

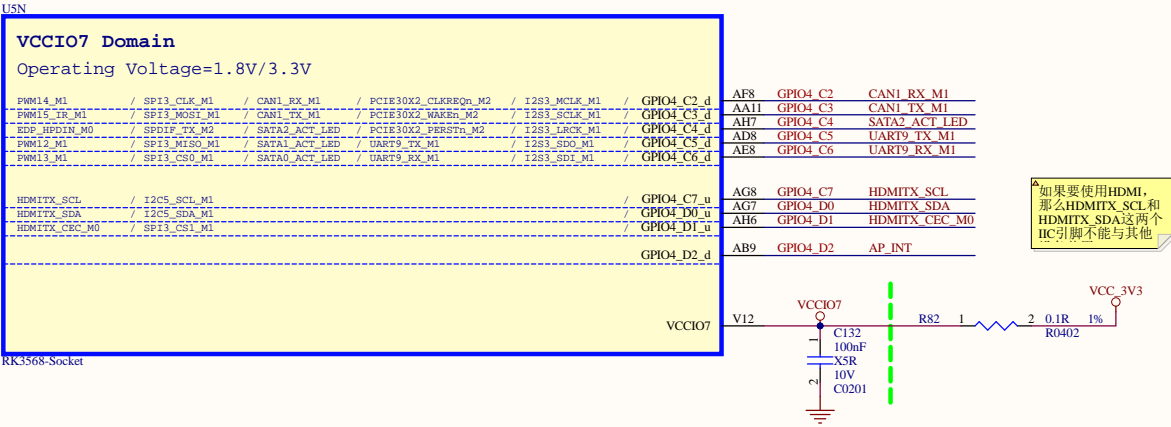


| | |
|---------------------------------------|--|
| Title: ATK_RK3568_Core v1.3.PriPcb |  正点原子 |
| Author: ALIENTEK | |
| Date: 2023-07-12 | |
| Revision: | |
| Size: A3 | |
| File: ATK_RK3568_Power_GND.SchDoc | |
| Version: | |

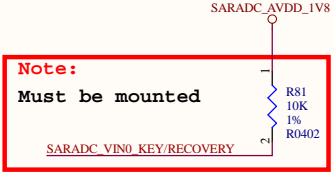
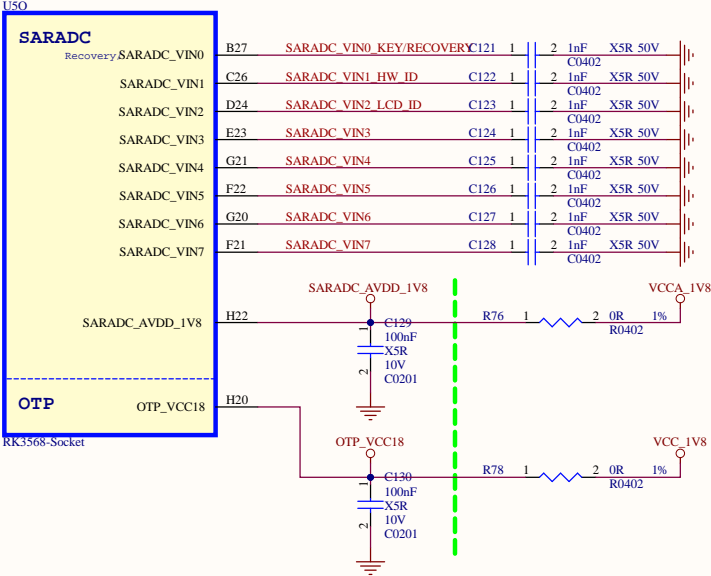
RK3568_K(VCCIO4 Domain)



RK3568_N(VCCIO7 Domain)

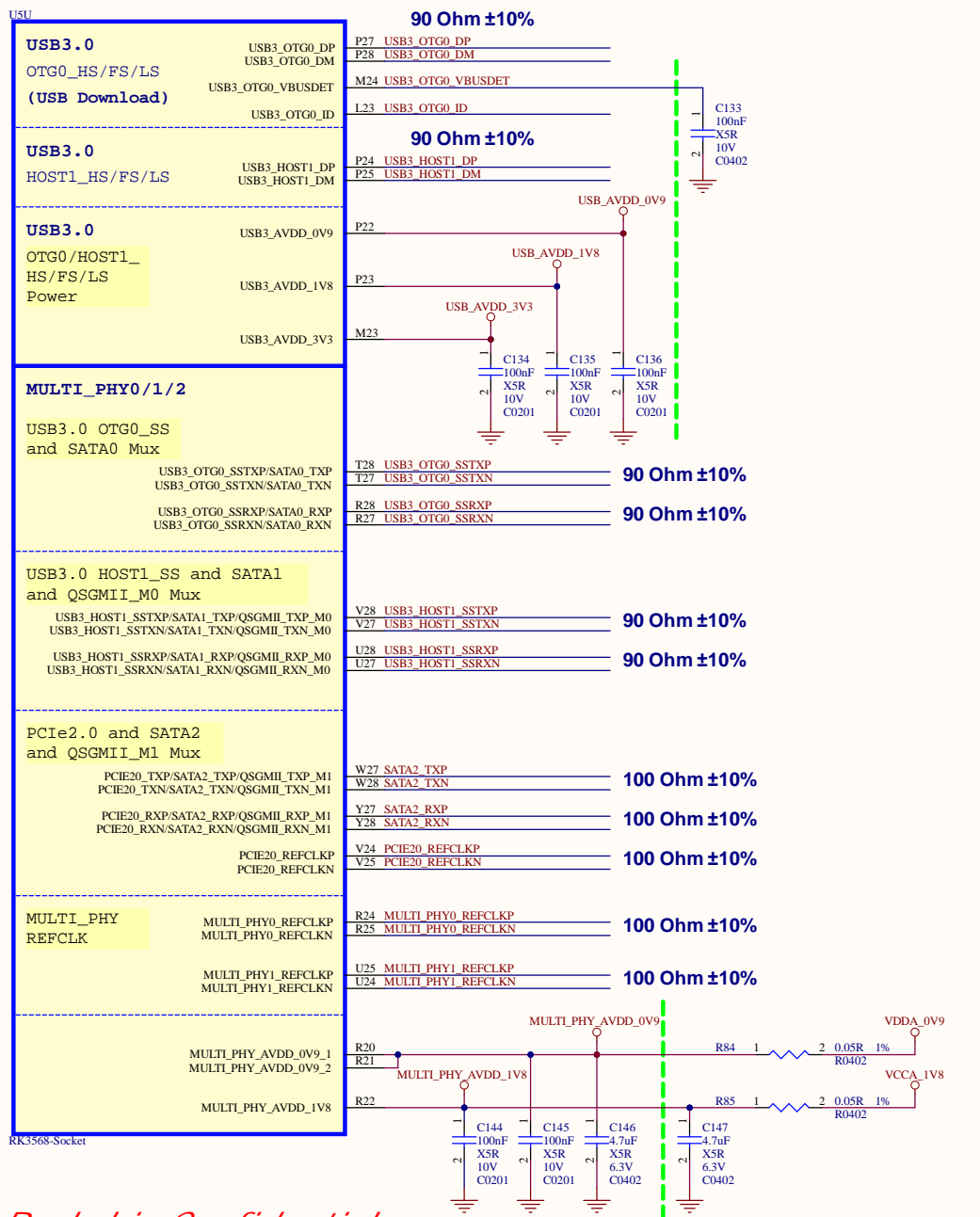


RK3568_O(SARADC/OTP)



Caps of between dashed green lines and U5 should be placed under the U5 package

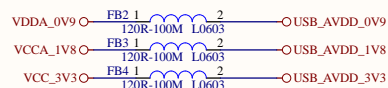
RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



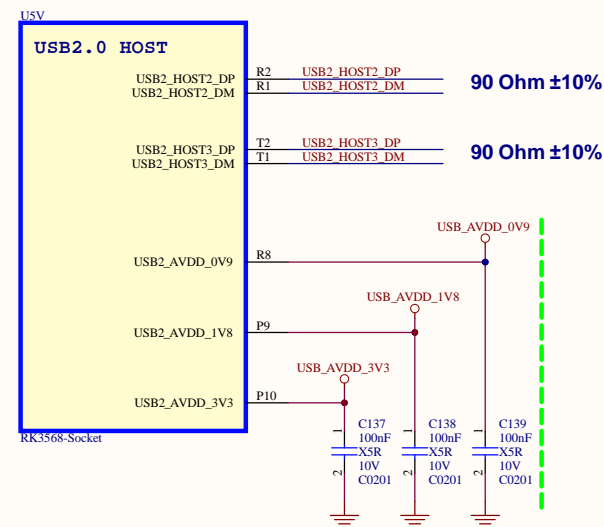
Rockchip Confidential

Note:

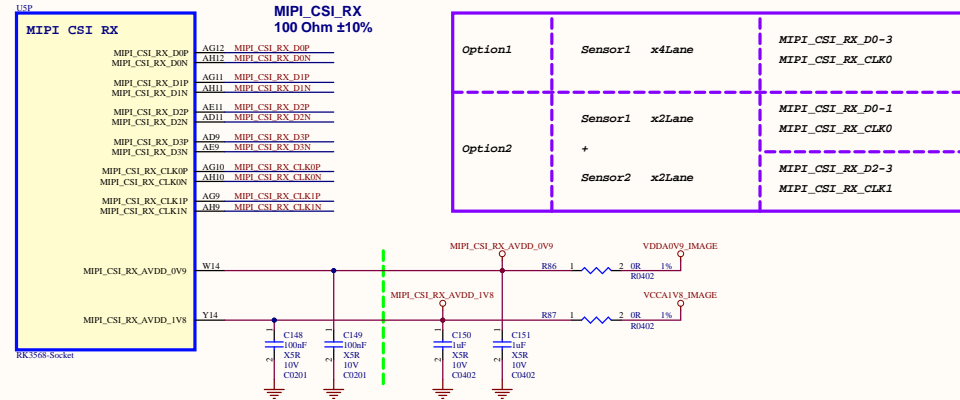
Caps of between dashed green lines and U5 should be placed under the U5 package.
Other caps should be placed close to the U5 package



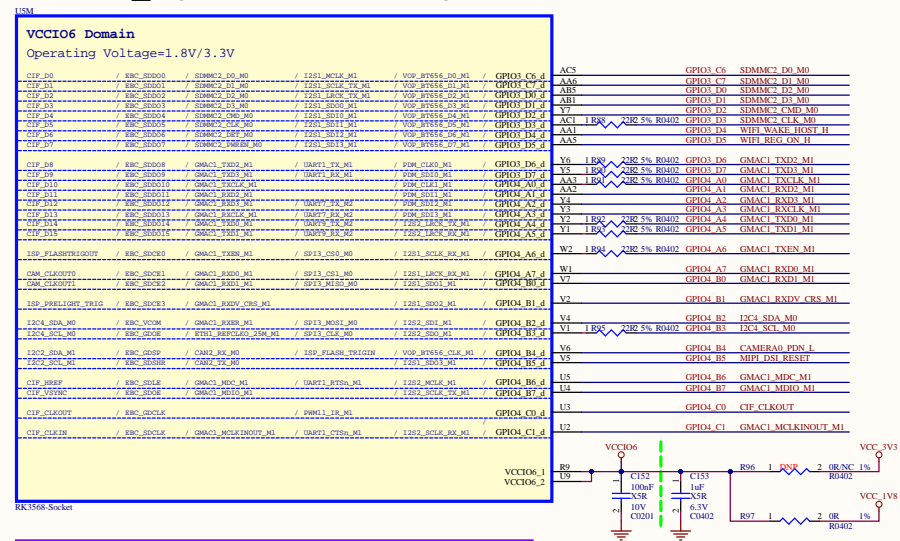
RK3568_V(USB2.0 HOST)



RK3568_P(MIPI_CSI_RX)



RK3568_M(VCCIO6 Domain)



| Mode | 16bit | 12bit | 10bit | 8bit |
|---------|-------|-------|-------|------|
| CIF_D0 | D0 | -- | -- | -- |
| CIF_D1 | D1 | -- | -- | -- |
| CIF_D2 | D2 | -- | -- | -- |
| CIF_D3 | D3 | -- | -- | -- |
| CIF_D4 | D4 | D0 | -- | -- |
| CIF_D5 | D5 | D1 | -- | -- |
| CIF_D6 | D6 | D2 | D0 | -- |
| CIF_D7 | D7 | D3 | D1 | -- |
| CIF_D8 | D8 | D4 | D2 | D0 |
| CIF_D9 | D9 | D5 | D3 | D1 |
| CIF_D10 | D10 | D6 | D4 | D2 |
| CIF_D11 | D11 | D7 | D5 | D3 |
| CIF_D12 | D12 | D8 | D6 | D4 |
| CIF_D13 | D13 | D9 | D7 | D5 |
| CIF_D14 | D14 | D10 | D8 | D6 |
| CIF_D15 | D15 | D11 | D9 | D7 |

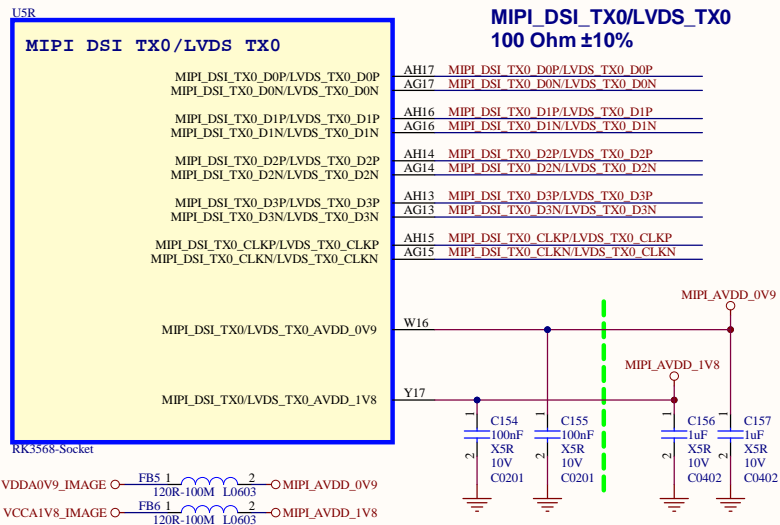
Note:

Caps of between dashed green lines and U5 should be placed under the U5 package.
Other caps should be placed close to the U5 package

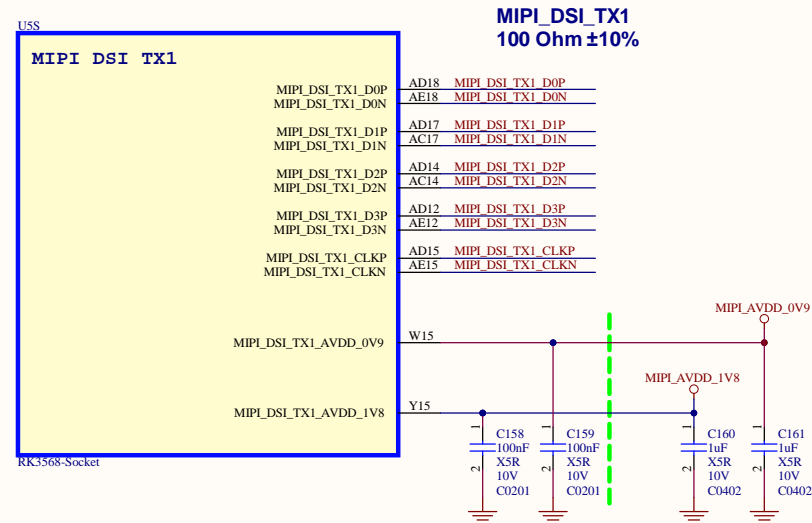
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Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

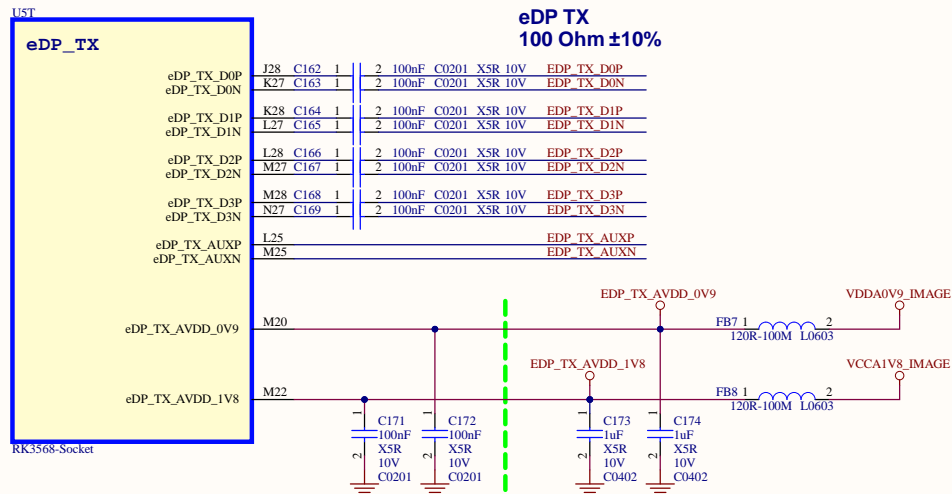
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



RK3568_S(MIPI_DSI_TX1)



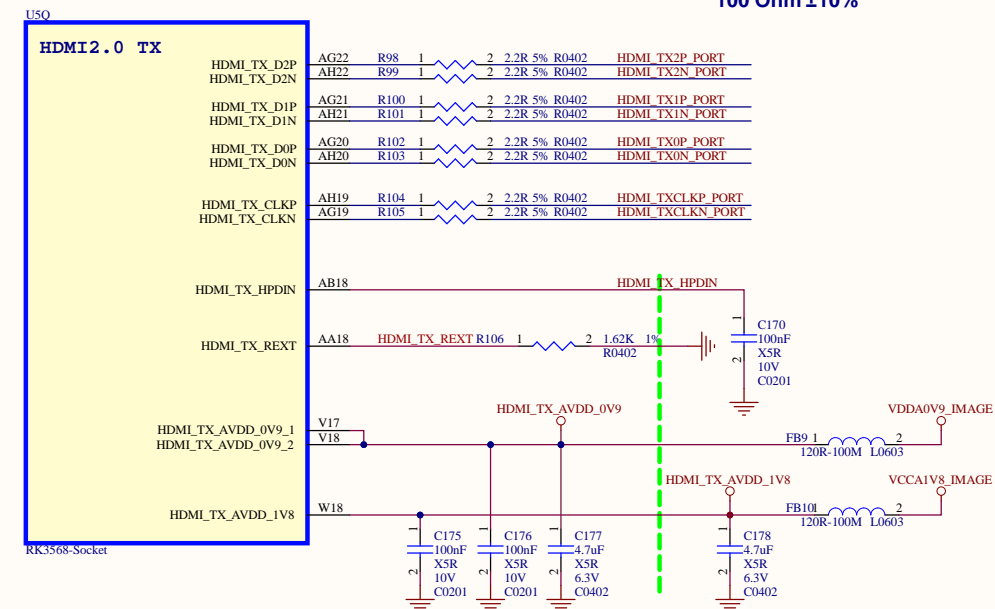
RK3568_T(eDP TX)



Note:

Caps of between dashed green lines and U5 should be placed under the U5 package.
Other caps should be placed close to the U5 package

RK3568_Q(HDMI2.0 TX)



| | | | |
|-----------|-----------------------------|----------|----------------------------------|
| Title: | ATK_RK3568_Core v1.3.PrjPcb | Size: | |
| Author: | ALIENTEK | File: | |
| Date: | 2023-07-12 | File: | ATK_RK3568_VO Interface_1.SchDoc |
| Revision: | V1.3 | Version: | |



RK3568_L(VCCIO5 Domain)

USL

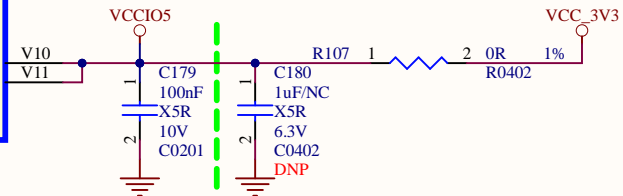
VCCIO5 Domain

Operating Voltage=1.8V/3.3V

| | | | | | | | | | | | | | |
|-------------|---|------------------|---|---------------------|---|---------------------|---|-----------------|---|------------|-----|----------|---------------------|
| LCDC_D0 | / | VOP_BT656_D0_M0 | / | SPI0_MISO_M1 | / | PCIE20_CLKREQn_M1 | / | I2S1_MCLK_M2 | / | GPIO2_D0_d | AG6 | GPIO2_D0 | GMAC1_INT/PMEB |
| LCDC_D1 | / | VOP_BT656_D1_M0 | / | SPI0_MOSI_M1 | / | PCIE20_WAKEn_M1 | / | I2S1_SCLK_TX_M2 | / | GPIO2_D1_d | AD7 | GPIO2_D1 | GMAC1_RSTn |
| LCDC_D2 | / | VOP_BT656_D2_M0 | / | SPI0_CS0_M1 | / | PCIE30X1_CLKREQn_M1 | / | I2S1_LRCK_TX_M2 | / | GPIO2_D2_d | AC8 | GPIO2_D2 | GMAC0_INT/PMEB |
| LCDC_D3 | / | VOP_BT656_D3_M0 | / | SPI0_CLK_M1 | / | PCIE30X1_WAKEn_M1 | / | I2S1_SDI0_M2 | / | GPIO2_D3_d | AC7 | GPIO2_D3 | GMAC0_RSTn |
| LCDC_D4 | / | VOP_BT656_D4_M0 | / | SPI2_CS1_M1 | / | PCIE30X2_CLKREQn_M1 | / | I2S1_SDI1_M2 | / | GPIO2_D4_d | AF5 | GPIO2_D4 | PCIE30X2_CLKREQn_M1 |
| LCDC_D5 | / | VOP_BT656_D5_M0 | / | SPI2_CS0_M1 | / | PCIE30X2_WAKEn_M1 | / | I2S1_SDI2_M2 | / | GPIO2_D5_d | AF6 | GPIO2_D5 | PCIE30X2_WAKEn_M1 |
| LCDC_D6 | / | VOP_BT656_D6_M0 | / | SPI2_MOSI_M1 | / | PCIE30X2_PERSTn_M1 | / | I2S1_SDI3_M2 | / | GPIO2_D6_d | AD6 | GPIO2_D6 | PCIE30X2_PERSTn_M1 |
| LCDC_D7 | / | VOP_BT656_D7_M0 | / | SPI2_MISO_M1 | / | UART8_TX_M1 | / | I2S1_SDO0_M2 | / | GPIO2_D7_d | AH5 | GPIO2_D7 | PCIE30X2_PRSTn_L |
| | | | | | | | | | | | AH4 | GPIO3_A0 | BT_REG_ON_H |
| LCDC_CLK | / | VOP_BT656_CLK_M0 | / | SPI2_CLK_M1 | / | UART8_RX_M1 | / | I2S1_SDO1_M2 | / | GPIO3_A0_d | AB8 | GPIO3_A1 | SPI1_CS0_M1 |
| LCDC_D8 | / | VOP_BT1120_D0 | / | SPI1_CS0_M1 | / | PCIE30X1_PERSTn_M1 | / | SDMMC2_D0_M1 | / | GPIO3_A1_d | AE5 | GPIO3_A2 | HOST_WAKE_BT_H |
| LCDC_D9 | / | VOP_BT1120_D1 | / | GMAC1_TXD2_M0 | / | I2S3_MCLK_M0 | / | SDMMC2_D1_M1 | / | GPIO3_A2_d | AG4 | GPIO3_A3 | I2S3_SCLK_M0 |
| LCDC_D10 | / | VOP_BT1120_D2 | / | GMAC1_TXD3_M0 | / | I2S3_SCLK_M0 | / | SDMMC2_D2_M1 | / | GPIO3_A3_d | AF4 | GPIO3_A4 | I2S3_LRCK_M0 |
| LCDC_D11 | / | VOP_BT1120_D3 | / | GMAC1_RXD2_M0 | / | I2S3_LRCK_M0 | / | SDMMC2_D3_M1 | / | GPIO3_A4_d | AH3 | GPIO3_A5 | I2S3_SDO_M0 |
| LCDC_D12 | / | VOP_BT1120_D4 | / | GMAC1_RXD3_M0 | / | I2S3_SDO_M0 | / | SDMMC2_CMD_M1 | / | GPIO3_A5_d | AG3 | GPIO3_A6 | I2S3_SDI_M0 |
| LCDC_D13 | / | VOP_BT1120_CLK | / | GMAC1_TXCLK_M0 | / | I2S3_SDI_M0 | / | SDMMC2_CLK_M1 | / | GPIO3_A6_d | AH2 | GPIO3_A7 | PCIECLKIC_OE_H |
| LCDC_D14 | / | VOP_BT1120_D5 | / | GMAC1_RXCLK_M0 | / | SDMMC2_DET_M1 | / | SDMMC2_DET_M1 | / | GPIO3_A7_d | AG2 | GPIO3_B0 | 5G_DISABLE |
| LCDC_D15 | / | VOP_BT1120_D6 | / | ETH1_REFCLKO_25M_M0 | / | SDMMC2_PWREN_M1 | / | SDMMC2_PWREN_M1 | / | GPIO3_B0_d | AG1 | GPIO3_B1 | UART4_RX_M1 |
| LCDC_D16 | / | VOP_BT1120_D7 | / | GMAC1_RXD0_M0 | / | UART4_RX_M1 | / | PWM8_M0 | / | GPIO3_B1_d | AF2 | GPIO3_B2 | UART4_TX_M1 |
| LCDC_D17 | / | VOP_BT1120_D8 | / | GMAC1_RXD1_M0 | / | UART4_TX_M1 | / | PWM9_M0 | / | GPIO3_B2_d | AF1 | GPIO3_B3 | I2C5_SCL_M0 |
| LCDC_D18 | / | VOP_BT1120_D9 | / | GMAC1_RXDV_CRS_M0 | / | I2C5_SCL_M0 | / | PDM_SDI0_M2 | / | GPIO3_B3_d | AE1 | GPIO3_B4 | I2C5_SDA_M0 |
| LCDC_D19 | / | VOP_BT1120_D10 | / | GMAC1_RXER_M0 | / | I2C5_SDA_M0 | / | PDM_SDI1_M2 | / | GPIO3_B4_d | AE2 | GPIO3_B5 | MIPICAM1_RST_L |
| LCDC_D20 | / | VOP_BT1120_D11 | / | GMAC1_TXD0_M0 | / | I2C3_SCL_M1 | / | PWM10_M0 | / | GPIO3_B5_d | AE3 | GPIO3_B6 | MIPICAM0_RST_L |
| LCDC_D21 | / | VOP_BT1120_D12 | / | GMAC1_TXD1_M0 | / | I2C3_SDA_M1 | / | PWM11_IR_M0 | / | GPIO3_B6_d | AD4 | GPIO3_B7 | UART3_TX_M1 |
| LCDC_D22 | / | PWM12_M0 | / | GMAC1_TXEN_M0 | / | UART3_TX_M1 | / | PDM_SDI2_M2 | / | GPIO3_B7_d | AD2 | GPIO3_C0 | UART3_RX_M1 |
| LCDC_D23 | / | PWM13_M0 | / | GMAC1_MCLKINOUT_M0 | / | UART3_RX_M1 | / | PDM_SDI3_M2 | / | GPIO3_C0_d | AD1 | GPIO3_C1 | SPI1_MOSI_M1 |
| LCDC_HSYNC | / | VOP_BT1120_D13 | / | SPI1_MOSI_M1 | / | PCIE20_PERSTn_M1 | / | I2S1_SDO2_M2 | / | GPIO3_C1_d | AA7 | GPIO3_C2 | SPI1_MISO_M1 |
| LCDC_VSYNC | / | VOP_BT1120_D14 | / | SPI1_MISO_M1 | / | UART5_TX_M1 | / | I2S1_SDO3_M2 | / | GPIO3_C2_d | AC4 | GPIO3_C3 | SPI1_CLK_M1 |
| LCDC_DEN | / | VOP_BT1120_D15 | / | SPI1_CLK_M1 | / | UART5_RX_M1 | / | I2S1_SCLK_RX_M2 | / | GPIO3_C3_d | AC3 | GPIO3_C4 | LVDS_TP_RST_L |
| PWM14_M0 | / | VOP_PWM_M1 | / | GMAC1_MDC_M0 | / | UART7_TX_M1 | / | PDM_CLK1_M2 | / | GPIO3_C4_d | AC2 | GPIO3_C5 | |
| PWM15_IR_M0 | / | SPDIF_TX_M1 | / | GMAC1_MDIO_M0 | / | UART7_RX_M1 | / | I2S1_LRCK_RX_M2 | / | GPIO3_C5_d | | | |

RK3568-Socket

VCCIO5_1
VCCIO5_2



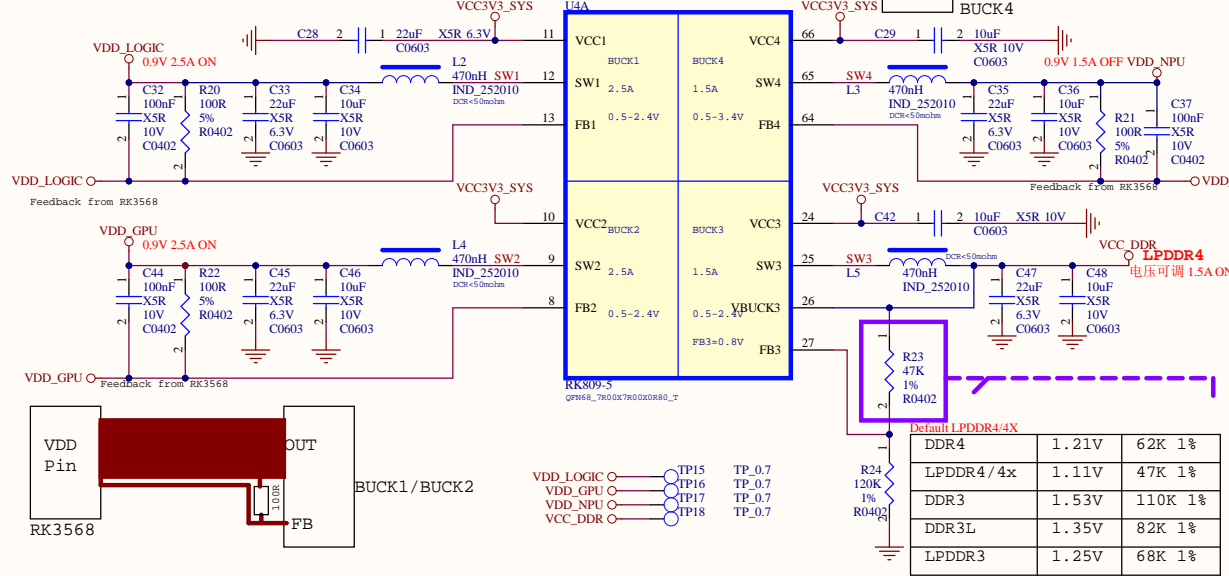
Note:

Caps of between dashed green lines and U5 should be placed under the U5 package

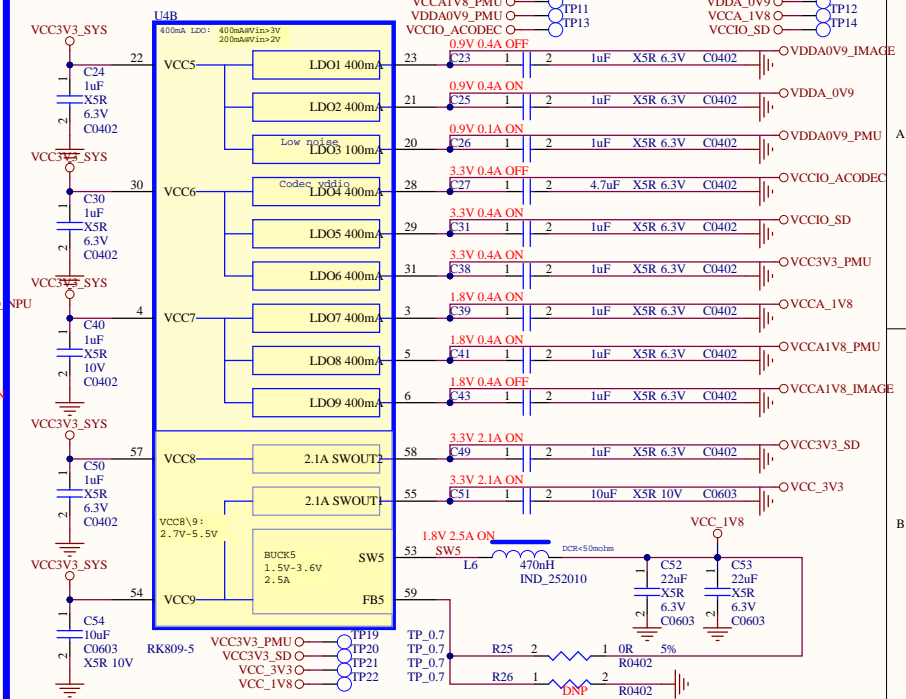
Rockchip Confidential

| | | |
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| Author: ALIENTEK | Size: A4 | |
| Date: 2023-07-12 | File: ATK_RK3568_VO_Interface_2.SchDoc | |
| Revision: V1.3 | Version: | |
| | | |

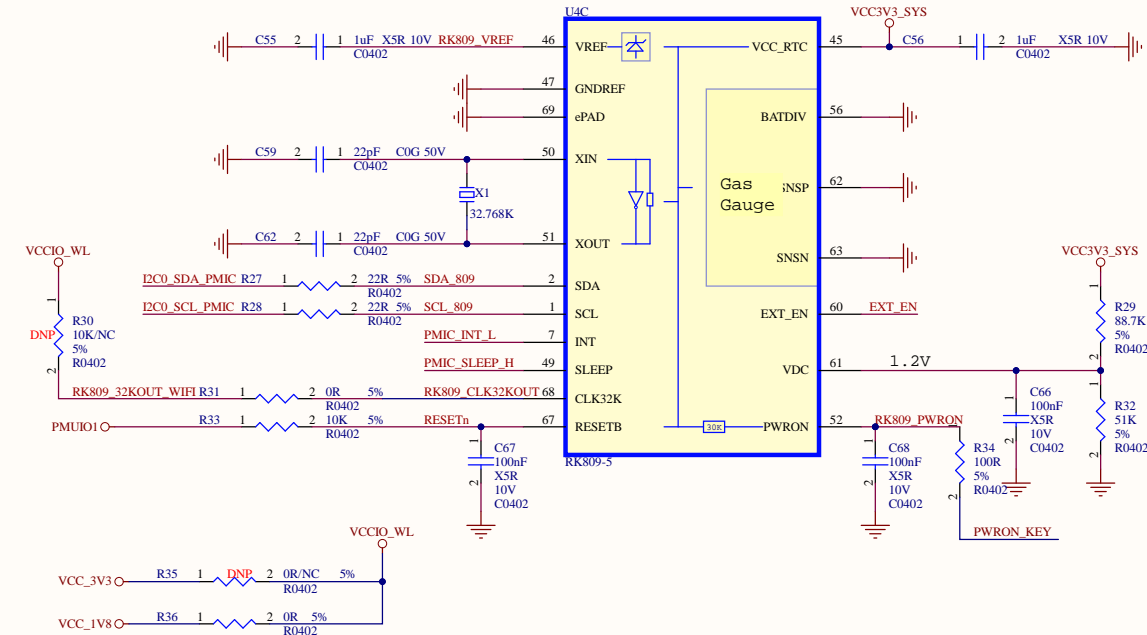
PMIC RK809 DCDC



PMIC RK809 LDO



PMIC RK809 Management



PMIC RK809 CODEC

