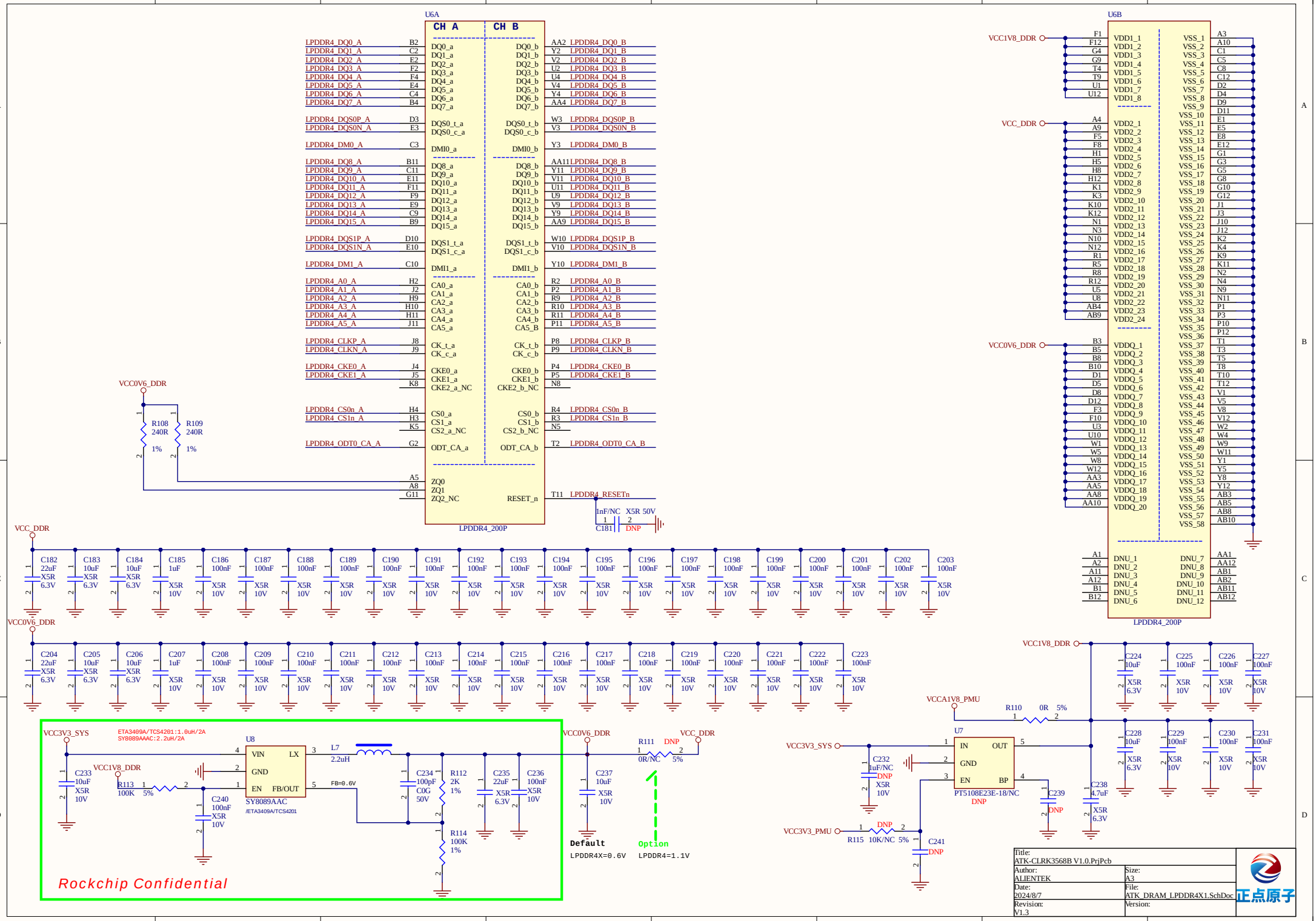
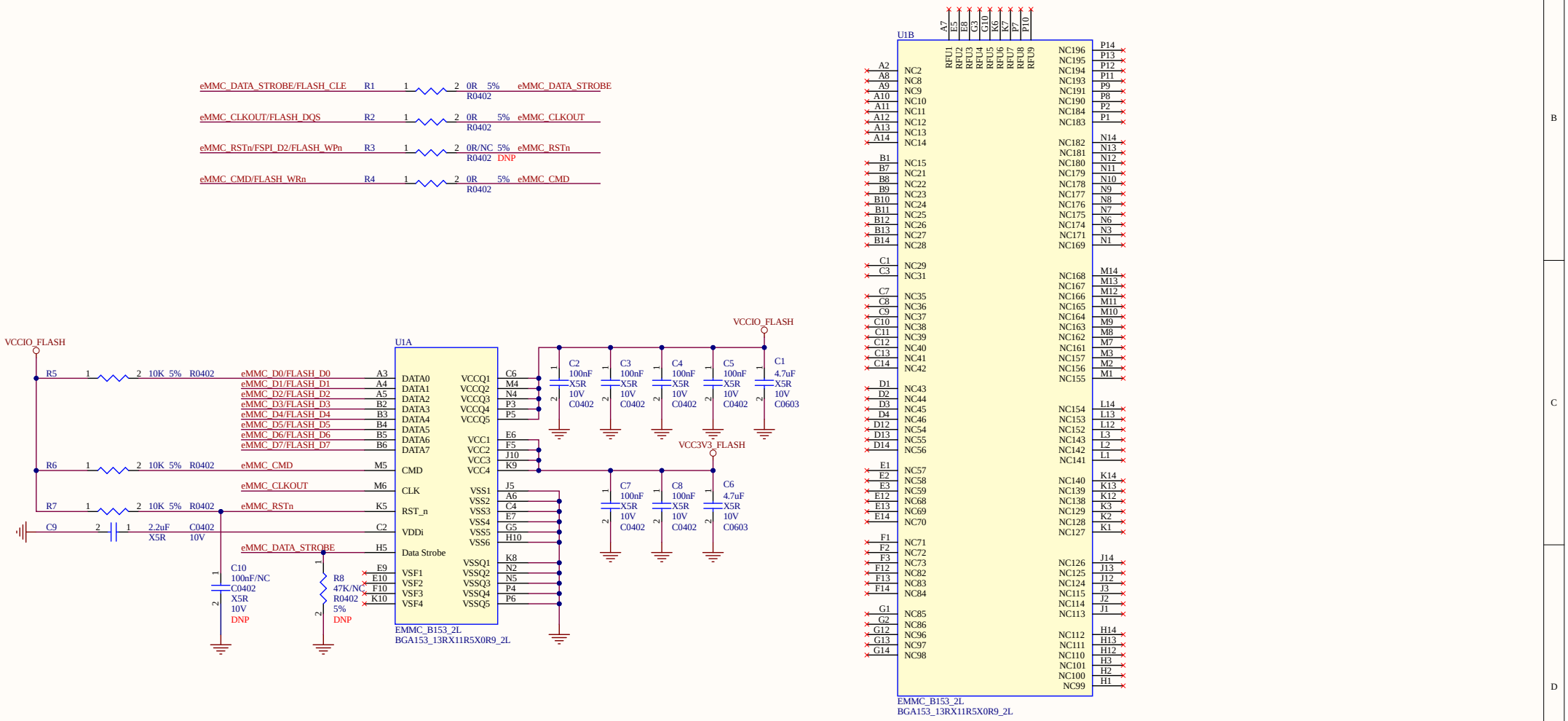
Revision History

Version	Date	By	Change Dsecription
V1.2	2023-6-30	zuozhongkai	1:Initial release version

Title: ATK-CLRK3568B V1.0.PrjPcb	
Author: ALIENTEK	Size: A4
Date: 2024/8/7	File: 01_ReviSion History.SchDoc
Revision: V1.3	Version:

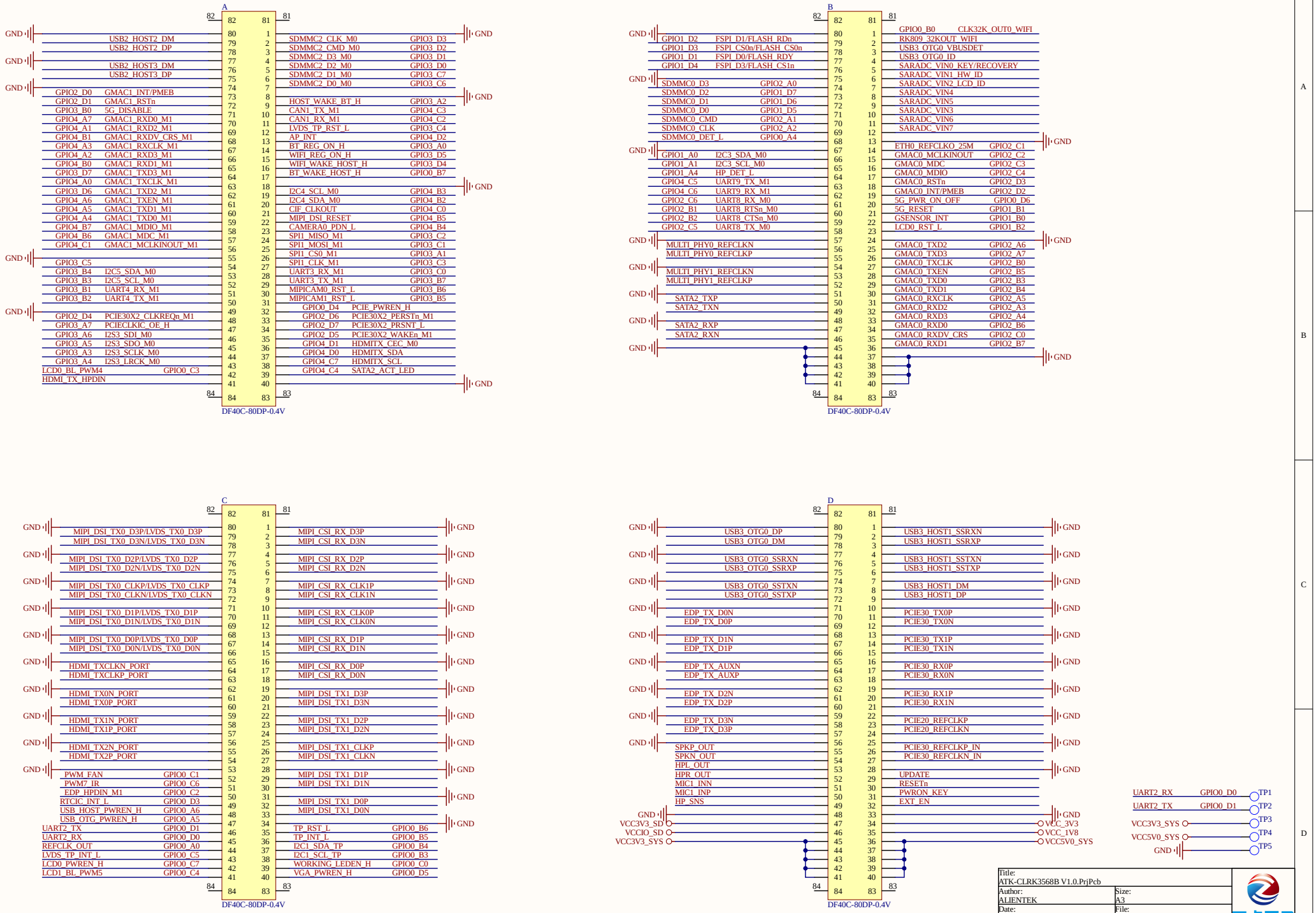
正点原子


U6A
CH A
CH B
LPDDR4_200P
U6B
LPDDR4_200P
VCC1V8_DDR
VCC_DDR
VCC0V6_DDR
R108 240R 1%
R109 240R 1%
1nF/NC X5R 50V
C181 DNP
C182 22uF X5R 6.3V
C183 10uF X5R 6.3V
C184 10uF X5R 6.3V
C185 1uF X5R 10V
C186 100nF X5R 10V
C187 100nF X5R 10V
C188 100nF X5R 10V
C189 100nF X5R 10V
C190 100nF X5R 10V
C191 100nF X5R 10V
C192 100nF X5R 10V
C193 100nF X5R 10V
C194 100nF X5R 10V
C195 100nF X5R 10V
C196 100nF X5R 10V
C197 100nF X5R 10V
C198 100nF X5R 10V
C199 100nF X5R 10V
C200 100nF X5R 10V
C201 100nF X5R 10V
C202 100nF X5R 10V
C203 100nF X5R 10V
C204 22uF X5R 6.3V
C205 10uF X5R 6.3V
C206 10uF X5R 6.3V
C207 1uF X5R 10V
C208 100nF X5R 10V
C209 100nF X5R 10V
C210 100nF X5R 10V
C211 100nF X5R 10V
C212 100nF X5R 10V
C213 100nF X5R 10V
C214 100nF X5R 10V
C215 100nF X5R 10V
C216 100nF X5R 10V
C217 100nF X5R 10V
C218 100nF X5R 10V
C219 100nF X5R 10V
C220 100nF X5R 10V
C221 100nF X5R 10V
C222 100nF X5R 10V
C223 100nF X5R 10V
VCC3V3_SYS
ETA3409A/TCS4201:1.0uH/2A
SY8089AAAC:2.2uH/2A
U8
VIN
LX
GND
EN
FB/OUT
SY8089AAC
/ETA3409A/TCS4201
L7 2.2uH
FB=0.6V
VCC1V8_DDR
R113 100K 5%
C233 10uF X5R 10V
C234 100pF C0G 50V
R112 2K 1%
C235 22uF X5R 6.3V
C236 100nF X5R 10V
C237 10uF X5R 10V
C240 100nF X5R 10V
R114 100K 1%
R111 DNP 0R/NC 5%
Default
LPDDR4X=0.6V
Option
LPDDR4=1.1V
Rockchip Confidential
VCCA1V8_PMU
R110 0R 5%
C224 10uF X5R 6.3V
C225 100nF X5R 10V
C226 100nF X5R 10V
C227 100nF X5R 10V
C228 10uF X5R 6.3V
C229 100nF X5R 10V
C230 100nF X5R 10V
C231 100nF X5R 10V
U7
IN
OUT
GND
EN
BP
PT5108E23E-18/NC
DNP
C232 1uF/NC DNP X5R 10V
C238 4.7uF X5R 6.3V
C239 DNP
VCC3V3_PMU
R115 10K/NC 5%
C241 DNP
Title:
ATK-CLRK3568B V1.0.PrjPcb
Author:
ALIENTEK
Size:
A3
Date:
2024/8/7
File:
ATK_DRAM_LPDDR4X1.SchDoc
Revision:
V1.3
Version:
正点原子

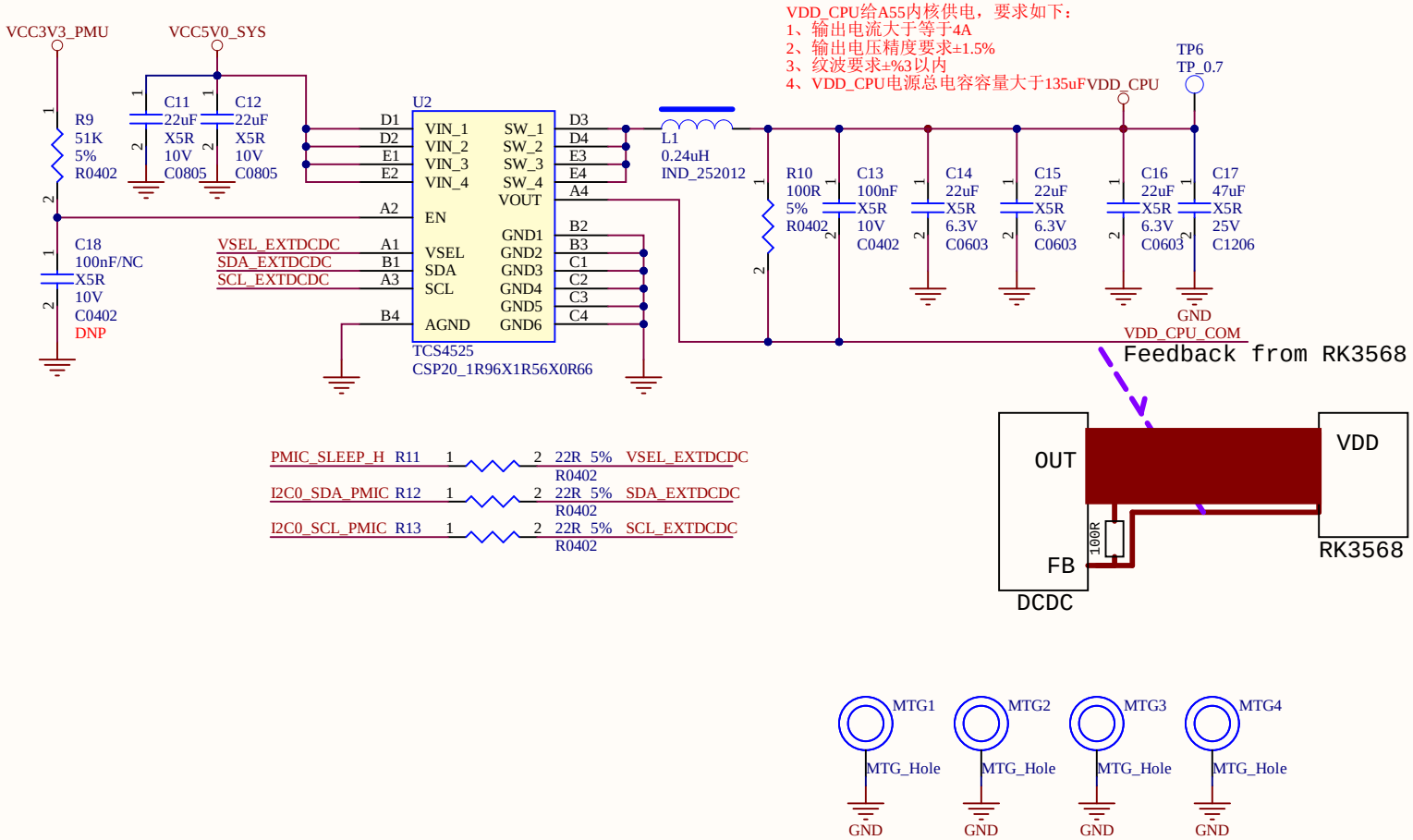


Title: ATK-CLRK3568B V1.0.PrjPcb	
Author: ALIENTEK	Size: A3
Date: 2024/8/7	File: ATK_Flash_EMMC Flash.SchDoc
Revision: V1.3	Version:

正点原子


A
B
C
D
DF40C-80DP-0.4V
GND
USB2_HOST2_DM
USB2_HOST2_DP
USB2_HOST3_DM
USB2_HOST3_DP
GPIO2_D0 GMAC1_INT/PMEB
GPIO2_D1 GMAC1_RSTn
GPIO3_B0 5G_DISABLE
GPIO4_A7 GMAC1_RXD0_M1
GPIO4_A1 GMAC1_RXD2_M1
GPIO4_B1 GMAC1_RXDV_CRS_M1
GPIO4_A3 GMAC1_RXCLK_M1
GPIO4_A2 GMAC1_RXD3_M1
GPIO4_B0 GMAC1_RXD1_M1
GPIO3_D7 GMAC1_TXD3_M1
GPIO4_A0 GMAC1_TXCLK_M1
GPIO3_D6 GMAC1_TXD2_M1
GPIO4_A6 GMAC1_TXEN_M1
GPIO4_A5 GMAC1_TXD1_M1
GPIO4_A4 GMAC1_TXD0_M1
GPIO4_B7 GMAC1_MDIO_M1
GPIO4_B6 GMAC1_MDC_M1
GPIO4_C1 GMAC1_MCLKINOUT_M1
GPIO3_C5
GPIO3_B4 I2C5_SDA_M0
GPIO3_B3 I2C5_SCL_M0
GPIO3_B1 UART4_RX_M1
GPIO3_B2 UART4_TX_M1
GPIO2_D4 PCIE30X2_CLKREQn_M1
GPIO3_A7 PCIECLKIC_OE_H
GPIO3_A6 I2S3_SDI_M0
GPIO3_A5 I2S3_SDO_M0
GPIO3_A3 I2S3_SCLK_M0
GPIO3_A4 I2S3_LRCK_M0
LCD0_BL_PWM4 GPIO0_C3
HDMI_TX_HPDIN
SDMMC2_CLK_M0 GPIO3_D3
SDMMC2_CMD_M0 GPIO3_D2
SDMMC2_D3_M0 GPIO3_D1
SDMMC2_D2_M0 GPIO3_D0
SDMMC2_D1_M0 GPIO3_C7
SDMMC2_D0_M0 GPIO3_C6
HOST_WAKE_BT_H GPIO3_A2
CAN1_TX_M1 GPIO4_C3
CAN1_RX_M1 GPIO4_C2
LVDS_TP_RST_L GPIO3_C4
AP_INT GPIO4_D2
BT_REG_ON_H GPIO3_A0
WIFI_REG_ON_H GPIO3_D5
WIFI_WAKE_HOST_H GPIO3_D4
BT_WAKE_HOST_H GPIO0_B7
I2C4_SCL_M0 GPIO4_B3
I2C4_SDA_M0 GPIO4_B2
CIF_CLKOUT GPIO4_C0
MIPI_DSI_RESET GPIO4_B5
CAMERA0_PDN_L GPIO4_B4
SPI1_MISO_M1 GPIO3_C2
SPI1_MOSI_M1 GPIO3_C1
SPI1_CS0_M1 GPIO3_A1
SPI1_CLK_M1 GPIO3_C3
UART3_RX_M1 GPIO3_C0
UART3_TX_M1 GPIO3_B7
MIPICAM0_RST_L GPIO3_B6
MIPICAM1_RST_L GPIO3_B5
GPIO0_D4 PCIE_PWREN_H
GPIO2_D6 PCIE30X2_PERSTn_M1
GPIO2_D7 PCIE30X2_PRSNT_L
GPIO2_D5 PCIE30X2_WAKEn_M1
GPIO4_D1 HDMITX_CEC_M0
GPIO4_D0 HDMITX_SDA
GPIO4_C7 HDMITX_SCL
GPIO4_C4 SATA2_ACT_LED
GPIO0_B0 CLK32K_OUT0_WIFI
RK809_32KOUT_WIFI
USB3_OTG0_VBUSDET
USB3_OTG0_ID
SARADC_VIN0_KEY/RECOVERY
SARADC_VIN1_HW_ID
SARADC_VIN2_LCD_ID
SARADC_VIN4
SARADC_VIN5
SARADC_VIN3
SARADC_VIN6
SARADC_VIN7
GPIO1_D2 FSPI_D1/FLASH_RDn
GPIO1_D3 FSPI_CS0n/FLASH_CS0n
GPIO1_D1 FSPI_D0/FLASH_RDY
GPIO1_D4 FSPI_D3/FLASH_CS1n
SDMMC0_D3 GPIO2_A0
SDMMC0_D2 GPIO1_D7
SDMMC0_D1 GPIO1_D6
SDMMC0_D0 GPIO1_D5
SDMMC0_CMD GPIO2_A1
SDMMC0_CLK GPIO2_A2
SDMMC0_DET_L GPIO0_A4
GPIO1_A0 I2C3_SDA_M0
GPIO1_A1 I2C3_SCL_M0
GPIO1_A4 HP_DET_L
GPIO4_C5 UART9_TX_M1
GPIO4_C6 UART9_RX_M1
GPIO2_C6 UART8_RX_M0
GPIO2_B1 UART8_RTSn_M0
GPIO2_B2 UART8_CTSn_M0
GPIO2_C5 UART8_TX_M0
MULTI_PHY0_REFCLKN
MULTI_PHY0_REFCLKP
MULTI_PHY1_REFCLKN
MULTI_PHY1_REFCLKP
SATA2_TXP
SATA2_TXN
SATA2_RXP
SATA2_RXN
ETH0_REFCLKO_25M GPIO2_C1
GMAC0_MCLKINOUT GPIO2_C2
GMAC0_MDC GPIO2_C3
GMAC0_MDIO GPIO2_C4
GMAC0_RSTn GPIO2_D3
GMAC0_INT/PMEB GPIO2_D2
5G_PWR_ON_OFF GPIO0_D6
5G_RESET GPIO1_B1
GSENSOR_INT GPIO1_B0
LCD0_RST_L GPIO1_B2
GMAC0_TXD2 GPIO2_A6
GMAC0_TXD3 GPIO2_A7
GMAC0_TXCLK GPIO2_B0
GMAC0_TXEN GPIO2_B5
GMAC0_TXD0 GPIO2_B3
GMAC0_TXD1 GPIO2_B4
GMAC0_RXCLK GPIO2_A5
GMAC0_RXD2 GPIO2_A3
GMAC0_RXD3 GPIO2_A4
GMAC0_RXD0 GPIO2_B6
GMAC0_RXDV_CRS GPIO2_C0
GMAC0_RXD1 GPIO2_B7
MIPI_DSI_TX0_D3P/LVDS_TX0_D3P
MIPI_DSI_TX0_D3N/LVDS_TX0_D3N
MIPI_DSI_TX0_D2P/LVDS_TX0_D2P
MIPI_DSI_TX0_D2N/LVDS_TX0_D2N
MIPI_DSI_TX0_CLKP/LVDS_TX0_CLKP
MIPI_DSI_TX0_CLKN/LVDS_TX0_CLKN
MIPI_DSI_TX0_D1P/LVDS_TX0_D1P
MIPI_DSI_TX0_D1N/LVDS_TX0_D1N
MIPI_DSI_TX0_D0P/LVDS_TX0_D0P
MIPI_DSI_TX0_D0N/LVDS_TX0_D0N
HDMI_TXCLKN_PORT
HDMI_TXCLKP_PORT
HDMI_TX0N_PORT
HDMI_TX0P_PORT
HDMI_TX1N_PORT
HDMI_TX1P_PORT
HDMI_TX2N_PORT
HDMI_TX2P_PORT
PWM_FAN GPIO0_C1
PWM7_IR GPIO0_C6
EDP_HPDIN_M1 GPIO0_C2
RTCIC_INT_L GPIO0_D3
USB_HOST_PWREN_H GPIO0_A6
USB_OTG_PWREN_H GPIO0_A5
UART2_TX GPIO0_D1
UART2_RX GPIO0_D0
REFCLK_OUT GPIO0_A0
LVDS_TP_INT_L GPIO0_C5
LCD0_PWREN_H GPIO0_C7
LCD1_BL_PWM5 GPIO0_C4
MIPI_CSI_RX_D3P
MIPI_CSI_RX_D3N
MIPI_CSI_RX_D2P
MIPI_CSI_RX_D2N
MIPI_CSI_RX_CLK1P
MIPI_CSI_RX_CLK1N
MIPI_CSI_RX_CLK0P
MIPI_CSI_RX_CLK0N
MIPI_CSI_RX_D1P
MIPI_CSI_RX_D1N
MIPI_CSI_RX_D0P
MIPI_CSI_RX_D0N
MIPI_DSI_TX1_D3P
MIPI_DSI_TX1_D3N
MIPI_DSI_TX1_D2P
MIPI_DSI_TX1_D2N
MIPI_DSI_TX1_CLKP
MIPI_DSI_TX1_CLKN
MIPI_DSI_TX1_D1P
MIPI_DSI_TX1_D1N
MIPI_DSI_TX1_D0P
MIPI_DSI_TX1_D0N
TP_RST_L GPIO0_B6
TP_INT_L GPIO0_B5
I2C1_SDA_TP GPIO0_B4
I2C1_SCL_TP GPIO0_B3
WORKING_LEDEN_H GPIO0_C0
VGA_PWREN_H GPIO0_D5
USB3_OTG0_DP
USB3_OTG0_DM
USB3_OTG0_SSRXN
USB3_OTG0_SSRXP
USB3_OTG0_SSTXN
USB3_OTG0_SSTXP
EDP_TX_D0N
EDP_TX_D0P
EDP_TX_D1N
EDP_TX_D1P
EDP_TX_AUXN
EDP_TX_AUXP
EDP_TX_D2N
EDP_TX_D2P
EDP_TX_D3N
EDP_TX_D3P
SPKP_OUT
SPKN_OUT
HPL_OUT
HPR_OUT
MIC1_INN
MIC1_INP
HP_SNS
USB3_HOST1_SSRXN
USB3_HOST1_SSRXP
USB3_HOST1_SSTXN
USB3_HOST1_SSTXP
USB3_HOST1_DM
USB3_HOST1_DP
PCIE30_TX0P
PCIE30_TX0N
PCIE30_TX1P
PCIE30_TX1N
PCIE30_RX0P
PCIE30_RX0N
PCIE30_RX1P
PCIE30_RX1N
PCIE20_REFCLKP
PCIE20_REFCLKN
PCIE30_REFCLKP_IN
PCIE30_REFCLKN_IN
UPDATE
RESETn
PWRON_KEY
EXT_EN
VCC3V3_SD
VCCIO_SD
VCC3V3_SYS
VCC_3V3
VCC_1V8
VCC5V0_SYS
UART2_RX GPIO0_D0 TP1
UART2_TX GPIO0_D1 TP2
VCC3V3_SYS TP3
VCC5V0_SYS TP4
GND TP5
Title: ATK-CLRK3568B V1.0.PrjPcb
Author: ALIENTEK
Size: A3
Date: 2024/8/7
File: ATK_Pinout.SchDoc
Revision: V1.3
Version:
正点原子

VDD_CPU

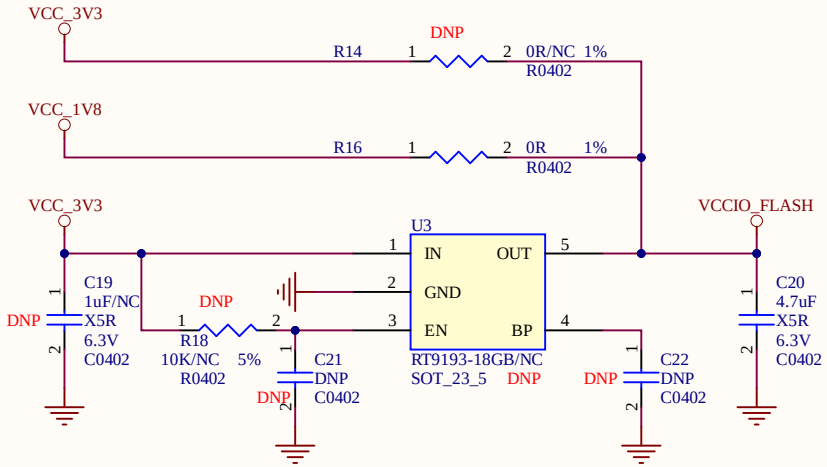


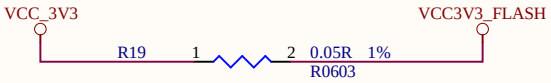
Title: ATK-CLRK3568B V1.0.PrjPcb	
Author: ALIENTEK	Size: A4
Date: 2024/8/7	File: ATK_Power_other.SchDoc
Revision: V1.3	Version:

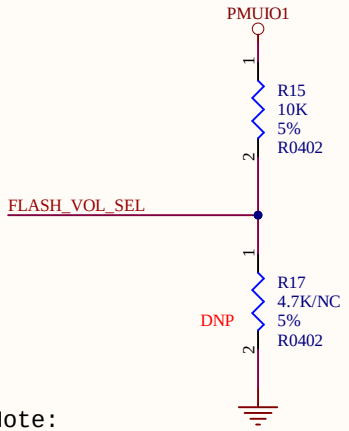
正点原子

Flash Power Manage

	VCCIO2 domain voltage: Recommend voltage value (VCCIO_FLASH)	FLASH_VOL_SEL state decided to VCCIO2 domain IO driven by default
eMMC	1.8V	FLASH_VOL_SEL --> Logic=H
Nand flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)
SPI flash	Default 3.3V, Adjust according to demand 1.8V	FLASH_VOL_SEL --> Logic=L(Default)







Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven

Title: ATK-CLRK3568B V1.0.PrjPcb	
Author: ALIENTEK	Size: A4
Date: 2024/8/7	File: ATK_Powr_Flash Power Manage.SchDoc
Revision: V1.3	Version:

正点原子

RK3568_H(VCCIO1 Domain)

U5H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0	/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/	GPIO1_A0_u
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0	/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/	GPIO1_A1_u
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERSTn_M2		/	GPIO1_A2_d
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2	/ ACODEC_DAC_CLK	/	GPIO1_A3_d
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0	/ SPDIF_TX_M0		/	GPIO1_A4_d
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2	/ ACODEC_DAC_SYNC	/	GPIO1_A5_d
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0	/ AUDIOPWM_ROUT_P		/	GPIO1_A6_d
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET	/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/	GPIO1_A7_d
I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2	/ ACODEC_DAC_DATAR	/	GPIO1_B0_d
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2	/ ACODEC_ADC_SYNC	/	GPIO1_B1_d
I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2		/	GPIO1_B2_d
	I2S1_SDI0_M0	/ PDM_SDI0_M0			/	GPIO1_B3_d

VCCIO1

RK3568-Socket

D18	GPIO1_A0	I2C3_SDA_M0
E18	GPIO1_A1	I2C3_SCL_M0
A19	GPIO1_A2	I2S1_MCLK_M0_RK809
B19	GPIO1_A3	I2S1_SCLK_TX_M0_RK809
F18	GPIO1_A4	HP_DET_L
A20	GPIO1_A5	I2S1_LRCK_TX_M0_RK809
C20	GPIO1_A6	PDM_CLK0_M0_RK809
B20	GPIO1_A7	I2S1_SDO0_M0_RK809
D20	GPIO1_B0	GSENSOR_INT
E20	GPIO1_B1	5G_RESET
A21	GPIO1_B2	LCD0_RST_L
B21	GPIO1_B3	I2S1_SDI0_M0/PDM_SDI0_M0_RK809

R3722R 5% R0402

R3822R 5% R0402

R3922R 5% R0402

R4022R 5% R0402

R4122R 5% R0402

R4222R 5% R0402

VCCIO1

H17

C72 100nF X5R 10V C0201

R43 0R 1% R0402

VCCIO_ACODEC

Note:

Caps of between dashed green lines and U5 should be placed under the U5 package

Title: ATK-CLRK3568B V1.0.PrjPcb	
Author: ALIENTEK	Size: A4
Date: 2024/8/7	File: ATK_RK3568_Audio Interface.SchDoc
Revision: V1.3	Version:

正点原子

RK3568_F (DDR PHY)

U5F

DDR4	LPDDR4	DDR3	LPDDR3		DDR4	LPDDR4	DDR3	LPDDR3	
LPDDR4_DQ0_A F2	DDR_DQ0_A	DDR4_DQL0_A	LPDDR4_DQ0_A	DDR3_DQ0	LPDDR3_DQ15	DDR4_A0	**LPDDR4_CLKP_B**	DDR3_A9	--- AC0	B6 LPDDR4_CLKP_B
LPDDR4_DQ1_A E1	DDR_DQ1_A	DDR4_DQL2_A	LPDDR4_DQ1_A	DDR3_DQ1	LPDDR3_DQ14	DDR4_A1	---	DDR3_A2	--- AC1	F5
LPDDR4_DQ2_A E2	DDR_DQ2_A	DDR4_DQL4_A	LPDDR4_DQ2_A	DDR3_DQ2	LPDDR3_DQ10	DDR4_A2	LPDDR4_A1_A	DDR3_A4	LPDDR3_A6 AC2	B1 LPDDR4_A1_A
LPDDR4_DQ3_A D1	DDR_DQ3_A	DDR4_DQL6_A	LPDDR4_DQ3_A	DDR3_DQ3	LPDDR3_DQ9	DDR4_A3	LPDDR4_CKE1_A	DDR3_A3	--- AC3	F4 LPDDR4_CKE1_A
LPDDR4_DQ4_A J1	DDR_DQ4_A	DDR4_DQL7_A	LPDDR4_DQ4_A	DDR3_DQ4	LPDDR3_DQ13					
LPDDR4_DQ5_A J2	DDR_DQ5_A	DDR4_DQL5_A	LPDDR4_DQ5_A	DDR3_DQ5	LPDDR3_DQ12	DDR4_A4	LPDDR4_A3_B	DDR3_BA1	LPDDR3_A3 AC4	D9 LPDDR4_A3_B
LPDDR4_DQ6_A H1	DDR_DQ6_A	DDR4_DQL3_A	LPDDR4_DQ6_A	DDR3_DQ6	LPDDR3_DQ8	DDR4_A5	LPDDR4_A5_B	DDR3_A11	LPDDR3_A2 AC5	B7 LPDDR4_A5_B
LPDDR4_DQ7_A H4	DDR_DQ7_A	DDR4_DQL1_A	LPDDR4_DQ7_A	DDR3_DQ7	LPDDR3_DQ11	DDR4_A6	LPDDR4_A1_B	DDR3_A13	LPDDR3_A1 AC6	A7 LPDDR4_A1_B
						DDR4_A7	LPDDR4_ODT0_CA_B	DDR3_A8	--- AC7	A8 LPDDR4_ODT0_CA_B
LPDDR4_DM0_A H5	DDR_DM0_A	DDR4_DML_A	LPDDR4_DM0_A	DDR3_DM0	LPDDR3_DM1					
						DDR4_A8	LPDDR4_ODT0_CA_A	DDR3_A6	LPDDR3_A9 AC8	C1 LPDDR4_ODT0_CA_A
LPDDR4_DQS0P_A G1	DDR_DQS0P_A	DDR4_DQSL_P_A	LPDDR4_DQS0P_A	DDR3_DQS0P	LPDDR3_DQS1P	DDR4_A9	**LPDDR4_CLKN_B**	DDR3_A5	--- AC9	A5 LPDDR4_CLKN_B
LPDDR4_DQS0N_A G2	DDR_DQS0N_A	DDR4_DQSL_N_A	LPDDR4_DQS0N_A	DDR3_DQS0N	LPDDR3_DQS1N	DDR4_A10	LPDDR4_CKE0_B	DDR3_A10	--- AC10	D6 LPDDR4_CKE0_B
						DDR4_A11	LPDDR4_A0_A	DDR3_A7	LPDDR3_A8 AC11	C2 LPDDR4_A0_A
LPDDR4_DQ8_A M1	DDR_DQ8_A	DDR4_DQU3_A	LPDDR4_DQ8_A	DDR3_DQ8	LPDDR3_DQ25	DDR4_A12	LPDDR4_A3_A	DDR3_BA2	--- AC12	C4 LPDDR4_A3_A
LPDDR4_DQ9_A N2	DDR_DQ9_A	DDR4_DQU1_A	LPDDR4_DQ9_A	DDR3_DQ9	LPDDR3_DQ24	DDR4_A13	LPDDR4_A0_B	DDR3_A14	LPDDR3_A0 AC13	B8 LPDDR4_A0_B
LPDDR4_DQ10_A L7	DDR_DQ10_A	DDR4_DQU7_A	LPDDR4_DQ10_A	DDR3_DQ10	LPDDR3_DQ26	DDR4_A14_WEn	LPDDR4_A4_A	DDR3_A15	LPDDR3_A5 AC14	C5 LPDDR4_A4_A
LPDDR4_DQ11_A L6	DDR_DQ11_A	DDR4_DQU5_A	LPDDR4_DQ11_A	DDR3_DQ11	LPDDR3_DQ29	DDR4_A15_CASn	LPDDR4_A2_A	DDR3_A0	--- AC15	E4 LPDDR4_A2_A
LPDDR4_DQ12_A K2	DDR_DQ12_A	DDR4_DQU2_A	LPDDR4_DQ12_A	DDR3_DQ12	LPDDR3_DQ26					
LPDDR4_DQ13_A J6	DDR_DQ13_A	DDR4_DQU4_A	LPDDR4_DQ13_A	DDR3_DQ13	LPDDR3_DQ31	DDR4_A16_RASn	LPDDR4_A5_A	DDR3_RASn	LPDDR3_A7 AC16	D5 LPDDR4_A5_A
LPDDR4_DQ14_A J7	DDR_DQ14_A	DDR4_DQU6_A	LPDDR4_DQ14_A	DDR3_DQ14	LPDDR3_DQ30	DDR4_ACTn	LPDDR4_CKE1_B	DDR3_CASn	--- AC17	E6 LPDDR4_CKE1_B
LPDDR4_DQ15_A L4	DDR_DQ15_A	DDR4_DQU0_A	LPDDR4_DQ15_A	DDR3_DQ15	LPDDR3_DQ27	DDR4_BA0	LPDDR4_A2_B	DDR3_A1	--- AC18	E11 LPDDR4_A2_B
						DDR4_BA1	LPDDR4_A4_B	DDR3_A12	LPDDR3_A4 AC19	E9 LPDDR4_A4_B
LPDDR4_DM1_A J4	DDR_DM1_A	DDR4_DMU_A	LPDDR4_DM1_A	DDR3_DM1	LPDDR3_DM3					F8
						DDR4_BG0	LPDDR4_ODT1_CA_B	DDR3_WEn	--- AC20	F7
LPDDR4_DQS1P_A L2	DDR_DQS1P_A	DDR4_DQSU_P_A	LPDDR4_DQS1P_A	DDR3_DQS1P	LPDDR3_DQS3P	DDR4_BG1	LPDDR4_ODT1_CA_A	DDR3_BA0	--- AC21	B3 LPDDR4_CKE0_A
LPDDR4_DQS1N_A L1	DDR_DQS1N_A	DDR4_DQSU_N_A	LPDDR4_DQS1N_A	DDR3_DQS1N	LPDDR3_DQS3N	DDR4_CKE	LPDDR4_CKE0_A	DDR3_CKE	LPDDR3_CKE AC22	
						DDR4_CLKP	**LPDDR4_CLKP_A**	**DDR3_CLKP**	**LPDDR3_CLKP** AC23	B4 LPDDR4_CLKP_A
LPDDR4_DQ0_B B10	DDR_DQ0_B	DDR4_DQU7_B	LPDDR4_DQ0_B	DDR3_DQ16	LPDDR3_DQ1	**DDR4_CLKN**	**LPDDR4_CLKN_A**	**DDR3_CLKN**	**LPDDR3_CLKN** AC24	A4 LPDDR4_CLKN_A
LPDDR4_DQ1_B A9	DDR_DQ1_B	DDR4_DQU5_B	LPDDR4_DQ1_B	DDR3_DQ17	LPDDR3_DQ5					
LPDDR4_DQ2_B D12	DDR_DQ2_B	DDR4_DQU3_B	LPDDR4_DQ2_B	DDR3_DQ18	LPDDR3_DQ6	DDR4_CS0n	LPDDR4_CS0n_A	DDR3_ODT1	LPDDR3_ODT0 AC25	A2 LPDDR4_CS0n_A
LPDDR4_DQ3_B E12	DDR_DQ3_B	DDR4_DQU1_B	LPDDR4_DQ3_B	DDR3_DQ19	LPDDR3_DQ4	DDR4_CS1n	LPDDR4_CS1n_A	DDR3_CS1n	LPDDR3_ODT1 AC26	B2 LPDDR4_CS1n_A
LPDDR4_DQ4_B A12	DDR_DQ4_B	DDR4_DQU0_B	LPDDR4_DQ4_B	DDR3_DQ20	LPDDR3_DQ2	DDR4_ODT0	LPDDR4_CS1n_B	DDR3_ODT0	LPDDR3_CS1n AC27	E8 LPDDR4_CS1n_B
LPDDR4_DQ5_B D15	DDR_DQ5_B	DDR4_DQU6_B	LPDDR4_DQ5_B	DDR3_DQ21	LPDDR3_DQ3	DDR4_ODT1	LPDDR4_CS0n_B	DDR3_CS0n	LPDDR3_CS0n AC28	D8 LPDDR4_CS0n_B
LPDDR4_DQ6_B E15	DDR_DQ6_B	DDR4_DQU4_B	LPDDR4_DQ6_B	DDR3_DQ22	LPDDR3_DQ7					
LPDDR4_DQ7_B E14	DDR_DQ7_B	DDR4_DQU2_B	LPDDR4_DQ7_B	DDR3_DQ23	LPDDR3_DQ0	DDR4_RESETn	LPDDR4_RESETn	DDR3_RESETn	--- AC29	F11 LPDDR4_RESETn
LPDDR4_DM0_B D14	DDR_DM0_B	DDR4_DMU_B	LPDDR4_DM0_B	DDR3_DM2	LPDDR3_DM0					
LPDDR4_DQS0P_B A11	DDR_DQS0P_B	DDR4_DQSU_P_B	LPDDR4_DQS0P_B	DDR3_DQS2P	LPDDR3_DQS0P					
LPDDR4_DQS0N_B B11	DDR_DQS0N_B	DDR4_DQSU_N_B	LPDDR4_DQS0N_B	DDR3_DQS2N	LPDDR3_DQS0N					
LPDDR4_DQ8_B A16	DDR_DQ8_B	DDR4_DQL0_B	LPDDR4_DQ8_B	DDR3_DQ24	LPDDR3_DQ18					
LPDDR4_DQ9_B B17	DDR_DQ9_B	DDR4_DQL2_B	LPDDR4_DQ9_B	DDR3_DQ25	LPDDR3_DQ19					
LPDDR4_DQ10_B A17	DDR_DQ10_B	DDR4_DQL4_B	LPDDR4_DQ10_B	DDR3_DQ26	LPDDR3_DQ22					
LPDDR4_DQ11_B B18	DDR_DQ11_B	DDR4_DQL6_B	LPDDR4_DQ11_B	DDR3_DQ27	LPDDR3_DQ23					
LPDDR4_DQ12_B B13	DDR_DQ12_B	DDR4_DQL7_B	LPDDR4_DQ12_B	DDR3_DQ28	LPDDR3_DQ16					
LPDDR4_DQ13_B A13	DDR_DQ13_B	DDR4_DQL5_B	LPDDR4_DQ13_B	DDR3_DQ29	LPDDR3_DQ17					
LPDDR4_DQ14_B D17	DDR_DQ14_B	DDR4_DQL1_B	LPDDR4_DQ14_B	DDR3_DQ30	LPDDR3_DQ20					
LPDDR4_DQ15_B B14	DDR_DQ15_B	DDR4_DQL3_B	LPDDR4_DQ15_B	DDR3_DQ31	LPDDR3_DQ21					
LPDDR4_DM1_B E17	DDR_DM1_B	DDR4_DML_B	LPDDR4_DM1_B	DDR3_DM3	LPDDR3_DM2					
LPDDR4_DQS1P_B B15	DDR_DQS1P_B	DDR4_DQSL_P_B	LPDDR4_DQS1P_B	DDR3_DQS3P	LPDDR3_DQS2P					
LPDDR4_DQS1N_B A15	DDR_DQS1N_B	DDR4_DQSL_N_B	LPDDR4_DQS1N_B	DDR3_DQS3N	LPDDR3_DQS2N					
P5	DDR_ECC_DQ0	DDR4_ECC_DQ7	--	DDR3_ECC_DQ0						
M4	DDR_ECC_DQ1	DDR4_ECC_DQ6	--	DDR3_ECC_DQ1						
M5	DDR_ECC_DQ2	DDR4_ECC_DQ2	--	DDR3_ECC_DQ2						
R5	DDR_ECC_DQ3	DDR4_ECC_DQ1	--	DDR3_ECC_DQ3						
M7	DDR_ECC_DQ4	DDR4_ECC_DQ6	--	DDR3_ECC_DQ4						
R7	DDR_ECC_DQ5	DDR4_ECC_DQ4	--	DDR3_ECC_DQ5						
P4	DDR_ECC_DQ6	DDR4_ECC_DQ3	--	DDR3_ECC_DQ6						
R4	DDR_ECC_DQ7	DDR4_ECC_DQ5	--	DDR3_ECC_DQ7						
P7	DDR_ECC_DM	DDR4_ECC_DM	--	DDR3_ECC_DM						
P2	DDR_ECC_DQS/P	DDR4_ECC_DQS_P	--	DDR3_ECC_DQS_P						
P1	DDR_ECC_DQS/N	DDR4_ECC_DQS_N	--	DDR3_ECC_DQS_N						

RK3568-Socket

Note: Sequences can not be swap

Note:
Except DDR3, other DQ sequences
can not be swap

DDR_RZQ

DDR_VREFOUT

DDR3L	=1.35V
DDR3	=1.5V
DDR4	=1.2V
LPDDR3	=1.2V
LPDDR4	=1.1V
LPDDR4x	=1.1V

DDRPHY_VDDQ_1
DDRPHY_VDDQ_2
DDRPHY_VDDQ_3
DDRPHY_VDDQ_4
DDRPHY_VDDQ_5
DDRPHY_VDDQ_6
DDRPHY_VDDQ_7
DDRPHY_VDDQ_8

DDR3L	=1.35V
DDR3	=1.5V
DDR4	=1.2V
LPDDR3	=1.2V
LPDDR4	=1.1V
LPDDR4x	**#NAME?**

DDRPHY_VDDQL_1
DDRPHY_VDDQL_2
DDRPHY_VDDQL_3
DDRPHY_VDDQL_4
DDRPHY_VDDQL_5
DDRPHY_VDDQL_6

DDR_AVSS

For DDR4/DDR3/LPDDR3 mode,
a 120 ohm +/-1% tolerance external
resistor must be connected between
the DDR_RZQ pin and VSS pin

H7 DDR_RZQ R44 1 2 120R 1% VCC_DDR

For LPDDR4/LPDDR4x mode,
a 120 ohm +/-1% tolerance external
resistor must be connected between
the DDR_RZQ pin and DDRPHY_VDDQ pin

P8

LPDDR4/LPDDR4x

H9 H11 H12 H14 H15 J9 L9 M9

VCC_DDR

C73 100nF X5R 10V
C74 100nF X5R 10V
C75 4.7uF X5R 6.3V
C76 4.7uF X5R 6.3V
C77 10uF X5R 6.3V

J11 J12 J14 K10 L10 M10

VCC0V6_DDR

C78 100nF X5R 10V
C79 100nF X5R 10V
C80 4.7uF X5R 6.3V
C81 4.7uF X5R 6.3V
C82 4.7uF X5R 6.3V

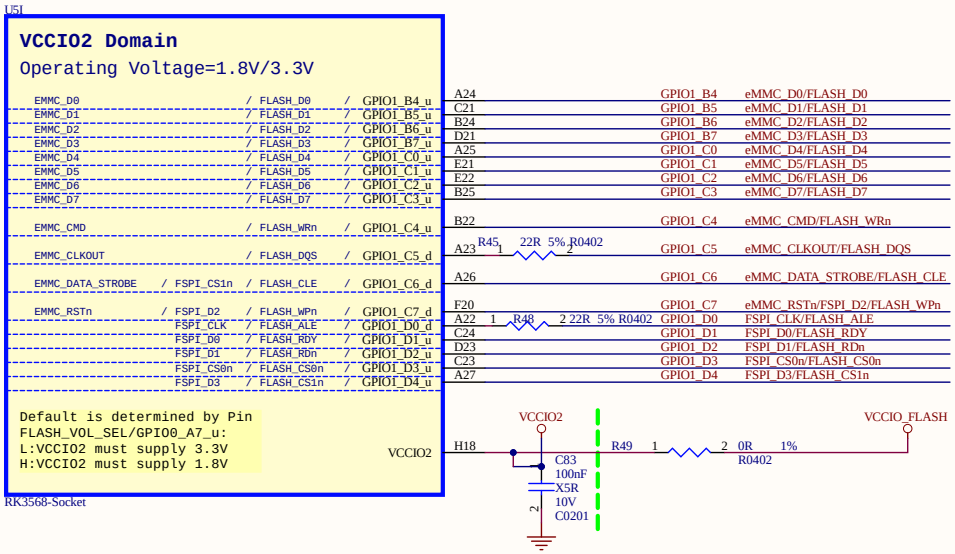
J8

Caps should be placed under
the U5 package

Title: ATK-CLRK3568B V1.0.PrjPcb	
Author: ALIENTEK	Size: A3
Date: 2024/8/7	File: ATK_RK3568_DDRPHY.SchDoc
Revision: V1.3	Version:

正点原子

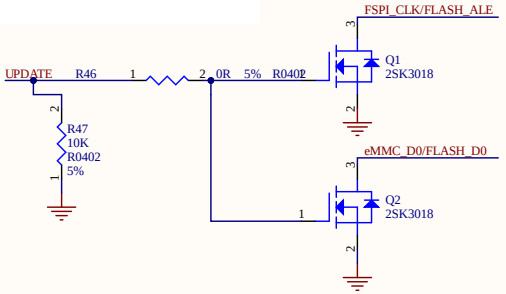
RK3568_I(VCCIO2 Domain)



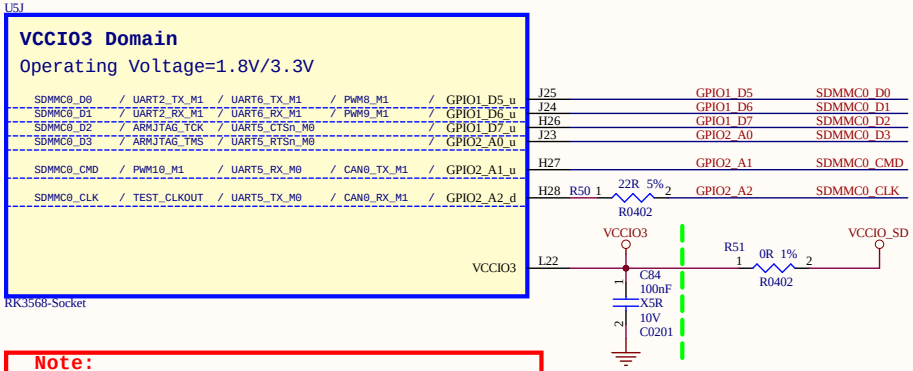
注意，上电和复位的时候：

如果UPDATE为低，因此2SK3018不导通。eMMC_D0/FLASH_D0保持默认电平(高)。

如果UPDATE为高电平，2SK3018导通，eMMC_D0/FLASH_D0此时就会接地，为低电平，工作在MASKROM模式，可以烧写系统



RK3568_J(VCCIO3 Domain)



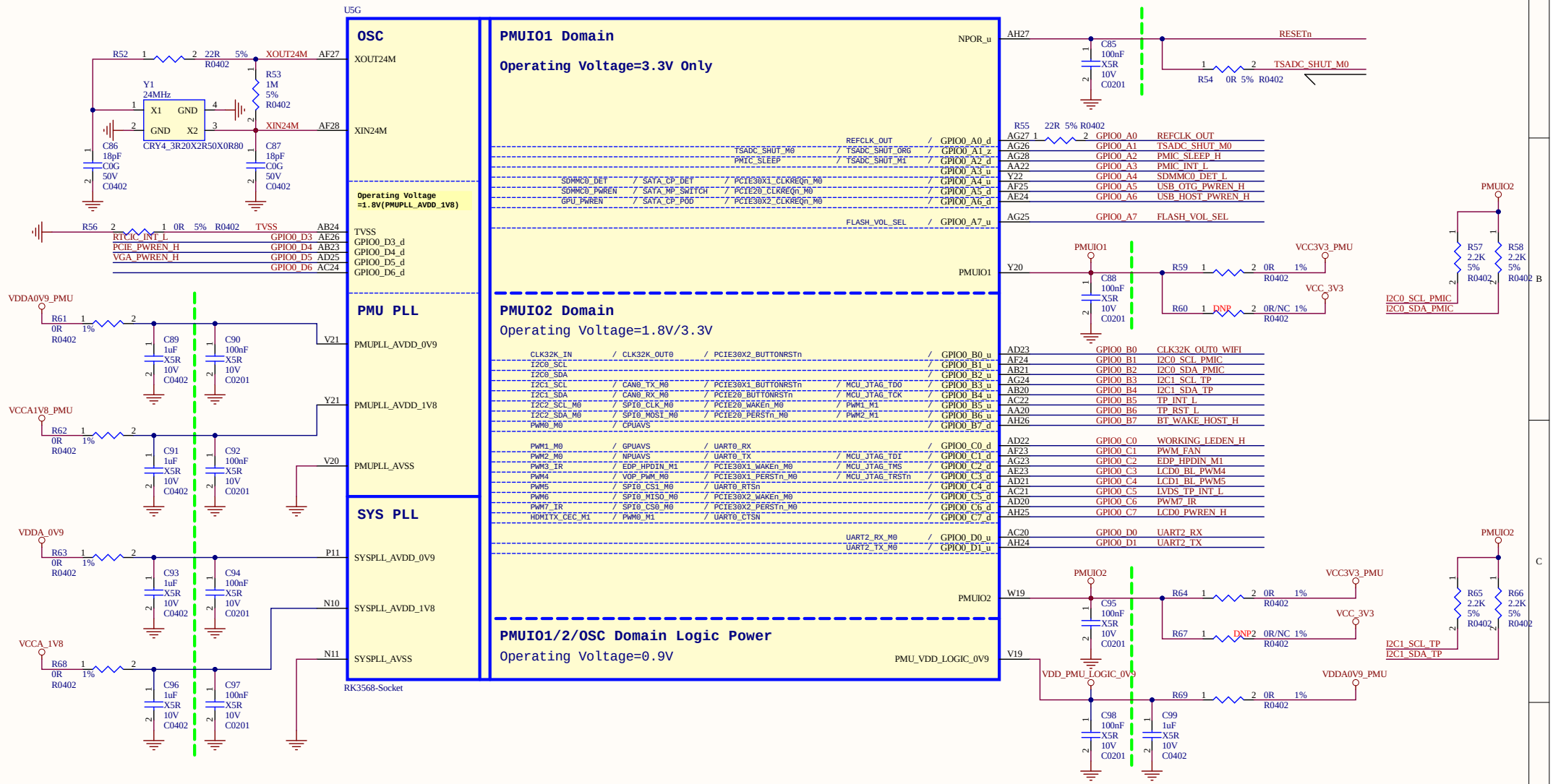
Note:

Caps of between dashed green lines and U5 should be placed under the U5 package

Title: ATK-CLRK3568B V1.0.PrjPcb	
Author: ALIENTEK	Size: A3
Date: 2024/8/7	File: ATK_RK3568_Flash_SD.SchDoc
Revision: V1.3	Version:

正点原子

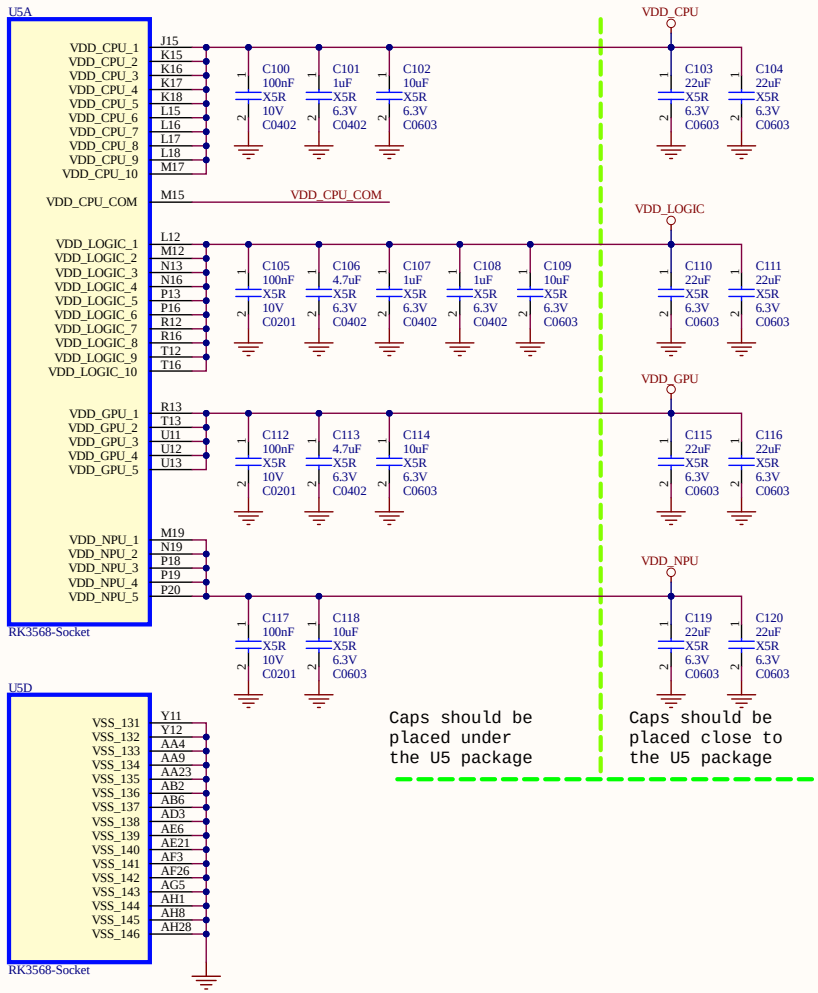
RK3568_G(OSC/PLL/PMUIO1/2)

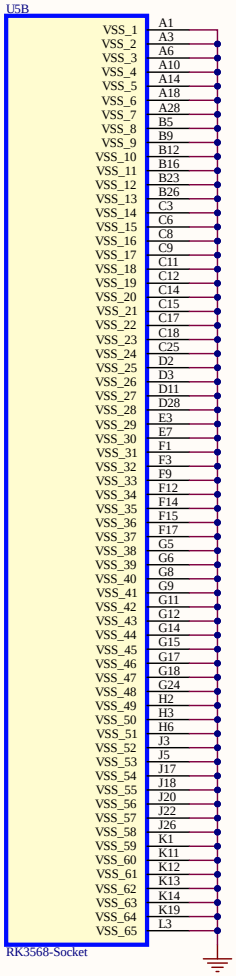


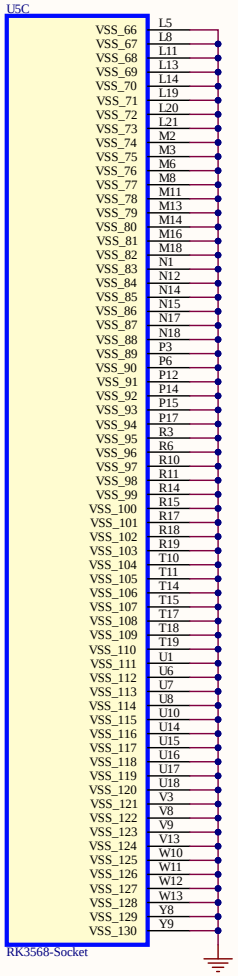
Note:
Caps of between dashed green lines and U5
should be placed under the U5 package.
Other caps should be placed close to the U5 package

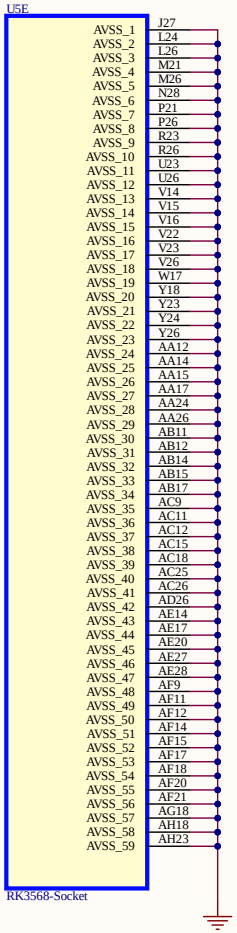
Title: ATK-CLRK3568B V1.0.PrjPcb	
Author: ALIENTEK	Size: A3
Date: 2024/8/7	File: ATK_RK3568_OSC_PLL_PMUIO.SchDoc
Revision: V1.3	Version:

RK3568_ABCDE (Power&Gnd)









Title: ATK-CLRK3568B V1.0.PrjPcb	
Author: ALIENTEK	Size: A3
Date: 2024/8/7	File: ATK_RK3568_Power_GND.SchDoc
Revision: V1.3	Version:

RK3568_K(VCCIO4 Domain)

U5K

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

SDMMC1_D0	/ GMAC0_RXD2	/ UART6_RX_M0		/ GPIO2_A3_u	E27	GPIO2_A3 GMAC0_RXD2
SDMMC1_D1	/ GMAC0_RXD3	/ UART6_TX_M0		/ GPIO2_A4_u	E28	GPIO2_A4 GMAC0_RXD3
SDMMC1_D2	/ GMAC0_RXCLK	/ UART7_RX_M0		/ GPIO2_A5_u	B28	GPIO2_A5 GMAC0_RXCLK
SDMMC1_D3	/ GMAC0_TXD2	/ UART7_TX_M0		/ GPIO2_A6_u	C27	R70 1 22R 5% 2 R0402 GPIO2_A6 GMAC0_TXD2
SDMMC1_CMD	/ GMAC0_TXD3	/ UART9_RX_M0		/ GPIO2_A7_u	C28	R71 1 22R 5% 2 R0402 GPIO2_A7 GMAC0_TXD3
SDMMC1_CLK	/ GMAC0_TXCLK	/ UART9_TX_M0		/ GPIO2_B0_d	D27	R72 1 22R 5% 2 R0402 GPIO2_B0 GMAC0_TXCLK
SDMMC1_PWREN	/ I2C4_SDA_M1	/ UART8_RTSn_M0	/ CAN2_RX_M1	/ GPIO2_B1_d	D26	GPIO2_B1 UART8_RTSn_M0
SDMMC1_DET	/ I2C4_SCL_M1	/ UART8_CTSn_M0	/ CAN2_TX_M1	/ GPIO2_B2_u	E25	GPIO2_B2 UART8_CTSn_M0
	GMAC0_TXD0	/ UART1_RX_M0		/ GPIO2_B3_u	F28	R73 1 22R 5% 2 R0402 GPIO2_B3 GMAC0_TXD0
	GMAC0_TXD1	/ UART1_TX_M0		/ GPIO2_B4_u	G27	R74 1 22R 5% 2 R0402 GPIO2_B4 GMAC0_TXD1
	GMAC0_TXEN	/ UART1_RTSn_M0	/ SPI1_CLK_M0	/ GPIO2_B5_u	G28	R75 1 22R 5% 2 R0402 GPIO2_B5 GMAC0_TXEN
	GMAC0_RXD0	/ UART1_CTSn_M0	/ SPI1_MISO_M0	/ GPIO2_B6_u	F27	GPIO2_B6 GMAC0_RXD0
I2S2_SCLK_RX_M0	/ GMAC0_RXD1	/ UART6_RTSn_M0	/ SPI1_MOSI_M0	/ GPIO2_B7_d	H25	GPIO2_B7 GMAC0_RXD1
I2S2_LRCK_RX_M0	/ GMAC0_RXDV_CRS	/ UART6_CTSn_M0	/ SPI1_CS0_M0	/ GPIO2_C0_d	F24	GPIO2_C0 GMAC0_RXDV_CRS
I2S2_MCLK_M0	/ ETH0_REFCLKO_25M	/ UART7_RTSn_M0	/ SPI2_CLK_M0	/ GPIO2_C1_d	G23	R77 1 22R 5% 2 R0402 GPIO2_C1 ETH0_REFCLKO_25M
I2S2_SCLK_TX_M0	/ GMAC0_MCLKINOUT	/ UART7_CTSn_M0	/ SPI2_MISO_M0	/ GPIO2_C2_d	F25	GPIO2_C2 GMAC0_MCLKINOUT
I2S2_LRCK_TX_M0	/ GMAC0_MDC	/ UART9_RTSn_M0	/ SPI2_MOSI_M0	/ GPIO2_C3_d	H24	GPIO2_C3 GMAC0_MDC
I2S2_SDO_M0	/ GMAC0_MDIO	/ UART9_CTSn_M0	/ SPI2_CS0_M0	/ GPIO2_C4_d	H23	GPIO2_C4 GMAC0_MDIO
I2S2_SDI_M0	/ GMAC0_RXER	/ UART8_TX_M0	/ SPI2_CS1_M0	/ GPIO2_C5_d	F26	GPIO2_C5 UART8_TX_M0
CLK32K_OUT1		/ UART8_RX_M0	/ SPI1_CS1_M0	/ GPIO2_C6_d	E26	GPIO2_C6 UART8_RX_M0
				VCCIO4	J21	

For BT

For BT

VCCIO4 C131 100nF X5R 10V C0201

R79 1 2 0.1R 1% R0402 VCC_1V8

R80 1 DNP 2 0.1R/NC 1% R0402 VCC_3V3

RK3568-Socket

RK3568_N(VCCIO7 Domain)

U5N

VCCIO7 Domain

Operating Voltage=1.8V/3.3V

PWM14_M1	/ SPI3_CLK_M1	/ CAN1_RX_M1	/ PCIE30X2_CLKREQn_M2	/ I2S3_MCLK_M1	/ GPIO4_C2_d	AF8 GPIO4_C2 CAN1_RX_M1
PWM15_IR_M1	/ SPI3_MOSI_M1	/ CAN1_TX_M1	/ PCIE30X2_WAKEn_M2	/ I2S3_SCLK_M1	/ GPIO4_C3_d	AA11 GPIO4_C3 CAN1_TX_M1
EDP_HPDIN_M0	/ SPDIF_TX_M2	/ SATA2_ACT_LED	/ PCIE30X2_PERSTn_M2	/ I2S3_LRCK_M1	/ GPIO4_C4_d	AH7 GPIO4_C4 SATA2_ACT_LED
PWM12_M1	/ SPI3_MISO_M1	/ SATA1_ACT_LED	/ UART9_TX_M1	/ I2S3_SDO_M1	/ GPIO4_C5_d	AD8 GPIO4_C5 UART9_TX_M1
PWM13_M1	/ SPI3_CS0_M1	/ SATA0_ACT_LED	/ UART9_RX_M1	/ I2S3_SDI_M1	/ GPIO4_C6_d	AE8 GPIO4_C6 UART9_RX_M1
HDMITX_SCL	/ I2C5_SCL_M1			/ GPIO4_C7_u	AG8	GPIO4_C7 HDMITX_SCL
HDMITX_SDA	/ I2C5_SDA_M1			/ GPIO4_D0_u	AG7	GPIO4_D0 HDMITX_SDA
HDMITX_CEC_M0	/ SPI3_CS1_M1			/ GPIO4_D1_u	AH6	GPIO4_D1 HDMITX_CEC_M0
				GPIO4_D2_d	AB9	GPIO4_D2 AP_INT
				VCCIO7	V12	

如果要使用HDMI，那么HDMITX_SCL和HDMITX_SDA这两个IIC引脚不能与其他

VCCIO7 C132 100nF X5R 10V C0201

R82 1 2 0.1R 1% R0402 VCC_3V3

RK3568-Socket

RK3568_O(SARADC/OTP)

U5O

SARADC

Recovery

SARADC_VIN0	B27	SARADC_VIN0_KEY/RECOVERY	C121 1 2 1nF X5R 50V C0402	
SARADC_VIN1	C26	SARADC_VIN1_HW_ID	C122 1 2 1nF X5R 50V C0402	
SARADC_VIN2	D24	SARADC_VIN2_LCD_ID	C123 1 2 1nF X5R 50V C0402	
SARADC_VIN3	E23	SARADC_VIN3	C124 1 2 1nF X5R 50V C0402	
SARADC_VIN4	G21	SARADC_VIN4	C125 1 2 1nF X5R 50V C0402	
SARADC_VIN5	F22	SARADC_VIN5	C126 1 2 1nF X5R 50V C0402	
SARADC_VIN6	G20	SARADC_VIN6	C127 1 2 1nF X5R 50V C0402	
SARADC_VIN7	F21	SARADC_VIN7	C128 1 2 1nF X5R 50V C0402	
SARADC_AVDD_1V8	H22			

SARADC_AVDD_1V8 C129 100nF X5R 10V C0201

R76 1 2 0R 1% R0402 VCCA_1V8

OTP

OTP_VCC18 H20

OTP_VCC18 C130 100nF X5R 10V C0201

R78 1 2 0R 1% R0402 VCC_1V8

RK3568-Socket

SARADC_AVDD_1V8

Note:

Must be mounted

R81 10K 1% R0402

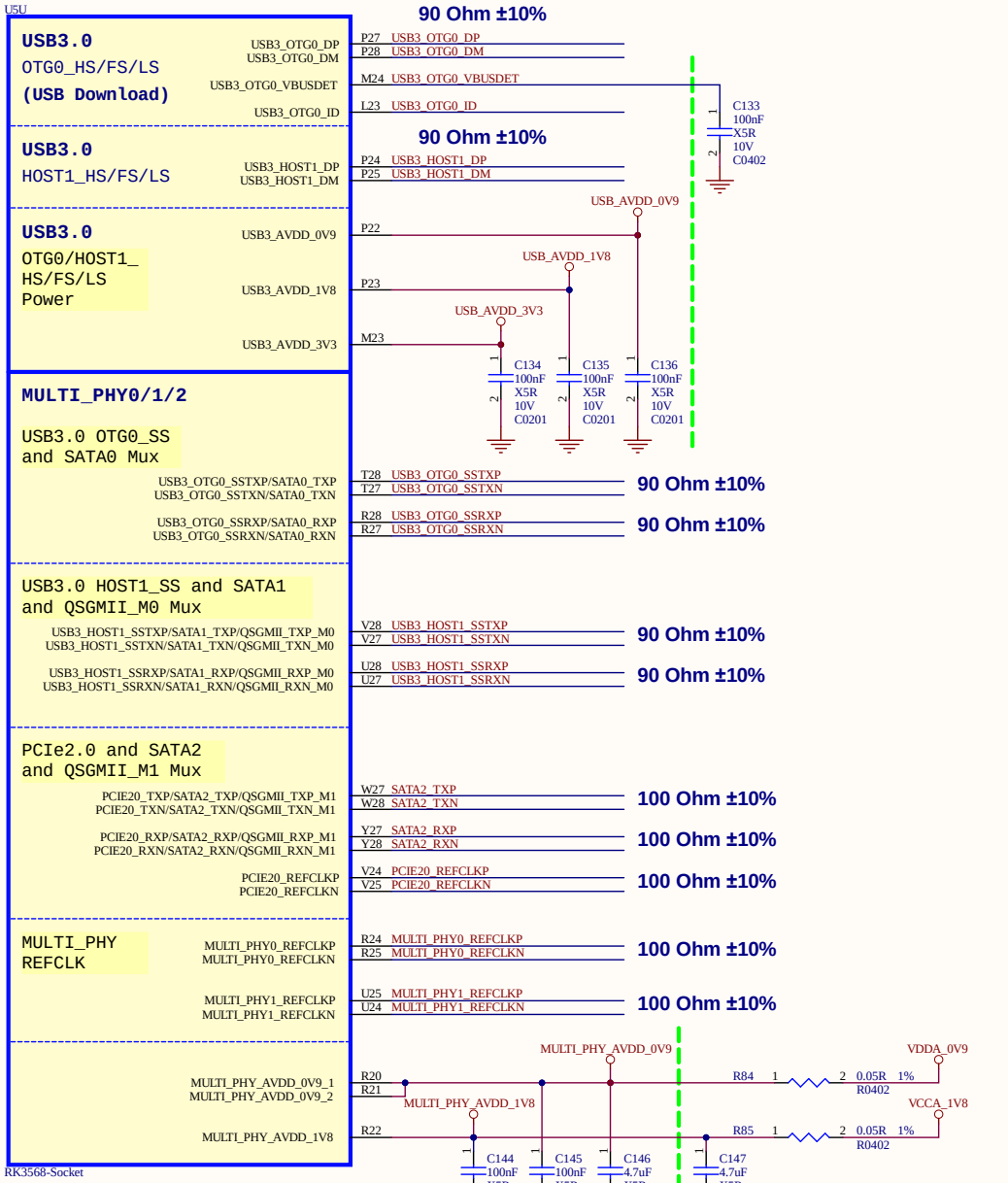
SARADC_VIN0_KEY/RECOVERY

Caps of between dashed green lines and U5 should be placed under the U5 package

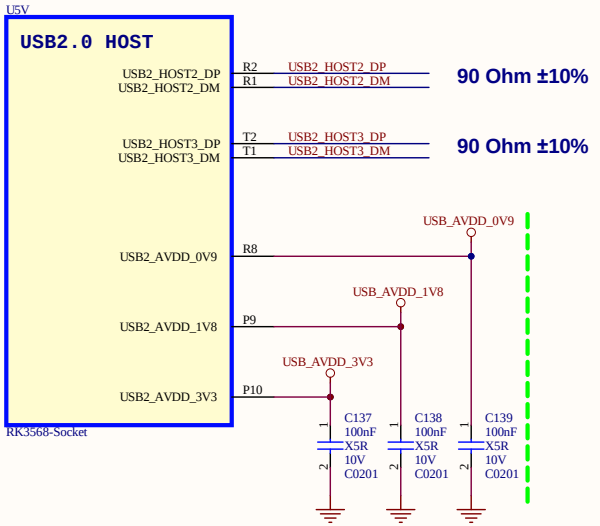
Title: ATK-CLRK3568B V1.0.PrjPcb	
Author: ALIENTEK	Size: A3
Date: 2024/8/7	File: ATK_RK3568_SARADC_GPIO.SchDoc
Revision: V1.3	Version:

正点原子

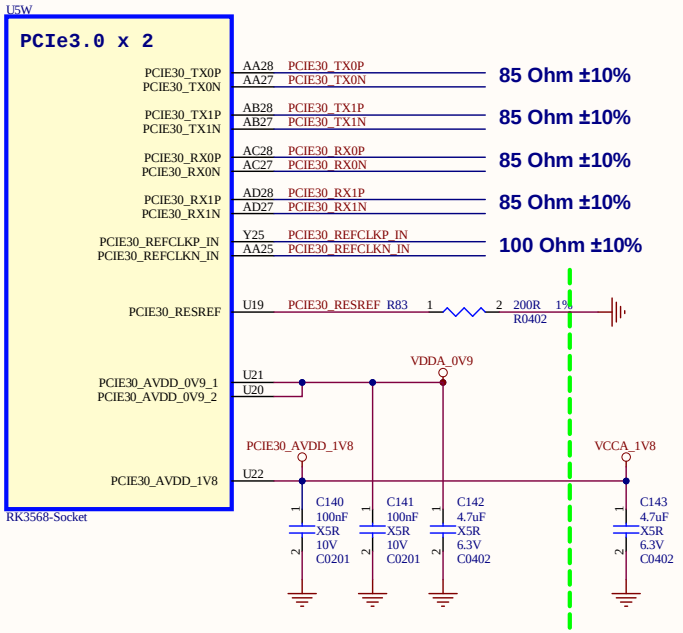
RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)



RK3568_V(USB2.0 HOST)



RK3568_W(PCIe3.0 x2)

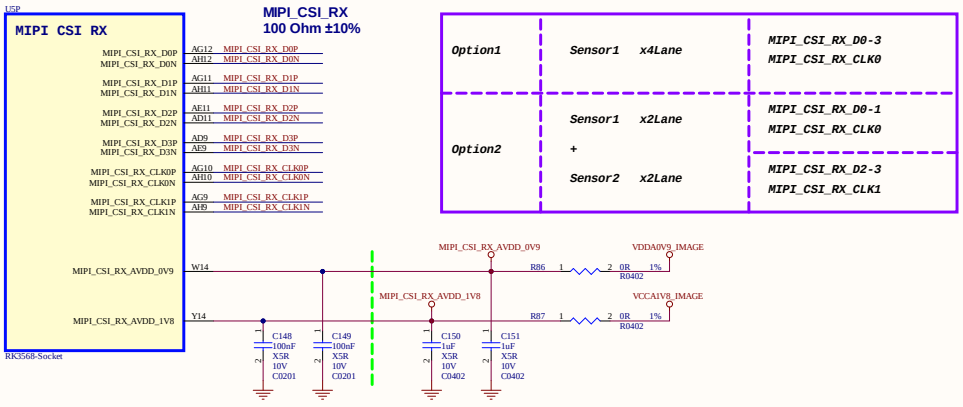


Rockchip Confidential

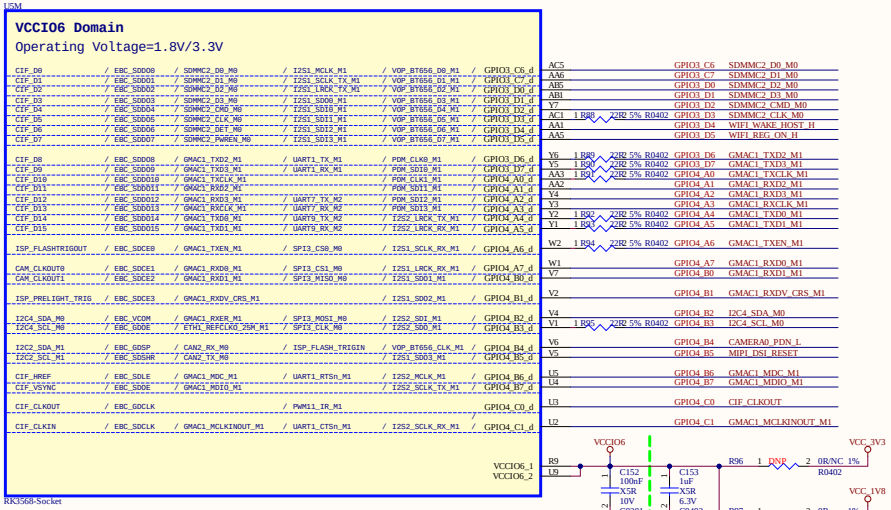
Note:
Caps of between dashed green lines and U5
should be placed under the U5 package.
Other caps should be placed close to the U5 package

Title: ATK-CLRK3568B V1.0.PrjPcb	
Author: ALIENTEK	Size: A3
Date: 2024/8/7	File: ATK_RK3568_USB_PCIE_SATA_PHY.SchDoc
Revision: V1.3	Version:

RK3568_P(MIPI_CSI_RX)



RK3568_M(VCCIO6 Domain)

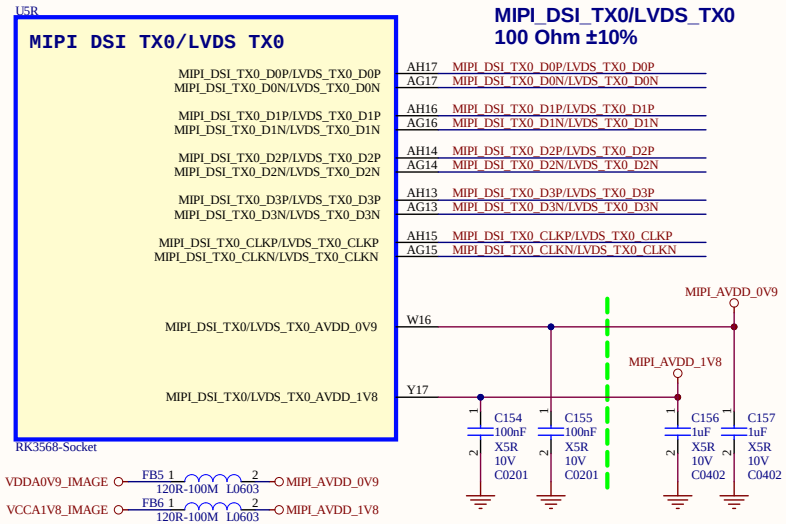


Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

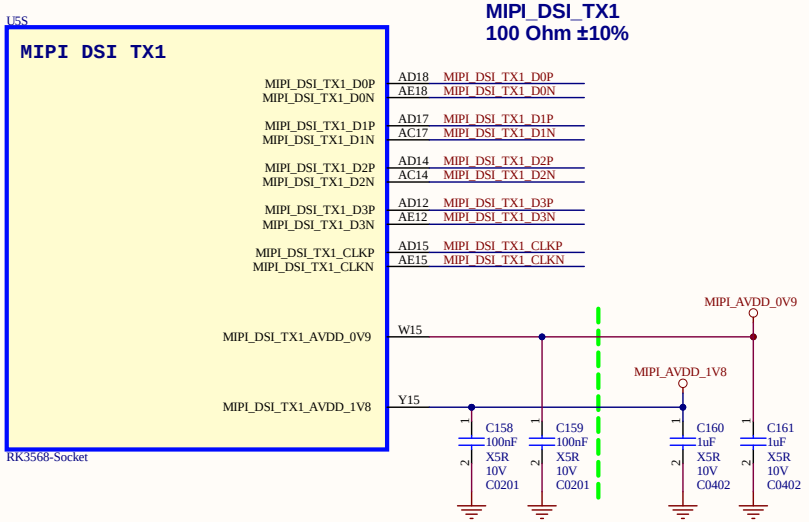
Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

Note:
Caps of between dashed green lines and U5
should be placed under the U5 package.
Other caps should be placed close to the U5 package

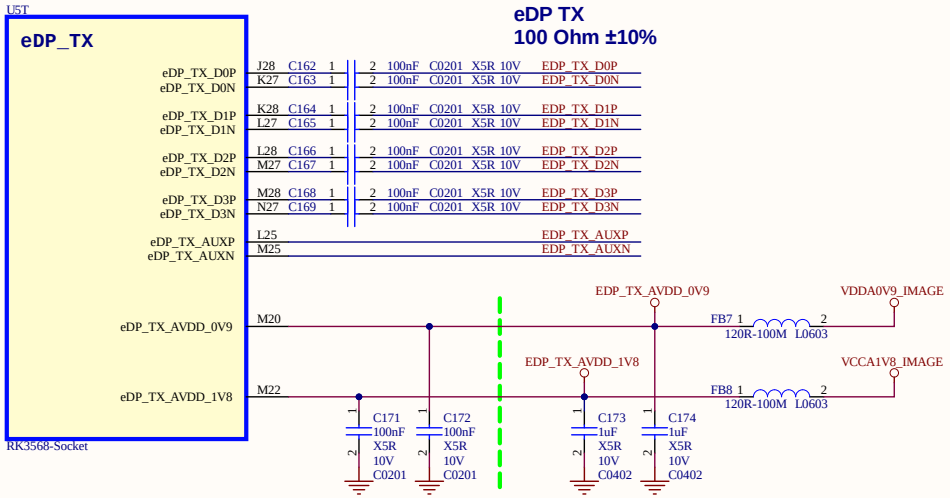
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



RK3568_S(MIPI_DSI_TX1)

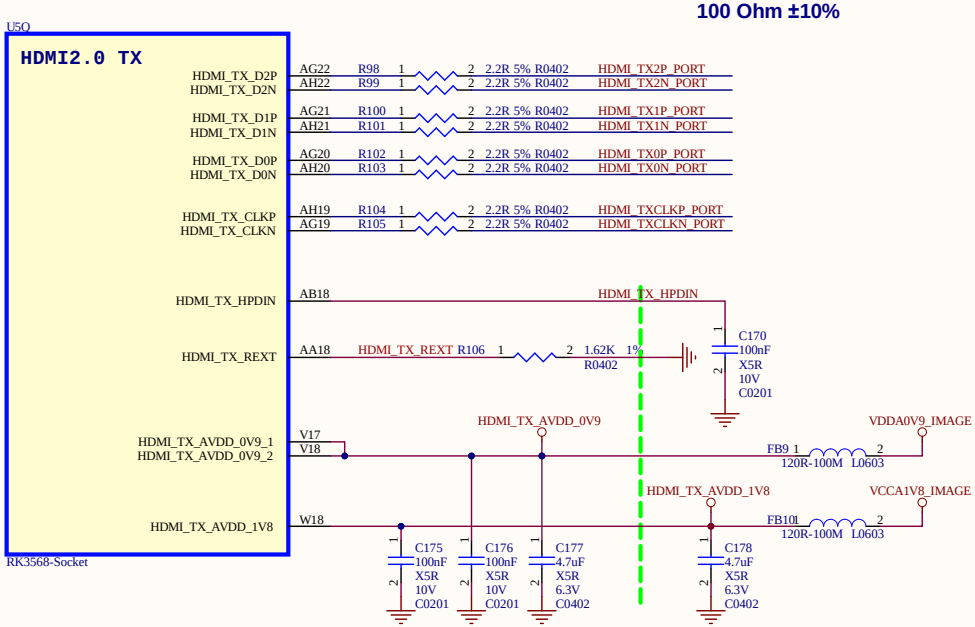


RK3568_T(eDP TX)



Note:
Caps of between dashed green lines and U5
should be placed under the U5 package.
Other caps should be placed close to the U5 package

RK3568_Q(HDMI2.0 TX)



Title: ATK-CLRK3568B V1.0.PrjPcb	
Author: ALIENTEK	Size: A3
Date: 2024/8/7	File: ATK_RK3568_VO Interface_1.SchDoc
Revision: V1.3	Version:

正点原子

RK3568_L(VCCIO5 Domain)

U5L

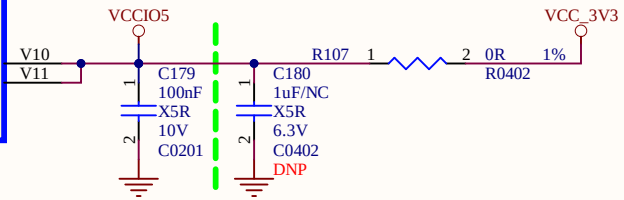
VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	VOP_BT656_D0_M0	SPI0_MISO_M1	PCIE20_CLKREQn_M1	I2S1_MCLK_M2	GPIO2_D0_d
LCDC_D1	VOP_BT656_D1_M0	SPI0_MOSI_M1	PCIE20_WAKEn_M1	I2S1_SCLK_TX_M2	GPIO2_D1_d
LCDC_D2	VOP_BT656_D2_M0	SPI0_CS0_M1	PCIE30X1_CLKREQn_M1	I2S1_LRCK_TX_M2	GPIO2_D2_d
LCDC_D3	VOP_BT656_D3_M0	SPI0_CLK_M1	PCIE30X1_WAKEn_M1	I2S1_SDI0_M2	GPIO2_D3_d
LCDC_D4	VOP_BT656_D4_M0	SPI2_CS1_M1	PCIE30X2_CLKREQn_M1	I2S1_SDI1_M2	GPIO2_D4_d
LCDC_D5	VOP_BT656_D5_M0	SPI2_CS0_M1	PCIE30X2_WAKEn_M1	I2S1_SDI2_M2	GPIO2_D5_d
LCDC_D6	VOP_BT656_D6_M0	SPI2_MOSI_M1	PCIE30X2_PERSTn_M1	I2S1_SDI3_M2	GPIO2_D6_d
LCDC_D7	VOP_BT656_D7_M0	SPI2_MISO_M1	UART8_TX_M1	I2S1_SDO0_M2	GPIO2_D7_d
LCDC_CLK	VOP_BT656_CLK_M0	SPI2_CLK_M1	UART8_RX_M1	I2S1_SDO1_M2	GPIO3_A0_d
LCDC_D8	VOP_BT1120_D0	SPI1_CS0_M1	PCIE30X1_PERSTn_M1	SDMMC2_D0_M1	GPIO3_A1_d
LCDC_D9	VOP_BT1120_D1	GMAC1_TXD2_M0	I2S3_MCLK_M0	SDMMC2_D1_M1	GPIO3_A2_d
LCDC_D10	VOP_BT1120_D2	GMAC1_TXD3_M0	I2S3_SCLK_M0	SDMMC2_D2_M1	GPIO3_A3_d
LCDC_D11	VOP_BT1120_D3	GMAC1_RXD2_M0	I2S3_LRCK_M0	SDMMC2_D3_M1	GPIO3_A4_d
LCDC_D12	VOP_BT1120_D4	GMAC1_RXD3_M0	I2S3_SDO_M0	SDMMC2_CMD_M1	GPIO3_A5_d
LCDC_D13	VOP_BT1120_CLK	GMAC1_TXCLK_M0	I2S3_SDI_M0	SDMMC2_CLK_M1	GPIO3_A6_d
LCDC_D14	VOP_BT1120_D5	GMAC1_RXCLK_M0		SDMMC2_DET_M1	GPIO3_A7_d
LCDC_D15	VOP_BT1120_D6	ETH1_REFCLKO_25M_M0		SDMMC2_PWREN_M1	GPIO3_B0_d
LCDC_D16	VOP_BT1120_D7	GMAC1_RXD0_M0	UART4_RX_M1	PWM8_M0	GPIO3_B1_d
LCDC_D17	VOP_BT1120_D8	GMAC1_RXD1_M0	UART4_TX_M1	PWM9_M0	GPIO3_B2_d
LCDC_D18	VOP_BT1120_D9	GMAC1_RXDV_CRS_M0	I2C5_SCL_M0	PDM_SDI0_M2	GPIO3_B3_d
LCDC_D19	VOP_BT1120_D10	GMAC1_RXER_M0	I2C5_SDA_M0	PDM_SDI1_M2	GPIO3_B4_d
LCDC_D20	VOP_BT1120_D11	GMAC1_TXD0_M0	I2C3_SCL_M1	PWM10_M0	GPIO3_B5_d
LCDC_D21	VOP_BT1120_D12	GMAC1_TXD1_M0	I2C3_SDA_M1	PWM11_IR_M0	GPIO3_B6_d
LCDC_D22	PWM12_M0	GMAC1_TXEN_M0	UART3_TX_M1	PDM_SDI2_M2	GPIO3_B7_d
LCDC_D23	PWM13_M0	GMAC1_MCLKINOUT_M0	UART3_RX_M1	PDM_SDI3_M2	GPIO3_C0_d
LCDC_HSYNC	VOP_BT1120_D13	SPI1_MOSI_M1	PCIE20_PERSTn_M1	I2S1_SDO2_M2	GPIO3_C1_d
LCDC_VSYNC	VOP_BT1120_D14	SPI1_MISO_M1	UART5_TX_M1	I2S1_SDO3_M2	GPIO3_C2_d
LCDC_DEN	VOP_BT1120_D15	SPI1_CLK_M1	UART5_RX_M1	I2S1_SCLK_RX_M2	GPIO3_C3_d
PWM14_M0	VOP_PWM_M1	GMAC1_MDC_M0	UART7_TX_M1	PDM_CLK1_M2	GPIO3_C4_d
PWM15_IR_M0	SPDIF_TX_M1	GMAC1_MDIO_M0	UART7_RX_M1	I2S1_LRCK_RX_M2	GPIO3_C5_d

AG6	GPIO2_D0	GMAC1_INT/PMEB
AD7	GPIO2_D1	GMAC1_RSTn
AC8	GPIO2_D2	GMAC0_INT/PMEB
AC7	GPIO2_D3	GMAC0_RSTn
AF5	GPIO2_D4	PCIE30X2_CLKREQn_M1
AF6	GPIO2_D5	PCIE30X2_WAKEn_M1
AD6	GPIO2_D6	PCIE30X2_PERSTn_M1
AH5	GPIO2_D7	PCIE30X2_PRSNT_L
AH4	GPIO3_A0	BT_REG_ON_H
AB8	GPIO3_A1	SPI1_CS0_M1
AE5	GPIO3_A2	HOST_WAKE_BT_H
AG4	GPIO3_A3	I2S3_SCLK_M0
AF4	GPIO3_A4	I2S3_LRCK_M0
AH3	GPIO3_A5	I2S3_SDO_M0
AG3	GPIO3_A6	I2S3_SDI_M0
AH2	GPIO3_A7	PCIECLKIC_OE_H
AG2	GPIO3_B0	5G_DISABLE
AG1	GPIO3_B1	UART4_RX_M1
AF2	GPIO3_B2	UART4_TX_M1
AF1	GPIO3_B3	I2C5_SCL_M0
AE1	GPIO3_B4	I2C5_SDA_M0
AE2	GPIO3_B5	MIPICAM1_RST_L
AE3	GPIO3_B6	MIPICAM0_RST_L
AD4	GPIO3_B7	UART3_TX_M1
AD2	GPIO3_C0	UART3_RX_M1
AD1	GPIO3_C1	SPI1_MOSI_M1
AA7	GPIO3_C2	SPI1_MISO_M1
AC4	GPIO3_C3	SPI1_CLK_M1
AC3	GPIO3_C4	LVDS_TP_RST_L
AC2	GPIO3_C5	

VCCIO5_1
VCCIO5_2



RK3568-Socket

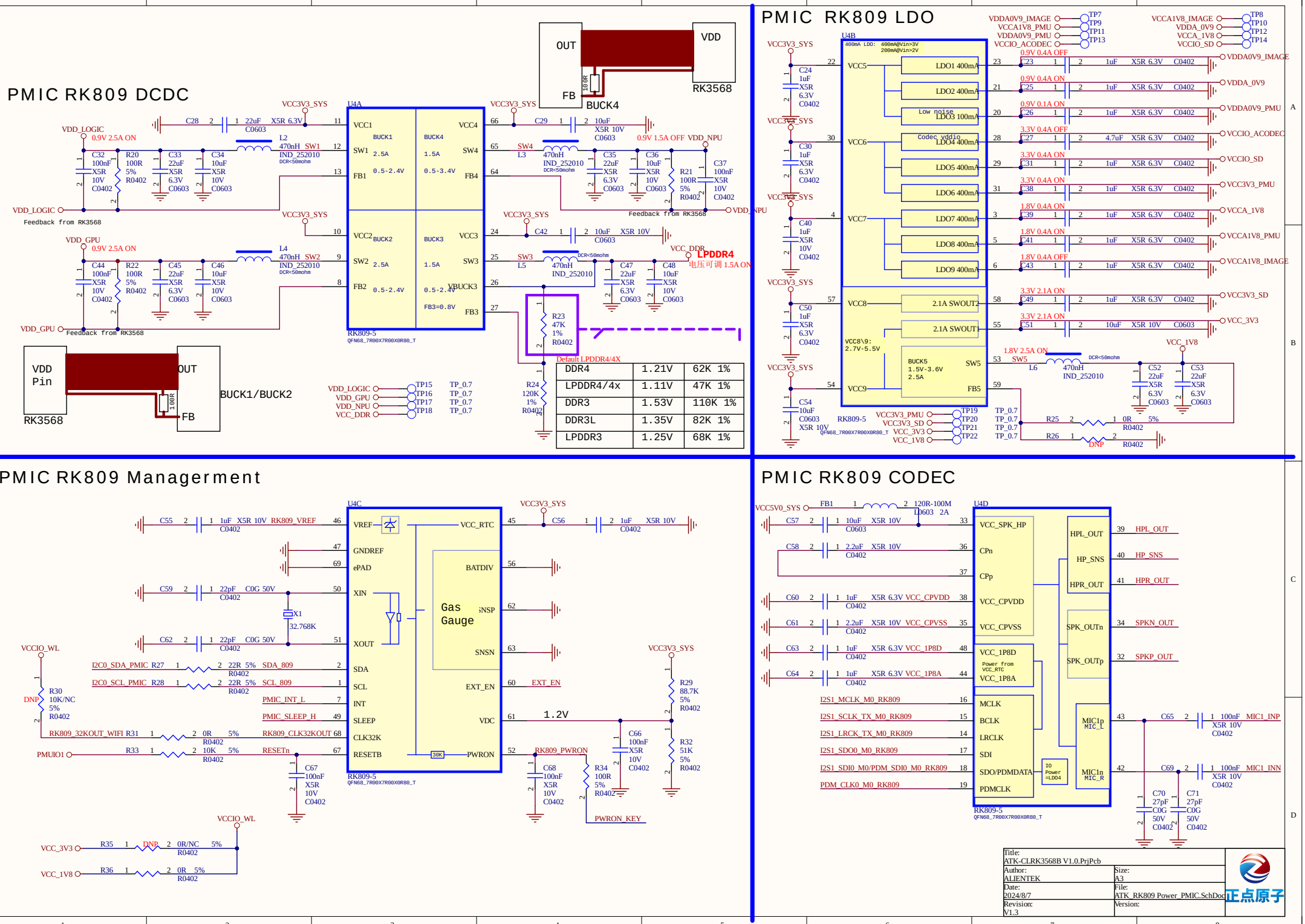
Note:

Caps of between dashed green lines and U5 should be placed under the U5 package

Rockchip Confidential

Title: ATK-CLRK3568B V1.0.PrjPcb	
Author: ALIENTEK	Size: A4
Date: 2024/8/7	File: ATK_RK3568_VO_Interface_2.SchDoc
Revision: V1.3	Version:

正点原子


PMIC RK809 DCDC
PMIC RK809 LDO
PMIC RK809 Managerment
PMIC RK809 CODEC
VDD_LOGIC
0.9V 2.5A ON
VDD_GPU
0.9V 2.5A ON
VDD_NPU
0.9V 1.5A OFF
VCC_DDR
LPDDR4
电压可调 1.5A ON
Default LPDDR4/4X
DDR4 1.21V 62K 1%
LPDDR4/4x 1.11V 47K 1%
DDR3 1.53V 110K 1%
DDR3L 1.35V 82K 1%
LPDDR3 1.25V 68K 1%
BUCK1/BUCK2
BUCK4
RK3568
RK809-5
Gas Gauge
1.2V
Title: ATK-CLRK3568B V1.0.PrjPcb
Author: ALIENTEK
Size: A3
Date: 2024/8/7
File: ATK_RK809 Power_PMIC.SchDoc
Revision: V1.3
Version:
正点原子