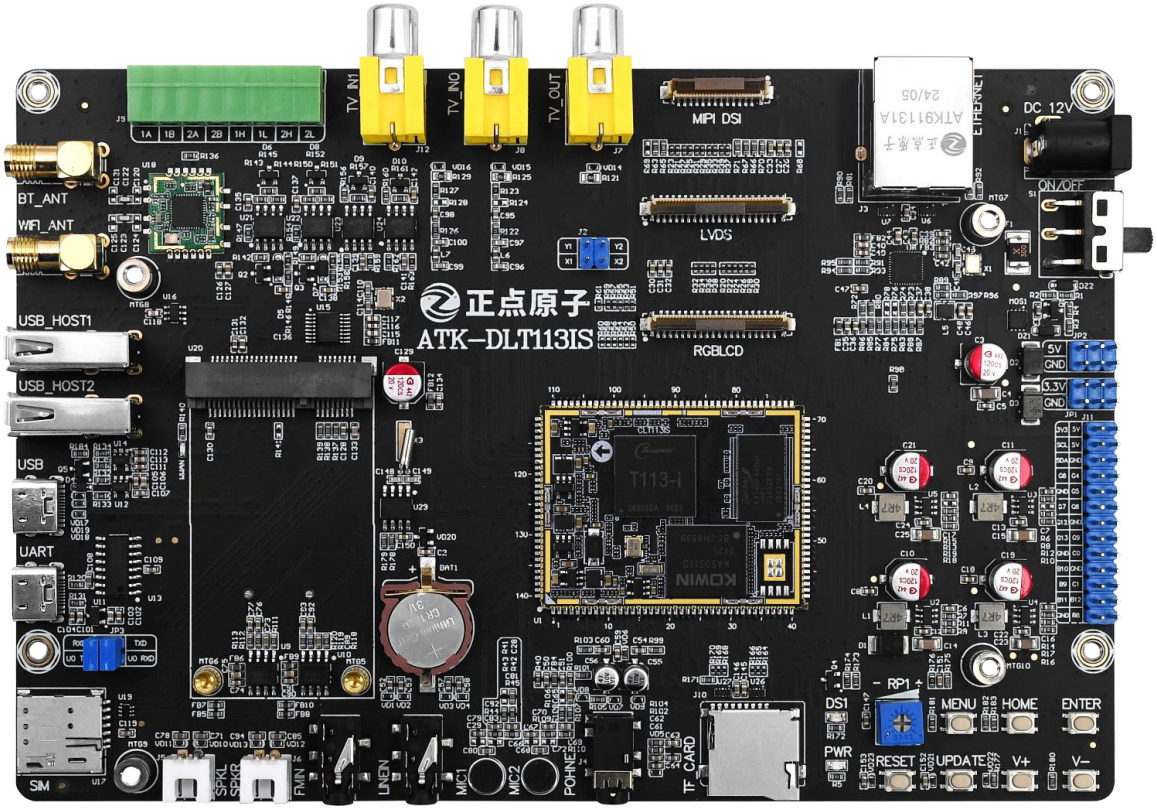
ATK-DLT113IS

Hardware Reference Manual

V1.0



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In order to get the latest version of product information, please regularly visit the download center or contact the customer service of Taobao ALIENTEK flagship store. Thank you for your tolerance and support.

Revision History:

Version	Version Update Notes	Responsible person	Proofreading	Date
V1.0	release officially	ALIENTEK	ALIENTEK	2024.04.29

Catalogue

Chapter 1. Research on resources of ATK-DLT113IS development board

ALIENTEK currently has multiple STM32, I.MXRT, Linux and FPGA development boards, which have consistently ranked as the top-selling products on Taobao for years, with cumulative shipments exceeding 100,000 units. This ATK-DLT113IS development board is the first Linux development board launched by ALIENTEK that is equipped with a chip from Allwinner Technology. Now, let's introduce the ATK-DLT113IS development board.

1.1 Resources of the ATK-DLT113IS Development Board

This development board adopts a design combining a base board and a core board, connected through a pin header. The core board occupies a small space and has excellent stability. The development board is powered by a 12V/1A power adapter. In terms of real-world interfaces, the development board has three screen interfaces, namely RGB, LVDS, and MIPI DSI, and also has three audio input interfaces and two audio output interfaces. Additionally, it has a gigabit Ethernet port, two 485 interfaces, and two CAN interfaces, making it highly suitable for industrial applications.

The resource diagram of the ATK-DLT113IS development board base is shown as follows:

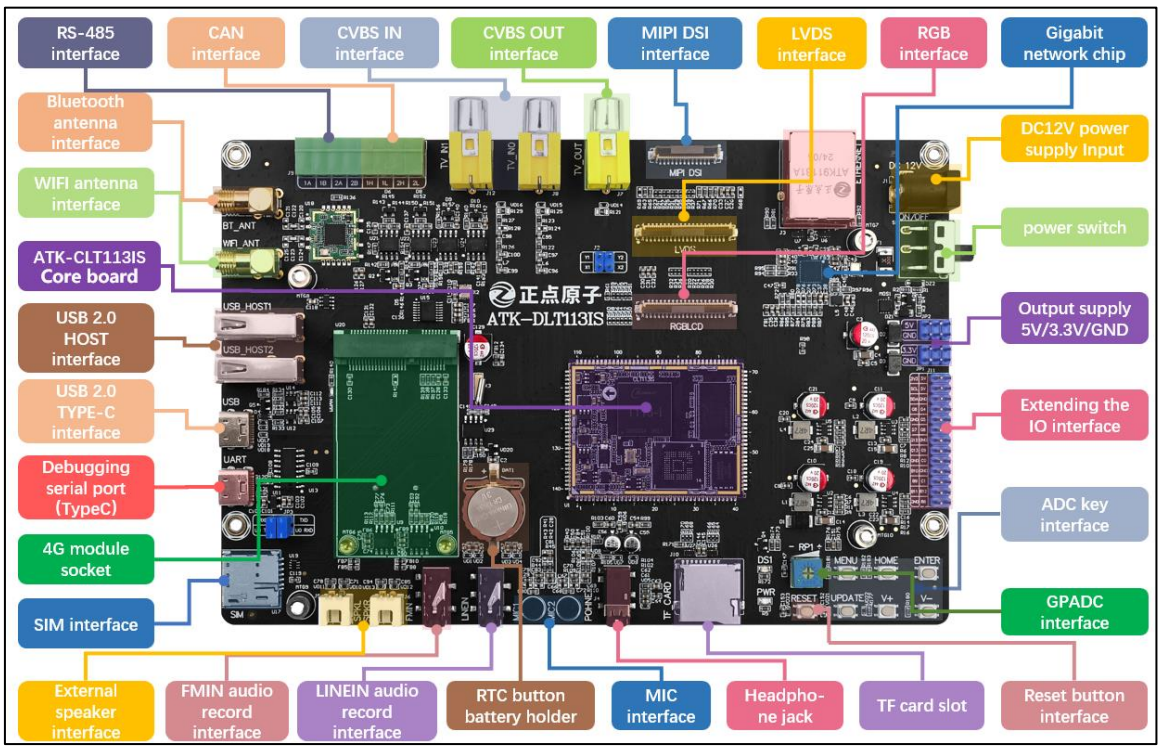

Figure 1.1-1 Development board resource map

1.2 Dimensional Diagram of ATK-DLT113IS Development Board

The dimensional diagram of the ATK-DLT113IS development board is as shown in the following figure:

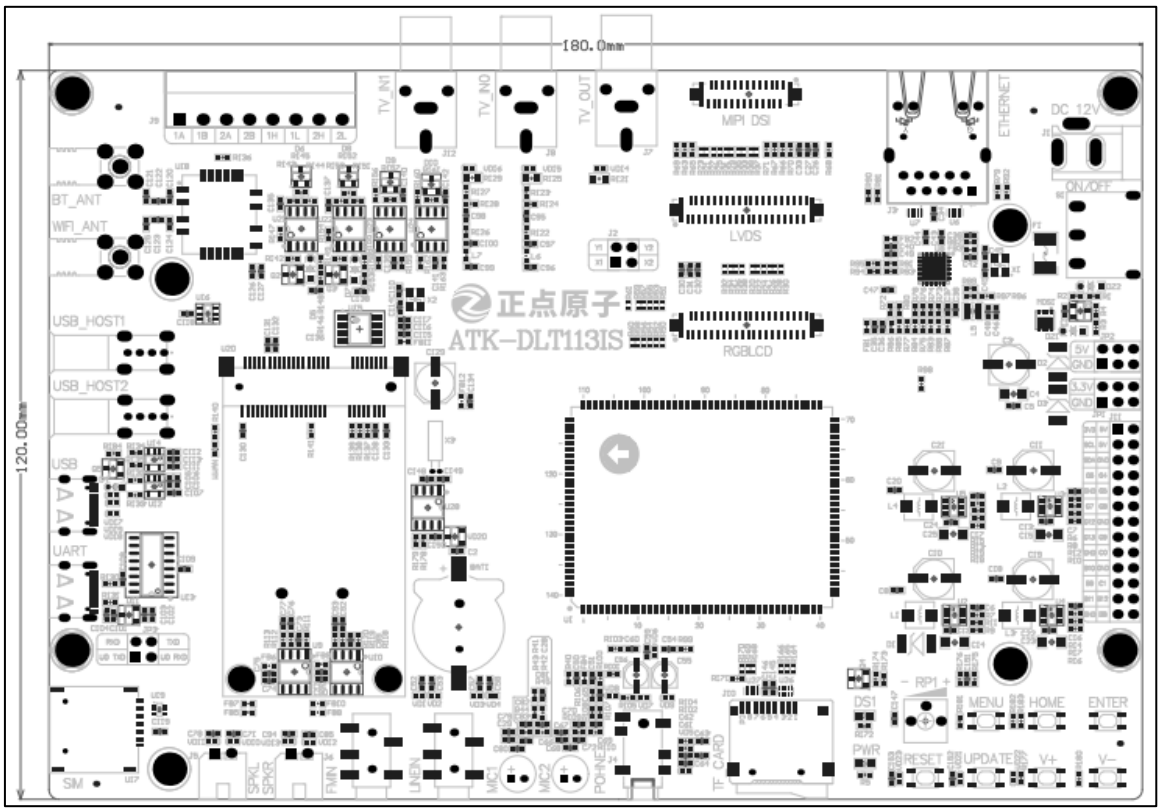

Figure 1.2-1 Development board size diagram

Chapter 2. ATK-DLT113IS Development Board Resource Description

2.1 Hardware Resource Description of the ATK-DLT113IS Development Board

1. RGB Interface

The ATK-DLT113IS development board provides a 18-bit data interface through the FPC socket, and is defaultly compatible with the ALIENTEK RGB screen.

2. LVDS Interface

The ATK-DLT113IS development board is equipped with one LVDS interface, which is defaultly supported by the ALIENTEK 10.1-inch LVDS screen.

3. MIPI DSI interface

The ATK-DLT113IS development board is equipped with one MIPI DSI interface, which is defaultly supported by the ALIENTEK 5.5-inch MIPI screen.

4. Network interface

The ATK-DLT113IS development board is equipped with one gigabit network port, supporting 10/100/1000Mbps auto-adaptation, and it is connected through the RJ45 connector.

5. RS485 interface

The ATK-DLT113IS development board is equipped with two self-transmitting and receiving RS-485 interfaces.

6. CAN interface

The ATK-DLT113IS development board is equipped with two CAN interfaces.

7. USB interface

The ATK-DLT113IS development board is equipped with two USB HOST interfaces and one USB OTG interface.

8. CVBS interface

The ATK-DLT113IS development board is equipped with two CVBS OUT interfaces and one CVBS IN interface.

9. USB-TTL interface

The ATK-DLT113IS development board is equipped with one USB-TTL serial debugging interface, which is recommended to be retained when designing the own baseboard.

10. 4G module interface

The ATK-DLT113IS development board is equipped with a 4G Mini PCIE interface, supporting the high-tech ME3630 and MTK's EC20 4G modules.

11. Audio interface

The ATK-DLT113IS development board is equipped with two MIC recording interfaces, one headphone interface, one LINE IN interface and one FMIN interface.

12. RTC

The ATK-DLT113IS development board is equipped with an independent RTC chip, powered by a button battery, and it records the time after the baseboard is powered off.

13. TF-CARD interface

The ATK-DLT113IS development board is equipped with one TF card interface, which can be used as a boot and burning function.

14. GPADC interface

The ATK-DLT113IS development board is equipped with one GPADC interface, with a range of 0~1.8V.

15. USB WIFI & Bluetooth interface

The ATK-DLT113IS development board is equipped with the RTL8733BU module, connected through the USB interface.

16. LED

The ATK-DLT113IS development board is equipped with two LEDs, one power indicator light (blue), one user LED (yellow-green).

17. Keys

The ATK-DLT113IS development board is equipped with 7 keys, among which 5 are 5 ADC keys with one ADC pin output, one reset key and one burn key.

18. 3.3V/5V power supply interface

The ATK-DLT113IS development board is connected by two 2 x 3 ribbon cables to provide 3.3V/5.0V power, facilitating debugging.

Chapter 3. ATK-DLT113IS Development Board Description

3.1 Core Board Interface

The ATK-DLT113IS development board is designed in the form of core board + base board. The core board and the base board are connected through stamp holes, which ensures excellent stability and the core board occupies a small space. The interface of the core board is shown in the following figure:

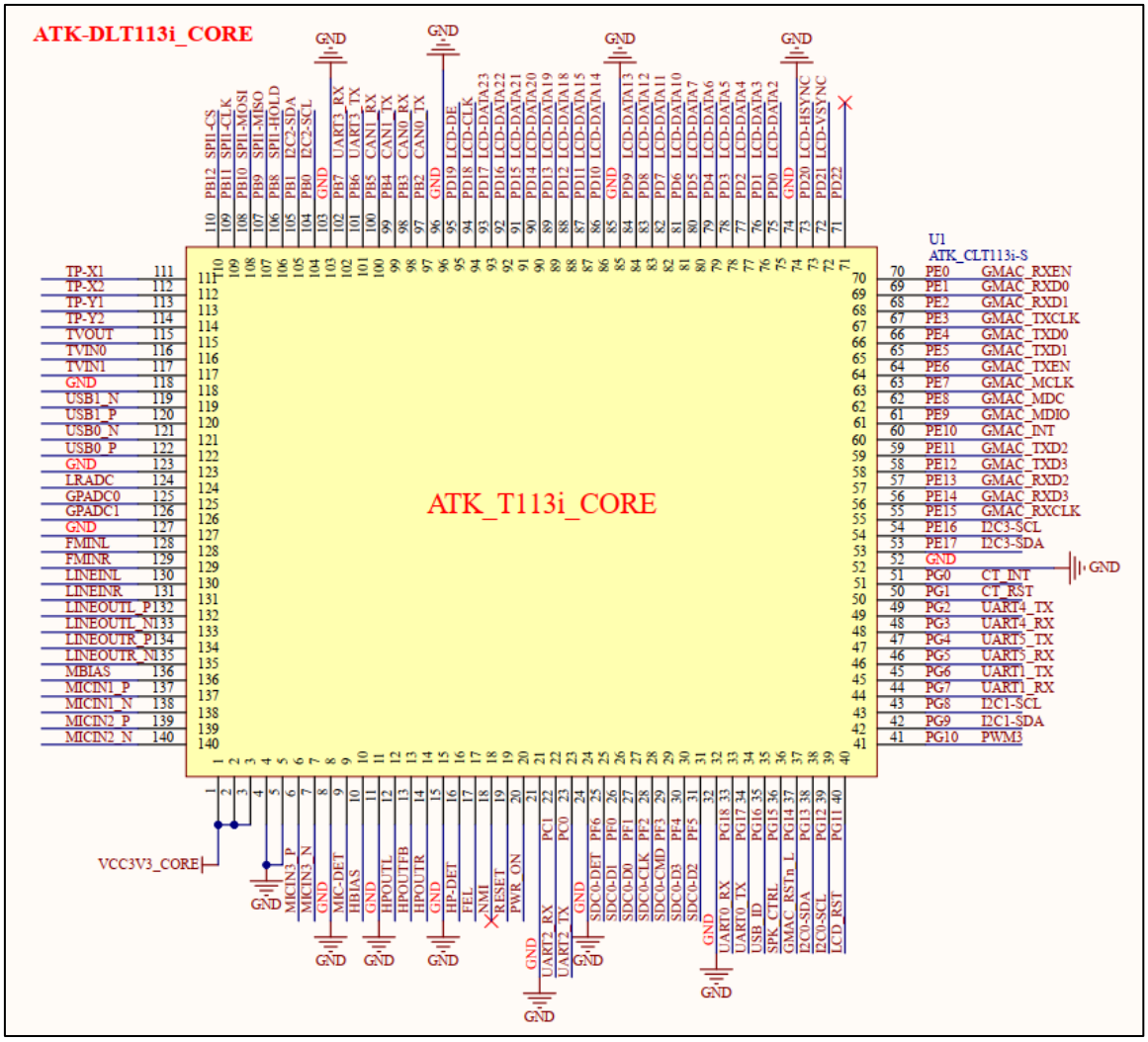

Figure 3.1-1 Core board pins

3.2 USB-TTL interface

The development board is equipped with a USB-to-TTL conversion chip CH343G, which converts serial port signals into TTL signals.

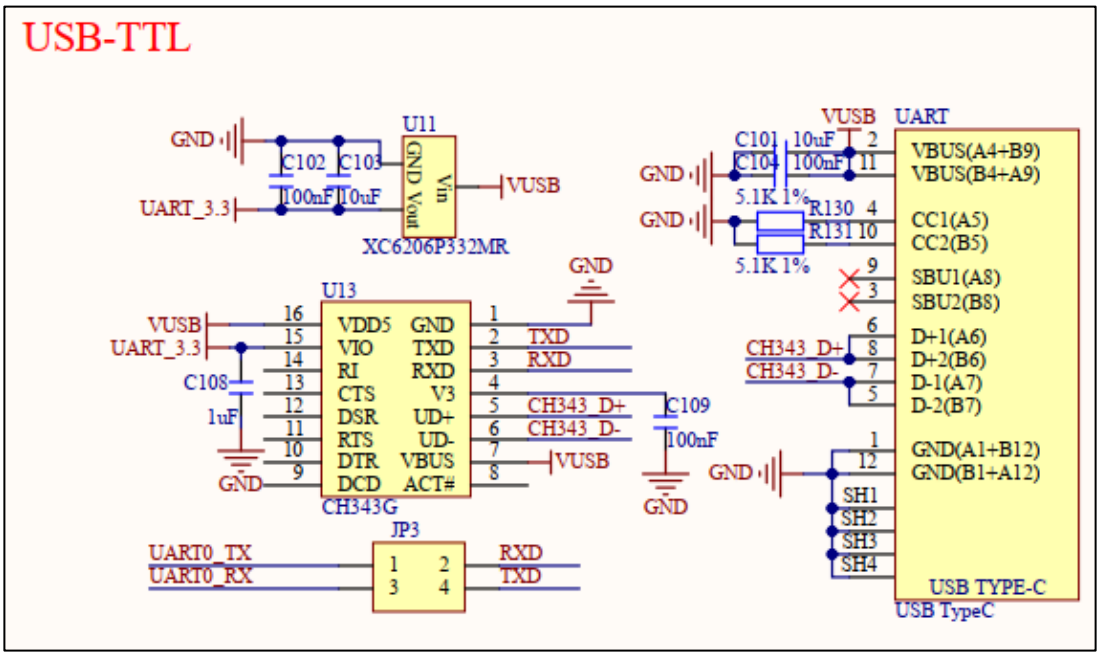

Figure 3.2-1 USB-TTL circuit diagram

3.3 RGB LCD module interface

The development board is equipped with the RGB LCD interface. The circuit for this part is shown in the figure:

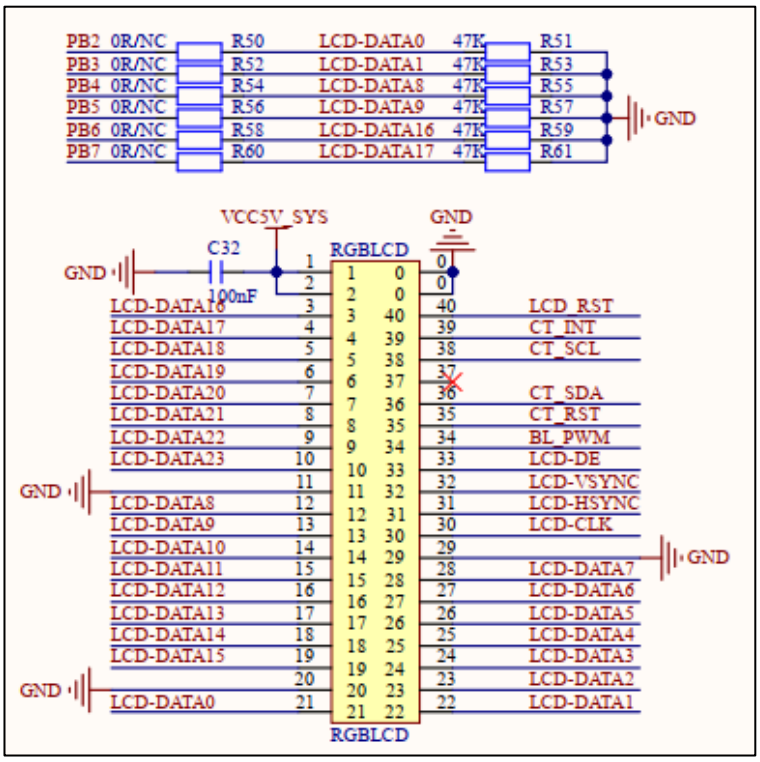

Figure 3.3-1 RGB interface circuit diagram

In the figure, the RGB LCD interface adopts the RGB565 data format and supports touch screens (both resistive and capacitive screens are supported). This interface only supports LCDs with RGB

interfaces (does not support LCDs with MCU interfaces). Currently, the RGB interface LCD modules from ALIENTEK include: 4.3 inches (480*272 and 800*480), 7 inches (800*480 and 1024*600), and 10 inches (1280*800) in various sizes.

The CT_SCL and CT_SDA in the figure are the two data lines of I2C2, connected to the I2C2-SCL and I2C2-SDA IOs respectively. BL_PWM is the backlight control IO of the LCD, connected to PWM3, used to control the backlight of the LCD.

3.4 LVDS interface

The development board is equipped with one LVDS LCD interface. The circuit of this part is shown in the figure. The LVDS interface is a four-channel interface and supports the ALIENTEK 10.1-inch LVDS display screen.

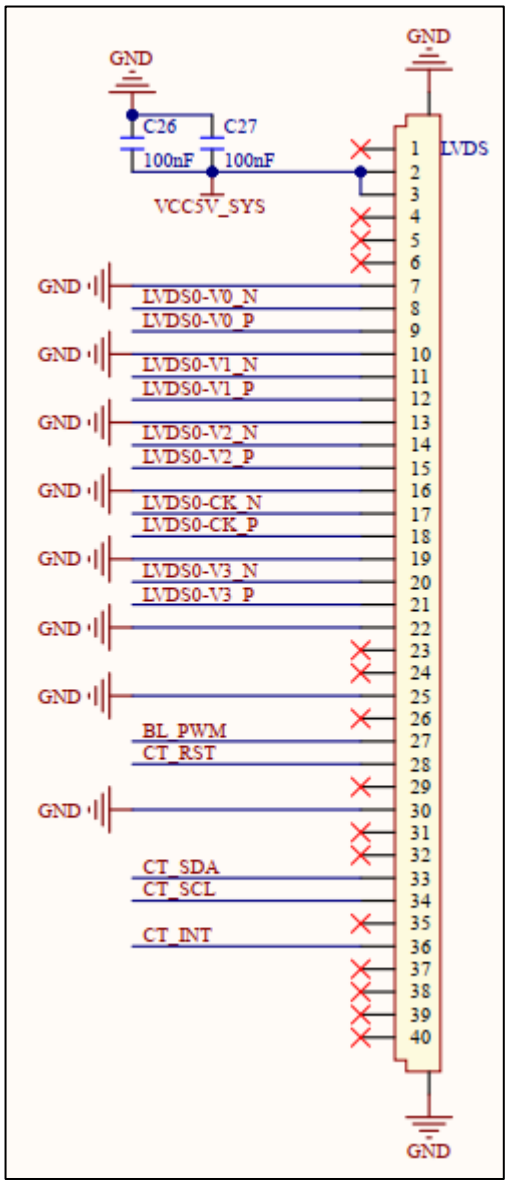

Figure 3.4-1 LVDS interface circuit diagram

3.5 MIPI DSI interface

The development board is equipped with a MIPI DSI interface. The circuitry for this part is shown in the figure. The MIPI DSI interface is a 4-wire system and supports the ALIENTEK 5.5-inch MIPI display.

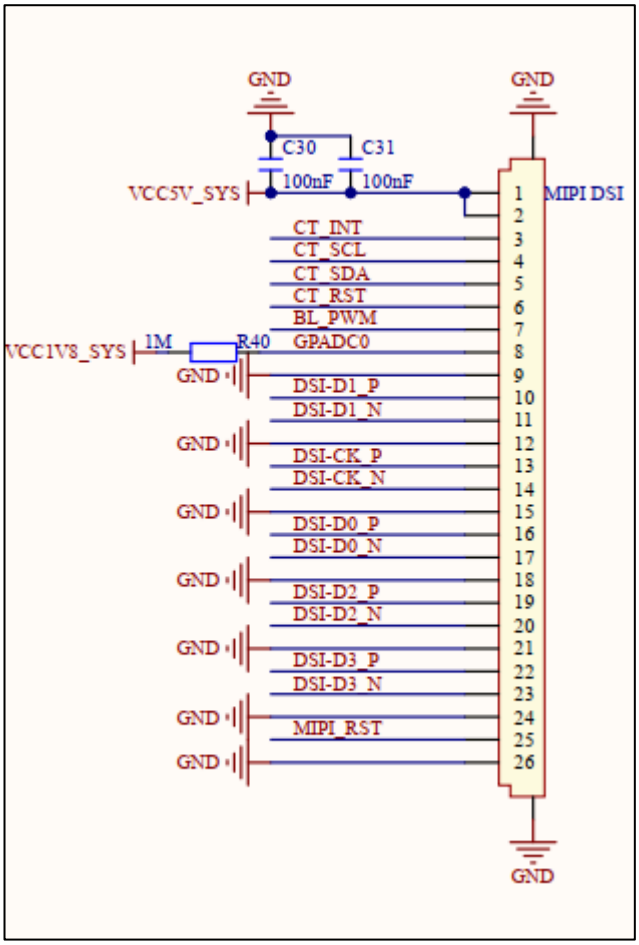

Figure 3.5-1 MIPI interface circuit diagram

3.6 Reset circuit

The schematic diagram of the reset circuit of the development board is shown as follows. VD23 is an ESD chip used to prevent static electricity, and a 100nF capacitor C153 is equipped to reduce power supply noise, ensuring stable startup and operation of the system.

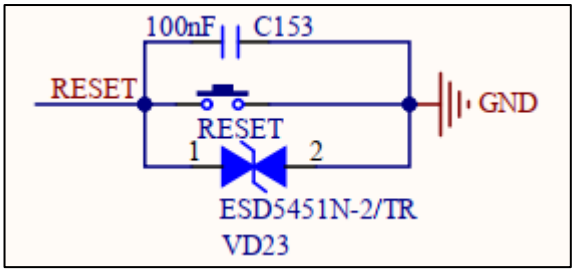

Figure 3.6-1 Reset circuit

3.7 RS485 interface

The schematic diagram of the RS485 interface circuit on the development board is shown in the following figure. The RS485 level cannot be directly connected to the T113 core board and requires a level conversion chip. Here, we use the SP3485 for 485 level conversion. R145/R152 are terminal matching resistors, while R14/R144 and R150/R151 are two bias resistors to ensure that the 485 bus maintains logic 1 in the silent state.

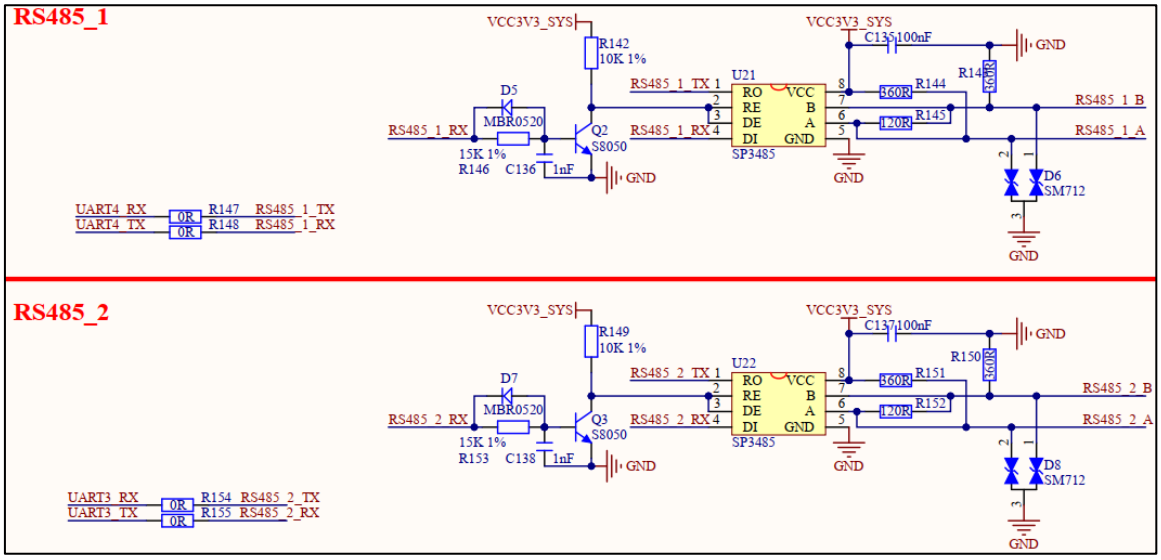

Figure 3.7-1 RS485 interface circuit

3.8 CAN interface

The schematic diagram of the CAN interface circuit on the development board is shown in the figure. The CAN chip used by the development board is TPT1051V. Among them, R157/R161 are termination matching resistors.

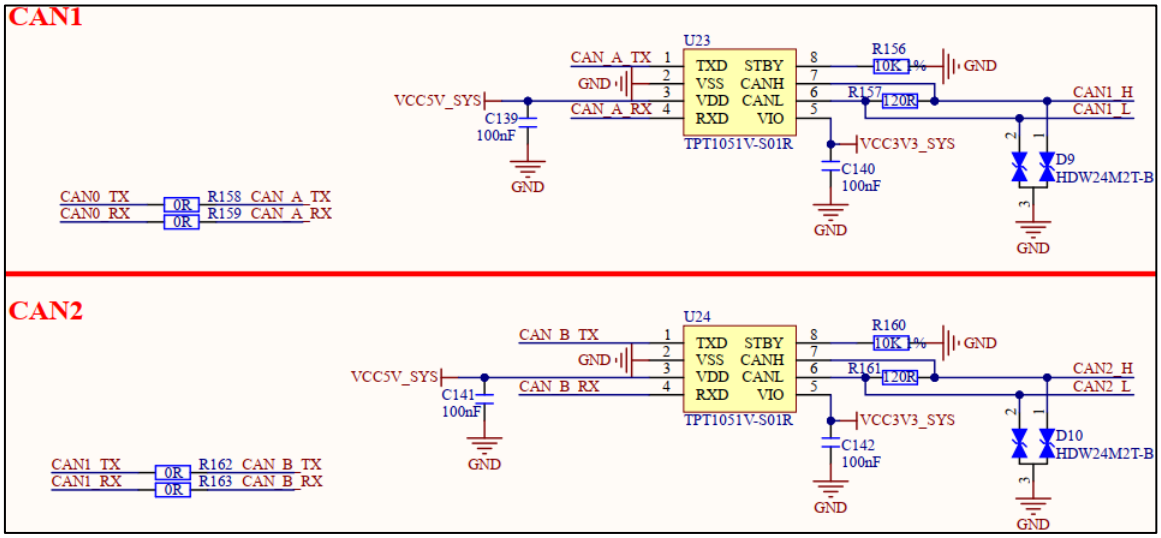

Figure 3.8-1 CAN interface circuit

3.9 USB HUB Interface

The development board is equipped with a 4-port USB HUB chip, which is used to expand the USB 1 interface to 4 USB HOST interfaces (one for the 4G module, one for the WIFI & BT module, and the remaining two can be used to connect external USB devices). The schematic diagram is shown below:

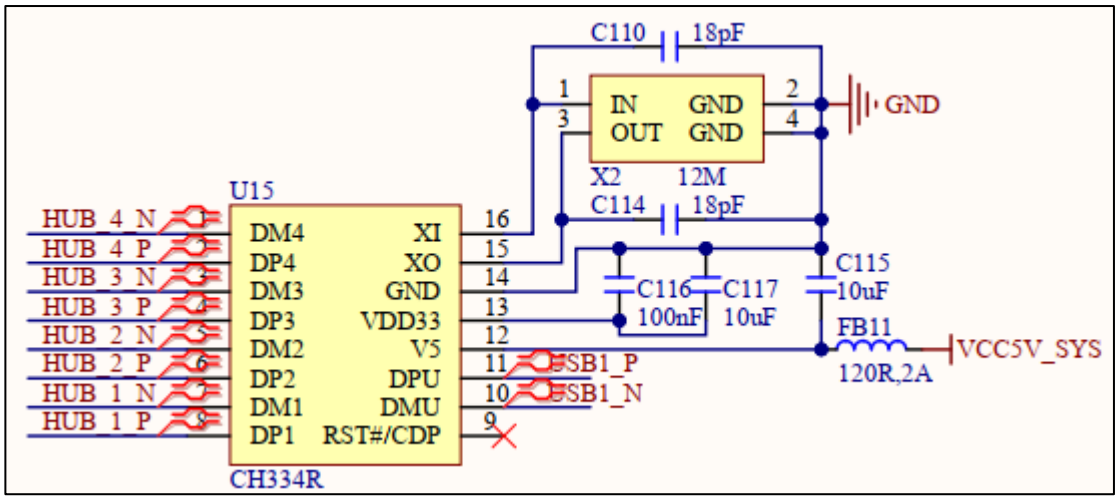

Figure 3.9-1 USB HOST interface circuit diagram

3.10 USB OTG (Type-C) interface

The development board is equipped with a USB OTG interface. The USB OTG interface uses T113-i's USB0. The schematic diagram of the USB OTG interface is shown below:

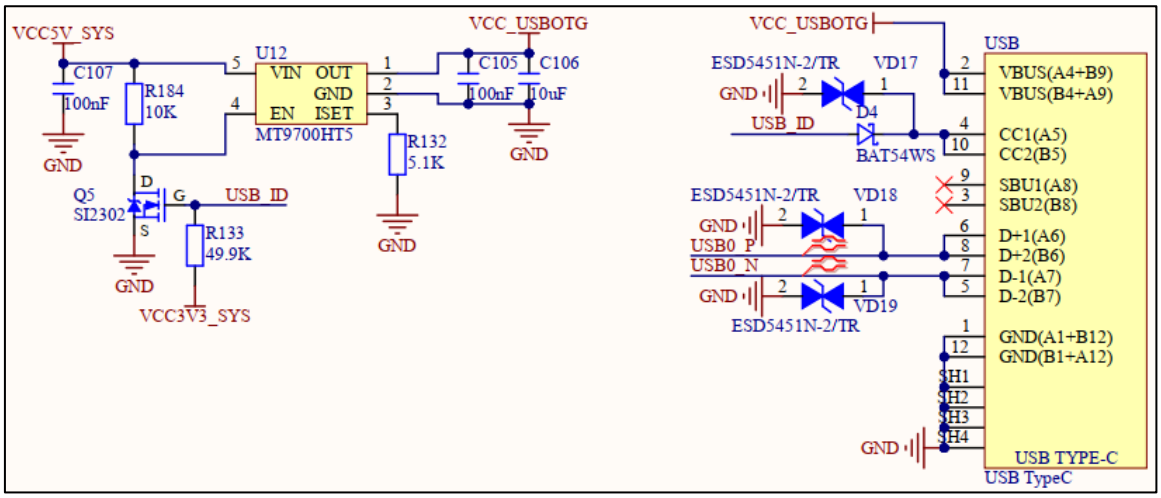

Figure 3.10-1 USB OTG Interface Circuit Diagram

This USB OTG interface can function as both a host (HOST) and a device (DEVICE), thereby achieving complete OTG functionality.

Device mode: In the diagram, the 49.9K resistor R133 is used to default to pulling up the OTG_ID line. When the ID line is at a high level, it indicates that the OTG is operating in device mode. At this time, since the OTG_ID is at a high level, Q6 (SI2302) is conductive, so the EN pin of MT9700HT5 is grounded. At this point, the OUT pin of MT9700HT5 does not output, and thus the USB_OTG_VBUS voltage is turned off. The USB_OTG_VBUS voltage is used to provide a 5V power supply to external

devices when the OTG is in host mode. Obviously, when the OTG is in device mode, the OTG does not need to provide the USB_OTG_VBUS power supply to the outside. Here, the MT9700HT5 chip is used to implement the control of the VBUS power supply switch.

Host mode: If you want to utilize the HOST function of OTG, then a Type-C OTG cable must be used. The Type-C OTG cable will pull down CC1 and CC2, so the OTG_ID line will also be pulled down. When the ID line is 0, it indicates that the OTG is operating in the host mode. At this time, since the OTG_ID is low, Q6 (SI2302) does not conduct, so the EN pin of MT9700HT5 will be pulled up to 5V by the 10K resistor R184. Therefore, the OUT pin of MT9700HT5 will output a 5V voltage, meaning that TYPEC-VBUS is now 5V and can provide a 5V power supply to external devices.

3.11 LED

The development board is equipped with one user button. Its schematic diagram is shown in the figure. Q4 is used for current amplification.

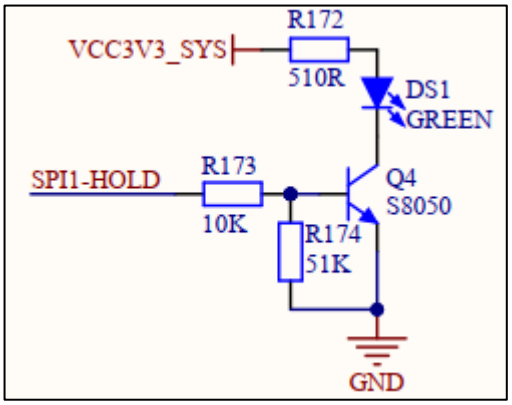

Figure 3.11-1 LED circuit

3.12 Keys

The development board has 7 keys, including one reset key and one programming key. The remaining five keys are ADC keys derived from the LRADC pins and are shown in the schematic diagram below:

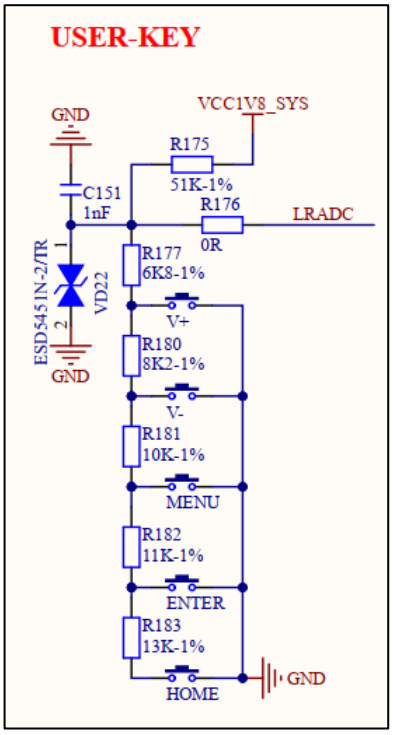

Figure 3.12-1 ADC key circuit

3.13 CVBS OUT interface

The development board is equipped with one CVBS OUT interface. The schematic diagram is shown as follows:

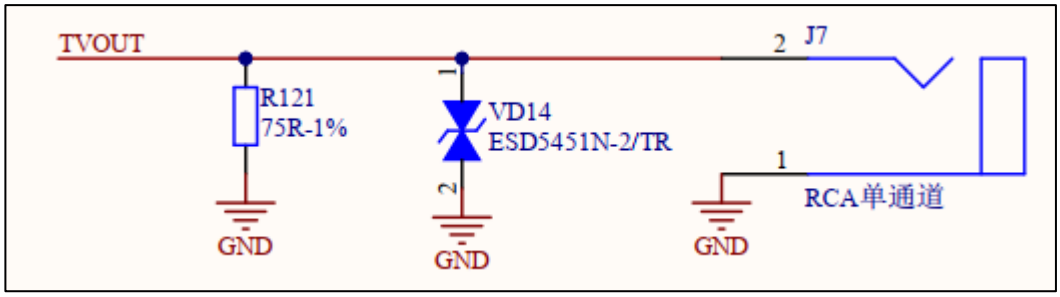

Figure 3.13-1 CVBS OUT interface circuit diagram

3.14 CVBS IN Interface

The development board is equipped with two CVBS IN interfaces. The schematic diagram is shown as follows. When the CVBS input voltage is greater than 1.8V, R2 = 4.7K, R1 = 10K. When the CVBS input voltage is less than or equal to 1.8V, R2 = 0R, R1 = NC.

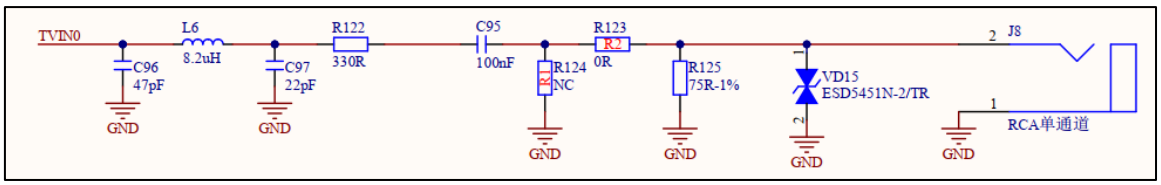

Figure 3.14-1 CVBS IN interface circuit diagram

3.15 TF card interface

The development board is equipped with a TF card (small card) interface. Its schematic diagram is shown in the figure. In the figure, TF_CARD represents the TF card interface, and the TF card is driven in 4-bit SDMMC mode, which is very suitable for situations requiring high-speed storage. SDC0-DET is the TF card detection pin, used for detecting the insertion and removal process of the TF card.

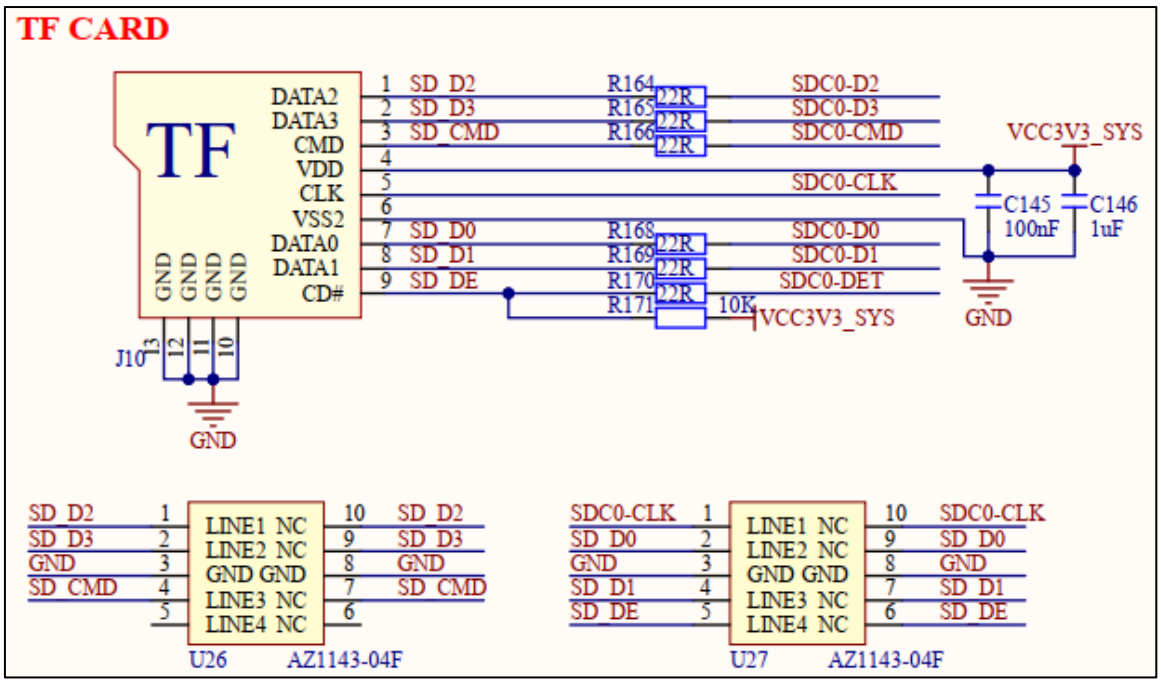

Figure 3.15-1 TF card interface circuit

3.16 WIFI & BT interface

The development board is equipped with a USB WIFI & BT module, as shown in the figure below. The WIFI & Bluetooth module uses RTL8733BU.

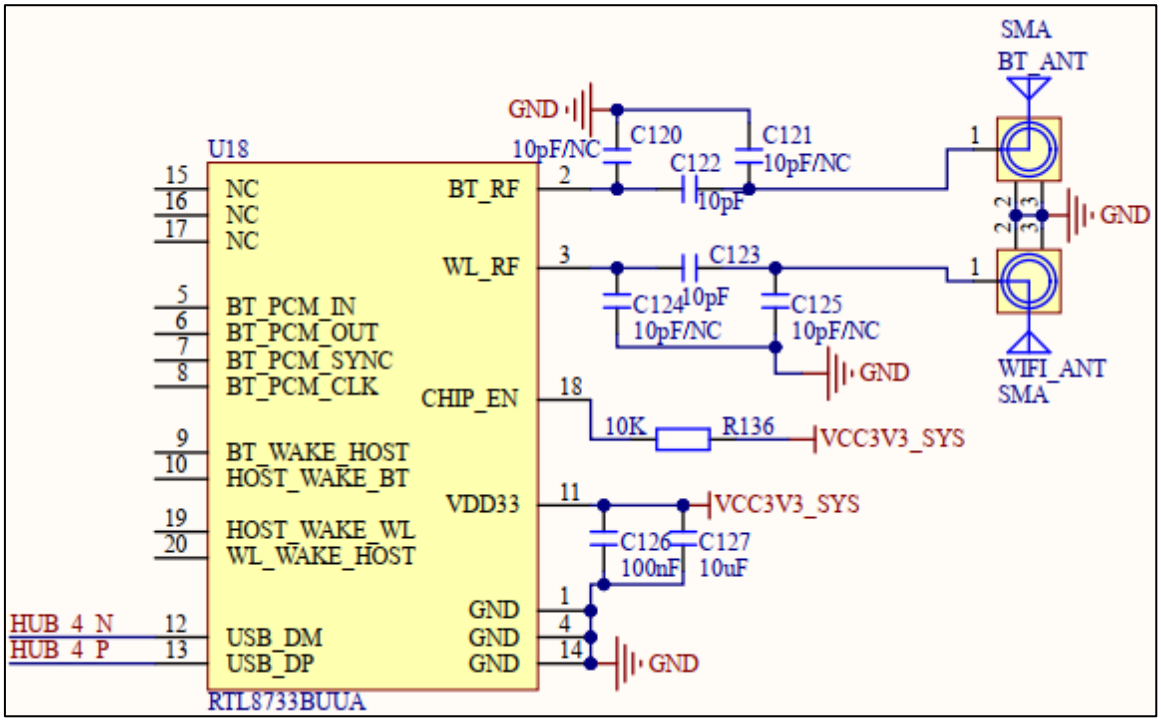

Figure 3.16-1 WIFI & BT Circuit

3.17 4G module interface

The development board is equipped with a 4G Mini PCIE interface. The schematic diagram is shown in the following figure. U20 is the 4G module socket for the Mini PCIE interface, used to connect the 4G module with the Mini PCIE interface, such as the ME3630 module from Gosuncn. Although the 4G module adopts the Mini PCIE interface, it actually uses the USB interface. Here, it is connected to a USB HOST interface expanded by the CH334R.

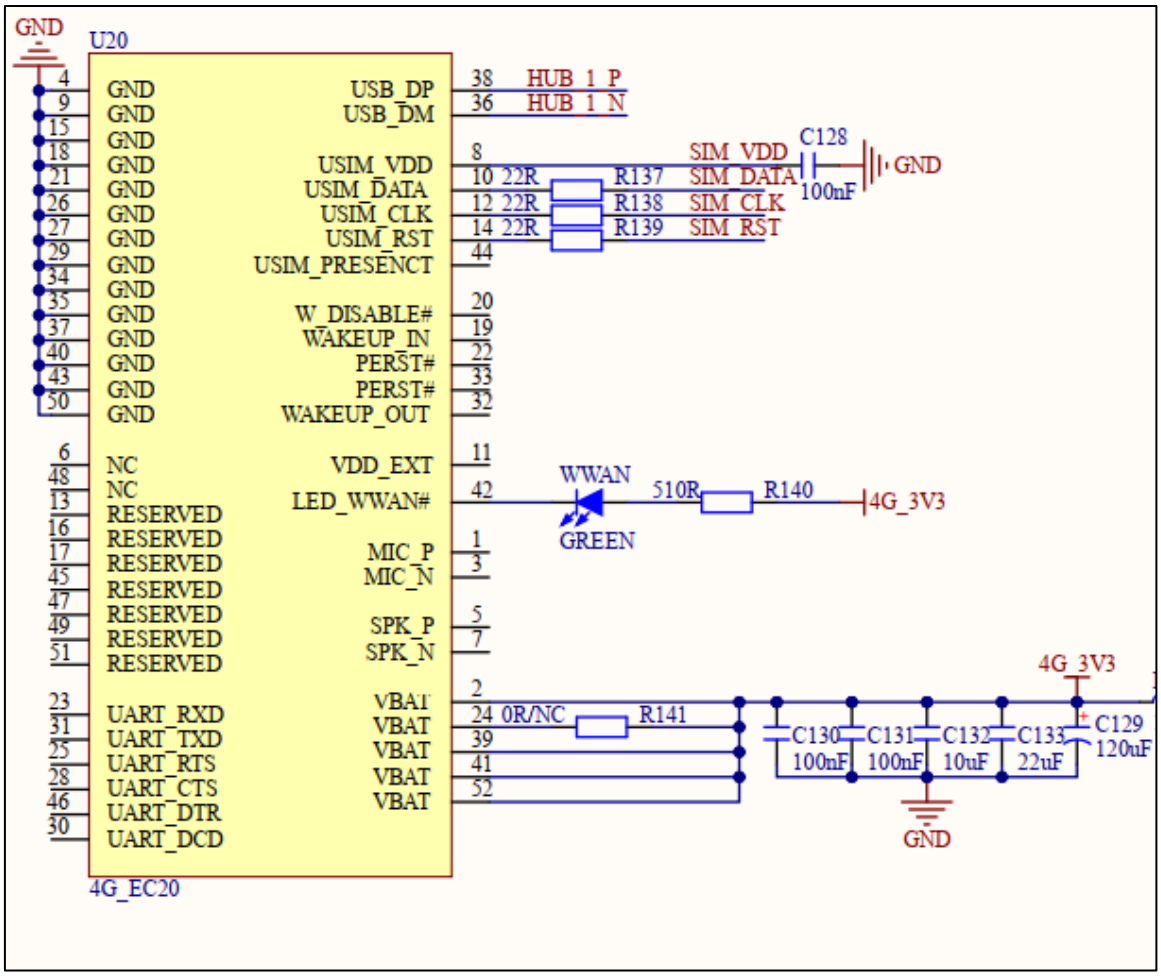

Figure 3.17-1 4G module interface circuit

3.18 Gigabit Ethernet interface

The development board is equipped with 1 Gigabit Ethernet interface (RJ45), which is adaptive to 10/100/1000M network speeds. The schematic diagram is shown as follows:

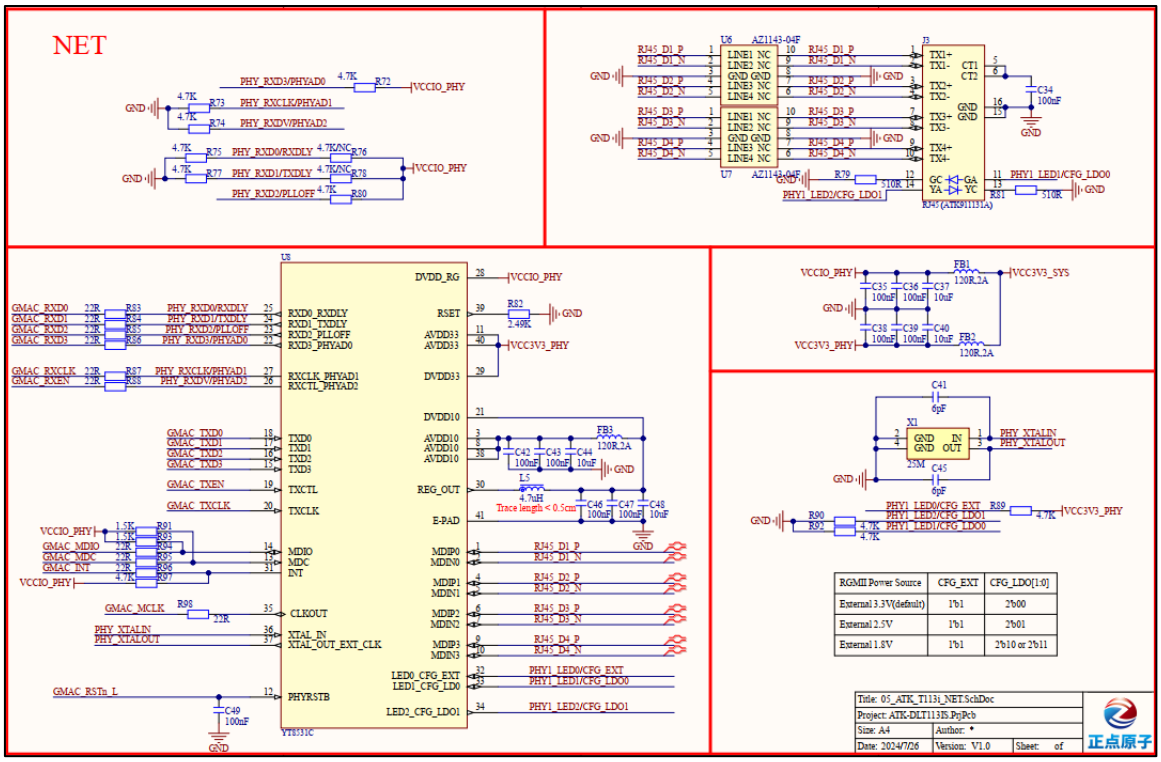

Figure 3.18-1 Gigabit Ethernet interface circuit diagram

When designing the base board by yourself, please pay attention to the following points:

1. The RGMII IO level is 3.3V. The PHY chip end needs to set the interface level to 3.3V;

2. PCB Layout should try to place the PHY close to the core board, and ensure the integrity of the RGMII signal reference plane. It is necessary to ensure the integrity of the peripheral power reference plane of the PHY chip;

3. Equal length requirement: The receiving and transmitting of RGMII can be of equal length. The equal length requirement is ≤ 2.5mm;

4. Impedance requirement: Single-ended 50 ohms;

Note: The measured speed is 710 Mb/s to 750 Mb/s

3.19 Audio interface

The development board is equipped with two LINEOUT outputs, two MIC recording channels, one LINE IN input, one FMIN input, one headphone interface, and the schematic diagram is shown in the following figure. In the figure, HT6872 is a single-channel D-class audio power amplifier. The audio from the LINEOUT output is amplified by the power amplifier chip and then played through the speaker. SPK- and SPK+ are connected to a built-in 8Ω 1W small speaker. There are two options for the microphone: one is the MIC built into the headphones, and the other is the built-in microphone. PHONE is a four-section 3.5mm headphone output interface that can be used to plug in headphones.

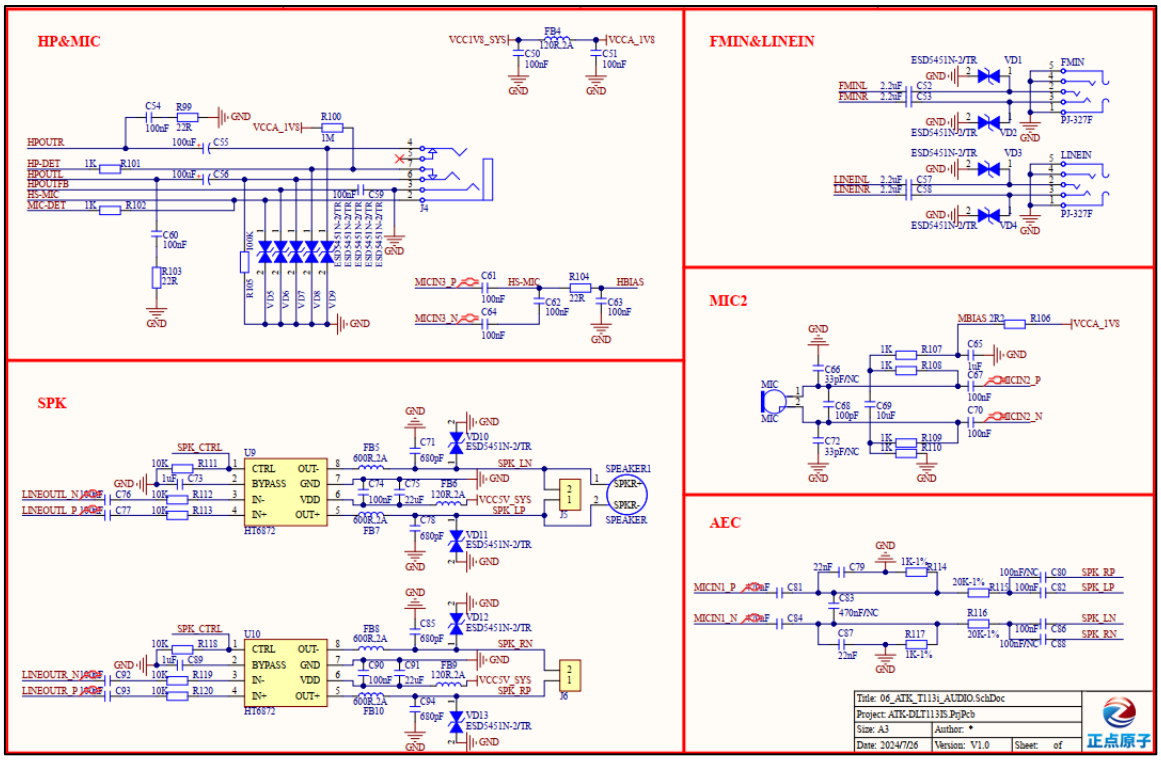

Figure 3.19-1 Audio interface circuit diagram

3.20 Power Supply Interface

The onboard power circuitry of the development board is designed as shown in the following figure. The development board uses a DC12V/1A power adapter as the power input. After the power is connected to the DC_IN port, it is converted by the SCT2230 chip to generate the VCC3V3_CORE voltage, which is used to power the core board. Once the VCC3V3_CORE voltage is successfully input to the core board, the core board immediately initiates the power-on process and outputs the PWR_ON signal. This signal activates the 3V3 and 5V power modules on the baseboard, namely, the U3 module will output the VCC5V_SYS voltage, while the U5 module will output the VCC3V3_SYS voltage. Subsequently, the VCC5V_SYS voltage is further converted by the U4 module to generate the VCC1V8_SYS voltage, providing 1.8V power supply to the baseboard. It is worth noting that the normal startup of the core board requires following specific power-on timing requirements. In terms of the power supply design of the baseboard, one can directly refer to the schematic diagram of the power section of the ATK-DLT113IS development board for planning.

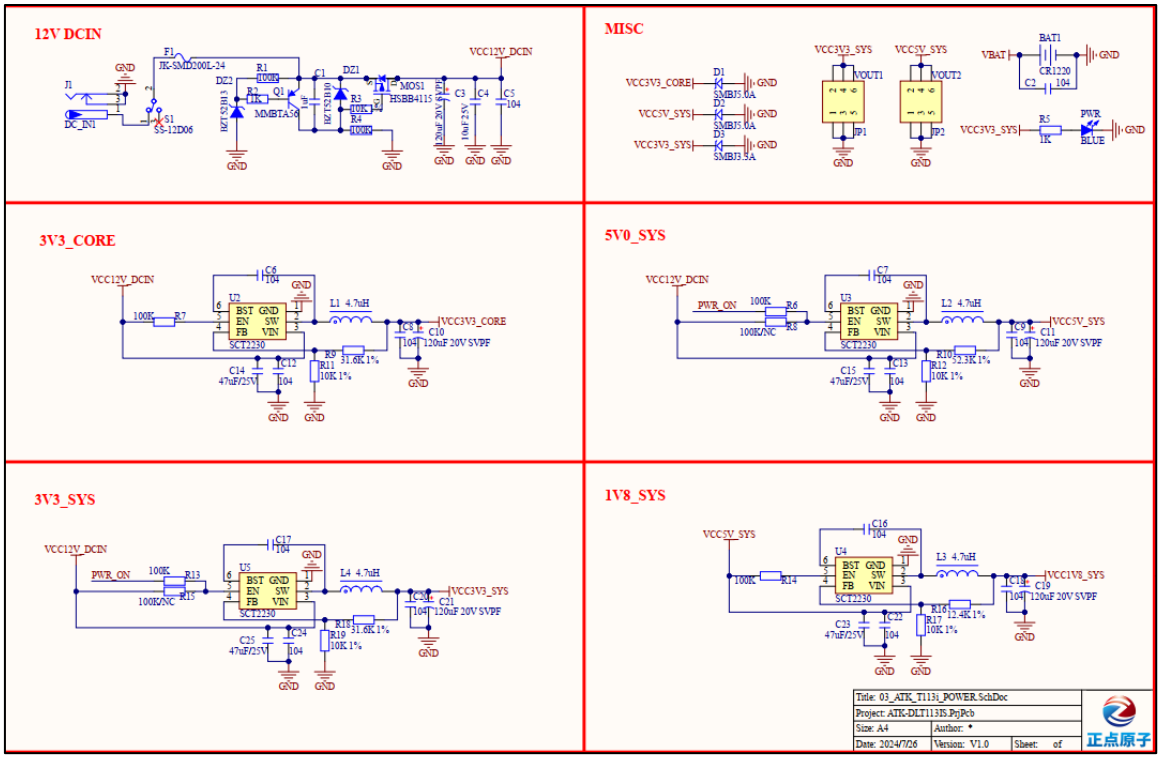

Figure 3.20-1 Power supply circuit diagram