Theory:

For a BJT to be used as an amplifier, DC bias is applied to fix I_C and V_{CE} at a constant I_B on the linear or active part of the characteristics. Biasing refers to the application of D.C. voltages to setup the operating point in such a way that undistorted output signal is provided during the operation. The DC bias point or operating point or quiescent point Q shown in Fig.1 has a direct impact on the maximum swing that can be obtained at the output.

Once selected properly, the Q point should not shift because of change of I_C due to

- β variation due to replacement of the transistor of same type
- Temperature variation

The reverse saturation current changes with temperature. Specifically, I_{CO} doubles for every 10^oC rise in temperature. The collector current I_C causes the collector junction temperature to rise, which in turn increases I_{CO}. As a result of this growth in I_{CO}, I_C will increase as $I_C = \beta I_B + (1+\beta) I_{CO}$ and will cause the operating point to shift. If the variation is small, it may at the most result in distortion which is not desired though. But if not stabilized, this may continue and the ratings of the transistors may get exceeded resulting in thermal runaway.

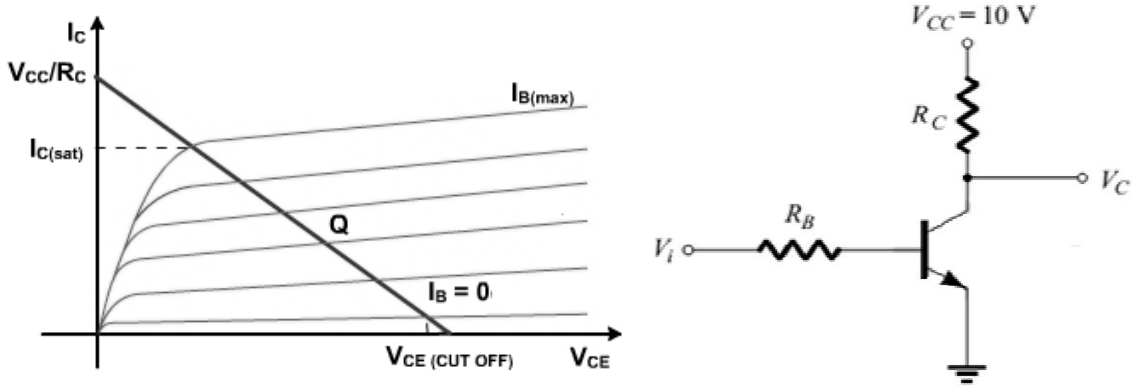
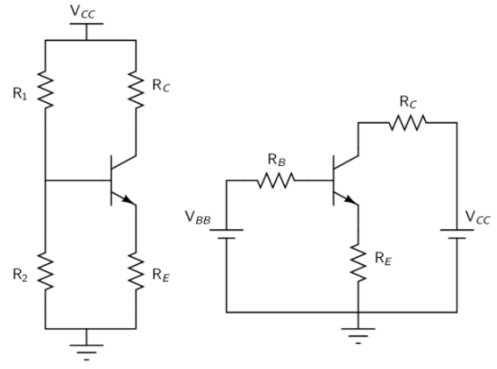


Figure 1 The DC load line and Q point (a) The amplifier circuit (b)

The most popular biasing circuit is potential divider biasing shown in Fig.2. A potential divider consisting of R_1 and R_2 (see Fig. 2a) is used to establish the desired DC bias voltage V_{BB} at the base.



(a) (b)

Figure 2 Potential divider biasing (a) and its Thevenin's equivalent circuit (b)

DC analysis:

1. Thevenin equivalent of base circuit gives,

   $V_{BB} = \frac{R_2}{R_1 + R_2} . V_{CC}$

2. $R_B = R_1 || R_2$
3. Applying KVL to base circuit loop and collector circuit loop we get,

   $V_{BB} = I_B . R_B + I_E . R_E + V_{BE}$

   $V_{CC} = I_C . R_C + V_{CE} + I_E . R_E$

   Solving we get,

   $I_E = \frac{(V_{BB} - 0.7)(\beta + 1)}{R_B + (\beta + 1) R_E}$ where, $V_{BE} = 0.7V$

- Since $V_{BB} >> V_{BE}$, small variations in V_{BE} can be swamped by V_{BB}.
  However, if V_{BB} is made too large, the voltage V_{CE} gets reduced and that limits the voltage swing. Hence as a rule of thumb while designing the biasing circuit;

  V_{BB}, V_{CE}, and $I_C R_C$ are chosen about $\frac{1}{3} V_{CC}$.

- $R_E >> \frac{R_B}{(\beta + 1)}$

If R_E is sufficiently large compared to R_B, any small variation in β does not affect I_E and hence I_C to a large extent. This is achieved by choosing small R_B. However, if R_B is made too small, the input resistance of the amplifier is reduced. Typically, current through the potential divider is chosen to be about $0.1 I_E$ to keep the current drain from power supply minimum.

Role of R_E: R_E provides negative DC feedback and stabilizes I_E and hence I_C. Any increase in I_E raises the emitter voltage V_E reducing base emitter forward bias. This reduces further increase in base current I_B and in turn I_C and hence I_E.

Design steps

If one wishes to design the bias network for an amplifier for given values of I_E and V_{CC}, following steps are to be followed.

1. Rule of thumb: $V_B = \frac{1}{3} V_{CC}$ (V_B voltage across R_2).
2. $V_E = V_B - 0.7$
3. $R_E = \frac{V_E}{I_E}$
4. Assuming negligible base current, current through $R_1 + R_2$,

   $I_1 = \frac{V_{CC}}{R_1 + R_2} = 0.1\ I_E$

   $R_1 + R_2 = \frac{V_{CC}}{0.1 I_E}$
5. $V_B = \frac{R_2}{R_1 + R_2} . V_{CC}$

   $R_2 = V_B \frac{(R_1 + R_2)}{V_{CC}}$
6. I_E to ensure the value of R_E.

   Obtain $I_E = \frac{(V_{BB} - 0.7)\ (\beta + 1)}{R_B + (\beta + 1) R_E}$

   There could be slight variation in this value of I_E from the nominal value. Adjust R_E to get close approximation to nominal value of I_E.
7. $I_C = (\frac{\beta}{1+\beta} . I_E)$

   $V_C = \frac{2}{3} V_{CC}$

   $R_C = \frac{V_{CC} - V_C}{I_C}$