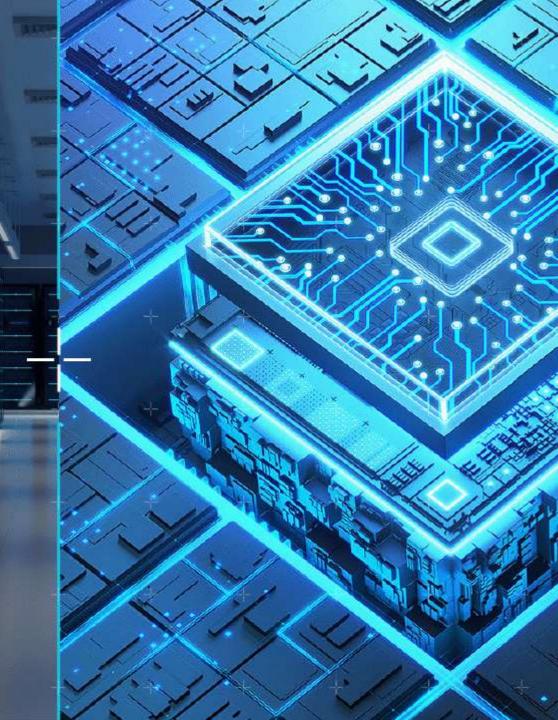
Open-Source SW Ecosystem on Arm for Infrastructure

openEuler Arm SIG Meetup

Jun He 21-Jun-2024



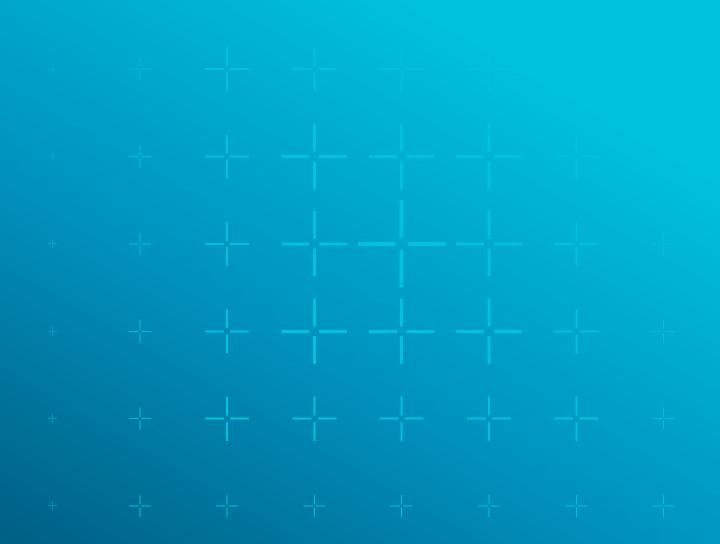


Agenda

- + Overview
- + Foundation OSS projects
- + Infrastructure Workloads & Solutions
- + Developer Ecosystem



Overview



Arm Neoverse Software Ecosystem

1000s of OSS

Native Build Projects

100+ ISVs

Commercial Support

200K+ Docker

Hub Images

1M+CI/CD

Build Minutes/Month

PERFORMANCE



Scalable Neoverse CPU Cores

EFFICIENCY



Best \$/throughput in the industry

PLATFORM DIVERSITY



Widest possible choice of Platforms

OPTIMIZATION



Purpose built use cases



Participation in Consortia and Initiatives

Collaborate with partners and ecosystem

- Open Source and standardization initiatives (SPDX, OpenChain)
- Cloud Native ecosystem (CNCF)
- Networking and 5G initiatives (O-RAN)
- Contribute to developing reference software implementations
- Confidential computing and security
- Software-defined infrastructure and datacenter management























Arm Contributing to 100+ Infra related Open-Source Projects

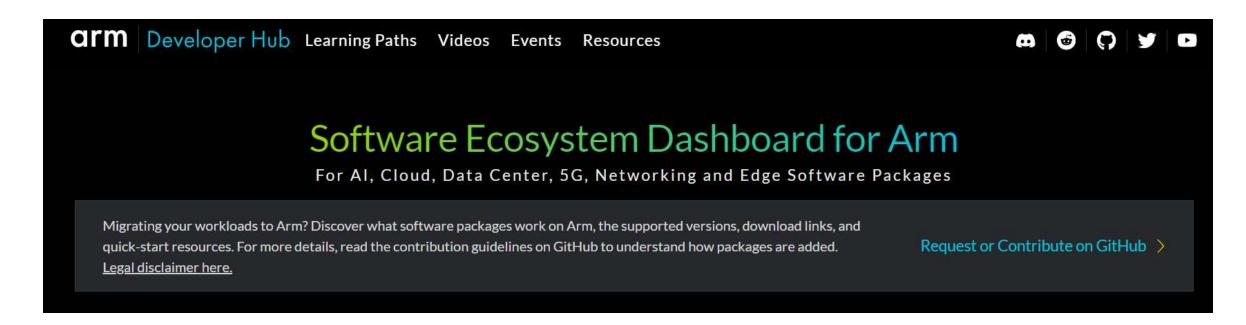
Enabling a Frictionless Cloud-Native Developer Experience





Software Ecosystem Dashboard

+ A centralized information hub for global Arm infra software developers and users



https://www.arm.com/developer-hub/ecosystem-dashboard/servers-and-cloud-computing/



Foundation OSS Projects



Linux Kernel

- → v3.7
 - The first mainline Kernel supporting Arm64
- - The first SLTS release with Arm64 support
- → V6.6
 - The latest LTS kernel with the projected EOL in Dec 2026
 - **⊹**V6.9
 - The latest stable kernel released in May 2024

Kernel	Arm feature
6.5	Arm v8.8: Feat_MOPS/memcpy HWCAP and user space support Arm 8.9: Feat_PIE Stage 1 support Consolidate all arm specific initialisation into acpi_arm_init() KVM: Force 63bit counters for M2 CPUs, initialize HCRX_EL2 switch HCRX_EL2 between host and guest
6.1	Arm v8.6 ECV vDSO support Arm 8.9 HWCAP support: Range Prefetch and Scalar Integer Instructions Arm 9.2 SME 1.0: ptrace support KVM: Fixes for single-stepping in the presence of async exception, and fix for SME trapping in VHE configuration
5.15	Arm 8.4 MPAM public snapshot Arm 8.5 MTE: optimisations for kernel entry/exit path Refactoring support for VirtIO transport for SCMI init/exit calls hyperV support and KVM improvements
5.10	Armv8.5 MTE: User-space heap tagging enablement Arm v 8.6 PAC2 +FPAC in-kernel enablement SMMU support for ASID spinning, SCMI system protocol support NUMA Kconfig: maximum number of NUMA nodes bumped from 4 to 16 [node-shift: 4] Perf PMU drivers: addition of the Arm CMN-600 PMU porter driver, support to handle CPU PMU IRQs as NMI
4.19	Support for qspinlock on arm64 GICv3 updates and LPI allocation refactoring GCC "stackleak" plugin Support for chained PMU counters KVM: Support for Group0 interrupts in guests



Compilers

GCC

GCC	Key Arm feature enabled
GCC 13	Arm Neoverse V2 support Armv9.1-a/9.2-a/9.3-a architectures support LRCPC support through +rcpc extension Common Short Sequence Compression instructions (CSSC) support through the +cssc extension LSE2 support
GCC 12	Support ShadowCallStack sanitizer currently only for AArch64 target Cortex-A710 support with new cpu flag The 64-byte atomic load/store intrinsics support through +ls64 Optimized the ACLE Advanced SIMD intrinsics
GCC 11	Support Linux Kernel Concurrency Sanitizer (KCSAN) Arm Neoverse N2, V1 support with new cpu flag Improve inlined memcpy and memset Support conditional selects to perform conditional stores AArch64 intrinsics code-gen improvement Support the full set of intrinsics defined by ACLE Q3 2020
GCC 10	Full support for SVE/SVE2 AArch64 BFloat16 instructions (BF16) Matrix Multiplier Extension (I8MM, F32MM, F64MM) Floating-point to integer instructions (FRINTTS) Transactional Memory Extension (TME of Armv9) MTE and RNG through ACLE intrinsics A new option to determine if LSE can be used at runtime

GCC	Key Arm feature enabled
GCC 9	Arm Neoverse N1 support Armv8.5-a architecture support Statistical Profiling Extensions (SPE) only at assembler level Random number instructions (RNG) only at assembler level Complex number SIMD extension (FCMA, >= armv8.3-a) Memory Tagging Extension (MTE, >= armv8.5-a) Branch Target Indicators (BTI) Execution and Data and Prediction instructions (SPECRES) Speculation Barrier instruction (SB) Speculative Store Bypass Safe (SSBS) New -mbranch-protection option for PAuth as well as BTI Stack clash protection support
GCC 8	Armv8.4-a architecture support Rounding Double Multiply Accumulate instructions (RDM) Weak release consistency extension (LRCPC) Dot Product extension (DotProd) AES/SHA2/SHA3/SHA512 cryptographic extension SM3/SM4 cryptographic extension Floating Point Multiplication instructions (FHM) on Armv8.2-a and above

More details:

https://developer.arm.com/Tools%20and%20Software/GNU%20Toolchain #Supported-Devices



Compilers

LLVM

LLVM	Key Arm feature enabled					
LLVM 17	Added Assembly Support for FEAT_GCS (Guarded Control Stacks), FEAT_CHK (Check Feature Status), and FEAT_ATS1A. Support for preserve_all calling convention is added. Added support for missing arch extensions in the assembly directives .arch <level>+<ext> and .arch_extension.</ext></level>					
LLVM 16	Added support for the Cortex-A715/Cortex-X3/Neoverse V2 CPU. Added support for assembly for RME MEC (Memory Encryption Contexts). Added codegen support for the Armv8.3 Complex Number extension. Implemented Function Multi Versioning in accordance with Arm C Language Extensions specification.					
LLVM 14	Added support for the Armv9-A, Armv9.1-A and Armv9.2-A architectures. The compiler now recognises the "tune-cpu" function attribute to support the use of the -mtune frontend flag Auto-vectorization now targets SVE by default when available.					
LLVM 13	Introduced assembly support for Armv9-A's Realm Management Extension (RME) and Scalable Matrix Extension (SME). Produce proper cross-section relative relocations on COFF Fixed the calling convention on Windows for variadic functions involving floats in the fixed arguments					

LLVM	Key Arm feature enabled
LLVM 12	Native 64-bit Arm LLVM toolchain for Windows-on-Arm Add some specific CPU flags for Neoverse V1 & Neoverse N2, Cortex-A78C, Cortex-R82, Fujitsu A64FX Support a new flag '-moutline-atomics' for LSE dynamically detection Add vector-length specific ACLE support(SVE/SVE2) SVE/SVE2 (VLS intrinsics) Experimental vector-length-agnostic (VLA) auto-vectorization
LLVM 11	SVE/SVE2 (VLA intrinsics) Bfloat16 (intrinsics) Matrix Multiplication Extension (intrinsics)
LLVM 10	Transactional Memory Extension (TME) (asm/disasm, intrinsics)
LLVM 9	Memory Tagging Extension (MTE) Branch Target Indicators (BTI) SVE2 (asm/disasm)
LLVM 8	Pointer Authentication (PAuth)

More details:

https://developer.arm.com/Tools%20and%20Software/LLVM%20Toolchai n#Supported-Devices



C/C++/Fortran toolchain for Neoverse Platforms

		I	I	I	I.
Neoverse IP Platform	NI/VI	VI/N2	VI/N2	N2/V2	Poseidon and future cores
	GCC10	GCC11	GCC12	GCC13	GCC-next
GNU Toolchain (GCC, Glibc, and GDB)	+10% SpecInt17Arm v8.6-v9.0SVE2 support	SVE2 improvementsV1 and N2 support	 Armv8.8-v9.3 SVE2 code-gen +% Intrinsic perf +% Auto-vec at -O2 	Armv8.9-v9.4SVE2 code-gen +%	 Architecture enablement Vectorized math routines SVE2 code-gen +% and libraries Workload specific tuning
	LLVM 10/11	LLVM 11/12	LLVM 13/14	LLVM 15/16	LLVM-Next
LLVM Toolchain (Clang, LLDB)	Armv8.6-v9.0SVE asmN1 support	 Armv8.7-v9.1 +2-5% SpecInt17 V1 and N2 support 	 Armv8.8-v9.3 +3% SpecInt17 SVE2 auto- vectorization 	 Armv8.9-v9.4 SVE2 core scheduling model Complex number auto-vec 	 Architecture enablement SPEC INT CPU +% SVE2 code-gen +% New LLVM Fortran Frontend LLVM backend +% to benefit other languages
Arm Compiler	20.x	21.x	22.x	23.x	Version-Next
for Linux (for HPC users) (Arm Compiler + Arm Perf Libraries)	+5% to 46% for HPC workloads • SVE2 support • Sparse matrix libraries	SVE/2 improvementsLLVM 11 based	 V1 support SVE/2 improvements LLVM 13 based compilers BLAS/LAPACK improvements 	 Demeter support LLVM 16 based compilers ArmPL Batched/Sparse functions 	 Demeter +% for HPC workloads New LLVM Fortran frontend-based compiler SVE/2 improvements
	2020	2021	2022	2023	2024 onwards

^{*} All % perf numbers are based on best possible flags and are relative to the previous compiler version



Runtime Languages

Java

AArch64 support since JDK8 AArch64 intrinsics improved in JDK11 Windows/MacOS support since JDK17 VectorAPI with NEON and SVE support Foreign function & Memory API contribution Optimized ZGC performance Multiple downstream forks

Python

First AArch64 commit in 2012 PyPy AArch64 support in 2019 PEP-599/600 accepted https://speed.python.org/

.NFT



NFON intrinsics added in v5 LSE atomics improved in v7 **Conditional Ops** improvement Consecutive register allocation support in v8

Rust

NFON intrinsics was stabilized in 2021 RFC for SVE support is in discussion

PHP

PHP8.1 released – fully enabled on AArch64 PHP-JIT CI and bug fixes

Open**JDK**

Golang

Arm64 support since 1.8.5/1.9 Memory sanitizer support in 1.11 Stack frame pointers support on all OSs Optimized function arguments passing in 1.17 Address sanitizer support in 1.18 PGO support since 1.21





Major Operating Systems Available on Arm



RHEL 9.4 released in April 2024

RHEL 8.10 released in May 2024

Fedora 40 released in April 2024

CentOS 7.1 AltArch is the first release with Arm64 support



SLES 15 SP5 for Arm64 released in June 2023

openSUSE Leap 15.5 released in June 2023 and 15.6 will be available in June 2024

openSUSE **Tumbleweed** available on Arm64



Debian 12.5 for Arm64 released in February 2024

Debian 11.9 released in February 2024

Debian 8 is the first release with Arm64 support

ubuntu®

Ubuntu 24.04 for Arm64 released in April 2024

Ubuntu 16.04 is the first release with Arm64 support



Latest openEuler 24.03 released in June 2024

openEuler 20.03 LTS released in Mar 2020 with full Arm64 support

Arm joined openEuler community in 2020

OpenAnolis

Latest OpenAnolis 23.1 released in June 2024

Anolis OS 8.4 released in July 2021 with full Arm64 support

Arm joined **OpenAnolis** community in 2021



Infrastructure Workloads & Solutions

Database







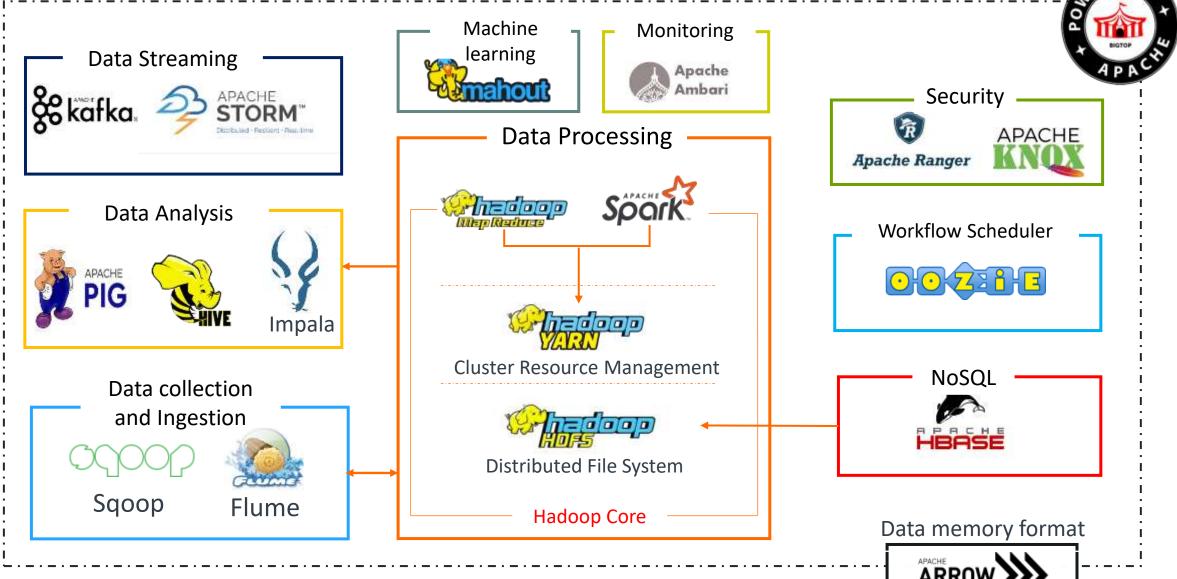




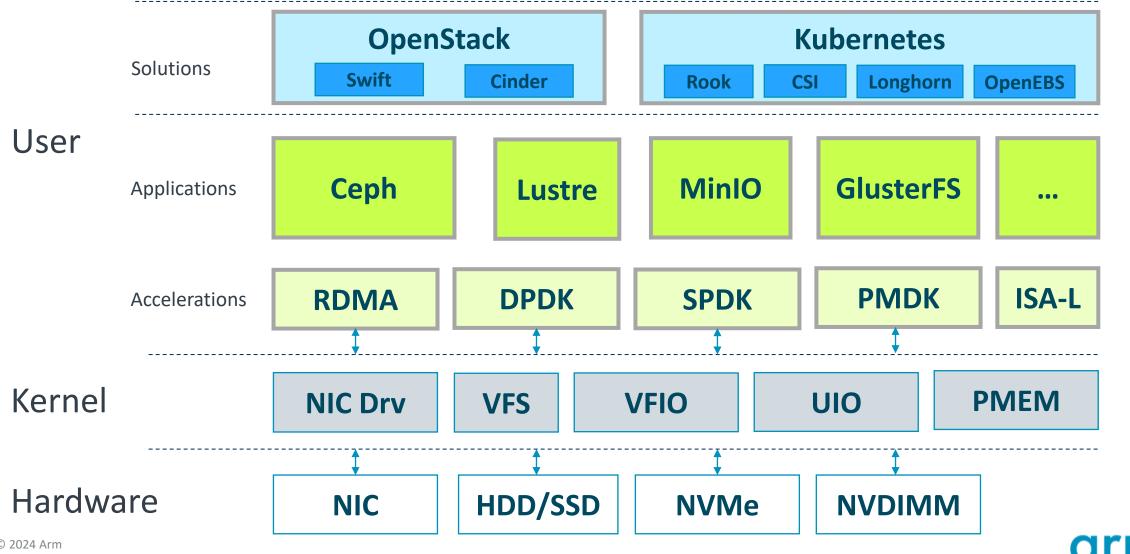




Big Data



Storage



Networking

Networking Application CNI, Service Mesh Snort VectorScan Userspace **IPSec** uBPF Crypto FD.io/VPP OVS Libraries (OpenSS **DPDK** ODP Kernel eBPF XDP **VX LAN IPIP**

Orchestration, Management & Control software

Datapath

Infrastructure

CPU, DPU, SoC, GPU, FPGA, ASIC, SmartNIC, ...





















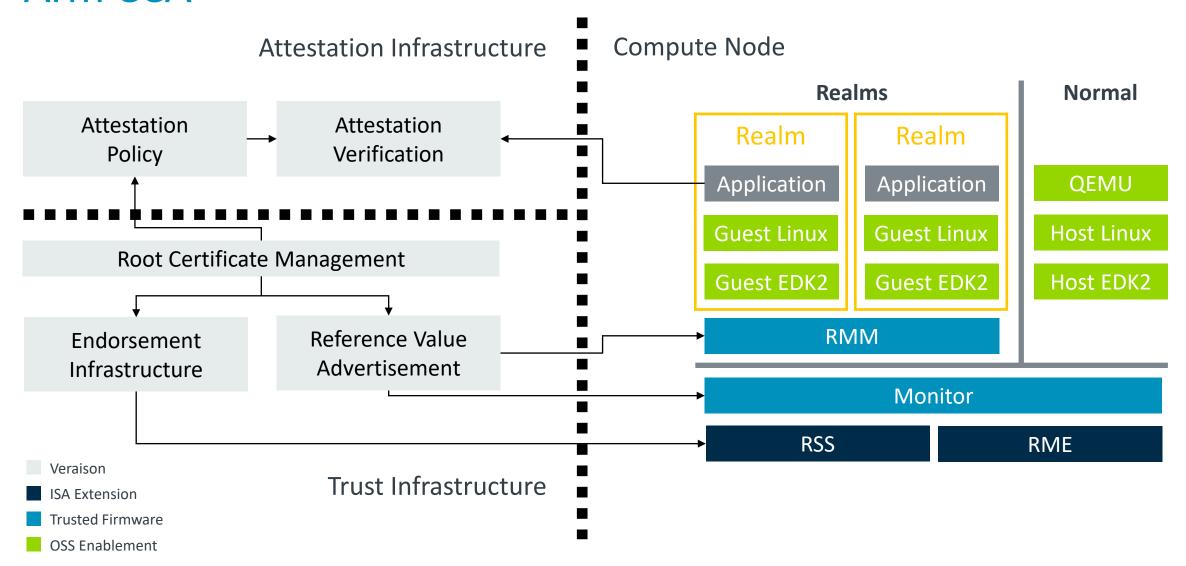






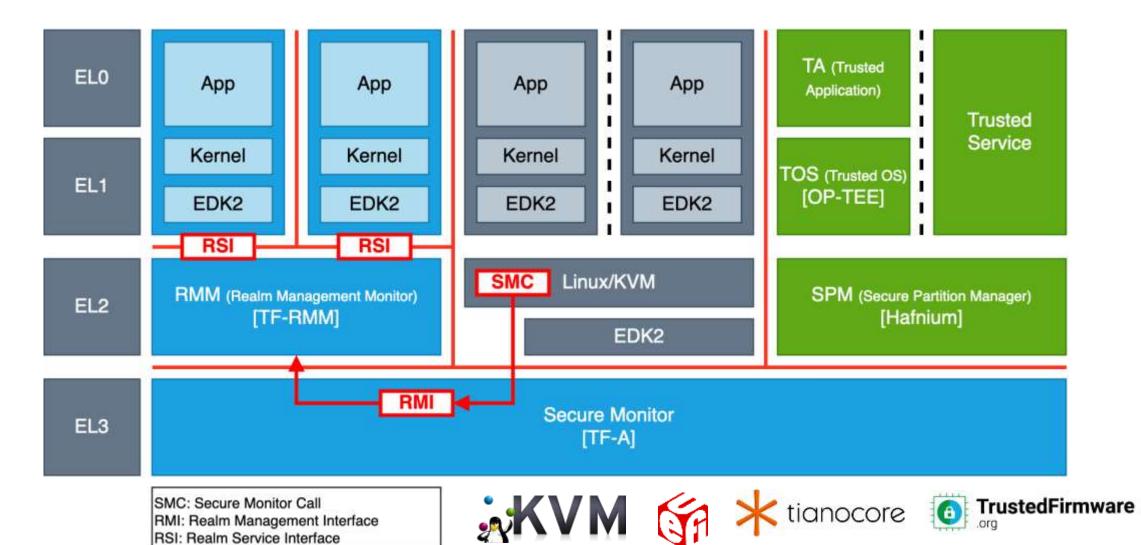


Arm CCA





Arm CCA - Open Source Components





ML Software Stack on Arm Neoverse

Open Source

Accelerator Vendor

nVidia

Arm



Models

Large Language Models

Generative Al

Vision

NLP

Recommender

Frameworks / Runtimes

TensorRT









llama.cpp, gemma.cpp

Libraries / Backends

CUDA

Custom

Accelerated

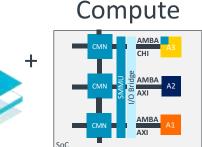
Arm Compute Library (ACL) (via oneDNN in some cases)

KleidiAl

XLA/MLIR

Hardware

Neoverse Host



Neoverse On-CPU ML



NEON

SDOT

FP16

BF16

SVE

SME



Developer Ecosystem



Developer Ecosystem

Enabling a Frictionless Developer Experience

Global

- + Learning Paths
- + Arm Community
- + Arm Developer Program
- → Arm Software on GitHub
- + Arm repositories on DockerHub
- → AWS Graviton Getting Started
- → Oracle Landing page
- + Ampere Solutions
- ___

China



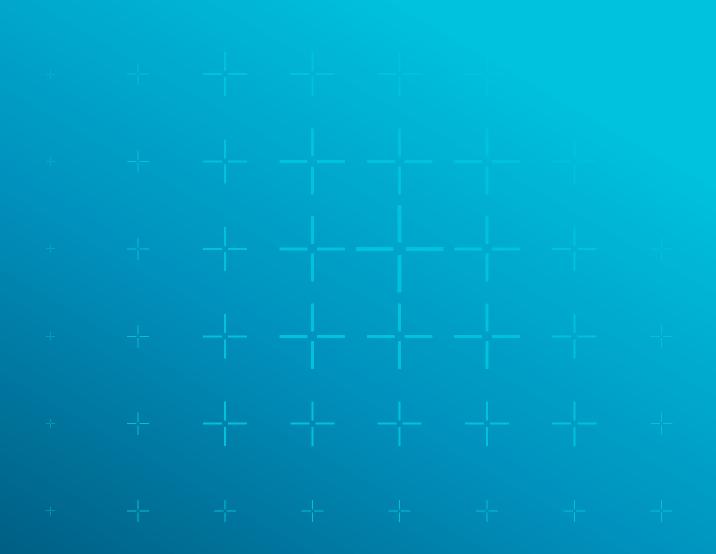
→ "Arm Community" on WeChat



- + Ali Yitian Developer Community



Q & A





Thank You Danke Gracias Grazie 谢谢 ありがとう **Asante** Merci 감사합니다 धन्यवाद

Kiitos

شکرًا

ধন্যবাদ

תודה ధన్యవాదములు

