在RISC-V国际基金会和RISE基金会的工作日常

吴 伟

openEuler ROS & RISC-V Maintainer

2024-4-27

报告人介绍

- 吴伟（Dropout, not Ph.D.）
  - PLCT Lab 创始人及项目总监(2019-)：聚焦 编译器、虚拟机、模拟器 等基础软件
  - TARSIER 团队创始人(2021-2023)：推动所有开源软件将 RISC-V 接纳为 Tier-1 支持
  - **甲辰计划**主理人(2024-)：用一纪的时间，在所有基础关键领域完成面向RISC-V的适配与优化
  - 隶属于中国科学院软件研究所智能软件研究中心

跟RISC-V和开源社区有关的经历和角色

- **RISC-V 国际基金会（RVI）技术委员会(TSC)委员**、ISA基础架构委员会主席等
- **RVI 中国区联络人、RISC-V大使**、RISC-V中国峰会 核心组织者
- RISE基金会TSC成员、CHIPS Alliance 基金会董事
- RISC-V中国社区(CNRV) 核心组织者
- LLVM基金会理事(2022-)
- HelloGCC社区负责人、HelloLLVM社区创始人

本报告内容不代表 ISCAS、LLVM 基金会或 RISC-V 国际基金会观点

PLCT实验室（隶属于中国科学院软件研究所智能软件研究中心）

基础软件领域的国家队，为国内企业提供「开源软件公共品」

- 致力编译工具链、模拟器等开源基础软件开发，在上游社区做贡献

- 积极开展国际开源社区/组织合作，共同筑建RISC-V开放生态

Technical

Specifications

The RISC-V instruction set architecture (ISA) and related specifications are developed, ratified and maintained by RISC-V International contributing members within the RISC-V International Technical Working Groups. Work on the specification is performed on GitHub, and the GitHub issue mechanism can be used to provide input into the specification.

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Join RISC-V International

RISC-V Board of Directors: Officers

Lu Dai
Board Chair, Premier

Senior Director of Technical Standards, Qualcomm

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David Patterson
Vice Chair, Premier

Distinguished Engineer, RIOS Laboratory

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Ted Speers
Secretary, Strategic Representative

Technical Fellow, Microchip

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Xiaoning Qi
Treasurer, Premier

Vice President, Alibaba Group

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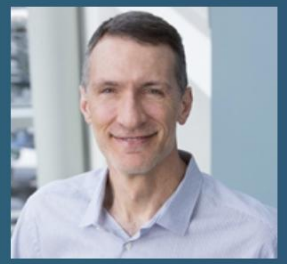
RISC-V Technical Steering Committee: Officers



Greg Favor
TSC Chair

Co-Founder and CTO, Ventana Micro Systems

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Philipp Tomsich
TSC Vice-Chair

Chief Technologist & Founder, VRULL GmbH

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Membership

Welcome to the Open Era of Computing!

RISC-V International is a non-profit organization supporting the open RISC instruction set architecture and extensions. We enable open community collaboration, technology advancements in the RISC-V ecosystem, and visibility of RISC-V successes.

Join us and see how open technical collaboration along with the support of many RISC-V programs can accelerate your business.

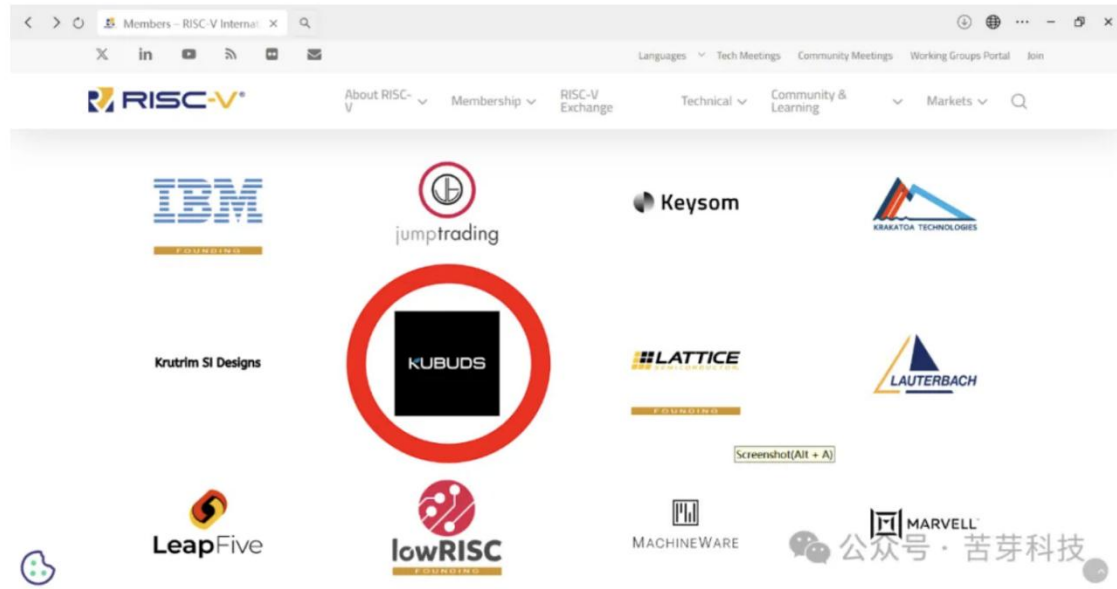
What Membership level is right for me?

Organization: Premier members have a seat on the Board of Directors, the Technical Steering Committee, and enhanced communications coverage via RISC-V content and social.

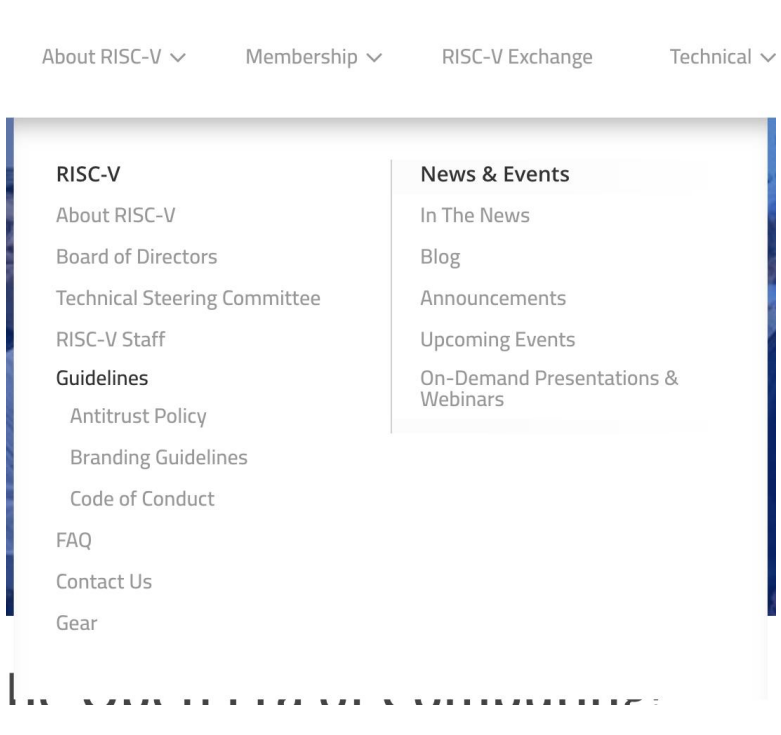
苦芽科技正式加入 RISC-V 国际基金会，共筑开放芯片生态

苦芽 苦芽科技 2024-04-25 12:44 浙江

苦芽科技正式加入 RISC-V International，成为 Strategic Membership。这一举动标志着苦芽科技在开放芯片生态领域迈出了重要的一步。



RISC-V International（RISC-V 国际基金会）是一个致力于推动 RISC-V 指令集架构发展的全球性非营利组织。通过开放式协作的方式，聚集不同公司、行业和地域的参与者，共同推动 RISC-V 生态系统的繁荣发展。加入 RISC-V 国际基金会，意味着苦芽科技将更深入地参与到 RISC-V 技术的研发、推广和应用中，与全球同行共同推动 RISC-V 技术的创新和发展。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In The News
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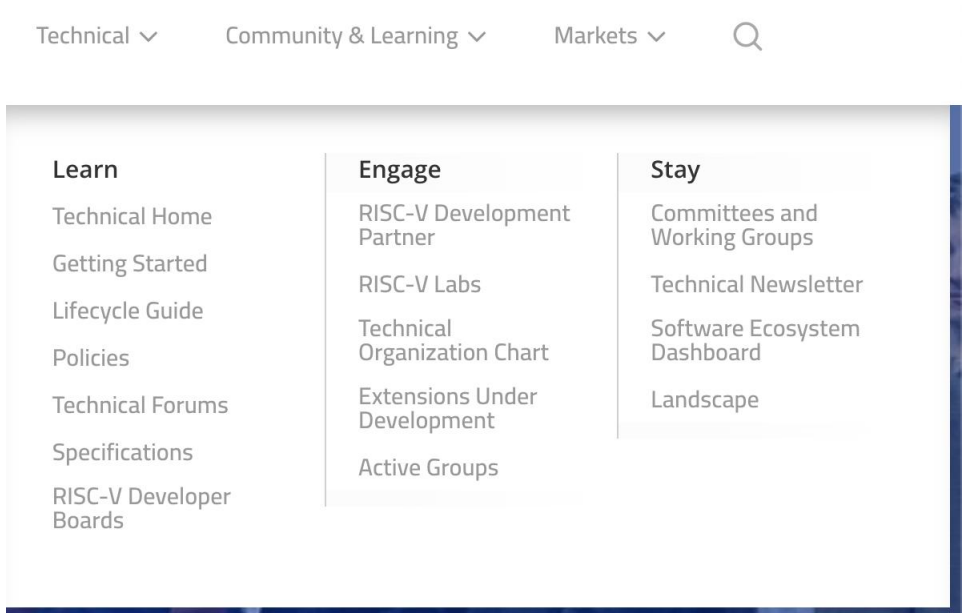
Technical
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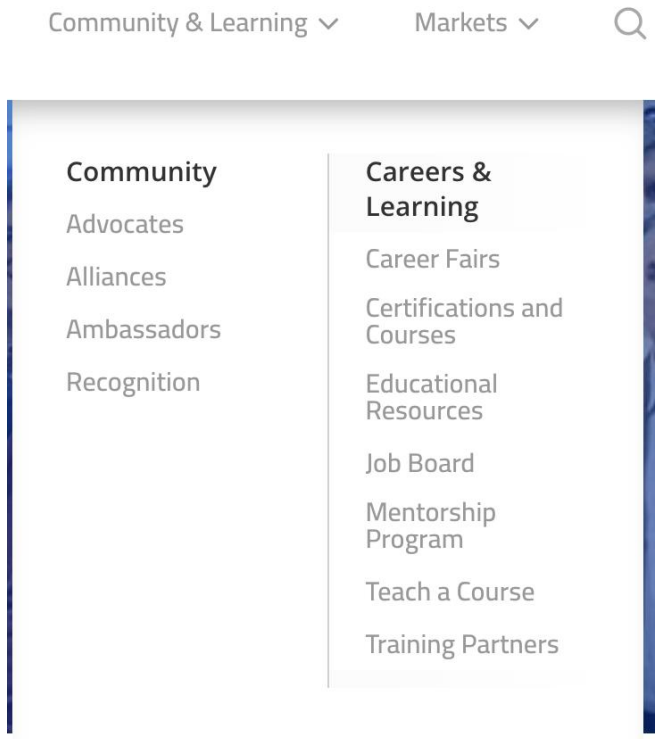
Landscape


Community & Learning
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Educational Resources
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Teach a Course
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RISC-V Advocate：年轻人的第一个国际身份

喜讯丨祝贺陈逸轩完成RISC-V国际基金会 RISC-V Advocate 首批认证：全球共4位、唯一女性代表、唯一东亚代表

Original YXChen的后援团 RUYISDK 2024-03-17 18:14 北京

围观地址：https://riscv.org/risc-v-advocates/

RISC-V® ADVOCATE

公众号 · RUYISDK

Yixuan Chen

Expertise: linux, compiler and open-source enthusiast,

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围观地址：https://riscv.org/risc-v-advocates/

Certification Steering Committee

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RISC-V International

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- Extension Naming Convention

RISC-V® Pages

Certification Steering Committee

Created by Rafael Sene, last modified by James Ball on Apr 25, 2024

Welcome to the RISC-V CSC Wiki Home Page!

Use this page to find the most recent links to CSC content.

Bookmark this Wiki page. Do *not* bookmark the links below since they are subject to change without notice.

CSC Links:

CSC Charter

- Find this under Administrative folder under CSC files link above
- v0.4 approved by BoD in their March 28, 2024 meeting

CSC Operating Guidelines (Draft)

- Find this under Administrative folder under CSC files link above

CSC Email List

- Uses RVI groups.io facility

CSC Document Repository

- Presentations, minutes, administrative, etc.
- Currently using Google Drive

CSC Meeting Recordings

- Contains links to Zoom recordings

CSC Work Groups:

- Industry Survey documents
- ACT Assessment documents
- Sail Assessment documents

CSC GitHub

- CSC has its own GitHub "organization" with one or more "repositories"
- Other RVI GitHub "organizations"
- Add people for GitHub access - Need permissions or you'll get a 404 error.

CSC Voting Rights

CSC-related Links:

ACT (Architectural Compliance Tests)

- ACT SIG - Oversees development of ACT
- ACT GitHub
- Test format specification
- ACT Tutorial (YouTube), Neel Gala & Pawan Kumar, NA Summit 2022

Sail

- Sail Language Documentation
- Formal ISA Language Selection Committee (2019)
- RVI Sail Survey Results (Jan 2024)
- Sail Tutorial by Bill McSpadden (NA Summit 2022, YouTube, 1hr)
- RISC-V Sail GitHub

Development Partners

- Volunteers from companies, universities, and research organizations reducing RISC-V's backlog of tests and test infrastructure.
- Tracked in GitHub (All activity, Activity by state)

Compatibility Test Framework

- Compares signature between two models and selects tests according to the model configuration
  - RISCOF (RISC-V Architectural Compatibility Test Framework) GitHub, Documentation
- Uses the RISCV-CONFIG tool to select and configure tests to match implementation choices
  - Test Framework Configuration Tool (RISCV-CONFIG) - GitHub, Documentation

RISC-V Branding Guidelines

Space tools

RISC-V Technical Meetings

Today | April 2024 | Week | Month | Agenda

Sun	Mon	Tue	Wed	Thu	Fri	Sat
31	Apr 1 10pm sig-datacenter@lists.risc 10pm tech-golden-model meet 11pm RISC-V Fast Interrupt TG 11pm RV Vector SIG 11pm RISC-V Performance Moc	2 12am RISC-V Performance Moc 10pm RISC-V Development Par 10pm RISC-V TC SIG (even WV 10:30pm RISC-V CHERI SIG an +3 more	3 12am [RISC-V] [sig-safety] Fu 1am DTPM SIG/E-Trace Encap 1:30am SoC Infra. HC monthly 6pm RISC-V AI/ML SIG 10pm Hold: RISC-V CCM	4 8pm RISC-V Dev Boards Meeti 10pm RISC-V RPMI TG Meeting 11pm RISC-V Perf Analysis SIG 11pm RISC-V Scalar Efficiency 11pm RISC_V - AI/ML Applicati	5 1am RISC-V Cryptographic Ext	6
7	8 2pm Unified Discovery Biweekl 10pm tech-golden-model meet 10pm Attached Matrix TG 11pm RISC-V IME TG +2 more	9 12am RISC-V Performance Moc 11pm RISC-V external debug s	10 12am Server SoC. TG 12:30am Runtime Integrity SIG 1am RISC-V TC SIG (odd WW) 1:30am RISC-V Security HC (oc 10pm RISC-V Tech Chairs - Hol	11 4pm IOPMP biweekly 10pm RISC-V PRS TG bi weekly 10pm RISC-V: Graphics SIG 10pm Toolchains SIG Bi-Weekly	12 12am Android SIG Meeting 12am J Extension Meeting 1am RISC-V Cryptographic Ext 10:30pm SIG SoftCPU Bi-Weekl	13
14	15 10pm sig-datacenter@lists.risc 10pm tech-golden-model meet 10pm Floating Point SIG meeti 11pm RISC-V Fast Interrupt TG 11pm RV Vector SIG	16 12am RISC-V Performance Moc 10pm RISC-V Development Par 10:30pm RISC-V CHERI SIG an 11pm RISC-V Certification Stee 11pm RISC-V Town Hall - Comr	17 1am RISC-V Debug Task Group 6pm RISC-V AI/ML SIG 10pm RISC-V Technical Commi 11:30pm RISC-V Performance M	18 10pm RISC-V RPMI TG Meeting 10pm RISC-V SIG-HPC monthly 11pm RISC-V Dev Boards Meet 11pm RISC-V Scalar Efficiency	19 12am RV Profiles SIG 1am RISC-V Cryptographic Ext	20
21	22 2pm Unified Discovery Biweekl 10pm tech-golden-model meet 10pm Attached Matrix TG 11pm RISC-V IME TG +2 more	23 12am RISC-V Performance Moc 10:30pm RISC-V Labs 11:30pm RV SoC Infra. HC	24 12am Documentation SIG (Ten 10pm RISC-V Tech Chairs - Hol 11pm RISC-V Performance Moc	25 4pm IOPMP biweekly 10pm RISC-V PRS TG bi weekly 10pm RV Graphics SIG (biweek 10pm RV psABI TG 11pm RISC-V Performance Eve	26 12am J Extension Meeting 1am RISC-V Cryptographic Ext 9am RISC-V CSC Task Force M 10:30pm RV SoftCPU SIG (bi-w	27
28	29 10pm sig-datacenter@lists.risc 10pm tech-golden-model meet 11pm RISC-V Fast Interrupt TG 11pm RV Vector SIG	30 12am Hypervisors SIG Monthly 12am RISC-V Performance Moc 10pm RISC-V Development Par 10pm RISC-V TC SIG (even WV +4 more	May 1 12am Functional Safety SIG bi- 1am DTPM SIG/E-Trace Encap 6pm RISC-V AI/ML SIG 10pm Hold: RISC-V CCM 11pm RISC-V Performance Moc	2 8pm RISC-V Dev Boards Meeti 10pm RISC-V RPMI TG Meeting 11pm RISC-V Perf Analysis SIG 11pm RISC-V Scalar Efficiency 11pm RISC_V - AI/ML Applicati	3 12am RV Profiles SIG 1am RISC-V Cryptographic Ext 9am RISC-V CSC Task Force M	4

Events shown in time zone: China Standard Time - Shanghai

Google Calendar

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Subgroups

ctrl + **shift** + **?** for shortcuts

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RISC-V main group main@lists.riscv.org

RISC-V Working Groups Portal

Welcome to the RISC-V Working Groups mailing list portal. RISC-V International is an open standard non-profit organization managing the IP and development activities for the RISC-V Instruction Set Architecture (ISA), an open standard hardware initiative that is rapidly transforming the way microprocessors are made. The primary website for the RISC-V architecture is at https://riscv.org.

The mailing lists on this portal are moderated, members-only discussions related to the development of the RISC-V ISA. Technical discussion groups are visible in read-only form to everyone, while marketing and administrative groups are restricted to members only.

If you are not a member, you can view the archives using these steps:

1. Click Subgroups to the left
2. Choose a technical group to view
3. Click Messages to view the messages in that group

Posting to a mailing list requires membership in RISC-V. To learn more or to become a member of the RISC-V International community, please see https://riscv.org/membership-application.

Details on using this portal are at **https://riscv.org/community/working-with-the-member-portal/**

RISE基金会的诞生：RISC-V 全球社区的最新投入

RISE
RISC-V Software Ecosystem

Advancing commercial software ecosystem readiness

RISE (RISC-V Software Ecosystem

Mission

- Accelerate the development of open source software for RISC-V
- Raise the quality of RISC-V Platform implementations
- Push the RISC-V Software ecosystem forward and align ecosystem partners' efforts

Board Members

Google intel Qualcomm MEDIATEK ANDES TECHNOLOGY T-HEAD Red Hat
Rivos SiFive VENTANA SAMSUNG NVIDIA Imagination

RISE

Focus Areas

Coordination and collaboration among the RISE members is across an array of software areas to deliver high quality and high performance implementations for RISC-V.

Compilers & Toolchains	LLVM, GCC
System Libraries	Glibc, OpenSSL, OpenBLAS, LAPACK, OneDAL, Jemalloc
Kernel & Virtualization	Linux, Android
Language Runtimes	Python, OpenJDK/Java, V8
Linux Distro Integration	Ubuntu, Debian, RHEL, Fedora, Alpine
Debug & Profiling Tools	Performance profiles, DynamoRIO, Valgrind
Simulator/Emulators	QEMU, SPIKE
System Software	UEFI, ACPI

RISE

https://riseproject.dev/wp-content/uploads/sites/25/2023/05/RISE-Overview-1.pdf

RISE Home

Pages

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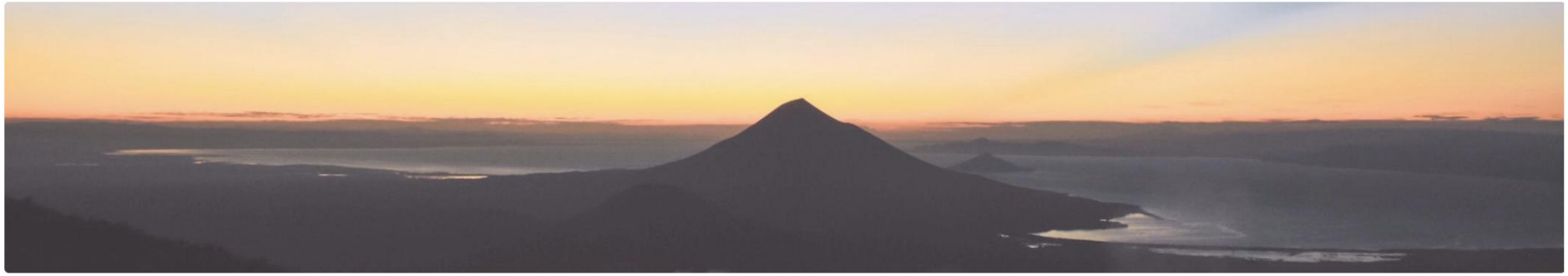
- About RISE
- RISE Governing Board
- RISE Technical Steering Committe
- RISE Work Groups
- Troubleshooting articles
- Wiki

RISE Project

Created by Anonymous, last modified by Michelle Martineau on Jun 29, 2023

Welcome to the RISE Project Confluence!



News

- 5/31/2023: RISE is officially launched

Resources

- RISE Web Site

Quick navigation

- About RISE
- RISE Governing Board
- RISE Technical Steering Committee
- RISE Work Groups
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Home

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  - Quick Wins
  - RISE RFP Process
  - TSC Decisions
  - TSC Meeting Notes
  - **TSC Meetings**
- RISE Work Groups
- Troubleshooting articles
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Space tools

TSC Meetings

Created by Andrei Warkentin, last modified on Jun 01, 2023

Weekly Meetings

See TSC Weekly Meeting Slides folder and meeting notes.

Every meeting gets its own slide deck (e.g. **[RISE] TSC Meeting Agenda 06/01/2023**). The slide deck for each meeting is created a week before the call (in fact, shortly after the previous call!). Anyone can thus update the slide deck throughout the week.

Every TSC meeting is recorded and we follow LF code of conduct and antitrust policies.

Usually the slides include a weekly RISE Work Groups update. Here are some helpful hints when adding slides:

- Highlight the aspects you'd like others to take note – consider folks looking at the deck in a week or so, what would you want them to remember?
- Don't go into excruciating detail if you're there in the call. If you are making an update for a meeting you aren't attending, do add all the details you would have liked to share in person (even if it means adding more slides).

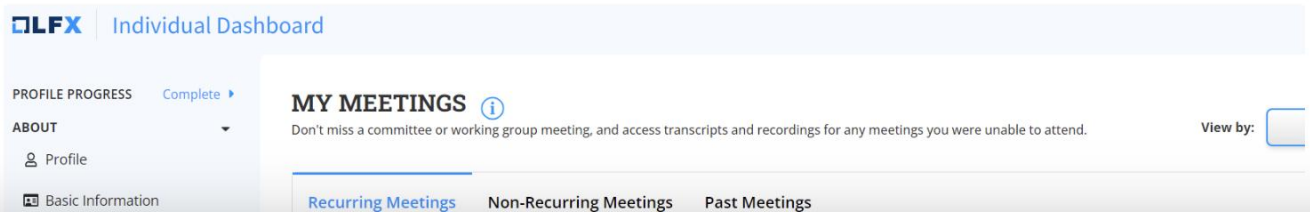
Board Updates

See TSC Org Update Slides (to the Board).

Missing Invites

Login to https://openprofile.dev/my-calendar.

If you have been added to a meeting, you should see this listed. If this is a non-recurring meeting, you'll have to click on **Non-Recurring Meetings**. E.g.:



2022，更“大”的期待：世界超算500强

“我们预测到2025年底的时候，世界超算500强（HPC500）将会出现RISC-V架构的超级计算机，并且不止一台。”

—— 吴伟, PLCT实验室项目总监

谢谢各位

RISC-V是一个遍地机会的新世界，欢迎加入 ☺

本PPT可以通过主办方或 https://github.com/lazyparser/talks 直接下载到

也可以通过 wuwei2016@iscas.ac.cn 找到我