Hi3519A V100 4K Smart IP Camera SoC

Breif Data Sheet

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Hi3519A V100 4K Smart IP Camera SoC

Introduction

Hi3519A V100 is a high-performance and low-power 4K Smart IP Camera SoC designed for IP cameras, action cameras, panoramic cameras, rear view mirrors, and UAVs. Hi3519A V100 introduces H.265/H.264 encoding and decoding, with performance up to 4K x 2K@60 fps and 1080p@240 fps. Integrating with the HiSilicon fourth-generation ISP, Hi3519A V100 provides WDR, multi-level NR, 6DoF DIS, and multiple image enhancement and correction algorithms, ensuring professional image quality. Hi3519A V100 also supports 4K raw data output, facilitating post editing. With the advanced low-power process and architecture design, Hi3519A V100 provides users with long-lasting battery life.

Hi3519A V100 integrates a powerful programmable neural network inference engine and a vector DSP, backing the application of multiple intelligent algorithms.

Hi3519A V100 supports multi-sensor inputs and introduces a built-in high-performance AVS engine to implement 4K 2-pipe to 4-pipe real-time panoramic video stitching.

With the hardware-based 6DoF DIS, Hi3519A V100 has reduced its dependence on the mechanical head during 4K@60 fps video recording.

Hi3519A V100 features efficient and ample computing resources to assist customers in developing industry and consumer applications. Backed by the dual-core A53 processor and the DSP, Hi3519A V100 offers the dual-system solution, enabling fast startup, real-time performance, and connections with rich peripheral drives.

Hi3519A V100 uses the advanced 12 nm low-power process and miniaturization package and supports DDR4/LPDDR4 SDRAMs, allowing the product miniaturization design.

With the stable and easy-to-use mobile SDK design provided by HiSilicon, Hi3519A V100 can assist customers in rapid product mass production.

Key Features

- **Low Power**

  1.9 W power consumption in a typical scenario for 4K x 2K (3840 x 2160)@30 fps H.265 encoding+neural network algorithm

- **SVP**
  - A neural network inference engine (NNIE), a high-performance DSP, and multiple CV acceleration engines that facilitate customers' algorithm development for achieving product differentiation
  - Multiple neural network options
  - 2.0 TOPS computing performance
  - Complete APIs and toolchains
  - Multiple applications such as face detection/recognition and target detection/tracking
- **4K@60 fps Encoding**

  4K x 2K (3840 x 2160)@60 fps or 1080p@240 fps H.265/H.264 encoding

- **Multi-Sensor Inputs**

  Up to 5-channel sensor inputs, supporting applications such as panoramic camera and UAVs

- **Hardware-based Multi-Channel Video Stitching**

  2-channel 3K x 3K (3000 x 3000)@30 fps or 4-channel 1080p@30 fps stitching and recording

- **High-Speed Interface**

  PCIe, USB 3.0, and SDIO 3.0 interfaces that facilitate customers' extension of external functional modules

Hi3519A V100 4K Smart IP Camera SoC

Key Specifications

Processor Core

- Dual-core ARM Cortex-A53@1.5 GHz, 32 KB I-cache, 32 KB D-cache or 256 KB L2-cache
- Neon acceleration and integrated FPU

DSP

- Integrated Tensilica Vision P6 DSP@630 MHz
- 32 KB I-cache, 32 KB I-RAM, and 512 KB D-RAM
- 0.3 TOPS neural network computing performance
- Huawei LiteOS

NNIE

- Multiple neural network options, such as AlexNet, VGG, ResNet, and GoogLeNet
- Multiple neural network options for target detection, such as the Faster R-CNN, SSD, and YOLOv2
- 2.0 TOPS neural network computing performance
- Complete APIs and tool chains (compilers and simulators) to adapt to customized networks

Video Encoding and Decoding

- H.265 main profile, level 5.1
- H.264 baseline/main/high profile, level 5.1
- I-/P-/B-slice supported for H.264/H.265 encoding and decoding
- Baseline JPEG
- Maximum resolution for H.264/H.265 encoding and decoding: 8192 x 8192
- H.265/H.264 encoding and decoding performance:
  - 3840 x 2160@60 fps+720p@30 fps encoding
  - 3840 x 2160@60 fps decoding
  - 3840 x 2160@30 fps encoding+3840 x 2160@30 fps decoding
- Maximum resolution for JPEG encoding and decoding: 8192 x 8192
- Maximum JPEG encoding and decoding performance: 16 MP (4608 x 3456)@30 fps
- Multiple bit rate control modes, such as CBR, VBR, AVBR, FixQp, and QpMap
- Up to a bit rate of 120 Mbit/s for H.265 encoding outputs and 200 Mbit/s for H.264 encoding outputs
- Encoding of up to eight ROIs

VI Interface

- 12-lane image sensor serial inputs, as well as MIPI, sub-LVDS, HiSPi, and SLVS-EC interfaces
- Up to 5-channel sensor serial inputs and multiple combination modes: 12-lane, 8-lane+4-lane, or 4-lane+4 x 2-lane
- Maximum input resolution: 7680 x 4320
- 10-/12-/14-bit Bayer RGB DC timing VI
- BT.656 and BT.1120 VI
  1–channel to 4-channel YUV inputs through the MIPI virtual channels

ISP and Image Processing

- Multi-channel TDM to process multi-sensor video inputs
- Adjustable 3A functions (AE, AWB, and AF)
- FPN removal
- 2-frame WDR exposure, local tone mapping, strong light suppression, and backlight compensation
- Defect pixel correction and lens shading correction
- Multi-level 3DNR, which removes motion smearing and chroma noise and provides excellent image effects in low illumination
- 3D-LUT color adjustment
- Image dynamic contrast enhancement and edge enhancement
- CAC and purple fringe removal
- Dehaze
- 6DoF DIS and rolling shutter correction
- LGDC and fisheye correction
- Image rotation by 90° or 270°
- Image mirroring and flipping
- Multi-channel 1/15.5x–16x scaling outputs
- OSD overlaying of up to eight regions before encoding
- ISP adjustment tool on the PC

2D Graphics Processing

- BitBlt operation
- Line drawing
- Alpha blending
- Color key
- CSC

Hardware Accelerated Engine for Video Stitching

- 2-channel and 4-channel AVS
- Stitching performance:
  - 2-channel 3000 x 3000@30 fps VI and 3840 x 2160@30 fps VO
  - 4-channel 1080 x 1920@30 fps VI and 3840 x 2160@30 fps VO

VO Interface

- HDMI 2.0, supporting up to 4K x 2K (4096 x 2160)@60 fps outputs
- 4-lane MIPI DSI, supporting up to 1080p@60 fps outputs
- 6-/8-/16-/24-bit digital LCD/BT.656/BT.1120 interface, supporting up to 1080p@60 fps RGB/YUV outputs
- Two independent HD VO channels (DHD 0 and DHD 1):
  - Any two interfaces can be used for the display of different sources.
  - DHD 0 supports 36-picture split display.
  - DHD 1 supports 16-picture split display.
- One PIP layer, which can be overlaid with DHD 0 or DHD 1
- Two full-screen GUI graphics layers in ARGB1555 or ARGB8888 format for DHD 0 and DHD 1
- One hardware cursor layer in ARGB1555 or ARGB8888 format (configurable), supporting a maximum resolution

of 256 x 256
- One scaling WBC channel

CV Hardware Accelerated Engine

- Hardware acceleration for binocular depth map computing, supporting the processing performance up to 720p@30 fps
- Hardware acceleration for IVE 2.1 intelligent operators for feature point detection, optical flow, and computer morphology processing, and so on

Audio Interface

- Integrated audio codec, supporting 16-bit audio inputs and outputs
- Dual-channel differential MIC inputs for reducing the background noise
- I^2S interface for 8-channel audio TDM inputs and dual-channel audio outputs (mutually exclusive with the built-in audio codec)
- HDMI audio output

Audio Encoding and Decoding

- Voice encoding and decoding complying with multiple protocols by software
- Audio encoding in formats such as G.711, G.726, and AAC
- VQE

Network Interface

- One GE interface:
  - RGMII and RMII modes
  - 10/100 Mbit/s half-duplex or full-duplex
  - 1000 Mbit/s full-duplex
  - TSO for reducing the CPU usage

Security Engine

- AES, DES, and 3DES algorithms implemented by using hardware
- RSA1024/2048/3072/4096 signature verification algorithm implemented by using hardware
- HASH-SHA1/224/256/384/512 and HMAC_SHA1/224/256/384/512 tamper proofing algorithms implemented by using hardware
- Integrated 32-kbit OTP storage space and hardware random number generator
- Secure boot
- Memory and I/O security isolation

Peripheral Interface

- Two SDIO 3.0 interfaces:
  - SDIO 0 supports the SDXC card.
  - SDIO 1 supports the Wi-Fi module.
- One USB 3.0/PCIe 2.0 multiplexing port
  - USB 3.0 only or PCIe 2.0 X1+USB 2.0.
  - RC and endpoint supported as the PCIe 2.0 interface
  - Configurable USB host/device mode as the USB 3.0 interface
- One USB 2.0 port, supporting configurable host/device mode
- Internal POR signal output and external reset input
- Independent battery for the built-in RTC
- Integrated 4-channel LSADC
- Nine UART interfaces (Some pins are multiplexed with other pins.)
- Multiple I^2C, SPI, and GPIO interfaces
- One IR interface
- Eight PWM interfaces (Some pins are multiplexed with other pins.)

External Memory Interface

- 32-bit DDR4/LPDDR4 SDRAM interface
  - Maximum frequency of 1333 MHz for the DDR4/LPDDR4 SDRAM
  - Maximum DDR address space of 3.5 GB
- SPI NOR flash interface
  - 1-/2-/4-line mode
  - 3-/4-byte address mode
  - Maximum capacity of 256 MB
- SPI NAND flash interface
  - SLC flash
  - 2 KB/4 KB page size
  - 8-/24-bit ECC (unit: KB)
  - Maximum capacity of 1 GB
- NAND flash interface
  - 8-bit data width
  - SLC flash
  - 2 KB/4 KB page size
  - 8-/16-/24-bit ECC (unit: KB)
  - Maximum capacity of 1 GB
- eMMC 5.1 interface
  - HS400
  - Maximum capacity of 2 TB

Configurable Boot Modes

- Booting from the BOOTROM
- Booting from the SPI NOR flash
- Booting from the SPI NAND flash
- Booting from the NAND flash
- Booting from an eMMC

Multiple Image Burning Modes

- Image burning through UART 0
- Image burning through an SD card
- Image burning through a USB device

SDK

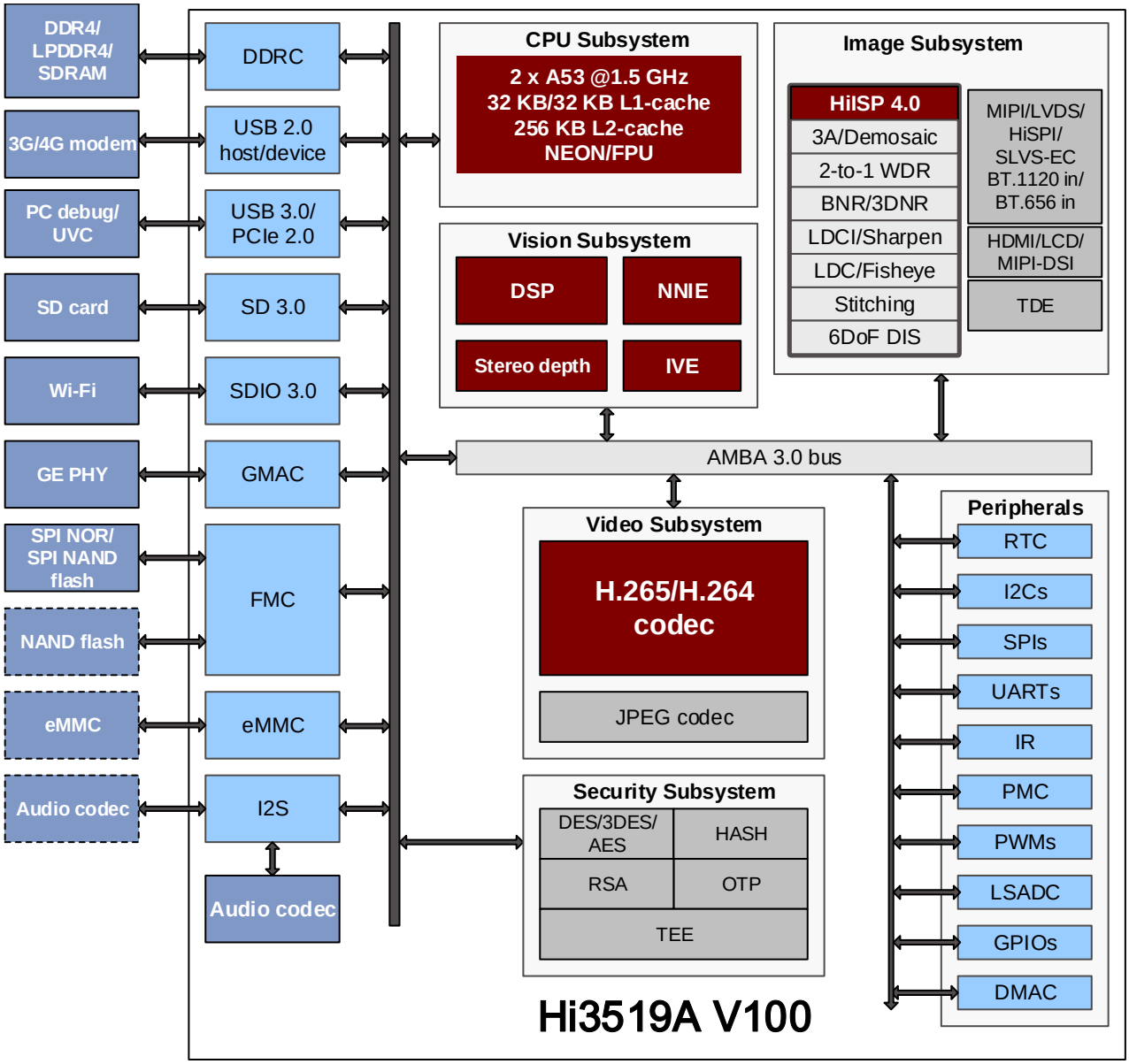
- Linux SMP
- High-performance H.265 iOS/Android decoding library

Physical Specifications

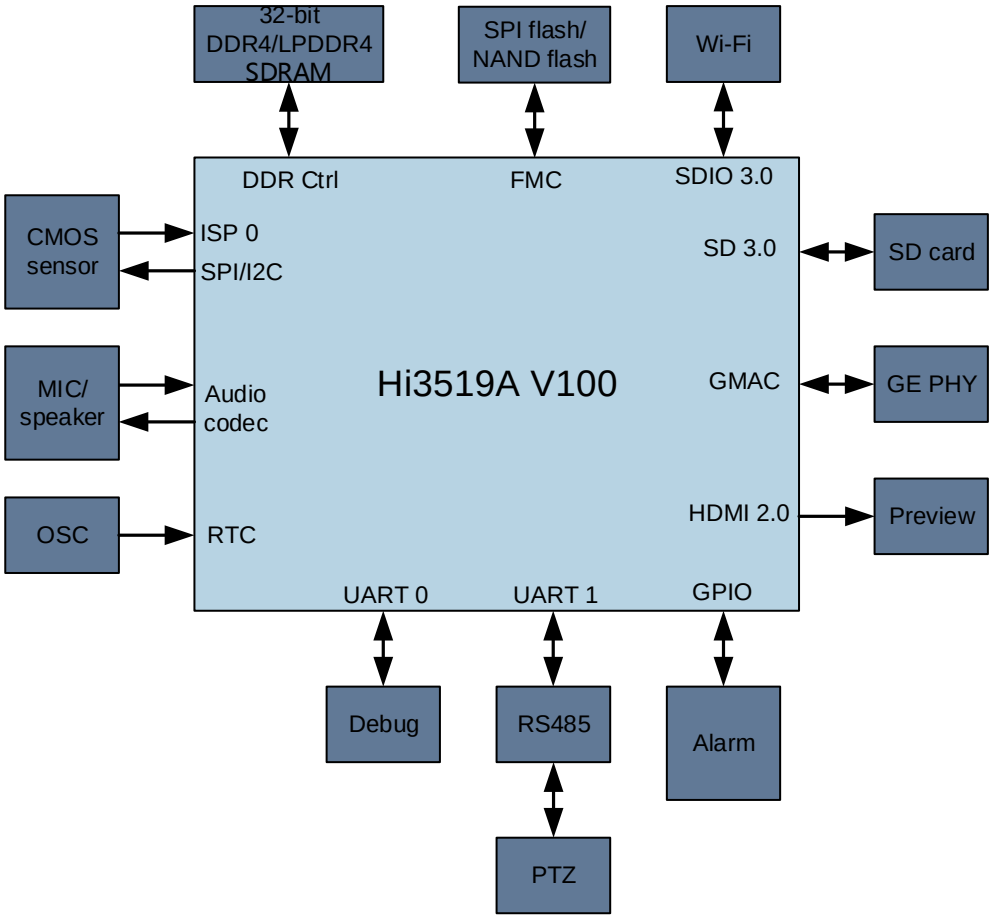
- Power consumption
  - 1.9 W power consumption in a typical scenario for 4K x 2K (3840 x 2160)@30 fps encoding+neural network algorithm
  - Multi-level power saving mode
- Operating voltages
  - 0.8 V core voltage

  - 1.8 V or 3.3 V I/O voltage
  - 1.2 V DDR4 SDRAM interface voltage
  - 1.1 V LPDDR4 SDRAM interface voltage
- Package
  - RoHS-compliant FCCSP
  - Body size: 15 mm x 15 mm (0.59 in. x 0.59 in.)
  - Lead pitch: 0.65 mm and 0.4 mm hybrid pitch
  - Operating temperature: 0°C–70°C

Functional Block Diagram

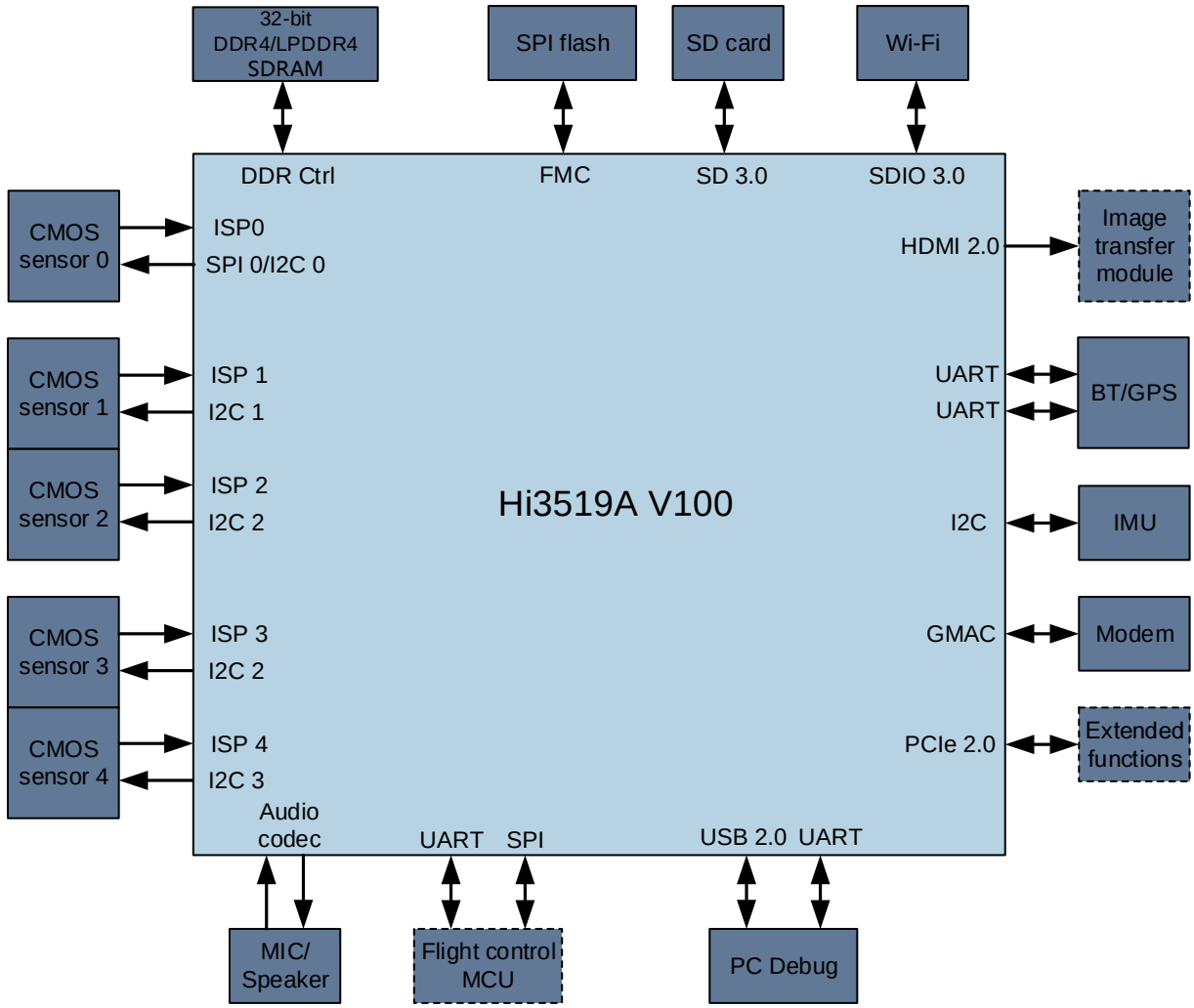


Hi3519A V100 Intelligent IP Camera Solution



- 4K x 2K (3840 x 2160)@30 fps for SD card storage+1080p@30 fps sub stream encoding for Wi-Fi VOD and remote preview
- 4K x 2K (3840 x 2160)@30 fps 6DoF DIS
- NNIE+DSP: facial detection/recognition or human/vehicle detection algorithms
- Two 16-bit DDR4 SDRAMs (2666 Gbit/s) or one 32-bit LPDDR4 SDRAM (2666 Gbit/s)
- Dual MICs with advanced dual-MIC NR algorithm

Hi3519A V100 UAV Camera Solution



- Main camera: 4K x 2K (3840 x 2160)@30 fps encoding for SD card storage+1080p@30 fps sub stream encoded sent to the wireless transmission module over the network or USB port
- 4K x 2K (3840 x 2160) @30 fps 6DoF DIS
- ISP 1/2 for connecting to a front-facing binocular camera. The DPU module extracts the binocular depth map, and sends it to the flight control MCU for obstacle avoidance.
- ISP 3/4 for connecting to a downward facing single-ocular or binocular camera. The DSP runs the SLAM algorithm and sends the calculation result to the flight control MCU for vision hovering.
- NNIE: facial recognition/detection, target detection, or gesture recognition algorithms
- Two 16-bit DDR4 SDRAMs (2666 Gbit/s) or one 32-bit LPDDR4 SDRAM (2666 Gbit/s)
- Wireless transmission: The GMAC sends the streams to the wireless modem module for transmission, or the HDMI output video streams in real time to the graphics transmission module for encoding and wireless transmission.

Acronyms and Abbreviations

3DES	triple data encryption standard
3DNR	three-dimensional noise reduction
6DoF	six degrees of freedom
AAC	advanced audio coding
AE	automatic exposure
AES	advanced encryption standard
AF	automatic focus
API	application programming interface
AVBR	adaptive variable bit rate
AVS	any view stitching
AWB	automatic white balance
CAC	chromatic aberration correction
CBR	constant bit rate
CMOS	complementary metal-oxide-semiconductor
codec	coder/decoder
DC	digital camera
DDR	double data rate
DDRC	double data rate controller
DES	data encryption standard
DIS	digital image stabilization
DSI	display serial interface
DSP	digital signal processor
ECC	error-correcting code
eMMC	embedded multimedia card
FCCSP	flip-chip chip scale package
FPN	fixed pattern noise
FPU	floating-point unit
GE	gigabit Ethernet
GMAC	Gigabit Ethernet Media Access Controller
GPIO	general-purpose input/output
GPU	graphics processing unit
GUI	graphical user interface
HD	high definition
HDMI	high definition multimedia interface
HiSPi	high-speed serial pixel interface
I^2C	inter-integrated circuit
I^2S	Inter-IC Sound
IR	infrared
ISP	image signal processor
IVE	intelligent video engine
LCD	liquid crystal display
LGDC	lens geometric distortion correction
LPDDR	low-power double data rate
LSADC	low-speed analog-to-digital converter
LUT	lookup table
LVDS	low-voltage differential signaling
MCU	microcontroller unit
MIC	microphone
MIPI	mobile industry processor interface
NNIE	neural network inference engine
NR	noise reduction

OS	operating system
OSD	on-screen display
OTP	one-time programming
PCIe	Peripheral Component Interconnect Express
PIP	Picture-in-Picture
POR	power-on reset
PWM	pulse-width modulation
RAM	random access memory
RC	root complex
R-CNN	region-based convolutional neural networks
RGB	red-green-blue
RGMII	reduced gigabit media-independent interface
RMII	reduced media-independent interface
RoHS	Restriction of hazardous substances
ROI	region of interest
RSA	Rivest-Shamir-Adleman
RTC	real-time clock
SD	secure digital
SDIO	secure digital input/output
SDK	software development kit
SDRAM	synchronous dynamic random access memory
SDXC	secure digital extended capacity
SLC	single-level cell
SLVS-EC	Scalable Low Voltage Signaling interface with Embedded Clock
SMP	symmetric multiprocessing
SoC	system-on-chip
SPI	serial peripheral interface
SSD	Single Shot MultiBox Detector
TDM	time division multiplexing
TOPS	Tera Operations Per Second
TSO	TCP segmentation offload
TX	transmit
UART	universal asynchronous receiver transmitter
UAV	unmanned aerial vehicle
USB	Universal Serial Bus
VBR	variable bit rate
VGG	visual geometry group
VI	video input
VO	video output
VOD	video on demand
VQE	voice quality enhancement
WBC	writeback
WDR	wide dynamic range