Hi3559 V200 4K Mobile Camera SoC

Brief Data Sheet

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Hi3559 V200 4K Mobile Camera SoC

Introduction

Hi3559 V200 is a high-performance and low-power 4K ultra-HD mobile camera SoC that is designed for action cameras and streaming media rear-view mirror cameras. Hi3559 V200 supports H.265/H.264 encoding and decoding, with performance up to 4K@P30/1080@P120. Integrated with the HiSilicon (Shanghai) fourth-generation ISP, Hi3559 V200 provides WDR, multi-level NR, 6-DoF DIS, and multiple image enhancement and correction algorithms, allowing customers to capture images of professional quality. With the advanced low-power process and architecture design, Hi3559 V200 provides customers with a long-lasting battery life.

With the hardware-based 6-DoF DIS, Hi3559 V200 has reduced its dependence on the mechanical head during 4K@P30 video recording.

Backed by the dual-core Cortex-A7 CPU, Hi3559 V200 offers the dual-system solution, enabling fast startup, real-time performance, and connections with rich peripheral drives.

Hi3559 V200 supports the product miniaturization design because it uses the advanced 28 nm low-power process and miniaturization package and supports DDR3(L)/DDR4/LPDDR3 SDRAMs.

With the stable and easy-to-use SDK design, Hi3559V 200 can assist customers in rapid product mass production.

Key Specifications

- Low Power Consumption

  Typical power consumption in the 3840 x 2160@30 fps H.265 encoding scenario: 1.1 W

- Advanced Gyro Image Stabilization 2.0 Algorithm

  Hardware acceleration stabilization algorithm with up to 4K@30 fps performance

- 4K30 Encoding

  3840 x 2160@30 fps or 1080p@120 fps H.265/H.264 encoding

- Highest 0.4T neural network computing capability

  Intelligent functions such as third-party object (face) detection and tracking as well as scenario identification

- Dual-Sensor Access

  Dual-channel input applications, such as streaming media rear-view mirror cameras.

- Fast Startup

Hi3559 V200 4K Mobile Camera SoC

Major Specifications

Processor Core

- ARM Cortex A7 MP2 @900 MHz, 32 KB I-cache, 32 KB D-cache, and 256 KB L2 cache
- Neon acceleration and integrated FPU

Video Encoding and Decoding

- H.265 Main Profile, level 5.1
- H.264 Baseline/Main/High Profile, level 5.1
- I-/P-slice supported in H.265/H.264 encoding and decoding
- Baseline JPEG

Video Encoding and Decoding Performance

- Maximum resolution for H.265/H.264 encoding and decoding: 3840 x 2160
- H.265/H.264 encoding and decoding performance:
  - 3840 x 2160@30 fps + 720p@30 fps encoding
  - 3840 x 2160@30 fps decoding
- Maximum resolution for JPEG encoding and decoding: 8192 x 8192
- Maximum JPEG encoding and decoding performance: 16 MP (4608 x 3456)@10 fps
- Multiple bit rate control modes such as CBR, VBR, and FIXQP
- Maximum bit rate for H.265/H.264 encoding output: 100 Mbit/s
- Encoding of eight ROIs

VI

- 4-lane image sensor serial input, and MIPI, sub-LVDS, and HiSPi interfaces
- Division of the 4-lane MIPI sensor input into two groups of 2-lane MIPI input
- Maximum resolution of the first input: 4608 x 3456; maximum resolution of the second input: 2048 x 1536
- 10-/12-/14-bit Bayer RGB DC timing VI
- BT.656 and BT.1120 video input in YUV format
- One YUV input through the MIPI

ISP and Image Processing

- Multi-channel TDM for processing 2-channel sensor video input
- Adjustable 3A functions (AE, AWB, and AF)
- FPN removal
- 2-frame WDR exposure, local tone mapping, strong light suppression, and backlight compensation
- Defect pixel correction and LSC
- Multi-level 3DNR, which removes motion smearing and chroma noise and provides excellent image effects in low illumination
- 3D-LUT color adjustment
- Image dynamic contrast enhancement and edge enhancement
- CAC and purple fringe removal
- Dehaze
- 6-DoF image stabilization (based on video or gyro information) and rolling-shutter correction
- Lens GDC
- Image rotation by 90° or 270°
- Image mirror and flip
- Multi-channel 1/15.5x–16x scaling for output
- OSD overlaying of up to eight regions before encoding
- ISP adjustment tool on the PC

Graphics Processing

- 2D graphics acceleration
- Maximum output resolution: 1920 x 1080.

VO

- Overlay of two layers (video layer and graphics layer)
- HDMI 1.4 interface, with the maximum output of 3840 x 2160@30 fps
- 4-lane MIPI DSI output
- 6-/8-/16-/18-/24-bit digital LCD interface
- BT.656/BT.1120 interface

Intelligent Analysis

- Intelligent functions such as third-party object (face) detection and tracking as well as scenario identification

- Neural network acceleration engine with processing performance up to 0.4 TOPS

Audio Interface

- Integrated audio codec, supporting 16-bit audio input and output
- Single-end dual-channel input and stereo output
- I^2S interface for connecting to external audio codec
- HDMI audio output

Audio Encoding and Decoding

- Voice encoding/decoding complying with multiple protocols by using software
- Audio encoding formats such as AAC/G.711/G.726/
- Audio VQE processing

Security Engine

- AES, DES, and 3DES encryption and decryption algorithms implemented by using hardware
- RSA 1024/2048/4096 signature verification algorithms implemented by using hardware
- HASH-SHA1/224/256/384/512 and HMAC_SHA1/224/256/384/512 tamper-proofing algorithms implemented by using hardware
- Built-in 8-kb OTP storage space
- Built-in hardware true random number generator

Peripheral Interfaces

- Two SDIO 3.0 interfaces. One can be connected to the SD3.0 card.
- One USB 2.0 port, supporting the configurable host or device mode
- Output of the internal POR signal
- Independent battery for the built-in RTC
- Integrated 2-channel LSADC
- Multiple I^2C interfaces, SPI, and UART interfaces
- One IR interface
- Three PWM interfaces

External Memory Interfaces(DDR4 is not supported currently)

- 32-bit DDR3(L)/DDR4/LPDDR3 SDRAM interface
  - Maximum frequency of the DDR3(L)/DDR4 SDRAM interface: 900 MHz
  - Maximum frequency of the LPDDR3 SDRAM interface: 800 MHz
- SPI NOR flash interface
  - 1-/2-/4-line mode
  - 3-/4-byte address mode
  - Maximum capacity: 256 MB
- SPI NAND flash interface
  - Up to 24 bit/1 KB ECC performance
  - Maximum capacity: 1 GB
- eMMC 4.5 interface
  - 4-bit data width

Boot

- Booting from the SPI NOR flash memory, SPI NAND flash memory, or eMMC

Image Burning Mode

- Image burning over UART 0
- Image burning over the SD card
- Image burning over the USB device

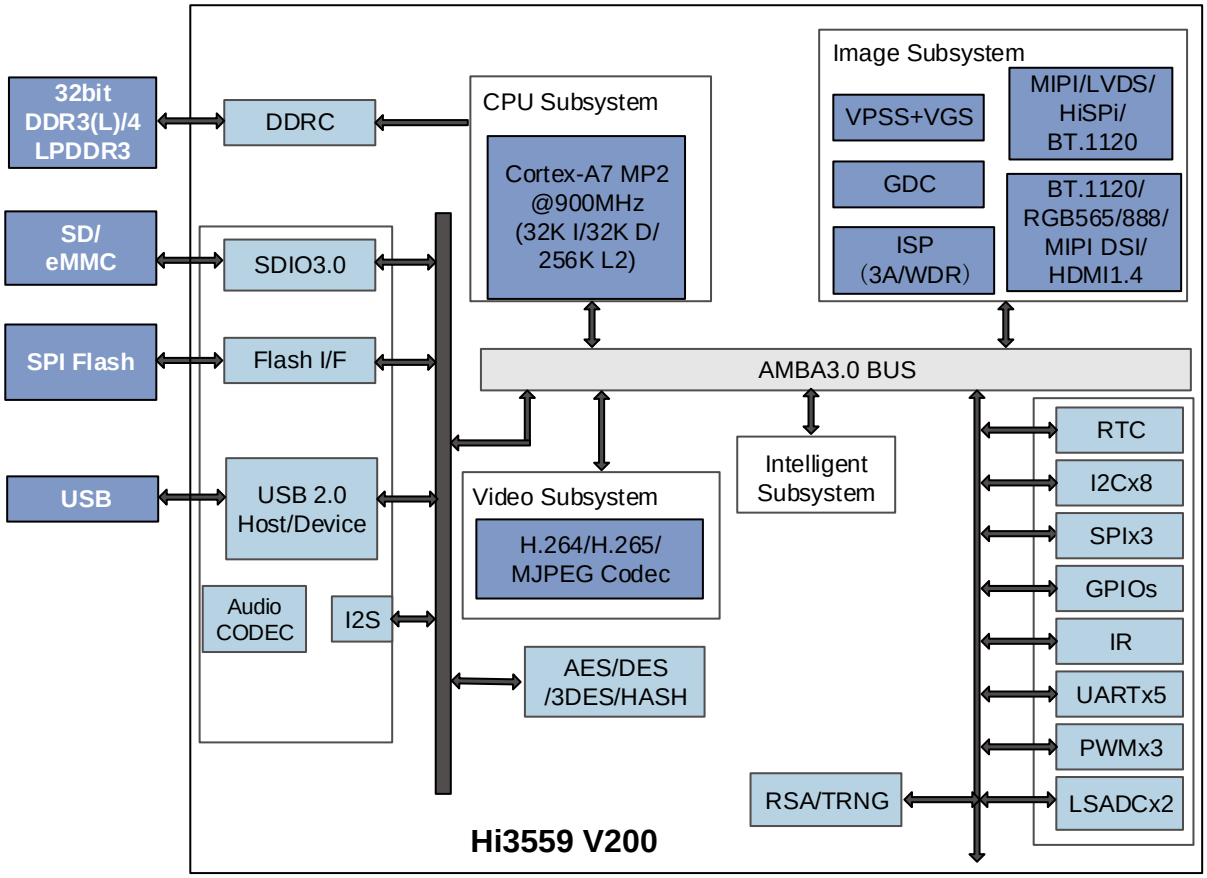
SDK

- Linux+Huawei LiteOS dual-system solution
- High-performance H.265 iOS/Android decoding library

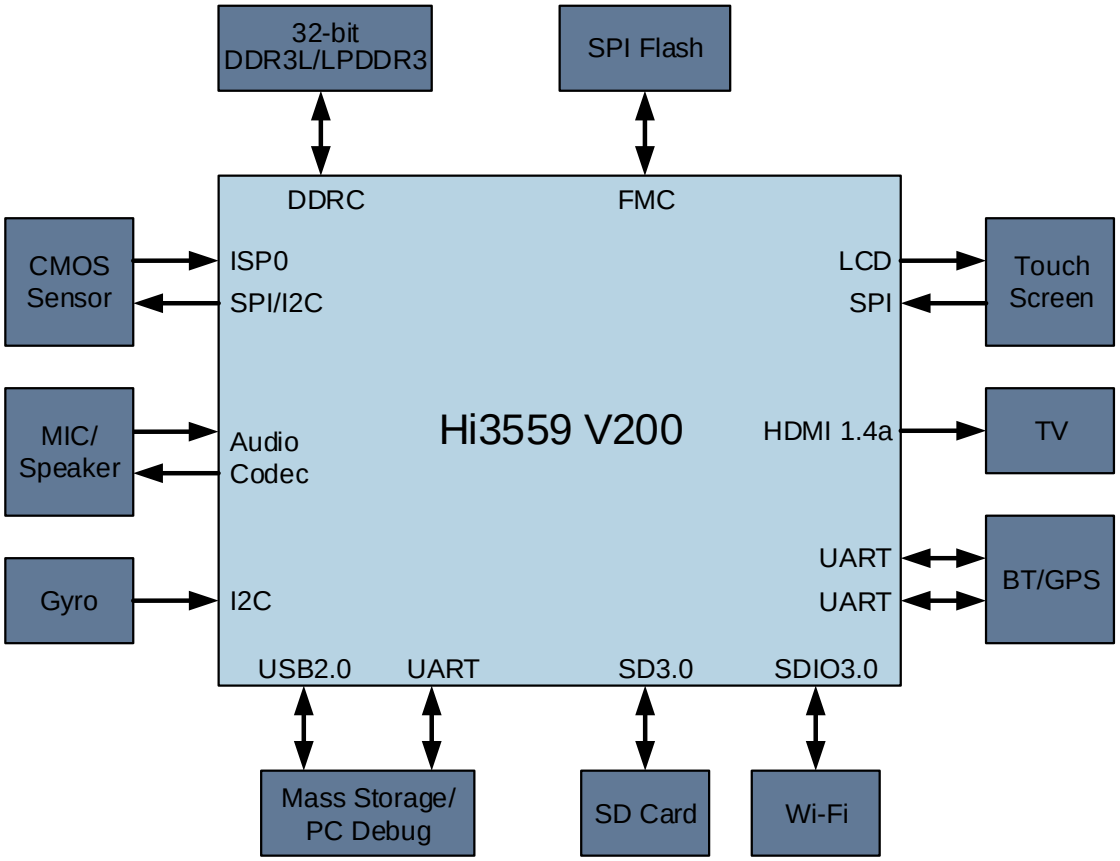
Physical Specifications

- Power consumption
  - Typical power consumption in the 3840 x 2160@30 fps H.265 encoding scenario: 1.1 W
- Operating voltages
  - 0.9 V core voltage
  - 1.8 V/3.3 V I/O voltage
  - 1.5 (1.35) V/1.2 V/1.2 V voltage for the DDR3(L)/DDR4/LPDDR3 SDRAM interface
- Package
  - Body size of 14 mm x 14 mm (0.55 in. x 0.55 in.), 0.65 mm (0.03 in.) ball pitch, TFBGA RoHS package with 367 pins

Functional Block Diagram

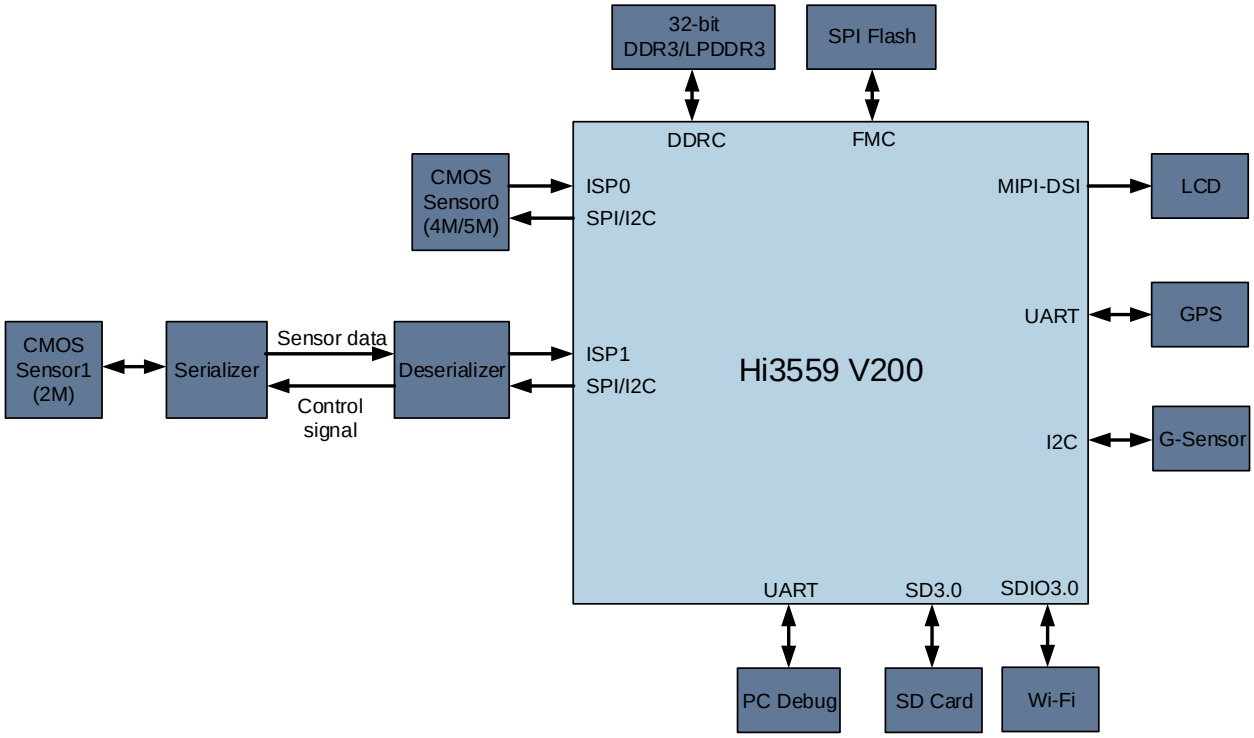


Hi3559 V200 Action Camera Solution



- Video recording mode: 3840 x 2160@30 fps encoding for SD card storage + 720p@30 fps sub-stream encoding for Wi-Fi VOD or preview
- 3840 x 2160@30 fps/1080p@60 fps 6-DoF digital image stabilization based on the gyro.
- Photographing mode: 16 MP (4608 x 3456)@10 fps/12 MP @15 fps burst mode
- Playback mode: 3840 x 2160@30 fps decoding + HDMI 3840 x 2160@30 fps for TV display
- Two 16-bit 1866 Mbit/s DDR3L SDRAMs or one 32-bit 1600 Mbit/s LPDDR3 SDRAM
- Dual MICs and advanced dual-MIC NR algorithm

Hi3559 V200 Streaming Media Rear-View Mirror Camera Solution



- MIPI interface input (4M WDR + 2M WDR) or (5M linear + 2M WDR)
- MIPI interface and BT. 656 input (5M WDR + 2M YUV)
- (5M + 2M) @30 fps H.265/H.264 encoding
- Interconnection with the 1080p screen through the MIPI-DSI interface for low-delay preview
- Two 16-bit 1866 Mbit/s DDR3 SDRAMs or one 32-bit 1600 Mbit/s LPDDR3 SDRAM

Acronyms and Abbreviations

3DNR	three-dimensional noise reduction
6-DoF	six degrees of freedom
AAC	advanced audio coding
AE	automatic exposure
AES	advanced encryption standard
AF	auto focus
AWB	automatic white balance
CAC	chromatic aberration correction
CBR	constant bit rate
CPU	central processing unit
DDR	double data rate
DES	data encryption standard
DIS	digital image stabilization
DSI	display serial interface
ECC	error checking and correction
eMMC	embedded multimedia card
GDC	geometric distortion correction
HD	high definition
HDMI	high definition multimedia interface
HiSPi	high-speed serial pixel interface
IR	infrared spectrum
ISP	image signal processor
LSADC	low-speed analog-to-digital converter
LSC	lens shading correction
LVDS	low-voltage differential signaling
MIC	microphone
MIPI	mobile industry processor interface

NR	noise reduction
OSD	on-screen display
OTP	one-time programmable
POR	power-on reset
PWM	pulse-width modulation
RoHS	restriction of hazardous substances
ROI	region of interest
RSA	Rivest-Shamir-Adleman
RTC	real-time clock
SDIO	secure digital input output
SDK	software development kit
SDRAM	synchronous dynamic random access memory
SoC	system on a chip
TFBGA	thin & fine ball grid array
UART	universal asynchronous receiver transmitter
VBR	variable bit rate
VI	video input
VO	video output
VOD	video on demand
VQE	voice quality enhancement
WDR	wide dynamic range
YUV	luminance-bandwidth-chrominance

