Hi3531D V200 H.265 Codec AI Processor

Brief Data Sheet

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Hi3531D V200 H.265 Codec AI Processor

Main Features

Processor Cores

- ARM Cortex-A53 quad-core@1.15 GHz
  - 32 KB L1 I-cache and 32 KB L1 D-cache
  - 512 KB L2 cache
  - NEON/FPU

Multi-Protocol Video Codec

- H.265 Main Profile, Level 5.0 encoding
- H.265 Main Profile, Level 5.1 decoding
- H.264 Baseline/Main/High Profile, Level 5.1 encoding
- H.264 Baseline/Main/High Profile, Level 5.2 decoding
- MJPEG/JPEG Baseline encoding and decoding

Video Codec

- H.265/H.264&JPEG multi-stream encoding and decoding performance:
  - 8 x 1080p@30 fps H.265/H.264 encoding+8 x D1@30 fps H.265/H.264 encoding+8 x 1080p@30 fps H.265/H.264 decoding+8 x 1080p@2 fps JPEG encoding
  - 16 x 1080p@15 fps H.265/H.264 encoding+16 x D1@30 fps H.265/H.264 encoding+16 x 1080p@15 fps H.265/H.264 decoding+16 x 1080p@2 fps JPEG encoding
  - 16 x 4M@7.5 fps H.265/H.264 encoding+16 x D1@30 fps H.265/H.264 encoding+16 x 4M@7.5 fps H.265/H.264 decoding+16 x 4M@1 fps JPEG encoding
- Seven bit rate control modes, including CBR, VBR, AVBR, CVBR, FIXQP, QPMAP, and QVBR
- Output bit rate up to 20 Mbit/s
- ROI encoding
- Color-to-gray encoding

SVP

- NNIE
  - Multiple neural network options
  - 1.2 TOPS computing performance
  - Complete APIs and toolchains
  - Multiple applications such as face detection, facial recognition, object detection, and object tracking
- IVE
  - Object tracking
- MAU
  - Single-precision or half-precision floats
  - Feature vector comparison

Video and Graphics Processing

- Pre-processing and post-processing including de-interlacing, sharpening, 3DNR, DCI, and mosaic
- Anti-flicker for video and graphic outputs
- Video scaling (1/15x to 16x)
- Graphics scaling (1/2x to 2x)
- Up to four Cover regions
- Up to 8-region OSD overlay

Video Interfaces

- VI interfaces
  - Eight MIPI D-PHY interfaces and one BT.1120 video cascade interface
  - Each MIPI interface supports:
    - Four lanes at rates up to1.5 Gbit/s
    - Single input, two multiplexed inputs, or four multiplexed inputs
    - Multiplexed as one 8-bit BT.656 interface
  - Every two BT.656 interfaces can form one 16-bit BT.1120 interface.
  - Both BT.656 and BT.1120 interfaces support dual-edge sampling at 148.5 MHz.
  - Up to 33 VI channels (including one video cascade channel)
  - 16-channel online video scaling
  - The source image and the scaled image can be output at the same time.
    - Maximum MIPI input performance:
      - 8-channel 4K@30 fps or 16-channel 4K@15 fps
      - 16-channel 4M@30 fps or 16-channel 5M@20 fps
      - 32-channel 1080p@30 fps
  - Maximum output performance: 16-channel 1080p@30 fps (or 4M/5M/4K images with the same data volume) +1-channel 4K@30 fps (cascade input image)
- VO interfaces
  - One HDMI 2.0 output interface with the maximum output of 3840 x 2160@60 fps
  - One VGA HD output interface at up to

2560 x 1600@60 fps
- One BT.1120 HD output interface at up to3840 x 2160@30 fps (dual-edge sampling)
- One CVBS SD output interface, supporting the PAL/NTSC standard output
- Two independent HD VO channels (DHD 0 and DHD 1)
  - Two HD interfaces with display from different sources
  - DHD 0 supports 64-picture display.
  - DHD 1 supports 64-picture display.
- One independent SD output channel (DSD 0)
- One PiP layer, which can be overlaid with DHD 0 or DHD 1
- Two graphics layers in ARGB1555, ARGB4444, or ARGB8888 format for DHD 0 and DHD 1, respectively
- One special graphics layer, which supports CLUT 2/CLUT 4 and can be bound to DHD 0, DHD 1, or DSD 0
- One hardware cursor layer in ARGB1555, ARGB4444, or ARGB8888 format (configurable) with a maximum resolution of 256 x 256

Audio Interfaces

- Three unidirectional I²S/PCM interfaces
  - Two inputs, supporting 20 multiplexed inputs
  - One output, supporting dual-audio channel output

ETH Interfaces

- Two GE interfaces
  - RGMII and RMII modes
  - 10/100 Mbit/s half-duplex or full-duplex
  - 1000 Mbit/s full-duplex
  - TSO for reducing the CPU overhead

Security Engine

- AES 128/192/256-bit encryption and decryption algorithms
- RSA 2048/4096-bit encryption and decryption algorithms
- SHA256/HMAC_SHA256
- OTP, providing 28-kbit user space to burn images
- Hardware-based true random number generator
- Secure boot
- Secure memory isolation

Peripheral Interfaces

- Four SATA 3.0/PCIe 2.0 combo interfaces
  - The interface combination can be as follows: 4*SATA, 2*SATA+1*PCIe x2, 2*SATA+2*PCIe x1, or 2*PCIe x2.
  - When the combo interface is configured as PCIe 2.0, the RC and EP functions are supported.
  - When the combo interface is configured as SATA 3.0, the eSATA and PM functions are supported.
- One USB 3.0 host interface
- Two USB 2.0 host interface
- Five UART interfaces, two of which support the 4-wire mode
- One SPI interface, supporting four chip selects
- One IR interface
- Two I²C interfaces
- Multiple GPIO interfaces

Memory Interfaces

- Two 32-bit DDR4/DDR3 interfaces
  - Dual channels
  - Maximum DDR4 clock frequency: 1200 MHz
  - Maximum DDR3 clock frequency: 1066 MHz
  - Maximum capacity: 8 GB
- SD/MMC interfaces
  - eMMC 4.5/eMMC 5.0/eMMC 5.1
  - HS400 (150 MHz dual-edge)
  - SDIO 3.0 (non-SD card)
- SPI NOR/NAND flash interfaces
  - Two CSs, which can be connected to different types of flash memories
  - For the SPI NOR flash:
    - 1-, 2-, or 4-line mode
    - 3- or 4-byte address mode
    - Maximum capacity: 256 MB
  - For the SPI NAND flash:

- SLC flash
- 2 KB or 4 KB page size
- 8- or 24-bit ECC (ECC is in the unit of 1 KB.)
- Maximum capacity: 2 GB

RTC with Independent Power Supply

The RTC can be independently powered by batteries.

Multiple Boot Modes

- Boot from the BootROM
- Boot from the SPI NOR flash
- Boot from the SPI NAND flash
- Boot from the eMMC
- Boot from the slave chip over the PCIe interface

SDK

- Linux SMP (64-bit)
- Audio codec libraries that support multiple protocols
- High-performance PC decoding library based on H.265/H.264

Chip Physical Specifications

- Power consumption
  - Power consumption in typical scenarios (16-channel 1080p@15 fps encoding+8-channel 1080p@15 fps decoding+deep learning intelligent algorithm): 4.6 W
  - Multi-level power consumption control
- Operating voltages
  - Core voltage: 0.9 V
  - CPU voltage: 1.0 V
  - I/O voltage: 1.8 V/3.3 V
  - Voltage of the DDR4 interface: 1.2 V
  - Voltage of the DDR3 interface: 1.5 V
- Package
  - ROHS, EHS-TFBGA
  - Ball pitch: 0.8 mm (0.03 in.)
  - Dimensions: 22.4 mm x 31.2 mm (0.88 in. x 1.22 in.)
  - Operating temperature: 0°C–70°C (32°F–158°F)

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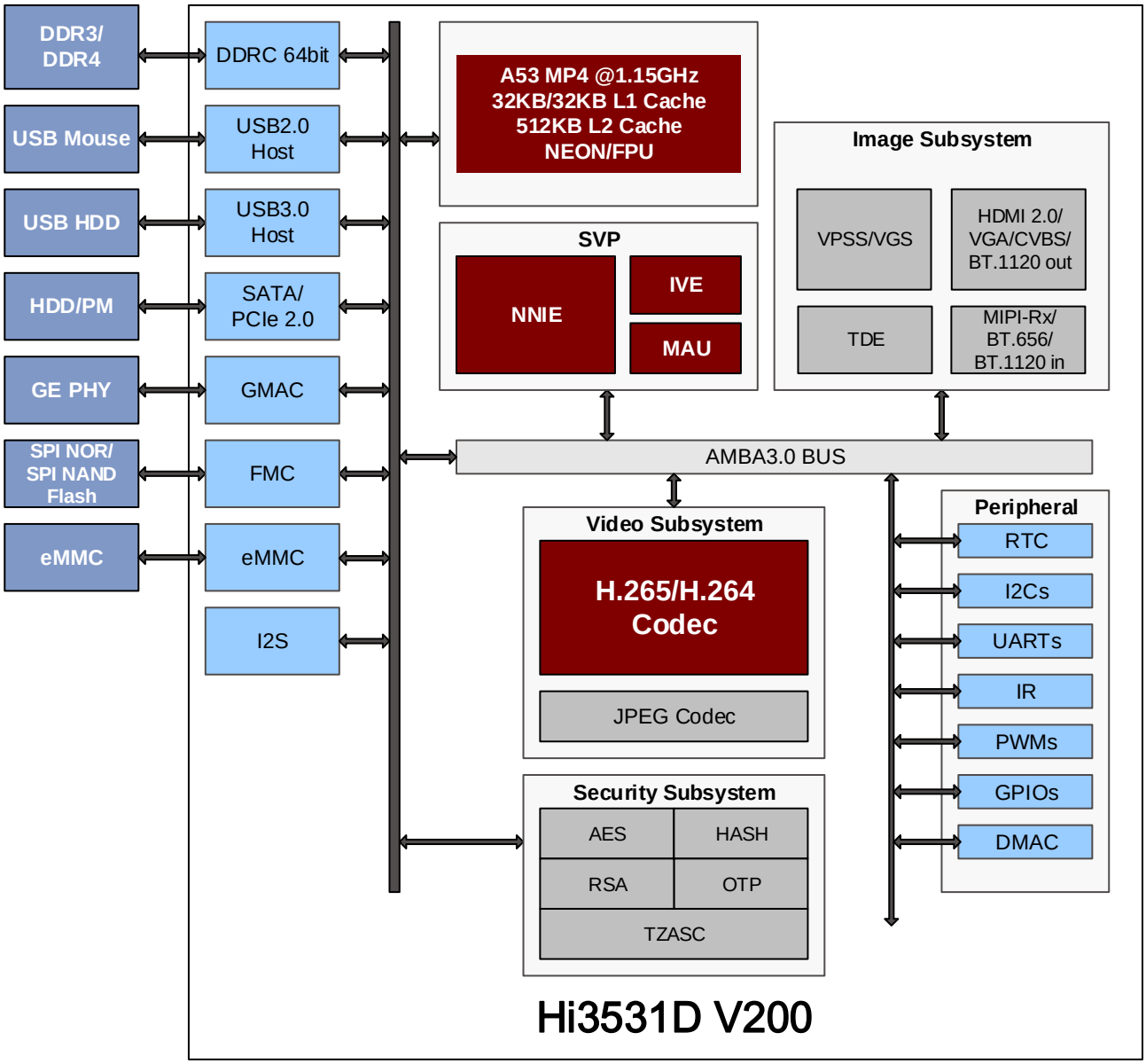
Functional Block Diagram



Hi3531D V200 is a new-generation professional SoC designed for multi-channel HD/UHD (1080p/4M/5M/4K) digital video recorder (DVR) applications. It integrates the ARM Cortex-A53 quad-core processor and powerful inference engine, supporting multiple intelligent algorithm applications. In addition, Hi3531D V200 integrates multiple MIPI D-PHY inputs, achieving new breakthroughs in the video input performance of digital interfaces and providing twice the video input capability of predecessor products. The H.265 video codec engine and video image processing algorithm are improved. The SoC provides high-performance and high-quality analog HD DVR solutions based on various peripheral devices and high-speed interfaces. It is widely used in analog HD surveillance markets and vehicle-mounted DVR markets.

Single-Chip Hi3531D V200 DVR Solution

16 x 1080p DVR

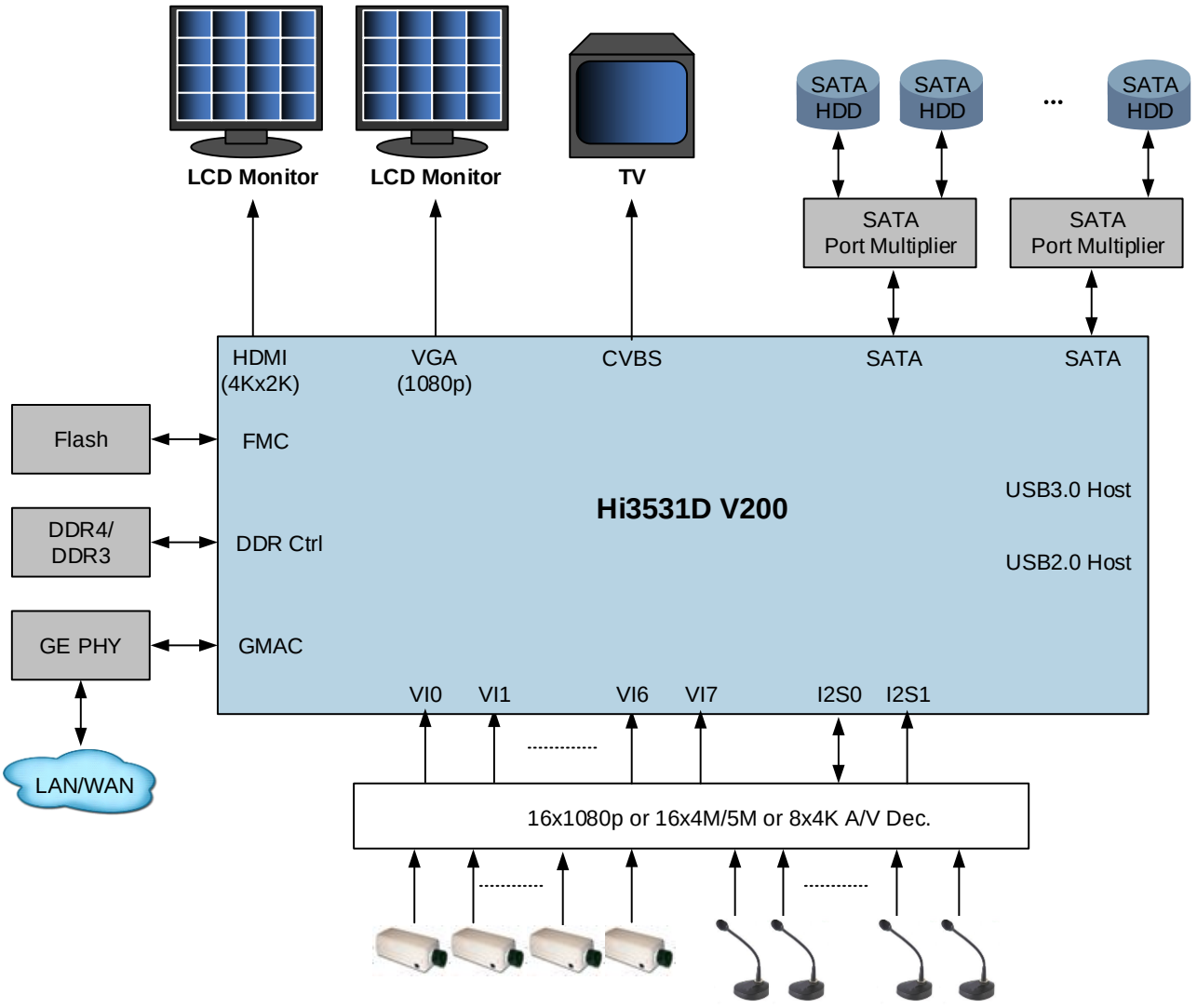
- 16 x 1080p@15 fps H.265/H.264 encoding+16 x D1@30 fps H.265/H.264 encoding+16 x 1080p@15 fps H.265/H.264 decoding+16 x 1080p@1 fps JPEG encoding
- 16 x 1080p@30 fps real-time video input+real-time preview+HDMI 4K x 2K@30 fps display output
- Multi-channel intelligent analysis (such as human/vehicle detection and face detection)

16 x 4M (2560 x 1440) DVR

- 16 x 4M@7.5 fps H.265/H.264 encoding+16 x D1@30 fps H.265/H.264 encoding+16 x 4M@7.5 fps H.265/H.264 decoding+16 x 4M@1 fps JPEG encoding
- 16-channel 4M input+real-time preview+HDMI 4K x 2K@30 fps display output
- Multi-channel intelligent analysis (such as human/vehicle detection and face detection)

8 x 4K (3840 x 2160) DVR

- 8 x 4K@7.5 fps H.265/H.264 encoding+8xD1@30 fps H.265/H.264 encoding+8 x 4K@7.5 fps H.265/H.264 decoding+8 x 4K@1 fps JPEG encoding
- 8-channel 4K input+real-time preview+HDMI 4K x 2K@30 fps display output
- Multi-channel intelligent analysis (such as human/vehicle detection and face detection)



Acronyms and Abbreviations

3DNR	three-dimensional noise reduction
AES	Advanced Encryption Standard
AVBR	adaptive variable bit rate
CBR	constant bit rate
CS	chip select
DCI	dynamic contrast improvement
DDR	double data rate
DVR	digital video recorder

ECC	error checking and correction
eMMC	embedded multimedia card
GPIO	general-purpose input/output
HD	high definition
HDMI	high definition multimedia interface
IR	Infrared radiation
IVE	intelligent video engine
JPEG	Joint Photographic Experts Group
MAU	matrix arithmetic unit
MIPI	Mobile Industry Processor Interface
NNIE	neural network inference engine
OSD	on-screen display
OTP	one-time programmable
PCIe	Peripheral Component Interconnect Express
PiP	Picture-in-Picture
ROI	region of interest
RSA	Rivest-Shamir-Adleman
RTC	real-time clock
SATA	Serial Advanced Technology Attachment
SD	standard definition
SDK	software development kit
SMP	symmetric multiprocessing
SoC	system on a chip
SPI	serial peripheral interface
SVP	smart vision processing
TCP	Transmission Control Protocol
UART	universal asynchronous receiver/transmitter

VBR	variable bit rate
VGA	video graphics array
VI	video input
VO	video output