



Hi3516C V500 Professional Smart IP Camera SoC

Brief Data Sheet

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| Issue | 01 |
| Date | 2018-06-28 |

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Hi3516C V500 Professional Smart IP Camera SoC

Key Specifications

Processor Core

- Dual-core ARM Cortex-A7@ 900 MHz, 32 KB I-cache, 32 KB D-cache, 256 KB L2 cache
- Neon acceleration and integrated FPU

VENC

- H.264 BP/MP/HP
- H.265 MP
- I-/P-frames and SmartP reference.
- MJPEG/JPEG baseline

VENC Performance

- Up to 2304-pixel wide and 2304 x 1296 resolution for H.264/H.265 encoding
- Real-time multi-stream H.264/H.265 encoding:
 - 1920 x 1080@30 fps+720 x 480@30 fps+360 x 240@30 fps
 - 2304 x 1296@20 fps+720 x 480@20 fps+360 x 240@20 fps
- JPEG encoding performance: 4608 x 3456 @10 fps
- Five bit rate control modes (CBR, VBR, FixQp, AVBR, and QpMap)
- Up to 50 Mbit/s output bit rate
- Up to 8-ROI encoding

Smart Video Analysis

- Neural network acceleration engine with processing performance up to 0.5 TOPS
- Smart computing acceleration engine

Video and Graphics Processing

- 3DNR, image enhancement, and DCI
- Anti-flicker processing for video and graphics output
- 1/15–16x video and graphics scaling
- Video graphics overlay
- 90°, 180°, and 270° image rotation
- Image mirroring and flipping
- Up to 8-region OSD overlay before encoding

ISP

- 3A functions (AE, AF, and AWB), supporting third-party 3A algorithms
- FPN removal and DPC
- LSC, LDC, and purple fringing correction
- Direction-adaptive demosaic
- Gamma correction, DCI, and color management and enhancement
- Region-adaptive dehaze
- Multi-level NR (including BayerNR and 3DNR), detail enhancement, and sharpening enhancement
- Local tone mapping
- Sensor built-in WDR and 2F WDR (line-based/frame-based/DCG)
- Video-/Gyro-based 6-DoF IS
- ISP tuning tools for the PC

Audio Encoding and Decoding

- Multi-protocol audio encoding and decoding (G.711, G.726, and ADPCM) by using software
- Audio 3A functions (AEC, ANR, and ALC)

Security

- Secure boot
- Hardware-based memory isolation
- Hardware-based encryption and decryption algorithms (including AES, DES, 3DES, and RSA)
- Hardware-based HASH algorithms (SHA1/SHA256/HMAC_SHA/HMAC_SHA256)
- Hardware random number generator
- 8-kbit OTP storage space

Video Interface

- VI
 - 1-channel VI
 - 8-/10-/12-/14-bit RGB Bayer DC timing VI
 - BT.601, BT.656, and BT.1120 VI interfaces
 - MIPI, LVDS/sub-LVDS, and HiSPi
 - Compatibility with mainstream HD CMOS sensors provided by vendors such as Sony, ON, OmniVision, and Panasonic
 - Compatibility with the electrical specifications of parallel and differential interfaces of various sensors
 - Programmable sensor clock output
 - Up to 2304-pixel wide and 2304 x 1296 resolution
- VO
 - One BT.656/BT.1120 VO interface
 - 6-/8-bit RGB serial LCD VO and 16-/18-/24-bit RGB parallel LCD VO
 - 4-lane MIPI-DSI VO

Audio Interface

- Audio codec, supporting 16-bit input and output
- Mono-channel differential MIC input for background NR
- Single-end dual-channel input
- I²S interface for connecting to external audio codec

Peripheral Interface

- POR
- High-precision RTC
- 2-channel LSADC
- I²C interfaces, SPIs, and UART interfaces
- Three PWM interfaces
- Two SDIO 3.0 interfaces, supporting the 3.3 V/1.8 V level
 - SD 3.0 card supported over one SDIO 3.0 interface
- One USB 2.0 host/device interface
- RMII mode, TSO network acceleration, 10/100 Mbit/s full-duplex or half-duplex mode, and PHY clock output

External Memory Interface

- SDRAM interface
 - 16-bit DDR3(L)/DDR4 SDRAM, supporting a maximum capacity of 8 Gbits
 - Up to 1800 Mbit/s rate
- SPI NOR flash interface



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- 1-/2-/4-line mode
- Maximum capacity of 256 MB
- SPI NAND flash interface
 - Up to 24 bit/1 KB ECC performance
 - Maximum capacity of 1 GB
- eMMC 4.5 interface
 - 4-bit data width

Startup

Booting from the SPI NOR flash, SPI NAND flash, or eMMC

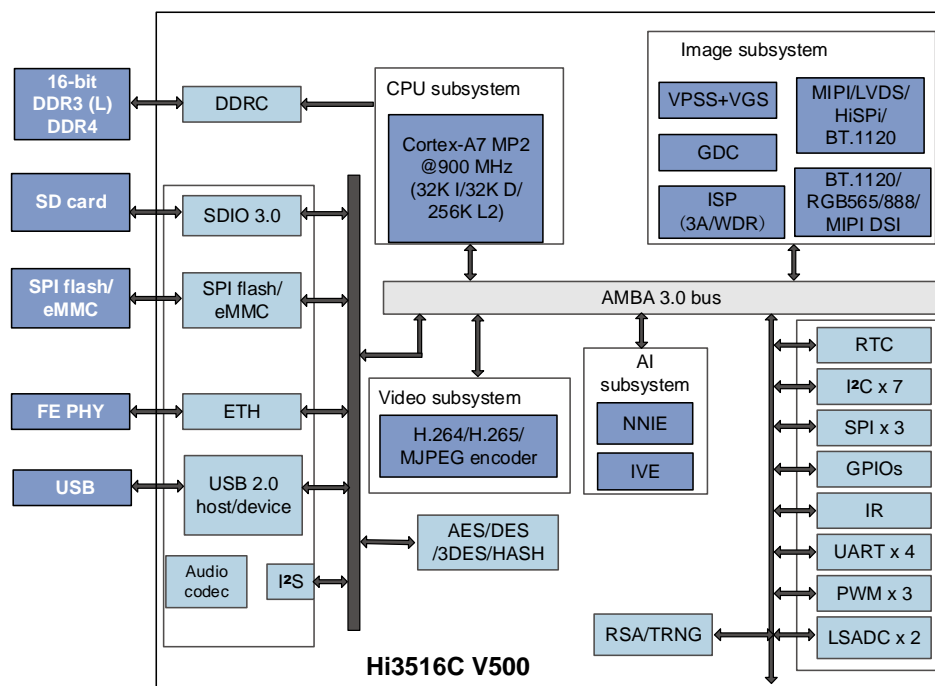
SDK

- Linux-4.9-based SDK
- High-performance H.264 PC decoding library
- High-performance H.265 PC, Android, and iOS decoding libraries

Physical Specifications

- Power consumption
 - Typical power consumption at 1080p@30 fps: 900 mW (650 mW with the NNIE disabled)
- Operating voltage
 - 0.9 V core voltage
 - 3.3 V I/O voltage ($\pm 10\%$)
 - 1.5 (1.35) V/1.2 V DDR3(L)/4 SDRAM interface voltage
- Package
 - Body size of 12 mm x 12 mm (0.47 in. x 0.47 in.), 0.65 mm (0.03 in.) ball pitch, TFBGA RoHS package with 280 pins

Functional Block Diagram

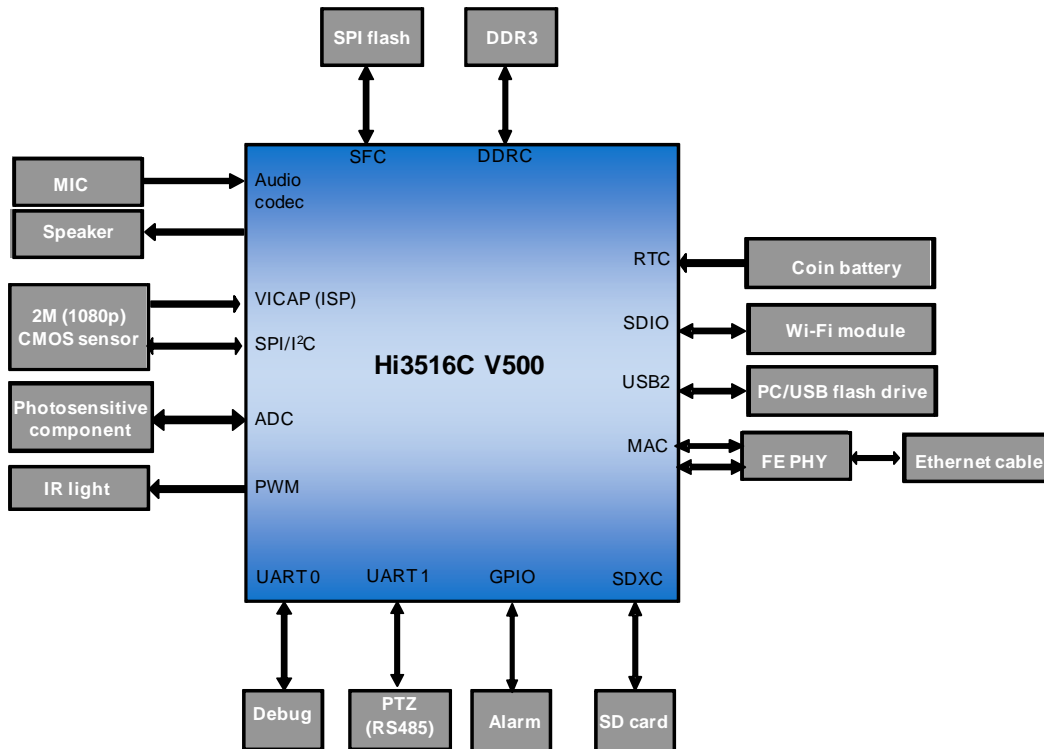


Hi3516C V500 is a new-generation SoC designed for the industry-dedicated smart HD IP camera. It introduces a new-generation ISP, the latest H.265 video compression encoder, and a high-performance NNIE engine, enabling Hi3516C V500 to lead the industry in terms of low bit rate, high image quality, intelligent processing and analysis, and low power consumption. Integrated with the POR, RTC, audio codec, and standby wakeup circuit, Hi3516C V500 can greatly reduce the EBOM costs for customers. Hi3516C V500 also provides similar interface designs to the HiSilicon DVR and NVR SoCs, facilitating rapid mass production.



Hi3516C V500 Professional Smart IP Camera SoC

Hi3516C V500 HD IP Camera Solution





Acronyms and Abbreviations

| | |
|------------------|---|
| 3DNR | three-dimensional noise reduction |
| 6DoF | six degrees of freedom |
| AE | automatic exposure |
| AEC | acoustic echo cancellation |
| AF | automatic focus |
| ALC | automatic level control |
| ANR | audio noise reduction |
| AVBR | adaptive variable bit rate |
| AWB | automatic white balance |
| CBR | constant bit rate |
| codec | coder/decoder |
| DC | digital camera |
| DCG | Dual Conversion Gain |
| DCI | dynamic contrast improvement |
| DDRC | double data rate controller |
| DPC | defect pixel correction |
| DVR | digital video recorder |
| EBOM | engineering bill of materials |
| ECC | error-correcting code |
| FPN | fixed pattern noise |
| I ² C | inter-integrated circuit |
| IR | infrared |
| LCD | liquid crystal display |
| LDC | lens distortion correction |
| LSADC | low-speed analog-to-digital converter |
| LSC | lens shading correction |
| NNIE | neural network inference engine |
| NR | noise reduction |
| NVR | network video recorder |
| OSD | on-screen display |
| OTP | one-time programming |
| POR | power-on reset |
| PWM | pulse-width modulation |
| RMII | reduced media-independent interface |
| ROI | region of interest |
| RTC | real-time clock |
| SDIO | secure digital input/output |
| SoC | system-on-chip |
| SPI | serial peripheral interface |
| TFBGA | thin & fine ball grid array |
| TOPS | tera operations per second |
| UART | universal asynchronous receiver transmitter |
| VBR | variable bit rate |
| VENC | video encoding |
| VI | video input |
| VO | video output |
| WDR | wide dynamic range |