Hi3519DV500 UHD Smart Vision SoC

Brief Data Sheet

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Hi3519DV500 UHD Smart Vision SoC

Overview

Hi3519DV500 is an ultra-HD (UHD) intelligent system-on-chip (SoC) tailored to the vision industry. This SoC provides up to four sensor inputs and optimum image processing capabilities, including 4K@30 fps image signal processing (ISP), AI-powered real-time noise reduction (NR), and a wide range of traditional image enhancement and processing algorithms, such as 2F wide dynamic range (WDR), multi-level NR, 6-DoF digital image stabilization (DIS), any view stitching (AVS), and Mono-Color-Fusion (MCF). It also allows for the access and processing of thermal infrared, structured-light, and time-of-flight (ToF) sensors.
Hi3519DV500 has a built-in quad-core Cortex-A55 processor, providing efficient, rich, and flexible CPU resources to meet customers' computing and control requirements.
Hi3519DV500 integrates an efficient neural network (NN) inference engine with up to 2.5 TOPS NN compute power, which supports mainstream NN frameworks.
With a stable and easy-to-use software development kit (SDK), Hi3519DV500 is set to facilitate mass production of customers' products.

Key Features

- Intelligent acceleration
  2.5 TOPS INT8 NN acceleration engine
- 4K@30 fps codec
  - H.265/H.264 encoding at 4K@30 fps
  - H.265/H.264 decoding at 4K@30 fps
- 2-channel 4M@30 fps video stitching
- 2-channel 4M@30 fps MCF
- AI ISP
- USB 3.0 high-speed peripheral interface
- Ultra-fast image generation in Linux (300 ms)

Hi3519DV500 UHD Smart Vision SoC

Key Characteristics

Processor Core

- Dual-core Arm Cortex-A55@1000 MHz
- 32 KB I-cache, 32 KB D-cache, and 256 KB L3 cache
- Neon acceleration and integrated floating-point unit (FPU)
- TrustZone

System-Level Acceleration Modules

- Hardware accelerated standard CRC32, CRC16, and CRC8 polynomial calculation unit
- Hardware accelerated high-speed direct memory access (DMA) module

Intelligent Video Analysis

- NN
  Complete APIs and toolchains
- Upgraded intelligent video engine (IVE) operators, including computer morphological operators for feature point detection, perimeters, optical flows, and more
- Upgraded depth processing unit (DPU) algorithm for the binocular depth image acceleration unit, supporting a resolution of up to 2048 x 2048 pixels, a parallax of up to 224 pixels, and 720p@30 fps processing performance

Video Codec

- H.264 Baseline Profile/Main Profile/High Profile Level 5.1
- H.265 Main Profile Level 5.1
- Up to 6144 x 6144 H.264/H.265 codec resolution
- I-frames and P-frames
- Typical performance of H.264/H.265 multi-stream codec:
  - 3840 x 2160@30 fps (encoding) + 1920 x 1080@30 fps (encoding) + 720 x 480@30 fps (encoding)
  - 3840 x 2160@30 fps (encoding) + 720 x 480@30 fps (encoding) + 1920 x 1080@30 fps (decoding)
  - 3840 x 2160@30 fps (decoding)
- On-screen display (OSD) overlay before encoding of eight regions
- CBR, VBR, AVBR, FixQp, and QpMap bit rate control modes
- Up to 80 Mbps output bit rate
- Encoding of eight regions of interest (ROIs)
- Mosaic encoding overlay on the video front end
- Digital watermark
- Perceptual video coding (PVC) for bitrate reduction
- JPEG baseline codec
- Up to 16384 x 16384 JPEG codec resolution
- Maximum JPEG performance:
  - Encoding: 3840 x 2160@60 fps (YUV420)
  - Decoding: 3840 x 2160@30 fps (YUV420)

ISP

- Synchronous processing of multiple sensors
- Adjustable 3A functions: automatic exposure (AE), automatic white balance (AWB), and automatic focus (AF)
- Fixed pattern noise (FPN)
- Defect pixel correction and lens shading correction
- 2-frame WDR, advanced local tone mapping, strong light suppression, and backlight compensation
- Multi-level three-dimensional noise reduction (3DNR)
- Image edge enhancement
- Dehaze
- Dynamic contrast improvement (DCI)
- 3D-LUT color adjustment
- Next-generation lens distortion correction
- Geometry correction of any shape such as fisheye
- 6-DoF DIS
- Gyro stabilization and rolling shutter correction
- Image mirroring, flipping, and rotation by 90 or 270 degrees
- NN-based real-time dynamic range

compression (DRC), Bayer noise reduction (BNR), 3DNR, or demosaicing (DM) processing on images
- Dual-light fusion of mono and color images
- ISP adjustment tool on the PC

Video and Graphics Processing

- Graphics and image scaling by 1/15.5x to 16x
- Horizontal AVS
  - Two 2560 x 1440@30 fps inputs and up to 5120 x 1440@30 fps or 2560 x 2880@30 fps output
  - Four 1920 x 1080@30 fps inputs and up to 6144 x 1080@30 fps or 1920 x 4320@30 fps output
- Overlaying of video and graphics layers
- Color space conversion (CSC)

Video Input Interfaces

- 8-lane image sensor serial inputs and multiple interfaces such as MIPI, LVDS, sub-LVDS, and HiSPI
- Multiple combinations such as 2x4-lane and 4x2-lane modes, and up to 4-sensor inputs
- 8-/10-/12-/14-bit RGB Bayer DC timing video input and up to 148.5 MHz clock frequency
- BT.601, BT.656, and BT.1120 video input interfaces
- One to four YUV inputs through the MIPI virtual channels
- Access of mainstream CMOS level thermal imaging sensors
- Structured light module
- Continuous-wave (CW) ToF image sensor

Video Output Interfaces

- One BT.1120 or BT.656 output interface with up to 1920 x 1080@60 fps for BT.1120
- 6-/8-bit serial output or 16-/18-/24-bit RGB parallel output with up to 74.25 MHz frequency
- 4-lane MIPI DSI/CSI output with up to 1.8 Gbps per lane and 3840 x 2160@30 fps
- Gamma correction and horizontal sharpening

Audio Interfaces and Processing

- Embedded audio codec, supporting 16-bit dual-channel differential voice inputs and dual-channel single-ended voice outputs
- One I^2S interface, compatible with the multi-channel time division multiplexing (TDM) transmission mode
- Eight digital mic array inputs
- Multi-protocol voice codec
- Audio 3A functions: AEC, ANR, and ALC

Security Isolation and Engines

- Secure boot
- REE and TEE hardware isolation based on TrustZone
- NN model and data protection
- Hardware-based AES128/256 symmetric encryption algorithms
- Hardware-based RSA3072/4096 signature verification algorithms
- Hardware-based ECC256/384/512 elliptic curve algorithms
- Hardware-based SHA-256/384/512 and HMAC_SHA256/384/512 algorithms
- Hardware-based SM2/3/4 Chinese cryptographic algorithms
- Hardware-based true random number generator (TRNG)
- 28-kbit one-time programming (OTP) storage space

Network Interface

- One GE interface:
  - RGMII and RMII modes
  - Acceleration units such as TCP segmentation offload (TSO), UDP fragmentation offload (UFO), and checksum offload engine (COE)

Peripheral Interfaces

- Two SDIO 3.0 interfaces
  - SDIO0 supports the secure digital extended capacity (SDXC) card with up to 2 TB storage.
  - SDIO1 supports the connection with a Wi-Fi module.

- One USB 3.0/USB 2.0 interface
  - USB host-device switchover
- Power-on reset (POR) and external input reset
- Real-time clock (RTC) with independent power supply
- Simplified power-on and power-off control logic for SoC standby wakeup
- 4-channel low-speed analog-to-digital converters (LSADCs)
- Three-wire control interface dedicated for RGB small-sized displays
- Multiple UART, I^2C, SPI, PWM, and GPIO interfaces

External Memory Interfaces

- DDR4, LPDDR4, and LPDDR4*x* interfaces
  - 2 x 16-bit DDR4
  - 1 x 32-bit LPDDR4 and LPDDR4*x*
  - Up to 2666 Mbps DDR4 rate
  - Up to 2933 Mbps LPDDR4 and LPDDR4*x* rate
  - Up to 4 GB storage
- SPI NOR and SPI NAND flash interfaces
  - 1-/2-/4-wire mode
  - 3-byte and 4-byte address modes for the SPI NOR flash
- eMMC 5.1 interface with up to 2 TB storage
- Booting from the eMMC, SPI NOR flash, or SPI NAND flash

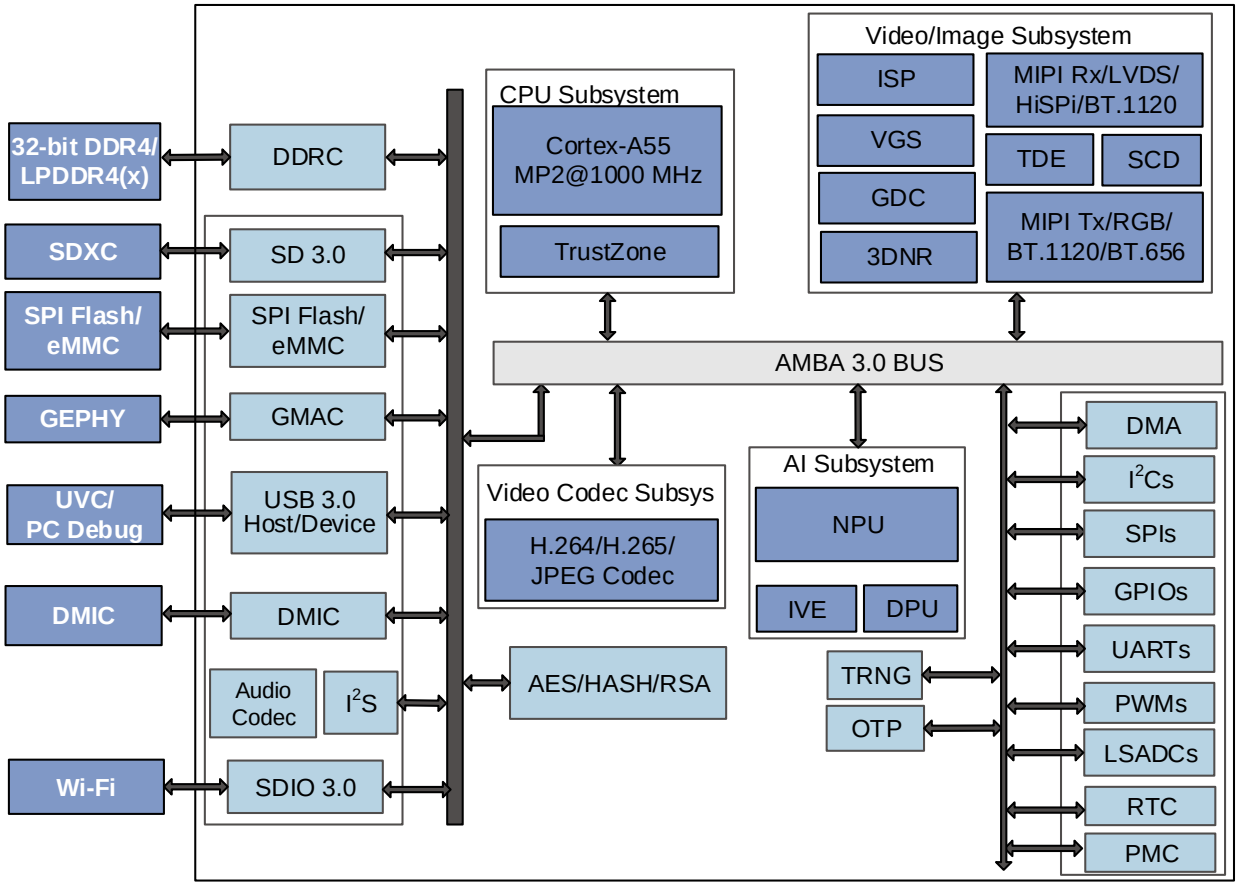
SDK

Linux 5.10 SDK

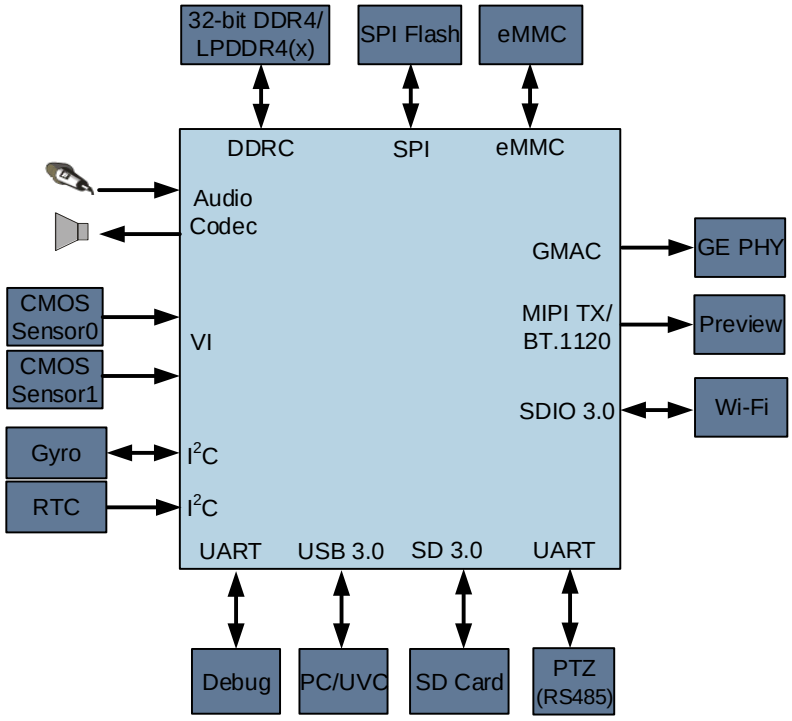
Physical Specifications

- Power consumption
  - 2.5 W typical power consumption (4Kp30 encoding + 2 TOPS)
- Operating voltage
  - Core voltage: 0.9 V
  - I/O voltage: 1.8 V or 3.3 V
  - DDR4, LPDDR4, and LPDDR4*x* interface voltages: 1.2 V, 1.1 V, and 0.6 V, respectively
- Package
  - RoHS, 15 mm x 15 mm FCCSP
  - 0.65 mm ball pitch

Functional Block Diagram



Hi3519DV500 UHD Smart Vision SoC Solution



Acronyms and Abbreviations

3DNR	three-dimensional noise reduction
AAC	advanced audio coding
AE	automatic exposure
AEC	acoustic echo control
AES	advanced encryption standard
AF	automatic focus
ALC	automatic level control
ANR	adaptive noise reduction
API	application programming interface
AVBR	adaptive variable bit rate
AVS	any view stitching
AWB	automatic white balance
CAC	chromatic aberration correction
CBR	constant bit rate
CMOS	complementary metal-oxide-semiconductor
CV	computer vision
codec	coder/decoder
COE	checksum offload engine
CSI	camera serial interface
DC	digital camera
DCI	dynamic contrast improvement
DDR	double data rate
DDRC	double data rate controller
DIS	digital image stabilization
DPU	depth processing unit
DSI	display serial interface

DSP	digital signal processor
DMIC	digital microphone
DMA	direct memory access
ECC	error-correcting code
eMMC	embedded multimedia card
EP	endpoint
FCCSP	flip-chip chip scale package
FPN	fixed pattern noise
FPU	floating-point unit
GE	gigabit Ethernet
GMAC	Gigabit Ethernet Media Access Controller
GPIO	general-purpose input/output
GUI	graphical user interface
HD	high definition
HiSPI	high-speed serial pixel interface
I^2C	inter-integrated circuit
I^2S	inter-IC sound
ISP	image signal processor
IVE	intelligent video engine
LCD	liquid crystal display
LGDC	lens geometric distortion correction
LPDDR	low-power double data rate
LSADC	low-speed analog-to-digital converter
LUT	lookup table
LVDS	low-voltage differential signaling
MAU	matrix arithmetic unit
MCU	microcontroller unit
mic	microphone

MIPI	mobile industry processor interface
NR	noise reduction
OSD	on-screen display
OTP	one-time programming
PIP	picture-in-picture
POR	power-on reset
PWM	pulse-width modulation
RAM	random access memory
RC	root complex
PMC	power management controller
RGB	red-green-blue
RGMII	reduced gigabit media-independent interface
RMII	reduced media-independent interface
RoHS	restriction of hazardous substances
ROI	region of interest
RSA	Rivest-Shamir-Adleman
RNG	random number generator
RTC	real-time clock
SD	secure digital
SDIO	secure digital input/output
SDK	software development kit
SDRAM	synchronous dynamic random access memory
SDXC	secure digital extended capacity
SMP	symmetric multiprocessing
SoC	system-on-chip
SPI	serial peripheral interface
SCD	start code detect
TDM	time division multiplexing

TOPS	Tera Operations Per Second
TSO	TCP segmentation offload
TX	transmit
UART	universal asynchronous receiver transmitter
USB	Universal Serial Bus
UFO	UDP fragmentation offload
VBR	variable bit rate
VI	video input
VO	video output
VQE	voice quality enhancement
WDR	wide dynamic range

