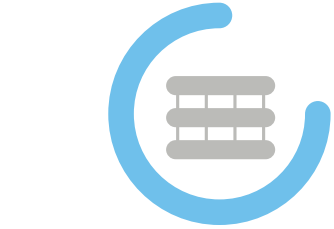

Meeting of the Technical Steering Committee (TSC) Board

Wednesday, May 3rd, 2023
11:00am ET

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Agenda/Updates

- Announcements, upcoming talks and deadlines
  - ISC BoF scheduled for Monday, May 22nd 4 PM (Europe/Berlin)
    - Chris S., Adrian, and David
  - PEARC BoF deadline May 12th
    - Chris S., Jeremy
    - Anyone else going to PEARC?
  - SC BoF deadline Jul 7th
    - Who is planning to attend?

- Release updates

Release Updates and Discussion

- should we enable -march=x86-64-v2 also for the Intel compiler

In the summer of 2020, AMD, Intel, Red Hat, and SUSE collaborated to define three x86-64 microarchitecture levels on top of the x86-64 baseline. The three microarchitectures group together CPU features roughly based on hardware release dates:

- **x86-64-v2** brings support (among other things) for vector instructions up to Streaming SIMD Extensions 4.2 (SSE4.2) and Supplemental Streaming SIMD Extensions 3 (SSSE3), the POPCNT instruction (useful for data analysis and bit-fiddling in some data structures), and CMPXCHG16B (a two-word compare-and-swap instruction useful for concurrent algorithms).
- **x86-64-v3** adds vector instructions up to AVX2, MOVBE (for big-endian data access), and additional bit-manipulation instructions.
- **x86-64-v4** includes vector instructions from some of the AVX-512 variants.

- should we release GCC 13 with 3.0?
- Warewulf3 and SUSE Leap 15.3 issues