Simulation results: The circuit has been simulated on HSPICE with a 0.8μm CMOS process. The transconductance gm_1 is fixed at 200ns. Fig. 4 shows the frequency response of the resonator at resonant frequency 100Hz, where I_3, I_4, I_5, I_7, I_9, I_{10} are set to 1nA and I_1, I_2, I_6 are set to 20nA. The Q-factor of the resonator is 100 and 1000 at the I_q of 100 and 600pA, respectively. At resonant frequency 10 kHz, where I_3, I_4, I_5, I_7, I_9, I_{10} are set to 10nA and I_1, I_2, I_6 are set to 20nA, the Q-factors are 30 and 550 at the I_q of 1nA and 2.5nA, respectively. At f_c = 10kHz the power consumption is ~0.6μW, with a 3.3V power supply. What is significant is that the f_oQ product of 5MHz is in fact the f_t of the weak inversion MOSFET. Since the integration function within the inductor is based on a log-domain integrator, this not only introduces new design issues for active inductor realisation but lends itself quite elegantly to high order filter synthesis in the micropower weak inversion region of the MOSFET using the more advanced LCR signal flow graph methods, as opposed to the state-space realisations given in [1, 3].

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N-folded cascode technique for high frequency operation of low voltage opamps

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Indexing terms: Operational amplifiers, Analogue circuits

A technique is described which enhances the high frequency operation of a low voltage folded cascode structure by introducing a zero at the nondominant pole position and providing phase compensation. This technique can be used to develop low voltage operational amplifiers with good gain bandwidth properties and no overhead in power consumption.

Limitations of the standard folded cascode structure: The architecture for a typical n-type folded cascode structure is shown in Fig. 1*a* and its small signal equivalent circuit in Fig. 1*b* using standard nomenclature. Analysis of the small signal operation of this structure with a compensation load capacitance, C_L is carried out. Using reasonable assumptions, that $C_L \gg Cgd_2$, $Cgs_2 \gg Cgd_1$ and $gm_2ro_2 \gg 1$

$$\frac{V_o}{V_{in}} = \frac{\frac{gm_2Cgd_1}{C_LCgs_2}\left(s - \frac{gm_1}{Cgd_1}\right)}{s^2 + s\left(\frac{gm_2}{Cgs_2}\right) + \frac{1}{ro_2ro_1C_LCgs_2}} \quad (1)$$

Eqn. 1 yields a two pole, one zero transfer function where the dominant pole (p_1), nondominant pole (p_2) and zero (z_1) are given by

$$p_1 = -\frac{1}{gm_2ro_2ro_1C_L} \quad p_2 = -\frac{gm_2}{Cgs_2} \quad z_1 = +\frac{gm_1}{Cgd_1}$$

The nondominant pole is determined by the cascode transistor M2. To obtain good phase margin the nondominant pole p_2 should be about two to three times larger than the dominant pole p_1. In general, good high frequency performance is obtained by making p_2 as large as possible. This suggests that gm_2 should be increased, and this can be achieved by increasing the (W/L) ratio of the transistor M2. If minimum sized devices are already being utilised, this means that an increase in the width W is required.

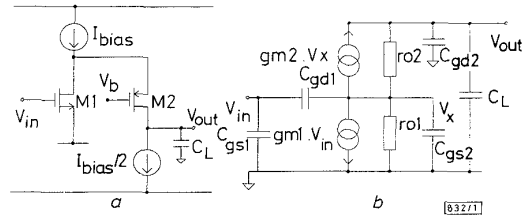

Fig. 1 *Standard folded cascode structure with small signal equivalent circuit*

a N-folded cascode structure (N = 1); *b* small signal equivalent circuit

However, doing this also causes a corresponding increase in the Cgs, which results in no overall change of p_2. Alternatively the bias current flowing through the transistor M2,could be increased, but this increases the power consumption. Therefore it can be seen that there is an upper limit for the value of the nondominant pole, which tends to naturally be at lower frequencies when designing for low supply voltages.

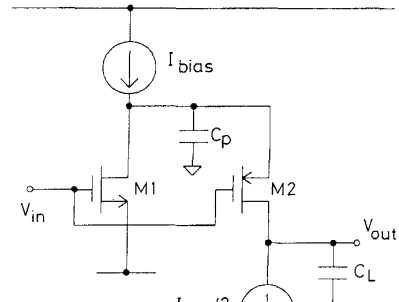

Fig. 2 *Folded cascode structure with feedforward N = 1*

Folded cascode structure with the feedforward connection: A modification is now made to the circuit of Fig. 1. The actual input signal is connected directly to the gate of the folded cascode device M2 as shown in Fig. 2. The capacitor C_p is connected from the parasitic node to ground, and its function will become apparent later. Performing an analysis on the small signal operation of this circuit yields the following:

$$\frac{V_o}{V_{in}} = \frac{\frac{Cgd_2}{(C_L+Cgd_2)}\left(s^2 + s\left(\frac{gm_2(Cgd_2-C_p)}{Cgd_2(Cgs_2+C_p)}\right) - \frac{gm_1gm_2}{(Cgs_2+C_p)Cgd_2}\right)}{s^2 + s\left(\frac{gm_2}{Cgs_2+C_p}\right) + \frac{1}{ro_2ro_1(Cgs_2+C_p)(C_L+Cgd_2)}} \quad (2)$$

Without C_p included in the circuit the following poles and zeros would be obtained: one left hand plane zero, z_1, one right hand plane zero, z_2 and two left hand plane poles p_1, the dominant pole and p_2, the nondominant pole):

$$p_1 = -\frac{1}{gm_2 ro_2 ro_1 C_L} \quad p_2 = -\frac{gm_2}{Cgs_2}$$
$$z_1 = -\frac{gm_1}{Cgd_2} \quad z_2 = +\frac{gm_2}{Cgd_2}$$

The cancellation of the nondominant pole as required is not obtained, and in fact the amplifier will probably now be unstable due to the lowering of the right-hand plane zero. If, however, Cp is included the full transfer function, eqn. 2 is valid. If $Cp \gg Cgs_2$ and Cgd_2 the coefficient of the s in the numerator changes from being positive to being negative. This results in the right hand plane zero now occurring at higher frequencies and the left hand plane zero occurring at a frequency very close to that of the nondominant pole such that cancellation can occur. The pole and zero values can be calculated to be:

$$p_1 = -\frac{1}{gm_2 ro_2 ro_1 C_L} \quad p_2 = -\frac{gm_2}{C_p + Cgs_2}$$
$$z_1 = -\frac{gm_1}{C_p - Cgd_2} \quad z_2 = +\frac{gm_2(C_p - Cgd_2)}{Cgd_2(C_p + Cgs_2)}$$

The optimum positions of the poles and zeros basically occur when the nondominant pole and left-hand plane zero cancel exactly, and to obtain this exact cancellation the following expression must be satisfied:

$$\frac{gm_2}{C_p + Cgs_2} = \frac{gm_1}{C_p - Cgd_2} \text{ or } C_p = \frac{gm_1 Cgs_2 + gm_2 Cgd_2}{gm_2 - gm_1} \quad (3)$$

From eqn. 3 it can be seen that gm_2 must be greater than gm_1, i.e. the folded cascode transistor must have larger transconductance than the input transistor. Another point to bear in mind is the requirement that $C_p \gg Cgs$ and Cgd and as such it must be ensured that $(gm_2 - gm_1)$ is small enough to achieve this.

From the transfer function expression and the poles and zeros derived from it, it can be seen that, if no load capacitance is used, the first pole will now have the following value: $-(1/(gm_2 ro_2 ro_1 Cgd_2))$. This indicates that this first pole has moved to higher frequencies. Since it is still lower in value compared to the other poles, the calculated pole positions of p_2 and p_3 are still valid. For a standard single stage folded cascode amplifier the load capacitance acts as a compensation capacitor by lowering the GBW and improving the phase margin. In general, if the load capacitance is not included the phase margin becomes unacceptable, i.e. below 45 degrees. However, with the feedforward method described here, the load capacitance at the output is not required to keep the phase margin satisfactory, and so an amplifier operating at several hundred MHz GBW frequencies can be obtained without sacrificing the phase margin.

One problem associated with the occurrence of a pole zero doublet is a slow settling component [1]. With careful design, the pole and zero need to be situated to be as close as possible such that the slow settling component acts only over a small amplitude.

The feedforward technique lends itself to the low supply voltage folded cascode structure since the DC bias voltage required at the gate of the cascode transistor is similar in value to that of the input transistor, i.e. midway between the positive and negative power supply voltages, thus allowing connection of the gates of these two transistors.

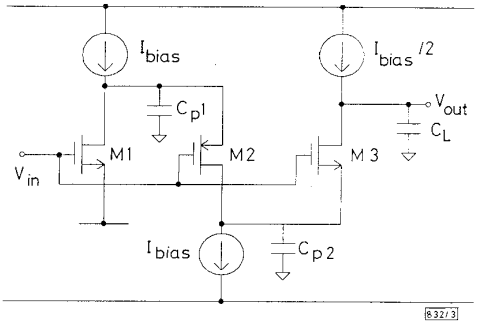

Fig. 3 *Double folded cascode structure with feedforward N = 2*

Double folded cascode structure with feedforward connection: To reduce the output conductance a second cascode device can be included, resulting in a double folded cascode structure as indicated by Fig. 3. The input signal is now fed forward to the gates of both cascode devices and a second capacitance C_{p2} is added to the new parasitic node that has been introduced. The open loop gain is now of the order of $(gm.ro)^3$. Analysis of the circuit of Fig. 3 results in a three zero and three pole solution: a low frequency dominant pole, a high frequency right-hand plane zero and two left-hand plane poles and zeros which can be designed such that they cancel. Theoretically it is possible to continue adding more folded cascode devices to the structure and feeding the input signal forward to create an extra pole zero pair to be cancelled. However, Fig. 3 is probably a sensible limit to the structure.

Simulation results: The circuits were designed using a 0.8μm CMOS technology, which forms part of a Northern Telecom BiCMOS technology and is simulated in HSPICE.

Results obtained are for two folded cascode operational amplifiers which were simulated with and without the feedforward connection to the cascode transistors. The opamp architectures were based on the standard single stage, differential input amplifier of [2]. The supply voltages for both these amplifiers was set to ±1.25V.

Table 1: Summary of simulation results obtained for standard folded cascode with and without feedforward and double folded cascode with feedforward, with supply voltages of ±1.25V

Performance	Load	Gain	GBW product	Phase
	pF	dB	MHz	deg
Single folded cascode without feedforward	10	54.4	63	74
Single folded cascode without feedforward	0	54.4	500	34
Single folded cascode with feedforward	10	55	65	88
Single folded cascode with feedforward	0	55	700	80
Double folded cascode with feedforward	10	79.7	30	86
Double folded cascode with feedforward	0	79.7	500	81

Table 1 gives a summary of the magnitude and phase results of the amplifier with and without a load capacitance of 10pF, with and without the feedforward connection. It can be seen that on addition of the feedforward connection, the amplifiers' open loop gain and GBW products increase, but more importantly, for both cases (with and without load capacitance) the phase margin increases by a large amount. A GBW product of 700MHz can be achieved while maintaining a phase margin of 80°. A voltage gain of 80dB is achieved for the double folded cascode amplifier whilst it still maintains excellent phase margin, 81°, at a GBW product of 500MHz. This structure should find widespread use in low voltage portable applications.

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Simple 4D chaotic oscillator

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Indexing terms: Chaos, Oscillators

An extremely simple 4-D chaotic oscillator is presented. It contains a single opamp, two *LC* circuits and a diode used as a nonlinear device. The chaotic oscillations have been characterised using the correlation dimension of the strange attractor, the Lyapunov exponents and the Lyapunov dimension. The dimensions are found to be >3.

Introduction: Over the past decade a variety of electronic circuits exhibiting chaotic behaviour have been described in the literature; see, for example [1 – 9] and references therein. Most of them are 3-D systems. In other words, the number of degrees of freedom in these systems is $N = 3$. The dimension N of a system should not be confused with the dimension of an underlying attractor d, which is usually a fractal quantity and is typically $<N$, say $2 < d < 3$ in a 3-D system. Only a few of the described circuits are the higher-dimensional ones [7 – 9], e.g. a 4-D oscillator with $d = 3.006$ [7], a 4-D oscillator with $2 \leq d \leq 2.5$ [8], and an infinite dimensional oscillator, namely a delay line based circuit [9], characterised by the dimension of the attractor ranging up to $d \simeq 7$.

In this Letter we propose an extremely simple 4-D chaotic oscillator with the dimension of the attractor $d > 3$.

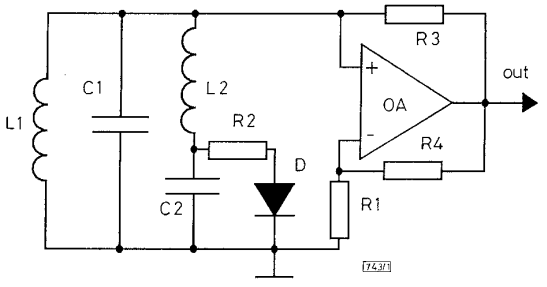

Fig. 1 *4D chaotic oscillator*

Circuit description: The suggested oscillator (Fig. 1) includes a combined parallel-series *LC* circuit, L1C1-L2C2. The opamp OA with the resistors R1, R3 and R4 plays the role of both the negative impedance converter (NIC) and the output amplifier. For $R_3 = R_4$ the input impedance Z of the NIC is simply $Z = -R_1$. The output voltage is $U_{out} = kU_{C1}$, where the gain $k = R_4/R_1+1$. The opamp operates in the linear region. The only nonlinearity is involved by the diode. We note that, for $C_2 = 0$, the circuit in Fig. 1 reduces in a sense to the 3-D chaotic oscillator described in [3] and characterised by $d \simeq 2$.

The oscillator in Fig. 1 is described by the set of equations:

$$\begin{aligned} C_1\frac{dU_{C1}}{dt} &= \frac{U_{C1}}{R_1} - I_{L1} - I_{L2} \\ L_1\frac{dI_{L1}}{dt} &= U_{C1} \\ L_2\frac{dI_{L2}}{dt} &= U_{C1} - U_{C2} \\ C_2\frac{dU_{C2}}{dt} &= I_{L2} - \frac{U_{C2} - U_0}{R_2}H(U_{C2} - U_0) \end{aligned} \tag{1}$$

Here U_0 is the forward voltage drop of the diode, and $H(u)$ is the Heaviside function, that is $H(u<0) = 0$ and $H(u\geq 0) = 1$.

Introducing the following notations:

$$\begin{aligned} &U_{C1}/U_0 = x, \quad \rho I_{L1}/U_0 = y, \quad \rho I_{L2}/U_0 = z \\ &U_{C2}/U_0 = v, \quad t/\tau = \theta, \quad \rho = \sqrt{L_1/C_1}, \quad \tau = \sqrt{L_1C_1} \\ &a = \rho/R_1, \quad b = \rho/R_2, \quad c = L_1/L_2, \quad e = C_1/C_2 \end{aligned} \tag{2}$$

also $\dot{u} \equiv du/d\theta$ one comes to:

$$\begin{aligned} \dot{x} &= ax - y - z \\ \dot{y} &= x \\ \dot{z} &= c(x - v) \\ \dot{v} &= e[z - b(v-1)H(v-1)] \end{aligned} \tag{3}$$

Simulation results: Eqn. 3 has been integrated numerically and the typical results are presented in Figs. 2 and 3.

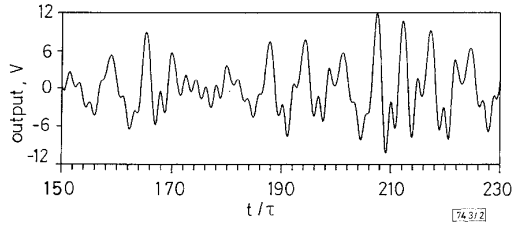

Fig. 2 *Typical output waveform at $a = 0.7$, $b = 10$, $c = e = 3$, $U_{out} = kU_{C1}$, $k = 5$, $U_{C1} = xU_0$, $U_0 = 0.7V$*

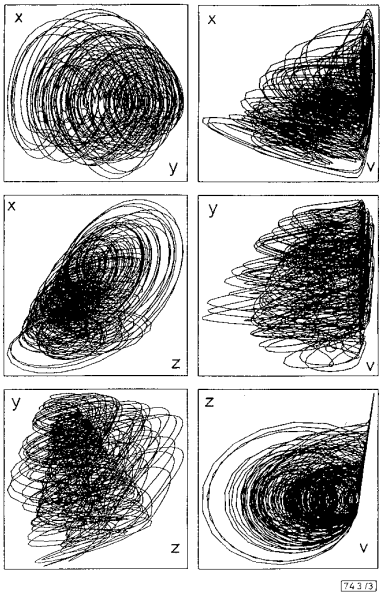

Fig. 3 *Typical phase portraits at $a = 0.7$, $b = 10$, $c = e = 3$*

Similar chaotic behaviour has been observed over a wide parameter range: $0.25 \leq a \leq 0.8$, $4 \leq b \leq 40$, $3 \leq c \leq 5$, $3 \leq e \leq 7$. The complex structure of the phase portraits is a characteristic feature of the higher dimensional chaotic systems [7].

For the quantitative characterisation of the oscillations, the correlation dimension of the attractor [10] and the Lyapunov exponents [11] have been estimated.

From $x(t)$ the discrete time series $\{x(ih)\}$, $i = 1, ..., n$, was obtained. Using the delayed co-ordinates $x_{im} = x[ih-(m-1)T_d]$ the m-dimensional vector $\vec{x}_i = \{x_{i1}, x_{i2}, ..., x_{im}\}$ was constructed. We chose $T_d = h = 1$. Further, the so called correlation integral [10] $J_m(r) = \Sigma_{i\neq j} H(r-|\vec{x}_i - \vec{x}_j|)$ was computed. At small r it scales as $r^{d(m)}$. For sufficiently large embedding dimension m the correlation exponent $d(m)$ saturates just to the correlation dimension d_{cor}. Along with the computed Lyapunov exponents λ_i we have calculated the Lyapunov dimension d_L using the Kaplan-Yorke formula [10]: $d_L = j + \Sigma^j_{i=1}\lambda_i/|\lambda_{j+1}|$, where j is the largest integer for which the sum in the numerator is positive. The summary results are shown in Table 1.