A Self Biased Operational Amplifier at Ultra Low Power Supply Voltage

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***Abstract*—This paper discusses the design of a self-biased folded cascode operational amplifier at an ultra low power supply voltage. The proposed design is first of its kind at 0.5 V where self-biasing techniques are used to reduce power and area overheads. The self-biasing scheme in this design is developed by using a current mirror for low voltage operation. This design is implemented in a 90 nm CMOS technology using Cadence General Purpose Design Kit (GPDK).**

I. INTRODUCTION

Modern wireless communication and biomedical applications require analog circuits with low power operation [1] [2]. One of the main analog building blocks, which needs to be designed for such applications is operational amplifier. One way to reduce the power consumption of operational amplifiers is use the self - biasing technique. This technique eliminates the external biasing circuitry by generating bias voltages from the internal nodes of the circuit and the two power supply rails and was first proposed in [3]. Using this technique a complementary folded cascode amplifier has been proposed which eliminates nine bias voltages [4]. This design has been improved in [5] by using a low voltage cascode current mirror to implement self - biasing. In this paper, further improvement to the op-amp proposed in [5] has been done to operate it at a power supply voltage 0.5 volts. Fig. 1 shows the design proposed in [5]. In this design transistors M_4, M_6, M_8 and M_{10} are connected in a low voltage cascode current mirror configuration. By virtue of these diode connections differential to single ended conversion of the input signal is performed. Low voltage current mirror techniques have been proposed in [6] which can be used in low voltage analog circuits. This current mirror makes a wise use of the PMOS transistor to bring the V_{ds} of NMOS near to $V_{ds,\ sat}$ and vice versa, which is required for low voltage operation. In this paper, a new self-biasing scheme is developed by combining a standard low voltage current mirror and the Rajput-Jamuar current mirror structures [6]. This self-biasing scheme is tolerant to process and temperature variations and bias voltages are less susceptible to noise and cross talk, which is very important to designs implemented in deep submicron CMOS technologies.

II. CIRCUIT DESIGN

In Fig. 1, the transistors M_4 and M_{10} are biased by connecting their gates to the drains of M_6 and M_8. In our design, transistors M_4 and M_{10} are biased by using current mirror in Fig. 2.

A. Implementation

Fig. 3 shows the proposed circuit. In this circuit, M_4 is biased using M_{12} and M_{10} is biased using M_{14}. The transistors M_{12} and M_{14} operate in the moderate inversion region. However, the transistors M_6 and M_8 are biased in the same way as shown in Fig. 1.

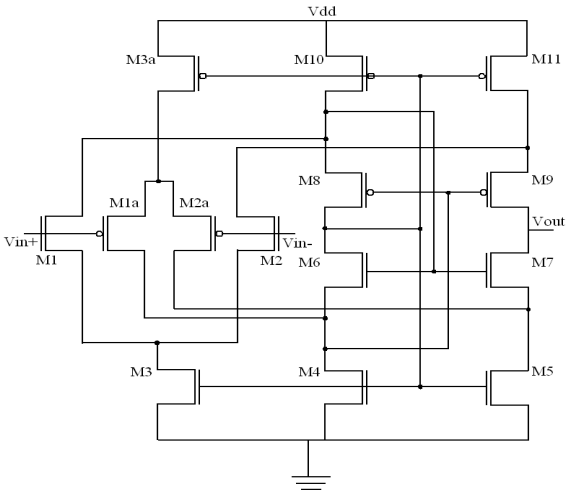

Figure 1. A Low Voltage Self-Biased Complementary Folded Cascode Amplifier

The current mirror shown in Fig. 2 is used to bias M_4 and M_{10}. The basic idea behind using this current mirror is to perform voltage level shifting. In Fig. 2 M_3 serves the purpose of fixing the drain voltage of M_1. I_{in} fixes the value V_{gs1} and thus the voltage at source terminal of M_3 is fixed. Since I_{bias} is known, V_{gs3} is also fixed. In this way, for a given value of I_{in}, varying I_{bias} can control V_{ds1} ie. $V_{ds1} = V_{gs1} - V_{gs3}$.

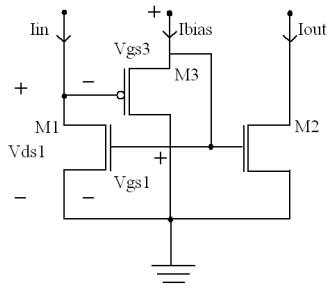

Figure 2. A Rajput-Jamuar Level Shifted Current Mirror

This current mirror enables the circuit to operate at low voltage. Moreover, the design in Fig. 1 has two diode-like connections in the current mirror. This reduces the tolerance of the circuit to variations. However, in our design due the use of an alternative current mirroring scheme the diode like connections in the op-amp are reduced ie. gate terminals of M_4 and M_{10} are free and the feedback network complexity is reduced. Hence, voltage changes at this terminal would not appear at the gates of other transistors. Thus, our op-amp is relatively more robust to variations. Also, the use of Rajput-Jamuar current mirrors gives more control over V_{gs} of M_6 and M_8 as their gate voltages can be fixed by varying the W/L's of M_{12} and M_{14}.

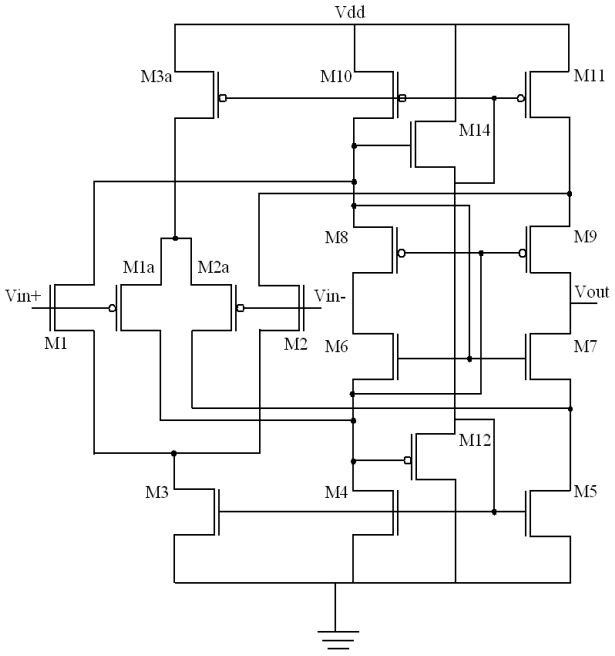

Figure 3. Proposed Design

The purpose of transistors M_{12} and M_{14} is to rigidly fix the gate voltage of M_4 and M_{10} and to ensure that V_{ds} of the transistors is less, which improves the output swing. M_{12} and M_{14} actually require a bias current for their operation but in this case they are stacked so that no separate bias current sources are required. In this way the power consumption of the circuit is reduced. A fully differential two stage folded cascode OTA has been proposed in [7] which uses two common mode feedback (CMFB) loops for fixing the output DC voltage.

TABLE I
COMPARISON WITH LOW VOLTAGE OP-AMPS

Parameter	Ext. Biased 2 Stage OTA [7]	0.5 V Bulk OTA [8]	Improved Self Biased [5]	Proposed Op Amp
Supply Voltage (V)	0.5	0.5	1.8	0.5
DC Gain (dB)	50	52	80.8	41.7
Power Consumption (μW)	265	110	240	70
UGF (MHz)	32	2.5	6.9	56
Load Capacitor (pF)	3	20	20	3
Output Swing (mV)	200	160	1400	160
Settling Time (nsec)	-	-	460	37
Slew Rate (V/μsec)	-	-	2.2	72.9
PSRR (@ 1 MHz)	-	43	42.3	67.3
Technology (μm)	0.09	0.18	0.6	0.09

However, in the proposed op-amp there is no need of CMFB due to the use of self-biasing technique. The self-biasing technique can only be used for differential to single-ended topologies where CMFB is not required. The V_{ds} of the transistors are also fixed in this design by virtue of the diode like connections and Rajput-Jamuar current mirror. The use of this current mirror also makes the operating point more tolerant to process and temperature variations. The threshold voltages of the input transistors are reduced by using an effect called as RSCE (Reverse Short Channel Effect) where the lengths are increased [7]. Hence, the op-amp has rail-to-rail input common mode range. The output DC voltage is set to $V_{dd}/2$ to get maximum output signal swings in both positive and negative half cycles.

B. Design Procedure

A nominal 120 mV V_{ds} has been allocated to each of the transistors for 0.5 V power supply voltage. Based on this the V_{gs} of all the transistors has been obtained and their drain current values were fixed. Using this information and the I_d vs. V_{gs} plots for NMOS and PMOS, the W/L values of the transistors were calculated and the circuit had been simulated.

TABLE 2
W/L'S OF TRANSISTORS

Devices	W/L (μM)
M_1, M_{1a}	41.72/0.36
M_2, M_{2a}	16.86/0.36
M_3	75/0.36
M_{3a}	33.72/0.36
M_4, M_5	27.77/0.36
M_6, M_7	11.125/0.36
M_8, M_9	21/0.36
M_{10}, M_{11}	78.3/0.36
M_{12}	16.17/0.36
M_{14}	36/0.36

III. SIMULATION RESULTS

The op-amp has been simulated using Spectre to predict its performance with respect to various parameters. Table I depicts the comparison of the proposed design with the measured results of other op-amps. Our design has a considerably low power consumption and high PSRR and bandwidth when compared to the other designs. However, the gain of the op-amp is less, which can be improved by adding gain stages.

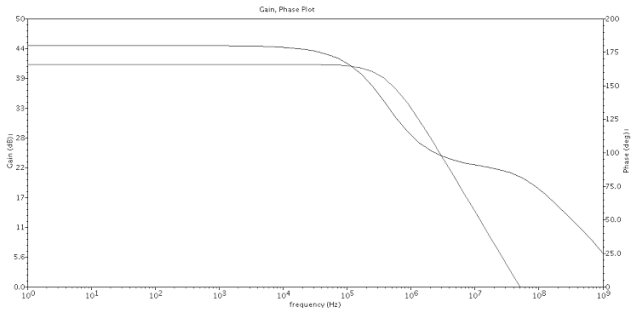

Figure 4. Bode and phase plots of our op-amp

IV. CONCLUSIONS

This paper discussed the design of a self-biased op-amp at 0.5 V in a 90 nm CMOS technology using a modified current mirror. A new self-biasing scheme has been proposed which combines a standard low voltage cascode current mirror with Rajput-Jamuar current mirror. The use of this current mirror makes the design less susceptible to process and temperature variations. It has been shown that the proposed op-amp consumes considerably low power and yet provides high bandwidth when compared to the other designs.

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