Adaptive Biasing CMOS Amplifiers

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Abstract—Two transconductance amplifiers are presented in which the concept of an input dependent bias current has been introduced. As a result, these amplifiers combine a very low standby power dissipation with a high driving capability. The first amplifier, suited for SC filters, is fairly small (0.075 mm^2) and has a slew rate which is more than an order of magnitude better than micropower amplifiers presented earlier. The second amplifier can be used as a micropower buffer. Nearly the whole supply current is used to charge the load capacitor so that this amplifier has a high efficiency.

I. Introduction

In recent years much effort has been made to reduce the power dissipation of amplifiers. The reported micropower amplifiers using classical schemes [1]-[3] have good small signal characteristics but their slew rate is too small for many applications. Therefore, dynamic amplifiers were introduced. Some of them [4]-[6] are based on a simple inverter. They are not generally applicable since they are not differential. Other dynamic amplifiers [5] are based on classical op amp schemes where the tail current source was replaced by a pulsed current source.

This paper presents two amplifiers, the bias current of which is made signal dependent so that the power consumption is reduced further.

Section II describes the characteristics of a basic transconductance amplifier (OTA) on which the adaptive biasing amplifiers are based. In Sections III and IV these amplifiers are described and experimental results are given.

II. The Transconductance Amplifier and Its Limitations

The transconductance amplifier (presented in Fig. 1) consists of a differential input stage and a double to single ended output stage.

This OTA has two important poles: the dominant pole, formed by the high output impedance and a load capacitor, and the second pole formed by the transconductance of the load transistors of the input stage and the internal capacitors. The ratio between the two poles is mainly determined by the capacitive load and the ratio of the currents in the first and second stage. As will be discussed below, in order to obtain enough phase margin for small capacitive loads this current ratio should be close to unity.

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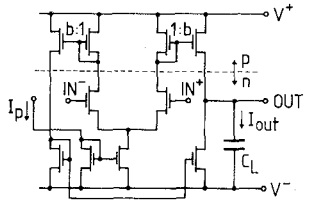

Fig. 1. Basic transconductance amplifier.

The gain-bandwidth product (GBW) of the amplifier is given by (1), where g_m is the sum of the transconductances of the input transistors, b is the ratio between the current in the second and the first stage, and C_1 is the load capacitor

$$\text{GBW} = g_m \cdot b/4 \cdot \pi \cdot C_1. \tag{1}$$

When the input transistors are operating in the weak inversion region the largest transconductance for a given current is reached [7]. Under these conditions the maximum achievable GBW for a given current is obtained as well as the maximum possible gain [1]. The GBW is then given by (2)

$$\text{GBW} = b \cdot I_p/(n \cdot 4 \cdot \pi \cdot C_1 \cdot V_T) \tag{2}$$

where n = slope factor in weak inversion

$$V_T = k \cdot T/q.$$

The slew rate (SR) of the amplifier is given by (3)

$$\text{SR} = b \cdot I_p/C_1. \tag{3}$$

By eliminating the current from (2) and (3), the relationship between SR and GBW is obtained in (4). An amplifier with a GBW of 500 kHz will thus have a slew rate of only 300 mV/μs

$$\text{SR} = 4 \cdot \pi \cdot n \cdot V_T \cdot \text{GBW} \cong 600\ \text{mV} \cdot \text{GBW}. \tag{4}$$

This means that the amplifier cannot handle large signals as fast as small signals.

Note that (4) has also been given by Solomon [8] for bipolar amplifiers where $n = 1$. To increase the slew rate in those amplifiers, and keeping the GBW constant, the g_m/I_p ratio is decreased [9], [10]. In MOS amplifiers this can easily be done by using the input transistors in strong inversion. However, this solution is not satisfactory for micropower applications where one wants to have the maximum GBW with the minimal possible current.

Since the slew rate is caused by the fact that the tail current source is limited, the slew rate can be improved by using a tail current source, the current of which increases as the disturbance of the virtual ground becomes larger. This principle

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then leads to the so-called adaptive biasing amplifier of which two possible realizations are discussed in Sections III and IV.

III. Differential Feedback Amplifier

A. Principle

When a voltage is applied across the inputs of the OTA (Fig. 1) the currents I_1 and I_2 become different. The bias current of the amplifier is made signal dependent by adding an additional current source to the main tail current source which realizes $A \cdot |I_1 - I_2|$. "A" will be called the current feedback factor. The additional current source is realized by two subtractors (Fig. 2).

Only if I_2 becomes larger than I_1, will the subtractor draw a current $A \cdot (I_2 - I_1)$. Otherwise the subtractor keeps drawing zero current.

By putting the subtractors in the scheme of the simple OTA, where the currents at the inputs of the subtractors are provided by means of current mirrors, we obtain the circuit in Fig. 3, which we define as a differential feedback amplifier.

If there is no disturbance at the virtual ground, the currents I_1 and I_2 are equal and the total bias current is thus I_p. When a signal is applied, the total bias current will be $I_p + A \cdot |I_1 - I_2|$.

B. Available Output Current

By using the current formula for the weak inversion region proposed by Vittoz and Fellrath [11] and by applying Kirchhoff's current law, (5) and (6) can be derived. V_{in} is the voltage across the inputs of the amplifier ($V_{in} = V_{in}^+ - V_{in}^-$).

$$I_1 = I_2 \cdot \exp(V_{in}/(n \cdot V_T)) \tag{5}$$

$$I_1 = \frac{I_p \cdot \exp(V_{in}/(n \cdot V_T))}{(A+1) - (A-1) \cdot \exp(V_{in}/(n \cdot V_T))}. \tag{6}$$

The current flowing in the load capacitor (I_{out}) is b times the difference between I_1 and I_2. This current can be calculated from (5) and (6) and is given in (7)

$$I_{out} = \frac{I_p \cdot (\exp(V_{in}/(n \cdot V_T)) - 1)}{(A+1) - (A-1) \cdot \exp(V_{in}/(n \cdot V_T))} \cdot b. \tag{7}$$

Fig. 4 shows the ratio I_{out}/I_p as a function of $V_{in}/(n \cdot V_T) \cdot (b = 1)$ for different current feedback factors. In Fig. 4 A equals zero represents the case of the simple OTA. The load current cannot become larger than I_p and thus the amplifier will slew for large input steps. For A between 0 and 1, the maximum possible output current is limited to the value of $I_p/(1 - A)$. For a current feedback factor of 0.9 the slew rate improves by a factor 10. If A is larger than unity the maximum load current becomes unlimited, so that the amplifier will never slew. The output current tends to infinity for a well-known value of the input signal. This voltage will be called the escape voltage and is given in (8).

$$V_{escape} = n \cdot V_T \cdot \ln((A+1)/(A-1)). \tag{8}$$

The current, of course, will not reach infinity. The input transistors will leave the weak inversion region and (7) is no longer valid. The maximum possible output current will be determined by the beta's of the transistors and the supply voltage.

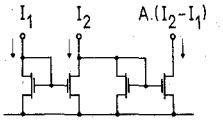


Fig. 2. Current subtractor realizing $A \cdot (I_2 - I_1)$.

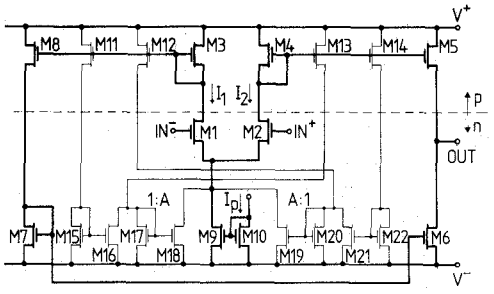


Fig. 3. Differential feedback amplifier.

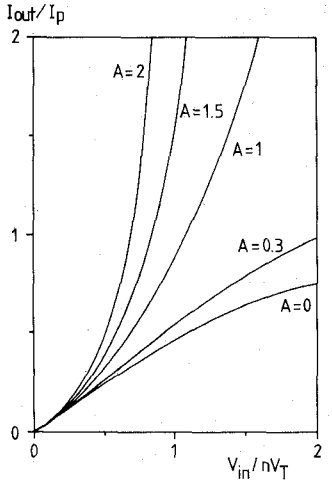


Fig. 4. Calculated output current versus input signal.

C. Effects of Mismatch

The previous analysis was based on ideally matched subtractors. Now the effect of mismatching in the current mirrors will be investigated. When taking all possible mismatches into account the subtractor equations become

$$A' \cdot (I_1 - c_1 \cdot I_2)$$

$$A'' \cdot (I_2 - c_2 \cdot I_1).$$

A' and A'' are the effective current feedback factors, c_1 and c_2 are mismatch factors. For the ease of derivation it will be supposed that $A' = A'' \neq A$ and $c_1 = c_2 = c$.

For c larger than unity, the current feedback circuit will not operate until the input voltage exceeds the minimum indicated by

$$V_{min} = -n \cdot V_t \cdot \ln(c). \tag{9}$$

For a mismatch of 20 percent ($c = 1.2$) the input voltage difference must be larger than 7 mV before the amplifier starts operating in the adaptive mode. This has, however, no effect on the driving capability of the amplifier since for such a small

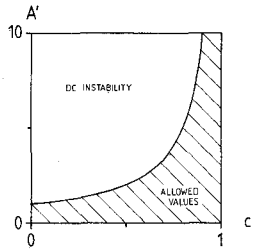


Fig. 5. Allowed feedback factors versus mismatch.

signal the amplifier does not slew. The designer can voluntarily introduce a c larger than unity in order to reduce the distortion of small signals.

For c's smaller than unity, the steady-state bias current is modified to

$$I_{\text{bias}} = I_p/(1 - A' \cdot (1 - c)). \tag{10}$$

For some combinations of the effective current feedback factor A' and the mismatch factor c, the bias current becomes infinite, which means that the amplifier is dc unstable. The allowed values of A' to insure dc stability are shown in Fig. 5 as a function of the mismatch factor. For a mismatch of 20 percent ($c = 0.8$), the effective current feedback factor A' should be smaller than 5.

D. Stability

Since there is no dc current flowing through the transistors $M18$ and $M19$, $g_{m_{18}}$ and $g_{m_{19}}$ are zero and no current is fed back. As a result the small signal scheme of the simple OTA is obtained but with larger internal capacitance due to the gate and overlap capacitance of the transistors $M11$, $M12$, $M13$, and $M14$.

The amplifier is designed to be stable for small capacitive loads and to have a gain of 60 dB for $I_p = 1$ μA. A small signal analysis shows that for a current ratio b of unity a minimal capacitive load of 5 pF is sufficient for compensation. For current ratios b larger than one, the dominant pole moves to higher frequencies so that a larger capacitive load is needed.

When large steps are applied the nonlinearity of the amplifier becomes important.

Since in nonlinear systems it no longer makes sense to speak about poles, bode diagram, settling time, etc., the stability of the amplifier cannot be studied by using classical tools. It is shown in the Appendix that the system has a single point of natural equilibrium to which the system always returns independently of the input signal amplitude.

E. Layout

The amplifier is integrated in a low voltage 5 μm CMOS technology. The total area is 0.075 mm^2, which is comparable to that of state of the art CMOS op amps, and this in spite of the fact that the adaptive biasing part takes about 20 percent of the total amplifier area. Table I shows the device dimensions and the corresponding weak inversion limits. Fig. 6 shows a photograph of the amplifier. The dimensions of the transistors of the subtractor were chosen to minimize the total amplifier size. The current feedback factor A of the amplifier equals 2.

TABLE I
MASK DEVICE DIMENSIONS DIFFERENTIAL FEEDBACK AMPLIFIER

Device	Dimension $w \times l$ [μm]	Weak-inversion limit $\beta \cdot V_T^2$ [nA]
3, 4, 11, 12, 13, 14	20 × 10	20
1, 2	120 × 10	264
5, 8	60 × 30	20
6. 7	60 × 30	44
9, 10	10 × 40	5
15, 16, 17, 20, 21, 22	14 × 18	17
18, 19	28 × 18	34

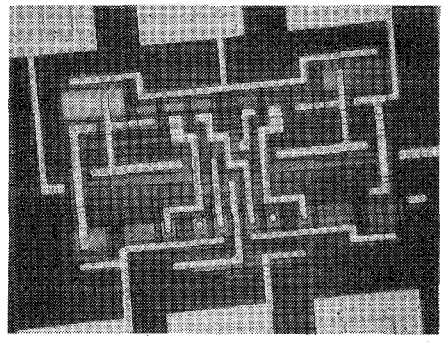


Fig. 6. Photograph of differential feedback amplifier.

In order to obtain good matching between the current mirrors, the layout was made as symmetrical as possible. Further, all transistors of a current mirror have 1) the same geometry, 2) the same neighborhood, and 3) the same orientation on the chip. Only the current mirror of the tail current source makes an exception to the last rule.

There is no static bias current source provided on chip; the bias current can therefore be set externally.

F. Experimental Results

In order to measure the escape voltage and the total power consumption as a function of the input voltage difference V_{in}, the configuration of Fig. 7(a) was used. The measured load current I_{out} as a function of V_{in} is given in Fig. 8 for $I_p = 0$ and $V^+ - V^- = 5$ V. For zero V_{in}, only leakage currents are flowing through the amplifier. When a voltage difference is applied, those leakage currents are fed back so that the current level in the amplifier increases. Once the escape voltage of about 40 mV is exceeded, the current level increases very drastically.

The total supply current, as a function of V_{in}, is represented in Fig. 9 for three different values of bias current I_p. Biased at 30 nA, the input transistors are operating in weak inversion. An input voltage difference of only 50 mV causes the total current consumption to increase to about 65 μA. Then the input transistors cease to operate in weak inversion so that the current will increase less than exponentially. For input signals exceeding a few hundred millivolts the total power consumption becomes almost independent of the bias current I_p. The maximum supply current, determined by the supply voltage and the beta's of the transistors, is about 300 μA. This maximum supply current determines the maximum rate of change of the output voltage.

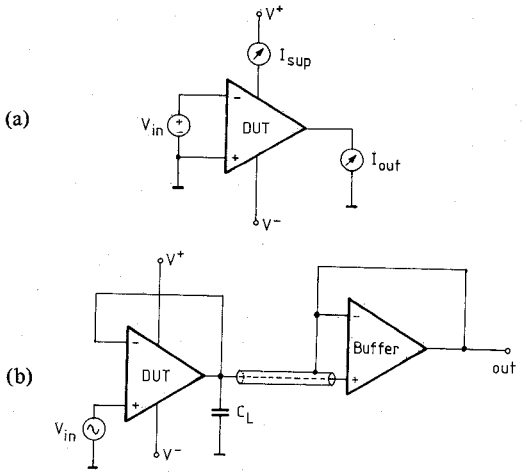


Fig. 7. (a) Measurement configuration for obtaining $I_{sup} - V_{in}$ curves. (b) Measurement configuration for determining ac characteristics.

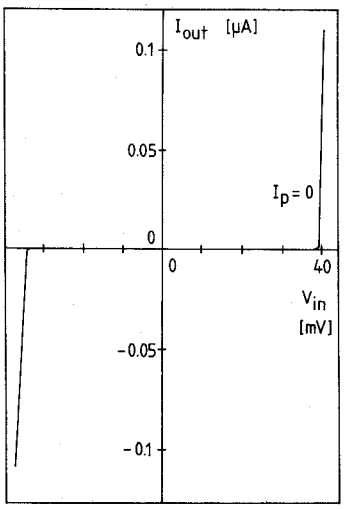


Fig. 8. Measured output current for $I_p = 0$.

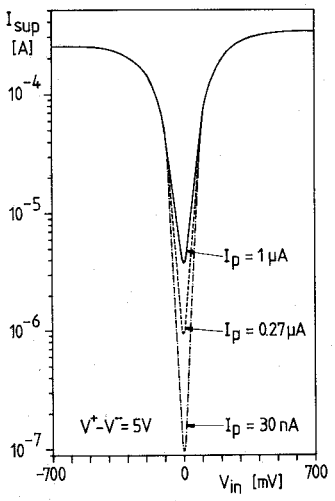


Fig. 9. Supply current as a function of the input signal.

With the amplifier connected in voltage follower configuration as shown in Fig. 7(b) and with a capacitive load of 470 pF, a slew rate of 0.25 V/μs is measured. For a capacitive load of 10 pF, the slew rate is more than 10 V/μs independent of the bias current I_p.

TABLE II
SMALL SIGNAL CHARACTERISTICS

$I_p = 1\ \mu A$	$V_{sup} = 5$ V
Gain	64 dB
Offset	3.68 mV ± 4 mV
Noise 1 kHz	190 nV/$\sqrt{Hz}$
10 kHz	60 nV/$\sqrt{Hz}$
CMRR	62 dB
PSRR V+	63 dB
V-	44 dB
"SR" (C_{load} = 470 pF)	0.25 V/μs

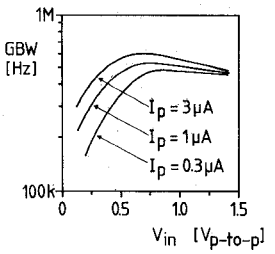


Fig. 10. Measured −3 dB breakpoint as a function of input amplitude (unity gain feedback).

Measured values of the most important small signal characteristics of the amplifier are listed in Table II. The negative power supply rejection ratio can be improved by putting the input transistors in a separate p-well and by using an on-chip bias current source which is independent of the supply voltage.

Fig. 10 shows the gain-bandwidth product of the amplifier as a function of the amplitude of the sine wave input signal. The −3 dB breakpoint frequency was measured using an oscilloscope, so these figures must be interpreted carefully since they include the higher harmonics of the output signal. However, one can see that the gain-bandwidth product increases with the amplitude of the input signal up to a certain maximum. This maximum occurs when the maximum current is flowing through the amplifier. For a classical fixed bias current amplifier, the gain-bandwidth product decreases with increasing input amplitude.

IV. Direct Feedback Amplifier

The direct feedback amplifier is designed to be used as a micropower buffer for large capacitive loads. The design is made so that nearly the whole supply current is used to charge the load capacitor.

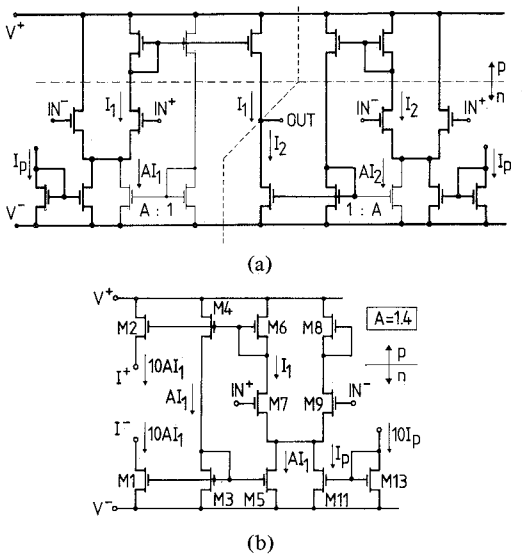
A. Principle

Fig. 11(a) represents the scheme of the amplifier. Thick lines show the simple transconductance amplifier discussed above. The amplifier is split up in two symmetrical parts. Then, without making a subtraction, in each input stage the current of one branch is directly fed back to the tail current source.

When the differential input voltage V_{in} equals zero, the currents I_1 and I_2 are equal and given by (11) and (12).

$$I_{1(2)} = \tfrac{1}{2}\,(I_p + A \cdot I_{1(2)}) \tag{11}$$

$$I_1 = I_2 = I_0 = I_p/(2 - A). \tag{12}$$



(a)

(b)

Fig. 11. (a) Direct feedback amplifier. (b) Realized scheme.

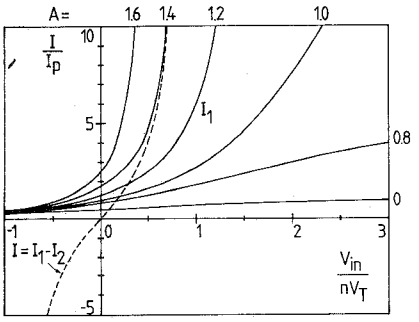


Fig. 12. Calculated currents as a function of the input signal.

Stability is ensured if the current feedback factor is smaller than two. When V_{in} is larger than zero, the current I_1 increases. Due to positive feedback the current may reach a value much larger than I_0 which results in a high driving capability. This is true as well for I_2 when V_{in} is negative. Simple calculations yield that $I_{1(2)}$ is given by (13) which is represented in Fig. 12 for various values of the current feedback factor $A \cdot (b = 1)$

$$I_{1(2)} = \frac{I_p}{(1 - A) + \exp(-(+) V_{in}/(n \cdot V_T))}. \tag{13}$$

The available output current, which equals I_1-I_2, is given by (14) and is represented in dotted lines in Fig. 12

$$I_{out} = \frac{I_p \cdot (\exp(V_{in}/(n \cdot V_T)) - 1)}{1 - (A - 1) \cdot \exp(V_{in}/(n \cdot V_T))} \cdot b. \tag{14}$$

Notice that, just as in the case of the differential feedback amplifier, this amplifier also has a well-determined escape voltage.

B. Layout

Only half of the amplifier was integrated [see Fig. 11(b)] since the amplifier can easily be realized by properly connecting two halves. Fig. 13 is a photograph of the amplifier. It is integrated in the same technology as the first amplifier. The device dimensions and the corresponding weak inversion limits are given in Table III. The total size of the amplifier is about 400 X 190 μm.

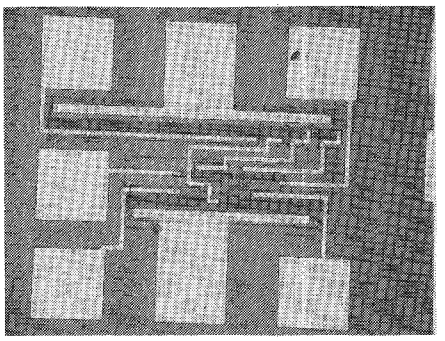


Fig. 13. Chip photograph of direct feedback amplifier.

TABLE III
MASK DEVICE DIMENSIONS DIRECT FEEDBACK AMPLIFIER

Device	Dimension $w \times l$ [μm]	Weak-inversion limit $\beta \cdot V_T^2$ [nA]
1, 13	100 X 12	200
3, 5, 11	10 X 12	20
7, 9	50 X 6	200
2	300 X 12	200
4	30 X 12	20
6, 8	21 X 12	14

The amplifier is designed to charge large capacitive loads ($\geqslant$100 pF). This makes a large width to length ratio of the output stage transistors possible without running into stability problems. The current flowing in the output stage is about 15 times the internal current resulting in a high efficiency.

C. Experimental Results

The measured supply and output current as a function of the input signal are represented in Fig. 14(a). One can see that almost the whole supply current is available at the output. The maximum output current, which is determined by the beta's of the transistors and the supply voltage, is about 50 μA.

Fig. 14(b) is a detail of Fig. 14(a) for small input signals. Biased at 2 X 10 nA, a transconductance of 20 μA/V is measured. Under these conditions and with a capacitive load of 100 pF the amplifier has a GBW of 30 kHz. The measured output current for zero I_p is shown in dotted lines in Fig. 14(b). Once the escape voltage is exceeded, the output current increases very drastically.

V. CONCLUSIONS

In this paper two amplifiers are presented which regulate their own bias current. If no signal is applied the amplifiers operate at a very low current level. Only when a signal is applied the current in the amplifiers increases so that these amplifiers have a high driving capability.

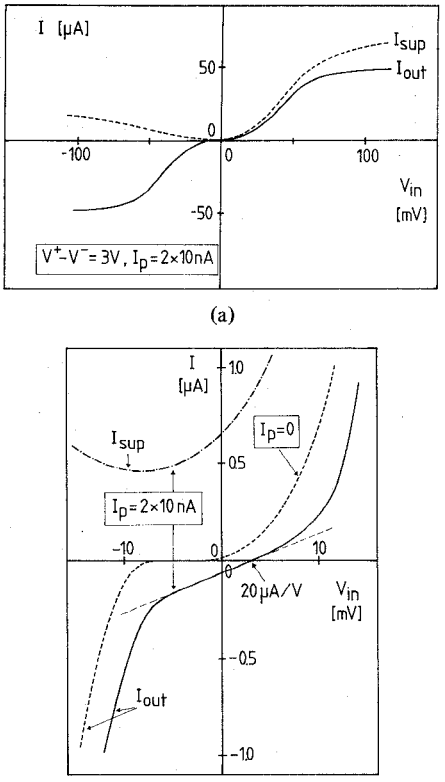


Fig. 14. Measured supply and output current versus input signal. (b) Detail of (a) for small input signals.

The first amplifier has a slew rate which is more than an order of magnitude better than earlier presented micropower amplifiers [2], [3]. Since this amplifier is fairly small it is well suited for the use in large micropower sampled data filters.

The second amplifier is well suited for use as a micropower buffer since it does not slew and has a high efficiency.

Appendix

In order to be able to study the step response of the differential feedback amplifier some assumptions have to be made.

1) The internal time constants of the amplifier can be neglected with respect to the time constant of the output stage.

2) The current feedback factor is close to one. (This guarantees a sufficient "slew rate" and results in a small size amplifier.)

3) For an increasing current level, the input transistors will work most of the time in strong inversion. Therefore, the input transistors are assumed to always work in strong inversion.

4) The output resistance of the amplifier can be modeled by

$$R = \frac{V_{\text{Early}}}{I + i} \tag{A1}$$

where I represents the dc current and i the ac current flowing through the output stage.

An SC integrator, during the integrating phase, using a differential feedback amplifier can be modeled by Fig. 15. The behavior of the integrator is fully described by the following pair of differential equations:

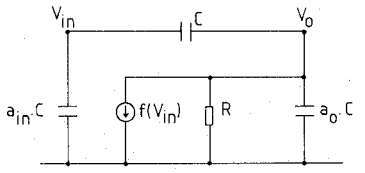


Fig. 15. SC integrator during integrating phase.

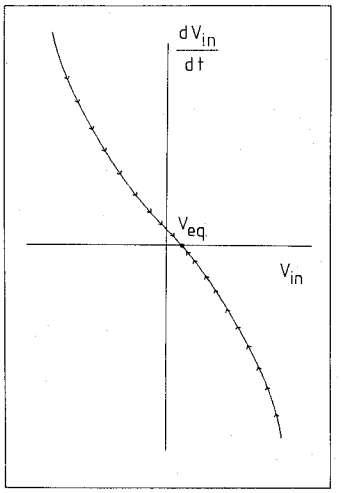


Fig. 16. Behavior of input of nonlinear amplifier in SC integrator.

$$C \cdot \frac{d(V_0 - V_{\text{in}})}{dt} = a_{\text{in}} \cdot C \cdot \frac{dV_{\text{in}}}{dt} \tag{A2}$$

$$C \cdot \frac{d(V_0 - V_{\text{in}})}{dt} + a_0 \cdot C \cdot \frac{dV_0}{dt} + \frac{V_0}{R} + f(V_{\text{in}}) = 0 \tag{A3}$$

where

$$f(V_{\text{in}}) = b \cdot (\text{beta} \cdot |V_{\text{in}}|/2 + \sqrt{\text{beta} \cdot I_p}) \cdot V_{\text{in}}$$

beta = beta of input transistor.

For a step input (A3) is then of the form

$$\frac{dV_{\text{in}}}{dt} = a_1 + a_2 \cdot V_{\text{in}} + a_3 \cdot \frac{V_{\text{in}}^3}{|V_{\text{in}}|} \tag{A4}$$

where

$$a_1 = \frac{V_{\text{step}} \cdot V_{\text{Early}}}{I \cdot C_1}$$

$$a_2 = -\left(\frac{V_{\text{Early}}}{I \cdot C_1} + \frac{b \cdot \text{beta} \cdot I_p}{(1 + a_{\text{in}}) \cdot C_1}\right)$$

$$a_3 = -\frac{b \cdot \text{beta}}{2 \cdot C_1}$$

$$C_1 = C \cdot \left(a_0 + \frac{a_{\text{in}}}{a_{\text{in}} + 1}\right).$$

This formula, represented in Fig. 16 has only one point where the derivate is equal to zero. This is an equilibrium

point since for V_{in} larger than V_{eq} the derivate is smaller than zero and thus the input will decrease until V_{eq} is reached. For V_{in} smaller than V_{eq}, the derivate is larger than zero and thus the input will increase until V_{eq} is reached.

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