Low-Voltage CMOS Op-Amp with Rail-to-Rail Input and Output Signal Swing for Continuous-Time Signal Processing Using Multiple-Input Floating-Gate Transistors

J. Ramírez-Angulo, R. G. Carvajal, J. Tombs, and A. Torralba

***Abstract*—A scheme for low-voltage CMOS op-amp operation with rail-to-rail input and output signal swing and constant g_m is presented. Single-ended and fully differential versions are discussed. The scheme is based on the use of multiple-input floating-gate transistors and allows direct implementation of linear weighted addition of continuous-time signals. Simulations are presented that verify the scheme operating with a 1.2-V single supply, 1.2-V input and output swing, 5-MHz op-amp gain-bandwidth product, and a 192-μW power dissipation with a 50-pF load and 300 $\times$ 300 μm^2 silicon area. These results are obtained for 0.85-V transistor threshold voltages. Experimental results are shown that verify the correct functionality of the proposed approach.**

***Index Terms*—Amplifiers, analog circuits, continuous-time systems, low-voltage CMOS circuits, operational amplifiers.**

I. Introduction

As downscaling of CMOS processes has progressed, analog circuits have been forced to operate with continuously decreasing supply voltages. This process has been mainly driven by the need to reduce digital power consumption in mixed-mode VLSI systems and by the low breakdown voltages of the gate oxide in technologies with very fine feature size. Several schemes for discrete-time (switched) operation with a single supply down to 1 V and large output signal swings have been reported recently [1]–[4]. In switched applications, no input swing is required for the op-amp since both input terminals operate at one of the supply rails. A continuous-time scheme for 1-V rail-to-rail input and output operation of a bipolar op-amp was proposed in [5], where level-shift resistors were placed at the op-amp input terminals to allow the simultaneous operation of two complementary differential pairs in the middle of the range of the input signals. A simpler approach was proposed in [6] for the CMOS case, where a feedback amplifier was used to eliminate the input common-mode voltage providing rail-to-tail input operation with constant g_m. Another continuous-time scheme for large-input signal swing using a 1-V CMOS op-amp was reported in [7]. This scheme is based on the utilization of the substrate terminal of an MOS transistor as an active input terminal (bulk-driven transistors) and imposes severe gain-bandwidth limitations due to a very large input capacitance and reduced input-stage transconductance. Like the approach in [5], g_m is not constant (it depends on the input signal); in addition, only one type of input transistor is available in a single-well CMOS process.

In this paper, a continuous-time scheme to operate op-amps with a single supply voltage close to just one transistor's threshold voltage and with rail-to-rail input and output swing is proposed. It is based on the use of multiple-input floating-gate transistors combined with a novel low-voltage class-AB op-amp architecture. The proposed scheme achieves constant g_m without the use of complementary differential pairs and allows easy implementation of low-voltage linear weighted addition of several signals, which is the basic operation of linear systems. A detailed study of the scheme in regard to bandwidth, offset, noise, and silicon area is made. A fully differential version of the scheme is also discussed, as are techniques for low-voltage common-mode signal sensing and control based on the use of multiple-input floating-gate transistors.

II. Rail-to-Rail Op-Amp Input Stage Using Floating-Gate Transistors

In what follows, we assume a single supply voltage $V_{\rm DD}$ only a few tenths of a volt higher than one transistor's threshold voltage but not so high as to allow the simultaneous operation of one NMOS and one PMOS stacked transistors whose gate-to-source junctions are in a series connection, i.e., $|V_{\rm thP}| + V_{\rm thN} > V_{\rm DD} > \{|V_{\rm thP}|, V_{\rm thN}\}$, where $V_{\rm thP}$ and $V_{\rm thN}$ denote the threshold voltages of P and N transistors, respectively. Note that the conventional rail-to-rail input stage is based on two complementary differential pairs that require $V_{\rm DD}$ to be higher than $|V_{\rm thP}|+V_{\rm thN}+2V_{\rm DSsat}$. Additional complex circuitry to maintain constant g_m at the input stage [8] ($V_{\rm DSsat}$ is the minimum drain-to-source voltage drop required to maintain in saturation the transistors that implement the current mirrors that provide the tail currents to both differential pairs).

In this section, a new input stage is proposed that is based on a single differential pair that uses multiple-input floating-gate transistors (MIGFTs). In order to allow rail-to-rail input operation, the op-amp input signals are attenuated and taken to a potential very close to one supply rail. This is done by means of a capacitive divider implemented with MIFGTs, following the ideas proposed in [9] and [10]. To this purpose, the floating gate of each MIFGT is biased by connecting one of its inputs to one supply rail [ground in Fig. 1(a)], while the other input terminals are used to apply signals. For very low-voltage operation, the capacitor connected to the supply rail needs to be larger than the capacitors connected to the signals. Assuming an ideal op-amp in Fig. 1(a) with null offset and with a PMOS differential input stage, the capacitive dividers formed by $C1$ and $C_{\rm cm}(C1 << C_{\rm cm})$ lead to the following voltages $V_{\rm FGi+}$ and $V_{\rm FGi-}$ at the floating gates of the differential pair transistors:

$$V_{\rm FGi+} = V_{i+} \cdot \frac{C1}{C1 + C_{\rm cm}} = \frac{V_{i+}}{A_{tt}}$$

$$V_{\rm FGi-} = V_{i-} \frac{C1}{C1 + C_{\rm cm}} = \frac{V_{i-}}{A_{tt}}$$

where $A_{tt} = (C1 + C_{\rm cm})/C1$ is the attenuation factor.

Under quiescent conditions ($V_{i+}^Q = V_{i-}^Q = V_{\rm DD}/2$), the quiescent differential-pair input voltages are given by $V_{\rm FG+}^Q = V_{\rm FG-}^Q = (V_{\rm DD}/2) \cdot (C1/C1 + C_{\rm cm}) = V_{\rm ref}$, where $V_{\rm ref}$ denotes the quiescent voltage drop across $C_{\rm cm}$. In order to maintain low-voltage operation, $V_{\rm ref}$ is selected to be very close to ground and $C_{\rm cm} \gg C1$. For instance, for $V_{\rm DD} = 1.2$ V and $C_{\rm cm} = 4C1$, a voltage $V_{\rm ref} = 0.12$ V

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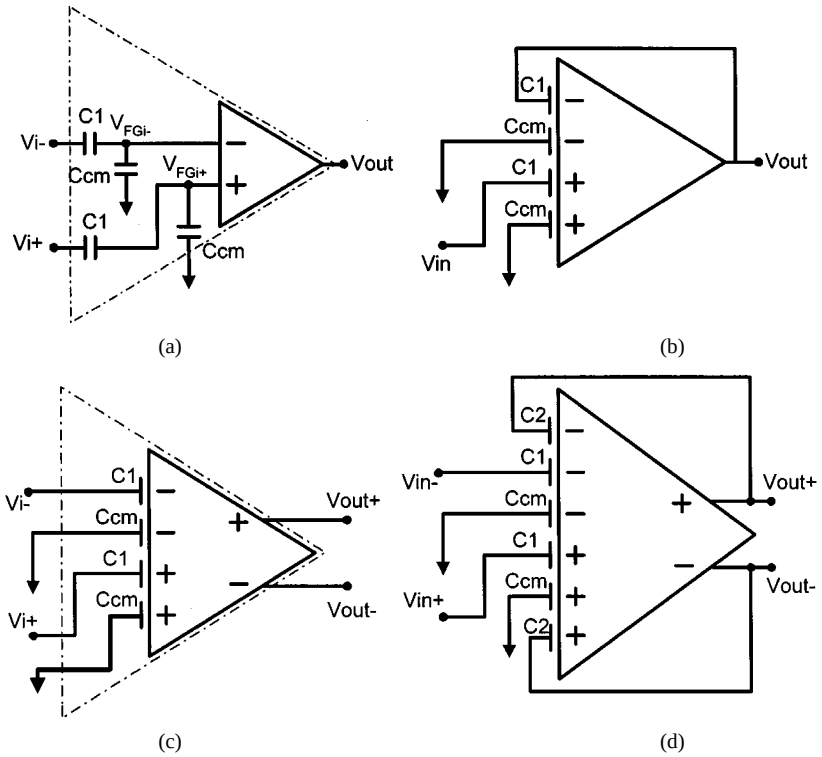


Fig. 1. Capacitive divider scheme: (a) basic scheme, (b) voltage follower, (c) fully differential scheme, and (d) fully differential amplifier with gain $C1/C2$.

and quiescent differential-pair input voltages $V_{\mathrm{FG}+}^{Q} = V_{\mathrm{FG}-}^{Q} = 0.12$ V result.

This approach has the following advantages.

1) As a single differential-pair is used, a constant g_m is obtained over the full input range and there is no CMRR degradation due to the operation of two complementary differential pairs.
2) Capacitive dividers do not introduce dc input impedance degradation; neither do they load the input sources or the output terminals of the op-amps.
3) No additional noise is introduced by the capacitive elements.
4) This scheme allows easy implementation of linear weighted addition of several signals, given that this is a basic characteristic of MIFGT circuits, with the weights being determined by input capacitor ratios.

The price paid for low-voltage operation using MIFGTs is an effective reduction in the input stage transconductance, and therefore, in the op-amp dynamic range and gain-bandwidth product. In order to avoid significant degradation of these op-amp characteristics, a value $C_{\mathrm{cm}}/C1 \sim 5$ has been found to be convenient.

Fig. 1(b) shows the single-ended version of the proposed op-amp in a voltage follower configuration. Fig. 1(c) shows the proposed symbol for the fully differential version and Fig. 1(d) shows a fully differential amplifier with gain $C1/C2$ that uses three-input floating-gate transistors in the input differential stage.

Another approach for the implementation of low-voltage op-amps using single-input floating-gate transistors was reported in [11]. Unlike the circuit proposed here, the approach in [11] is based on injecting charge into the floating gate. It requires complex circuitry to adjust V_{th}, using high voltage that might not be allowed in a CMOS process, and lacks the flexibility of the approach reported here because it uses single-input floating-gate transistors. In [12], a new design technique called FGUVMOS was introduced. Although the FGUVMOS technique allows very low-voltage operation, there are some constraints in the cell architecture, as well as in the programming process, that make it more appropriate for digital circuits than for analog cells. A similar approach to the one reported in this paper for rail-to-rail input signal swing was proposed in [13], but no op-amp implementation suitable for low-voltage operation with rail-to-rail output swing was shown.

III. Low-Voltage Op-Amp

Fig. 2(a) shows the basic architecture of the proposed low-voltage op-amp [14]. It has a two-stage architecture: the first stage is the aforementioned differential pair with MIFG transistors (depicted as conventional MOS transistors) and the second stage is an original low-voltage class-AB CMOS inverter modified by the addition of a floating biasing battery with value V_{bias} between the gates of the inverter's transistors. This battery has a negative polarity, which allows the supply voltage V_{DD} to be reduced to a value close to one transistor's threshold voltage.

Fig. 2(b) shows two practical implementations of the floating battery V_{bias}. The first one (on the left) uses a transistor M_b biased with a small current I_b. In this case, $V_{\mathrm{bias}} = V_{\mathrm{SGMb}}$. In the second case (on the right), a resistor R_b is used instead of M_b. In this case, $V_{\mathrm{bias}} = I_b R_b$ and an additional biasing source I_b on the bottom is required. A capacitor C_{bp}, is used to bypass M_b (or R_b) at high frequencies.

Notice from Fig. 2(a) that the output-stage biasing loop forces $V_{\mathrm{DD}} + V_{\mathrm{bias}} = V_{\mathrm{SGMoutp}} + V_{\mathrm{GSMoutn}}$. A positive signal excursion at node V_x decreases V_{GSMoutp} and increases V_{GSMoutn} in the same amount. According to the MOS transistor quadratic law, these variations in gate-to-source voltages produce significant changes in the output transistor currents, characteristic of class-AB operation. The proposed low-voltage class-AB output stage provides the circuit with very attractive characteristics: 1) rail-to-rail output swing, 2) low quiescent power dissipation, and 3) high slew rate, since the maximum load current can be much greater than the quiescent current (although, for small load capacitances, the slew rate is limited by the tail current of the input differential pair and the compensation capacitor C_C). This op-amp has been used to verify the proposed continuous-time input stage.

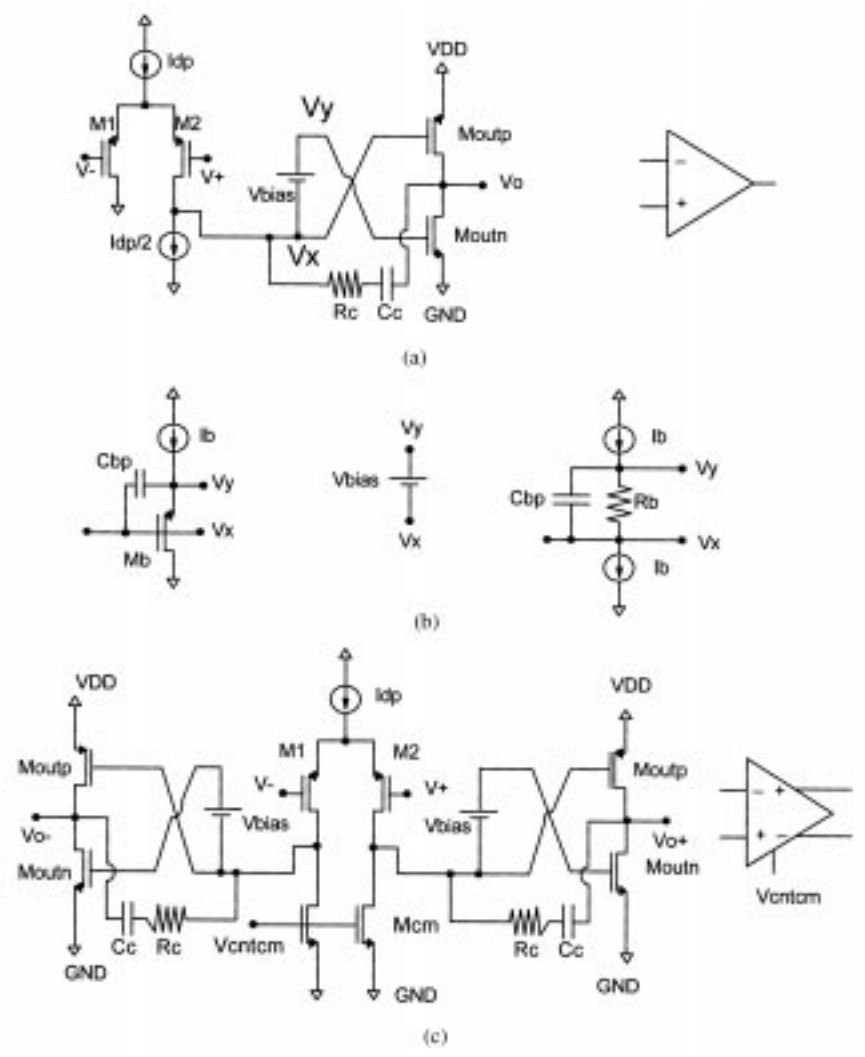


Fig. 2. Proposed low-voltage two-stage op-amp: (a) single-ended scheme, (b) two possible implementations of the floating battery, and (c) fully differential scheme.

A. Low-Voltage Common-Mode Sensing Schemes

Fig. 2(c) shows the fully differential version of the CMOS op-amp of Fig. 2(a). It uses transistors $M_{\rm cm}$ to control the common-mode output voltage. A low-voltage continuous-time approach is introduced here [Fig. 3(a)]. It uses two equal-valued capacitors C to sense the common-mode output signal $V_{{\rm out}cm} = (V_{o+} + V_{o-})/2$. This approach was reported originally in [15] and used to sense the common-mode output signals in feedforward voltage follower structures, but not within the context of low-voltage applications.

The common-mode amplifier of Fig. 3(a) must also operate with the constraint of low-voltage supply. To this end, an additional capacitor C_m at the input terminals of the common-mode amplifier forms a capacitive divider, which allows operation of both input terminals of the common-mode amplifier with a potential close to ground. The common-mode amplifier generates a signal $V_{\rm cntcm}$ that forces $V_a = V_{{\rm out}cm}C/(C_m + 2C)$ to a value $V_a = V_{\rm refcm}C/(C_m + 2C)$, where $V_{\rm refcm}$ is the desired common-mode voltage (assumed to be $V_{\rm DD}/2$). As in the main amplifier, the capacitive divider of the common-mode amplifier is implemented by means of a differential pair with two-input floating-gate transistors. Fig. 3(b) shows implementation of the common-mode amplifier. $M_{\rm LS}$ generates a dc-level shift so that $V_{\rm cntcm}$ is appropriate for the N-transistors $M_{\rm cm}$ in Fig. 2(b).

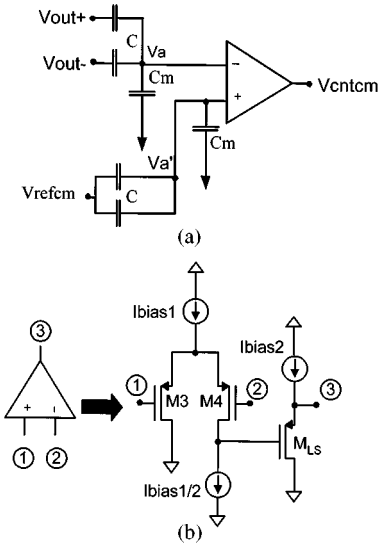


Fig. 3. Low-voltage common-mode amplifier scheme: (a) capacitive dividers at the input terminals and (b) common-mode amplifier implementation.

TABLE I
OP-AMP DESIGN PARAMETERS

V_{DD}	1.2 V
W/L (M1, M2)	2000/2
W/L (Mb)	350/2
W/L (Moutn)	600/2
W/L (Moutp)	1800/2
I_{dp}	100 μA
I_{out}^{Q}	30 μA
R_C	600 Ω
C_C	30pF
C_L	50 pF

B. Output Quiescent Current Control

In Fig. 2(a), the output quiescent current $I_{\rm out}^{Q}$ is related to $V_{\rm bias}$ and to transistor gain factors (β_n, β_p) and threshold voltages ($V_{\rm thN}$, $V_{\rm thP}$) through the equation set

Transistor M_{outn}:

$$I_{\rm out}^{Q} = (\beta_n/2)(V_{\rm GSMoutn}^{Q} - V_{\rm thN})^2$$

Transistor M_{outp} :

$$I_{\rm out}^{Q} = (\beta_p/2)(V_{\rm SGMoutp}^{Q} - |V_{\rm thP}|)^2$$

Biasing loop:

$$V_{\rm DD} = V_{\rm SGMoutp}^{Q} - V_{\rm bias} + V_{\rm GSMoutn}^{Q}$$

that leads to

$$V_{\rm GSMoutn} = \frac{V_{\rm DD} + V_{\rm bias} + V_{\rm thN}\sqrt{\dfrac{\beta_n}{\beta_p}} - |V_{\rm thP}|}{1 + \sqrt{\dfrac{\beta_n}{\beta_p}}}.$$

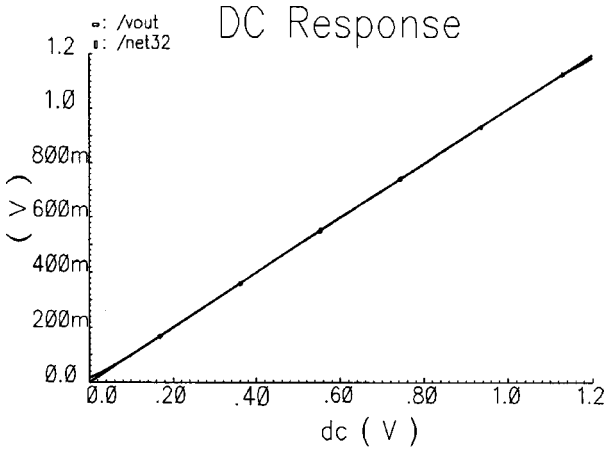
For the common design case $\beta_n \approx \beta_p$ (and making the simplifying assumption $V_{\rm thN} \approx |V_{\rm thP}|$), this expression reduces to

$$V_{\rm GSMoutn} \approx \frac{V_{\rm DD} + V_{\rm bias} + V_{\rm thN} - V_{\rm thP}}{2} \approx \frac{V_{\rm DD} + V_{\rm bias}}{2} \approx V_{\rm GSMoutp}.$$

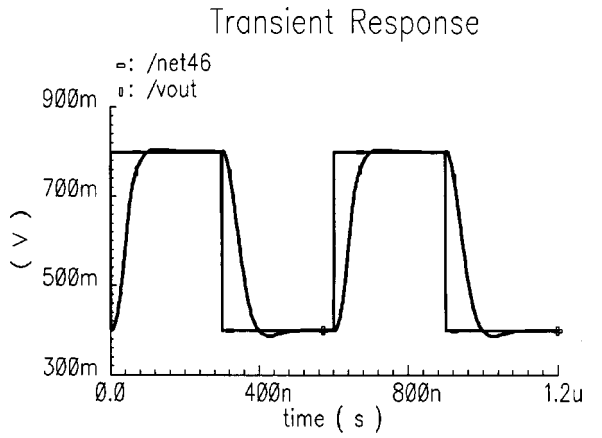
For example, with $V_{\rm DD} = 1.2$ V and $V_{\rm bias} = 0.6$ V, the approximate value for output transistor gate–source biasing voltages is 0.9 V. Assuming $V_{\rm thN} = |V_{\rm thP}| = 0.85$ V, $V_x^{Q} = V_{\rm DD} - V_{\rm SGMoutp}^{Q} = 0.30$ V. A replica bias circuit can be used to set the output quiescent current $I_{\rm out}^{Q}$ to a nominal value $I_{\rm ref}^{Q}$ independent on the supply voltage. A detailed description and analysis of the replica bias circuit was reported in [18].

IV. SIMULATION AND EXPERIMENTAL RESULTS

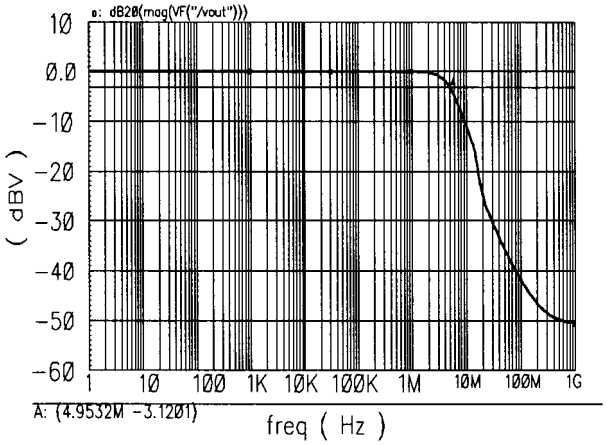
The op-amp has been verified by simulation with files extracted from a layout generated in the CADENCE Design Framework II and for the AMS-CXQ 0.8-μm CMOS process. The MIFGTs have been simulated using the model in [16] transformed into a CADENCE design kit [17]. The op-amp was designed for a capacitive load $C_L = 50$ pF with the circuit parameters shown in Table I. For the input capacitive divider,



(a)



(b)

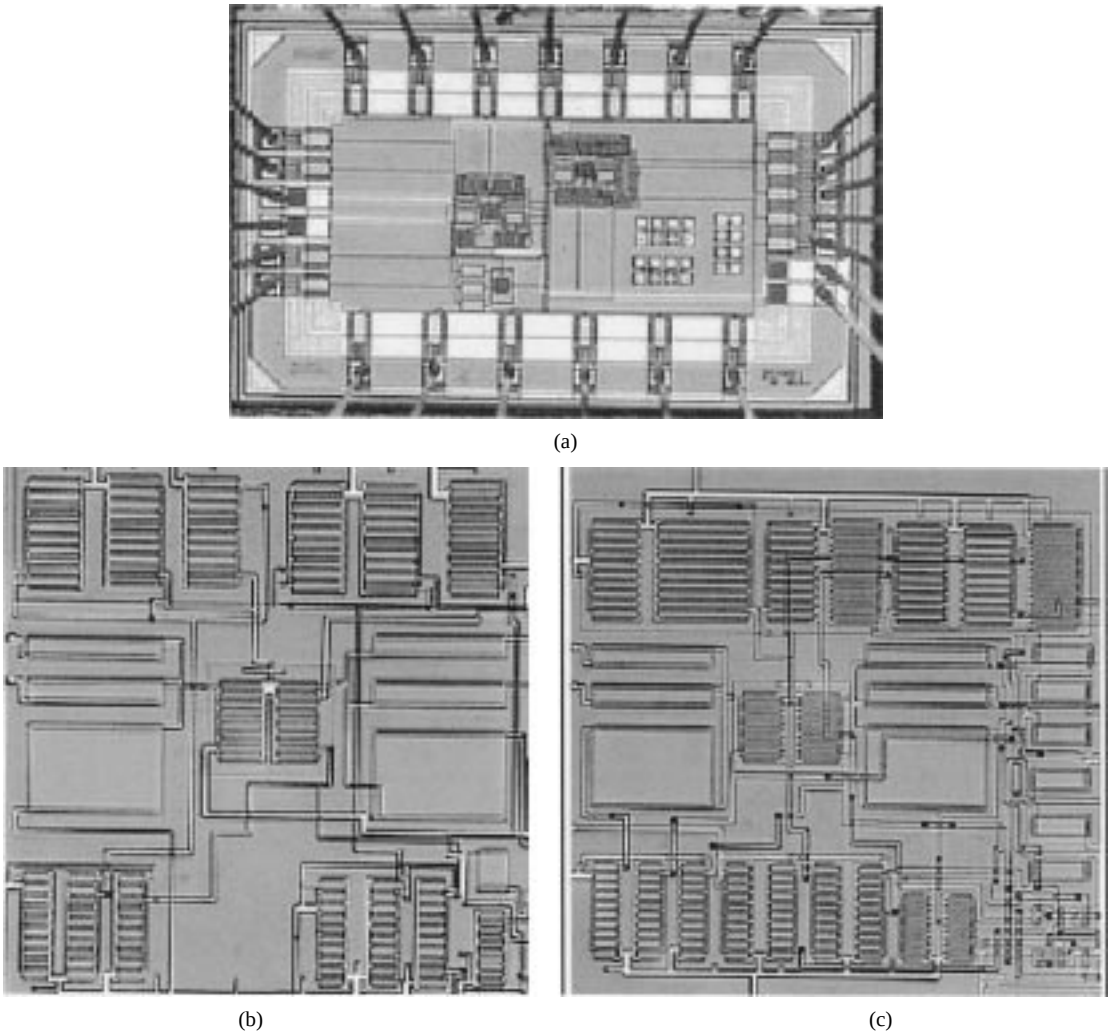


(c)

Fig. 4. Simulation results: (a) dc response, (b) transient response, and (c) frequency response.

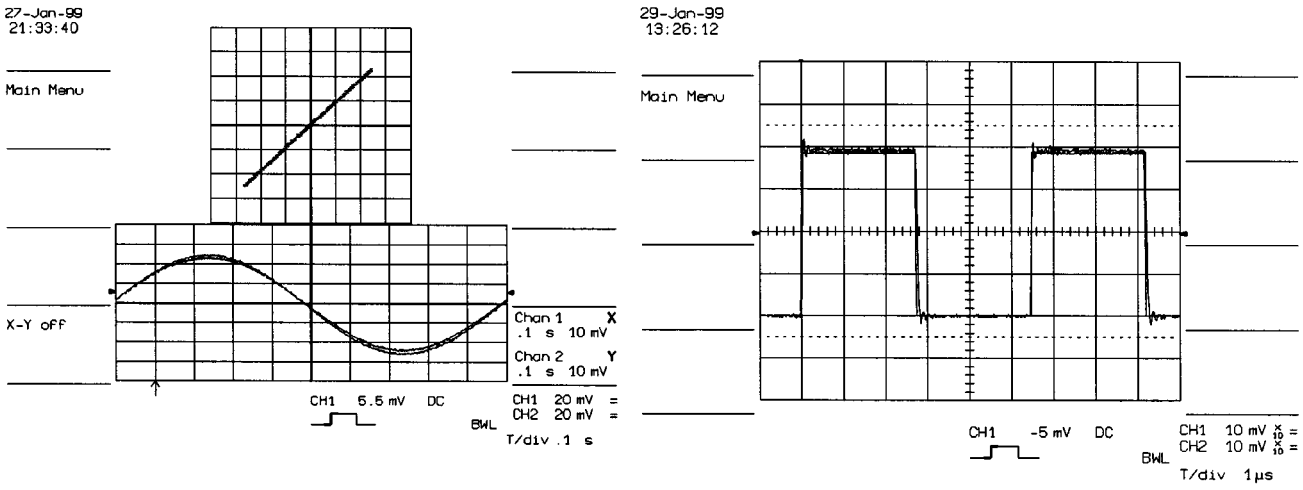
$C1 = 4.4$ pF and $C_{\rm cm} = 22$ pF were used, providing an attenuation factor of $A_{tt} = 6$. Fig. 4(a)–(c) presents the dc transfer characteristic, the step response, and the ac characteristic of the op-amp in a voltage follower configuration. Rail-to-rail input and output signals can be observed in Fig. 4(a). Fig. 4(c) shows a 3-dB bandwidth of 5 MHz. The intermediate column in Table II lists the simulated op-amp performances. Notice that a slew rate of 7 V/μs, a dc open-loop gain of 60 dB, and a phase margin of 70° were obtained.

A test chip prototype [Fig. 5(a)] with the single-ended and fully differential versions of op-amp [see Fig. 5(b) and (c)], including MIFG



(a) (b) (c)

Fig. 5. (a) Microphotograph of fabricated chip, (b) detail of the single ended amplifier, and (c) fully differential version.



(a) (b)

Fig. 6. Experimental results: (a) dc transfer characteristic and (b) step transient response.

transistors in the input stage, was fabricated. It can be observed that the area occupied by the floating POLY-I POLY-II capacitors is less than one-third of the overall area occupied by the op-amp. The single-ended op-amp was connected in a voltage follower configuration, just as the circuit simulated in the previous section. The last column in Table II summarizes the measured op-amp performances, which reasonably agree with simulated values. Fig. 6(a) shows the measured dc characteristic and Fig. 6(b) shows the transient response with a step input signal. The charge in the capacitors implementing the MIFGT

TABLE II
EXPERIMENTAL VERSUS SIMULATED RESULTS FOR OP-AMP WITH CAPACITIVE DIVIDERS AT ITS INPUT TERMINALS (ATTENUATION FACTOR $A_{tt} = 6$)

	Simulation	Experimental
Minimum V_{DD}	1.15 V	1.1 V
Input Range	1.2 V	1.2 V
Output Range	1.2 V	1.2V
Offset	0.2 mV	1 mV
DC Gain	60 dB	-
Phase Margin	70°	70°
GB	5 MHz	5 MHz
PSRR	40dB	-
CMRR	47 dB	-
THD (100 kHz)	0.09 %	0.1 %
Slew Rate	7 V/μs	7 V/μs
Peak output Current	0.8 mA	-

was not programmed, but they were erased using ultraviolet light while connecting all circuit terminals to ground.

V. CONCLUSION

A scheme for rail-to-rail continuous-time input signal swing using MIFGTs has been proposed. This scheme provides constant g_m. Single-ended and fully differential op-amp architectures based on this scheme and with a novel class-AB output stage have been introduced. The op-amp operates with a single supply voltage of 1.2 V for transistor threshold voltages of 0.85 V. The op-amp has rail-to-rail input and output signal swings, open-loop gain of 60 dB, phase margin of 70°, 5-MHz gain-bandwidth product, and a slew rate of 7 V/μs. This has been verified by simulations and experiments with a fabricated test-chip prototype.

REFERENCES

[1] A. Baschirotto and R. Castello, "A 1-V 1.8-MHz CMOS switched-opamp SC filter with rail-rail output swing," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1979–1996, Dec. 1997.

[2] A. Baschirotto, R. Castello, and G. P. Montagna, "Active series switch for switched opamp circuits," *Electron. Lett.*, vol. 34, no. 14, pp. 1365–1366, July 1998.

[3] V. Peluso, P. Vancorenland, M. Steyaert, and W. Sansen, "900 mV differential class AB OTA for switched opamp applications," *Electron. Lett.*, vol. 33, no. 17, pp. 1455–1456, Aug. 14, 1997.

[4] G. Ferri, W. Sansen, and V. Peluso, "A low voltage fully differential constant-Gm rail-to-rail CMOS operational amplifier," *Analog Integr. Circuits Signal Process.*, vol. 16, pp. 5–15, 1998.

[5] J. Fonderie, M. M. Maris, E. J. Schnitger, and J. H. Huijsing, "1-V operational amplifier with rail-to-rail input and output ranges," *IEEE J. Solid-State Circuits*, vol. 24, pp. 1551–1559, Dec. 1989.

[6] J. Ramírez-Angulo, A. Torralba, R. G. Carvajal, and J. Tombs, "Low-voltage CMOS amplifiers with wide input-output swing based on a novel scheme," *IEEE Trans. Circuits Syst. I*, vol. 48, May 2000.

[7] B. J. Blalock, P. E. Allen, and G. A. Rincón-Mora, "Designing 1-V op amps using standard digital CMOS technology," *IEEE Trans. Circuits Syst. II*, vol. 45, pp. 769–780, July 1998.

[8] J. H. Huising, K. de Langen, R. Hogervorst, and R. G. H. Eschaiuzier, "Low-voltage low-power amplifiers with optimized dynamic range and bandwidth," in *Low-Voltage/Low-Power Integrated Circuits and Systems*. Piscataway, NJ: IEEE Press, 1999, vol. 9, pp. 272–299.

[9] J. Ramírez-Angulo, S. C. Choi, and G. González-Altamirano, "Low-voltage circuits building blocks using multiple-input floating-gate transistors," *IEEE Trans. Circuits Syst. I*, vol. 42, pp. 971–974, Nov. 1995.

[10] J. Ramírez-Angulo, "Ultracompact low-voltage analog CMOS multiplier using multiple input floating gate transistors," in *Proc. Eur. Solid State Circuits Conf.*, Neuchatel, Switzerland, May 11–13, 1996, pp. 99–103.

[11] C. Yu and R. L. Geiger, "Very low-voltage operational amplifiers using floating-gate MOS transistors," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. II, Chicago, IL, May 3–6, 1993, pp. 1152–1155.

[12] Y. Berg, D. T. Wisland, and T. S. Lande, "Ultra low-voltage/low-power digital floating-gate circuits," *IEEE Trans. Circuits Syst. II*, vol. 46, pp. 930–941, July 1999.

[13] K. Yang and A. G. Andreou, "A multiple input differential amplifier based on charge sharing on a floating-gate MOSFET," *Analog Integr. Circuits Signal Process.*, vol. 6, pp. 197–208, 1994.

[14] J. Ramírez-Angulo, R. G. Carvajal, J. Tombs, and A. Torralba, "A simple technique for op-amp continuous-time 1V operation," *Electron. Lett.*, vol. 35, no. 4, pp. 263–264, Feb. 1999.

[15] G. González-Altamirano and J. Ramírez-Angulo, "Analog building blocks for a sampled data fast wavelet transform CMOS VLSI implementation," in *Proc. IEEE Int. Conf. Circuits and Systems*, Monterrey, CA, May 31–June 3, 1998, pp. 382–385.

[16] J. Ramírez-Angulo, G. González-Altamirano, and S. C. Choi, "Modeling multiple-input floating-gate transistors for analog signal processing," in *Proc. 1998 IEEE Int. Conf. Circuits and Systems*, Hong Kong, June 9–12, 1997, pp. 382–385.

[17] J. Tombs, J. Ramírez-Angulo, R. Carvajal, and A. Torralba, "Integration of multiple-input floating gate transistors into a top-down CAD design flow," in *Proc. Design of Circuits and Integrated Systems*, Mallorca, Nov. 1999, pp. 767–771.

[18] A. Torralba, R. G. Carvajal, and J. Ramírez-Angulo, "Class AB output stage for low voltage CMOS op-amps with accurate quiescent current control," *Electron. Lett.*, vol. 36, no. 21, pp. 1753–1754, Oct. 2000.

A Second-Order Section Built from Autozeroing Floating-Gate Amplifiers

Paul Hasler, Theron Stanford, and Bradley A. Minch

***Abstract*—We introduce the autozeroing floating-gate (AFGA) second-order section. We built this second-order filter where the corner frequency and Q are electronically tunable based on a classic filter topology and principles of operational transconductance amplifiers. We built this second-order filter using three AFGAs—our floating-gate amplifier that sets its operating point by the interaction of hot-electron injection and electron tunneling.**

***Index Terms*—AFGA, floating-gate circuits, second-order filters, second-order selections.**

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