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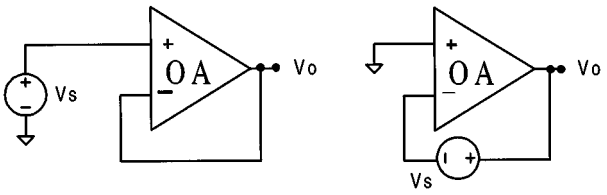

(a) (b)

Fig. 1. Proposed FVCVS technique. (a) Op amp in voltage follower configuration. (b) Grounding the opamp input and inserting a FVCVS in the feedback path.

Low-Voltage CMOS Operational Amplifiers with Wide Input–Output Swing Based on a Novel Scheme

J. Ramírez-Angulo, A. Torralba, R. G. Carvajal, and J. Tombs

***Abstract*—A scheme to achieve low-voltage wide-bandwidth operation of CMOS op -amps with rail-to-rail input and output swing and constant gm is presented. It is based on a novel concept that uses a floating voltage controlled voltage source in the feedback path of the op amp in order to keep its input terminals close to one of the supply rails. Postlayout simulations on a 1.2-V rail-to-rail op amp with 13 MHz GB are presented which verify the proposed scheme.**

***Index Terms*—CMOS analog integrated circuits, operational amplifiers.**

I. Introduction

Low-voltage op-amp operation requires, on the one hand, utilization of class-AB output stages to achieve wide output signal swing and, on the other hand, to maintain both op-amp input terminals close to one of the supply rails to reduce the supply requirements of the op-amp input stage. Several class-AB op amps have been reported that operate with a supply voltage close to a transistor's threshold voltage and that achieve rail-to-rail output swing [1]–[4]. These schemes are restricted to discrete-time operation. We present here a novel scheme that allows implementation of low-voltage continuous-time (and discrete-time) CMOS amplifiers with wide bandwidth, wide input and output signal swings and constant transconductance gain.

II. The Floating VCVS Technique

Traditionally, rail-to-rail input swing operation is based on the use of complementary MOS differential input stages. This technique is restricted for supply voltages greater than two threshold voltages. In this section, a technique is introduced that allows almost rail-to-rail input signal supply with a total supply close to a transistor's threshold voltage. To introduce the proposed technique let us consider an op amp in voltage follower configuration [Fig. 1(a)]. Assuming that a PMOS differential pair is used at the input stage, both inputs should operate at ground potential and a very small swing would be available for the input voltage source V_s.

The proposed technique grounds the positive op-amp input and reproduces the input signal as a floating voltage controlled voltage source (FVCVS) in the feedback path of the op amp [Fig. 1(b)]. In this way, the op-amp input stage consists of only one PMOS differential pair which always operates with both inputs at ground potential. The proposed technique provides the amplifier with rail-to-rail input swing and constant transconductance gain (g_m), remaining functional even for a very low supply voltage.

The technique proposed here is the first one that allows very low-voltage supply continuous-time operation with rail-to-rail input swing, constant g_m, and high-input impedance. The techniques used in [2]–[4] keep the op-amp input terminals close to a supply rail but can only be used in sampled-data schemes, since they are based on charge compensation techniques using switched capacitors. A continuous-time counterpart to these techniques was reported in [5] but lacks high-input impedance and only allows implementation of inverting amplifiers. In [6] a continuous-time technique for 1-V supply operation based on bulk-driven transistors is described. This technique causes a reduction in the transconductance gain and for this reason, it has serious limitations regarding frequency response, noise, and signal dependent g_m.

III. A Practical Implementation

A low-voltage implementation of the FVCVS technique is shown in Fig. 2. The voltage-to-voltage transfer is split into two steps: 1) a voltage-to-current conversion [Fig. 2(a)] where ideally a current $Ib = V_s/R$ is obtained and 2) a current-to-voltage conversion [Fig. 2(b)] where an output voltage $V_o = Ib \cdot R = V_s$ is obtained.

The voltage-to-current conversion is achieved by means of the transadmittance amplifier depicted in Fig. 2(a). It has a resistor R and two matched current sources, whose value I_b is forced by the feedback loop to take a value $I_b = (V_s - V_{\rm ref})/R$. To this end, an amplifier (denoted DA) compares a reference voltage $V_{\rm ref}$ to the voltage at node C. DA generates a voltage at node A which controls the current I_b in the resistor R connected between the input signal source V_s and node C. Low-voltage mirroring techniques are used to replicate I_b on the bottom of the circuit by means of the control voltage at node B. Although, in the ideal case $V_{\rm ref}$ can be tied to ground, in the practical implementation the bottom current source requires a minimum voltage of $V_{\rm DSsat} = V_{\rm GS} - V_t$ to operate. $V_{\rm DSsat}$ (and, hence, $V_{\rm ref}$) can be selected to have a value as small as 0.1 V. Notice that, since both input terminals of DA are at $V_{\rm ref}$ potential, the amplifier DA can operate with a single supply voltage close to a transistor's threshold voltage. In the ideal case, the input impedance is infinite, although in the practical implementation the input impedance is determined by the impedance of the I_b current sources.

The current to voltage conversion [(Fig. 2(b)] is achieved in a similar way by means of a transresistance amplifier. A resistor with value R and two current sources with value I_b are placed in the feedback path of the main operational amplifier OA, whose positive input terminal is also connected to $V_{\rm ref}$. Negative feedback leads to an output voltage $V_{\rm out} = I_b R + V_{\rm ref} = V_s$. Similarly to the previous case, a minimum voltage $V_{\rm ref} = V_{\rm DSsat}$ is required for operation of the bottom current

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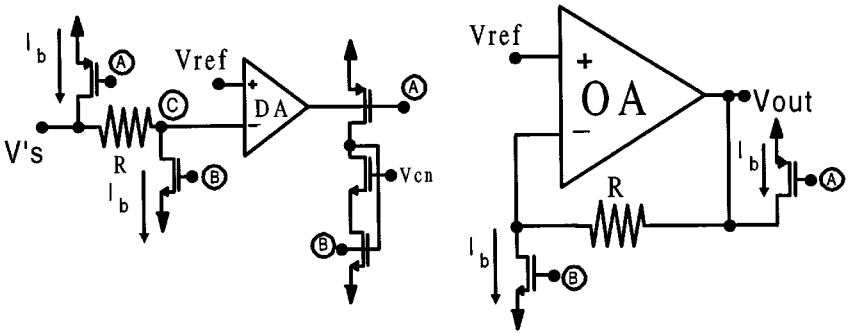
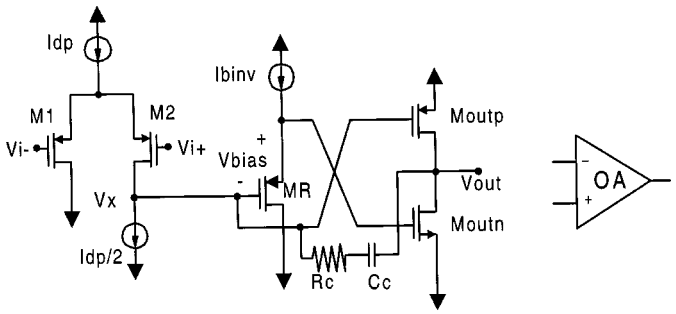


(a) (b)

Fig. 2. An implementation of the FVCVS. (a) STEP 1: Voltage-to-current conversion with an auxiliary opamp DA. (b) STEP 2: Current-to-voltage conversion inserting the FVCVS in the feedback path of the main operational amplifier OA.



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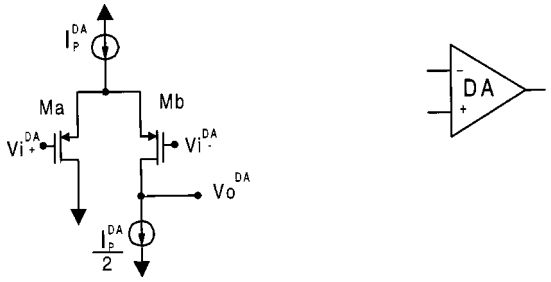
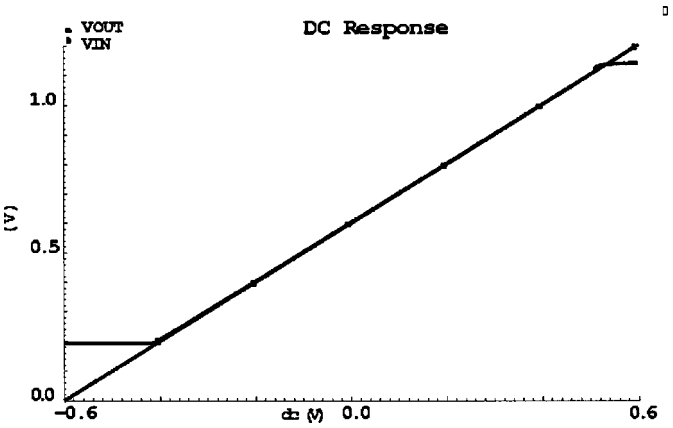
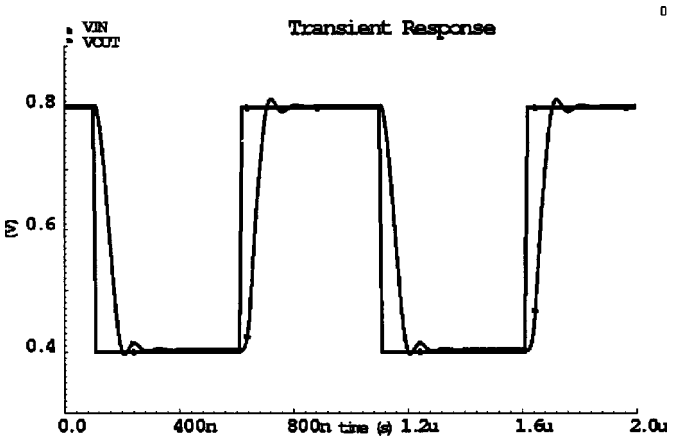


(b)

Fig. 3. Low-voltage implementations: (a) Main op amp OA. (b) Auxiliary op amp DA.



(a)



(b)

Fig. 4. Post-layout simulations. (a) DC-transfer characteristic. (b) Pulse response.

source. Notice that for an ideal op amp, the current source located in the op-amp output terminal is not necessary, although in the practical implementation this source is convenient to prevent increasing the input offset voltage of the op amp.

In both steps the input terminals of the amplifiers (OA and DA) operate at $V_{\rm ref}$, which enables operation with a supply voltage close to a transistor's threshold voltage. Fig. 3 shows the possible implementation of the amplifiers of OA and DA. OA is a two-stage class-AB low-voltage amplifier with rail-to-rail output swing [5]. DA is a simple differential pair with active load. Both implementations can operate with a total supply close to a transistor's threshold voltage.

IV. Simulated Results

Fig. 4 shows postlayout simulations of the dc transfer characteristic and the pulse response of the unity gain amplifier. For simulations, 0.8-μ CMOS technology parameters of the AMS-CXQ process extracted from a layout were used. A value $R = 20$ KΩ and W/L of $200/2$ and $90/2$ were used for P and N transistors in DA and for the current sources. A single supply voltage $V_{\rm DD} = 1.2$ V and a capacitive load $C_L = 10$ pF was used. In Fig. 4(a) near rail-to-rail input and output signal swings can be observed. Simulated gain-bandwidth product was 13 MHz. The simulated THD for a 150-KHz sinusoidal input was 0.09%. The total equivalent input noise in the bandwidth of the circuit was 127 μ V and the input noise power density at 100 kHz was 48 nV/$\sqrt{\rm Hz}$. The quiescent power consumption was 70 μ W.

V. Implementation of Amplifiers with Gain A Based on the FVCVS Technique

Simple extension of the FVCVS technique allows implementation of low-voltage amplifiers with a nominal gain A. For this, the current

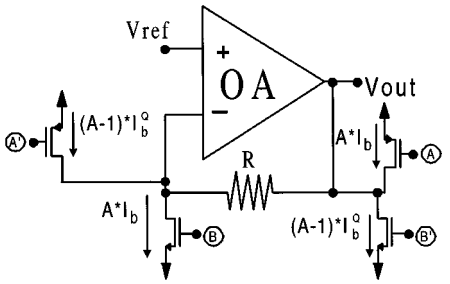


Fig. 5. Implementation of an amplifier with gain A using the FVCVS technique. This circuit replaces the circuit in Fig. 2(b). I_b and I_b^Q are obtained using two copies of the circuit in Fig. 2(a), with inputs V_s and V_s^Q, respectively.

$I_b = V_s/R$ generated in the first stage is scaled by the factor A (using a current mirror) and the resulting current $I_b' = A \cdot I_b$ is transformed into an output voltage $V_o = I_b' \cdot R = A \cdot I_b \cdot R = A \cdot V_s$ in the second stage. Cancellation of common mode components is required as explained below.

Consider following notation: let V_s^Q denote the DC value of the input signal source V_s, which, for the sake of simplicity, is also assumed to be the DC value of the op-amp output terminal $V_{\rm out}$. Let v_s denote the signal component of the input signal source V_s, so that $V_s = V_s^Q + v_s$.

In order to obtain an amplified output voltage, a floating VCVS with value $V_f = A \cdot v_s + V_s^Q - V_{\rm ref}$ must be inserted in the feedback path of the main op amp OA. Coming back to Fig. 2(a), $I_b = (V_s - V_{\rm ref})/R = (v_s/R) - I_b^Q$, where $I_b^Q = (V_s^Q - V_{\rm ref})/R$ is the DC value of the current source I_b.

Simple calculations lead to $V_f = [AI_b - (A-1)I_b^Q] \cdot R$ and to $V_o = A \cdot v_s + V_s^Q$. Hence, the implementation of V_f uses a resistor R and two pairs of matched current sources with values $A \cdot I_b$ and $(A-1) \cdot I_b^Q$. In order to achieve subtraction, the currents $A \cdot I_b$ and $A \cdot I_b^Q$ must flow through R in opposite directions, as shown in Fig. 5. The current I_b is obtained using the circuit in Fig. 2. Another copy of that circuit is used to generate I_b^Q using an input voltage $V_s = V_s^Q$. The technique introduced here can be easily extended to implement fully differential amplifiers. This will be discussed in detail in a future publication.

General Building Block of Low-Voltage Linear Systems: Notice that the proposed approach allows also low-voltage implementation of the linear weighted addition which is the basic operation of linear systems. This can be done by weighting currents $I_1 = V_1/R \ldots I_n = V_n/R$ generated in transconductance stages by factors $A_i \ldots A_n$ and then applying the summation of these currents to a transresistance stage to transform them into an output voltage $V_o = R \cdot (A_i \cdot I_1 + \cdots + A_n \cdot I_n) = A_1 \cdot V_1 + \cdots + A_n \cdot V_n$. Common mode components can be cancelled using the same technique discussed above.

VI. Conclusion

A novel technique to implement low-voltage CMOS amplifiers with rail-to-rail input swing, operating from a supply close to a transistor's threshold voltage, was introduced. Its practical implementation was discussed and functionality was demonstrated based on postlayout simulations. This technique offers potential for the implementation of low-voltage linear systems operating in continuous time.

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Low-Distortion CMOS Complementary Class E RF Tuned Power Amplifiers

Steve Hung-Lung Tu and Chris Toumazou

***Abstract*—A low-distortion tuned power amplifier which is suitable for integrated circuit implementation is proposed. The amplifier is a complementary class-E tuned power amplifier because of both P-type and N-type transistors are employed to achieve a highly symmetrical topology, thereby reducing the significant distortion in the output signal of the conventional single-ended class-E power amplifier. In this paper, a complementary class-E power amplifier is presented together with HSPICE simulation results.**

***Index Terms*—CMOS circuits, radio frequency, tuned power amplifiers, wireless transceivers.**

I. Introduction

The class-E tuned power amplifier has been an important building block in the wireless RF transceiver system for the past several years [1]. This is due to its high power efficiency [2], simplicity, and relatively high tolerance to circuit variations [3]. Recently, much research has focused on analysis as well as implementation issues of class-E amplifiers [4]–[6]. Fig. 1 shows the configuration of a conventional single-ended class-E power amplifier. Since the transistor acts as a switch rather than an amplifier, large-gate-width transistors are necessary in order to approach the ideal switch. However, the transistors also lead to large parasitic junction capacitances. For class-E power amplifiers, since the capacitance of the resonant circuits are different in switch-on and switch- off states, it leads to harmonic distortion of the output signal. Therefore, a higher performance RF passive filter is required after the power amplifier [7]. This requirement, however, may lead to a larger insertion power loss through the RF filter and reduces the power efficiency of the power amplifier by lowering the output power at the antenna for a given input power. In addition, for integrated implementations, this approach not only consumes a large chip area but it also presents difficulties in obtaining high-Q inductors. It has shown that monolithic inductors have often been limited to 10

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