Chapter 12
The Flipped Voltage Follower: Theory and Applications

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Abstract. The "flipped voltage follower (FVF)" is an enhanced buffer cell widely employed for low-power and/or low voltage operation. The applications of the FVF and its variations in analog and mixed signal (AMS) circuit design have increased continuously over the last few years. These are specially promising in deep submicrometer CMOS technology. In 2004 the paper "The Flipped Voltage Follower: A useful cell for low-voltage low-power circuit design" was published [1], where the most important information about this versatile cell was compiled. Since then, several modifications of the FVF and a wide variety of new applications have been reported. No other article with a similar purpose has been published since then. The aim of this chapter is to make a compendium summarizing some of the most relevant information published to date on the FVF. In order to facilitate AMS designers the utilization of this cell in this chapter we revisit, classify and summarize most applications of the basic FVF and its variations. Although it is tutorial in nature, it can be helpful for those who want to introduce themselves in the study of this cell or for experienced designers who want to become familiar with the principle of operation, improved versions and applications, so that both can exploit to its maximum the potential of the FVF in a wide number of applications or also to develop new ones.

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12.1 Introduction

The interest in low voltage analog cells has increased in recent years since the downscaling of CMOS processes has forced analog circuits to operate with continuously decreasing supply voltages. The demand for low voltage systems has been driven mainly by the need to reduce power consumption of the digital circuitry in mixed-signal very large-scale integrated (VLSI) systems, to prevent oxide breakdown with decreasing gate-oxide thickness and also to satisfy the requirements of the portable electronic equipment market. The reduction of supply voltages has forced to reconsider or modify many of the existing CMOS analog building blocks. In fact, some of them are not functional at all in the reduced supply environment of current CMOS technology.

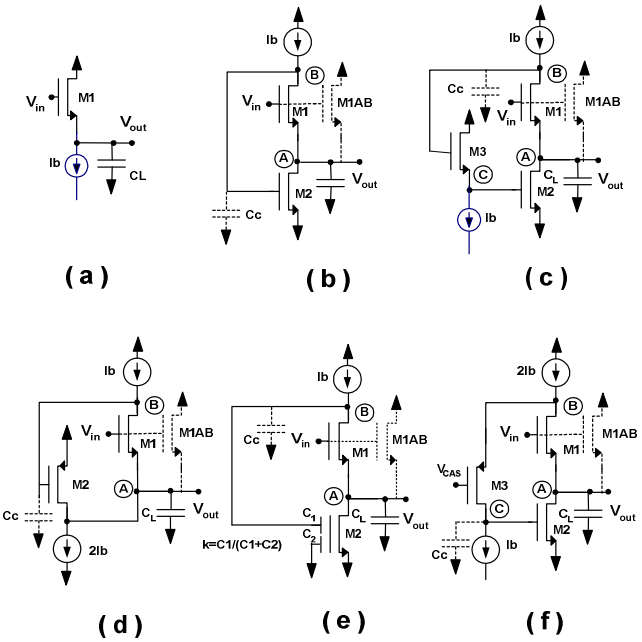

Fig. 12.1 Voltage followers: (a) Conventional Voltage follower (VF), (b) Flipped voltage follower (FVF), (c) Flipped voltage follower with VF level shifter (LSFVF), (d) Folded flipped voltage follower (FFVF), (e) Flipped voltage follower using floating gate level shifter (FGFVF), (f) Cascoded flipped voltage follower (CASFVF)

The voltage follower (VF, Fig. 12.1(a)), also known as source follower, is one of the basic building blocks of analog VLSI systems. The VF is biased on the source side with a constant current source I_b which ideally keeps the gate-source voltage V_{GS} of M1 constant. If body effect is neglected, the output follows the input voltage with a DC level shift, i.e., $V_0 = V_{in} - V_{GS}$. This feature, together with its high input impedance, relatively low output impedance $R_{out}=1/g_{m1}$ (in the range

of few kΩ) high bandwidth $BW=g_{m1}/(2\pi C_L)$ and large input/output swing $V_{inpp}=V_{DD}-(V_T+2V_{DSsat})$ are the main reasons why the VF is used as a voltage buffer. Following notation is used throughout this chapter: V_{DSsat} is the drain-source saturation voltage, V_{GS} the gate-source voltage, V_T and g_m the transistor's threshold voltage and small signal transconductance gain.

Nevertheless, in practice, the VF suffers from various problems: a) In many applications the output resistance is not low enough. It can be decreased only by increasing the transconductance gain g_m. This requires a large bias current and/or large W/L dimensions. b) The output current is given by $I_{out}(\omega)=V_{out}\omega C_L$ and the drain current is $I_{D1}(\omega)= I_b-I_{out}(\omega)$. Given that I_{out} is a function of the input signal, the gate-source voltage of M1 varies with the input signal, which leads to distortion that increases at high frequencies. c) The slew rate is non-symmetrical since the sourcing capability is very large, while the sinking capability is limited by the bias current I_b. The Flipped Voltage Follower (FVF) is an enhanced voltage follower cell that overcomes some of the limitations of the VF [1]. In this chapter we summarize its characteristics, implementations and applications.

This chapter is structured as follows: In section 2 the basic single input, single branch FVF is presented and discussed together with six improved modifications, which overcome some of its limitations. In section 3, a detailed study and classification of low-voltage/low-power CMOS circuits based on the FVF is shown. In section 4, new FVFs with differential input are presented and discussed. In each section we revisit the applications of the different FVF cells in linear and nonlinear circuits that were reported originally and summarize new applications that have been reported since then. Although for the sake of space some remarks are just made on the applications of the different cells, the authors have made their best to compile a comprehensive (but not exhaustive) list of references. The chapter is finished with the conclusions drawn in section 5 where we summarize the most important facts of the FVF and hint at possible future applications.

12.2 Single Input FVF Structures

12.2.1 Flipped Voltage Follower

The basic FVF (Fig. 12.1(b)) corresponds to a voltage follower with improved characteristics [1]. In fact, it can be described as a cascode amplifier with negative feedback where the gate terminal of M1 is used as the input and its source as output voltage. It is characterized by very low output impedance $R_{out} = 1/(g_{m2}g_{m1}r_{o1})$ (tens of Ωs), high current sinking capability, very low supply requirements ($V_{DDmin}=V_{GS2}+V_{DSsat}$) close to a transistor's threshold voltage, low static power dissipation and high gain-bandwidth $GB=g_{m2}/(2\pi C_c)$. Output current variations are absorbed by the current sensing transistor M2, keeping the current in M1 essentially constant. Neglecting body effect and channel modulation, the gate-source voltage of M1 remains also constant. As a result, distortion remains low even at high frequencies. In the basic FVF of Fig. 12.1b, the output swing of M1 is 'strangled' by the gate-source voltage V_{GS2} of M2. This leads to a small input/output

peak-peak swing $V_{inpp} = V_T - V_{DSsat}$. Unlike the case for most circuits, swing does not increase with the supply voltage V_{DD}. This is a severe limitation in modern deep sub-micrometer CMOS technology with V_T~0.4V peak-to-peak input/output swing is very small, typically $V_{inpp} < 300$mV.

12.2.2 FVF with Level Shifter

A possible solution to overcome the problem of the small input/output swing of the FVF is to include a DC level shifter between the drain of M1 and the gate of M2 [2]. Fig. 12.1(c) shows a modified version of the FVF that includes a DC level shifter (transistor M3) using a conventional voltage follower (LSFVF). In this circuit the input/output swing is increased by the DC level shift of the follower (V_{GS}) to a value $V_{inpp}=2V_T$, which is still independent of V_{DD} and might still be small in modern CMOS technologies. Bandwidth is moderately degraded due to the introduction of an additional high frequency pole at node C in the negative feedback loop formed by M1-M2 and M3. In addition, the introduction of M3 increases the quiescent power consumption and the minimum supply requirements of the circuit to the relatively high value $V_{DDmin}=2V_{GS}+V_{DSsat}$.

12.2.3 Folded Flipped Voltage Follower

In the folded flipped voltage follower (FFVF) or 'super source follower' [3] (Fig. 12.1(d)), the current sensing transistor M2 is folded (the NMOS is replaced by a PMOS transistor) by introducing an additional biasing source $2I_b$, making the FFVF to require additional power dissipation. The gain-bandwidth product is given by $GB=g_{m2}/(2\pi C_B)$, where C_B is the capacitance at node B. Given that all FVF structures are negative feedback structures, stability requires a dominant pole which should limit the gain bandwidth product (GB) to a value typically one half to one third of the effective high frequency pole of the open loop.

The effective high frequency open loop pole for the FVF, the LSFVF and the FFVF is given by $f_{phf}=f_{pout}=g_{m1}/(2\pi C_L)$. In general the additional high frequency pole introduced by M3 at node C is at much higher frequency than the pole at the output node. This assumption is valid if the load capacitance C_L is much greater than the parasitic capacitance at node C. In order to ensure stability in all FVF circuits (including the ones to be discussed below) a small compensation capacitor C_c can be used at node B to introduce a dominant pole that limits the gain bandwidth product to a value $GB=g_{m2}/(2\pi C_c)$.

12.2.4 Flipped Voltage Follower with Floating Gate Level Shifter

In the Flipped voltage follower with floating gate level shifter (Fig. 12.1(e)), denoted as FGFVF [2], the DC level shifting is achieved by using for M2 a two input floating gate transistor with capacitors C_1 and C_2 connected to the drain of M1 and to V_{SS} (ground) respectively. Capacitors C_1 and C_2 form a capacitive voltage divider, and based on charge conservation [4] the voltage at the gate of M2 is given by $V_{GS2} = kV_{D1}$ where $k = C_1/(C_1+C_2)$. Therefore, the voltage at the drain of M1

will be $V_{D1} = V_{GS2}\ (1+C_2/C_1)$. In this circuit V_{D1} is level shifted by $(C_2/C_1)V_{GS1}$ with respect to V_{GS1}. The minimum supply requirements of this circuit are given by $V_{DDmin} = V_{GS2}\ (1+C_2/C_1) + V_{DSsat}$.

12.2.5 Cascoded FVF

In the cascoded FVF [2] or CASFVF (Fig. 12.1(f)) a PMOS cascoding transistor M3 is introduced between the gate of M2 and the drain of M1. This transistor MC provides additional gain to the FVF negative feedback loop, leading to an extremely low output resistance $R_{out}=1/[g_m(g_m r_o)^2]$ (tenths of Ω). The quiescent voltage at the drain of M1 is set by the cascode biasing voltage of MC, with a value $V_{D1}=V_{CAS}+V_{SG,MC}$ that can be close to V_{DD}, in order to maximize the signal swing. The minimum supply requirements are $V_{DDmin}=V_{GS}+2V_{DSsat}$. The peak-to-peak output swing is dependent on V_{DD} and given by $V_{outpp}=V_{DD}-3V_{DSsat}$. An advantage of the CASFVF with respect to other FVF configurations is that due to the additional loop gain provided by MC, the voltage variations at the drain of M1 are reduced by the factor $g_m r_o$ (the gain of MC) with respect to those at the gate of M2. In this case lambda effect on M1 and on the transistor acting as biasing current source $2I_b$ are minimized.

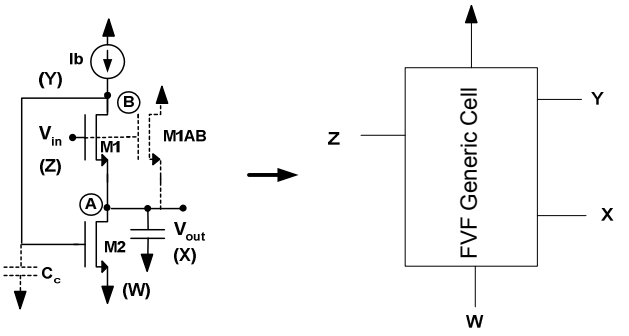

Fig. 12.2 Generic FVF cell. Note the identification of nodes: X is the low impedance node corresponding to the source terminal of the input transistor M1 (Node A), Z is a high impedance node corresponding to the gate terminal of the input transistor M1 (V_{in}), Y is a moderate low impedance node corresponding to the gate terminal of the current.

12.2.6 Other Improvements of Single Input FVF Structures

As can be easily identified from the FVF cell and its variations presented above all these cells are characterized by the presence of three terminals X, Y and Z (Fig. 12.2), where Z is a very low impedance node, Y is a moderate low impedance node (with value $1/g_{m2}$) and Z is a high impedance node. In this way, in node X current may be taken as the input or output variable, while voltage is the input or output variable for nodes Y and Z. An additional low impedance node W can be identified, which is the source terminal of the current sensing transistor M2, and

that is usually connected to a rail. For simplicity in notation and generality, from here onwards, we will refer to the FVF as the FVF generic cell with four terminals X, Y, Z and W presented in Fig. 12.2. The following techniques can be applied both separately or combined.

12.2.6.1 Class AB Operation of Single Input FVF Structures

Similar to the conventional voltage follower, all FVF structures are characterized by nonsymmetrical slew rate. They all have large current sinking capability but their current sourcing capability is limited to the bias current I_b. A simple modification of the basic FVF [5]-[6] consists of including an additional input transistor M1AB with its drain terminal connected to V_{DD}, that provides class AB operation with both large current sourcing and sinking capabilities. This simple solution can be used in all FVF structures discussed above as shown in Figs. 12.1 and 12.2 in discontinuous trace. Although M1AB increases quiescent current dissipation by I_b (assuming same W/L for M1 and M1AB), it allows class AB operation with large positive and negative output currents $I_{out}>>I_b$. Table 12.1 shows a comparison summarizing the characteristics of the single input FVFs discussed and those of the conventional voltage follower.

Table 12.1 Comparison of buffer performance characteristics

Single Input Buffer comparison					
Circuit	**R_{out}**	**V_{DD}^{min}**	**V_{outPP}**	**GB**	**I_{DD}**
VF	$1/g_m$	$V_{GS}+V_{Dsat}$	$V_{DD}-V_{DD}^{min}$	g_{m1}/C_L	Ib
FVF	$1/(g_m(g_m r_o))$	$V_{GS}+V_{Dsat}$	V_T-V_{Dsat}	g_{m2}/C_c	Ib
LSFVF	$1/(g_m(g_m r_o))$	$2V_{GS}+V_{Dsat}$	$2V_T$	g_{m2}/C_c	2Ib
FGFVF	$1/(kg_m(g_m r_o))$	$V_{GS}/k+V_{DSsat}$	$V_{GS}/k-2V_{DSsat}$	kg_{m2}/C_c	Ib
FFVF	$1/(g_m(g_m r_o))$	$V_{GS}+2V_{Dsat}$	$V_{DD}-V_{DD}^{min}$	g_{m2}/C_c	2Ib
CASFVF	$1/g_m(g_m r_o)^2$	$V_{GS}+2V_{Dsat}$	$V_{DD}-V_{DD}^{min}$	g_{m2}/C_c	2Ib

12.2.6.2 Non Trapped Current Single Input FVFs

In all FVF cells discussed above, the current that flows in the current sensing transistor M2, I_{FVF}, is 'trapped', that is, it is not available as an output current. It can be replicated using mirroring techniques by tying the gate of an additional mirroring transistor to V_B. However, current mirroring inevitably introduces distortion and degrades the circuit's frequency response. This is especially critical in the implementation of highly linear OTAs [7].

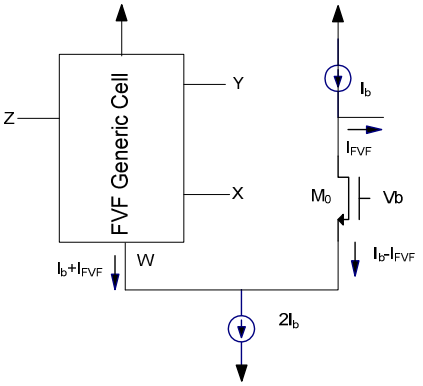

Fig. 12.3 Current 'de-trapping' technique

A solution to overcome this problem is to use the scheme depicted in Fig. 12.3 for NMOS input transistor. As it can be seen, now node W (the source of the current sensing transistor M2 in Fig. 12.2) is connected to a constant current source instead of being tied to a rail. In this way, the current I_{FVF} is transferred to transistor M_0 whose current equals $I_0 = I_b - I_{FVF}$. The additional component I_b is subtracted at the drain of M_0, leading to an output current $I_{out} = I_b - I_0 = I_{FVF}$, which is free of the distortion and the degradation in frequency behavior introduced by current mirroring. The output node is a high impedance, high swing node. In addition to its simplicity, this technique can be applied to any of the FVF cells discussed above.

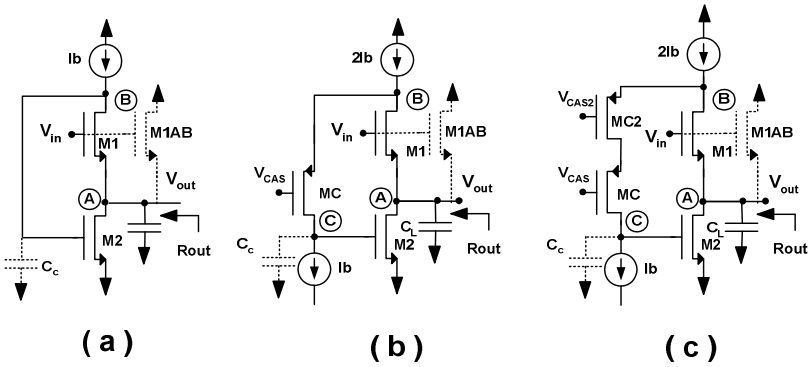

Fig. 12.4 Illustration of multiple cascoding technique: (a) Basic FVF, (b) Cascoded FVF, (c) double cascoded FVF using additional cascode transistor MC2

12.2.6.3 Multiple Cascoding Techniques

Note that the performance of FVF cells can be improved at no cost in power consumption by including additional cascode transistors in the negative feedback loop of the FVF. This leads to an increase in the open loop gain of the FVF cell with

the consequent further reduction of the output resistance at node A by a factor $A_i = g_{mi}r_{oi}$ for each additional cascoding stage. This has very little effect on the phase margin since cascode transistors introduce very high frequency poles in the feedback loop. Fig. 12.4 illustrates how the conventional FVF (Fig. 12.4(a) with $R_{out}=1/[g_m(g_m r_o)]$) is transformed into the cascoded FVF (Fig. 12.4(b) with $R_{out}=1/[g_m(g_m r_o)^2]$) by adding a cascode transistor MC. Fig. 12.4(c) shows the addition of another cascode transistor, MC2, to achieve an extremely low output resistance with value $R_{out}=1/[g_m(g_m r_o)^3]$.

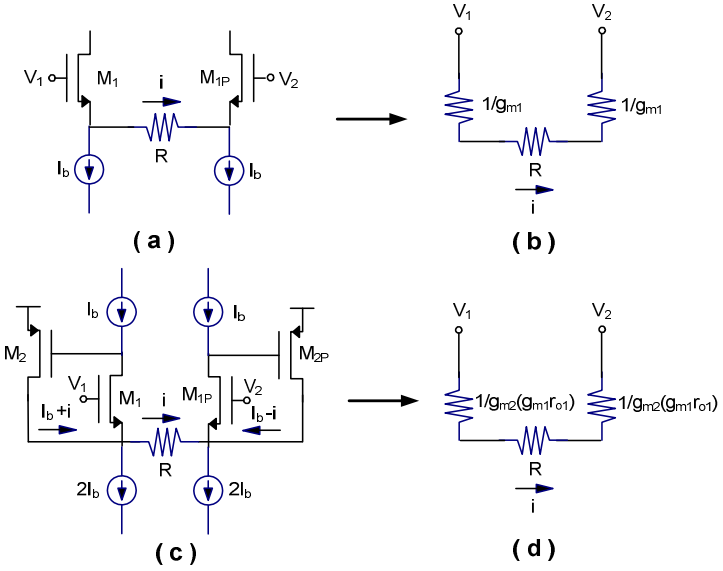

Fig. 12.5 (a) Source degeneration technique, (b) Equivalent circuit, (c) FVF CMOS linear transconductor employing source degeneration technique, (d) equivalent circuit of (c)

12.2.7 Applications of Single Input FVF Structures

As said before, the FVF can be seen as a high performance buffer. Therefore the basic applications of the FVF are those in which a high performance buffer is required. One example is in the implementation of linear CMOS transconductors. Linearization techniques have to be used to reduce the total harmonic distortion (related to the quadratic relation of the output current into the input voltage in a MOS transistor operating in saturation). A commonly used linearization technique is based on source degeneration [8], in which a resistor R is connected between the sources of a differential pair (Fig. 12.5(a)). Fig. 12.5(b) shows the equivalent circuit of Fig. 12.5(a), in which we have neglected the output impedance of the bias currents I_b and those of the input transistors. The input voltage $V_{i\ (i = 1, 2)}$ of each input transistor is translated into its source $V_{Si\ (i = 1, 2)}$ with a level shift. In this way, $V_{Si} = V_i - V_{shift}$, where V_{shift} depends inversely on their transconductance g_{mi}.

If $g_{m1} = g_{m2} = g_m$, the current which flows in the linear resistor R is given by $i = (V_1 - V_2)/((2/g_m) + R)$. If $R >> 2/g_m$, then $G \approx i/(V_1 - V_2) = 1/R$, and the transconductance G is linear since it only depends on R and not in the non-linear resistor $r_{nl} = 1/g_m$, (whose value depends on the current i and input voltage V_i). In this way, linearity increases, but the price paid is that the transconductance G decreases inversely. Note that the gain bandwidth product (GB) and signal to noise ratio (SNR) of a circuit with OTAs is proportional to the transconductance gain. A possible solution to improve GB and SNR would be to reduce the value of r_{nl}, so R can be lower (and G higher). This requires a larger bias current and/or large transistor dimensions in the differential pair. An alternative is shown in Fig. 12.5(c) [9] the input pairs have been replaced by FVFs (actually FFVFs). In this case $r_{nl} = 1/(g_{m2}g_{m1}r_{01})$, which is much smaller than in the previous case, and $G = 1/[2/(g_m^2 r_0) + R]$ where we have assumed $g_m = g_{m1} = g_{m2}$, $r_{o2} = r_o$. In addition, the frequency response of the system is unaltered, since the bandwidth of the FVF is the same as a conventional voltage follower. Note that in this case it is possible to use a much smaller R value corresponding to a much higher linear transconductance gain $G \approx 1/R$ (with correspondingly higher GB and SNR).

In fine line CMOS technologies, the transistor's intrinsic gain $A_i = g_m r_o$ has decreased drastically which has resulted in decreased open loop gain of conventional Op-Amp architectures. For example, in one stage Op-Amps the gain bandwidth product (GB) and A_{OL} are given by $GBW \approx g_{mDP}/C_L$ and $A_{OL} \approx g_{mDP} \cdot R_{OUT}$ respectively, where C_L is the capacitive load connected to the output of the Op-Amp, R_{OUT} is the output resistance and g_{mDP} is the transconductance gain of the input differential pair. In a conventional Op-Amp $g_{Mdp} \approx g_m$, corresponds to the transconductance gain of the input stage transistors. One possible solution to tackle the problem of low intrinsic gain in modern CMOS technology is to increase g_{mDP} by replacing the differential input stage by the circuit of Fig. 12.5(c) with R=0 [9]. In this case the effective transconductance gain g_m'is given by $g_m' = g_{m1}g_{m2}r_{o2} \approx g_m^2 \cdot r_0$. Therefore, both GB and AOL are increased by the factor $A_i = g_m r_o$ achieving $GB \approx g_m^2 \cdot r_0/C_L$ and $A_{OL} \approx g_m^2 \cdot r_0 \cdot R_{OUT}$. Note that the g_m enhancement factor depends on the FVF used. For example, if the cascoded FVF is used instead of the FFVF of Fig. 12.5(c) the gm (and gain) enhancement factor is A_i^2.

12.3 Basic Single Input FVF Based Structures

For simplicity, in this section we will only refer to one implementation of the FVF, usually the basic one of Fig. 12.1(a). Note that, in every case, we can replace the FVF by the generic cell with four terminals X, Y, Z and W presented in Fig. 12.2. In this way, by FVF we can refer not only to the original FVF presented in section 2.1, but also to all improved FVF variations studied along section 2.

12.3.1 FVF Current Sensor (FVFCS)

The FVF can be used as a current sensing cell [1], where node X in Fig. 12.6(a) is the input current sensing node. This very low impedance node X can source large

current variations. They are translated by the FVF into compressed voltage variations at node Y. Fig. 12.6(b) shows the DC response of the circuit in Fig. 12.6(a). The output and the input currents are related through the expression $I_{out} = I_{in} + I_b$.

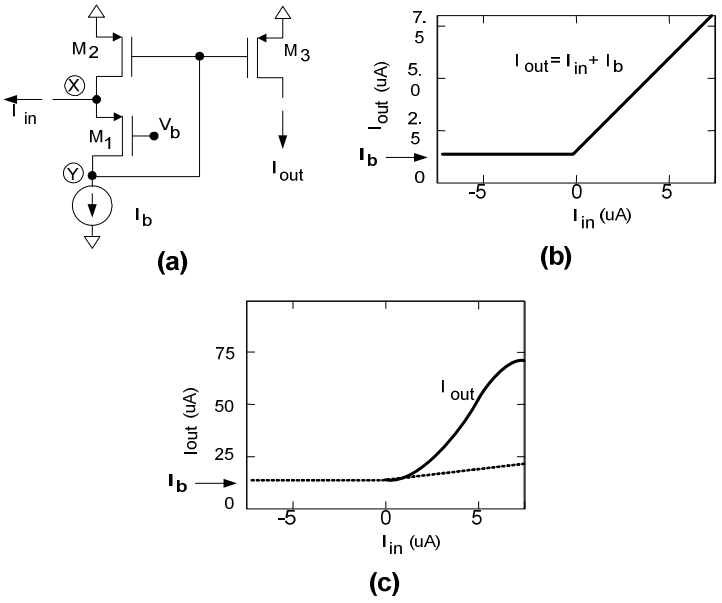

Fig. 12.6 FVF Current Sensor (FVFCS): (a) Basic implementation, (b) DC response with M_2 in saturation, (c) DC response with M_2 biased near the linear region

If transistor M2 is biased with voltage V_b near the linear region and M3 is maintained in the saturation region, the output current can increase by a very large factor compared to the input current (Fig. 12.6(c)). This is due to the fact that with input current increases M2 enters triode mode and a large source-gate voltage, V_{SG2}, is developed in M2. This can be used to achieve class AB operation as was demonstrated in [10].

12.3.1.1 FVFCS Applications

The FVFCS has been used in the past for different applications [11-13]. For example, in [12] the FVFCS was used as a part of a power amplifier. A well-known application is at the input stage of a high performance low-voltage current mirror [11,12,14], but many other applications exist, such as in digital IDDQ and Mixed-signal iDD testing [15], which is employed to detect the presence of faults in CMOS integrated circuits.

A recent useful application of the FVF has been found in Low Dropout Voltage Regulators (LDO) [16,17]. An LDO is a circuit which provides a nearly constant DC output voltage despite changes in load current or its input (supply) voltage with a small drop between its supply and output regulated voltage.

Generic LDO structures have two high impedance nodes and a tradeoff exists between accuracy and feedback stability: A high loop gain improves the line regulation and load regulation factors, but degrades closed-loop stability. Besides low drop in the pass transistor, stability is an important issue in LDOs because they are required to operate with a wide range of load currents. This causes very large variations in the output pole of the feedback loop. Therefore, different methodologies such as advanced pole–zero cancellation schemes, load-dependent reference voltage concept, pole-splitting schemes, and extremely large capacitive loads were proposed [16]. However, this increases the complexity and the power consumption and cost of the devices.

The properties of the FVF as an enhanced voltage buffer make it a simple and excellent solution to overcome these drawbacks. The FVF's low supply requirements and reduced output impedance due to shunt feedback connection [16], is the key for obtaining high regulation and achieving frequency compensation with wide load variations. The FVF has a feedback loop with only one high impedance node. In fact, the enhancement of the output resistance by means of cascoding techniques improves its characteristics in terms of line and load regulation, with negligible impact in stability. In addition, the FVF is very simple, can be biased with low currents and has very low drop, leading to high power efficiency.

12.3.2 FVF Differential Structure (FVFDS)

The FVF differential structure (FVFDS) is built by adding an extra transistor M3 connected to node X of the FVF cell, as it is shown in Fig. 12.7(a) [11]. As the impedance at node X is very low, its voltage remains approximately constant for large input currents.

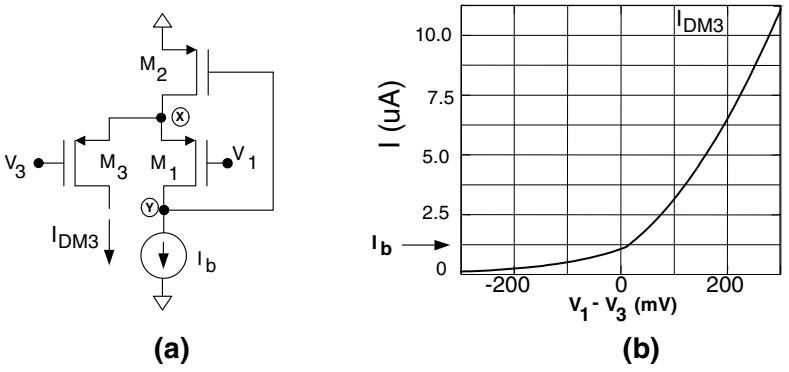

Fig. 12.7 (a) FVF Differential structure (FVFDS), (b) DC transfer characteristic

Under quiescent conditions (V_1=V_3) assuming that transistors M1 and M3 have the same size then $I_{DM1} = I_{DM3} = I_b$. A nonzero differential voltage V_1–V_3 adds to V_{SG3} and generates current variations in M3 that follow approximately the MOS square law. These current variations are supplied by M2. In this way, the FVFDS maximum output current I_{DM3} can be much larger than the quiescent current. Fig. 12.7(b) shows the DC transfer characteristic for I_{DM3} vs. V_1–V_3. The typical class AB behavior can be observed. On the other hand the FVFDS shows similar high common mode rejection (CMRR) as a conventional differential pair (DP). Since common mode input voltage variations do not lead to changes in IDM3.

12.3.2.1 FVFDS Applications

FVFDSs are mainly applied to build low-power, low-voltage, class-AB stages with a wide variety of applications: transconductance operational amplifiers [18], output stages [19] and buffers [1].

12.3.3 FVF Pseudo-Differential Pair (FVFPDP)

The FVF pseudo-differential pair (FVFPDP) is constructed from the FVF by adding an extra input transistor (M4) connected to node X, as it is shown in Fig. 12.8(a) [20].

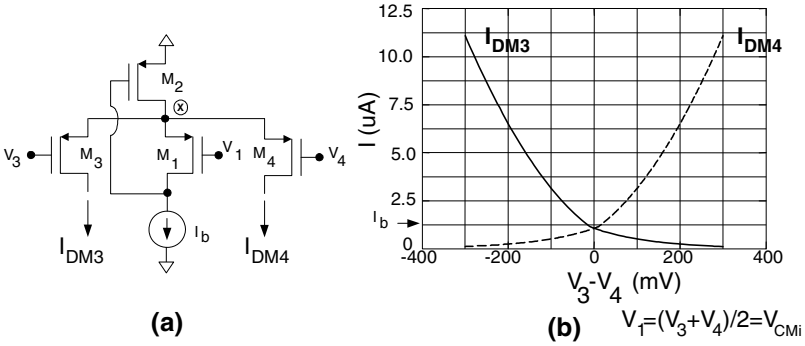

Fig. 12.8 (a) FVF Pseudo-Differential pair (FVFPDP), (b) DC transfer characteristic

Fig. 12.8(b) shows the DC output currents I_{DM3} and I_{DM4} versus the differential input voltage $V_{34} = V_3$–V_4, in a typical case. The pseudo-differential pair also exemplifies the characteristic behavior of a class-AB circuit, where the quiescent output current I_b can be much lower than the peak output current. In this case, we have considered that, under quiescent conditions, $V_1 = V_3 = V_4$. That is, the voltage at the gate of M1 corresponds to the common mode of M3 and M4: V_1=(V_3+V_4)/2=V_{CMi}. If the common mode value V_{CMi} of input voltages V_3 and V_4

is not equal to V_1 the DC output characteristic will have the same shape, but a DC level shift will appear.

The main difference between the FVFDS and the FVFPDP is that the latter has a true differential output. The output current I_{DM3} of the FVFDS can be large if V_1-V_3 is positive and zero if $V_1 - V_3$ is negative, while in the FVFPDP we can have positive or negative large differential output currents ($I_{out} = I_{DM3} - I_{DM4}$) depending on the value of the input differential voltage ($V_{in} = V_3 - V_4$). This pseudo-differential pair can be also operated with a minimum supply voltage of $V_{DDmin} = |V_{TP}| + 2\,|V_{DSsat}|$, as in the case of the FVFCS and FVFDS. The FVF formed by M1,M2 and Ib can be replaced by any of the variations discussed in section 2 in order to increase the input signal swing. The FVFPDP requires a common mode input voltage detector or complementary input signals with a well defined constant common mode voltage applied to the gate of M1. This is available in fully differential circuits where the common mode voltage of a signal is set by the output common mode feedback network of the previous stage.

12.3.3.1 FVFDP Applications

FVFPDPs can be applied as input stage in Class-AB Op-Amps [20], Class AB operational transconductance amplifiers for switched capacitor (SC) applications, Class AB operational transconductance amplifiers for continuous time operation [21] and multipliers [22].

12.3.4 Other Structures

The FVF cell can be used in many other applications such as in Translinear Circuits [1]: FVF Voltage Translinear loops and Static Nonlinear Circuits (Geometric-Mean circuit, Squarer/Divider circuit ([1], [23]), Multiplier/Divider circuit and Dynamic linear and nonlinear circuits [1].

12.4 Differential Input FVF Structures

12 4.1 Differential Voltage Follower (DVF)

Fig. 12.9(a) shows a simple buffer without DC level shift between the input and the output terminals. It consists of an active loaded differential pair with unity gain negative feedback (shown in dashed lines connecting nodes 2 and 3). This class A circuit has an output resistance given by $R_{out} = 1/g_{m1}$, gain-bandwidth product GB $= g_{m1}/(2\pi C_L)$ and symmetrical slew rate $SR = 2I_b/C_L$, which is determined by the maximum output current $I_{outMAX} = 2I_b$. The input swing is $V_{inpp} = V_{DD} - V_{SS} - 2V_{DSat} - |V_{TN}|$. The minimum supply voltage is $V_{DDMIN} = V_{GS} + V_{DSsat} + |V_{TP}| - V_{TN}$, while the output swing is $V_{outpp} = V_{DD} - V_{SS} - 2V_{DSat} - |V_{TN}|$.

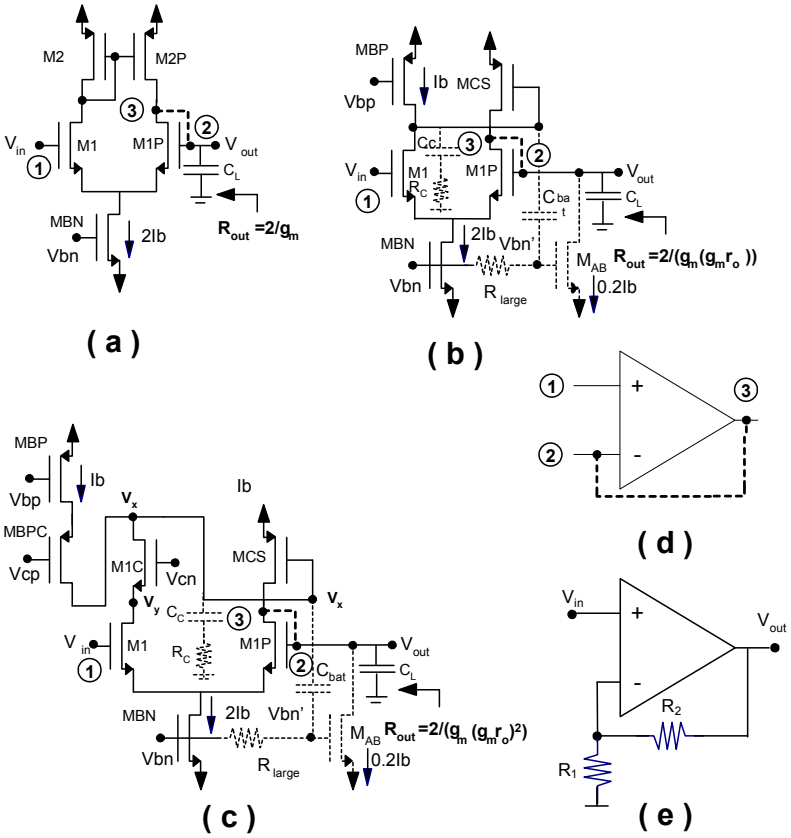

Fig. 12.9 Differential buffers: (a) Conventional DP buffer, (b) Differential FVF buffer (c), Cascoded Differential FVF buffer, (d) Generic differential amplifier representation, (e) DFVF used as op-amp with resistive feedback network

12.4.2 Differential Flipped Voltage Follower (DFVF)

The Differential Flipped Voltage Follower was reported as a part of a current conveyor in [24] and as general three terminal structure in [25]. The DFVF of Fig. 12.9(b) can be derived from the FVF of Fig. 12.1(b) by replacing the transistor M1 by a differential pair M1-M1P and a tail current source as explained in section 2.6.5 and illustrated in Fig. 12.5. This is done by diode connecting M1P and flipping the currents sensing transistor MCS from NMOS to PMOS type. Besides the fact that there is no DC level shift between the input and output, the input range V_{inpp} is higher than in the FVF, dependent on V_{DD}. It is given by $V_{inpp} = V_{DD} - V_{SS} - 3V_{DSat}$. The minimum supply voltage is $V_{DDMIN} = V_{GS} + 2V_{DSsat} - V_{TN}$, while the output swing is $V_{outpp} = V_{DD} - V_{SS} - 3V_{DSat} - V_{TN}$. Other features of this circuit are lack of body effect attenuation and low output resistance $R_{out}=1/[g_m(g_m r_o)]$ (~ 50Ω).

12.4.3 Cascoded Differential Flipped Voltage Follower (CDFVF) [24]

In Fig. 12.9(c) an additional cascoding transistor M1C is introduced in the negative feedback loop formed by M1-M1P, MCS and M1C. In this case the FVF corresponds to a folded double cascoded amplifier with unity gain negative feedback. M1C increases the open loop gain of the cascode amplifier negative feedback by the factor $g_{m1C}r_{o1C}$ and leads to an extremely low output resistance given by $R_{out}=1/[g_m(g_mr_o)^2]$ (~ tenths of Ω). The input swing is slightly reduced since the maximum input voltage now is given by $V_{inMAX} = V_{DD} - V_{SS} - 3V_{DSat} + V_{TN}$. The minimum supply voltage is $V_{DDMIN} = V_{GS} + 4V_{DSsat} - V_{TN}$, while the output swing is $V_{outpp} = V_{DD} - V_{SS} - 2V_{DSat} - V_{TN}$.

12.4.4 Other Improvements of Differential Input FVF Structures

12.4.4.1 Class AB Operation

The DFVFs of Fig 12.9(b) and Fig 12.9(c) are class A circuits characterized by nonsymmetrical slew rate. They all have large current sinking capability thanks to the current sensing transistor MCS but their current sourcing capability is limited by the bias current $2I_b$. Similar to single input FVFs, a simple modification of the basic FVF provides class AB operation to DVFVs with both large current sourcing and sinking capabilities. This modification is based on the quasi floating gate technique described in [26], and it is shown in discontinuous line in Figs. 12.9(b) and 12.9(c). It requires an additional transistor M1AB whose gate is connected to the DC biasing voltage V_{bn} through a very large valued resistive element R_{large} (~ 100 GΩ) and the connection of the gate of the current sensing transistor MCS through a capacitor C_{bat}. This transistor has a quiescent gate voltage $V_{bn}' = V_{bn}$ and small dimensions $(W/L)_{AB} = (W/nL)$ with $n > 3$ and for this reason it has a small quiescent drain current ($\sim 2I_b/n$). Under dynamic conditions R_{large} prevents flow of charge into the gate of MAB. For this reason C_{bat} performs as a floating battery so that V_{bn}' follows the gate voltage variations of MCS. During negative slewing (when a negative current flows into C_L), the current of M1 and M1P remains constant and the drain current if MCS increases so it does its gate voltage. As a consequence, the gate voltage V_{bn}' of MAB increases so that its drain current can increase significantly over the quiescent value $2I_b/n$. During positive slewing the gate of MCS decreases. Due to this it can provide very large positive currents to C_L which can be much larger than $2I_b$. At the same time MAB decreases its current and turns off.

As shown in Fig. 12.9(d) the DFVF can be seen as a more general three terminal amplifier (or Op-Amp) with two differential input terminals (1 and 2) and an output terminal (3). This was reported in [25]. As such it has an open loop output resistance $R_{out}=1/g_m$ and the same open loop gain $A_{ol}= g_mr_o/2$ as the conventional circuit of Fig. 12.16(a) which has a much higher open loop output resistance $R_{out}=r_o/2$. The circuits of Fig. 12.9(b) (and 12.9(c) with even higher open loop gain and lower output resistance) can be considered transposed versions of the conventional circuit of Fig. 12.9(a). They have the same power dissipation and complexity but given it

has lower open loop output resistance it can be used as a compact buffered Op-Amp and operate with resistive feedback as shown in Fig. 12.9(e). This is in general only possible using more complex two stage (or three stage) Miller op-amps.

Table 12.2 shows a comparison summarizing the characteristics of the differential input FVFs discussed and those of the conventional differential input voltage follower.

Table 12.2 Comparison of buffer performance characteristics

Differential Input Buffer comparison					
Circuit	$\mathbf{R_{out}}$	$\mathbf{V_{DD}^{min}}$	$\mathbf{V_{outPP}}$	$\mathbf{V_{inpp}}$	$\mathbf{I_{DD}}$
DVF	$1/g_m$	$V_{GS}+V_{DSsat}+\lvert V_{TP}\rvert - V_{TN}$	$V_{DD}-V_{SS}-3V_{DSat}$	$V_{DD}-V_{SS}-2V_{DSat}-\lvert V_{TP}\rvert$	2Ib
DFVF	$1/(g_m(g_m r_o))$	$V_{GS}+2V_{DSsat}-V_{TN}$	$V_{DD}-V_{SS}-3V_{DSat}-V_{TN}$	$V_{DD}-V_{SS}-3V_{DSat}$	2Ib
CDFVF	$1/(g_m(g_m r_o)^2)$	$V_{GS}+4V_{DSsat}-V_{TN}$	$V_{DD}-V_{SS}-5V_{DSat}-V_{TN}$	$V_{DD}-V_{SS}-5V_{DSat}$	2Ib

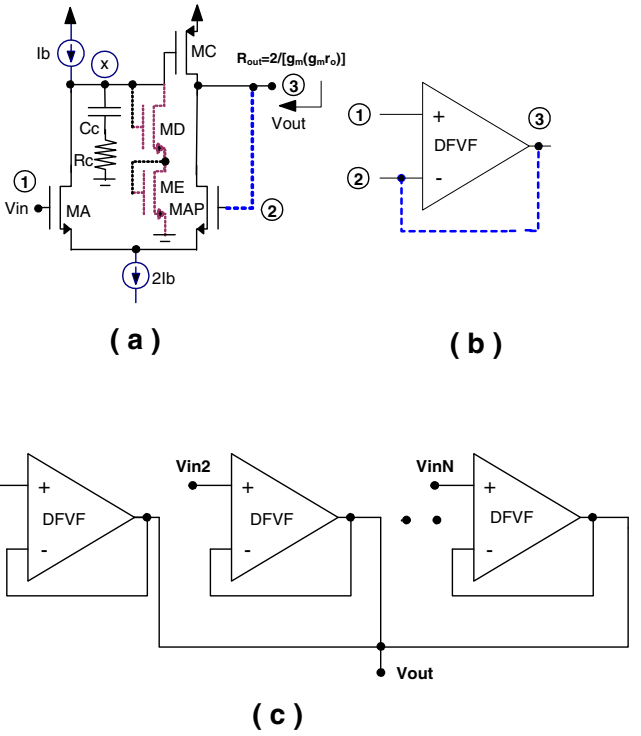

Fig. 12.10 (a) Differential flipped voltage follower cell, (b) Symbol, (c) WTA MAX Circuit based on DFVF cells with their output connected in parallel

12.4.5 Applications of the Differential Input FVF Structures

Due to its characteristics and compactness, the main application of differential input FVF structures are in high performance voltage buffers [25], but recently they have also been employed in non-linear circuits such as winner-take-all circuits (WTA) [27,28], programmable gain voltage amplifiers [29] and current conveyors [30].

WTA circuits are widely employed in non-linear systems. They are typically based on the parallel connection of identical buffer cells (driven by the input voltage or current signals) to a common low-impedance output node. Input signals "compete" to set the voltage at the output branch, so that, in a WTA, only the branch with the highest or lowest voltage or current input signal remains active and sets the output voltage (current), depending if the circuit performs the maximum (MAX) or minimum (MIN) function, respectively.

Fig. 12.10 shows an implementation of a high-performance WTA circuit based on the differential FVF (DFVF) [28]. The circuit features high precision, high speed, very low supply voltage requirements and high input/output signal swing which is dependent on V_{DD}. The use of DFVF versus the single input FVF presents several advantages: with the same low output resistance and supply requirements as the FVF, it does not introduce a DC level shift between the input and the output terminals; it has wide input signal swing and it is not subject to the body effect attenuation, featuring close to unity gain; it has wide input/ output swing which is dependent on V_{DD}. As opposed to most other WTA circuits reported in literature this circuit can operate with a single supply close to a transistor's threshold voltage and with high speed and accuracy, finding application in the sub-volt supply environment required by modern deep sub-micrometer CMOS technologies.

Differential input FVFs can be also employed in the implementation of high performance, second generation current conveyors (CCII) and current feedback operational amplifiers (CFOAs) [30]. They are used in many current mode analog circuits as basic building blocks due to the suitability of current mode signal processing for the implementation of low voltage, low power, and high bandwidth analog circuits.

12.5 Conclusion

In this work a cell denoted "Flipped Voltage Follower" has been revisited. In this revision, several improved FVF cells (with single and differential input) and structures derived from the basic cell have been discussed, comparing their performances and characteristics. It has also been shown to be a useful cell with many applications in low-power, low-voltage analog design. The large number of linear and nonlinear structures that can use and be derived from this cell demonstrate its usefulness for low-power, low-voltage analog circuit design. However, FVF applications do not finish here. New fields and new possibilities exist. An area where the applicability of FVF has not been studied, is in line drivers and in digital

circuits. But there are many additional possibilities essentially any application where a very high performance buffer is required.

References

[1] Carvajal, R.G., Ramírez-Angulo, J., López-Martin, A., Torralba, A., Galán, J., Carlosena, A., Muñoz, F.: The Flipped voltage follower: A useful cell for low-voltage low-power circuit design. IEEE Transactions on Circuits and Systems I 52, 1276–1291 (2005)

[2] Gupta, S., Padilla, I., Ramirez-Angulo, J., Torralba, A., Jimenez, M.: Comparison of conventional and new flipped voltage follower structures. In: IEEE Midwest Symposium on Circuits and Systems, pp. 1151–1154 (2005)

[3] Gray, P.R., Hurst, P.J., Lewis, H., Meyer, R.G.: Design of analog integrated circuits, 4th edn. John Wiley and Sons, New York (2001)

[4] Ramirez-Angulo, J., Lopez, A.: MITE Circuits: The continuous time counterpart to switched capacitor circuits. IEEE Transactions on Circuits and Systems II 48, 45–55 (2001)

[5] Torralba, A., Carvajal, R.G., Jiménez, M., Muñoz, F., Ramírez-Angulo, J.: A new low-voltage CMOS unity-gain buffer. In: Proc. of the IEEE International Symposium on Circuits and Systems, pp. 919–922 (2006)

[6] Torralba, A., Carvajal, R.G., Jiménez, M., Muñoz, F., Ramírez-Angulo, J.: A new, true low voltage, Class-AB current mirror. IEICE Electronics Express ELEX 2, 103–107 (2005)

[7] Acosta, L., Jimenez, M., Lopez-Martin, A., Ramirez-Angulo, J.: Highly linear tunable CMOS Gm-C low-pass filter. IEEE Transactions on Circuits and Systems 56, 2145–2158 (2009)

[8] Acosta, L., Carvajal, R.G., Jimenez, M., Ramirez-Angulo, J., Lopez-Martin, A.: A CMOS transconductor with 90 dB SFDR and low sensitivity to mismatch. In: Proc. of the IEEE International Symposium on Circuits and Systems (2006)

[9] Sanchez-Rodriguez, T., Ramirez-Angulo, J., Lopez-Martin, A., Carvajal, R.G., Patil, C.: Gain enhancement and low voltage techniques for analogue circuits in deep submicrometer CMOS Technology. In: Krysztof, I. (ed.) CMOS Nanoelectronics: Analog and RF VLSI Circuits. McGraw Hill, New York (2009)

[10] You, F., Embabi, S.H.K., Sánchez-Sinencio, E.: Low-voltage class AB buffers with quiescent current control. IEEE Journal of Solid-State Circuits 33, 915–920 (1998)

[11] Peluso, V., Steyaert, M., Sansen, W.: Design of low-voltage low-power Sigma-delta A/D converters. Kluwer Academics Publishers, Boston (1999)

[12] Pardoen, M.D., Degrauwe, M.G.: A rail-to-rail CMOS input/output power amplifier. IEEE Journal of Solid-State Circuits 25, 501–504 (1990)

[13] Ramírez-Angulo, J., Carvajal, R.G., Torralba, A.: Low supply voltage high-performance CMOS current mirror with low input and output voltage requirements. In: Proc. of the IEEE Midwest Symposium on Circuits and Systems, pp. 510–513 (2000)

[14] Torralba, A., Carvajal, R.G., Ramirez-Angulo, J., Munoz, F.: Output stage for low supply voltage, high-performance CMOS current mirrors. IEE Electronics Letters 38, 1528–1529 (2002)

[15] Ducoudray, G.O., Carvajal, R.G., Ramírez-Angulo, J.: A High-speed dynamic current sensor scheme for iDD test using a flipped voltage follower. In: Proc. of the Southwest Symposium on Mixed-Signal Design, pp. 50–53 (2003)

[16] Man, T.Y., Leung, K.N., Leung, C.Y., Mok, P.K.T., Chan, M.: Development of single transistor control LDO based on flipped voltage follower for SoC. IEEE Transactions on Circuits and Systems I 55, 1392–1401 (2008)
[17] Chen, H., Leung, K.N.: A fast transient LDO based on buffered flipped voltage follower. In: Proc. of the IEEE Electron. Devices and Solid State Circuits (2010)
[18] Peluso, V., Coreland, P.V., Steyaert, M., Sansen, W.: A 900 mV differential class AB OTA for switched op-amp applications. IEE Electronics Letters 33, 1455–1456 (1997)
[19] Torralba, A., Carvajal, R.G., Martínez-Heredia, J., Ramírez-Angulo, J.: Class AB output stage for low voltage CMOS Op-Amps with accurate quiescent current control. IEE Electronics Letters 36, 1753–1754 (2000)
[20] Carvajal, R.G., Galán, J., Ramírez-Angulo, J., Torralba, A.: Low-power low-voltage differential class-AB OTAs for SC circuits. IEE Electronics Letters 38, 1304–1305 (2002)
[21] Ramírez-Angulo, J., Carvajal, R.G., Torralba, A., Nieva, C.: A new class AB differential input stage for implementation of low-voltage high slew rate op amps and linear transconductors. In: Proc. of the IEEE International Symposium on Circuits and Systems, pp. 671–674 (2001)
[22] Ramirez-Angulo, J., Thoutam, S., Lopez-Martin, A., Carvajal, R.G.: Low voltage CMOS analog four quadrant multiplier based on flipped voltage followers. IEE Electronic Letters Proc. 39, 1771–1772 (2003)
[23] Lopez-Martin, A., Ramirez-Angulo, J., Chintham, R., Carvajal, R.G.: Class AB CMOS analogue squarer circuit. IEE Electronics Letters 43, 1059–1060 (2007)
[24] Palmisano, G., Palumbo, G.: A simple CMOS CCII+. International Journal of Circuit Theory and Applications 6, 599–603 (1995)
[25] Ramirez-Angulo, J., Gupta, S., Carvajal, R.G., Lopez-Martin, A.: New improved class AB buffers based on differential flipped voltage followers. In: Proc. of the IEEE International Symposium on Circuits and Systems, pp. 3914–3917 (2006)
[26] Ramirez-Angulo, J., Lopez-Martin, A., Carvajal, R.G., Chavero, F.M.: Very low-voltage analog signal processing based on quasi-floating gate transistors. IEEE Journal of Solid State Circuits 39, 434–442 (2004)
[27] Ramírez-Angulo, J., Ducoudray-Acevedo, G., Carvajal, R.G., López-Martín, A.: Low voltage high performance voltage mode and current mode WTA circuits based on flipped voltage follower. IEEE Transactions on Circuits and Systems II 52, 420–423 (2005)
[28] Ramirez-Angulo, J., Molinar-Solis, J.E., Gupta, S., Carvajal, R.G., Lopez-Martin, A.: A high swing, high speed CMOS WTA using differential flipped voltage follower. IEEE Transactions on Circuits and Systems II 54, 668–672 (2007)
[29] Bikumandla, M., Ramírez-Angulo, J., Urquidi, C., Carvajal, R.G., Lopez-Martin, A.: Biasing CMOS amplifiers using MOS transistors in subthreshold region. IEICE Electronics Express 1, 339–345 (2004)
[30] Marri, S., Ramirez-Angulo, J., Lopez-Martin, A., Carvajal, R.G.: New high performance second generation CMOS current conveyor. In: Proc. of the XXIV Conference on Design Circuits and Integrated Systems, pp. 388–391 (2009)