A High-Swing, High-Impedance MOS Cascode Circuit

EDUARD SÄCKINGER, STUDENT MEMBER, IEEE, AND
WALTER GUGGENBÜHL, SENIOR MEMBER, IEEE

Abstract — **A simple cascode circuit with the gate voltage of the cascode transistor being controlled by a feedback amplifier, and thus named a "regulated cascode," is presented. In comparison to the standard cascode circuit, the minimum output voltage is lower by about 30 to 60 percent while the output conductance and the feedback capacitance are lower by about 100 times. An analytical large-signal, small-signal, and noise analysis is carried out. Some applications like current mirrors and voltage amplifiers are discussed. Finally, experimental results confirming the theory are presented.**

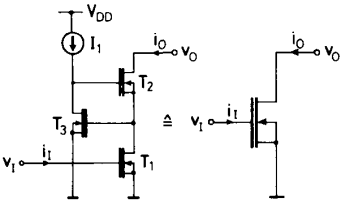

Fig. 1. The RGC circuit (left) behaves like a "super transistor" (right).

I. Introduction

CIRCUITS that behave like a MOS transistor but feature a much higher output impedance and a significantly lower feedback capacitance are an important prerequisite for the design of high-performance analog circuits. If such a circuit is used in a tail current source of a differential stage, the common-mode and power-supply rejection ratios are improved. If it is used in a voltage amplifier, a large dc gain factor and a single low-frequency pole is obtained.

Typically such a "super transistor" is constructed by stacking a second transistor with a fixed gate voltage on top of the main transistor yielding a so-called *cascode* circuit. Applications of this two-transistor circuit are, e.g., the cascode current mirror [1, p. 233] or the cascode op amp [1, p. 410]. These circuits show an increased output impedance in comparison to the simple current mirror or op amp, however, the usable output-voltage swing becomes narrower. By choosing optimum bias conditions, this restriction can be somewhat relaxed. This is done so in the so-called improvement cascode current source [1, p. 226]. In this paper a circuit, called a regulated cascode or RGC circuit, which further improves the respective characteristics, is presented (see Fig. 1). The output impedance is even higher than that of the simple cascode, and the output-voltage range usable for signal swing is enlarged compared to that of the optimally biased simple cascode (OBC) circuit.

For VLSI and high-frequency circuits, transistors with minimum feature size are often used. Such transistors exhibit pronounced channel-length modulation and carrier multiplication, even at relatively low voltages, as well as a moderate transconductance. The maximum dc-voltage gain, g_m/g_o, achievable with these transistors is therefore restricted to relatively small values. Scaling devices down, according to most scaling laws, further reduces this gain [2]. In such cases the RGC circuit with minimum-size transistors can be applied to obtain a small circuit area, good frequency response, and high dc gain simultaneously.

The operating principle of the RGC circuit shown in Fig. 1 is briefly described as follows. Transistor T_1 converts the input voltage v_I into a drain current i_O that flows through the drain–source path of T_2 to the output terminal. To obtain a high output resistance, i.e., to suppress channel-length modulation of T_1, the respective drain–source voltage must be kept stable. In the simple, that is nonregulated cascode circuit, this is done by loading the drain with the low source input resistance of the stacked transistor T_2. In the regulated cascode this is accomplished by a feedback loop consisting of an amplifier (T_3 and I_1) and T_2 as a follower. In this way the drain–source voltage of T_1 is *regulated* to a fixed value. Please note that the feedback mechanism upon which the stabilization is based works even if T_2 is driven into the ohmic operating region, which extends the usable range for the output signal.

In Section II the output swing, the small-signal parameters, the noise characteristics, and the transient behavior of the proposed circuit are analyzed. Some applications like current sources, current mirror, and voltage amplifiers are

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E. Säckinger was with the Electronics Laboratory, Swiss Federal Institute of Technology Zurich, Zürich, Switzerland. He is now with AT&T Bell Laboratories, Holmdel, NJ 07733.
W. Guggenbühl is with the Electronics Laboratory, Swiss Federal Institute of Technology Zurich, ETH Zentrum, CH-8092 Zürich, Switzerland.
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given in Section III. In the last section, experimental results are presented and put into relation with the theory.

II. Analysis

A. Output Swing

In the following, the selection of the operating point for the RGC circuit is discussed. Furthermore, we will derive analytical expressions for the output swing showing the superiority of the RGC circuit over the OBC circuit like, e.g., the improved cascode current source.

The subsequent calculations of the large-signal performance are based on the simple quadratic strong-inversion model of the MOS transistor [1, p. 100] ignoring channel-length modulation. There are several reasons for choosing this simple model. 1) Although no precise numerical results can be expected from it, the obtained formulas remain simple and show the basic dependence of the typical characteristics on the design parameters. 2) The design rules usually given for the improved cascode current source are based on the above model, i.e., the edge of saturation is assumed to be at $v_{GS} - V_{TH}$. Therefore a reasonable comparison with the regulated cascode is only possible if the same model is applied here.

In the following discussion of the optimal biasing, the input voltage is assumed to be constant, $v_I = V_I = V_{GS1}$ (see Fig. 1). If we require T_1 to operate in saturation, its drain voltage v_{DS1} must exceed $V_{GS1} - V_{TH}$. To maximize the voltage swing, the lowest possible quiescent value for v_{DS1} satisfying this condition should be realized. Since the quiescent voltage V_{DS1} is mainly determined by the feedback amplifier (T_3, I_1), this condition leads to a design equation for β_3 and I_1, assuming that T_3 operates in strong inversion:

$$V_{DS1} = V_{GS1} - V_{TH} = \sqrt{\frac{2I_1}{\beta_3}} + V_{TH}. \tag{1}$$

In the case where v_I is not constant, its maximum value $\max(v_{GS1})$ must be inserted for V_{GS1}. This asserts saturated operation of T_1 for all input voltages. A more elaborate method to handle variable input voltages is to adaptively bias the feedback amplifier according to (1). An analogous method for the simple cascode circuit is described in [3].

Equation (1) shows that it is only possible to find solutions for β_3 and I_1 if the input voltage V_{GS1} is larger than $2V_{TH}$. This is not a serious limitation, however, because a relatively large gate–source voltage is often justified for other reasons as well: e.g., to obtain a temperature-independent operating point [4] or to reduce the $1/f$ noise contribution of current-source or current-mirror transistors. Note that (1) does not state that it is impossible to use the RGC circuit with gate voltages below $2V_{TH}$, but only that in this case no optimum output swing is achieved.

If the amplifier transistor T_3 is operated in weak inversion (T_1 and T_2 remain in strong inversion), the above-mentioned restriction no longer applies, because the gate voltage of T_3 may now assume lower values than that given on the right-hand side of (1). Using the simple drain-current equation for weak inversion, $i_D = W/L \cdot I_{D0} \cdot \exp\{v_{GS}/(nV_T)\}$ [1, p. 126], the design equation for optimum biasing becomes

$$V_{DS1} = V_{GS1} - V_{TH} = nV_T \ln\left(\frac{L_3 I_1}{W_3 I_{D0}}\right). \tag{2}$$

This condition can be fulfilled for any input voltage larger than V_{TH}.

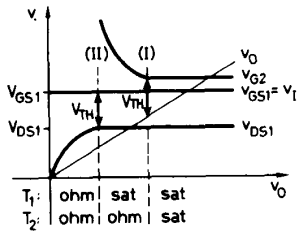

Fig. 2. Transistor gate and drain voltages of the RGC circuit as a function of the output voltage v_O.

Fig. 2 illustrates the performance of the RGC circuit for low output voltages v_O. The figure is drawn for a fixed input voltage $v_I = V_{GS1}$. If the circuit is biased according (1) or (2), v_{DS1} is one threshold below V_{GS1} for high output voltages. In order to conduct the output current, v_{G2} must be somewhat more than one threshold voltage above v_{DS1}. (Note that the figure is drawn from the case when T_1 and T_2 have different dimensions.) If v_O is decreased starting from high values in Fig. 2, we see that at point (I) v_O has dropped by one threshold below v_{G2}, meaning that T_2 enters into the ohmic operation region. Under this condition more gate voltage for T_2 is needed to conduct the current asserted by T_1; the respective increase of v_{G2} is realized by the feedback amplifier (T_3, I_1). For even lower output voltages, point (II) will be reached when further increasing of v_{G2} cannot force T_2 to conduct the saturation current from T_1, i.e., this latter transistor is driven into the ohmic operating region as well. Note that during all phases T_3 stays in saturation because $v_{DS3} > v_{GS3}$ is asserted by v_{GS2} being positive.

In the following a mathematical description for the lowest value of v_O where the circuit still "performs properly" is developed. With proper performance it is often meant that all transistors of the respective circuit are operating in the saturated mode [1]. The output voltage where the first transistor, in our case T_2, leaves the saturated operating mode is marked with (I) in Fig. 2. This voltage shall subsequently be called $V_{O\min}(\mathrm{RGC}, s)$ and can be calculated easily: if (1) or (2) holds, the voltage at the drain of T_1 is $V_{GS1} - V_{TH}$, while the minimum voltage across T_2 is $V_{GS2} - V_{TH}$. Thus we obtain

$$V_{O\min}(\mathrm{RGC}, s) = V_{GS1} - V_{TH} + V_{GS2} - V_{TH} \tag{3}$$

for the minimum output voltage of the RGC circuit leav-

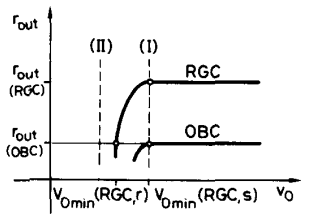

Fig. 3. Output resistance as a function of the output voltage for the RGC and the OBC circuits, respectively.

ing both stacked transistors in saturation. Note that this voltage is equal to the minimum output voltage usually given for the improved cascode current source [1, p. 225].

From (3) it might seem that we have gained nothing compared to the optimally biased simple cascode with respect to voltage swing. However, the comparison based on this "saturation criterion" is not a fair one. It is more appropriate to define the minimum output voltage of the RGC circuit as the voltage where the small-signal output resistance of the regulated cascode is equal to that of the improved cascode in saturation. This new limit shall be denoted $V_{O\min}(\mathrm{RGC}, r)$, and its definition is illustrated in Fig. 3.

AC parameters like the output resistance are discussed in the next section. However, in order to calculate $V_{O\min}(\mathrm{RGC}, r)$ we have to use some of the results in advance. The small-signal output resistance for low frequencies of the RGC and OBC circuits can be approximated by

$$r_{\mathrm{out}}(\mathrm{RGC}) = \frac{1}{g_{o1}} \cdot \frac{g_{m2} g_{m3}}{g_{o2}(g_{o3} + g_{oi})} \tag{4}$$

and

$$r_{\mathrm{out}}(\mathrm{OBC}) = \frac{1}{g_{o1}} \cdot \frac{g_{m2}}{g_{o2}} \tag{5}$$

respectively, where $g_{o\nu}$ is the output conductance and $g_{m\nu}$ is the transconductance of the respective transistor T_ν (for $\nu = 1, 2, 3$) and g_{oi} is the conductance of the current source I_1. We see from (4) and (5) that $r_{\mathrm{out}}(\mathrm{RGC})$ exceeds $r_{\mathrm{out}}(\mathrm{OBC})$ by a factor $g_{m3}/(g_{o3} + g_{oi})$, which approximately corresponds to the loop gain of the RGC circuit and is typically in the neighborhood of 100.

As shown earlier, if v_O of the RGC circuit is lowered, the first transistor leaving the saturated operating mode is T_2. This means that the output resistance of the regulated cascode will decrease initially because the factor g_{m2}/g_{o2} of (4) becomes smaller when T_2 enters into the ohmic operation mode. From the MOS equation and (4) and (5), the minimum output voltage $V_{O\min}(\mathrm{RGC}, r)$ can be derived:

$$V_{O\min}(\mathrm{RGC}, r) = V_{GS1} - V_{TH} + \sqrt{\frac{2\Psi}{2+\Psi} \cdot \frac{I_O}{\beta_2}} \tag{6}$$

where

$$\Psi = \frac{g_{m2}(\mathrm{sat}) \cdot (g_{o3} + g_{oi})}{g_{o2}(\mathrm{sat}) \cdot g_{m3}} \tag{7}$$

and the corresponding values for g_{o1}, g_{m2}, and g_{o2} of the RGC and OBC circuits in saturation are taken to be equal.

To compare the minimum output voltages of the regulated and the optimally biased simple cascode, a merit factor η_s is defined:

$$\eta_s = \frac{V_{O\min}(\mathrm{OBC})}{V_{O\min}(\mathrm{RGC}, r)}. \tag{8}$$

To obtain a meaningful result, the RGC and OBC circuits on which the comparison is based should have comparable dimensions. It seems reasonable to assume equal output currents I_O for both circuits and that the lower and upper transistors (T_1 and T_2) of the respective circuits have corresponding betas (β_1 and β_2). The merit factor of (8) then becomes

$$\eta_s = \frac{1 + \sqrt{\frac{\beta_1}{\beta_2}}}{1 + \sqrt{\frac{\beta_1}{\beta_2}} \sqrt{\frac{1}{1 + 2/\Psi}}}. \tag{9}$$

The merit factor η_s is independent of the output current or the input voltage and improves for an increasing β_1/β_2 ratio or a decreasing Ψ. The latter means that a high loop gain in the regulated cascode is profitable.

In order to illustrate the theoretical calculations as a basis for later approximations of symbolic expressions, we will introduce a practical circuit example which has been simulated with ESPICE.[1] The transistors feature the dimensions $T_1 = T_2 = T_3 = 25\ \mu\mathrm{m}/3\ \mu\mathrm{m}$ and are simulated for the 3-μm SACMOS technology [5]. The current source I_1 is realized with a 3-μm/3-μm p-channel current mirror and a 4-MΩ resistor from the mirror input to ground supplying about 1.3 μA at $V_{DD} = 5$ V. The input voltage is chosen to be 1.1 V yielding an output current of $I_O \approx 60\ \mu\mathrm{A}$. The simulated V_{DS1} is 0.60 V which is exactly one threshold voltage (0.5 V) below V_I, confirming the correct dimensions of the feedback amplifier according to (1). For an output voltage of 5 V all transistors are in saturation and a v_{G2} of 1.63 V and an output resistance of 905 MΩ are obtained. For an output voltage of 0.83 V, T_2 is in the ohmic operating region and v_{G2} increases to 1.76 V while the output resistance decreases to 13.0 MΩ. This is about the output resistance of the corresponding simple cascode and thus $V_{O\min}(\mathrm{RGC}, r) = 0.83$ V. The merit factor for the output swing follows as $\eta_s = (1.63\ \mathrm{V} - 0.50\ \mathrm{V})/0.83\ \mathrm{V} = 1.36$.

Inserting the numbers $\beta_1/\beta_2 = 1$ and $\Psi = 0.88$ (calculated with the small-signal parameters of the next section) into (9) yields a theoretical merit factor $\eta_s = 1.29$.

[1] ESPICE (Extended Simulation Program with Integrated Circuit Emphasis) is an extension of SPICE developed by Philips.

TABLE I
TYPICAL SMALL-SIGNAL PARAMETERS OF THE TRANSISTORS CONSTITUTING AN RGC CIRCUIT

Parameter	T_1	T_2 (sat)	T_2 (ohm)	T_3	Unit
g_m	205	222	133	33	μS
g_o	5.1	3.5	148	0.3	μS
C_g	44	44	41	44	fF
C_{gd}	8.4	8.4	22	8.4	fF
C_o	58	30	68	44	fF
C_b	-	78	78	-	fF

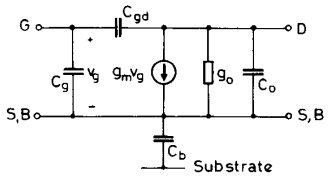

Fig. 4. Small-signal model of an MOS transistor.

B. Small-Signal Parameters

All small-signal calculations presented in this section are based on the ac MOS-transistor model shown in Fig. 4. The source and bulk terminals of all transistors are supposed to be interconnected as shown in Fig. 1. As a consequence of the floating p-well of T_2, the transistor has a capacitance C_{b2} from the source/bulk node to the substrate (v_{dd}). The current source I_1 is modeled by a parallel connection of a conductance g_{oi}, a capacitance C_{oi}, and a transconductance g_{mi} controlled by v_{dd}. The latter models the power-supply dependence of the auxiliary current source.

The regulated cascode circuit of Fig. 1 is a three-port network whose small-signal characteristics can be described by nine y parameters in the s domain:

$$\begin{aligned} I_i &= y_{11}V_i + y_{12}V_o + y_{13}V_{dd} \\ I_o &= y_{21}V_i + y_{22}V_o + y_{23}V_{dd} \\ I_{dd} &= y_{31}V_i + y_{32}V_o + y_{33}V_{dd}. \end{aligned} \tag{10}$$

The interesting parameters, namely y_{11} (input admittance), y_{12} (reverse admittance), y_{21} (transmittance), y_{22} (output admittance), and y_{23} (influence of V_{dd} to I_o) have been calculated symbolically with the help of the SYNAP and MACSYMA programs.[2] The expressions thus obtained are very large and unwieldy. It is therefore reasonable to evaluate these symbolic expressions in a first step for typical numerical values in order to become familiar with the parameter's order of magnitude and the approximate pole/zero locations.

In Table I typical values for the transistor's small-signal parameters are given. The values for the current-source small-signal model are $g_{oi} = 0.16$ μS, $C_{oi} = 2.7$ fF, and $g_{mi} = 0.29$ μS. All values correspond to the example circuit introduced in the previous section. The parameters of T_2 are given for the saturated and the nonsaturated operating modes discussed in the example.

[2]SYNAP (SYmbolic aNAlysis Program) is a circuit analysis program developed at the Integrated Systems Laboratory, ETHZ, and CSEM, Switzerland. MACSYMA (MAC's SYmbolic MAnipulation system) is a computer algebra program developed at the M.I.T. Laboratory for Computer Science.

TABLE II
NUMERICAL VALUES FOR THE ZEROS AND POLES OF THE y PARAMETERS BASED ON THE VALUES OF TABLE I. FREQUENCIES ARE GIVEN IN CYCLES PER SECOND

Parameter	Saturated Case	T_2 not Saturated
	zeros	
y_{11}	0	0
	$(-56.4 + 63.6i)$ MHz	-26.5 MHz
	$(-56.4 - 63.6i)$ MHz	-130 MHz
y_{12}	0	0
	-114 kHz	-533 kHz
	-98.2 MHz	-357 MHz
y_{21}	-125 MHz	-29.8 MHz
	-414 MHz	-423 MHz
	$+3.88$ GHz	$+3.88$ GHz
y_{22}	-16.1 kHz	-98.1 kHz
	-27.7 MHz	-20.2 MHz
	-85.9 MHz	-324 MHz
y_{23}	$+145$ kHz	$+140$ kHz
	-157 MHz	-29.8 MHz
	-305 MHz	-401 MHz
	poles	
y_{ij}	$(-45.4 + 71.4i)$ MHz	-32.7 MHz
	$(-45.4 - 71.4i)$ MHz	-105 MHz

TABLE III
NUMERICAL VALUES FOR THE CAPACITANCES AND (TRANS-)CONDUCTANCES OF THE y PARAMETERS BASED ON THE VALUES OF TABLE I

Parameter	Saturated Case	T_2 not Saturated
C_i	52.5 fF	52.6 fF
C_r	0.00182 fF	0.127 fF
g_m	205 μS	205 μS
g_o	1.1 nS	76.8 nS
g_{mdd}	68.6 nS	67.5 nS

The numerical values for the poles and zeros of the y parameters for two cases—1) all transistors saturated and 2) all transistors except T_2 saturated—are summarized in Table II. Parameters y_{21} and y_{22} have nonzero dc values that we will denote as g_m and g_o, respectively.[3] Because parameters y_{11} and y_{12} are zero at dc, we eliminate the respective zero and specify the corresponding capacitances C_i and C_r at dc. Numerical values for these (trans-)conductances and capacitances are given in Table III.

In order to obtain a simple design equation, we will now ignore all poles and zeros above 20 MHz in Table II. With this assumption the y parameters can be written in the form

$$\begin{aligned} y_{11} &= sC_i \quad y_{12} = -sC_r(1 + sT_r) \\ y_{21} &= g_m \quad y_{22} = g_o(1 + sT_o) \\ y_{23} &= g_{mdd}(1 - sT_d). \end{aligned} \tag{11}$$

[3]Some symbols like g_o have several meanings in this text. For example, g_o can stand for the output conductance of a single transistor, of the RGC circuit, or of an application circuit. From the context, however, the intended meaning should always be obvious.

The following symbolic approximations for the capacitances and (trans-)conductances have been obtained:

$$C_i = C_{g1} + C_{gd1}$$

$$C_r = C_{gd1} \cdot \frac{g_{o2}(g_{o3} + g_{oi})}{g_{m2} g_{m3}}$$

$$g_m = g_{m1}$$

$$g_o = g_{o1} \cdot \frac{g_{o2}(g_{o3} + g_{oi})}{g_{m2} g_{m3}}$$

$$g_{mdd} = (g_{oi} + g_{mi}) \cdot \frac{g_{o1}}{g_{m3}} \tag{12}$$

and

$$T_r = \frac{C_{gd2} g_{m2} + (C_{o3} + C_{m2}) g_{o2}}{g_{o2}(g_{o3} + g_{oi})}$$

$$T_o = \frac{C_{gd2}(g_{m2} + g_{o2})(g_{m3} + g_{o1}) + C_{m2} g_{m3} g_{o2}}{g_{o1} g_{o2}(g_{o3} + g_{oi})}$$

$$T_d = \frac{C_{b2} g_{m3}}{g_{o1}(g_{m1} + g_{oi})}. \tag{13}$$

In the above equations C_{m2} is the sum of C_{g2} and C_{gd3}. While C_i and g_m of the regulated cascode circuit are about the same as those of a single transistor (T_1), the parameters C_r and g_o are improved by a factor $g_{m2}/g_{o2} \cdot g_{m3}/(g_{o3} + g_{oi})$, that is the intrinsic gain of T_2 times the amplifier gain. The power-supply dependence is that of the auxiliary current source $(g_{oi} + g_{mi})$ reduced by a gain factor g_{m3}/g_{o1}. The time constants T_r and T_o depend mostly on C_{gd2}. T_o will be larger than T_r since it contains two gain factors while T_r contains only one. The right half-plane zero described by T_d is mainly due to C_{b2}. If the p-well of T_2 were grounded, T_d would be much smaller.

It is interesting to compare the y parameters of the regulated cascode to those of the simple cascode. A calculation for the saturated simple cascode (OBC) shows that the y parameters have the same form as those given in (11) for the regulated cascode. The main difference is that the output resistance $r_{out} = 1/g_o$ of the RGC circuit is a factor $g_{m3}/(g_{o3} + g_{oi})$ larger than that of the simple cascode. We can thus define a second merit factor η_r for the output resistance in the saturated region:

$$\eta_r = \frac{r_{out}(\text{RGC})}{r_{out}(\text{OBC})} = \frac{g_{m3}}{(g_{o3} + g_{oi})}. \tag{14}$$

The value for η_r using the typical small-signal parameters of Table I is 72. Furthermore, the regulated cascode features a 72 times lower feedback capacitance C_r. The input capacitance C_i of the regulated cascode is smaller than that of the simple one by about $C_{gd1} \cdot g_{m1}/g_{m2}$ (= 7.8 fF for the typical values). The dc power-supply dependence of the simple cascode is determined by the stability of the bias voltage V_{G2} instead of the bias current I_1. Both time constants T_r and T_o are increased with respect to the simple cascode circuit.

C. Noise

A noise analysis of the RGC circuit for low frequencies has been carried out. For this purpose noise sources $\overline{v_{nv}^2}$ are inserted into the gate leads of all transistors T_v and a noise current source $\overline{i_{n1}^2}$ is connected in parallel to I_1. The small-signal circuit of Fig. 4, without the capacitors, was used to model the low-frequency behavior of the transistor.

With these assumptions the equivalent noise source $\overline{v_{eq}^2}$ at the input of the circuit has been approximated:

$$\overline{v_{eq}^2} = \overline{v_{n1}^2} + c_2 \overline{v_{n2}^2} + c_3 \overline{v_{n3}^2} + c_3/g_{m3}^2 \cdot \overline{i_{n1}^2} \tag{15}$$

where

$$c_2 = \left(\frac{g_{o1}(g_{o3} + g_{oi})}{g_{m1} g_{m3}} \right)^2$$

$$c_3 = \left(\frac{g_{o1}}{g_{m1}} \right)^2.$$

Typical exact numbers for c_2 based on the values of Table I are 117×10^{-9} in the saturated and 113×10^{-9} in the nonsaturated case; the values of c_3 are 602×10^{-6} and 584×10^{-6}, respectively. The reason why the operating mode of T_2 has nearly no influence on the noise factors can be understood by the following analogy. The equation for the equivalent input noise voltage, (15), is similar to that describing a three-stage amplifier whose first stage consists of T_1, second of T_3 and I_1, and third of T_2. But the gain of an amplifier's last stage, which in our case varies strongly with v_O, is of practically no importance for the input-referred noise performance.

Transistor T_1 is the dominant noise source ($\overline{v_{n1}^2}$) in the regulated as well as the simple cascode circuit; the noise performances of both cascodes are therefore virtually the same. On the other hand, the noise generated by T_2 is more fully suppressed in the RGC circuit than in the simple cascode, where $c_2 = 600 \times 10^{-6}$ in the example. On the other hand, the RGC circuit contains an additional noise source introduced by the feedback amplifier, however, it contributes only a negligible amount of noise to $\overline{v_{eq}^2}$.

D. Large-Signal and Transient Behavior

The large-signal and transient behavior of the RGC circuit shall be analyzed in a qualitative way. Typical numbers obtained with ESPICE simulations for the example RGC circuit and a correspondingly dimensioned optimally biased simple cascode are given.

The dc large-signal output characteristics of the RGC circuit has already been covered in Section II. To summarize, the output conductance as well as the minimum allowable output voltage are lower than that of the optimally biased simple cascode. The dc large-signal transfer characteristic of the RGC circuit is quadratic as long as v_I

is small enough and T_1 operates in saturation. For larger v_I, the relation between v_I and i_O becomes linear, because T_1 enters into the ohmic operating region and v_{DS1} is still kept constant. In contrast, the output current of the simple cascode is limited for large v_I because v_{DS1} breaks down with increasing current. In our example, the RGC circuit delivers 320 μA for $v_I = 2$ V, while the simple cascode supplies only 170 μA for the same input voltage. This means that the large-signal transfer characteristic of the RGC circuit is superior to that of the simple cascode.

If a positive voltage step is applied to the input of the RGC circuit, v_{DS1} decreases initially and then is regulated back to its original value. Because of the noninverting feedforward path (mainly through C_{g2}) of the feedback amplifier (T_3, I_1), this initial breakdown will be larger than in the nonregulated case. As a consequence T_1 may temporarily be driven into the ohmic operating mode thus delivering less current than expected. If an input voltage step from 0.7 to 1.1 V is applied to the example circuits, the full current is reached after 18 ns for the RGC and after 8 ns for the simple cascode circuit. This effect may cause a slew-rate reduction of the respective op amp or OTA to which the regulated cascode is applied. To avoid this effect, a feedback amplifier with low feedforward should be used. A negative input-voltage step has no corresponding effect on the output current.

If the input or output voltage of the RGC circuit is forced to zero, the output of the feedback amplifier will saturate near ground or V_{DD}, respectively. Switching on the input or output voltage thus necessitates the amplifier output to slew several volts to reach its operating value. In the example circuit a delay of about 100 ns from input- or output-voltage switching to the respective output-current change is observed. The corresponding delays of the simple cascode are a few nanoseconds. In switching applications like comparators the output swing of the feedback amplifier should therefore be limited, e.g., by clamping.

III. Basic Applications

Some basic applications of the RGC circuit are analyzed and compared to conventional implementations. The circuits being discussed are a current mirror, a constant current source, and a voltage amplifier.

A. Regulated Cascode Current Mirror

A current mirror based on two RGC circuits is shown in Fig. 5. The input current is denoted as i_I and the output current is designated i_O. Because of the circuit's symmetric topology, there is virtually no systematic error in the ratio of the input and output currents at dc in contrast to, e.g., the simple Wilson current mirror [1, p. 235]. The output swing of the regulated cascode current mirror is comparable to that of the simple current mirror [1, p. 227] and much better than that of the simple cascode current mirror [1, p. 233], because the latter is neither regulated nor optimally biased. Compared to other stacked current mirrors (cascode or Wilson), the regulated cascode current mirror has the advantage of a lower input-voltage drop v_I: For the RGC current mirror v_I is equal to the gate–source voltage of T_1, while in the other cases the sum of two gate–source voltages is lost. The simple cascode and simple current mirror need no bias sources and thus have the advantage of power-supply independence at dc.

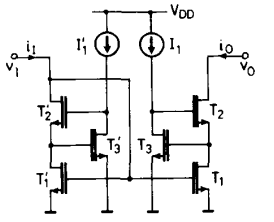

Fig. 5. Current mirror based on two RGC circuits.

If we assume that the regulated cascodes in the left (primed) and right (unprimed) part of the current-mirror circuit (Fig. 5) are characterized by equal small-signal parameters and the input is driven by an ideal current source, we can approximate the output admittance $y_o = I_o/V_o$ for $V_{dd} = 0$ as

$$y_o = g_o(1 + sT_o) = \frac{1}{r_{\text{out}}} + sC_{\text{out}} \tag{16}$$

where

$$r_{\text{out}} = \frac{1}{g_{o1}} \cdot \frac{g_{m2}g_{m3}}{g_{o2}(g_{o3} + g_{oi})}$$

$$C_{\text{out}} = C_{gd2}\left[1 + \frac{(2g_{o3} + g_{o1})}{g_{m3}} + \frac{g_{o2}}{g_{m2}}\right] + C_{m2}\frac{g_{o2}}{g_{m2}}.$$

The result obtained is approximately equal to y_{22} of the RGC circuit alone. Since there is a single low-frequency zero, the output admittance y_o can be modeled by a parallel connection of r_{out} and C_{out}. The main contribution to the output capacitance is C_{gd2}. When T_2 is driven into the ohmic region, g_{o2}/g_{m2} will increase and C_{m2} will add some extra capacitance to C_{out}. This increase of the output capacitance can also be explained by the fact that for low output voltages the gate voltage of T_2 is strongly dependent on v_O (see Fig. 2), thus giving rise to a charge transfer between the output terminal and T_2.

It is interesting to compare the output admittance of the regulated cascode current mirror to that of other current mirrors. Approximative calculations done for the simple current mirror shown that

$$r_{\text{out}} = \frac{1}{g_{o1}}$$

$$C_{\text{out}} = C_{o1} + 2C_{gd1}. \tag{17}$$

Calculations done for the simple cascode current mirror

yield

$$r_{\text{out}} = \frac{1}{g_{o1}} \cdot \frac{g_{m2}}{g_{o2}}$$

$$C_{\text{out}} = 2C_{gd2} + (2C_{g2} + C_{o1} + C_{b2})\frac{g_{o2}}{g_{m2}} + C_{o2}\frac{g_{o1}}{g_{m2}}. \quad (18)$$

Beside the expected differences in the output resistances, there are also significant differences in the output capacitances. Using our sample values, we get 47.1 fF for the simple current source, 20.4 fF for the cascode current source, and 10.9 fF for the regulated cascode current source. The capacitance of the simple current mirror is mainly determined by C_{o1}, that of the simple cascode mirror is about $2C_{gd2}$, and that of the regulated cascode mirror is approximately C_{gd2}. How can the factor 2 in the output capacitance of the simple cascode be explained? This is a consequence of the capacitive current through C_{gd2} which flows into the biasing network. Because this network is at the same time the current-mirror input path, this current is mirrored to the output where it appears a second time. In the regulated cascode current mirror this capacitive current flows into a path isolated from the current-mirror input, thus explaining the lower output capacitance of the regulated cascode current mirror.

The small-signal current-transfer function $A_i(s) = I_o/I_i$ for $V_o = V_{dd} = 0$ has been investigated numerically. The dc value of $A_i(s)$ is very close to one, as expected. Unfortunately, $A_i(s)$ has more than one dominant pole and an approximative formula of the frequency behavior has not been found. Numerical calculations based on our example circuit yield three poles, one at -90.9 MHz and the others at $(-26.1 \pm 136i)$ MHz, as well as three zeros located at -125 MHz, -414 MHz, and $+3.88$ GHz. This corresponds to a 3-dB low-pass bandwidth of 200 MHz which compares to the bandwidths of the simple current mirror and the cascode current mirror with 270 and 200 MHz, respectively.

From the complex-conjugated poles at $(-26.1 \pm 136i)$ MHz, which are caused by the feedback mechanism of the RGC circuits, one can expect a peaking of the current-transfer function. A peaking of 7 dB at 140 MHz can actually be observed in the example, but it is not a serious problem for most applications.

B. Regulated Cascode Constant Current Source

The circuit of Fig. 5 can also be used as a constant current source, if i_I is kept constant. When the circuit is used as a current source, i.e., an exact matching of i_I and i_O is not imperative, the left part of the circuit (T_1', T_2', T_3', and I_1') can be replaced by a single gate–drain connected transistor (T_1'), thus simplifying the original circuit. For the case where the circuit is driven by a bias voltage $V_I = V_{\text{BIAS}}$, the left part of the circuit can be omitted completely. These simplifications have little influence on the output characteristic and the above results for y_o also apply to the regulated cascode current source.

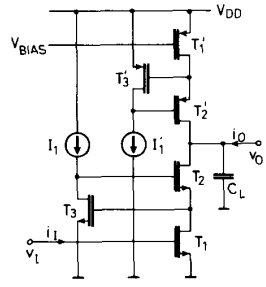

Fig. 6. Single-ended amplifier using one RGC circuit as a transconductance element and a second one as current source.

The output characteristics of the simple current source [1, p. 219] and the standard cascode current source [1, p. 224] are equal to the corresponding mirrors discussed above. The improved cascode current source [1, p. 226] is optimally biased and therefore features a better output swing than the simple cascode current source, but as has been shown in Section II, it is still inferior to that of the regulated cascode current source. The output impedance of the improved cascode can be approximated by

$$r_{\text{out}} = \frac{1}{g_{o1}} \cdot \frac{g_{m2}}{g_{o2}}$$

$$C_{\text{out}} = C_{gd2} + (C_{g2} + C_{o1} + C_{b2})\frac{g_{o2}}{g_{m2}} + C_{o2}\frac{g_{o1}}{g_{m2}}. \quad (19)$$

The output resistance is equal to that of the simple cascode, but the output capacitance (12.0 fF in the example) corresponds to that of the regulated cascode because the bias network of the improved cascode is decoupled from the input path. Note, that the improved cascode current source, like the regulated cascode current source, has a dc power-supply dependence.

C. Regulated Cascode Voltage Amplifier

The single-ended amplifier depicted in Fig. 6 is based on two complementary RGC circuit blocks. The unprimed one acts as a transconductance element while the primed one is used as a constant current source as discussed earlier. This amplifier features a single low-frequency pole and a large output swing. A similar circuit is investigated in [6]. The use of such an amplifier with capacitive loading is typical in switched-capacitor circuits where the static gain A_{v0} determines the precision of these circuits.

An approximation based on the typical values of the example RGC circuit and $C_L = 1$ pF yields

$$A_v(s) = A_{v0} \cdot \frac{1}{1 + sT_a} \quad (20)$$

where

$$A_{v0} = -\frac{g_{m1}g_{m2}g_{m3}}{2g_{o1}g_{o2}(g_{o3} + g_{oi})}$$

$$T_a = C_L \cdot \frac{g_{m2}g_{m3}}{2g_{o1}g_{o2}(g_{o2} + g_{oi})}.$$

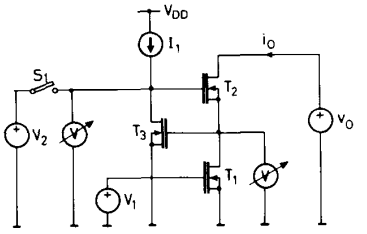

Fig. 7. Test circuit for measuring the output characteristics of a regulated (S_1 open) and an optimally biased simple cascode (S_1 closed) circuit.

The gain–bandwidth product $|A_{v0}|/T_a$ is thus g_{m1}/C_L. For the example circuit we obtain an A_{v0} of 99 dB and a gain–bandwidth product of $2\pi \cdot 31.9$ MHz.

A conventional three-stage amplifier exhibits a similar dc gain, but it would necessitate a compensation scheme, because it has three poles at nearby frequencies. The regulated cascode amplifier, featuring only one load-capacitor dependent pole, has the advantage of being self-compensating.

The input conductance of the regulated cascode amplifier can be approximated by

$$y_i = sC_{\text{in}} \frac{1+sT_i}{1+sT_a} \tag{21}$$

where

$$C_{\text{in}} = C_{gd1}\left(\frac{g_{m1}}{2g_{o1}}+1\right)+C_{g1}$$

$$C'_{\text{in}} = C_{\text{in}} \cdot \frac{T_i}{T_a} = C_{g1}\left(1+2\frac{g_{o3}+g_{oi}}{g_{m3}}\right)+C_{gd1}.$$

C'_{in} is the input capacitance for frequencies much higher than the pole (-344 Hz) and zero (-1.44 kHz) of the input admittance. For very low frequencies the input capacitance is relatively high due to the Miller multiplication of C_{gd1} ($C_{\text{in}} = 221$ fF); for frequencies above some kilohertz this capacitance reduces to about C_{g1} ($C'_{\text{in}} = 52.8$ fF).

It is also possible to use the RGC circuit to improve a differential amplifier. In this case the differential-pair transistors are each replaced by a RGC circuit and the current mirror is built as described in Section III-A. The advantages are the same as for the single-ended amplifier: high gain, self-compensation, and large output swing.

IV. Experimental Results

A test circuit which can be operated as a regulated or an optimally biased simple cascode has been bread-boarded (see Fig. 7). All transistors used in the circuit are fabricated in a 4-μm technology and have the dimensions $W = 7\,\mu$m and $L = 4\,\mu$m. If switch S_1 is open, the gate of T_2 is controlled by the feedback amplifier (T_3, I_1), that is, the circuit operates as a regulated cascode; if S_1 is closed, the gate voltage of T_2 is supplied by the voltage source V_2 which is chosen such that the circuit is an optimally biased simple cascode. The input voltage $V_1 = V_I = V_{GS1} = 1.4$ V and the auxiliary current source $I_1 = 1.4\,\mu$A are constant. I_1 has been chosen according to (1) such that the drain voltage of T_1 is one threshold voltage below its gate voltage; this is $V_{DS1} = 0.75$ V for a measured threshold voltage $V_{TH} = 0.65$ V. During the measurement the output voltage v_O is swept while the output current i_O and the node voltages v_{DS1} and v_{G2} are monitored with a HP 4145A semiconductor parameter analyzer.

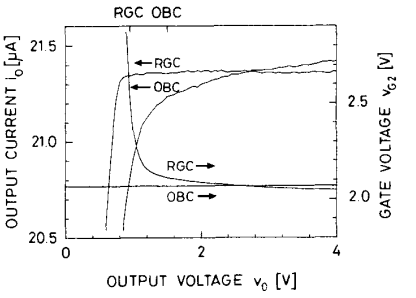

Fig. 8. Measured output characteristics of the RGC and OBC circuits for low output voltages. In order to illustrate the regulating process, v_{G2} is also plotted (scale on the right-hand side).

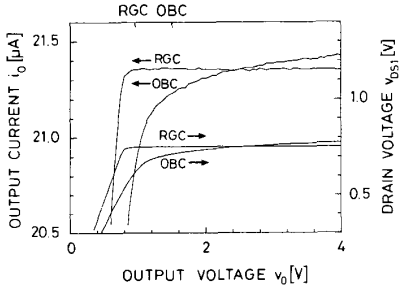

Fig. 9. Measured output characteristics of the RGC and OBC circuits for low output voltages. On the right-hand scale the dependence of v_{DS1} is given.

The plot of Fig. 8 shows the output current and the gate voltage of T_2 of the RGC and the OBC circuits for an output voltage range of 0 to 4 V. The higher output resistance and larger voltage swing of the RGC circuit can be seen clearly from this measurement. The underlying regulating process is also illustrated nicely by this figure: for output voltages above 1.5 V, v_{G2} varies only very little and is about equal to that of the simple cascode. The small variations compensate for the channel-length modulation of T_2 and thus make the output resistance high. Below 1.5 V, v_{G2} increases rapidly driving T_2 into the ohmic operation region. As a consequence i_O is kept stable for output voltages well below 1 V. Fig. 9 additionally shows the drain–source voltage of T_1. This plot confirms that I_1 for the regulated cascode and V_2 for the simple cascode are chosen such that T_1 is biased at the edge of saturation (0.75 V) in both cases, and thus the comparison is fair. It is shown by the curves how the feedback loop in the RGC circuit stabilizes v_{DS1} for as low voltages as possible. An analogous measurement to that depicted in Fig. 8 has been carried out for the larger output-voltage range of 0 to 30 V in Fig. 10. For the simple cascode a significant increase in

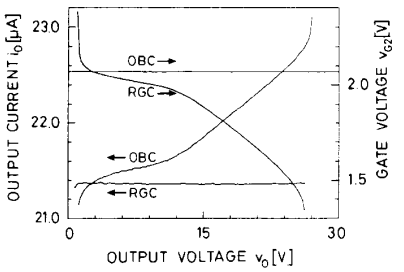

Fig. 10. Measured output characteristics of the RGC and OBC circuits in an extended voltage range.

output current above 12 V due to carrier multiplication can be noticed, until breakdown takes place at about 27 V. In contrast, the regulated cascode supplies a stable output current up to the breakdown voltage. The plot shows the feedback mechanism of the RGC circuit, i.e., how the gate voltage of T_2 varies in order to suppress the effects of carrier multiplication.

In order to compare these experimental results with the theory, the characteristic parameters of the transistors used for the measurements in Figs. 8–10 have been determined experimentally in the respective operating point: $g_{m1} = g_{m2} = 57\ \mu S$, $g_{m3} = 12\ \mu S$, $g_{o1} = g_{o2} = 3.3\ \mu S$, $g_{o3} + g_{oi} = 0.11\ \mu S$, $\beta_1 = \beta_2 = 75\ \mu A/V^2$, $V_{TH} = 0.65$ V, and $I_O = 21\ \mu A$.

From (6) and (3) we can calculate the minimum output voltages for the two cascode circuits: $V_{O\min}(\text{RGC}, r) = 0.75\ \text{V} + 0.20\ \text{V} = 0.95\ \text{V}$ and $V_{O\min}(\text{OBC}) = 0.75\ \text{V} + 0.75\ \text{V} = 1.5\ \text{V} = V_{O\min}(\text{RGC}, s)$. The merit factor for the output swing of the RGC circuit thus is $\eta_s = 1.57$, which is confirmed by (9). The theoretical values for the minimum voltages are marked in Figs. 8 and 9; they are in reasonable agreement with the measured curves. The plots suggest that the calculated value of $V_{O\min}(\text{OBC})$ is optimistic and the gain in output swing for the regulated cascode is better than the calculated merit factor.

The theoretical values of the output resistances, (4) and (5), for both cascodes are $r_{\text{out}}(\text{RGC}) = 570\ \text{M}\Omega$ and $r_{\text{out}}(\text{OBC}) = 5.2\ \text{M}\Omega$ corresponding to a merit factor $\eta_r = 110$. If these resistances are compared to the slopes of the curves in Fig. 10, we find that the actual output resistances are larger than predicted. This discrepancy can be explained by the fact that the transistor output conductances g_{o1}, g_{o2}, and g_{o3} used for the calculation were determined at the edge of saturation. According to the simple MOS model (with $\lambda \neq 0\ \text{V}^{-1}$), these conductances should stay constant in the whole saturated operating region; in reality, however, they decrease for drain–source voltages above the edge of saturation, thus leading to a higher output resistance.

V. Conclusions

A cascode circuit which improves the relevant analog characteristics of MOS transistors like usable output-voltage swing, output resistance, and feedback capacitance well beyond the values known for the simple cascodes used today has been presented. The superiority of this regulated cascode over the simple cascode circuit has been demonstrated analytically and experimentally. Applications of this circuit include high-impedance tail current sources, precision current mirrors, and differential amplifiers with high-gain, common-mode, and power-supply rejection ratios. The regulated cascode circuit is suitable for VLSI and high-frequency circuits where minimum-size transistors usually exhibiting bad dc characteristics are used.

The proposed RGC circuit has been successfully applied to the OTA's of a switched-capacitor A/D converter, to differential difference amplifiers (DDA's) [7]–[9], and to a high-frequency OTA. Further applications might be in high-frequency, high-Q SC filters [10].

The regulated cascode principle can also be realized in bipolar technology resulting in similar advantages as those described here.

Acknowledgment

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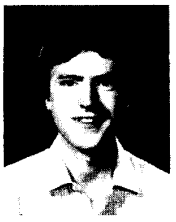

Eduard Säckinger (S'84) was born in Basel, Switzerland, on August 13, 1959. He received the M.S. and Ph.D. degrees in electrical engineering from the Swiss Federal Institute of Technology, Zurich, Switzerland, in 1983 and 1989, respectively.

In the fall of 1983 he joined the Electronics Laboratory of the Swiss Federal Institute of Technology where he investigated analog applications to floating-gate devices. His doctoral work was on the theory and CMOS integration

of a differential difference amplifier. Since September of 1989 he has worked as a consultant for AT&T Bell Laboratories, Holmdel, NJ, in the field of neural network chip design. His research interests include analog CMOS integrated circuit design.

Walter Guggenbühl (SM'60) received the diploma in electrical engineering in 1950 from the Swiss Federal Institute of Technology, Zurich, Switzerland.

He was an Assistant in the Department of Electrical Engineering of the Swiss Federal Institute of Technology for about six years, while pursuing the Ph.D. degree. Thereafter, he joined Contraves AG, Switzerland, where he was Manager of an R&D Department, involved in the field of electronic circuit and subsystem design. Since 1973 he has been a full Professor of Electronic Circuit Design at the Swiss Federal Institute of Technology. His main interests are low-noise circuits and computer hardware for signal processing.