New Improved CMOS Class AB Buffers Based on Differential Flipped Voltage Followers

Jaime Ramirez-Angulo and Sheetal Gupta
Klipsch School of Electrical and Computer Engineering
New Mexico State University
Box 30001/Dept.3-0 Las Cruces, NM 88003-0001
jramirez@nmsu.edu, sgupta@nmsu.edu

Ramon G. Carvajal
Escuela Superior de Ingenieros
University of Seville
Camino de los Descubrimientos s/n, 41092 Sevilla, Spain
carvajal@gte.esi.us.es

Antonio J. Lopez-Martin
Dpto. Ing. Eléctrica y Electrónica, Univ. Pública de Navarra
Campus Arrosadia, 31006 Pamplona, Spain
antonio.lopez@unavarra.es

Abstract— **A new family of high performance buffers is introduced. It is characterized by very low output impedance, wide signal range, wide bandwidth, low power dissipation, no DC level shift between input and output terminals and class AB operation. The proposed circuits are validated with simulations in 0.5μm CMOS technology and with experimental results.**

I. INTRODUCTION

The basic implementation of a voltage buffer is the voltage follower shown in Fig. 1a. It has an output impedance $R_{out}=1/g_m$ (~2 kΩ), gain bandwidth $GB=g_m/2\pi C_L$ and negative slew rate $SR=I_b/C_L$. Maximum and minimum input voltages are given by $Vin_{MAX}=V_{DD}$ and $Vin_{MIN}=V_{SS}+(V_{GS}+V_{DSsat})$. (Notation: C_L is the load capacitance, g_m the small signal transconductance gain, r_o the output resistance, V_{TN} and V_{TP} the threshold voltages of NMOS and PMOS transistors respectively, V_{DSsat} the drain-source saturation voltage and V_{GS} the gate-source voltage). The Flipped Voltage Follower [1], also known as super voltage follower [2] is shown in Fig. 1b and it is denoted here FVF. It is essentially a cascode amplifier with negative feedback. It has been used to implement enhanced buffers with very low output resistance $R_{out}=1/[g_m(g_m r_o/2)]$ (~50Ω). The FVF of Fig. 1b has a very limited peak to peak swing $V_{pp}=V_T-V_{DSsat}$. Fig. 1c shows a modified version of the FVF that includes a DC level shifter using a conventional voltage follower. This increases signal swing to a value $V_{pp}=2V_T$ but it requires increased power dissipation and swing is still relatively small (specially in modern deep submicrometer technologies with V_T<0.4V) and does not increase with V_{DD}. The circuits of Fig. 1 show non-negligible attenuation due to body effect, and a DC level shift between input and output terminals: $V_{out}=V_{in}-V_{GSQ1}$ (V_{GSQ1} is the quiescent gate source voltage of the input transistor). The FVF circuits of Fig. 1b and 1c are class A circuits but a simple modification reported in [3]-[4] transforms them into power efficient class AB circuits. This modification consists of adding another input transistor M1AB with its drain connected to V_{DD} as shown in dashed lines in Fig. 1. A buffer without level shift can be implemented using a differential pair with an active load and with negative feedback as shown in Fig. 2a. Other options for implementing buffers make use of one or two stage op-amps in voltage follower configuration or a cascade of a differential pair and a voltage follower [5]. The output impedance of the circuit Fig. 2a and of one stage op-amps is $R_{out}=1/g_{mDP}$ (~2kΩ) while for two stage op-amps $R_{out}=1/g_{mDP}(g_m r_o)_{II}$ (~50Ω), where g_{mDP} is the transconductance gain of the differential pair transistors, and $(g_m r_o)_{II}$ the voltage gain of the second stage in a two stage op-amp. In this paper we introduce two new high performance buffers that show no attenuation and no DC level shift between input and output terminals and that have improved output resistance and bandwidth. These are based on a new differential version of the FVF. They have signal

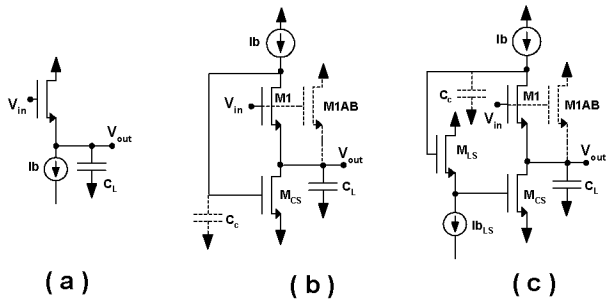

Fig. 1. Buffers with DC level shift (a) Conventional voltage follower (b) Flipped voltage follower (c) Flipped voltage follower with level shifter

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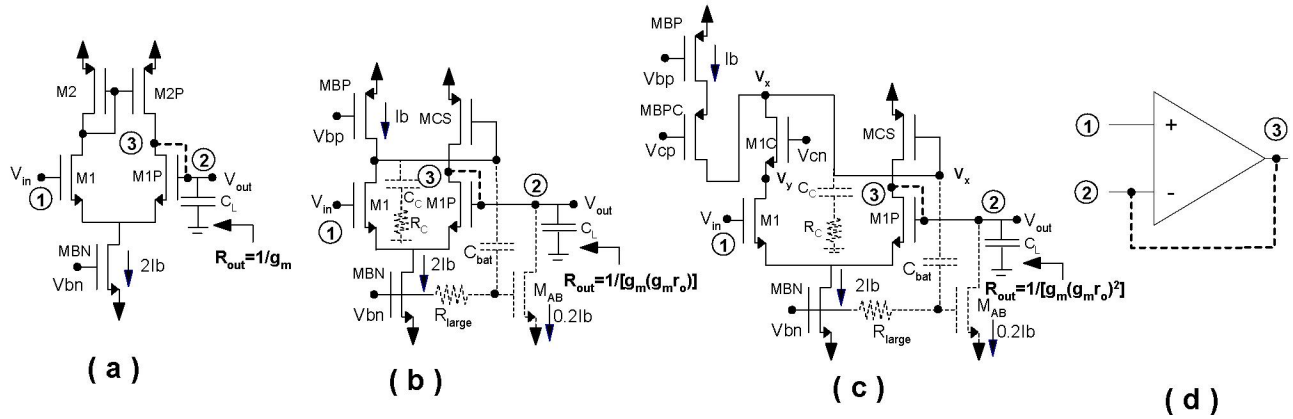


Fig. 2. Differential buffers: (a) Conventional DP buffer (b) Differential FVF buffer (c) Cascoded differential FVF buffer (d) Simplified diagram

swing comparable to the conventional buffer of Fig. 2a. One of these circuits has extremely low output resistance which is three to four orders of magnitude lower than the conventional buffer of Fig. 2a. They have the same power dissipation than the conventional buffer of Fig. 2a. We also discuss a very simple modification of the proposed circuits in order to achieve class AB operation at the expense of very small additional hardware and negligible power dissipation. This is based on the newly introduced quasi-floating gate technique [6] and on the implementation of large valued resistive elements with transistors operating in subthreshold [7]. Simulations and experimental results validate the proposed structures.

II. New Buffers Based on Differential Flipped Voltage Followers

A. *Single stage differential FVF buffers*

A simple buffer free of DC level shift between input and output terminals is shown in Fig. 2a. It consists of an active loaded differential pair with unity gain negative feedback (shown as thick broken lines connecting nodes "2" and "3"). This circuit is a class A topology and it is characterized by a gain bandwidth product $GB=g_{mDP}/2\pi C_L$, output resistance $R_{out}=1/g_{mDP}$ and symmetrical slew rate $SR=2I_b/C_L$. The slew rate is limited by the maximum output current $I_{outMAX}=2I_b$. The signal swing is characterized by $Vin_{MIN}=V_{SS}+V_{TN}+V_{DSsat}$, $Vin_{MAX}=V_{DD}-(|V_{TP}|-V_{TN})$.

Fig. 2b shows one of the proposed new buffers. It is based on a differential version of the FVF denoted here DFVF. In this circuit transistor M1 of Fig. 1b is replaced by a differential pair M1-M1P and a tail current source. This is done by diode connecting M1P, and flipping the current sensing transistor MCS from NMOS to PMOS type. This has the benefit of an increased range characterized by maximum and minimum input voltages: $Vin_{MAX}=V_{DD}-V_{DSsat}$ and $Vin_{MIN}=V_{SS}+V_{GS}+V_{DSsat}$. This circuit is characterized by no attenuation, no DC level shift and output resistance $R_{out}=1/[g_m(g_m r_o)]$ (~50Ω). Fig. 2c shows another buffer where an additional cascoding transistor M1C is introduced in the negative feedback loop formed by M1-M1P, MCS and M1C. In this case the FVF corresponds to a folded double cascoded amplifier with unity gain negative feedback. M1C increases the open loop gain of the cascode amplifier negative feedback loop by the factor $g_{m1C}\,r_{o1C}$ of M1C and leads to an extremely low output resistance $R_{out}=1/[g_m(g_m r_o)^2]$ (~1Ω). This buffer has a slightly reduced swing since the maximum input voltage is $Vin_{MAX}=V_{DD}-2V_{DSsat}-(|V_{TP}|-V_{TN})$. For example with V_{DS}=0.15V and in 0.5μm CMOS technology with V_{TN}=0.75V and V_{TP}=-0.95V this leads to $Vin_{MAX}=V_{DD}$-0.5V. All FVF based buffers of Fig. 2 have a bandwidth which is higher by almost one order of magnitude than the bandwidth of the conventional buffer of Fig. 2a and are characterized by very low distortion as it is discussed later.

B. *Modification of differential FVFs for Class AB operation.*

The FVF buffers of Fig. 2b and 2c are class A circuits and have asymmetrical slew rate. This is due to the fact that the current sensing transistor MCS can source large currents into C_L but the maximum negative current in C_L is limited by the bias current $2I_b$. A simple modification transforms the FVF buffers of Fig. 2 into power efficient class AB circuits. This modification is based on the quasi-floating gate technique described recently [6]. It requires an additional transistor MAB. The gate of MAB is connected to the DC biasing voltage V_{bn} through a very large valued resistive element R_{large} (~100GΩ) and it is also connected to the gate of the current sensing transistor MCS through a capacitor C_{bat}. This transistor has a quiescent gate voltage $V_{bn}'=V_{bn}$ and small dimensions $(W/L)_{AB}=(W/nL)$ with $n>3$ and for this reason it has a small quiescent drain current (~$2I_b/n$). Under dynamic conditions R_{large} prevents flow of charge into the

gate of MAB and for this reason C_{bat} performs as a floating battery so that V_{bn}' follows the gate voltage variations of MCS. During negative slewing (when negative current flows into C_L), M1 and M1p have a constant current and MCS decreases its drain current and increases its gate voltage. This causes the gate voltage V_{bn}' of MAB to increase so that its drain current can increase significantly over the quiescent value $2I_b/n$. During positive slewing the gate of MCS decreases. Due to this it can provide very large positive currents to C_L which can be much larger than $2I_b$. At the same time MAB decreases its current and turns off. This provides class AB operation to the proposed buffers of Figs. 2b and 2c. R_{large} is implemented with a minimum size transistor operating in subthreshold mode according to the techniques described in [7]. C_{bat} requires a relatively small valued capacitance ~1pF.

C. *Utilization as op-amps and rail to rail operation*

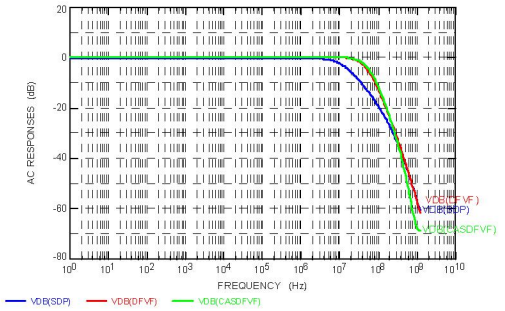
The FVF circuits of Figs. 2b and 2c can be used as power efficient class AB low output resistance single stage op-amps by opening the diode connection in M1P and using terminals "3" and "2" as op-amp output and negative input terminals respectively. Input rail to rail operation can be provided easily to all circuits by using the techniques discussed in [8]. This takes place at the expense of reduction by approximately a factor two in the open loop gain.

III. Simulation Results.

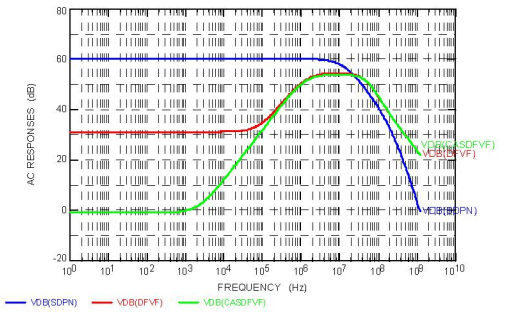
The circuits of Fig. 2 were simulated in SPICE using 0.5μm CMOS AMI-MOSIS technology parameters with supplies V_{DD}=1.5V, V_{SS}=-1.5V, I_b=30μA load capacitance C_L=10pF and phase lead compensation elements C_C=2pF and R_C=13kΩ. Transistor sizes were W/L=48/0.6 for PMOS and NMOS transistors with quiescent current $2I_b$ and 24/0.6 for transistors with quiescent current I_b. MAB had dimensions W/L=12/0.6, R_{large} was implemented with a minimum size transistor biased in subthreshold and C_{bat}=1pF). Fig. 3a shows a comparison of the frequency response of the circuits of Fig. 2. It can be observed that the FVF buffers have bandwidths BW=70MHz while the conventional buffer has a bandwidth BW=11MHz. Simulated THD was 0.11%, 0.25%, 0.23% for 300mV$_p$ input signals with 2MHz frequency and for the circuits of Figs. 2a, 2b and 2c respectively. Fig. 3b shows a comparison of the (magnitude) of the output impedance obtained by applying a 1A AC current source to the buffer's output terminals with the input grounded. The voltage in this case corresponds directly to the output impedance. It can be seen that the simple buffer of Fig. 2a has an output impedance of 2kΩ, the FVF buffer of Fig. 2b on the order of 40Ω, the buffer of Fig. 2c approximately 0.5Ω. All circuits have similar peak-peak swing of 1.6V with exception of the circuit of Fig. 2c that has slightly reduced swing. Fig. 4a shows a comparison of the pulse response without the class AB elements (MAB, R_{large} and C_{bat}). The maximum and minimum levels of the input pulse waveform were selected to avoid output saturation (from –0.6V to 1V). It can be seen that the conventional buffer of Fig. 2a has, as expected, symmetrical slew rate with relatively slow rise and fall times (both limited by $2I_b$) while the other circuits have a very short rise time (due to the sourcing effect of MCS with current not limited by $2I_b$) and a similar slow fall time (limited also by $2I_b$). Fig. 4b shows a comparison of the buffer pulse responses including the class AB elements (MAB, C_{bat} and R_{large}). It can be seen that the FVF buffers show class AB operation with enhanced fall times. Figs. 5a and 5b show plots of the load currents in C_L for the class A and class AB cases respectively. It can be seen that the class AB versions of the FVF circuits have peak load currents essentially larger than $2I_b$ while for the class A circuit of Fig. 2a the peak current corresponds to the value of $2I_b$ (60μA).

IV. Experimental Results

Functionality and the basic characteristics (gain, offset, output impedance bandwidth, positive and negative slew rate) of the circuits of Fig. 2 has been verified using breadboard prototypes built with ALD1106 and ALD11007 transistor arrays. Testing was done with V_{DD}=2V, V_{SS} =-2V and I_b=50μA. Negligible attenuation and no DC level shift could be verified experimentally in all cases. Measured



(a)



(b)

Fig. 3. (a) Frequency response comparison.
(b) Output impedance comparison.
Simple differential pair buffer V(SDPN), differential FVF buffer V(DFVF), cascaded FVF buffer V(CASDPFVF)

output impedance of the circuits of Figs. 2a, 2b and 2c was 4.5kΩ, 300Ω, and 20Ω, respectively. Higher values are attributed to the relatively low transconductance gain factors and relatively large channel length modulation parameters of the commercial arrays. Experimental bandwidth was approximately 2MHz with load capacitance C_L=100pF.

V. Conclusions

Two new high performance single stage buffers based on differential FVFs were introduced. They are characterized by low static power dissipation, no attenuation, no DC level shift between input and output, very low output resistance, wide signal swing, enhanced bandwidth and low distortion. A simple modification to achieve class AB operation with dynamic output currents significantly larger than the bias current was introduced. The characteristics of the proposed circuits were validated with simulations and experimentally.

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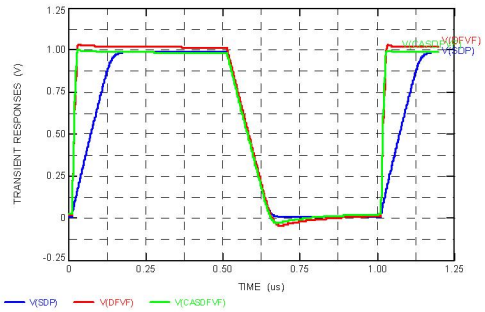
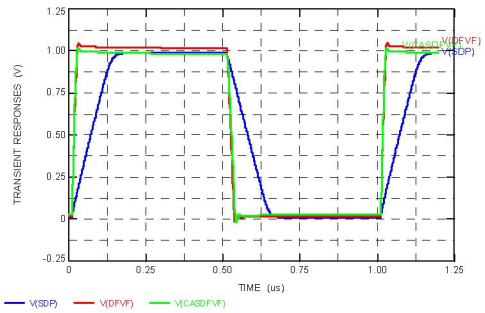
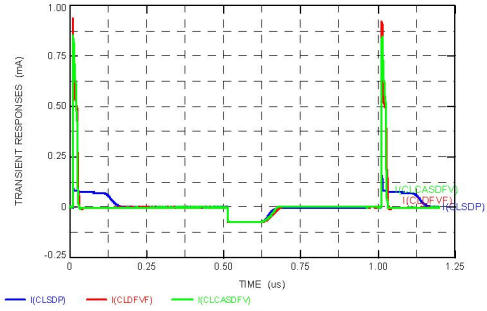


(a)

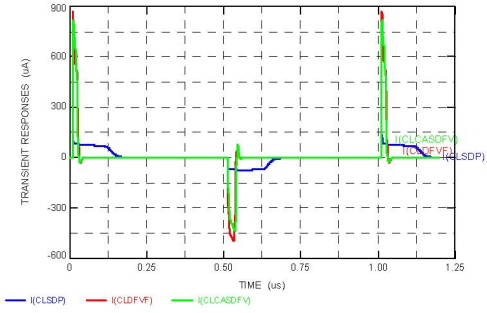


(b)

Fig. 4. Buffer pulse response comparison: differential pair buffer: (a) class A buffers (b) Class AB buffers. Simple differential pair buffer V(SDP), differential FVF buffer V(DFVF), cascoded FVF buffer V(CASDFVF)



(a)



(b)

Fig. 5. Load current comparison: differential pair buffer: I(CLSDP), differential FVF buffer I(CLDFVF), cascoded FVF buffer I(CLCASDFVF) (a) Class A buffers (b) Class AB buffers