Output stage for low supply voltage, high-performance CMOS current mirrors

A. Torralba, R.G. Carvajal, J. Ramírez-Angulo and F. Muñoz

A new simple output stage for CMOS current mirrors is presented. The stage is a new low-voltage regulated cascode circuit, which achieves a very high output impedance and accurate current copy when combined with the input stage shown by Rijns. A 122 MHz bandwidth with 1 V supply voltage has been obtained using a standard 0.35 μm CMOS technology.

Introduction: Low supply, high-performance, CMOS current mirrors use the input stage in Fig. 1*a* that provides shunt feedback to achieve low input impedance with very low input voltage requirement. A high performance current mirror should also provide accurate current copy and very high output impedance. It has to be able to operate at a high frequency with low supply voltage and low input/output voltage requirements. Several output stages for low voltage CMOS current mirrors have been proposed. Fig. 1*c* [1] is a complex implementation of the well-known regulated cascode output stage of Fig. 1*b* [2], where the drain to source voltage V_{DS} of transistor M_2 is forced to be equal to that of transistor M_1 by means of feedback, using two opamps.

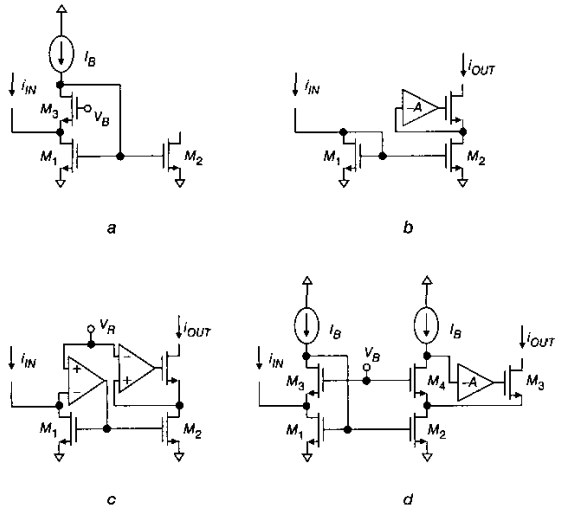

Fig. 1 *High-performance low-voltage current mirrors*
a Input stage [1] *b* Reference [2] *c* Reference [3] *d* Proposed current mirror

In this Letter a new simple output stage for high performance CMOS current mirrors with low voltage supply requirements is proposed (Fig. 1*d*). It uses the input stage of Fig. 1*a* [3], which forces the V_{DS} voltage of transistor M_1 to a constant value by means of transistor M_3, current source I_B, and voltage source V_B. A replica of this circuit is used to force the V_{DS} voltage of the output transistor M_2 to be equal to that of transistor M_1 by means of transistor M_4, current source I_B, and voltage source V_B. To have high output impedance, the output cascode transistor M_5 is driven by the drain of transistor M_4. As the polarity in the drain of transistor M_4 is reversed, an inverting stage is required to drive the gate of transistor M_5. This inverting stage provides additional gain-boosting, which increases the output impedance [4]. A simple implementation of the proposed current mirror is depicted in Fig. 2*a*, where the inverter amplifier has been implemented by means of transistor M_6 and biasing current I_{B1}. Note that transistors M_4, M_5, and M_6, and their biasing currents I_B and I_{B1} implement a 'super-cascode transistor'.

Discussion: Unlike other existing current mirrors, in the proposed one, the input and output stages are decoupled. The analysis of the input stage can be found elsewhere [5]. The minimum supply voltage is limited by the path formed by I_B, M_3, and M_1, to $V_{DDmin} = V_{TN} + 3\ V_{DSsat}$, where V_{TN} is the transistor threshold voltage and V_{DSsat} is the minimum drain-to-source voltage required to maintain a transistor in saturation. V_{DDmin} is about 900 mV for a 0.35 μm CMOS technology with $V_{TN} = 600$ mV. Due to the input feedback, it has a very low input impedance given by $R_{in} \simeq 1/(g_{m3}\ g_{m1}\ r_{o3})$, where g_{mi} and r_{oi} are the transconductance and output resistance of transistor M_i, respectively. Concerning the proposed output stage, as it uses a replica circuit, it has the same supply voltage requirements of the input stage. Its output impedance, given by $r_{out} \simeq g_{m6}\ r_{o6}\ g_{m5}\ r_{o5}\ g_{m4}\ r_{o4}\ r_{o2}$, is very high (in the GΩ range).

When compared to the current mirrors in Figs. 1*b* and *c*, the proposed current mirror has better performances in terms of low input voltage and low input impedance at the input stage, without the stability problems of the circuit in Fig. 1*c*. Like the circuit in Fig. 1*c*, it forces $V_{DS1} = V_{DS2}$ for accurate current copy, but the circuit in Fig. 1*c* does it indirectly, using two opamps. As a consequence, the difference between V_{DS1} and V_{DS2} is limited by the cumulative input offset and gain errors of both opamps. This degradation effect increases with frequency. The circuit proposed in this Letter forces $V_{DS1} = V_{DS2}$ in a more efficient way in terms of area, power consumption, and speed, as it uses a simple replica bias circuit to perform this task.

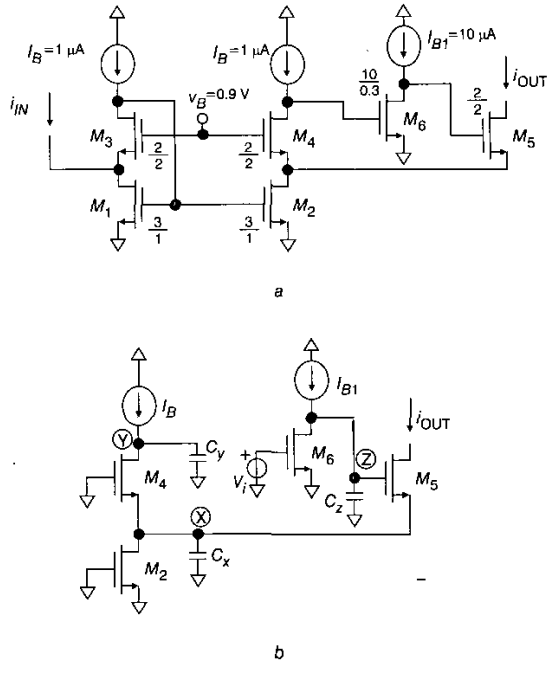

Fig. 2 *Current mirror implementation and AC open loop model*
a Current mirror implementation *b* AC open loop model

Stability conditions: Open loop analysis of the input section can be found elsewhere [5]. It can be shown to have a gain-bandwidth product and a non-dominant pole given by $GB_{IN} = g_{m1}/C_1$ and $p_a = g_{m3}/C_2$, where C_1 and C_2 are the parasitic capacitances at the drain of transistors M_3 and M_1, respectively. Absolute stability without compensation can be guaranteed if condition $p_a > 2\ GB_{IN}$ is satisfied (i.e. $g_{m3} > 2\ g_{m1}$).

Open loop analysis of the output section (Fig. 2*b*) shows a system with three poles located in nodes X, Y, and Z. The open loop gain is given by $A_L \simeq -g_{m4}\ r_{o4}\ g_{m6}\ r_{o6}$. To ensure stability with such a high open loop gain, it is necessary to have one dominant pole and two high frequency poles. The pole located at node X ($p_x \simeq (g_{m4} + g_{m5})/C_x$, where C_x is the capacitance at node X), is at a high frequency pole. However, nodes Y and Z are high-impedance nodes and their associated poles can be close in frequency. To have a dominant pole at node Y, there are different possibilities:

(i) To make the equivalent resistance at node Y very high using non-minimum transistor channel length to implement current source I_B and transistor M_4, and a selecting a value of I_B relatively low. Also making the equivalent resistance at node Z as low as possible using minimum transistor channel lengths to implement current source I_{B1} and transistor M_5, and selecting a value of I_{B1} relatively high compared to I_B.

(ii) To use a Miller compensating capacitor between nodes Y and Z.
(iii) To combine both techniques.

Circuit simulations and experimental results: The circuit in Fig. 2*a* was designed using the AMS 0.35 μm CMOS technology with a 1 V supply voltage and a load resistance of 10 KΩ. Transistor sizes and values of biasing currents and voltages are shown in Fig. 2*a*. No compensating capacitor was required. The frequency response of the proposed current mirror was simulated with SPECTRE using BSIM 3.3 transistor models. Fig. 3*a* shows a −3 dB bandwidth of 122 MHz. The simulated input referred noise was 1.5 pA/√Hz at 10 MHz. Fig. 3*b* shows the transient response. The 1% settling time for a 4 μA step is approximately 20 ns. The circuit is highly linear, with −66 dB of THD at 100 KHz. The experimental DC output characteristics were measured via an experimental chip prototype. The voltage at the output node was swept from 0 to 1 V, and the input current i_{IN}, was stepped from 1 to 20 μA, using a curve tracer. The measured value for the voltage at the input node was approximately constant and close to 155 mV. A very high output impedance (in the range of GΩ) was observed for an output current $i_{OUT} = 10$ μA and output voltages larger than 220 mV.

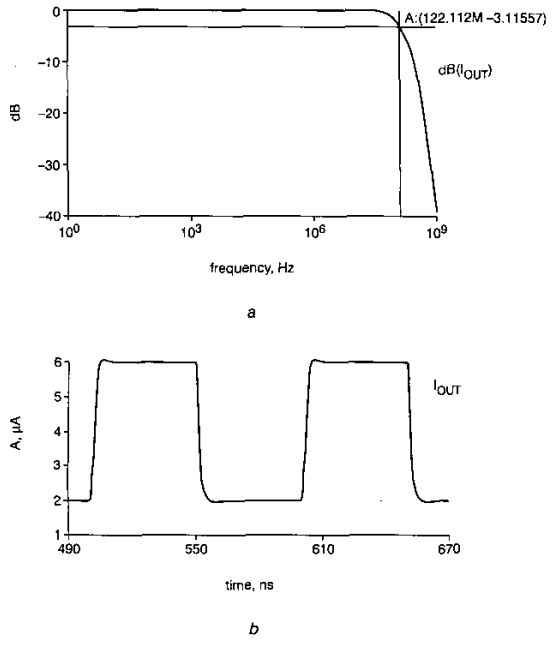

Fig. 3 *Simulation results*
a Frequency response *b* Transient response

Conclusions: An efficient implementation of a low-voltage high-performance output stage for CMOS current mirrors has been presented and verified through simulations and experimental results. The supply requirements of the mirror's control circuitry are close to a transistor's threshold voltage. An implementation of the proposed scheme using a standard 0.35 μm CMOS technology shows a 122 MHz bandwidth, very high output impedance and very low input impedance with only 1 V of supply voltage. The circuit can be used as a building block in low-voltage mixed-mode VLSI systems.

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100 Gbit/s multiplexing and demultiplexing IC operations in InP HEMT technology

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The 100 Gbit/s multiplexing operation of a selector IC and the demultiplexing operation of a D-type flip-flop (D-FF) using a production-level 0.1 μm-gate InP HEMT IC technology is described. Eye-openings of the selector IC at 100 Gbit/s and its error-free operation were confirmed using a test chip containing the selector and the D-FF. To the authors' best knowledge, this is the first report of 100 Gbit/s operation of a transistor-based integrated circuit.

Introduction: High-speed integrated circuit (IC) technology has greatly contributed to the development of economical high-speed and large-capacity optical communication systems. The announcement of the optical transport network standard based on 40 Gbit/s electrical multiplexing technology [1] has accelerated the race to develop cost-effective 40 Gbit/s ICs. The possibility of 100 Gbit/s class electronics is now being discussed [2]. In the last few years, high-speed multiplexing operations at over 80 Gbit/s have been reported for selector ICs using InP HEMT [3,4] and InP HBT [5] technologies. The record operating speed is, however, still 90 Gbit/s [4]. Furthermore, the performance of all these ICs was characterised only by means of a waveform observation on digitising sampling oscilloscopes. Such observation is necessary for IC characterisation, but it alone is not sufficient because a non-return-to-zero (NRZ) signal of over 80 Gbit/s has higher frequency components than the 50 GHz bandwidth of the oscilloscopes. Error-free operation should be confirmed through bit error rate measurements along with waveform observations.

Circuit configurations: The circuit block diagram of the selector IC is shown in Fig. 1*a*. The IC consists of two data buffers, a clock buffer, and a 2:1 selector core circuit. The most important feature in the circuit configuration is the elimination of both output buffers and the driver, which are normally incorporated into the IC to amplify the output signal of the 2:1 selector core to the voltage level that can drive the external 50 Ω load. The required bandwidth for these amplifiers is approximately over 70% of the data bit rate, but it is not easy to satisfy the requirement for the 100 Gbit/s NRZ signals. To avoid this problem, we designed the 2:1 selector core so that it can directly drive the external 50 Ω load, as shown in Fig. 1*b*. The circuit is based on the two-stage series-gated circuitry of conventional source-coupled FET logic, in which source followers are omitted to achieve an open drain circuit configuration with impedance-matched internal termination resistors *RT*1 and *RT*2. To improve the circuit speed further, an inductor peaking technique that enhances the voltage gain at around 50 GHz was incorporated. We set the gate width of the selector core so as to output a 1 Vp-p voltage swing.

For bit error rate measurements of the 100 Gbit/s selector IC, we first need a packaged D-FF or demultiplexer IC that can demultiplex the 100 Gbit/s signal into 50 Gbit/s signal. Since such packaged ICs are not