the effectiveness of the proposed CMFB. Fig. 3 shows the percentage voltage change at the output of the first stage ($V_{o1}^+$, $V_{o1}^-$) due to a change in $V_{b2}$ for two cases: when the CMFB is not active and when the CMFB is active. Clearly, the proposed CMFB is very effective in reducing the effect of some of the parameter variations during the fabrication process.

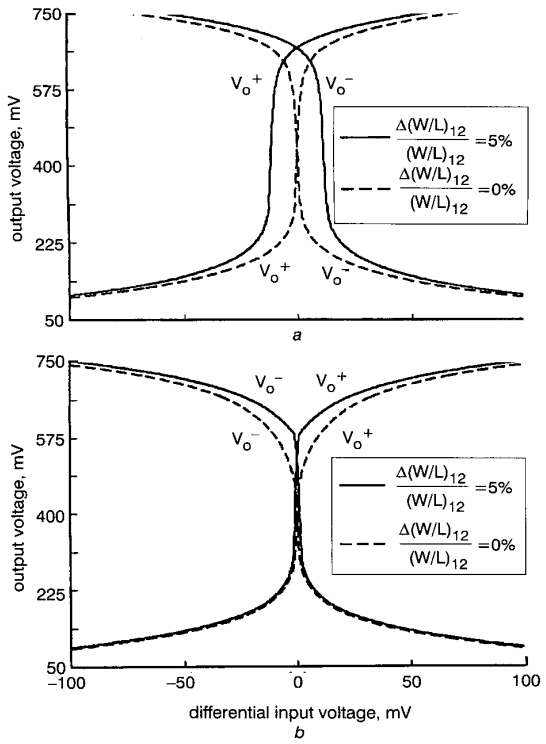


**Fig. 2** *DC transfer characteristic of folded cascode amplifier*
*a* Without CMFB
*b* With CMFB

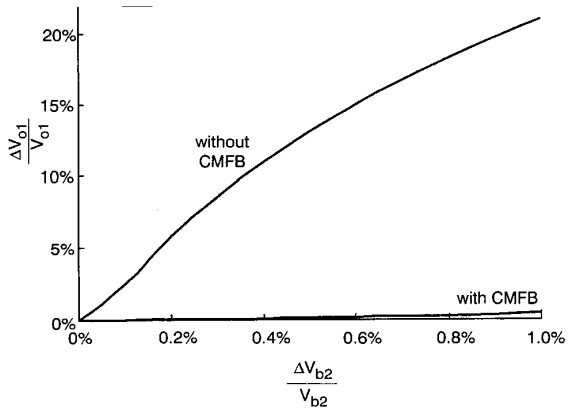


**Fig. 3** *Percentage change in $V_{o1}$ due to change in $V_{b2}$*

**Table 1:** Performance parameters of amplifier ($V_{dd}$ = 0.8 V)

| | Schematic simulation | | Post-layout simulation | |
|---|---|---|---|---|
| | Without CMFB | With CMFB | Without CMFB | With CMFB |
| DC differential gain | 52.05 dB | 51.95 dB | 52.19 dB | 52.17 dB |
| CMRR | 36.0 dB | 47.4 dB | 35.9 dB | 51.8 dB |
| Unity gain BW ($C_L$ = 1 pf) | 40.44 MHz | 40.44 MHz | 43.16 MHz | 41.53 MHz |
| Phase margin | 69° | 69° | 71.9° | 71.4° |
| Die area | – | – | 3165 (μm)$^2$ | 3825 (μm)$^2$ |

In the case of low voltage amplifiers, obtaining a high CMRR is not very simple. For the above amplifier the output resistance of the current source M11 affects the CMRR. Using the proposed CMFB circuit the output resistance of current source M11 is increased and the CMRR is improved. Table 1 shows some of the performance parameters of the amplifier obtained from schematic and post-layout simulations. As can be seen, the proposed CMFB circuit has increased the CMRR of the amplifier while it has a negligible effect on the differential mode parameters.

*Conclusion:* A 0.8 V fully differential folded cascode amplifier with a new continuous time common mode feedback has been presented. The circuit has been simulated and laid out using 0.18 μm CMOS technology. The proposed CMFB technique is effective for reducing parameter perturbations during fabrication. It also improves the CMRR of the amplifier. This technique is especially suitable for low-voltage applications where it is not possible to use several transistors in series between the supply rails and there is not enough voltage overhead to tolerate parameter variations. Even though the proposed technique is used in the folded cascode amplifier, it can be used for other kinds of differential amplifiers as well.


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## Simple technique using local CMFB to enhance slew rate and bandwidth of one-stage CMOS op-amps

J. Ramirez-Angulo and M. Holmes

A simple modification to a one-stage op-amp for operation as a class AB amplifier leads to significant slew rate and bandwidth enhancement with essentially equal silicon area and static power dissipation requirements. Experimental results of a prototype in 0.5 μm CMOS verify SR and bandwidth enhancement factors of almost one order of magnitude.

*Introduction:* It is well known that the maximum gain-bandwidth (GB) product of a one stage operational amplifier (Fig. 1*a*) is limited by the internal pole(s) of the amplifier, mainly, by those associated to the internal mirror (nodes A and B in Fig. 1*a*). Typically the condition $GB < 2\omega_{PA}$ is used as a practical design guideline in order to provide enough phase margin [1, 2]. Wireless and other battery powered systems require high GB values, high slew rates (SR), and at the same

time very low static power dissipation. These requirements are difficult to achieve with class A configurations. Class AB amplifiers can be used for this purpose [3]. A simple modification to the conventional one stage op-amp is discussed which transforms it into a very efficient class AB circuit. The modified circuit is shown in Fig. 1*b*. In this circuit the active load transistors M3,4 are reconnected to have a common gate (node C) and matched resistors R1, R2 are used to connect the gate and drain terminals of M3, M4. This simple modification, denoted by other authors [1, 4] as local common mode feedback, leads to essential SR and GB improvements in one-stage op-amps as will be shown

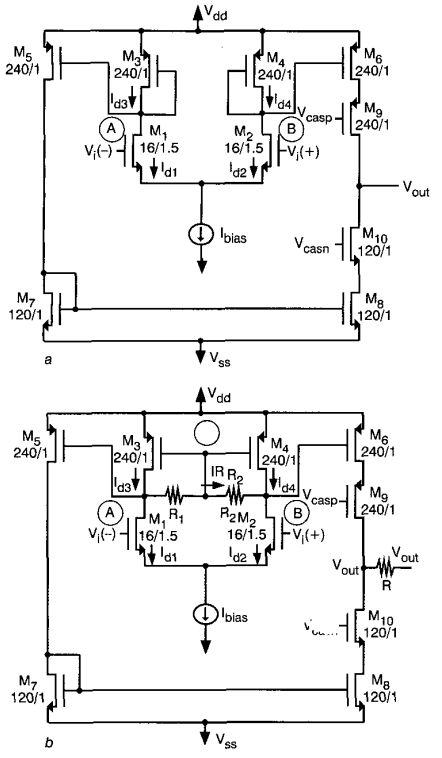


**Fig. 1** *One stage OTA*

*a* Conventional cascode structure *b* Proposed high slew rate structure

*Conventional op-amp:* Fig. 1*a* shows a conventional one stage op-amp. The internal poles of this op-amp are given approximately by: $f_{PA}=g_{m3,4}/2\pi C_A$ where $g_{m3,4}$ is the small signal transconductance gain of M3,4 and $C_A=C_B$ is the parasitic capacitance associated to node A (or B). This is determined mainly by the gate-source parasitic capacitances of M3 and M5: $C_A=C_{gs3}+C_{gs5}$. The open loop gain is given by $A_{OL}=g_{m1}R_{\text{out}}$ where $R_{\text{out}}$ is the output resistance and $g_{m1}$ the small signal transconductance gain of M1, M2. The output dominant pole is given by $f_{P\text{out}}=1/(2\pi R_{\text{out}}C_L)$. The gain-bandwidth product is given by $GB=g_{m1}/(2\pi C_L)$ where $C_L$ is the load capacitance. For a given load capacitance the SR is limited by the bias current $I_{bias}$ and given by: $SR=I_{bias}/C_L$. $I_{bias}$ is related to the quiescent drain-source saturation voltage $V_{DS,SAT}$ and the transconductance gain factor $\beta$ of transistors M3–M6 by the expression $I_{bias}/2=\beta\,(V_{DS,SAT})^2$.

*Modified op-amp:* Fig. 1*b* shows the modified op-amp. For quiescent (or common mode) operation the drain currents of all transistors M1–M10 have equal values ($I_{bias}/2$) while the current $I_R$ in resistors R1,2 is zero. The source-gate voltage of M3,4 is the same as their drain-source voltage. For common mode signals these transistors perform as a low impedance (diode connected) load with value $R_{L,CM}=1/g_{m3,4}$. Upon application of a differential signal, the signal component ($I_R$) of $Id1,2$ flows through resistors R1,2 ($Id1=(I_{bias}/2)+I_R$, $Id2=(I_{bias}/2)-I_R$, $I_R\simeq g_{m1,2}v_d/2$) while the drain currents in M3,4 remain unchanged. The current $I_R$ generates differential complementary voltage changes at nodes A and B. Given that the common gate of M3,4 has a constant voltage, the differential signal impedance at nodes A and B is given by:

$$R_A=R_B=R1,2\|r_{o3,4}\|r_{o1,2} \tag{1}$$

Signal voltages at nodes A and B are given by:

$$V_A=-V_B=I_R R_A \tag{2}$$

The open loop gain of the op-amp of Fig. 1*b* is given by:

$$A'_{OL}=g_{m_1}R_A g_{m_5}R_{\text{out}} \tag{3}$$

The pole at A (B) is given by:

$$f'_{PA}=1/2\pi R_A C'_A \tag{4}$$

where:

$$C'_A\simeq C_A/2=C_{GS5} \tag{5}$$

Given that node C is a virtual ground, the parasitic capacitance at node A (B) does not include the gate-source capacitance of M3 (M4), and it is reduced by approximately a factor 2: $C'_A\approx C_{GS5}=C_A/2$.

It can be seen that resistors R1,2 provide class AB operation to the shell of the op-amp (section formed by transistors M5–M10). The maximum output current is given by:

$$I_{\text{OUT}}^{\text{MAX}}=\beta(V_{DS,SAT3,4}^{Q}+\Delta V_{GS}^{\text{MAX}})^2 \tag{6}$$

where $\Delta V_{GS}^{\text{MAX}}=(I_{bias}/2)\,R1,2$ represents the maximum swing at nodes A and B and unity gain mirrors are assumed.

*Remarks on modified op-amp:* (i) By proper selection of R1,2 the maximum output current can be made essentially larger than the maximum current of a class A op-amp ($I_{bias}$). From (6) a selection $V_{DS,SAT\,3,4}^{Q}+\Delta V_{GS}^{\text{MAX}}>\sqrt{2}(V_{DS,SAT})$ leads to $I_{\text{OUT}}^{\text{MAX}}>I_{bias}$ and improved SR. (ii) The product $R_A g_{m5}$ determines the open loop gain and GB enhancement factor. (iii) A resistor R between the op-amp output terminal and $C_L$ (Fig. 2) can be used to provide phase lead compensation. R in combination with $C_L$ introduces a left-half plane zero $f_Z$ in the op-amp open loop gain at a frequency $f_Z=1/RC_L$. For $f_Z=f_{PA}$ the zero cancels the phase of the internal op-amp pole and allows to extend GB even further. The ideal condition for the phase cancellation is: $RC_L=C'_A R_A$. (iv) The value R1,2 can be used to trade off GB/SR enhancement with phase margin reduction. Implementation of R1,2 with MOS transistors allows a programmable value for R1,2. (v) For large values $R1,2\simeq r_{o3,4}\|r_{o1,2}$ the op-amp behaves as a two stage amplifier. R1,2 enables a gradual transition from a one stage op-amp behaviour (for $R1,2\simeq 1/g_m$) to a two stage amplifier (for $R1,2\simeq r_{o3,4}\|r_{o1,2}$). In this last case, cascoding transistors are not required, and Miller compensation should be used. (vi) Class AB operation improves linearity (the analysis is not presented here for the sake of space). This is important for many applications (high resolution D/A converters, linear OTA-C circuits, etc.). (vii) The scheme is especially attractive since it does not impose additional silicon area (resistors R1,2 require small size MOS transistors) and/or additional static power dissipation. (viii) The scheme is very efficient since large dynamic output currents only flow in the op-amp shell while the internal section (M1–M4) has the same dynamic power dissipation as the conventional op-amp.

*Design example:* PMOS transistors were used to implement resistors $R1,2$ that can take values from 1 to 2 kΩ by adjusting $V_R$ from −2.5 V to −1.0 V. Utilisation of $I_{bias}=80$ μA, $C_L=5$ pF, and transistors sizes shown in Fig. 1*b*, lead to $V_{DS,SAT}=0.1$ V, transconductance gain $g_m=750\ \mu\text{A/V}^2$ for M3–M6, and $g_{m1,2}=375\ \mu\text{A/V}^2$, with $C_{GS3,4}=C_{GS5,6}\simeq 1$ pF. A conventional op-amp with the same bias current and transistor sizes as those of the modified op-amp is considered for comparison purposes. The conventional op-amp has: $GB=12$ MHz, $f_{pA}=42$ MHz, and $SR=16\ \text{V/μS}$. By selecting $R1,2=8$ kΩ (such that $g_{m5}R_A=3$) values $GB'=36$ MHz, $SR'=141\ \text{V/μs}$ and $f'_{pA}=30$ MHz result for the modified op-amp. It can be seen that GB increases by a factor 3 and SR by a factor 8.8. The internal pole is reduced from 42 MHz to 30 MHz but phase lead compensation (with $R=400\ \Omega$, Fig. 2*a*) allows stable operation.

*Simulation results:* Fig. 2 shows a comparison of the pulse response of the op-amp of Fig. 1*b* in voltage follower configuration and the conventional op-amp with identical transistor sizes. Control voltages $V_R = -2.5, -1.5, -1$ were used for the simulations. 0.5 μm CMOS technology parameters and transistor sizes of Fig. 1*a* were used for the simulations. It can be seen that the SR increases by a factor close to 20. AC simulations (omitted for space) indicated bandwidth increasing from 1.5 MHz for the conventional op-amp to 8.35 MHz for the modified op-amp.

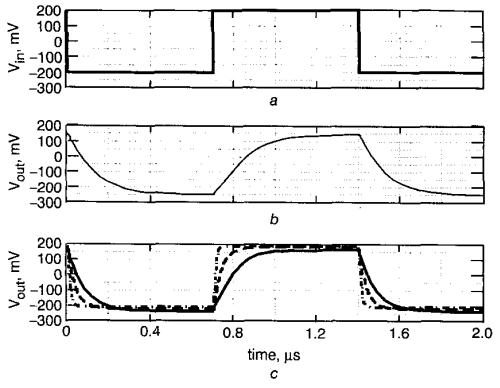


**Fig. 2** *Transient simulations*
*a* Input signal
*b* Response of conventional op-amp
*c* Response of modified op-amp for three values of control voltage $V_R$

*Experimental results:* A test chip prototype including a conventional and a modified op-amp was fabricated in 0.5 μm CMOS (MOSIS) technology. The op-amp had dimensions of $\sim 300 \times 150\ \mu m^2$. Experimental values for GB and SR (with $I_{bias} = 80\ \mu A$, $C_L = 5$ pF, $V_{DD} = -V_{SS} = 2.5$ V, $V_R = -2.5$ V) showed a factor close to 3 improvement for both SR and GB. The modified op-amp had experimental values $GB' = 20$ MHz and $SR' = 11$ V/μS while the conventional op-amp had values $GB = 7$ MHz and $SR = 3.5$ V/μS.

*Conclusions:* A simple scheme to improve SR and gain-bandwidth of a one stage op-amp was presented. The scheme was verified experimentally and it is especially attractive since it requires no additional silicon area and/or power dissipation.

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## Axial ratio improvement in aperture antennas using high-impedance ground plane

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High-impedance surfaces are studied as a means of improving the radiation pattern symmetry in aperture antennas. Compared to a solid metal ground plane, the results suggest that high-impedance surfaces can significantly improve the axial ratio of circularly polarised antennas. This can be used to reduce interference between left and right polarisation components.

*Introduction:* Many communication systems use circular polarisation. However, the task of designing an antenna that transmits or receives in circular polarisation over a wide range of angles is often complicated by the presence of the metallic structures on which the antenna is mounted. For example, antennas on a flat metal ground plane will tend to emit in vertical polarisation at low angles, because horizontal fields are shorted by the metal surface, while vertical fields can propagate along the metal. We often describe the polarisation purity of a wave in terms of its axial ratio, which is the ratio of the major axis to the minor axis of the polarisation ellipse.

It is known that a variety of surface textures can improve the radiation characteristics of antennas. Soft and hard surfaces [1] are often used to alter the electromagnetic boundary condition of a metal surface, to either suppress or enhance surface waves of either polarisation. These typically consist of corrugations running either transverse or longitudinal to the direction of propagation across the surface. For example, a radially symmetric soft surface has been shown to reduce the axial ratio of various kinds of circularly polarised antennas [2]. However, for arrays or other complex antennas, where one may want to surround several separate radiators with such a material, it may not be possible to use a structure with only radial symmetry. Another candidate is a two-dimensionally periodic structure called the high-impedance surface.

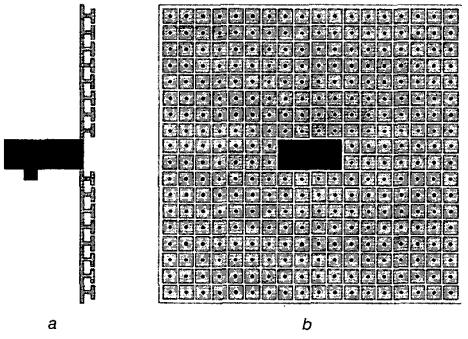


**Fig. 1** *Side and front view of aperture antenna in high-impedance surface*
*a* Side view
*b* Front view

*High-impedance surface:* By covering a metal sheet with a resonant surface texture, we can alter its electromagnetic surface impedance, and also its surface wave properties. One such texture is a two-dimensionally periodic structure often known as a high-impedance surface [3]. It consists of an array of small metal patches connected to the metal surface by conducting posts. It is often built using printed circuit board techniques. An example of such a structure is shown in Fig. 1. The surface can be modelled as a resonant LC circuit, where the proximity of the metal patches provides capacitance, and the conductive path between them provides inductance. Near the resonance frequency, the impedance of the surface is high compared to the impedance of free space, and the surface has a reflection phase of 0, compared to a flat metal surface with a reflection phase of $\pi$. For the surface studied in this Letter, we used metal patches 3.2 mm$^2$, and with a lattice constant of 3.7 mm. The circuit board was made of Rogers Duroid 5880, and was 1.57 mm thick. These dimensions provide a resonance frequency near 15 GHz.

The resonance frequency lies within a surface wave bandgap, where surface waves of both TM and TE polarisation are suppressed. An example of this suppression is shown in Fig. 2. Two small coaxial