Feedforward Compensation Techniques in the Design of Low Voltage Opamps and OTAs

Suma Setty (currently at)
Ericsson Components AB
Pagoda House
Westmead Drive
Swindon SN5 7UN
email: s.setty@swindon.ericsson.se

Chris Toumazou
Information Engineering
Dept. of Electrical & Electronic Engineering
Imperial College
London SW7 2B
email: c.toumazou@ic.ac.uk

Abstract:

This paper presents feedforward compensation techniques for low voltage fully differential folded cascode amplifiers and OTAs. Fully differential folded cascode cells have been fabricated and tested with different feedforward configurations in order to demonstrate and compare the usefulness of these techniques for broadbanding the Gain-Bandwidth product of low voltage, low power CMOS amplifiers and for providing high quality low voltage CMOS OTA integrators.

1. Introduction:

The feedforward ideas are directed at low voltage, low power fully differential CMOS folded cascode amplifiers. The limitation of the folded cascode amplifier for low voltage high frequency operation occurs due to the presence of a non-dominant pole at the source of the cascode device. Good phase margin is obtained by making the non-dominant pole position, P2, as large as possible. This is generally achieved by increasing the transconductance of the cascode device, M2 of Fig.1, by either increasing the width of the device or the current flowing through it. Increasing the width also increases Cgs2, (Cgs=W.L.Cox). Increasing the biasing current increases the power consumption. Furthermore, since the folded cascode structure is to be used with low supply voltages, too large an increase in the bias current can cause the transistor acting as a current source, M3, to move out of the strong inversion region of operation. We see that there is an upper limit for the value of the non-dominant pole which tends to be at lower frequencies when designing for lower supply voltages. The expressions for the poles and zero of the standard folded cascode configuration are given as follows:

$$p_1 = -\frac{1}{gm_2 . ro_2 . ro_1 . (C_L + Cgd_2 + Cdb_2)}$$

$$p_2 = -\frac{gm_2}{Cgs_2 + Cbs_2 + Cdb_1 + Cgd_1}$$

$$z_1 = +\frac{gm_1}{Cgd_1}$$

2. Folded Cascode Structure with Feedforward Connection:

A simple modification of feeding the input signal forward to the gate of the folded cascode is shown in Fig.2. This is possible for a folded cascode structure with lower supply voltages since the biasing voltage required at the gate of the cascode under this situation moves closer to the mid-supply level (i.e. towards the input signal level.). The operation of this amplifier can be described intuitively as follows: at low frequencies the operation is basically that of a folded cascode amplifier. As the frequency increases the parasitics at the cascode node short the signal to ground. However, since the signal is fed forward to the gate of the cascode device the operation of the amplifier at these higher frequencies is that of a single device.
Analysis of the structure of Fig.2 indicates that the dominant and non-dominant pole positions remain the same as those for the standard folded cascode configuration of Fig.1 but the expressions for the zeros can be given by:

$$z_1 = -\frac{gm_1}{Cbs_2 + Cdb_1 - Cgd_2}$$

$$z_2 = +\frac{gm_2 . (Cbs_2 + Cdb_1 - Cgd_2)}{(Cgs_2 + Cbs_2 + Cdb_1 + Cgd_1) . Cgd_2}$$

It can be seen that the high frequency right hand plane zero has moved to lower frequencies. However, the non-dominant pole can be designed to cancel with the left hand plane zero by equating their expressions. Potentially, exact cancellation can be achieved if the following expression is satisfied:

$$gm_2 = gm_1 . \frac{(Cgs_2 + Cbs_2 + Cdb_1 + Cgd_1)}{(Cbs_2 + Cdb_1 - Cgd_2)}$$

If extra grounded parasitic capacitance,Cp, is added to the cascode node, (source node of M_2 in Fig. 2), it is seen to be in parallel with Cdb_1 and Cbs_2. The dominant

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pole position remains the same but the non-dominant pole and zero positions can be given as follows:

$$p_2 = -\frac{gm_2}{Cp + Cgs_2 + Cbs_2 + Cdb_1 + Cgd_1}$$

$$z_1 = -\frac{gm_1}{Cp + Cbs_2 + Cdb_1 - Cgd_2}$$

$$z_2 = +\frac{gm_2.(Cp + Cbs_2 + Cdb_1 - Cgd_2)}{(Cp + Cgs_2 + Cbs_2 + Cdb_1 + Cgd_1).Cgd_2}$$

As long as Cp is greater than the transistor parasitic capacitances, i.e. Cp >>Cgs_2 (since in strong inversion Cgs is the largest device parasitic), the left hand plane zero moves back towards its original high frequency position:

$$z_2 = +\frac{gm_2}{Cgd_2}$$

The non-dominant pole and left hand plane zero have now moved to lower frequencies but exact cancellation can still be achieved by equating the two expressions.
The ability to exactly cancel the pole and the zero is important since the greater the separation between the pole and zero to cancel, the slower the settling component in the transient response [3], [4]. An expression for the slow settling component can be given as follows:

$$V_{slow\text{-}settling}(t) = V.\frac{2.\pi.(Z_1 - P_2)}{GBW}.\exp(2.\pi.Z_1.t)$$

As already mentioned, increasing the extra parasitic capacitance, Cp, reduces the frequency at which the doublet occurs. From the above expression this suggests a slower settling component. However, swamping device parasitics also allows the position of the non-dominant pole and zero to be more easily controlled which leads to more accurate pole zero cancellation (i.e. (Z_1-P_2) reduces). Therefore, the two effects counteract each other causing little deterioration in the overall settling time.
Addition of extra parasitic capacitance at the cascode node also acts to improve the PSRR since signals which pass from the supply rail through the channel of the current source are suppressed by this capacitance. However, the disadvantage of using this extra parasitic at the internal node is in the lowering of the slew rate since this capacitance needs to be charged and discharged resulting in a basic trade-off.
As well as improving the phase margin of the amplifier by providing cancellation of the non-dominant pole, this feedforward compensation technique results in an improvement in the open loop gain from ($gm_2.ro_2.gm_1.ro_1$+$gm_1.ro_1$) to ($gm_2.ro_2.gm_1.ro_1$+$gm_1.ro_1$+ $gm_2.ro_2$).
Since the dominant pole position is the same in both cases this means an improvement in the GBW product, or speed, of the amplifier and the expression can be given as follows:

$$GBW = \frac{gm_2.ro_2.gm_1.ro_1 + gm_1.ro_1 + gm_2.ro_2}{gm_2.ro_2.ro_1.(C_L + Cgd_2 + Cdb_2)}$$

In the standard configuration the load capacitance also acts as compensation, but with the feedforward connection, with or without the addition of the extra parasitic capacitance, the load capacitance can be removed entirely with the amplifier still remaining stable.

3. Folded Cascode Structure with Feedforward Capacitance:

A floating capacitor, Cf, can be used to feed an inverted input signal forward to the cascode node of the amplifier. The resulting structure indicated in Fig.3. is used to provide input pole cancellation which occurs due to source resistance at the input. However, analysing the structure in a similar manner to the previous amplifier structures assuming negligible source resistance indicates the occurrence of a left hand plane zero which again can be used to cancel the non-dominant pole. This configuration shows no high frequency right hand plane zero. This is due to the feedforward capacitance, Cf, compensating for the Cgd of the input device, M1. The expressions for the poles and zero are given as follows:

$$p_1 = -\frac{1}{gm_2.ro_2.ro_1.(C_L + Cgd_2 + Cdb_2)}$$

$$p_2 = -\frac{gm_2}{C_f + Cgs_2 + Cbs_2 + Cdb_1 + Cgd_1}$$

$$z_1 = -\frac{gm_1}{C_f - Cgd_1}$$

If exact pole-zero cancellation is achieved by equating the left hand plane zero with the non-dominant pole a true single pole response is achieved, i.e. a better integrator response. However, the open loop gain of this configuration remains the same as for the standard configuration and therefore also the gain bandwidth product since the dominant pole and bandwidth have not changed in value. Addition of the extra capacitance can reduce the slew rate.

4. Folded Cascode Structure with Combined Feedforward Compensation

A further configuration of Fig.4 can be introduced which includes both the feedforward techniques discussed. Analysis indicates that both the dominant and non-dominant poles remain the same as for the configuration with purely capacitive feedforward, i.e. Fig.3, but the zero positions are given as follows:

$$z_1 = -\frac{gm_1}{2.C_f + Cbs_2 + Cdb_1 - Cgd_2}$$

$$z_2 = +\frac{gm_2.(2.C_f + Cbs_2 + Cdb_1 - Cgd_2)}{(C_f + Cgs_2 + Cbs_2 + Cdb_1 + Cgd_1).Cgd_2}$$

The high frequency right hand plane zero does not disappear in this case, even with the feedforward capacitance compensating for Cgd1, since the feedforward connection to the gate of the cascode device, M2, brings into the equation Cgd2 which is not compensated for. However, if Cf>>Cgs2 this R.H.P. zero moves towards the value 2.gm2/Cgd2. Since the input signal is being fed forward the open loop gain and therefore also GBW are again larger when compared with the standard configuration.

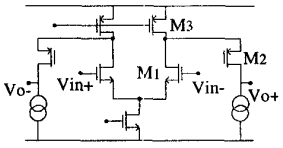


Fig.1

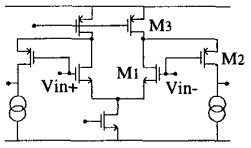


Fig.2

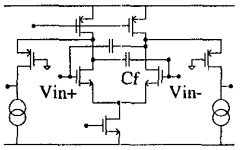


Fig.3

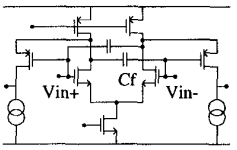


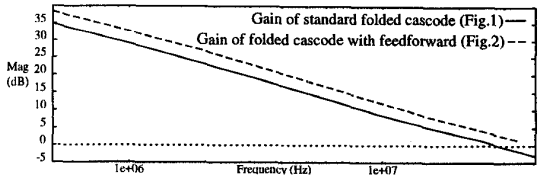
Fig.4

Fig.1 indicates the standard folded cascode configuration and Fig.2 the folded cascode with feedforward connection. Fig.3 shows the folded cascode with capacitive feedforward and Fig.4 indicates the folded cascode configuration with combined feedforward compensation.

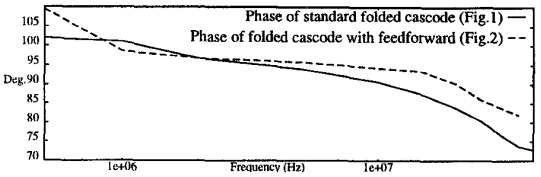
The sizes of the devices used for each of the configurations are the same: M1 being 120μ/1μ, M2 being 360μ/1μ and M3 being 600μ/1μ.

5. Testing and Results:

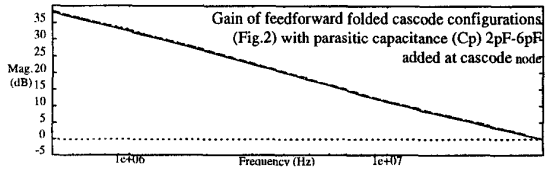
A test chip of the amplifiers of Figs.1 to 4 have been fabricated in a digital CMOS technology and a plot of the layout shown in Fig.5. The structures are fully differential and hence a BALUN transformer was used to provide a differential balanced input signal. The supply rails used were +/-1.25V with the power consumption of each structure being 3mW. Due to the chip packaging and test setup the load capacitance was estimated to be about 10pF.



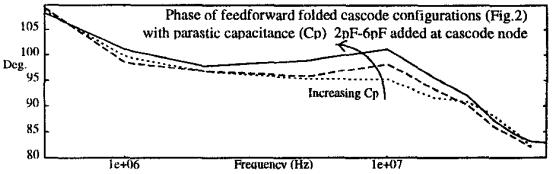
Plot 1a



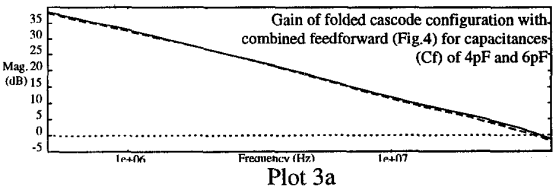
Plot 1b



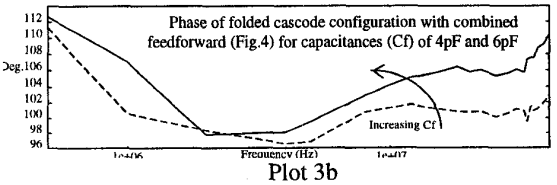
Plot 2a



Plot 2b



Plot 3a



Plot 3b

Plots 1a and 1b show an improvement in the phase margin from 76° to 83°, GBW product from 30MHz to 40MHz, and open loop gain at 500KHz from 35dB to 38dB as expected with the feedforward connection. Adding extra load capacitance (on top of the 10pF already present) to the feedforward structure of Fig.2 such the GBW reduces to 30MHz, a phase margin of

87° was measured. Plot 2b indicates how overcompensation can occur with the extra grounded capacitance added at the cascode node of the structure. Plots 3a and 3b indicate that the gain and phase response of the combined feedforward compensation and in this case overcompensation occurs due to the fact that the cascode node of M2 is brought out to a pin for testing purposes and consequently already has approximately an 8pF grounded parasitic loading. Table 1 indicates some of the slew rate data obtained by measurement. It is clear that whichever feedforward configuration is used, slewing is always improved when compared with the standard folded cascode configuration.

6.Conclusion:

The paper has presented analysis and measurements for various feedforward configurations for use in low voltage, low power folded cascode amplifiers. Their improvements over the standard configuration have been indicated. The feedforward techniques demonstrated are intended for use in on-chip low voltage folded cascode OTAs and as a consequence are not likely to be driving capacitive loads as high as 10pF. This suggests that their range of operation can extend to much higher frequencies and with the use of the feedforward compensation techniques the phase margin will remain high, above 80°. This could not be achieved with the standard configuration which relies on a certain loading capacitance to keep it stable. It is clear that the improvements to the standard folded cascode configuration have been achieved with no increase in power consumption or chip area.

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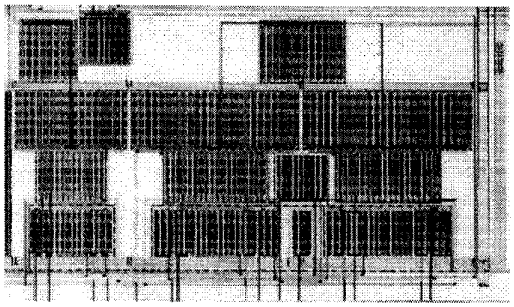

Fig.5 Layout plot of the amplfiier configurations

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Configuration	Capacitance (pF)	Positive Slew (V/μs)	Negative Slew(V/μs)
Standard folded cascode (Fig.1)	-	10.632	10.696
Feedforward connection (Fig.2)	Cp=0pF	16.440	13.514
Feedforward connection (Fig.2)	Cp=2pF	18.627	13.986
Feedforward connection (Fig.2)	Cp=6pF	18.500	13.930
Combined feedforward (Fig.4)	Cf=2pF	17.514	13.044
Combined feedforward (Fig.4)	Cf=3pF	17.577	13.005

Table 1. Slew rate data for various amplifier configurations