A Novel Dynamic Current Boosting Technique for Enhancement of Settling Time and Elimination of Slewing of CMOS Amplifiers

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Abstract— **A very simple technique to achieve low settling time is presented. It is based on the combination of class AB differential input stages, local common-mode feedback (LCMFB), and clamping circuit which provides additional current boosting, keeping the gain-bandwidth product (GBW) nearly constant. The slew enhancement is provided by an auxiliary circuit which is activated only during transients. The design is based on the "TSMC 180nm CMOS technology".**

I. Introduction

With the present trend towards the VLSI integration of analogue systems, there is a strong need for efficient output buffers which can drive large loads. This paper focuses on applications which present a need for the settling time to be low. Fast settling characteristics of MOS amplifiers are extremely important in the design of data conversion and switched-capacitor circuits [8][7]. In synchronous circuit operation, the amplifier output has to settle down to the final value in one clocking period. The slew-rate limited period and the small-signal settling period are the two distinct parts on which the settling response of a differential pair depends. Slewing of the circuit happens when all of the current flows though one branch of the circuit. This can happen when the differential input is a step or a pulse train [8]. Slew Rate is the maximum rate at which the capacitor charges linearly, which happens when the current flowing through the capacitance at the node reaches a maximum and becomes constant. Thus, the amplifier output voltage is changed at a rate equal to the ratio of bias current to the frequency compensation capacitor [8]. The techniques to enhance slew rate include dynamically biasing the circuit [1][3]. However, this method is bound to put the circuit under stress during transients. A more power efficient method to improve settling time is by boosting the rate of charging the output node during transients [6][5]. Since, the output is taken on a two-stage buffer; it becomes cardinal to include a nonsaturated input stage. The corresponding amplifier response will hence not be limited by the input stage behavior [3]. Here, we propose a circuit which will eliminate slewing by combining techniques efficiently, and improve the settling time also.

II. Basic System Architecture

Keeping in mind the necessary requirements of the output stage, a two stage buffer was chosen for implementing the slew rate enhancement circuitry, an output buffer stage with PMOS differential inputs. The two-stage buffer stage has diode connected NMOS as loads, which are used to bias the second stage NMOS. The second stage is a differential common source amplifier with single ended output. The structure was selected because of the simplicity of the design.

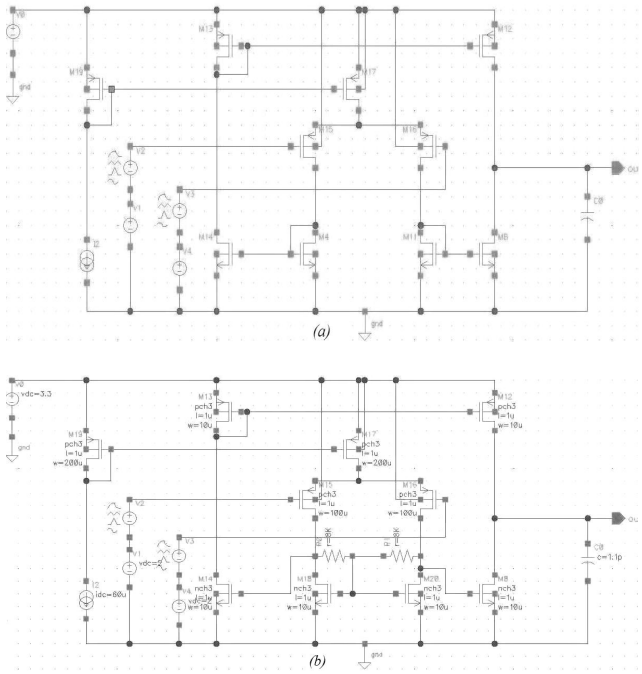

Fig.1 (a) Circuit Schematic diagram of Class A OTA. (b) Circuit Schematic diagram of OTA with LCMFB - Class AB

Low-voltage and power-efficient operation, these OTAs should have a fast settling response, not limited by slew rate [9]. Conciliating all these requirements is difficult with conventional (class A) OTA topologies, since the bias current limits the maximum output current. It is observed that class AB amplifier has better slew rate than the normal class A for which a simple modification to the circuit has been suggested [4]. Fig.1 (a) shows the schematic of the topology employed for the op-amp.

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A. LCMFB

One drawback of the fully differential amplifiers is that a common mode feedback circuit must be added. This is needed to establish the common mode (average) voltage, Fig.1 (b). For quiescent operation, the drain currents of all transistors have equal values ($I_2/2$) while the current I_R in resistors R0, R1 is zero. The source-gate voltage of M18, M20 is the same as their drain-source voltage. For common mode signals these transistors perform as a low impedance (diode connected) load with value $R_{L,\ CM}=1\ /\ g_{m18,20}$ [4]. Upon application of a differential signal, the current I generates differential complementary voltage changes at nodes A and B. By proper choice of R0, R1 the maximum output current can be made essentially larger than the maximum current of a class A op-amp (I_2)

B. Clamping

The input stage consists of two complementary differential pairs (M2, M4, and M15, M16). Transistors M3 and M5 are used as level shifters between the two differential pairs. The input voltage applied to the lower differential pair is transmitted to the corresponding transistor of the upper differential pair Fig.2 (a).

In the circuit, the output of M15 is fed at the source of the diode connected M3-acting as a common gate input. M3 acts as the current mirror for M2 [3]. This arrangement makes sure that the voltage never falls below a certain minimum, in the process making sure that the settling time is improved.

C. Auxiliary circuit to boost current at output node

Fig.2 (b) shows the circuit schematic diagram of a simple OTA. The amplification function is provided by the transistors M15, M16, M18, M20, M8, M14, M13, M12, M19, M17. The slewing capability is provided by the transistors M4, M2, M9, M7. The differential pair M4 – M2 is used for detecting the occurrence of fast signal transitions. The load devices for M4 and M2 are p-channel constant current sources biased to carry a current I2 (for the sake of simplicity, these sources have been taken as ideal $I_{9,10}$ while simulating the circuit).

The tail current is set to 2I1 with a condition that I2<I1. However, there is no specific condition between the bias current and I1, I2. Hence, again for simplicity, while simulating, the biasing of M6 is same as that of M17. Under normal conditions, the input terminals M15 and M16 are virtually at the same potential and thus the transistors M4, and M2 are biased to carry a current of I1 each. The devices for the I2 current sources are made to operate in triode region causing the voltages at the drains of M4 and M2 to be pulled close to GND. This ensures that the transistors M9 and M7 are normally off [6].

D. Proposed Circuit with Enhanced Slew Rate

Fig.3 shows the schematic of proposed OTA. It uses a combination of clamping along with LCMFB technique in a novel way to eliminate slewing. The results are discussed and compared with published results achieve enhanced settling time and eliminating slewing of amplifier. Also, an extra differential auxiliary circuit is added to boost the current when required in both positive and negative slew direction without

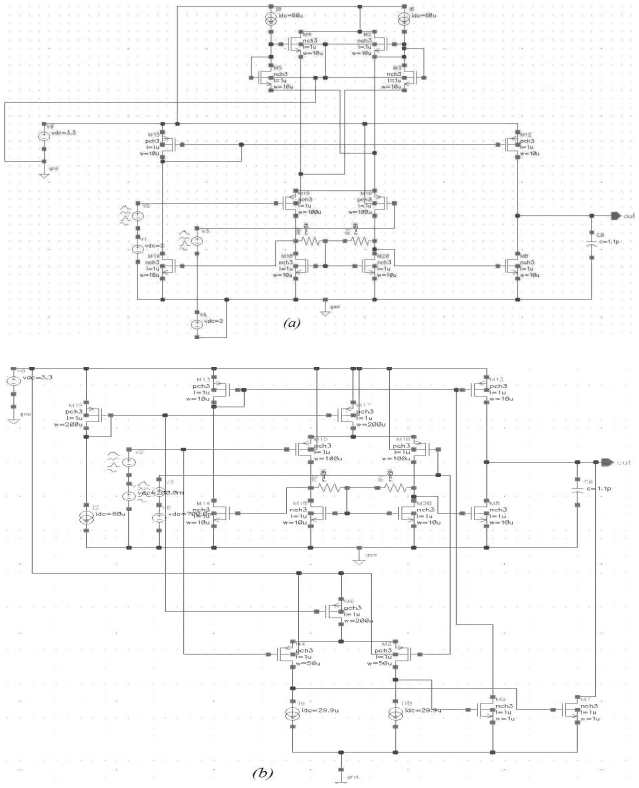

Fig.2 Circuit Schematic diagram of (a) OTA with Clamping & LCMFB. (b) OTA with Auxiliary Circuit & LCMFB.

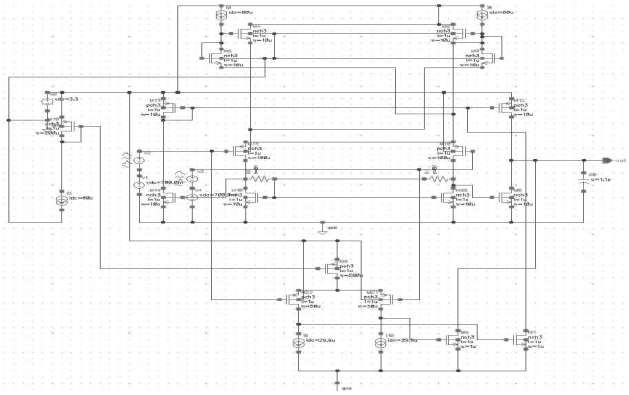

Fig.3 Circuit Schematic diagram of proposed OTA with circuits used to boost current at output node.

stressing the transistors of amplifier. The operation of these techniques is as mentioned previously. The challenge and importance lies in designing the amplifier with all the three techniques working properly. Care should be taken to keep transistors in ON state throughout the current boosting operation while nodes are taking large voltage excursions.

III. RESULTS AND SIMULATIONS

Table I shows the performance parameters of the op-amp along with various additional circuits. A graph between voltage and time is shown in Fig.4 (a) and slew rate in Fig.4(b). The constant region in first two graphs of fig. 4(b) indicates that circuit is slewing. As can be observed from Fig.4 (b), the slew rate improves from 50 to 650 V/µsec.

TABLE I
SUMMARY OF DESIGN RESULTS

PARAMETER	Class A OTA	OTA with LCMFB	OTA with Auxiliary Circuit & LCMFB	OTA with Clamping & LCMFB	OTA with Clamping & Auxiliary Circuit & LCMFB	UNITS
GAIN	52.38	60.14	60.14	61.05	61.05	dB
BANDWIDTH	130	130	127	260	265	kHz
SETTLING TIME	80	34	23	20	17	n sec

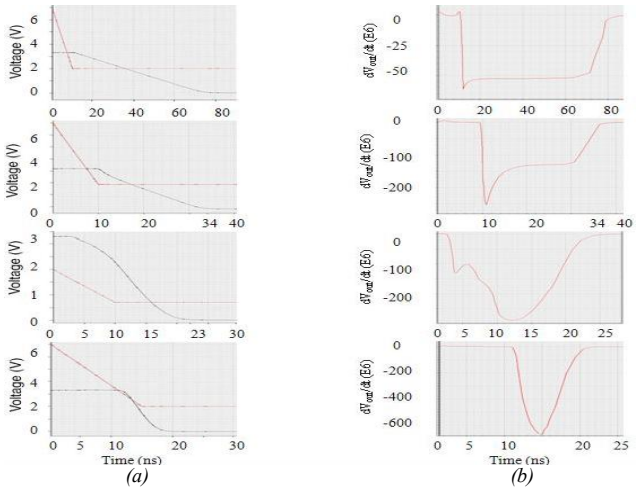

Fig.4 Transient response of the OTAs (a) Various OTA's studied. (b) Rate of change of output voltage level i.e. slew rate.

The proposed OTA is found to have very high bandwidth and low settling time in comparison to OTA with Auxiliary Circuit & LCMFB with no slewing at all.

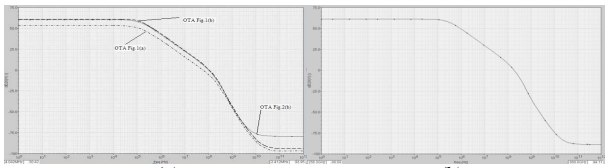

Fig.5 Measured Open Loop Frequency Response of (a) Various OTA's studied. (b) Proposed OTA from Fig.3.

The techniques have been successfully used to reduce settling time by about 80% as can be seen in Table I. The bandwidth shows improvement of more than 100%. The gain shows an improvement of almost 150%.

IV. CONCLUSION

A range of CMOS Class AB output buffers based on LCMFB have been proposed. The proposed circuit provides extremely small response times and hence very high slew rate. The use of clamping circuit has practically removed the slewing as can be seen from the furnished graphs. Hence it is suitable for efficient output buffers which can drive large loads.

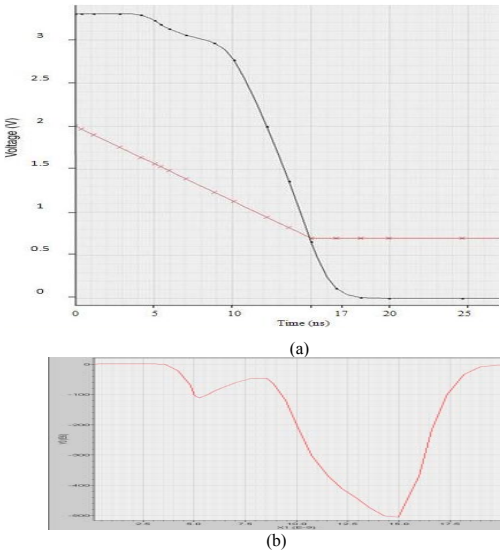

Fig.6 (a) Transient response of the proposed OTA.(b) Derivative of transient response of proposed OTA

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