Self-Biasing High Precision CMOS Current Subtractor for Current-Mode Circuits

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***Abstract*—In this study, a novel, differential pair based, high performance and high bandwidth current subtractor is proposed. Very low equivalent impedances are obtained at input ports *n* and *p* by using source follower transistors. Furthermore, the proposed circuit is self-biasing which makes it resistant to process, supply voltage and temperature variations. The proposed current subtractor can be used as an input stage for current-mode active circuits like current differencing buffered amplifier (CDBA), operational transresistance amplifier (OTRA) and current differencing transconductance amplifier (CDTA) which employ current subtractors. A numeric figure-of-merit is defined and it is used to demonstrate the superior performance of the proposed circuit.**

***Index Terms*—CDBA, CDTA, current subtractor, self-biasing, OTRA.**

I. INTRODUCTION

Current-mode circuits are providing their importance in the fields of analog signal processing and integrated circuit design [1-5]. Some of the performance features of current-mode circuits are high bandwidth, high linearity and wide dynamic range capability with low voltage operation and low power consumption [4]. In the literature, there are many current-mode circuits that serve solutions to a wider spectrum of problems [6-8]. Much research has been done over the last few decades to design high performance, low voltage, low power current-mode circuits [9-13]. These circuits need additional circuitries to bias the transistors and to keep them in saturation region. It is known that, using such biasing circuitries causes some disadvantages some of which are area and power consumption, additional pads that are exposed to noise and crosstalk [14-18].

Low input impedance is one of the critical design parameters of current-mode circuits; because the signal transformation efficiency is enhanced by the lower impedance values. In addition, decreasing the input impedance increases the bandwidth of the circuit because the product of the intrinsic capacitance and the input impedance forms a dominant pole. In order to have large bandwidth response, it is of great importance to derogate the input impedance values [19].

The current subtractor (CS) or, in other words, the differential current controlled current source (DCCCS), is one of the most important stages in some current-mode circuits like CDTA [6], CDBA [7] and OTRA [12]. These active elements can be implemented by cascading the CS and voltage (or current) buffer. In the literature, there are large numbers of CMOS implementations of these active elements that use biasing current or voltage sources [10, 12, 20-22]. For example the CDTA in [21] uses 2 and the CDBA in [22] uses 3 biasing sources and these circuits are exposed to the drawbacks that are mentioned above. In this paper, the CMOS implementation of high performance, differential pair-based and self-biasing CMOS CS is discussed. The proposed CS is completely self-biasing and it is free from afore mentioned drawbacks. By using the proposed self-biasing CS, it will be possible to implement the CMOS implementations of self-biasing CDBA, OTRA or CDTA. The circuit also has very low input impedances at input ports that allow the CS to operate in high frequencies.

The paper is structured as follows: the internal structure of the CS is discussed in Section 2. Simulation results are given in Section 3. In Section 4, a CMOS CDTA circuit is proposed as an application example that employs the proposed CS as the input stage. Finally, Section 5 concludes the paper.

II. THE PROPOSED CMOS CS

The equivalent model of a CS is given in Fig. 1. Z_n and Z_p denote the equivalent impedance values at ports n and p, respectively. Ideally they are equal to zero. Z_z denotes the equivalent output impedance and it is ideally infinite. α is the current transfer gain and ideally α=1.

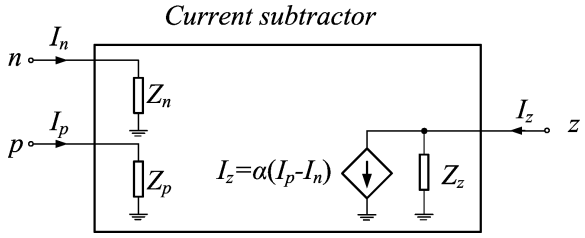

Figure 1. The equivalent circuit of a CS

The structure of the proposed CMOS CS is based on differential pairs and it is given in Fig. 2. The circuit operates as follows: transistors M9 and M10 act as DC current sources for differential pair transistors. The biasing current is formed by transistors M11_1 and M12_1. This biasing current is then copied to differential pairs by the current mirror transistors M13_1, M9 and M14_1, M10. Transistors M7, M8_1, M8_2 and M5, M6_1, M6_2 serve as active loads. The biasing current is also copied to p port by mirror transistors M13_1, M13_2 and M14_1, M14_2. Transistors M11_2, M12_2, M13_2, M14_2 and M15-M20 form a current subtracting circuit at the output port for the input currents I_n and I_p. M11_1, M12_1 at port n and

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M11_2, M12_2 at port *p* are connected in source follower configurations to minimize the input equivalent impedance which effectively transfers the input current into subtractor circuit. In order to demonstrate the performance parameters, the small signal equivalent circuits are given in Fig. 3 and Fig. 4 for the *n* and *p* ports, respectively.

The following equation defines the equivalent resistance seen on port *n* as:

$$R_n \cong \frac{1}{g_{m4\_2}g_{m11\_1}r_{oA}} \left\| \frac{1}{g_{m3\_2}g_{m12\_1}r_{oB}} \right. \quad (1)$$

where g_m is the transconductance of a MOS transistor. r_{oA} and r_{oB} are the equivalent resistances seen at nodes A and B, respectively and they are equal to:

$$r_{oA} = r_{o4\_2} \left\| r_{o6\_2} \right. \quad (2)$$

$$r_{oB} = r_{o3\_2} \left\| r_{o8\_2} \right. \quad (3)$$

With the assumption that all the differential pair transistors have the same small signal parameters (equal r_o's), r_{oA} and r_{oB} can be simplified as:

$$r_{oA} \cong r_{oB} \cong r_o/2 \quad (4)$$

Then the equivalent resistance on port *n* can be approximated as [17]:

$$R_n \cong \frac{2}{g_{m4\_2}g_{m11\_1}r_o} \left\| \frac{2}{g_{m3\_2}g_{m12\_1}r_o} \right. \quad (5)$$

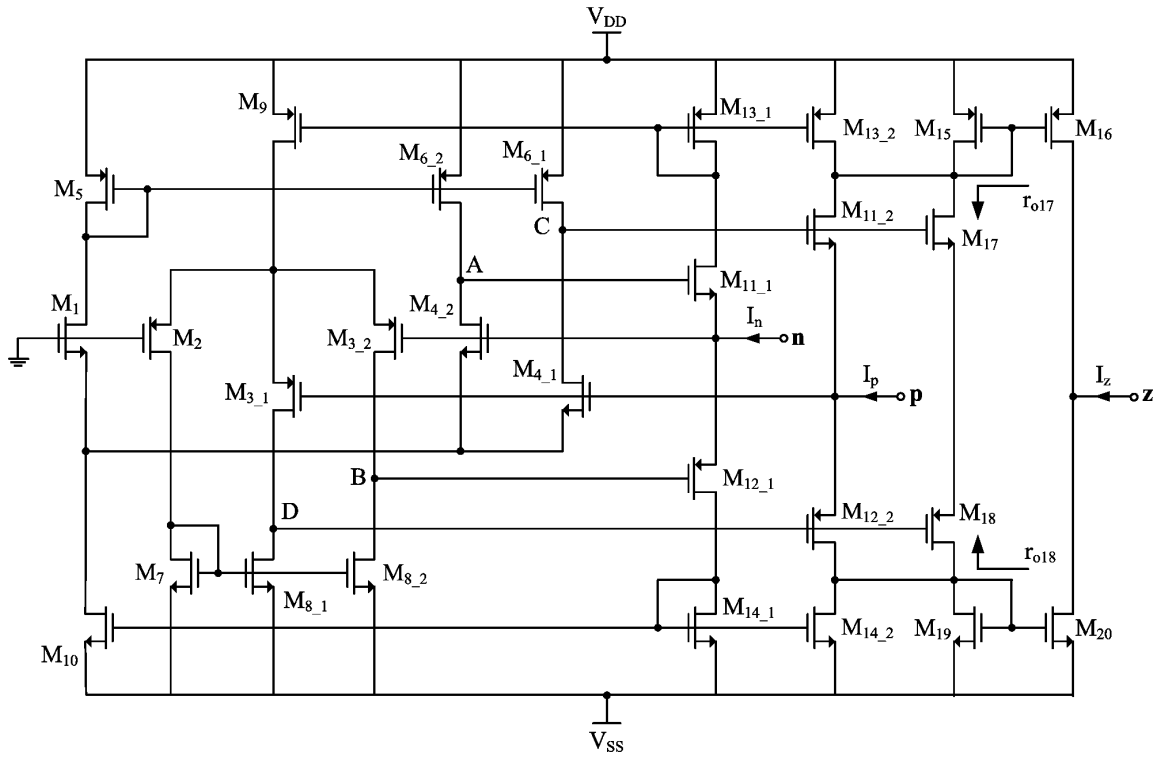

Figure 2. The proposed self-biasing CMOS CS

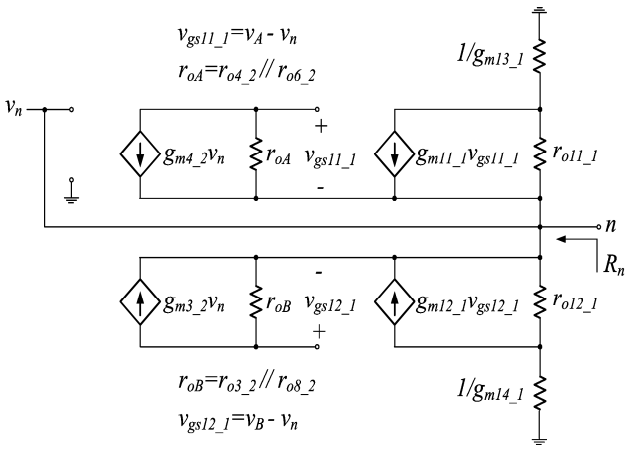

Figure 3. Small signal equivalent circuit for *n* port

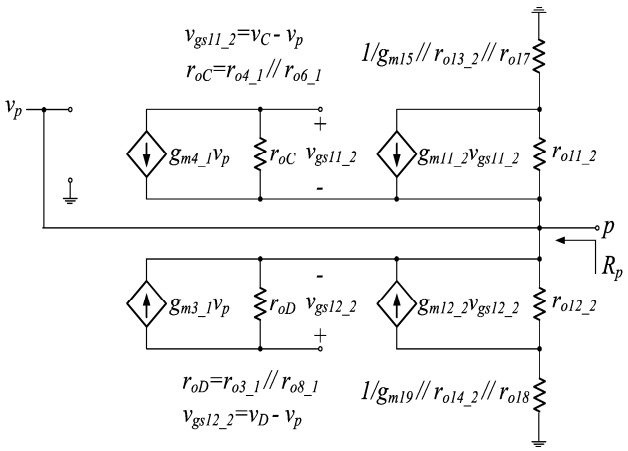

Figure 4. Small signal equivalent circuit for *p* port

Similarly, the equivalent resistance seen on port p can be calculated as:

$$R_p \cong \frac{1}{g_{m4\_1} g_{m11\_2} r_{oC}} \left\| \frac{1}{g_{m3\_1} g_{m12\_2} r_{oD}} \right. \quad (6)$$

r_{oC} and r_{oD} are the equivalent resistances seen at nodes C and D, respectively and they are equal to:

$$r_{oC} = r_{o4\_1} \left\| r_{o6\_1} \right. \quad (7)$$

$$r_{oD} = r_{o3\_1} \left\| r_{o8\_1} \right. \quad (8)$$

If the differential pair transistors have equal r_o's, the equivalent resistance on port p can be approximated as:

$$R_p \cong \frac{2}{g_{m4\_1} g_{m11\_2} r_o} \left\| \frac{2}{g_{m3\_1} g_{m12\_2} r_o} \right. \quad (9)$$

The α parameter is defined as the ratio of output current to input differential current and it can be given as [19]:

$$\alpha \cong \frac{i_z}{i_p - i_n} \cong \frac{g_{m16,20}}{g_{m15,19}} \cong \frac{(W/L)_{16,20}}{(W/L)_{15,19}} \quad (10)$$

where W and L are the transistor width and length, respectively. It is equal to the transconductance ratios of the current mirror transistors, so it is very close to the ideal unitary value.

The equivalent resistance seen on output port is formed by the parallel connection of output resistances of M16 and M20 as:

$$R_z \cong \frac{r_{16} r_{20}}{r_{16} + r_{20}} \quad (11)$$

III. Simulation Results

The proposed current subtractor circuit is simulated with HSpice using AMS 0.35µm CMOS process parameters. The aspect ratios are given in Table I. The supply voltages are $V_{DD} = -V_{SS} = 1.65V$. No other biasing voltage or current sources are used during simulations.

TABLE I. ASPECT RATIOS OF THE TRANSISTORS

Transistor	W/L (µm/µm)
$M_{14\text{-}1}$, $M_{14\text{-}2}$, M_{19}, M_{20}	10/0.5
M_{10}	15/0.5
M_7, $M_{8\text{-}1}$, $M_{8\text{-}2}$, $M_{11\text{-}1}$, $M_{11\text{-}2}$, M_{17}	20/0.5
M_1, $M_{4\text{-}1}$, $M_{4\text{-}2}$, $M_{13\text{-}1}$, $M_{13\text{-}2}$, M_{15}, M_{16}	30/0.5
M_9	45/0.5
M_5, $M_{6\text{-}1}$, $M_{6\text{-}2}$, $M_{12\text{-}1}$, $M_{12\text{-}2}$, M_{18}	60/0.5
M_2, $M_{3\text{-}1}$, $M_{3\text{-}2}$	90/0.5

The simulation results of the equivalent impedance magnitudes on input ports are given in Fig. 5(a). Resistance values are obtained as 3.6Ω and 3.88Ω for n and p inputs, respectively. They are obtained theoretically using Eq. (5) and (9) as 3.9Ω and 4.3Ω for n and p inputs, respectively. It is important to note that none of the impedance values exceed 200Ω at frequencies below 100MHz. That enables the CS to operate accurately at high frequencies. The simulation result for the equivalent impedance magnitude on z port is given in Fig. 5(b). The resistance value is obtained as 127kΩ.

The AC transfer characteristic of the proposed circuit is illustrated in Fig. 6. The current transfer ratio, α, is found to be 0.997 with 450MHz current transfer bandwidth. The current flowing through differential pair transistors is about 22µA and the power consumption of the circuit is 1.02mW.

Transient analyses of the proposed CS are also performed. A 500kHz, triangular input current waveform with amplitude of 100µA peak-to-peak and a 250kHz, square input current waveform with the same amplitude are applied to n and p ports, respectively. Time domain signal waveforms are illustrated in Fig. 7. In Fig. 8, time domain simulation results are given for 1MHz sinusoidal input currents of 200µA peak-to-peak at p port and 150µA peak-to-peak at n port. The current flowing through z port is 200µA -150µA = 50µA peak-to-peak.

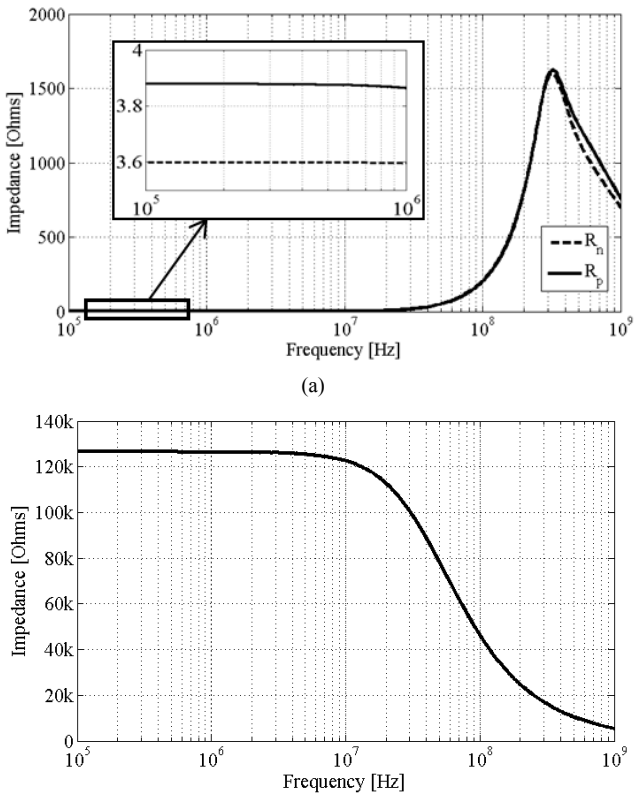

Figure 5. The impedance magnitudes at a) n and p ports and b) z port

In order to look at the effects of variations in process parameters like device geometry, threshold and supply voltages, Monte-Carlo simulations are performed. W (transistor width), L (transistor length), t_{ox} (oxide thickness) and V_{T0} (threshold voltage) parameters of each transistor are varied by using the values supplied by AMS. Simulation results are given in Fig. 9. Variations on the current gain are below 10% in Fig. 9(a). Monte-Carlo simulation for time

domain response is also performed. The maximum change in the offset current is about 7.5µA as given in Fig. 9(b).

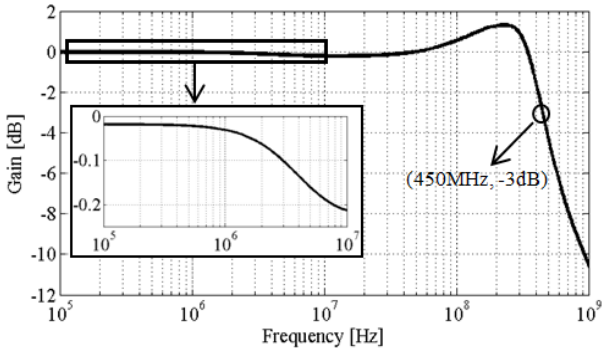

Figure 6. AC transfer characteristic

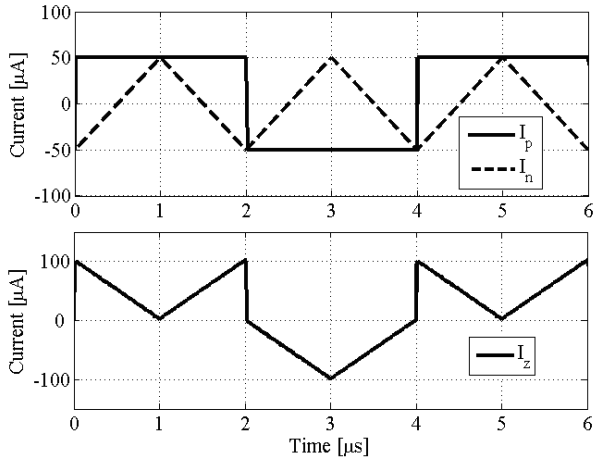

Figure 7. Time-domain simulation results for triangular wave input current at *n* port and square wave input current at *p* port.

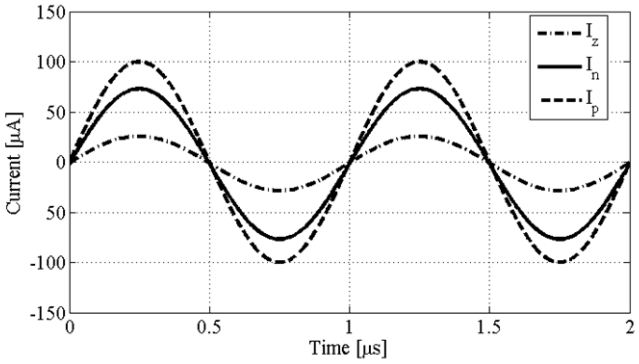

Figure 8. Time-domain simulation results for sinusoidal input currents at *n* and *p* ports.

In order to determine the total harmonic distortion (THD) of the proposed circuit, Fourier analysis is also performed as part of the transient analysis. In Fig. 10, THD is determined by applying 50MHz sinusoidal current input signals with various amplitudes. THD is found less than 10% for the input currents below 250µA. In the case given in Fig. 11, the input current difference is set to a constant value, I_p-I_n=100µA and the input signal frequency is increased. It is shown that THD remains below 10% for the signal frequencies up to 140MHz.

Fig. 12 gives the variation of differential pair current with supply voltages. ±3% variation in supply voltages changes the current from 15µA to 30µA.

The rise and fall times of the proposed CS is found to be 0.22ps and 0.16ps, respectively for 1MHz, 100µA peak-to-peak current input signal.

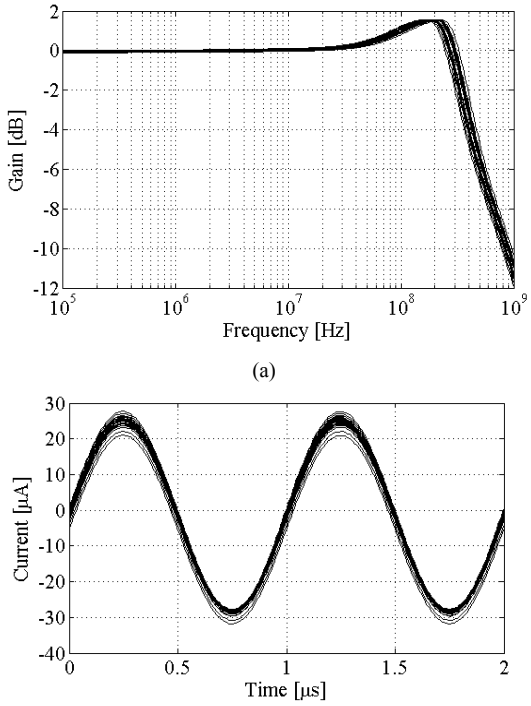

Figure 9. Monte-Carlo simulation results for a) frequency domain and b) time domain

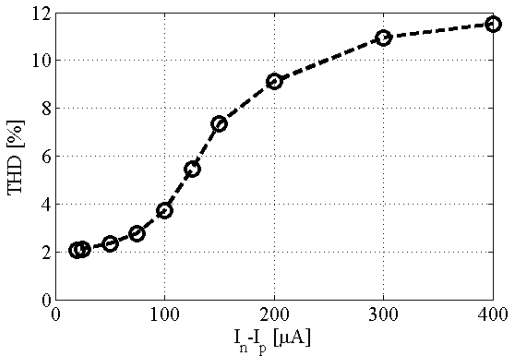

Figure 10. Total harmonic distortion for 50MHz current input

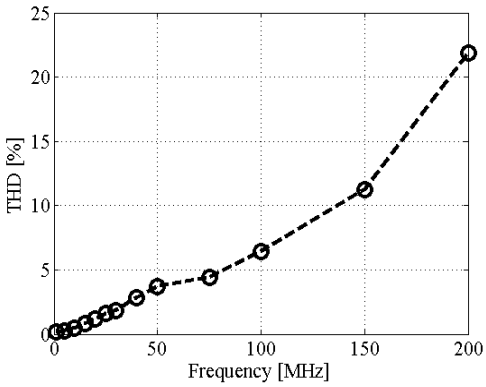

Figure 11. Total harmonic distortion for constant current inputs. (I_n-I_p=100µA)

A numeric figure-of-merit (FOM) is defined to provide a fair comparison with current subtractor stages of the

previously proposed CMOS CDTA, CDBA and OTRA circuits. The FOM equation is given as:

$$FOM = \frac{BW_\alpha \times R_z}{(k+1)\times R_n \times R_p} \tag{12}$$

where BW_α is the bandwidth in MHz, k represents the number of biasing sources, R_n, R_p and R_z are the equivalent resistances on input ports n, p and the z port, respectively. Higher values of FOM denote superior circuit performance. The comparison results are given in Table 2.

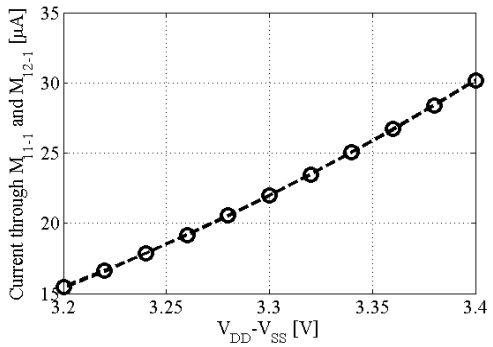

Figure 12. Variation of differential pair current with supply voltages

IV. Application Example

The proposed circuit can be used to realize CMOS implementations of CDTA, CDBA and OTRA which utilize current subtractors as the input stages. The ideal port equations of the CDTA [6], CDBA [7] and OTRA [12] can be given respectively as:

$$V_p=V_n=0,\ I_z=I_p-I_n,\ I_{x+}=g_mV_z,\ I_{x-}=-g_mV_z \tag{13}$$

$$V_p=V_n=0,\ I_z=I_p-I_n,\ V_w=V_z \tag{14}$$

$$V_p=V_n=0,\ V_w=R_m(I_p-I_n) \tag{15}$$

where g_m and R_m are the transconductance and transresistance gains of the CDTA and OTRA, respectively. As can be seen from Eq. (14) and (15), the only difference between a CDBA and an OTRA is the z-port. If the z port is left open and the voltage is taken from w-port with a gain, which is R_m, then an OTRA can be implemented from a CDBA.

A self-biasing, low voltage and low power implementation of the current output stage is given in Fig. 13 [23]. If the input of this buffer is connected to the z-port of the CS in Fig. 2, a self-biasing CMOS CDTA can be obtained. Similarly if the input of the self-biasing voltage output stage given in Fig. 14 [24] is connected to z-port of the CS, a self-biasing CDBA and/or OTRA implementation can be obtained.

The proposed CMOS CS and the current output stage given in Fig. 13 are used to form a CMOS CDTA. The aspect ratios for the current output stage are selected as 15μm/0.5μm for M_{o1}-M_{o4} and 5μm/0.5μm for M_{o5}-M_{o8}. 448MHz current transfer bandwidths are obtained both for x+ and x- ports.

TABLE II. PERFORMANCE COMPARISONS

Parameter	[20]	[21]	[22]	This work
Technology	MOSIS 0.5μ	TSMC 0.35μ	UMC 0.18μ	AMS 0.35μ
Supply voltage [V]	±1.25	±1.5	±0.6	±1.65
Current transfer bandwidth [MHz]	500	609	25	450
Port n resistance [Ω]	14	348	56.4	3.6
Port p resistance [Ω]	14	812	56.4	3.88
Port z resistance [kΩ]	290	1080	157	127
# of biasing sources, k	1	2	3	**none**
FOM [MHz/Ω]	$0.37\text{x}10^6$	$0.78\text{x}10^3$	$0.31\text{x}10^3$	**$4.09\text{x}10^6$**

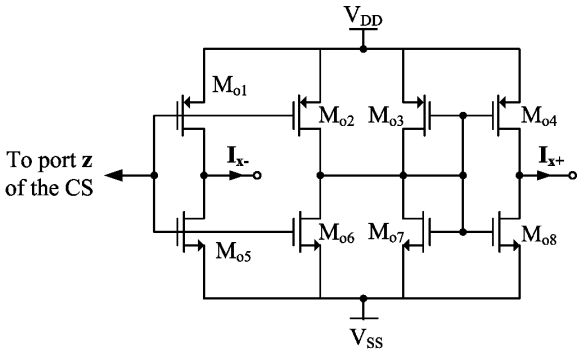

Figure 13. Current output stage to obtain self-biasing CMOS CDTA [23]

A current-mode second-order filter [25] that employs a single CDTA, a resistor and two grounded capacitors are selected to demonstrate the performance of the proposed circuit. The filter circuit is given in Fig. 15. Considering an ideal CDTA, the transfer functions of the filter responses are [25]:

$$\frac{I_{LP}}{I_{in}} = \frac{g_m}{RC_1C_2s^2 + sC_2 + g_m} \tag{16}$$

$$\frac{I_{HP}}{I_{in}} = \frac{RC_1C_2s^2}{RC_1C_2s^2 + sC_2 + g_m} \tag{17}$$

$$\frac{I_{BP}}{I_{in}} = \frac{sC_2}{RC_1C_2s^2 + sC_2 + g_m} \tag{18}$$

where g_m is the transconductance value of the CDTA as described in Eq. (13). During simulations, passive element values are selected as: R=1k, C_1=C_2=10p which determine the center frequency as 17MHz. Simulation results are given in Fig. 16.

V. Conclusion

In this paper, a precise CMOS current subtractor for current-mode circuits is proposed. The input impedance values are decreased by employing source follower stages. It is important to note that the proposed circuit employs no biasing voltage or current sources. To evaluate the performance of the proposed circuit, all the required parameters such as input impedance, output impedance, THD and Monte-Carlo analysis are analyzed over a wide frequency range. It is shown by simulations that the proposed current subtraction circuit can be applied to current-mode circuits. The simulation results also show that the proposed current subtractor circuit provides accurate and precise subtraction between two terminals with varied

currents. A self-biasing CMOS CDTA, which employs the proposed current subtractor, is also implemented.

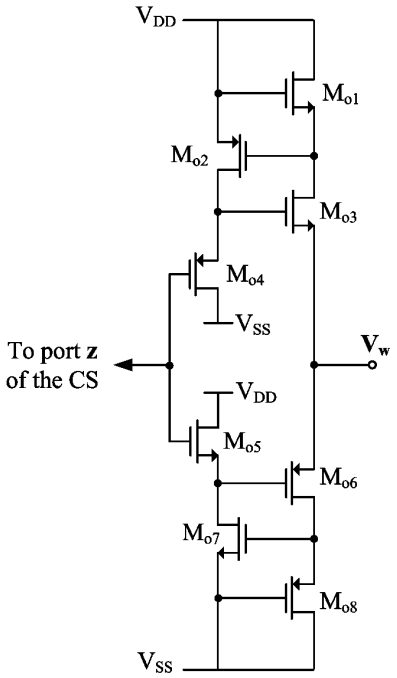

Figure 14. Voltage output stage to obtain self-biasing CMOS OTRA and/or CDBA [24]

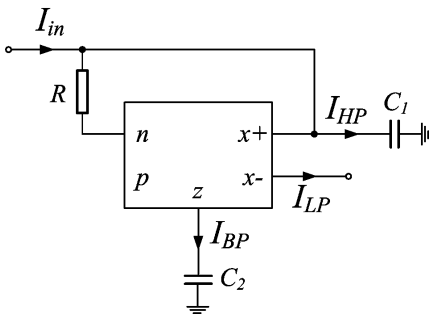

Figure 15. Current-mode second order filter proposed in [32]

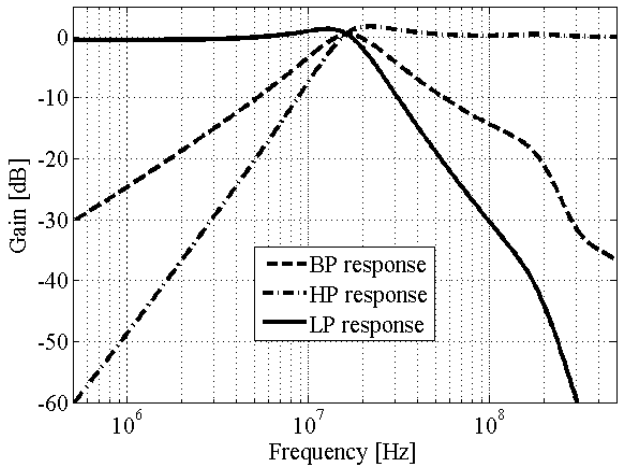

Figure 16. Simulation results of the filter circuit

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