FP 12.1: Toward Sub 1V Analog Integrated Circuits in Submicron Standard CMOS Technologies

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Lower channel lengths lead to lower supply voltages. For 0.25µm MOSTs the supply voltage is 2.5V. Even lower supply voltages will follow. This paper deals with analog integrated circuits that can handle the reduction of the supply voltage down to 1V. Existing solutions for such low supply voltages are: 1) reduction of threshold voltages from 0.7V to 0.3 - 0.4V, 2) use of voltage multipliers. It is possible to reduce supply voltages to 1V in standard CMOS without voltage multipliers. The advent of deep submicron CMOS dictates reduced supply voltage.

Reduced supply voltage forces current consumption to increase for several reasons: 1) For deep submicron transistors the square law relationship vanishes. The cross-over value of V_{GSsv} - V_T between the strong inversion region and the velocity saturation region at high current is approximated by [1]:

$$V_{GSsv} - V_T = 4nL\frac{v_{sat}}{\mu} \qquad (1)$$

For L = 0.25µm, this is about 2.5V. For smaller L, V_{GSsv}-V_T decreases further. The cross-over value of V_{GSws} - V_T between weak inversion and strong inversion is constant, about 80mV. The strong inversion region with the square-law relationship slowly decreases for smaller channel length and is expected to vanish altogether by year 2004 [2]. For the highest speed of MOST operation, this maximum value of V_{GSsv} - V_T. The corresponding value of transconductance per unit current,

$$\frac{g_m}{I_{DS}} = \frac{2}{V_{GSsv} - V_T} \qquad (2)$$

is low. Beyond V_{GSsv} - V_T increased current does not lead to an increase in transconductance. Smaller values of L lead to smaller supply voltages but not necessarily to corresponding lower power consumption.

2) Reduction of supply voltages reduces signal levels. For the same dynamic range, noise and or mismatch error must be decreased. Noise and mismatch error improve as the square root of increased area [3]. The spreading in V_T is described by

$$\sigma(\Delta V_T) = \frac{A_{VT}}{\sqrt{WL}} \qquad (3)$$

with A_{VT} slowly decreasing with L about 10mVµm for a nMOST with 0.5µm channel length. For the same dynamic range, larger areas are required, leading to larger capacitances and hence to higher current.

3) Dedicated low-voltage circuit techniques can be classified as: rail-to-rail input stages, pseudo-differential stages (without current source), and current differential schemes (using local feedback). All require additional circuitry for common-mode operation or bias current control. Higher current again results. Rail-to-rail input stages are required for buffers at low supply voltages. In these input stages, an nMOST and a pMOST differential pair are connected in parallel. To achieve a constant transconductance over the entire common-mode input range, special biasing is required. Figure 1 depicts biasing in which a current regulator loop keeps the sum of the currents through the nMOS and the pMOS differential pair constant. For transistors operating in weak inversion, this results in constant total transconductance over the common-mode input range.

A comparison of the existing biasing circuits shows that none of them reaches 1V (Table 1) [4]. A 1V (or less) power supply can be achieved only in technologies with reduced threshold voltages (0.3 to 0.4V). For input transistors operating in strong inversion, the minimum supply voltage is:

$$(V_{DD})_{min} = 2 \cdot V_{GS} + 2 \cdot V_{DSsat} \qquad (4)$$

This shows that it is necessary to operate the input transistors in weak-inversion for operation with supples below 1V.

An internal voltage multiplier can be used to bias the nMOS input pair at a voltage VDDx much higher than a VDD of 1V [11] (Figure 2). Pseudo-differential stages, used to increase input and output swings, consist of a common differential pair without current mirror. (Figure 3) [12]. Inputs must be preceded by a filter stage that limits the common-mode excursion. There are additional requirements such as high CMRR, low common-mode capacitive coupling, etc.

The best strategy for low-voltage analog systems is to combine circuit and system-level design techniques. An example is the switched opamp (SO) technique. It allows switched-capacitor operation at low supply voltage without voltage multipliers or low-V_T devices. The idea is to leave out switches at amplifier output s because those fail to operate when supply voltage is low. The dc or common-mode levels are explicitly set at V_{SS} at the opamp input and in the middle of the signal range at the opamp output. This avoids rail-to-rail input stages and allows maximal switch overdrive. The SO technique calls for dedicated low-voltage building blocks. At sub-1V supply, cascode transistors cannot be used in the output branch to increase gain because restricted swing would result. For high gain, two-stage amplifiers are required. Figure 4 shows a 1V two-stage amplifier designed for the SO technique [14]. The p-type input pair allows an input common-mode level of VSS. An operational amplifier for supply below 1V uses a current differential scheme based on the low-voltage I-I and V-I converters of Figure 5 [15]. They operate as follows. Transistor M1 is in a feedback loop and therefore does not conduct ac current. Input current is forced into transistor M2 and mirrored by transistor M3. dc voltages, indicated for 1V supply, illustrate low-voltage operation. The minimum supply voltage is

$$(V_{DD})_{min} = V_{GS} + V_{DSsat} \qquad (5)$$

Biasing the (input) transistors in the moderate inversion region allows supply down to 0.9 V.

The differential input voltage to current converter operates in a similar way (Figure 5b). Because of the feedback, no ac current can flow in transistor M1a. Its source is maintained at V_{in2}. V_{in1}-V_{in2} appears across the Gate-Source terminals of M1b. The ac current in M1b flows through M2 and is mirrored by M3. This current obeys the MOST square-law relationship and yields a class AB characteristic for larger input voltage V_{in1}-V_{in2}. Again dc voltages are indicated for 1V. Both inputs operate at about the supply V_{DD}. This input stage can be used as is in a single-ended SC integrator where special measures are taken to set the input dc level at V_{DD}. For this purpose, different reference levels must be introduced. This is done in the SC integrator shown in Figure 6. The signal is assumed to have a dc level of $V_{DD}/2$. It must then be sampled at that dc level. Capacitor Cs then samples only the ac signal. When integrating, Cs must be connected to the opamp onput reference level, V_{DD}. In a single-ended system, overall feedback establishes the dc drop of $V_{DD}/2$ over Cint, so dc at opamp output is $V_{DD}/2$ and rail-to-rail swing is established. Reduction of supply voltage of analog building blocks to 1V is feasible but does not always bring reduction in power consumption. More current is required to compensate for reduced gm. Additional circuits are required for input rail-to-rail operation and local voltage multipliers.

References: *See page 435.*

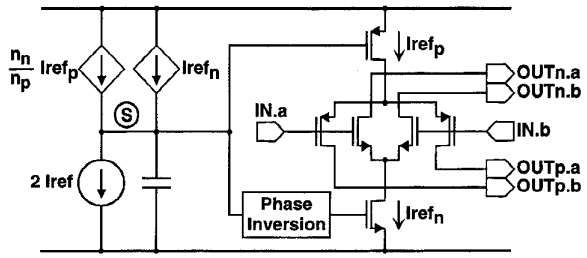


Figure 1: Rail-to-Rail input stage with current regulated biasing.

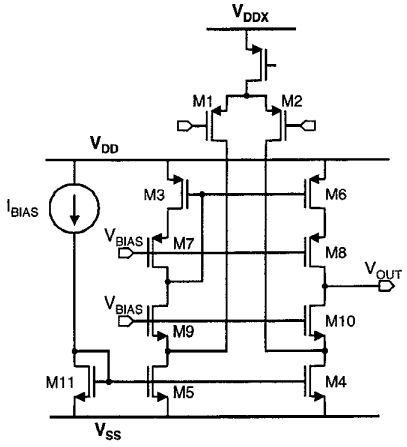


Figure 2: Input-pair biasing with internal voltage pump.

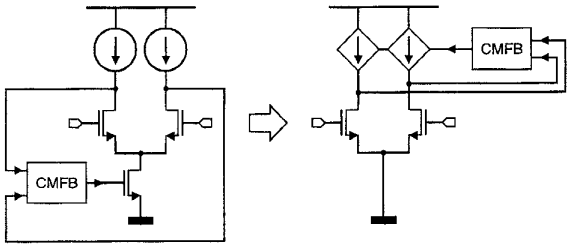


Figure 3: Pseudo differential stage.

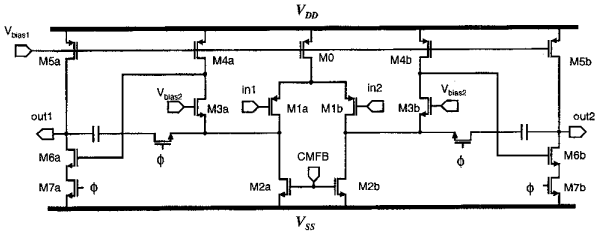
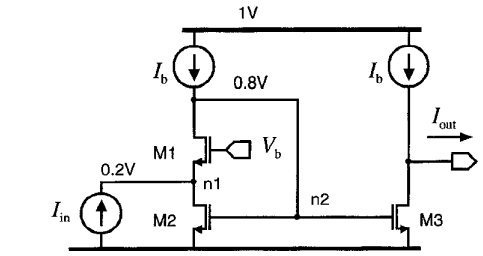


Figure 4: Two-stage 1V amplifier for differential switched opamp applications.



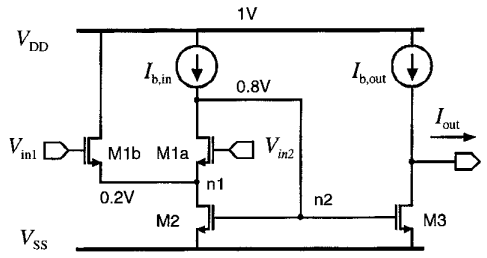


Figure 5a: Sub-1V I-I Converter.
Figure 5b: Sub-1V V-I Converter.

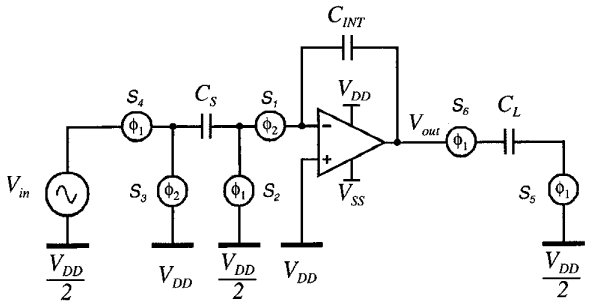


Figure 6: Sub-1V switched capacitor integrator.

	$\frac{\Delta g_m}{g_m}$ [%]	$\frac{GBW \cdot CL}{P_{tot}}$ [MHz·pF/mW]	P_{tot} [W]	V_{DD} Range [V]	Signal Swing	Die area [mm²]	Technology
Current regulator [4]	4%	210	300µ	1.5-3.3	RtR	0.25	0.7µm
MOS Translinear [5]	8%	4.2	2m	2.5	RtR		10µm
Regulating V_{DD} [7]	15%	56	460µ	1.3-3.3	RtR	1.3	0.7µm
I-switch/I-mirror [6]	8%	1.1	1.5m	3.3	RtR		10µm
3× I-mirror [8]	15%	110	550µ	3-6	RtR	0.04	
Improved CMRR [9]	9%	3	7.2m	5	RtR	0.7	2µm
Electronic zener [10]	6%	70	580µ	2.7-5.5	RtR	0.06	1µm

Table 1: Rail-to-rail topologies comparison.