A Very High-Frequency CMOS Complementary Folded Cascode Amplifier

Richard E. Vallee and Ezz I. El-Masry

Abstract— **A wide-band, fast settling CMOS complementary folded cascode (CFC) transconductance amplifier for use in analog VLSI high frequency signal processing applications is introduced. The superior performance of the CFC architecture over that of the folder cascode (FC) or mirrored cascode (MC) approaches for VLSI amplifiers is demonstrated. The symmetrically configured complementary input stage provides a wide common-mode input voltage range. The amplifier performs as an operational transconductance amplifier (OTA) and displays a first-order dominant pole when loaded by a shunt capacitor. The transconductance amplifier is small in area (0.016 mm^2), and well suited for high frequency analog signal processing applications. Simulation and experimental results demonstrate a dc gain of approximately 50 dB, witth a 0.1% settling response of under 10 ns for loads varied from 0 to 2 pF.**

I. Introduction

EXISTING CMOS technologies provide ample opportunity to integrate entire systems on to a single integrated circuit. To date, the ability to integrate large digital systems has far outweighed the ability to integrate analog systems. The greatest impediment to analog CMOS VLSI design has been the inability to provide consistent circuit performance over the broad range of requirements for signal gain, frequency response, phase response, delay, and signal fidelity imposed by analog designs. To date, numerous analog signal processing systems (continuous time and sampled data) have been integrated for signals of interest below the low megahertz range. There remains a long standing difficulty to integrate analog signal processing systems above this range. This is primarily due to the lack of high-frequency or high-speed amplifiers suitable for today's fine geometry CMOS processes.

This paper introduces a very fast CMOS transconductance amplifier that can be used for both continuous-time and sampled-data signal processing applications. In Section II, the complementary folded cascode amplifier (CFC) architecture is presented and compared with present design approaches. In Section III, simulation and fabricated test chip results are presented. The excellent settling characteristics and wide-band performance of the CFC amplifier demonstrate that it is the architecture of choice for implementing high frequency CMOS VLSI amplifiers.

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TABLE I
Simulation Results for Complementary Folded Cascode (CFC) Amplifiers

Technology	1.2-μm CMOS N-well process			
Supply voltage	$V_{dd} = +3.0$ V $V_{ss} = -3.0$ V			
Load capacitor	1.0 pF			
	Various Bias Currents			
Parameter	50 μA	100 μA	200 μA	300 μA
dc Power dissipation	2.7 mW	3.5 mW	5.0 mW	6.5 mW
Input offset voltage	−0.6 mV	1.2 mV	3.7 mV	5.5 mV
dc Gain	55 dB	55 dB	56 dB	57 dB
Unity gain bandwidth	126 MHz	126 MHz	178 MHz	200 MHz
Phase margin	71°	71°	63°	59°
Slew rate	85 V/μs	165 V/μs	265 V/μs	310 V/μs
Settling time (0.1%)	15.0 ns	10.1 ns	10.1 ns	12.0 ns

II. VLSI Amplifier Analysis and Design

The design specifications of a desirable CMOS VLSI amplifier include a very wide unity gain bandwidth (> 100 MHz), a fast settling time over a variety of low load capacitor values, suitability for fabrication in a short-channel digital CMOS process, capable of near rail-to-rail input and output voltage capability, dissipate nominal power, and occupy a small area.

Investigations into high speed, high frequency single-stage CMOS VLSI amplifiers have produced two general architectures [1]–[3]. These are the current mirroring or mirrored cascode (MC), and the current steering or folded cascode (FC) architectures. In order to truly evaluate these design techniques, circuits were taken from previously published work [4] and [5]. Due to the differences in technology, supply voltage, and power dissipation between the published amplifier results, it remained difficult to directly compare the performance of the two architectural approaches. In order to overcome this problem, both circuits were designed with PMOS input stages and simulated using CADENCE SPICE (cdsSpice), and process parameters for the Northern Telecom 1.2-μm N-well CMOS process. Care was exercised to ensure the designs employed similar transistor sizes with a W/L of generally 30, and given equivalent bias currents.

For the purposes of this analysis, the amplifier settling time has been chosen as the performance measure since it incorporates almost all the other desired performance criteria. The simulation results are shown in Fig. 1. For various load capacitors the MC architecture demonstrates a superior settling time for large capacitive loads due to its superior slew rate capability. For smaller capacitive loads, the FC approach provides the best settling time, due to its superior small signal

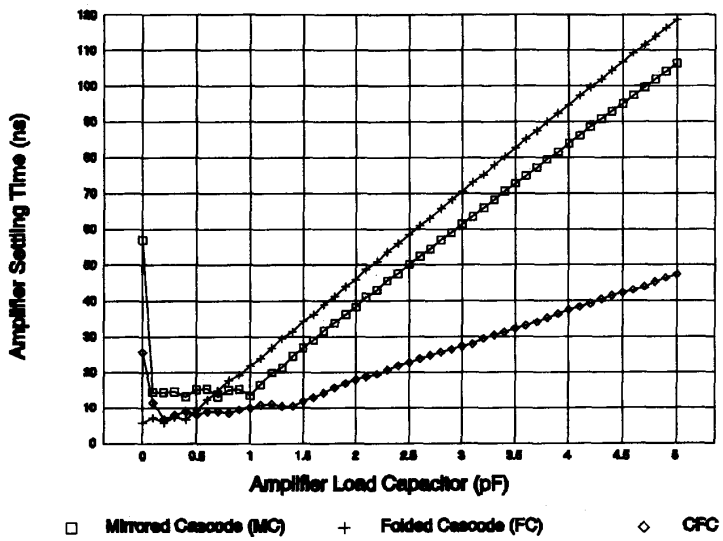

Fig. 1. Simulation settling times for the MC, FC, and CFC amplifiers.

ac response. Milkovic [4] recognized that the MC structure was limited to a minimum load capacitor for stable operation, and provided a minimum C_{Load} expression of the form,

$$C_{\text{Loadmin}} = M\left(\frac{g_{m1}}{g_{m2}}\right)(C_p + C_g). \tag{1}$$

A similar expression can also be derived for the FC structure and is of the form

$$C_{\text{Loadmin}} = \left(\frac{g_{m1}}{g_{m2}}\right)C_p. \tag{2}$$

The FC structure possesses a reduced current gain stage input capacitance, thus allowing it to be designed with a smaller minimum load capacitor limitation. It is thus capable of higher frequency operation than is the current mirrored approach for small capacitive loads. Based on this observation, a CMOS VLSI amplifier is desired, which can exhibit the fast settling ac response of the FC architecture for small capacitive loads, while providing a high slew rate for the fast settling of larger loads as depicted by the MC architecture. Such an amplifier would be well suited for on-chip VLSI analog signal processing applications in both the continuous-time and sampled-data domains.

By making use of the composite op-amp concept introduced by Mikhael and Michael [6], the complementary folded cascode (CFC) amplifier architecture was developed. The CFC amplifier is based on the FC architecture because of its excellent small-signal ac response and settling characteristics for very small capacitive loads. The CFC architecture is a modified current steering architecture that incorporates a class AB cascode stage. A schematic of the CFC architecture amplifier is shown in Fig. 2. The output current I_o for this amplifier is given by

$$I_o = (I_5 + I_2) - (I_6 + I_1) \tag{3}$$

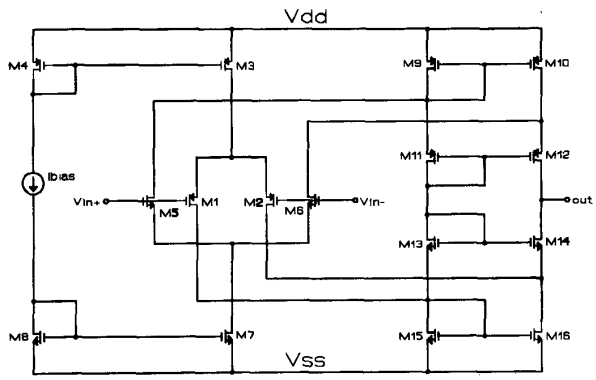

Fig. 2. Complementary folded cascode (CFC) amplifier schematic.

where the subscript represents the drain current (I_d) through the respective transistors. If the tail bias currents of the p-channel and n-channel differential pair are defined as $2I_b$, then the maximum output source current provided by the amplifier is $I_o = \pm 4I_b$. Simulation results for the CFC amplifier are provided in Table I.

Simulation results for the settling time performance of the CFC amplifier are shown in Fig. 1. Fig. 1 clearly demonstrates the superior performance of the CFC structure over that of the FC and MC structures. For loads of less than 1 pF, the settling times are only slightly better, but for loads of greater than 1 pF, the settling times improve significantly due to the superior slew rate performance of the CFC amplifier.

III. Results

A test chip was developed that contained several CFC amplifiers. The amplifiers were implemented in the Northern Telecom 1.2-μm N-well CMOS (CMOS4S) processes

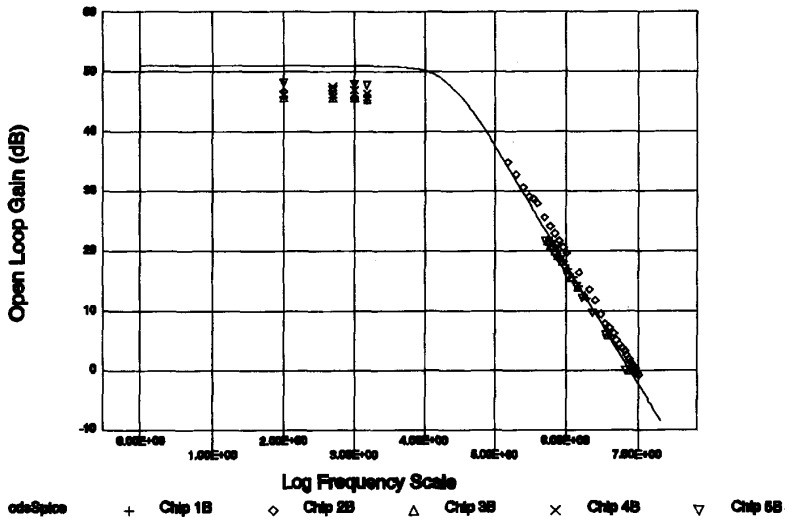

Fig. 3. Measured and simulation results of the ac open-loop frequency response of the complementary folded cascode amplifier. (C_{Load} = 20pF, V_{dd} = +3V, V_{ss} = −3V, R_{Load} = 1 MΩ, I_{Bias} = 100 μA.)

made available by the Canadian Microelectronics Corporation (CMC). The layout is compact in order to save area as well as to reduce any internal stray parasitic capacitances, and care was taken to ensure that transistor mismatches would be kept to a minimum. The total area occupied by the CFC amplifier is 0.016 mm^2(190 μm × 84 μm). The device was packaged in a 40 pin ceramic DIP and tested. The measured and simulation results for a 20 pF load capacitance and 1 MΩ load resistance are presented in Table II.

The measured results obtained from 5 test chips of the amplifier are in good agreement with the simulation results. The open loop response of the complementary folded cascode amplifier was measured and plotted with the simulation results obtained using cdsSpice. A C_{Load} = 20 pF, and an R_{Load} = 1 MΩ was used for the simulation results in order to reproduce the output conditions of the test chip. The data is presented in Fig. 3. The measured 5 dB loss in dc gain is due to ideal simulation conditions with 0 Ω source and drain resistance.

TABLE II
MEASURED AND SIMULATION RESULTS FOR COMPLEMENTARY F OLDED CASCODE AMPLIFIER

Technology	1.2 μm CMOS N-well process	
Supply voltage	V_{DD} = +3.0 V V_{SS} = −3.0 V	
Bias current	100 μA	
Load capacitor	20.0 pF	
Load resistance	1.0 MΩ	
Parameter	Measured	Simulation
dc Power dissipation	4.6 mW	3.5 mW
Input offset voltage	−2 mV	−0.3 mV
dc Gain	46 dB	51 dB
Unity gain bandwidth	9 MHz	8.0 MHz
Phase margin	90°	89°
Slew rate (rise, fall)	11.9 V/μs, 13.7 V/μs	12.0 V/μs, 12.4 V/μs
Settling time (0.1%)	175 ns	182 ns

IV. DISCUSSION AND CONCLUSION

The CFC amplifier presented in Fig. 2 was arrived at using one of the most efficient FC biasing schemes possible. Reviewing the generic FC amplifier structure, it is clear that it is possible to take a similar approach to derive a family of CFC amplifiers based on slightly different biasing arrangements. Besides alternate biasing configurations, the CFC architecture can be used to develop fully differential amplifiers [7] which provide improved noise performance for high frequency filter topologies. The CFC architecture can also be combined with other previously published design techniques to enhance such performance parameters as the dc gain and slew rate. Two techniques identified in the literature include the use of "regulated cascode" (RGC) transistors presented by Sackinger and Guggenbuhl [8] and Bult and Geelen [9] to provide "gain boosting," and the use of dynamic slew rates presented by Klinke *et al*. [10] to improve slew rate performance for large input voltages and load capacitances.

Comparing the results achieved with the CFC amplifier topology, to those for MC and FC circuits, it is clear that significant gains in performance can be made. The results presented suggest that the CFC architecture is the topology of choice for all high frequency CMOS VLSI amplifier implementations.

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