NVC-MDCS42A Datasheet

– Class2 Bluetooth V2.1+EDR

Innovative Communication in Wireless World

Version –V 2.3

Issue Date – .Oct 02, 2012

Description:

NVC-MDCS42A is a class 2 Bluetooth® 2.1+EDR (Enhanced Data Rates) module. It is a highly integrated and sophisticated module which contains all the necessary elements from radio to antenna and a fully implemented protocol stack. It is an idea solution for integrating Bluetooth® into various products with limited knowledge of Bluetooth® and RF technologies.

With NovaComm's iNova® bluetooth stack firmware, designers can easily customize their applications to support different Bluetooth profiles, such as SPP, HID, AG, HFP, DUN and etc.

And the module can also interface with Apple's Authentication Coprocessor and build an iAP over Bluetooth application. Please contact NovaComm for special firmware.

Typical Bluetooth applications:

- Cable replacement
- Bar code and RFID scanners
- Measurement and monitoring systems
- Industrial sensors and controls
- Medical devices
- Industrial PCs and laptops

Features:

- Bluetooth V2.1+EDR (class2)
- TX power +4dbm, / -84dBm RX sensitivity
- Onboard Meander line PCB antenna support 10 meters
- Support sniff and deep sleep mode
- Supports master and slave
- Supports Bluetooth profiles SPP, OPP, HID, iAP over Bluetooth
- UART and USB programming and data interfaces
- I2C Master interface
- Support Apple iAP protocol (with special firmware)
- PCM digital audio interfaces
- 8MBit onboard flash
- 25.80x13.40x2.2mm
- BQB/FCC/CE Certified
- RoHS compliant

Table 1: Ordering Information

Ordering Number	Package	Items in One Package	Comments
NVC-MDCS42A	Plastic tray	84 PCS	

Please also supply the customer firmware code issued by NovaComm Technologies when you place the order.

Release Record

Version	Release Date	Comments
2.1	Jan 25, 2012	Release
2.2	Sep 04 ,2012	Increase feature: RF power / RX sensitivity
2.3	Oct 02, 2012	Updates reference design. Fix several format and spell errors

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Pinout and Description

1.1. Pin Configuration

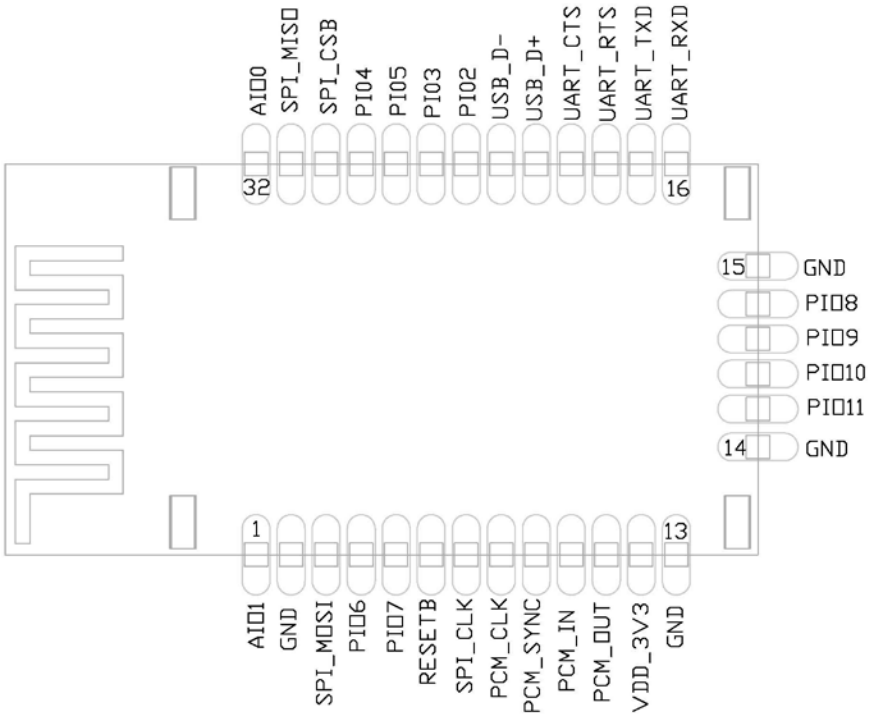

Figure 1: Pinout of NVC-MDCS42A(TOP View)

Pin	Symbol	I/O Type	Description
1	AIO1	Bi-directional	Programmable input/output line
2	GND	Ground	Ground
3	SPI_MOSI	CMOS input, with weak internal pull-down	Serial Peripheral Interface data input
4	PIO6	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
5	PIO7	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
6	RESETB	CMOS input with weak internal pull-up	Reset if low. Input denounced so must be low for >5ms to cause a reset
7	SPI_CLK	input with weak internal pull-down	Serial Peripheral Interface clock
8	PCM_CLK	Bi-directional with weak internal pull-down	Synchronous Data Clock
9	PCM_SYNC	Bi-directional with weak internal pull-down	Synchronous Data Sync
10	PCM_IN	CMOS Input, with weak internal pull-down	Synchronous Data Input
11	PCM_OUT	CMOS output, tristate, with	Synchronous Data Output

		weak internal pull-down	
12	VDD_3V3	3V3 power input	3V3 power input
13	GND	Ground	Ground
14	GND	Ground	Ground
15	PIO11	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
16	PIO10	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
17	PIO9	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
18	PIO8	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
19	GND	Ground	Ground
20	UART_RX	CMOS input with weak internal pull-down	UART data input
21	UART_TX	CMOS output, tristate, with weak internal pull-up	UART data output
22	UART_CTS	CMOS input with weak internal pull-down	UART clear to send active low
23	UART_RTS	CMOS output, tri-state, with weak internal pull-up	UART request to send active low
24	USB_D+	Bi-directional	USB data plus with selectable internal 1.5K pull-up resistor
25	USB_D-	Bi-directional	USB data minus
26	PIO2	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
27	PIO3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
28	PIO5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
29	PIO4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
30	SPI_CSB	CMOS input with weak internal pull-up	Chip select for Synchronous Serial Interface active low
31	SPI_MISO	CMOS output, tri-state, with weak internal pull-down	Serial Peripheral Interface data output
32	AIO0	Bi-directional	Programmable input/output line

Table 2: Pin Definition

2. Electrical Characteristic

2.1. Absolute Maximum Rating

Rating	Min	Max	Unit
Storage Temperature	-40	+120	°C
PIO/AIO Voltage	-0.4	+3.7	V
VDD Voltage	-0.4	+3.7	V
Other Terminal Voltages except RF	-0.4	VDD+0.4	V

Table 3: Absolute Maximum Rating Recommended Operating Conditions

2.2. Recommend operation conditions

Operating Condition	Min	Typical	Max	Unit
Storage Temperature	-40	--	+85	°C
Operating Temperature Range	-20	--	+70	°C
VDD Voltage	+2.7	+3.3	+3.7	V

Table 4: Recommended Operating Conditions

2.3. Power consumptions

Operating Condition	Min	Typical	Max	Unit
Radio On*(Discovery)		23		mA
Radio On*(Inquiry window time)		35		mA
Connected (Deep sleep disable, sniff enable)	1.4	3	11	mA
Connected (Deep sleep enable, sniff enable)	0.04	2.4	11	mA
Connected with data transfer	3	10	15	mA

Table 5: Power consumptions

Note :

Power consumption depends on the firmware used. Typical values are shown in the table.

Sniff mode ----- In Sniff mode, the duty cycle of the slave's activity in the piconet may be reduced. If a slave is in active mode on an ACL logical transport, it shall listen in every ACL slot to the master traffic, unless that link is being treated as a scatter net link or is absent due to hold mode. With sniff mode, the time slots when a slave is listening are reduced, so the master shall only transmit to a slave in specified time slots. The sniff anchor points are spaced regularly with an interval of Tsniff.

2.4. Input/output Terminal Characteristics

2.4.1. Digital Terminals

Supply Voltage Levels	Min	Typical	Max	Unit
Input Voltage Levels				
V_{IL} input logic level low	-0.4	-	+0.8	V
V_{IH} input logic level high	0.7VDD	-	VDD+0.4	V
Output Voltage Levels				
V_{OL} output logic level low, I_{OL} = 4.0mA	-	-	0.2	V
V_{OH} output logic level high, I_{OH} = -4.0mA	VDD-0.2	-	-	V
Input and Tri-state Current				
Strong pull-up	-100	-40	-10	µA
Strong pull-down	10	40	100	µA
Weak pull-up	-5	-1.0	-0.2	µA
Weak pull-down	0.2	+1.0	5.0	µA
I/O pad leakage current	-1	0	+1	µA
C_I Input Capacitance	1.0	-	5.0	pF

Table 6: Digital Terminal

2.4.2. USB

USB Terminals	Min	Typical	Max	Unit
Input Threshold				
V_{IL} input logic level low	-	-	0.3VDD	V
V_{IH} input logic level high	0.7VDD	-	-	V
Input Leakage Current				
GND < VIN < VDD[(a)]	-1	1	5	µA
C_I Input capacitance	2.5	-	10.0	pF
Output Voltage Levels to Correctly Terminated USB Cable				
V_{OL} output logic level low	0.0	-	0.2	V
V_{OH} output logic level high	2.8	-	VDD	V

Table 7: USB Terminal

[(a)]Internal USB pull-up disable

3. Physical Interfaces

3.1. Power Supply

The module accepts a 3.3V DC power input.

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3.2. Reset

The module may be reset from several sources: RESETB pin, power-on reset, a UART break character or via software configured watchdog timer.

The RESETB pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESETB being active. It is recommended that RESETB be applied for a period greater than 5ms.

Pin Name / Group	Pin Status on Reset
PIOs	Input with weak pull-down
AIOs	Output, driving low
PCM_OUT	Tristated with weak pull-down
PCM_IN	Input with weak pull-down
PCM_SYNC	Input with weak pull-down
PCM_CLK	PD
UART_TX	Output tristated with weak pull-up
UART_RX	Input with weak pull-down
UART_RTS	Output tristaed with weak pull-up
UART_CTS	Input with weak pull-down
USB_DP	Input with weak pull-down
USB_DN	Input with weak pull-down
SPI_CSB	Input with weak pull-up
SPI_CLK	Input with weak pull-down
SPI_MOSI	Input with weak pull-down
SPI_MISO	Tristated with weak pull-down
RESETB	Input with weak pull-up

Table 8: Pin Status on Reset

3.3. Internal Antenna

The module integrates a Meander line PCB chip antenna so there's no need to use antenna on customer's PCB. Simply pay attention to leave enough clearance for the antenna as shown in Figure 17.

3.4. PIO

NVC-MDCS42A has a total of 10 digital programmable I/O terminals. They are powered from VDD (3.3V). Their functions depend on firmware running on the device. PIO lines can be configured through software to have either weak or strong pull-ups or pull-downs.

Note:

All PIO lines are configured as inputs with weak pull-downs at reset.

Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes.

3.5. AIO

NVC-MDCS42A has 2 analogue I/O terminals. Their functions depend on software. Typically ADC functions can be configured to battery voltage measurement. They can also be used as a digital PIO.

3.6. UART

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

The UART CTS and RTS signals can be used to implement RS232 hardware flow control where both are active low indicators.

Table 9: Possible UART Settings

Parameter		Possible Values
Baud Rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	3M baud (≤1%Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per Byte		8

3.7. I2C Master

PIO6, PIO7 and PIO8 can be used to form a master I^2C interface. The interface is formed using software to drive these lines. It is suited only to relatively slow functions such as driving a LCD, keyboard scanner or EEPROM. In the case, PIO lines need to be pulled up through 2.2KΩ resistors.

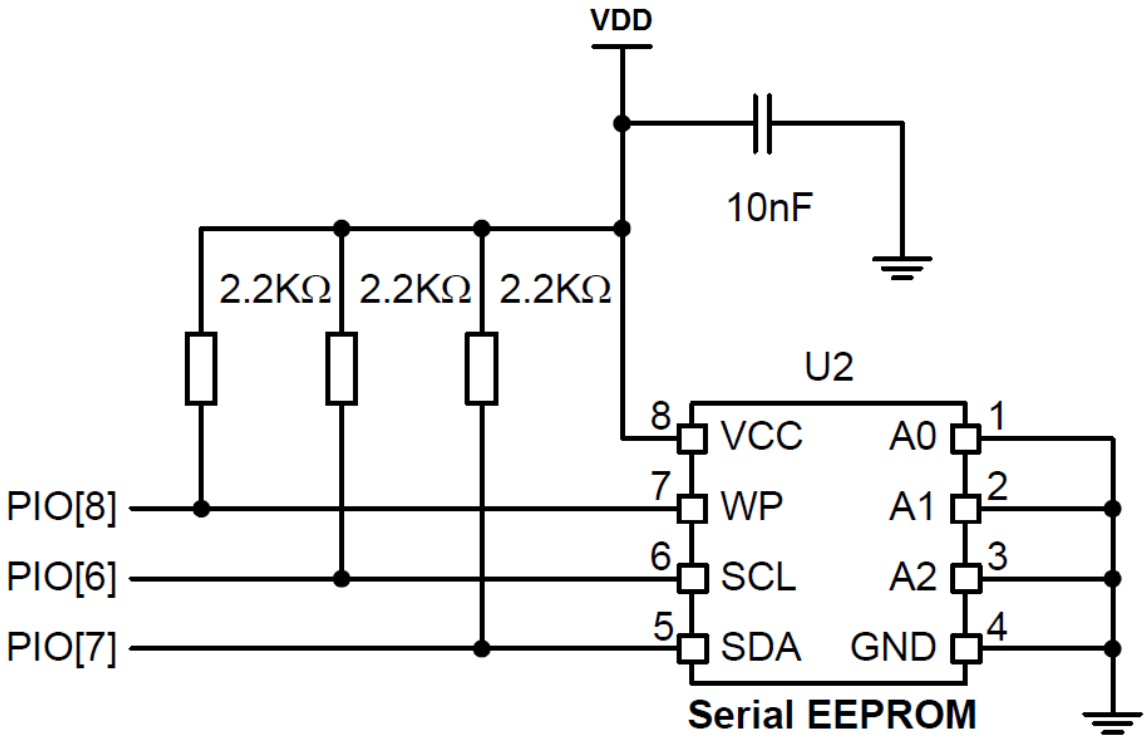

Figure 2 : Example EEPROM Connection with I²C Interface

3.8. SPI interface

The synchronous serial port interface (SPI) is used for flash/debug the module only. It can not be used for any user functionality. Please always design test points for this interface on the PCB in case that the module is needed to re-flash or flash-in-field in manufacture.

3.9. PCM interface

PCM is a standard method used to digitize audio (particularly voice) for transmission over digital communication channels. Through its PCM interface, the module has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for applications. The module offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on the module allows the data to be sent to and received from a SCO connection. Up to three SCO connections can be supported by the PCM interface at any one time.

The module can operate as the PCM interface master generating an output clock of 128, 256 or 512kHz. When configured as PCM interface slave, it can operate with an input

clock up to 2048kHz. The module is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13-bit or 16-bit linear, 8-bit μ-law or A-law companied sample formats at 8k samples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC.

The module interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channels A-law and μ-law CODEC
- Motorola MC145481 8-bit A-law and μ-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs
- The module is also compatible with the Motorola SSI™ interface.

3.9.1. PCM Interface Master/Slave

When PCM is configured as a master, the module generates PCM_CLK and PCM_SYNC.

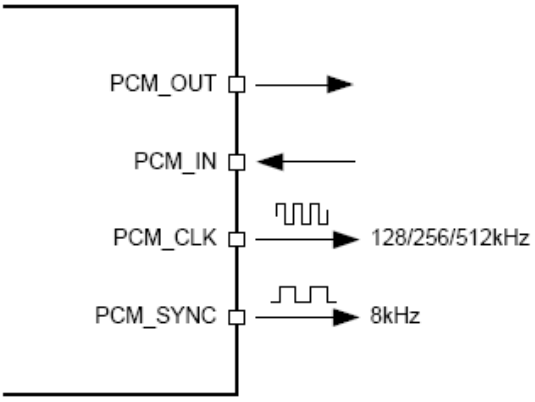

Figure 3: Configured PCM as a Master

When PCM is configured as the slave, the module accepts PCM_CLK rates up to 2048kHz.

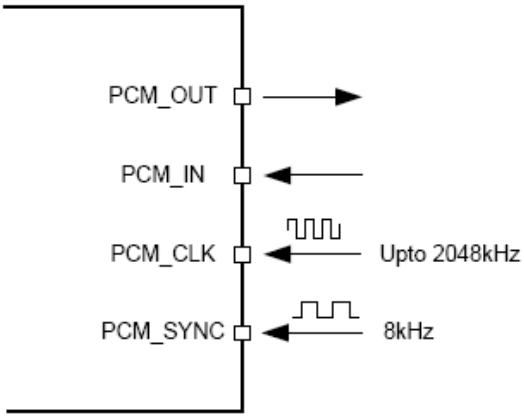

Figure 4: Configured PCM as a Slave

3.9.2. Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When the module is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When the module is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e., 62.5µs long.

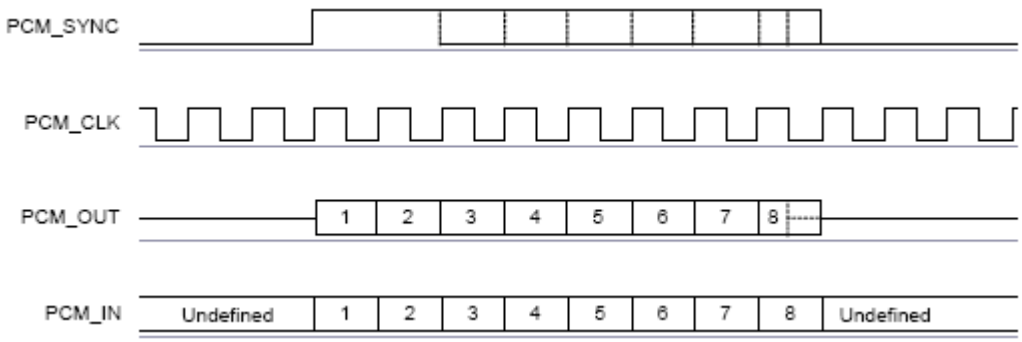

Figure 5: Long Frame Sync (Shown with 8-bit Companded Sample)

3.9.3. Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

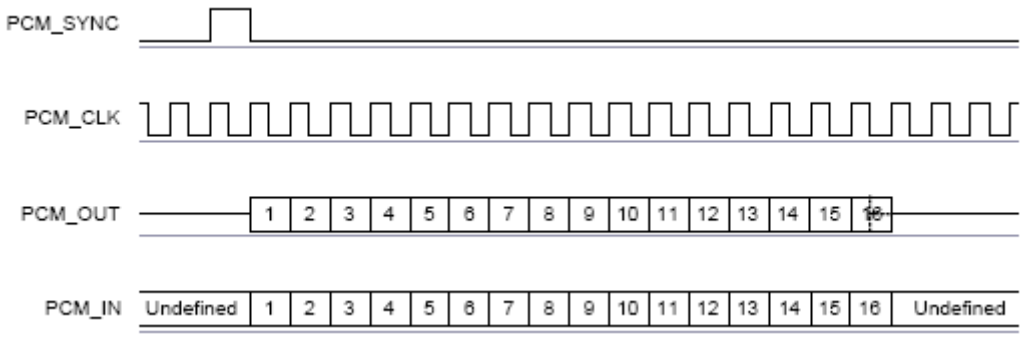

Figure 6: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, the module samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

3.9.4. Multi-slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

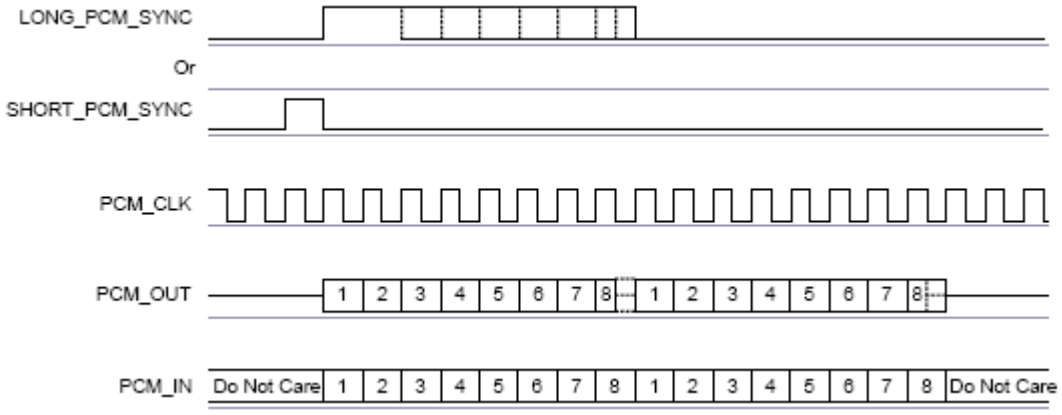

Figure 7: Multi-Slot Operation with Two Slots and 8-bit Companded Samples

3.9.5. GCI Interface

The module is compatible with the General Circuit Interface (GCI), a standard synchronous 2B+D ISDN timing interface. The two 64Kbps B channels can be accessed when this mode is configured.

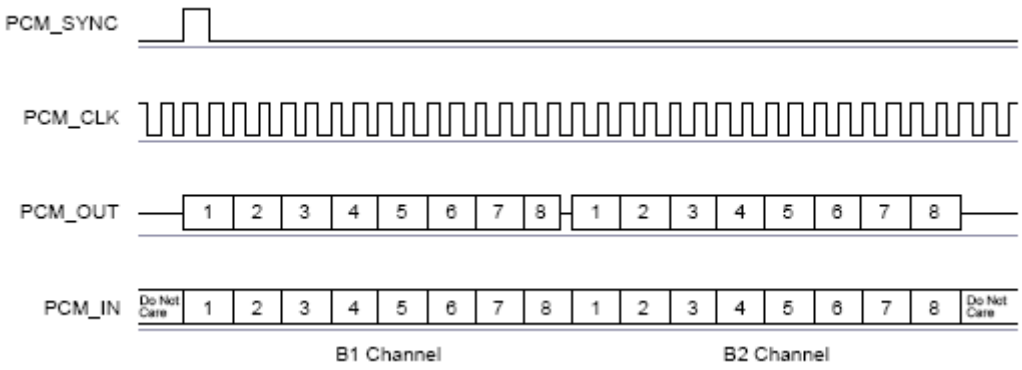

Figure 8: GCI Interface

The start of a frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With the module in slave mode, the frequency of PCM_CLK can be up to 4.096MHz.

3.9.6. Slots and Sample Formats

The module can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8-bit, 13-bit or 16-bit sample formats. The module supports 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats. The sample rate is 8k samples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

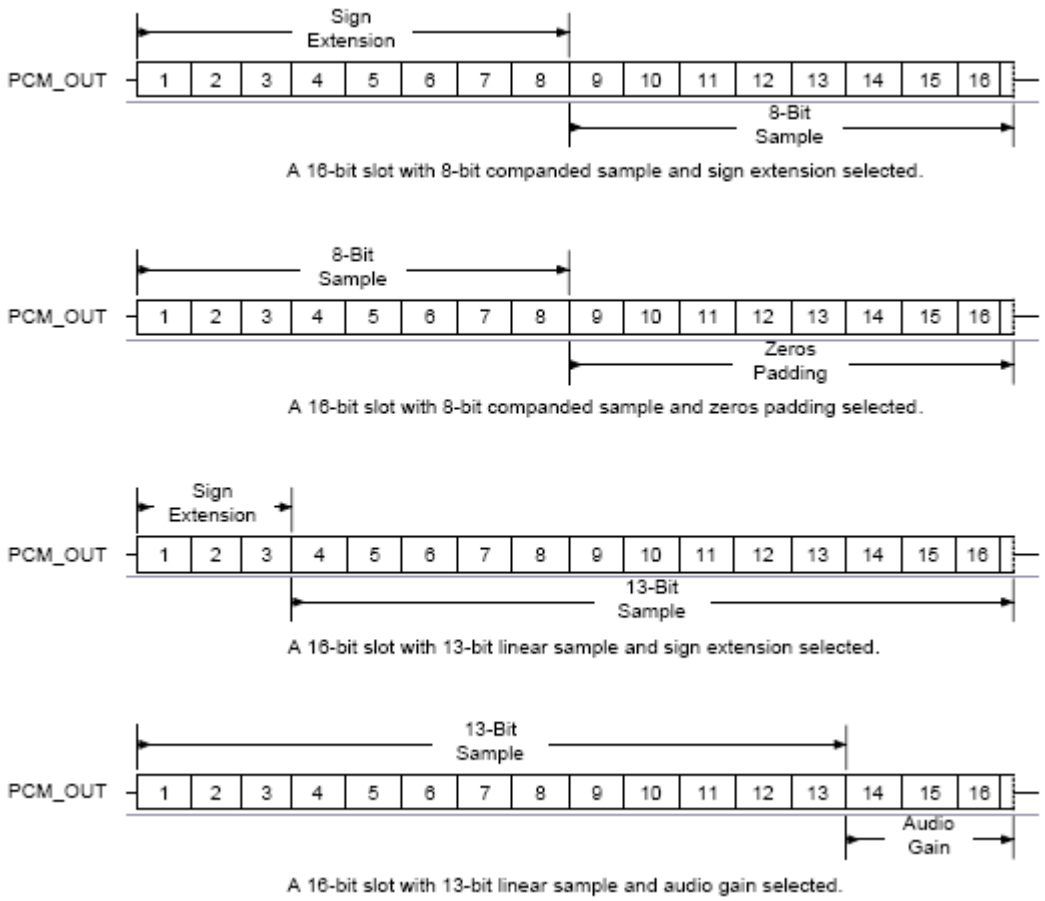

Figure 9: 16-Bit Slot Length and Sample Formats

3.9.7. Additional Features

The module has a mute facility that forces PCM_OUT to be 0. In master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECS use to control power down.

3.9.8. PCM Timing Information

Symbol	Parameter		Min	Typical	Max	Unit
f_{mclk}	PCL_CLK Frequency	4MHz DDS generation. Selection of frequency is programmable.	-	128 256 512	-	kHz

		48MHz DDS generation. Selection of frequency is programmable.	2.9		-	kHz
	PCM_SYNC frequency		8	-		kHz
t_{mclkh} (a)	PCM_CLK high	4MHz DDS generation	980	-	-	ns
t_{mclkl} (a)	PCM_CLK low	4MHz DDS generation	730	-		ns
	PCM_CLK jitter	48MHz DDS generation	-		21	ns pk-pk
$t_{dmclksynch}$	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
$t_{dmclkpout}$	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
$t_{dmclklsyncl}$	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
$t_{dmclkhsyncl}$	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
$t_{dmclklpoutz}$	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
$t_{dmclkhpoutz}$	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
$t_{supinclkl}$	Set-up time for PCM_IN valid to PCM_CLK low		30	-	-	ns
$t_{hpinclkl}$	Hold time for PCM_CLK low to PCM_IN invalid		10	-	-	ns

Table 10: PCM Master Timing

(a) Assumes normal system clock operation. Figures will vary during low power modes, when system clock speeds are reduced.

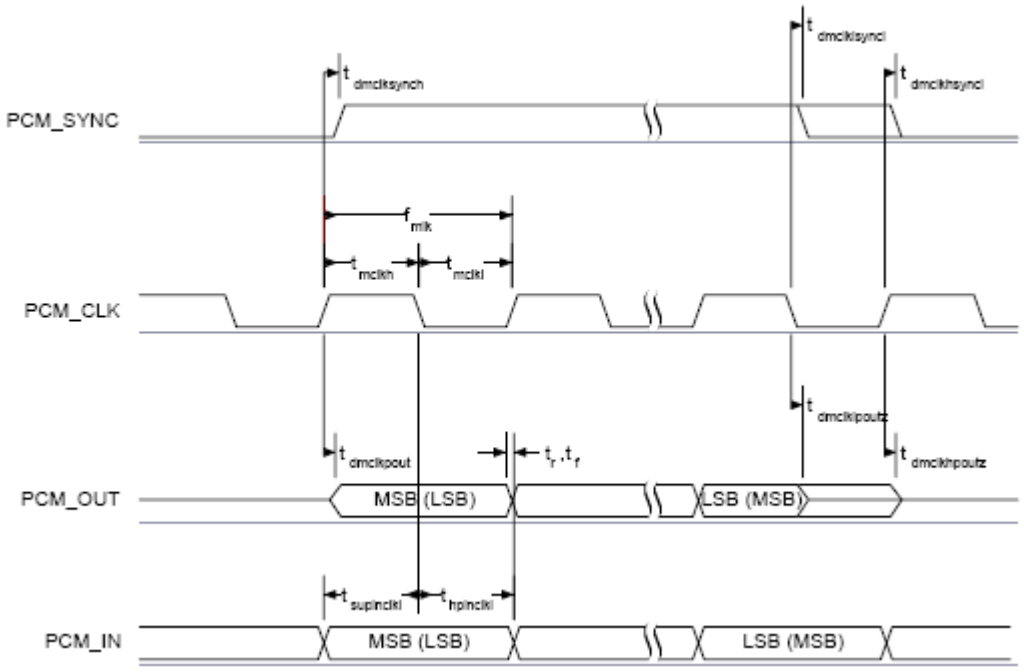

Figure 10: PCM Master Timing Long Frame Sync

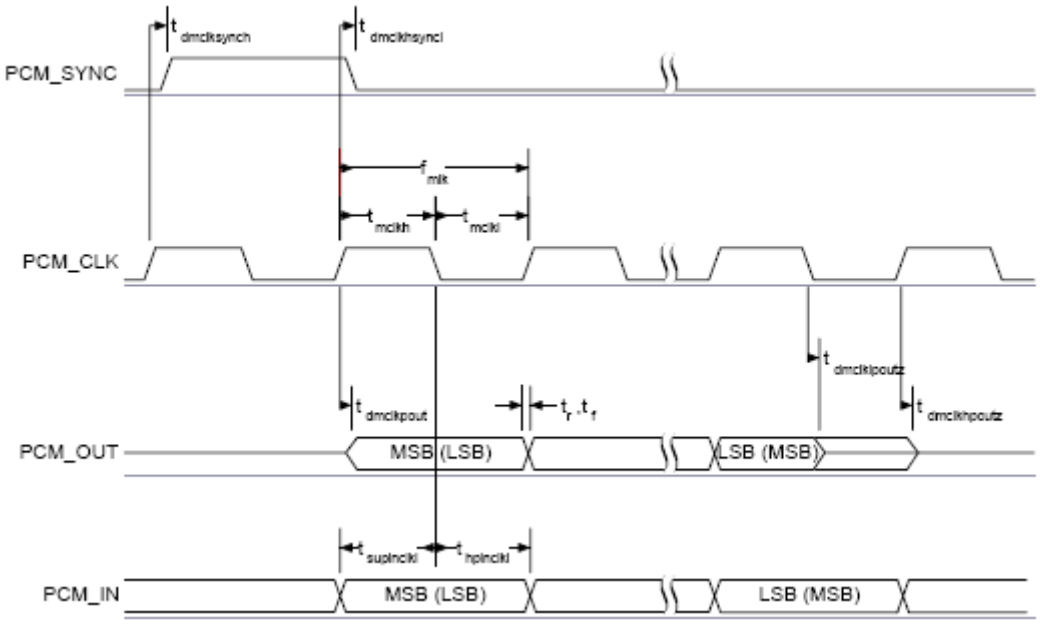

Figure 11: PCM Master Timing Short Frame Sync

Symbol	Parameter	Min	Typical	Max	Unit
fsclk	PCM clock frequency (Slave mode: input)	64	-	2048	kHz

fsclk	PCM clock frequency (GCI mode)	128	-	4096	kHz
tsclkl	PCM_CLK low time	200	-	-	ns
tsclkh	PCM_CLK high time	200	-	-	ns
thsclksynch	Hold time from PCM_CLK low to PCM_SYNC high	30	-	-	ns
tsusclksynch	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
tdpout	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
tdsclkhpout	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
tdpoutz	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
tsupinsclkl	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
thpinsclkl	Hold time for PCM_CLK low to PCM_IN invalid	30	-	-	ns

Table 11: PCM Slave Timing

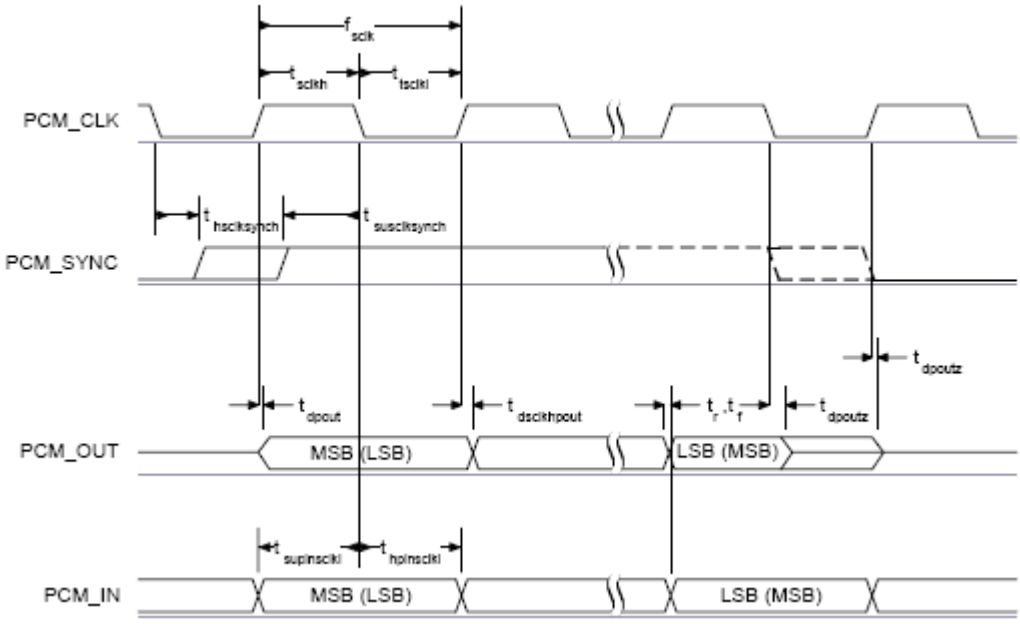

Figure 12: PCM Slave Timing Long Frame Sync

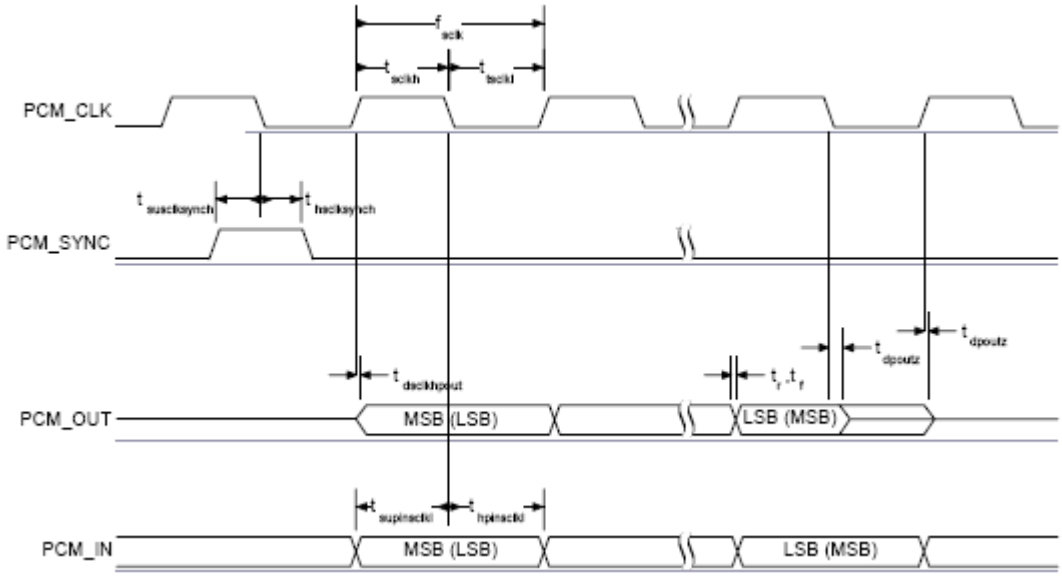

Figure 13: PCM Master Timing Short Frame Sync

3.10. USB

This is a full speed (12M bits/s) USB interface for communicating with other compatible digital devices. The module acts as a USB peripheral, responding to request from a master host controller, such as a PC.

The USB interface is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth specification v2.0+EDR or alternatively can appear as a set of endpoints appropriate to USB audio devices such as speakers.

The module has an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when module is ready to enumerate. It signals to the USB master that it is a full speed (12Mbit/s) USB device.

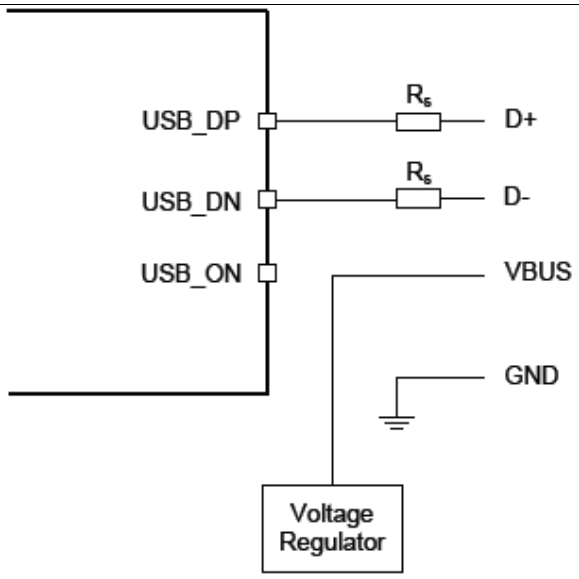

Figure 14: USB Connections

Identifier	Value	Function
R_S	27Ω Nominal	Impedance matching to USB cable

Table 12: USB Interface Component Values

Note:

USB_ON is only used when the firmware need an input to detect if USB is connected and the USB function shall be enabled. In such case it is shared with the module PIO terminals. If detection is not needed (firmware already runs with USB, such as USB DFU or USB CDC), USB_ON is not needed.

4. Software Stacks

NVC-MDCS42A is Bluetooth 2.1+EDR module, the embedded iNova Bluetooth Stack firmware supports the SPP, SDP, OPP, FAX, HID Profile, and supports up to seven devices simultaneously connected.

Furthermore, the Apple iAP (iPod Accessory Protocol) which is used to connect with iOS devices has also been implemented and included in iNova Bluetooth Stack firmware.

Contact with the sales agent for support for more profiles and applications with iNova Bluetooth stack firmware.

4.1. iNova Stack

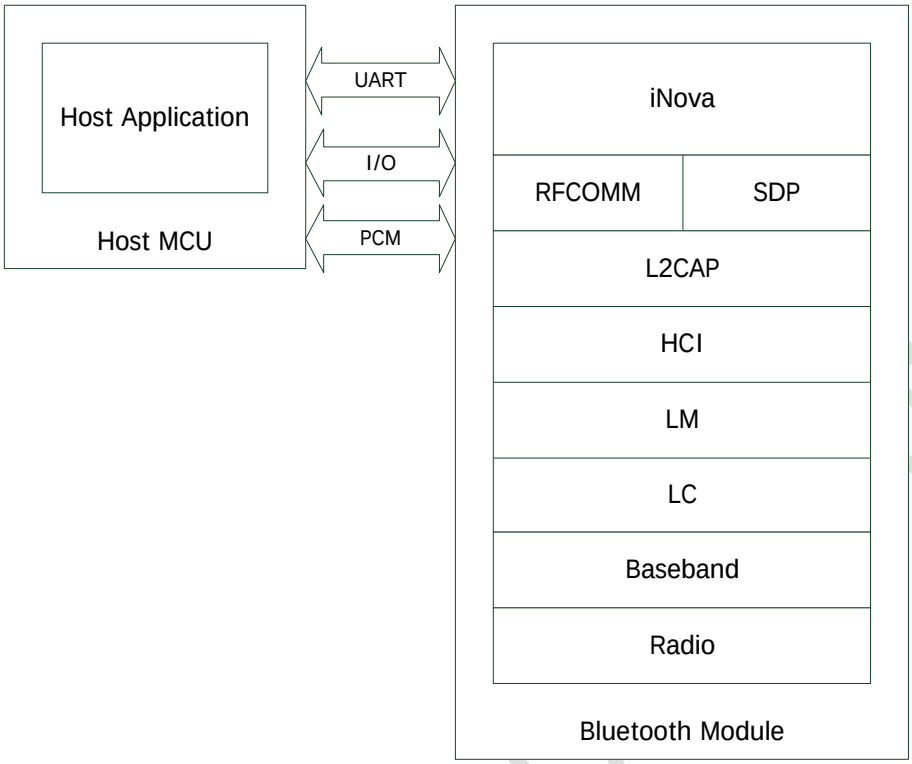

Figure 15: iNova Stack

NVC-MDCS42A is supplied with Bluetooth 2.1+EDR compliant stack firmware. With Novacomm's iNova profile stacks, the host MCU can easily integrate HFP, A2DP, AVRCP, SPP, HID profiles and iAP over Bluetooth functions.

Please refer to the Novacomm Control Interface User Guide (NCCI) for the details.

To develop accessories for iOS devices or products to connect to iOS devices, the developers must register and be approved by Apple's Made for iPod (MFi) program. Licensed developers gain access to technical documentation, hardware components, technical support and certification logos.

To get more detailed information, you can visit Apple's developer portal at:

http://developer.apple.com/ipod/

5. Reference Design

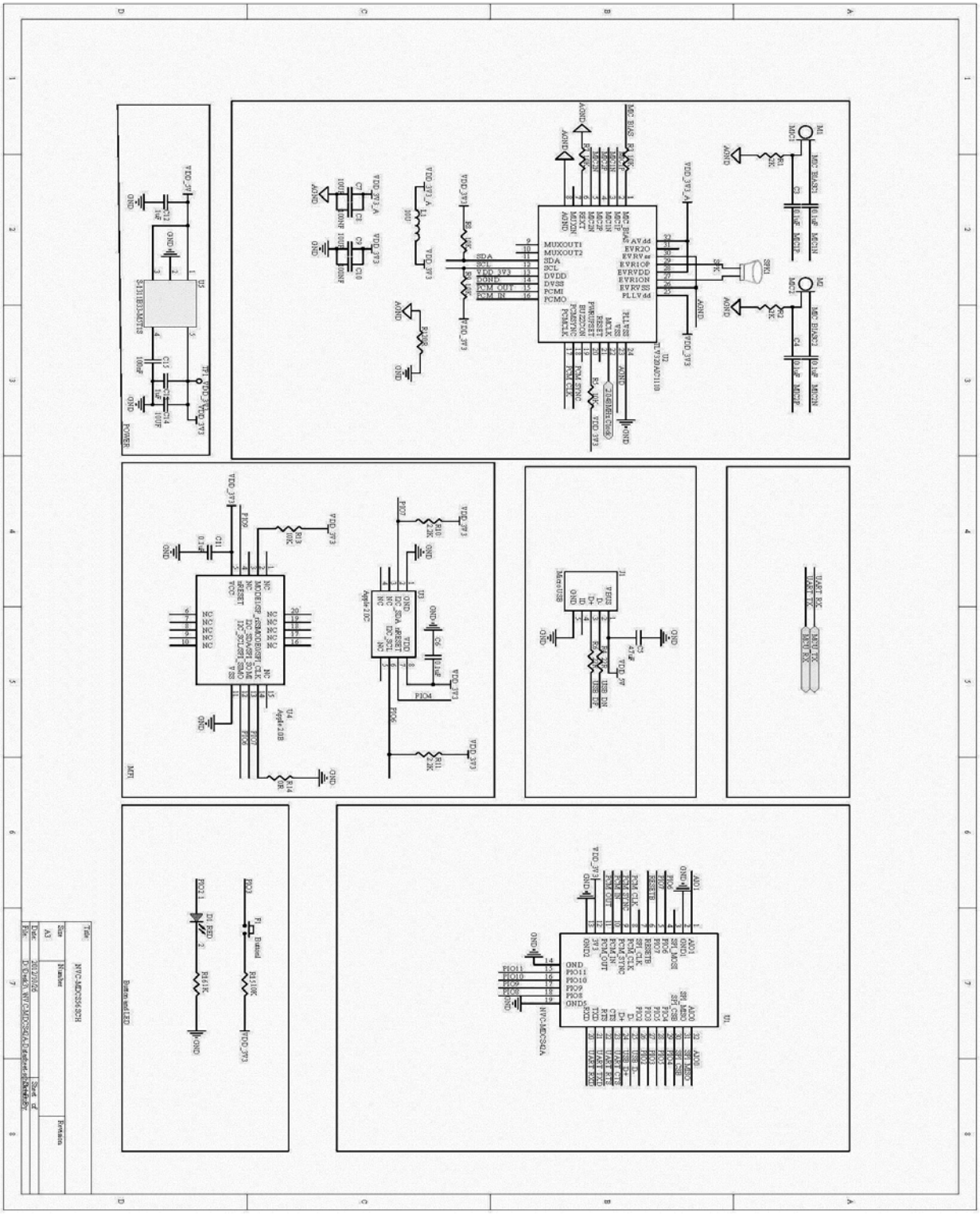

Figure 16: Reference Design

6. RF Layout Guidelines

NVC-MDCS42A has an on-board PCB antenna. So it's very important to make a good PCB placement for the module to ensure the design a good RF performance. Please follow the recommendations shown in Figure 17.

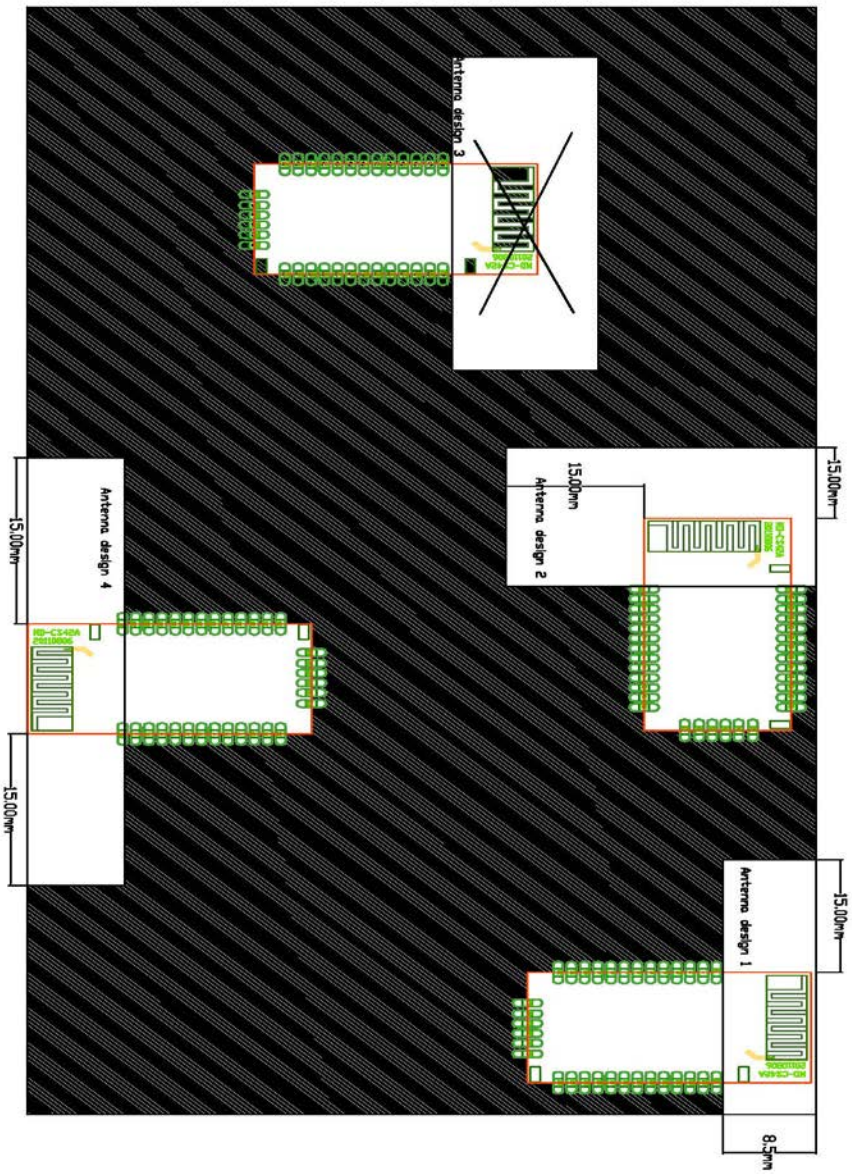

Figure 17: Placement of the Module on a Main Board

7. Reflow Profile

NVC-MDCS42A is compatible with industrial standard reflow profile for Pb-free solders. The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder re-flow.

There are four zones:

- Preheat Zone - This zone raises the temperature at a controlled rate, typically 1-2.5°C/s.
- Equilibrium Zone - This zone brings the board to a uniform temperature and also activates the flux. The duration in this zone (typically 2-3 minutes) will need to be adjusted to optimise the out gassing of the flux.
- Reflow Zone- The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint.
- Cooling Zone - The cooling rate should be fast, to keep the solder grains small which will give a longer lasting joint. Typical rates will be 2-5° C/s.

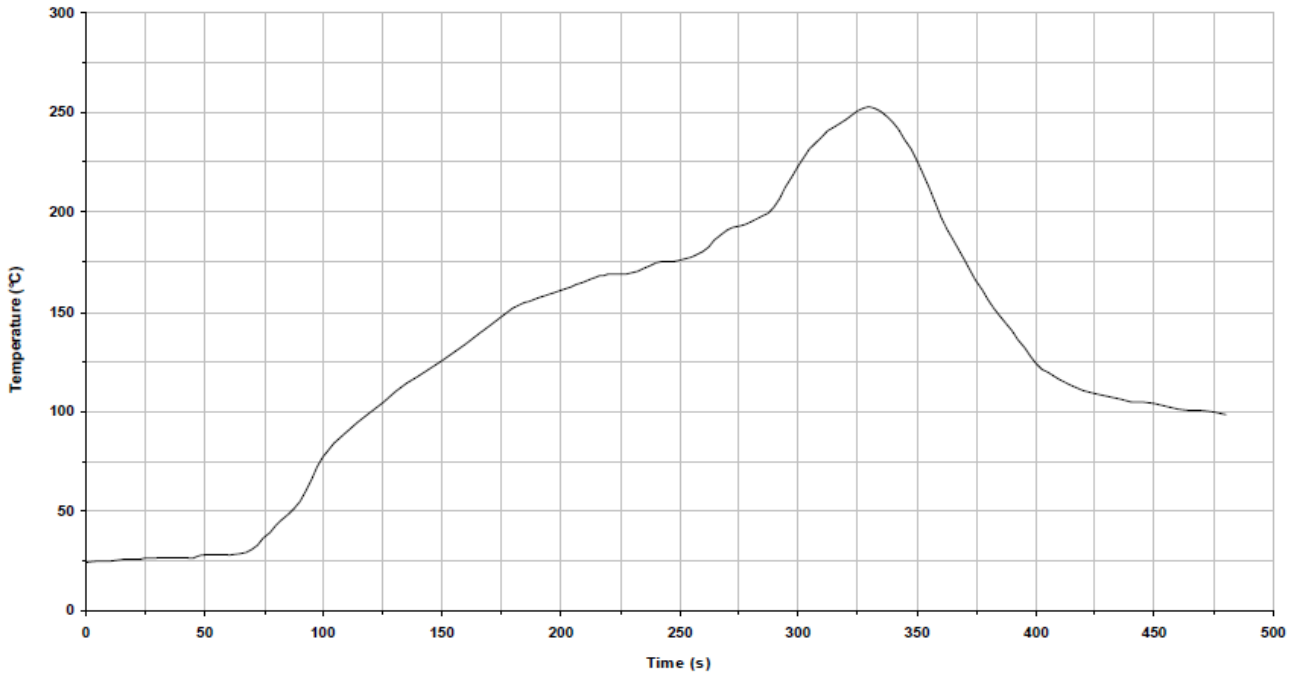

Figure 18: Typical Lead-Free Re-flow Solder Profile for NVC-MDCS42A

Key features of the profile:

- Initial Ramp = 1-2.5° C/sec to 175° C ±25° C equilibrium
- Equilibrium time = 60 to 180 seconds
- Ramp to Maximum temperature (250° C) = 3° C/sec max.
- Time above liquidus temperature (217° C): 45-90 seconds
- Device absolute maximum reflow temperature: 255° C

8. Physical Dimensions

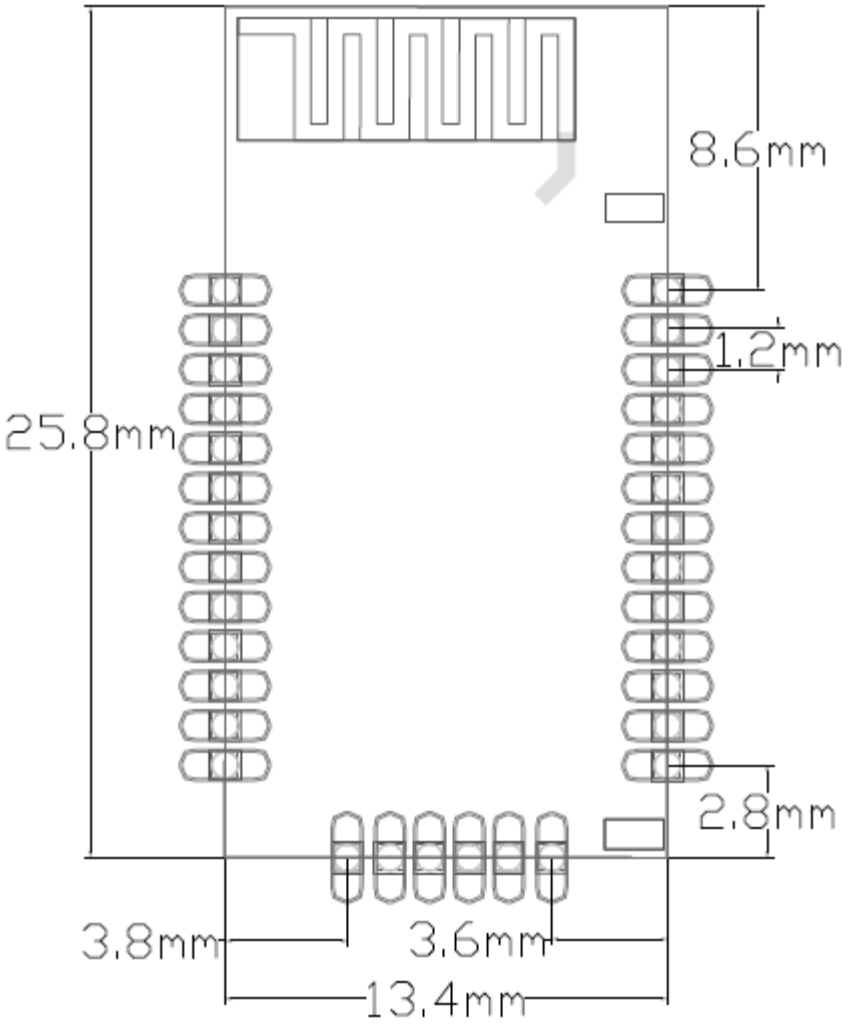

Figure 19: Physical Dimensions and Recommended Footprint (Unit: mm, Deviation:0.02mm)TOP View

9. Package

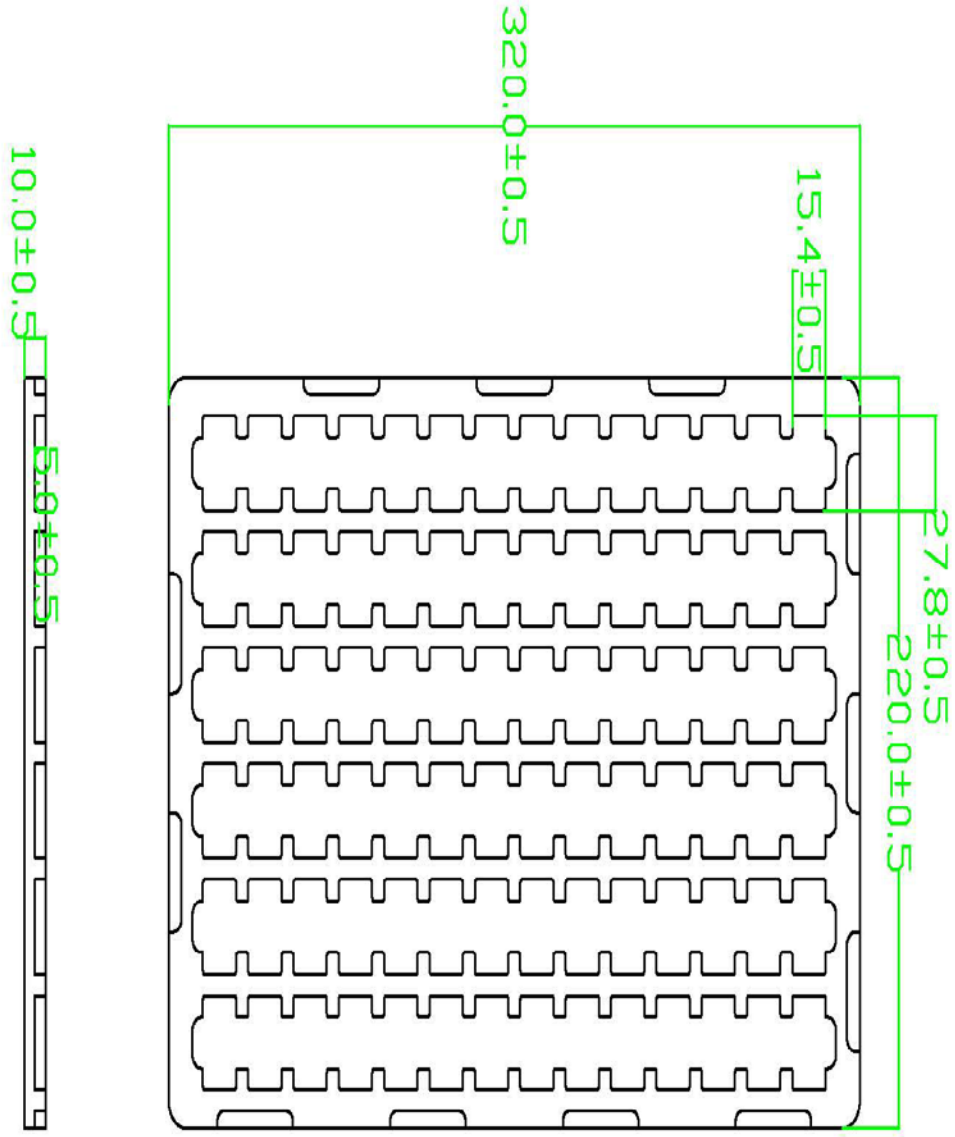

Figure 20: NVC-MDCS42A Package

Plastic tray, plus aluminum bags do vacuum packing. Items in One Package number of 84PCS

10. Contact Information

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