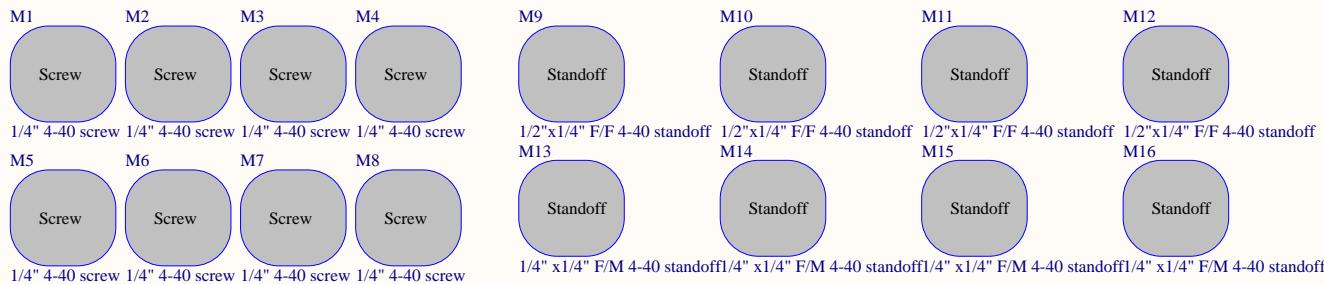


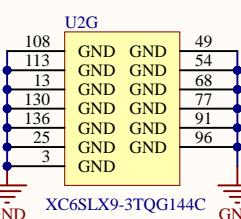
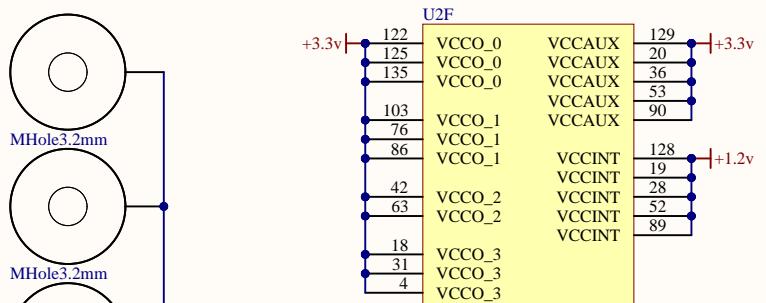
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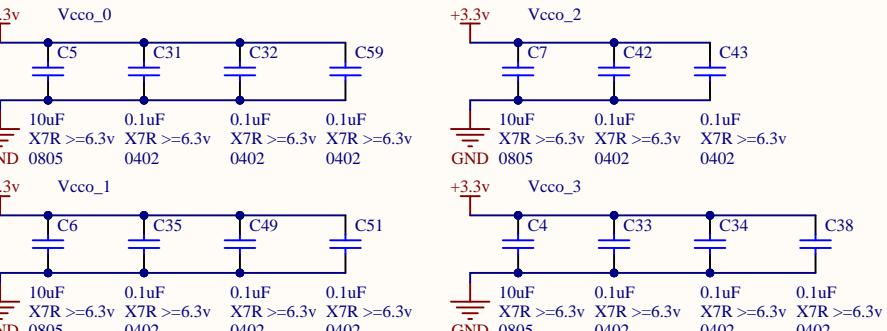
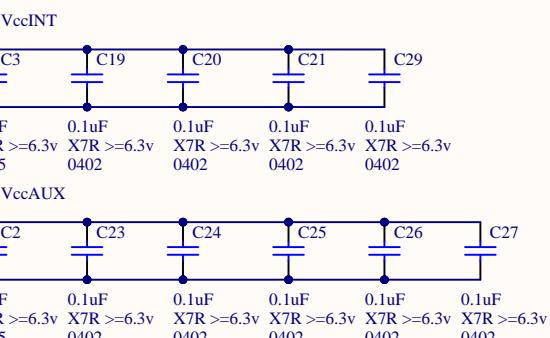
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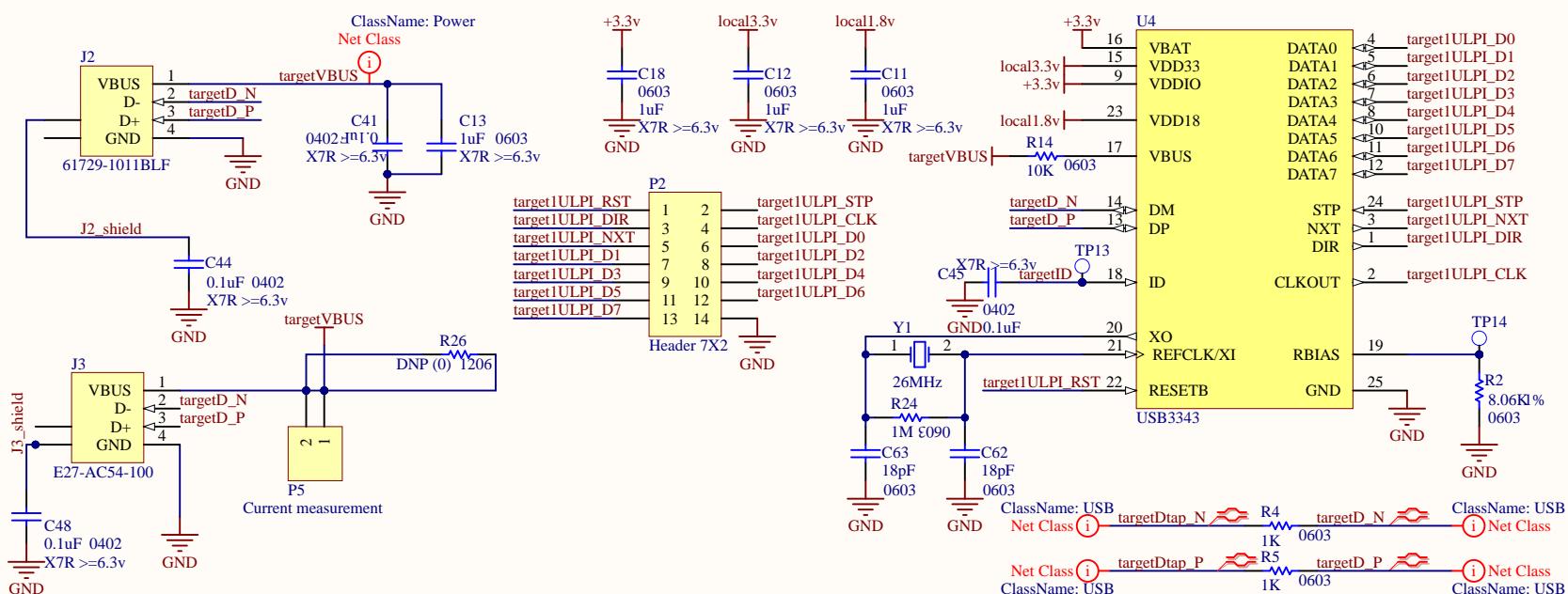
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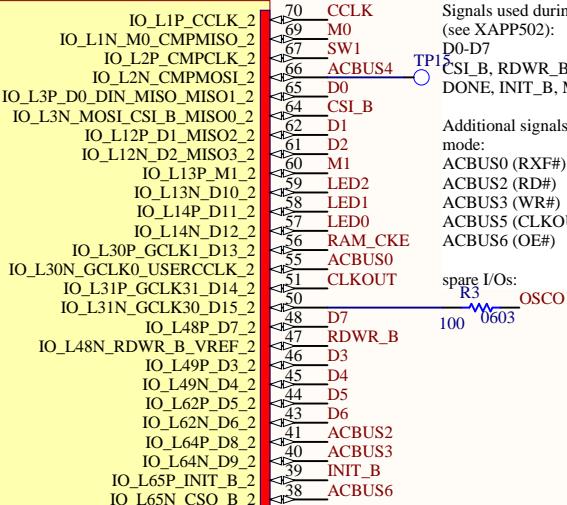
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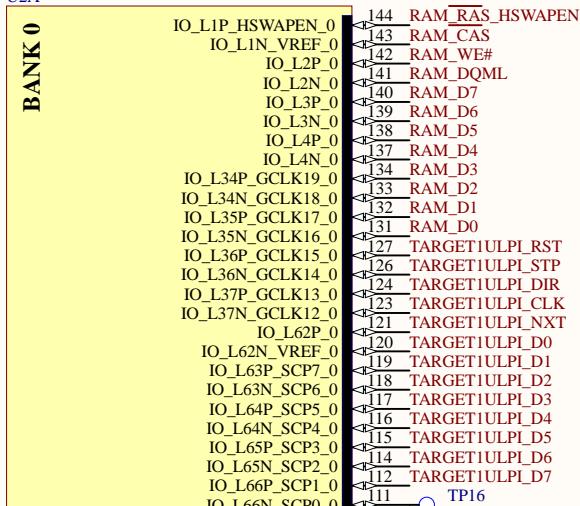
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BANK 2

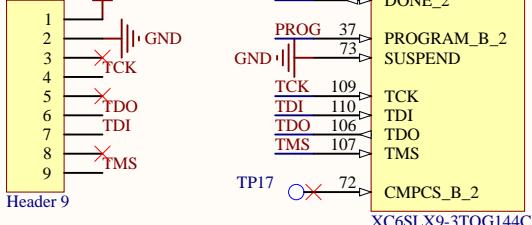
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BANK 0

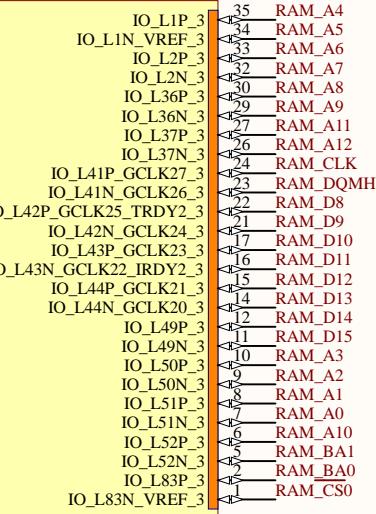
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P1

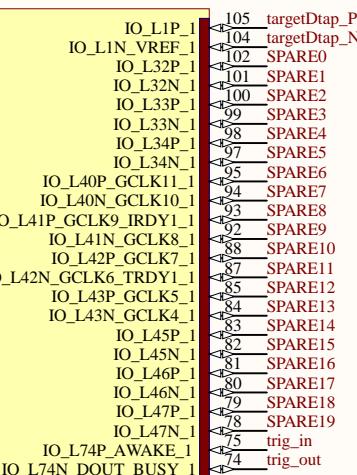


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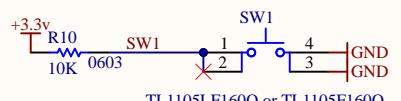
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BANK 3

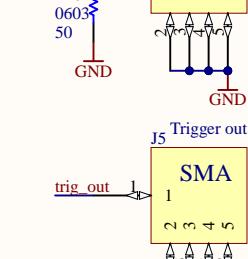
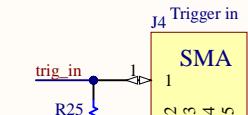
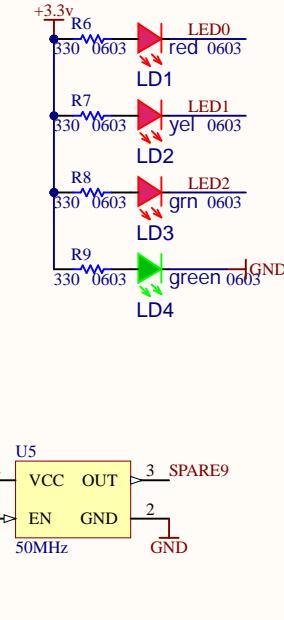
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BANK 1

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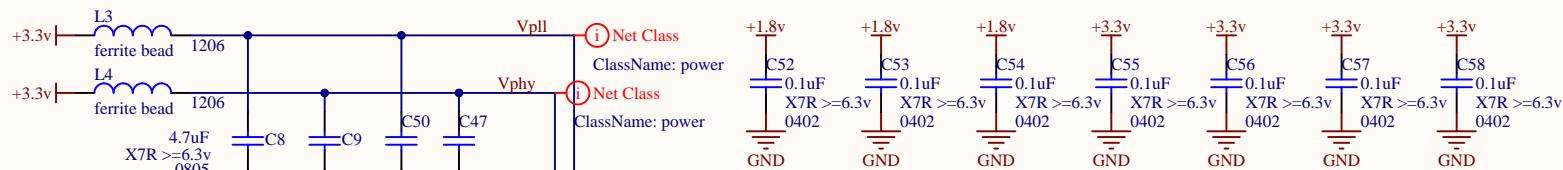
TL1105LF160Q or TL1105F160Q



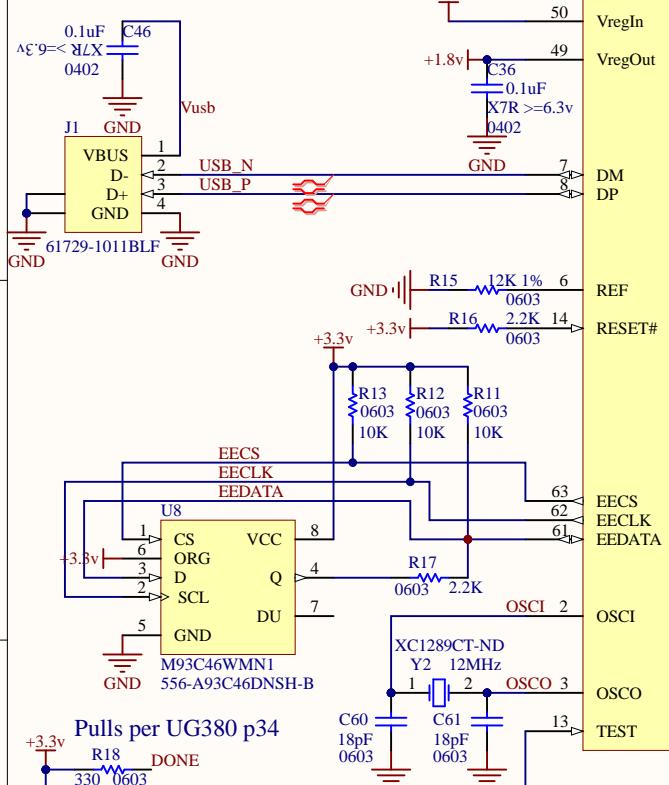
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B



D

GND

FT2232H

Configuration / FIFO to FPGA

Signals used during FPGA configuration
(see XAPP502):
D0-D7
CSI_B, RDWR_B, CCLK, PROG_B,
DONE, INIT_B, M0, M1

Additional signals used during FIFO mode:
ACBUS0 (RXF#)
ACBUS2 (RD#)
ACBUS3 (WR#)
ACBUSS (CLKOUT)
ACBUS6 (OE#)

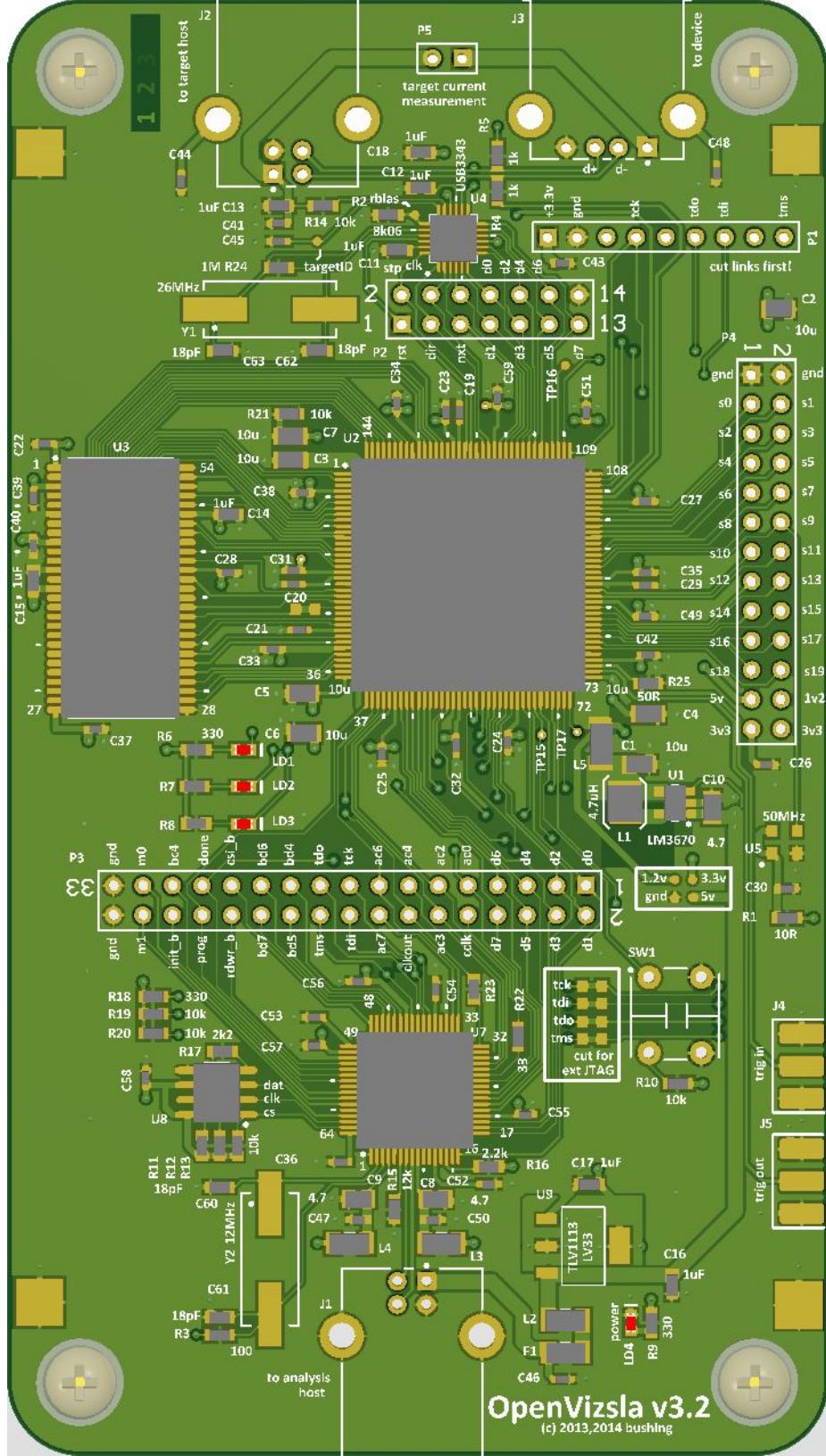
spare I/Os:

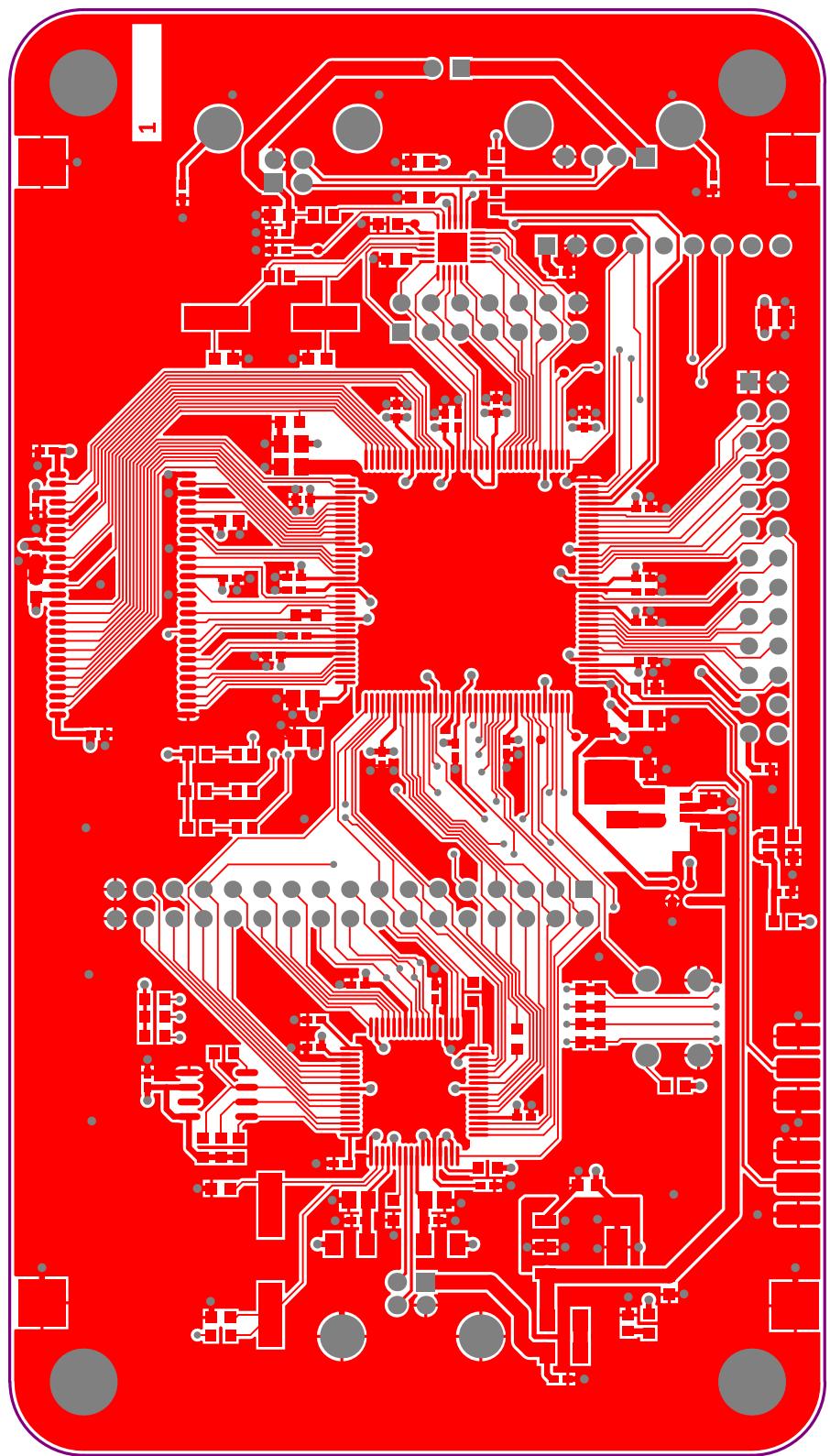
P3	D0	D1	D2	D3	D4	D5	D6	D7	CCLK	CLKOUT
	1	2	3	4	5	6	7	8	0603	0603
	D0	D1	D2	D3	D4	D5	D6	D7	ACBUS0	ACBUS1
	ACBUS1	ACBUS2	ACBUS3	ACBUS4	ACBUS5	ACBUS6	ACBUS7		ACBUS0	ACBUS1
	ACBUS2	ACBUS3	ACBUS4	ACBUS5	ACBUS6	ACBUS7			ACBUS0	ACBUS1
	ACBUS3	ACBUS4	ACBUS5	ACBUS6	ACBUS7				ACBUS0	ACBUS1
	ACBUS4	ACBUS5	ACBUS6	ACBUS7					ACBUS0	ACBUS1
	ACBUS5	ACBUS6	ACBUS7						ACBUS0	ACBUS1
	ACBUS6	ACBUS7							ACBUS0	ACBUS1
									ACBUS0	ACBUS1
									ACBUS2	ACBUS3
									ACBUS4	ACBUS5
									ACBUS6	ACBUS7
									FTDI_TCK	FTDI_TDI
									FTDI_TDO	FTDI_TMS

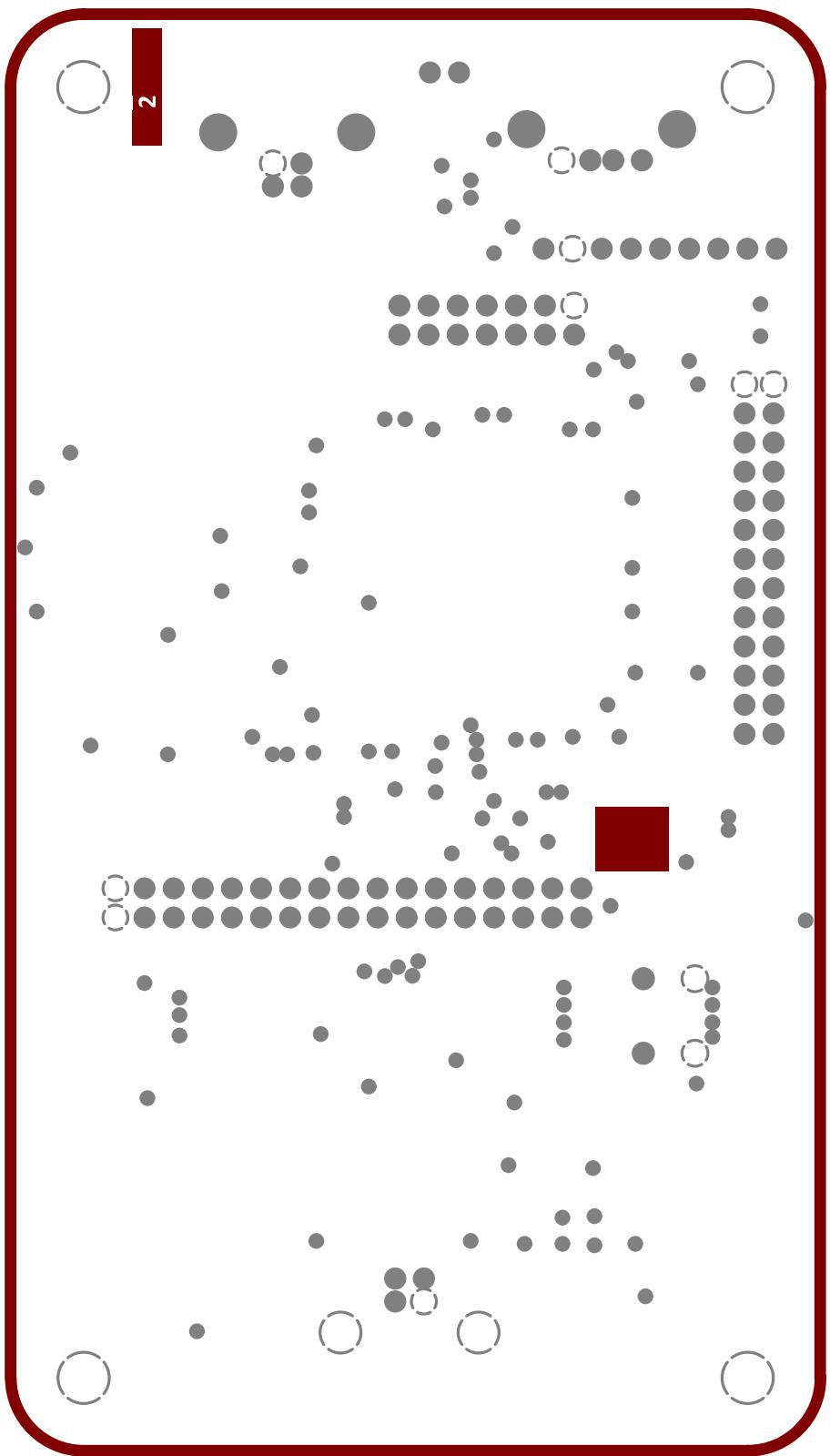
	TCK	TDI	TDO	TMS
FTDI_TCK	NT			
FTDI_TDI	NT	TDI		
FTDI_TDO	NT		TDO	
FTDI_TMS	NT			TMS

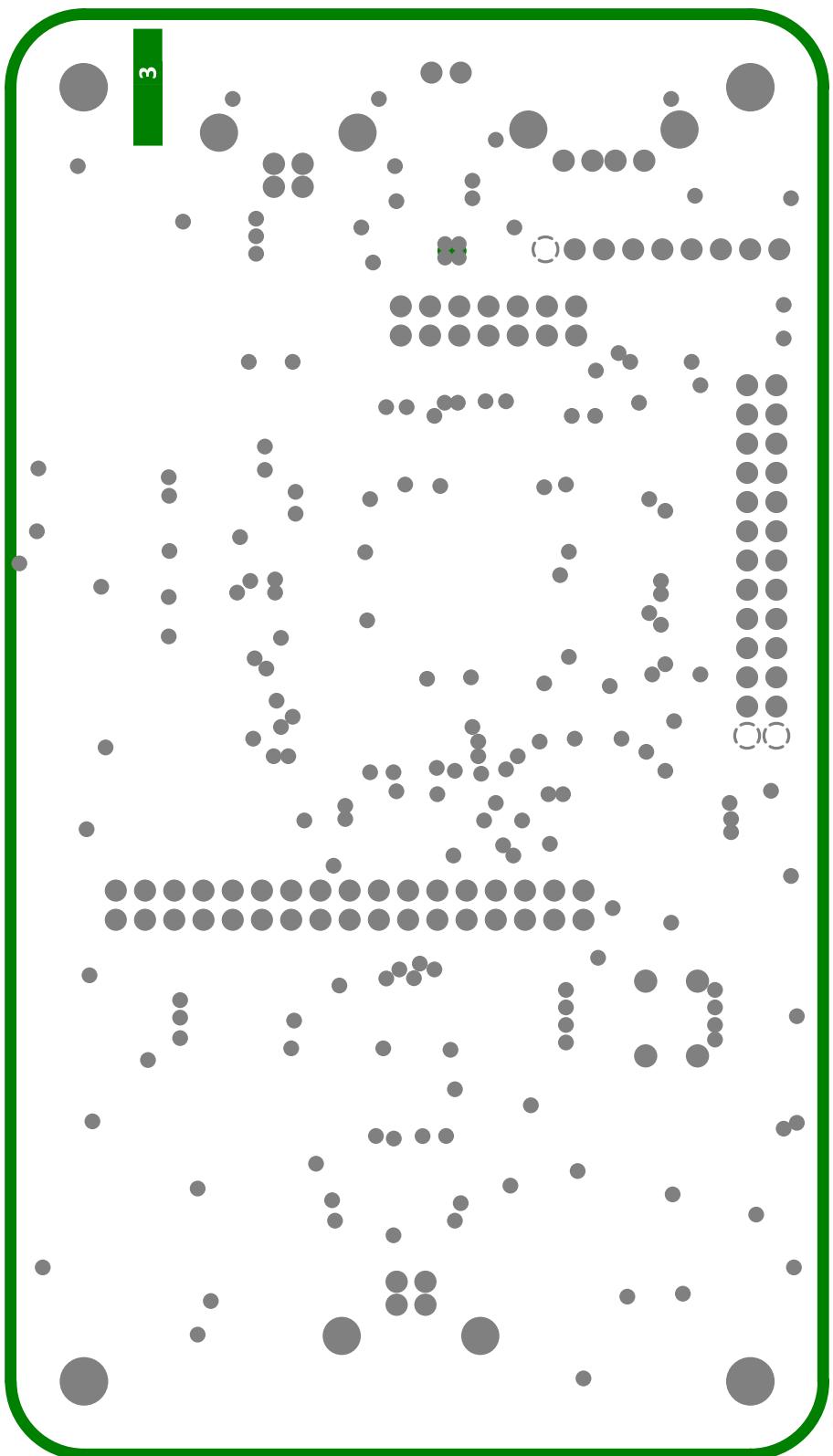
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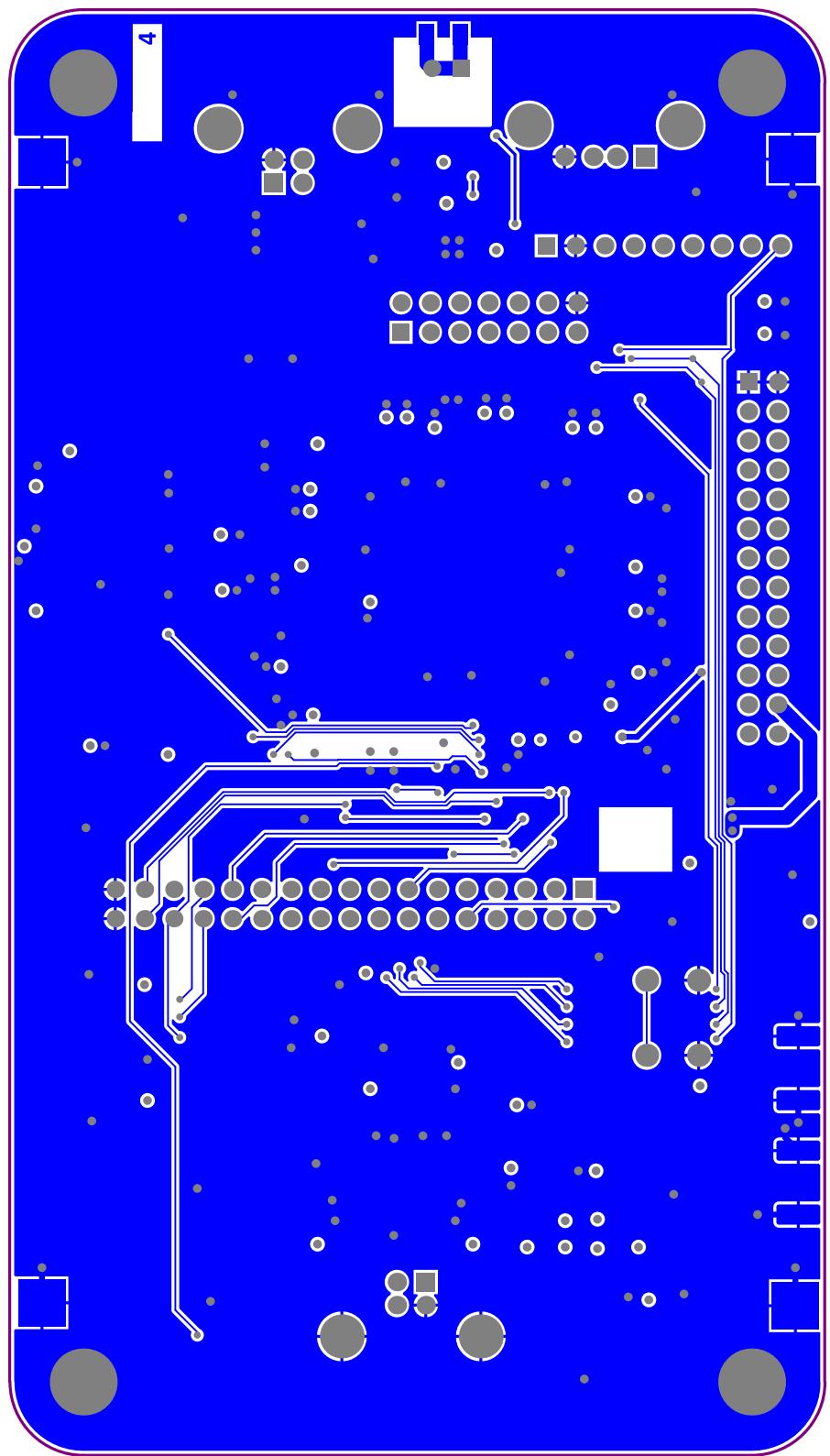


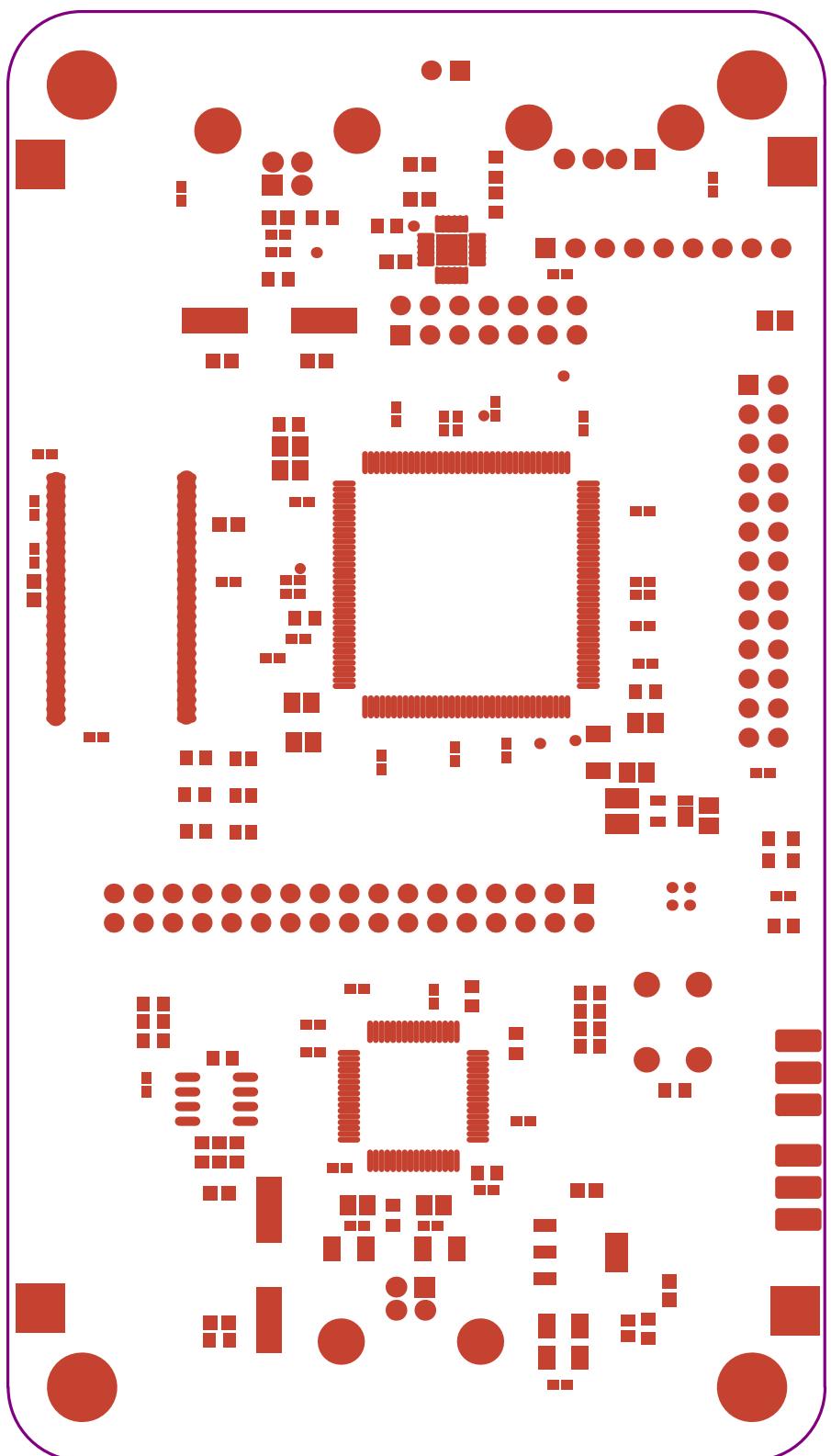


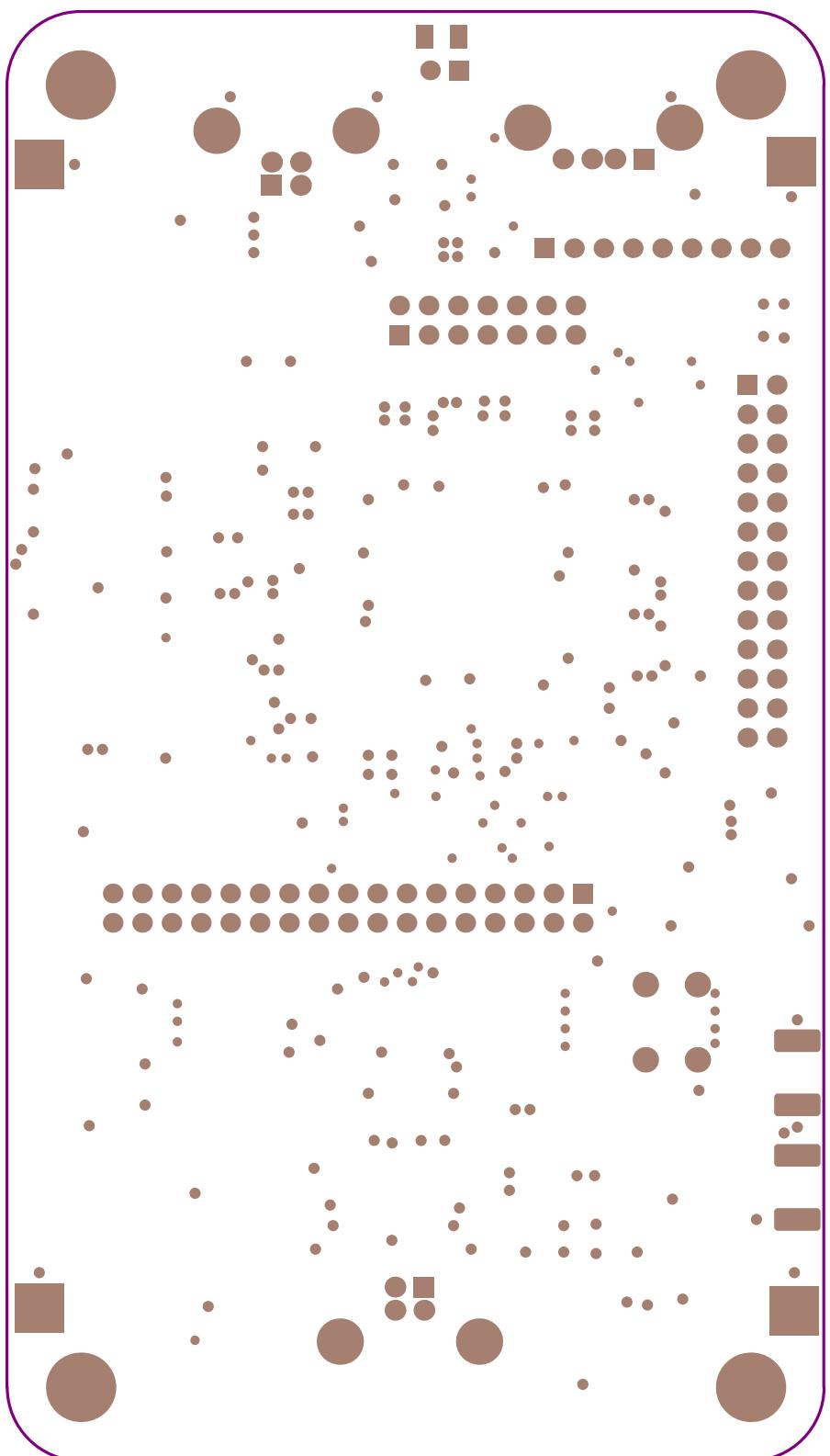


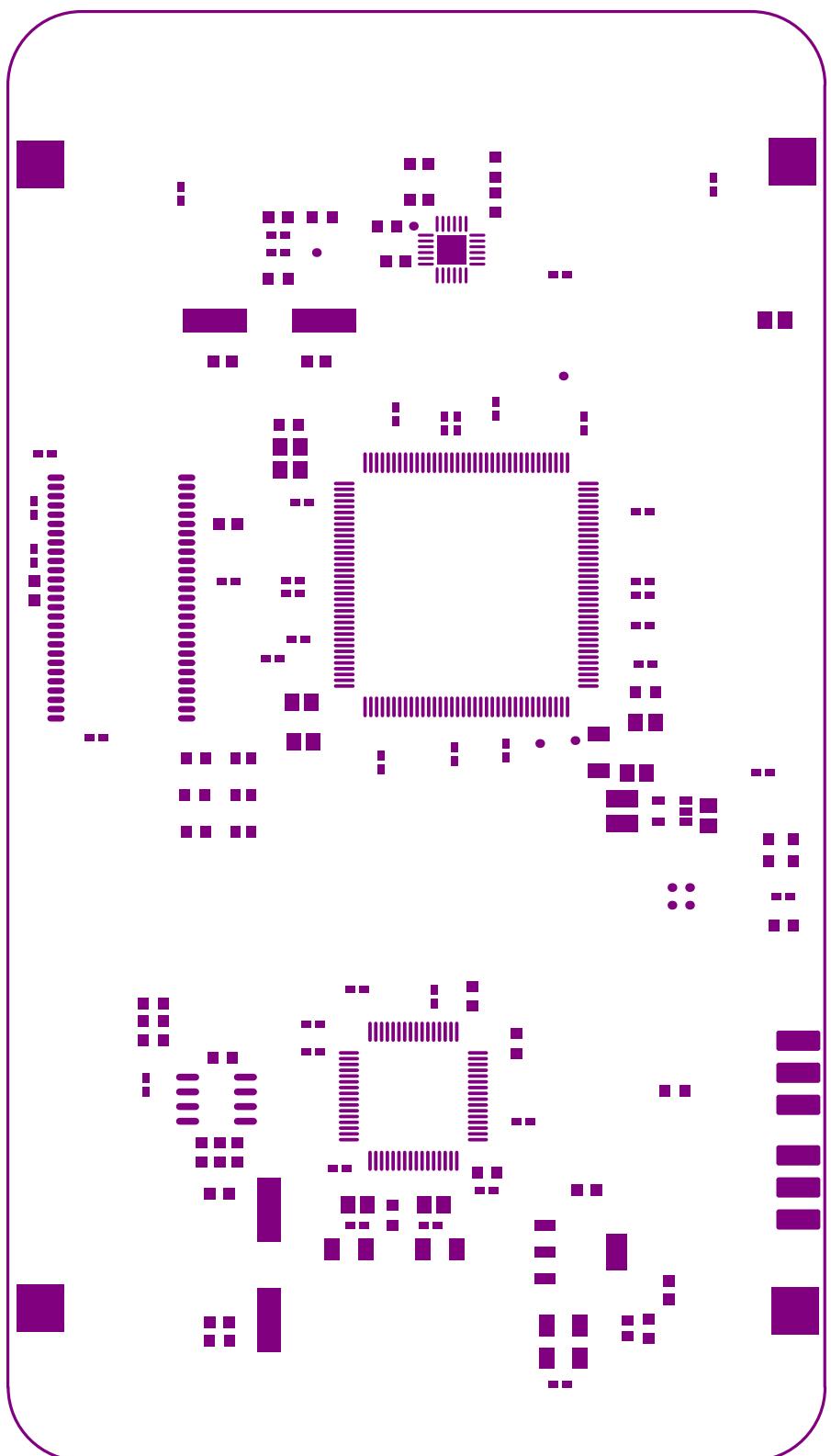


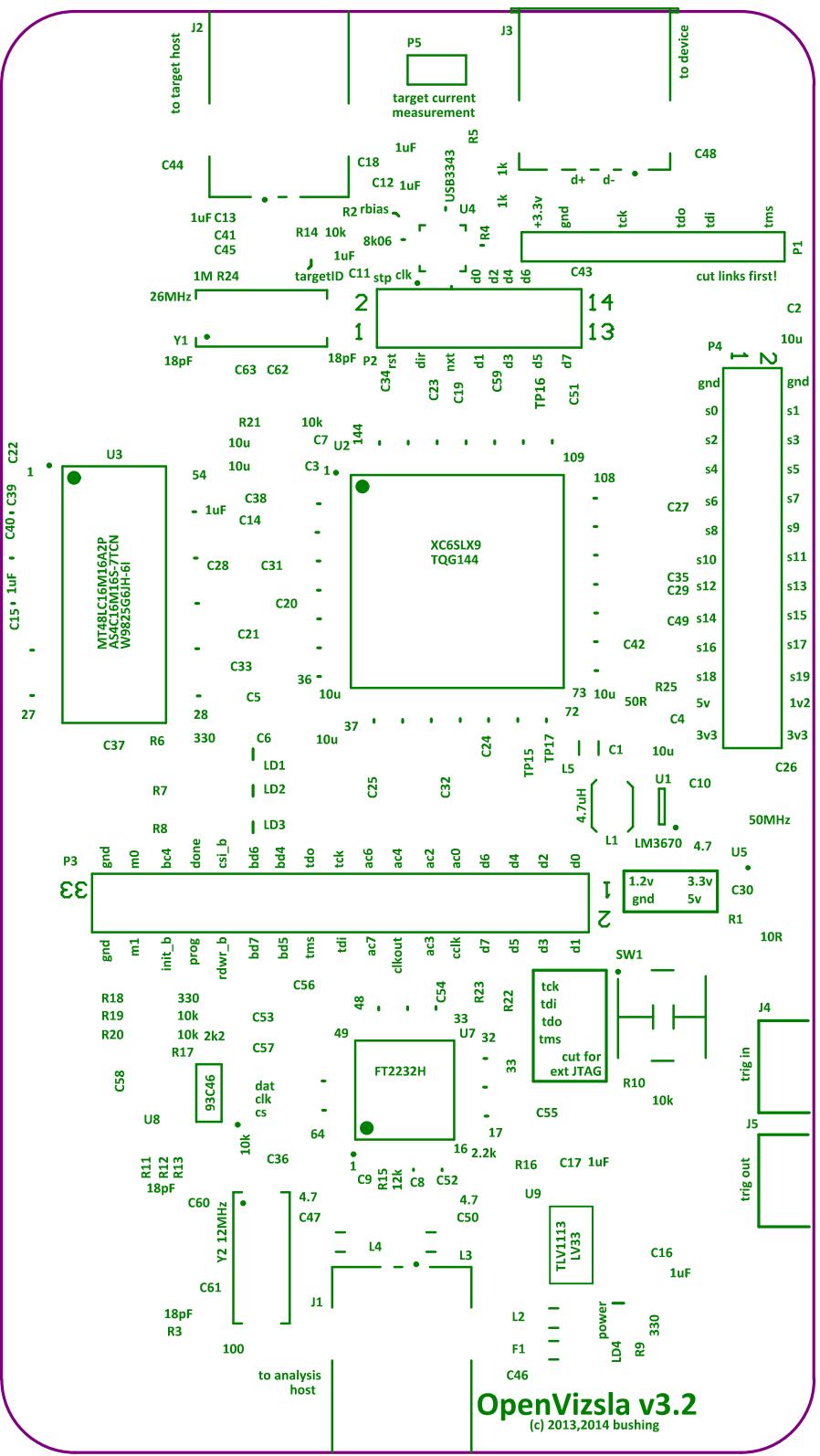
3











measures must be taken to
ensure that the
target audience
can take full
advantage of
the new measure.

Adv
D+

smj
ibj
obj

cut links first!

bring

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