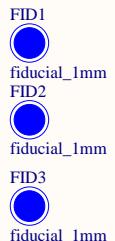
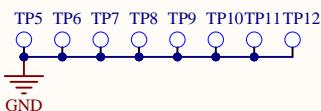
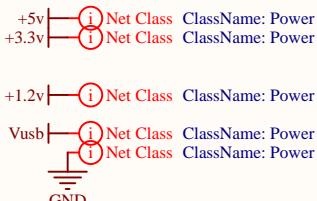
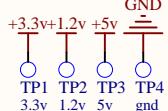


### Ground clip pads



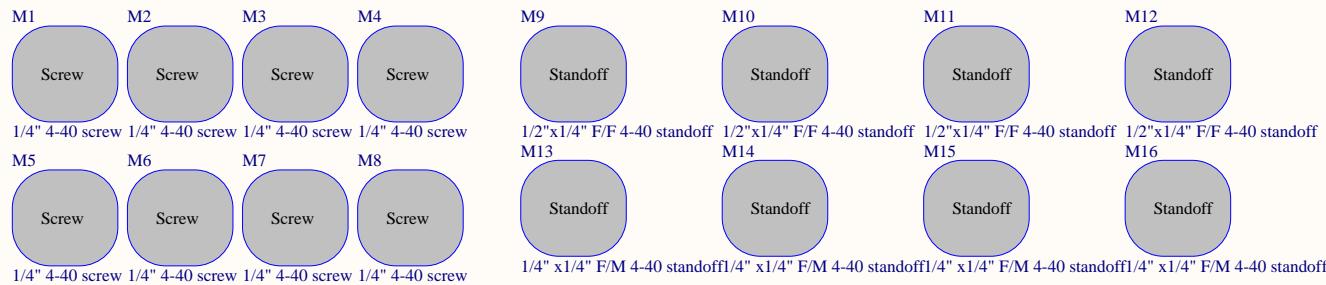
### Power supply test points, top side



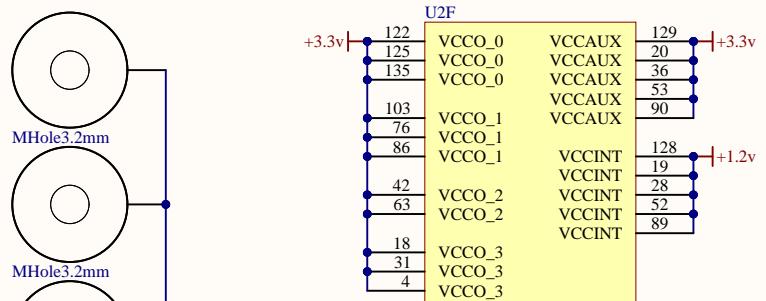
Copyrights: CC-BY-SA 3.0 Patents: Apache 2.0

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File:	C:\Users\...\power.SchDoc	Drawn By:

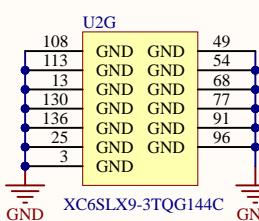
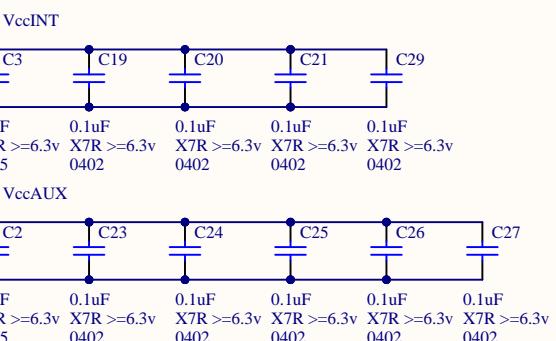
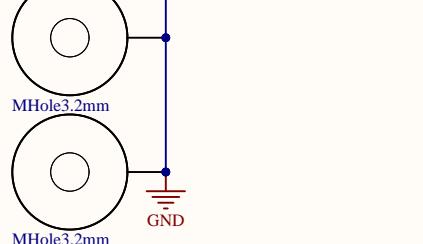
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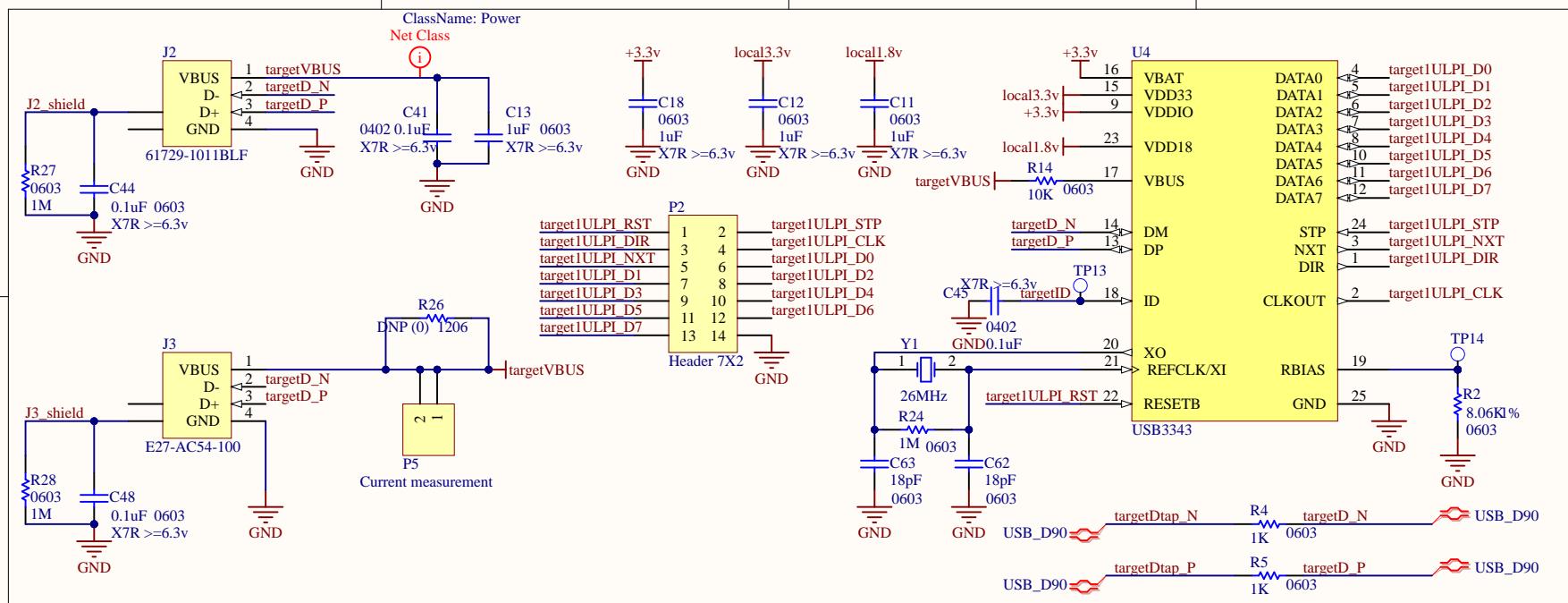


C



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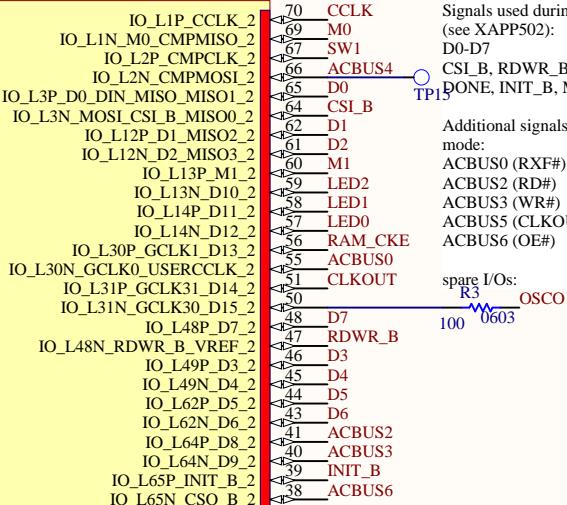
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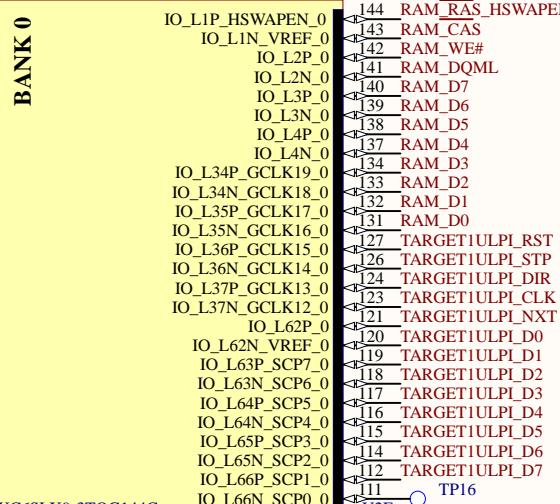
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U2C

**BANK 2**

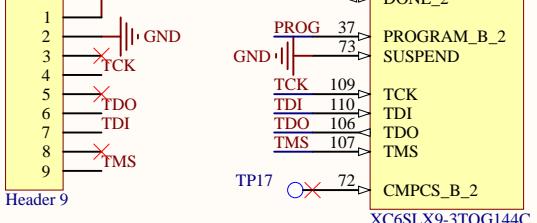
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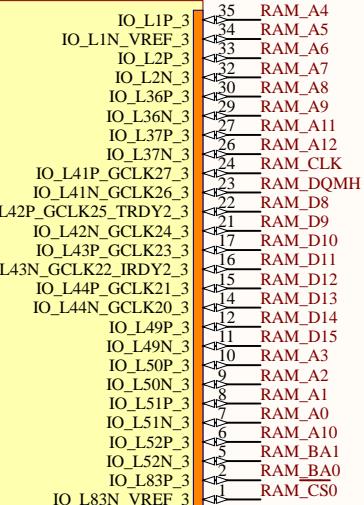
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P1

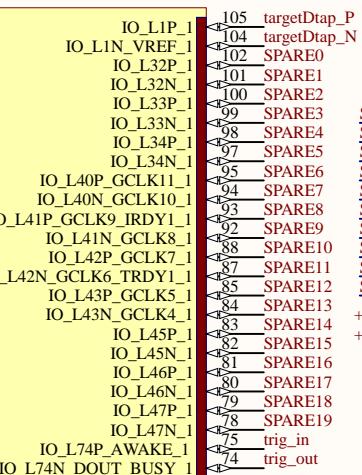


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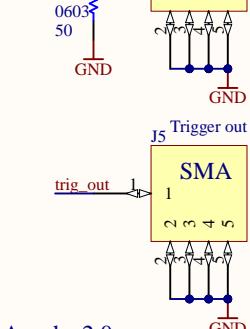
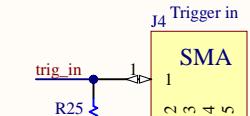
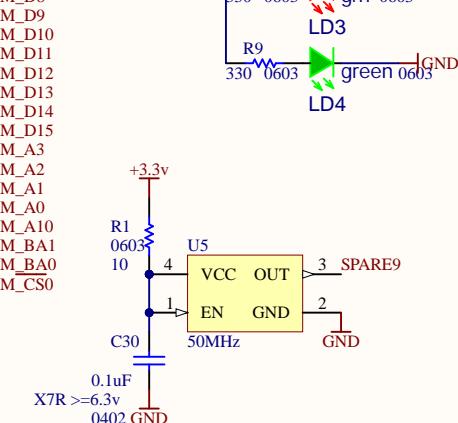
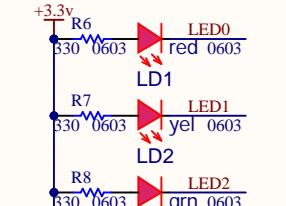
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**BANK 3**

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**BANK 1**

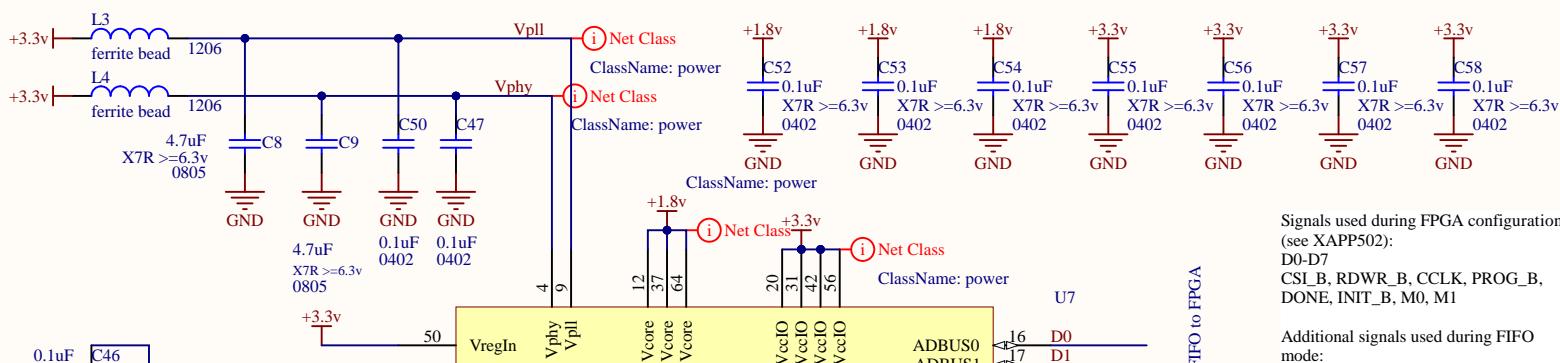
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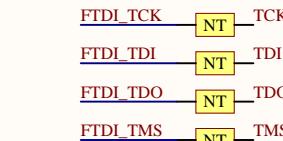
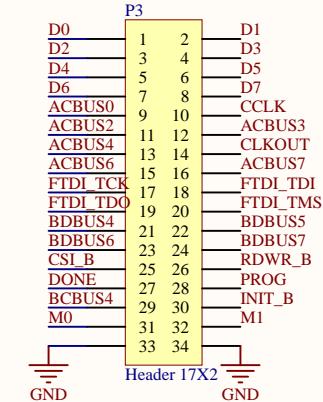
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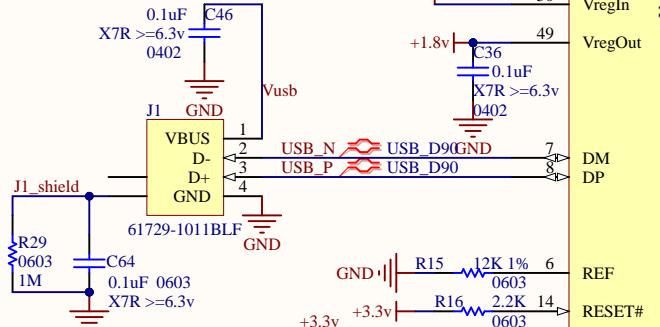
Signals used during FPGA configuration (see XAPP502):  
D0-D7  
CSI\_B, RDWR\_B, CCLK, PROG\_B,  
DONE, INIT\_B, M0, M1

Additional signals used during FIFO mode:  
ACBUS0 (RXF#)  
ACBUS2 (RD#)  
ACBUS3 (WR#)  
ACBUSS (CLKOUT)  
ACBUS6 (OE#)

spare I/Os:

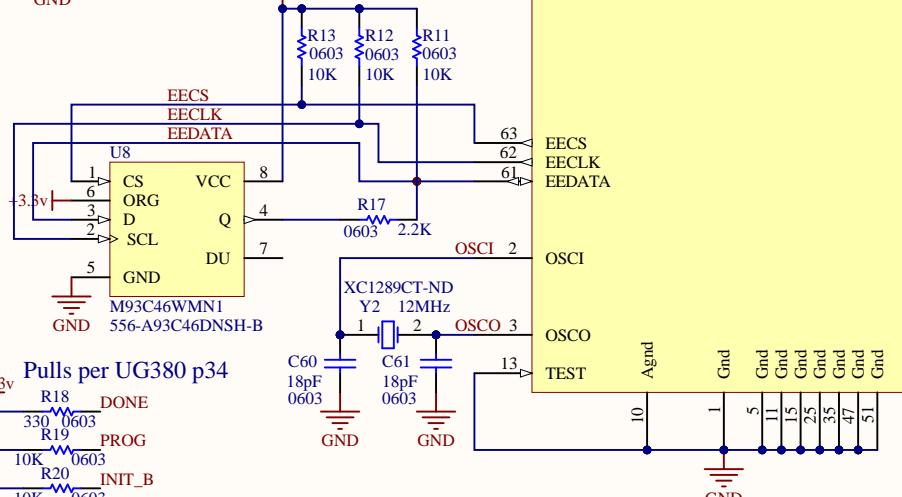


B



FT2232H

C

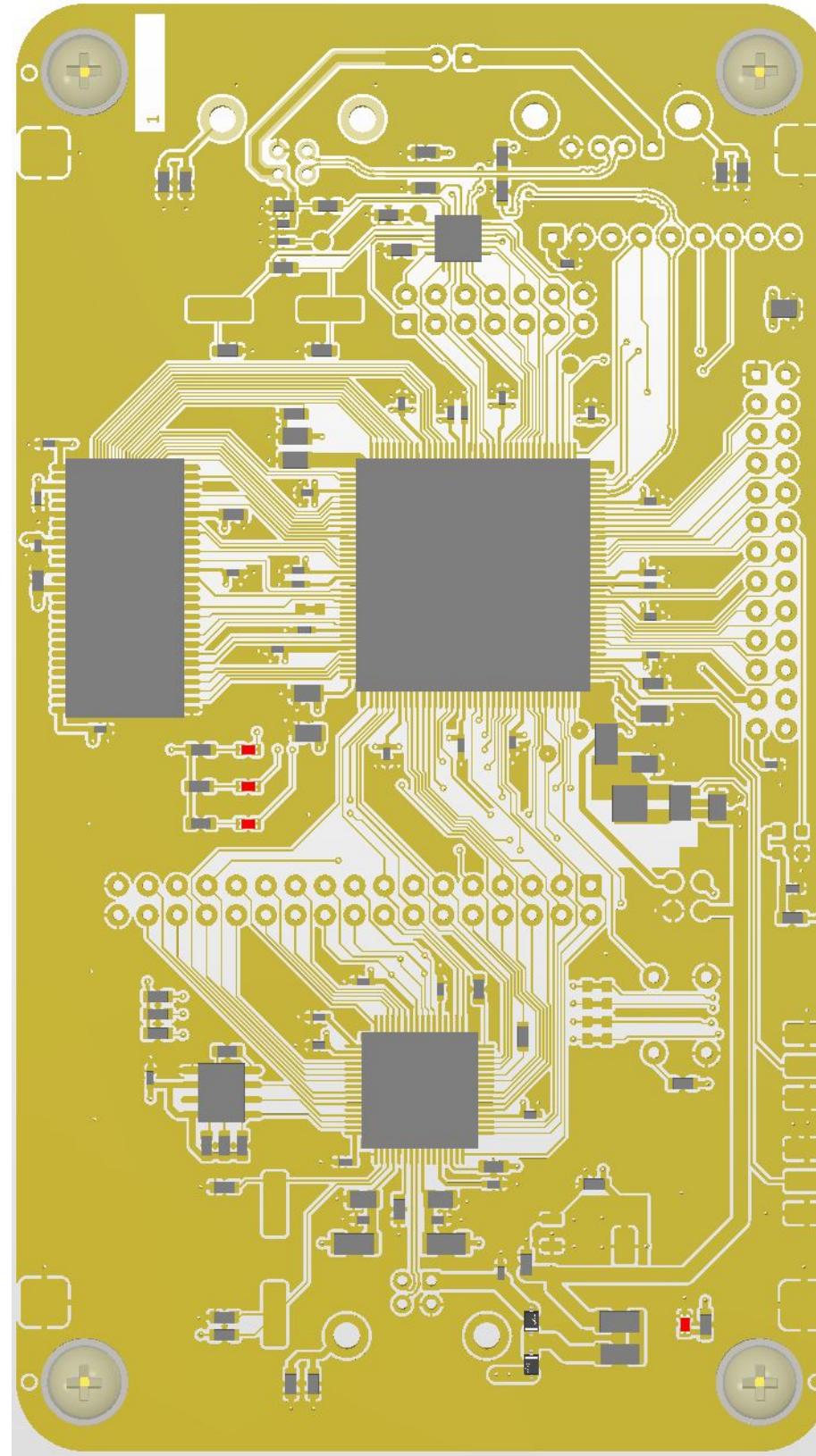


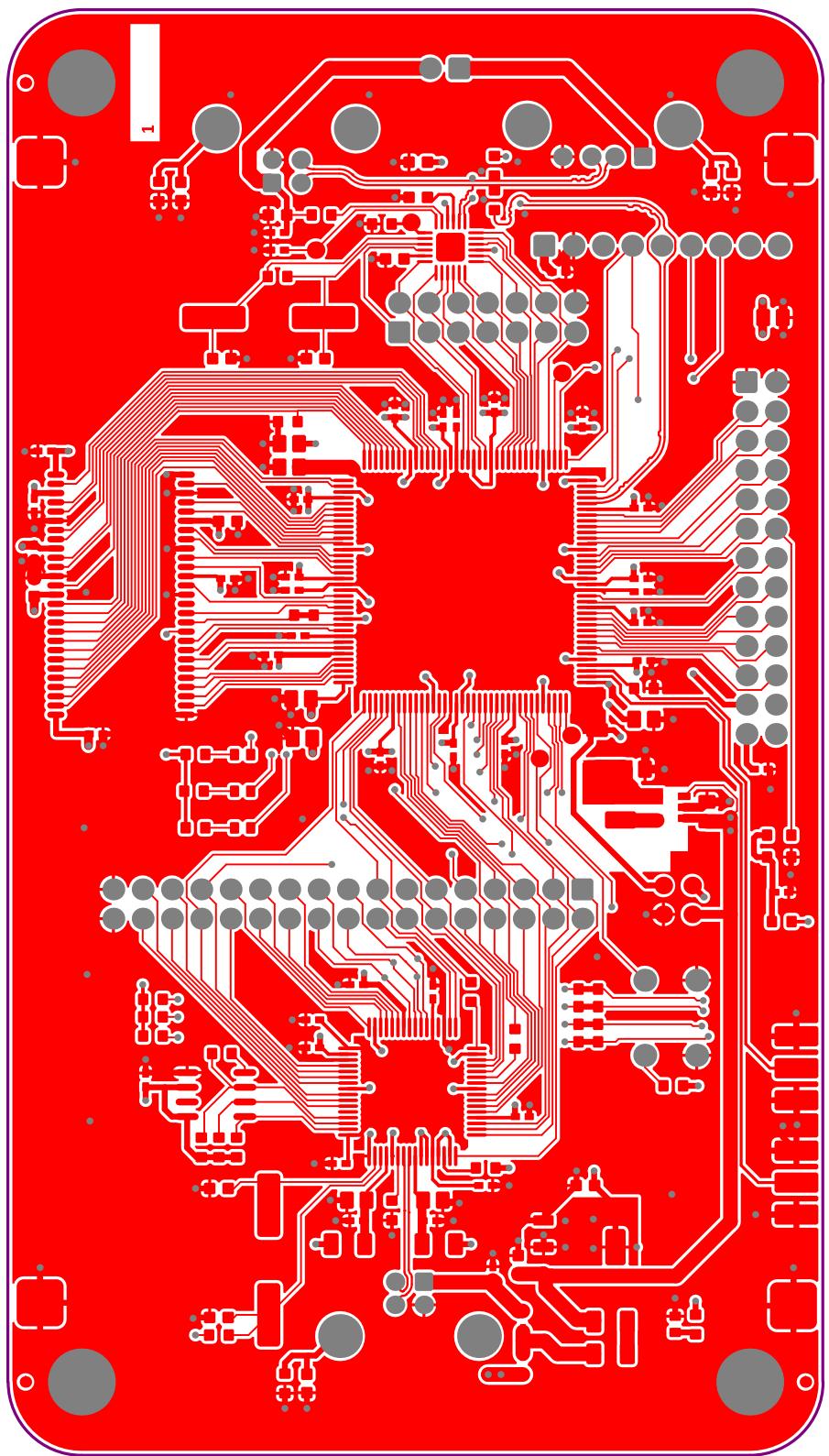
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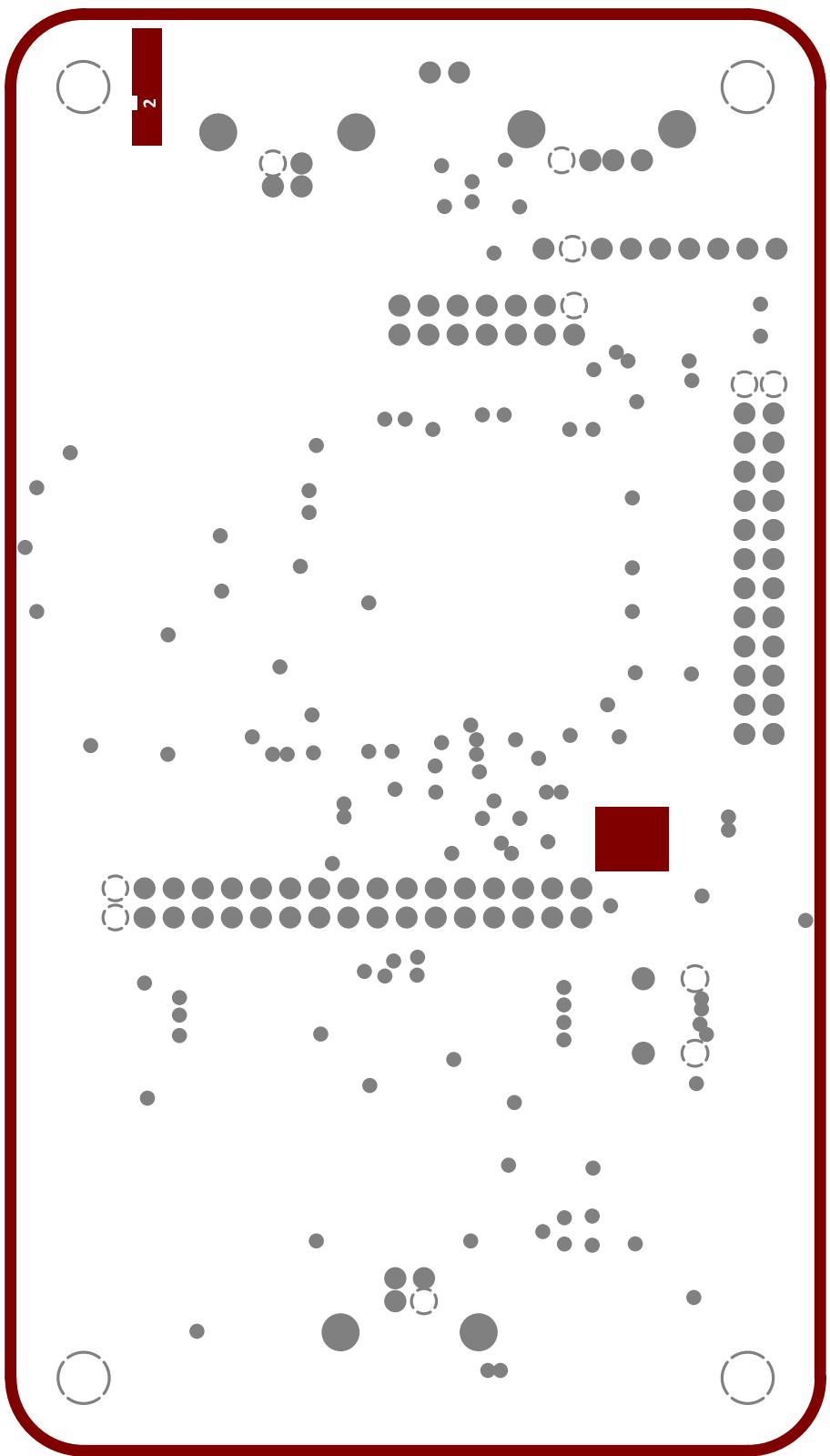


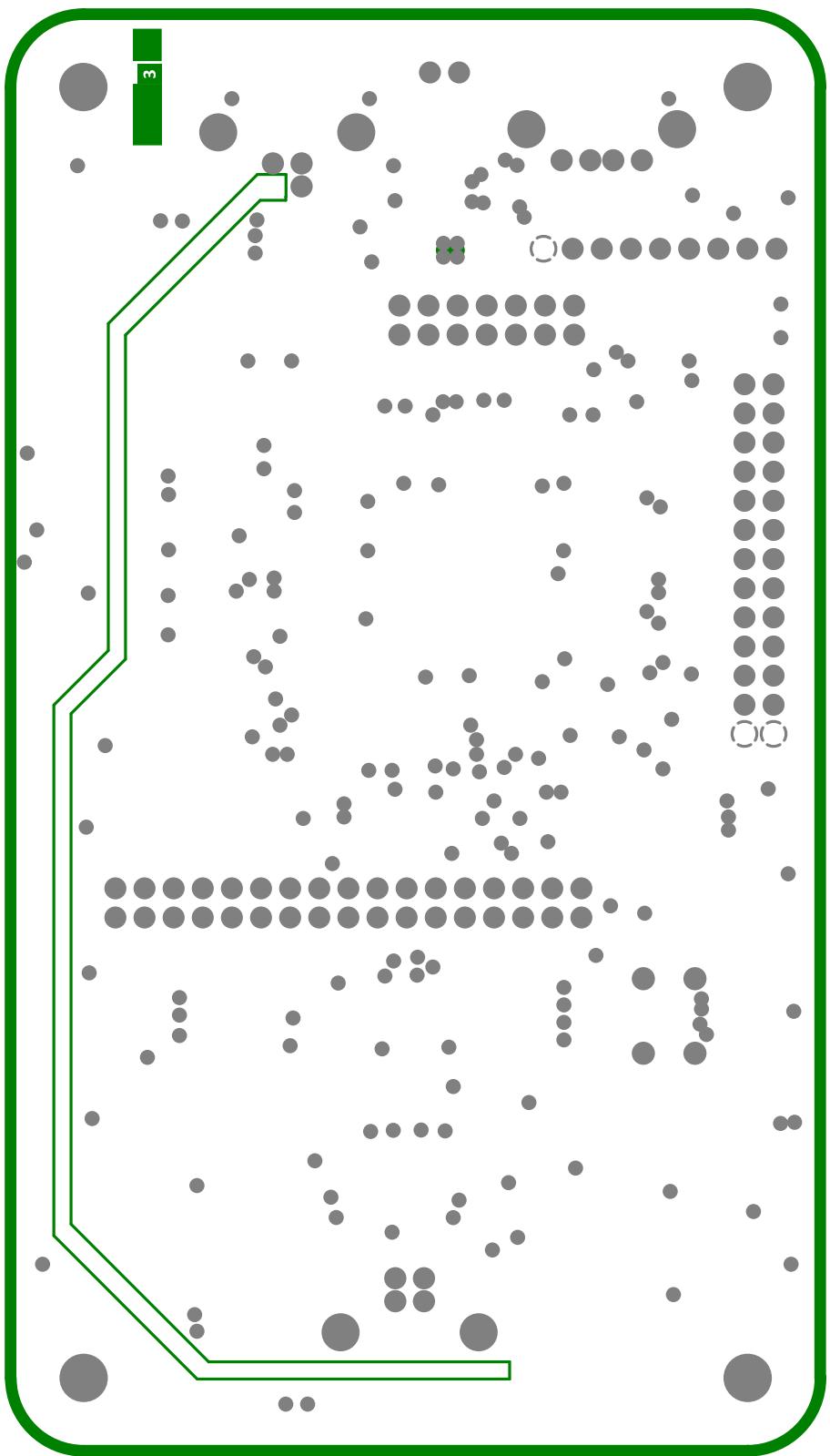
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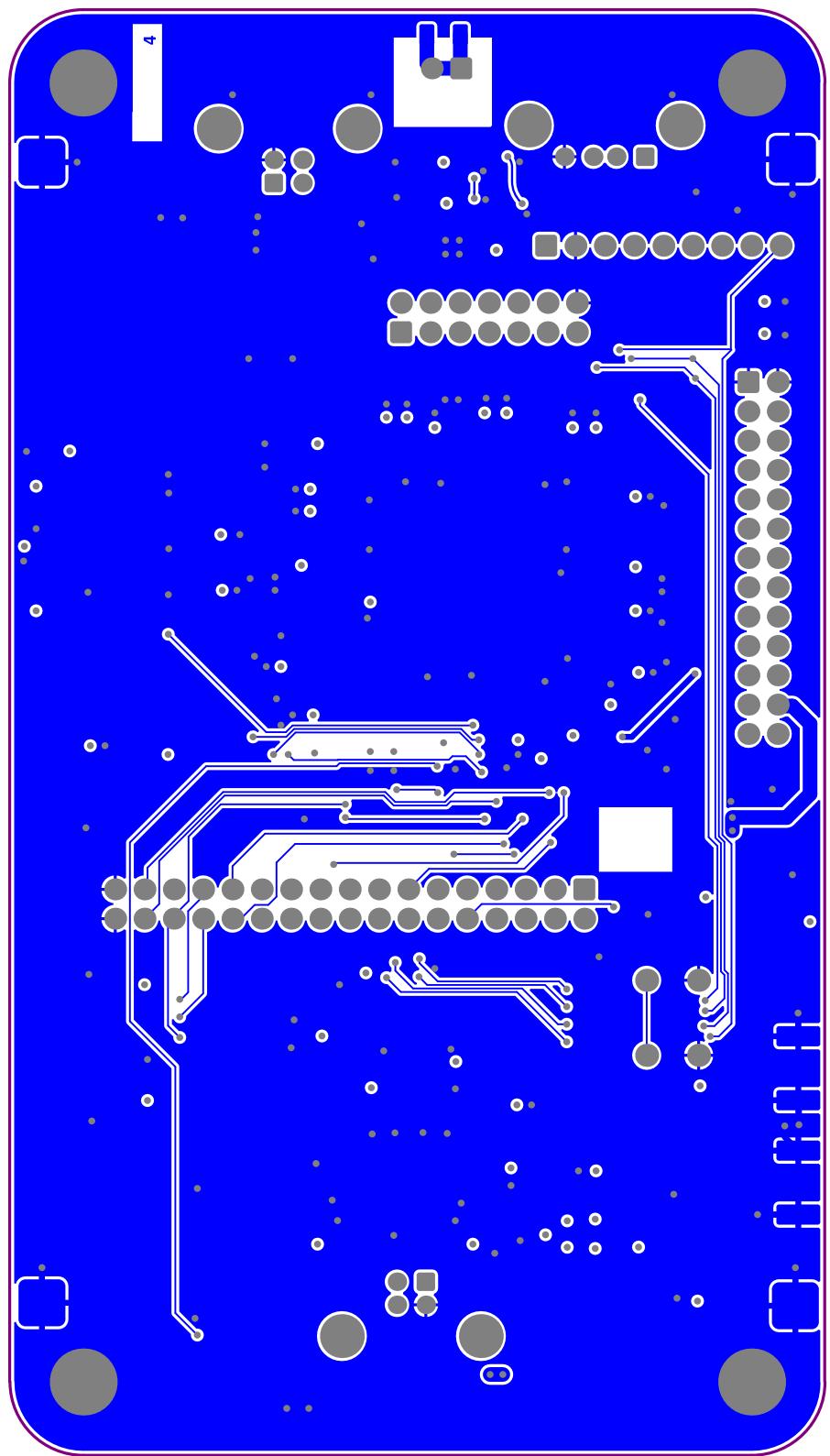
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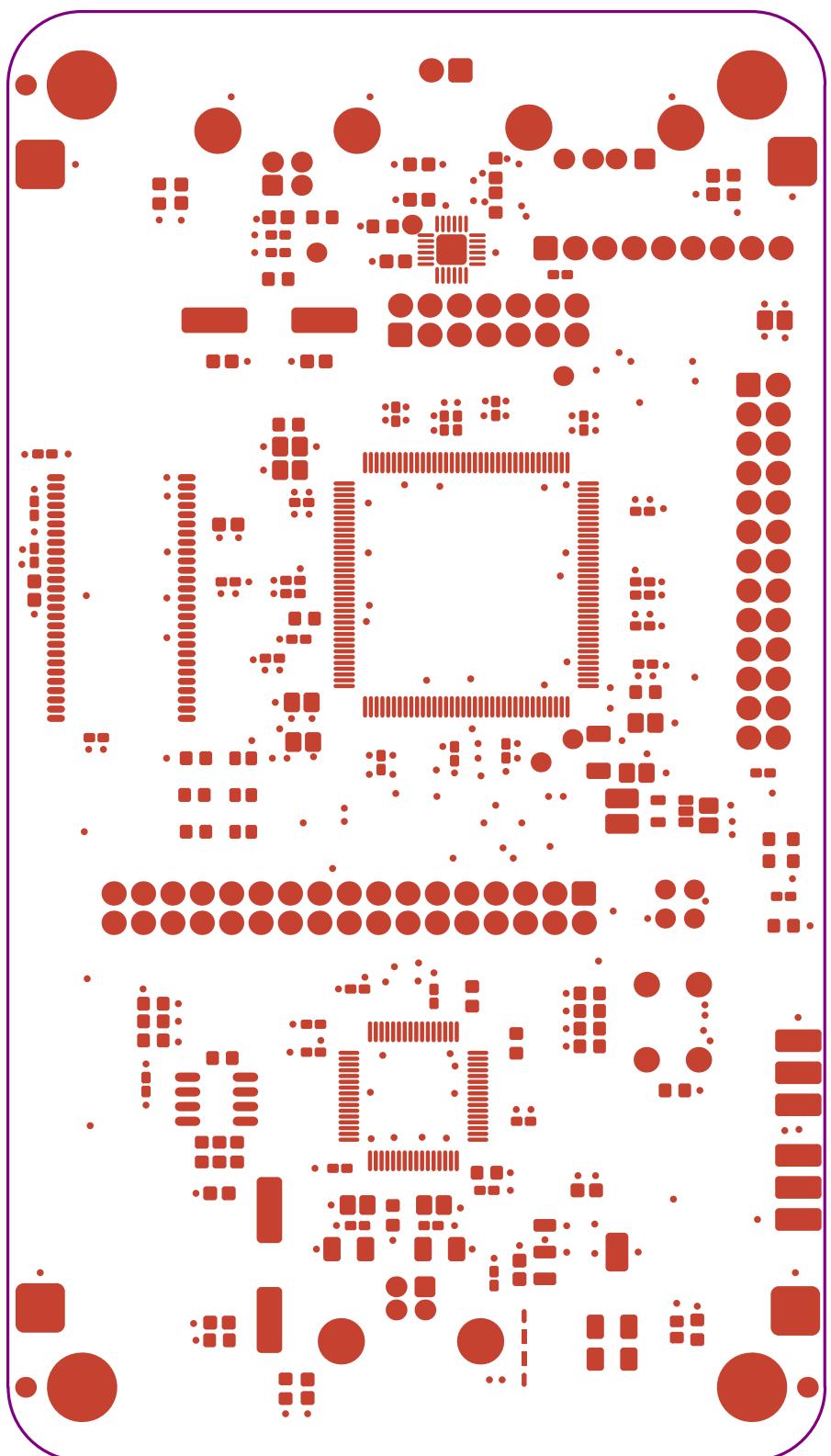


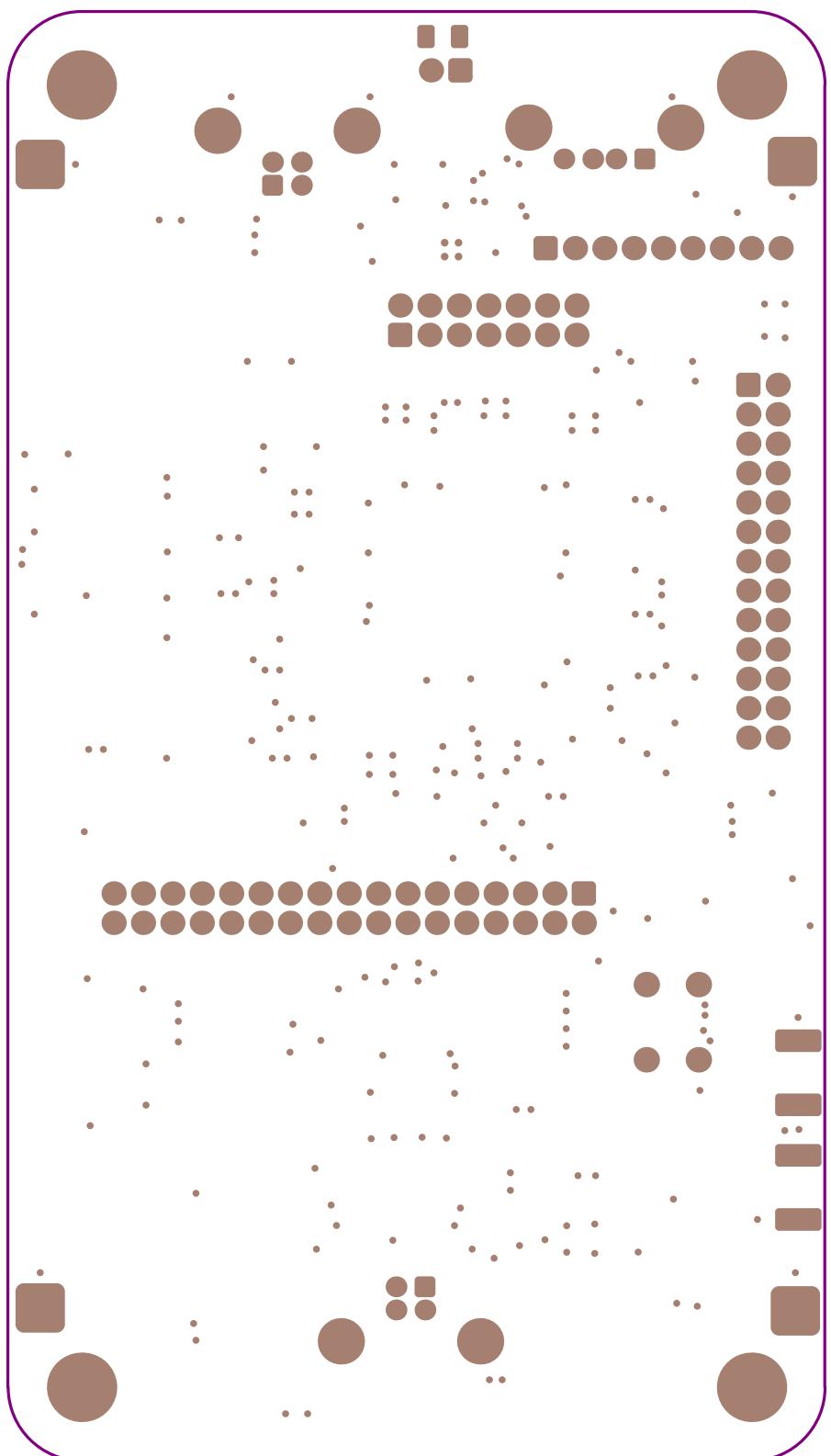


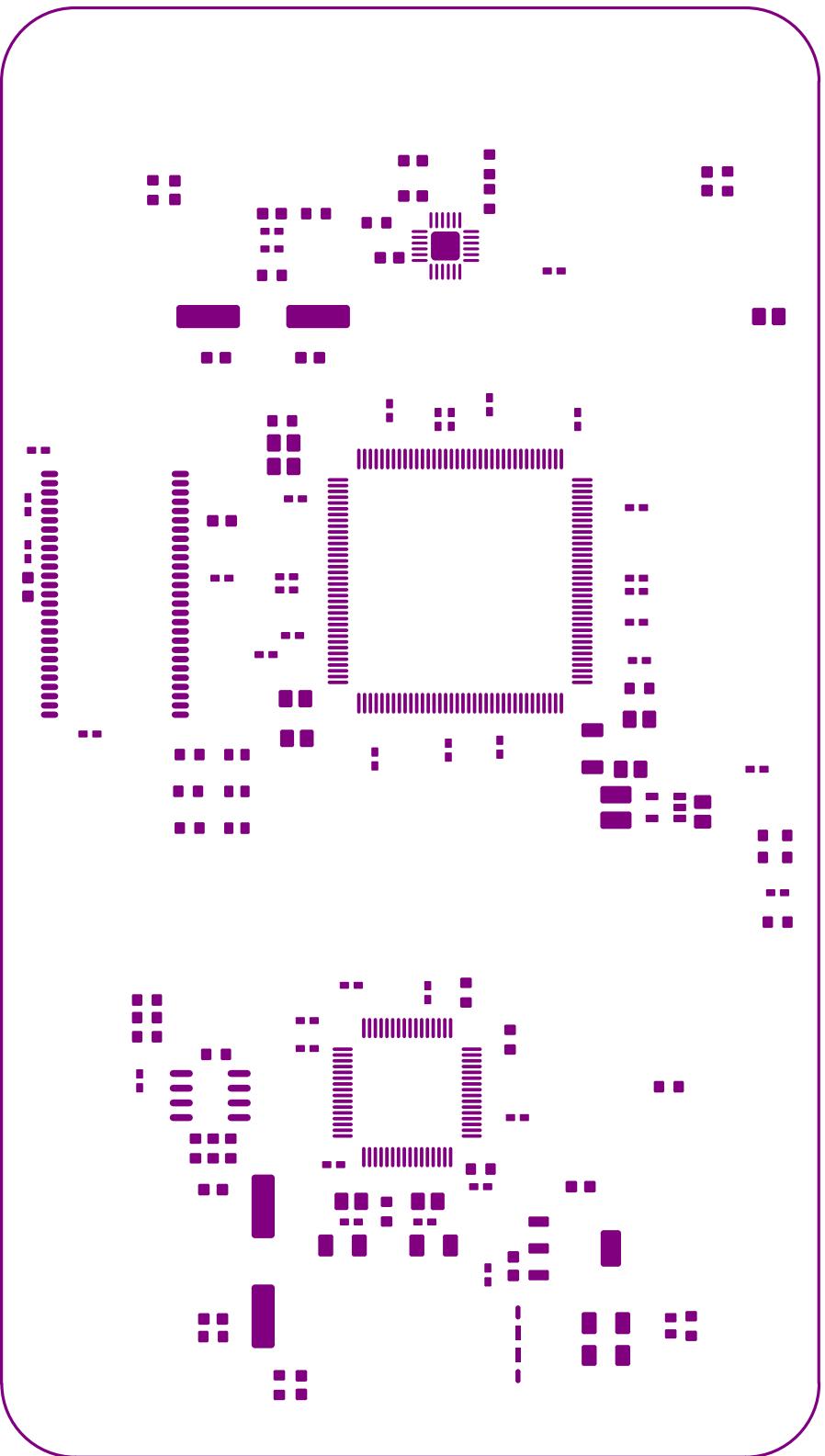


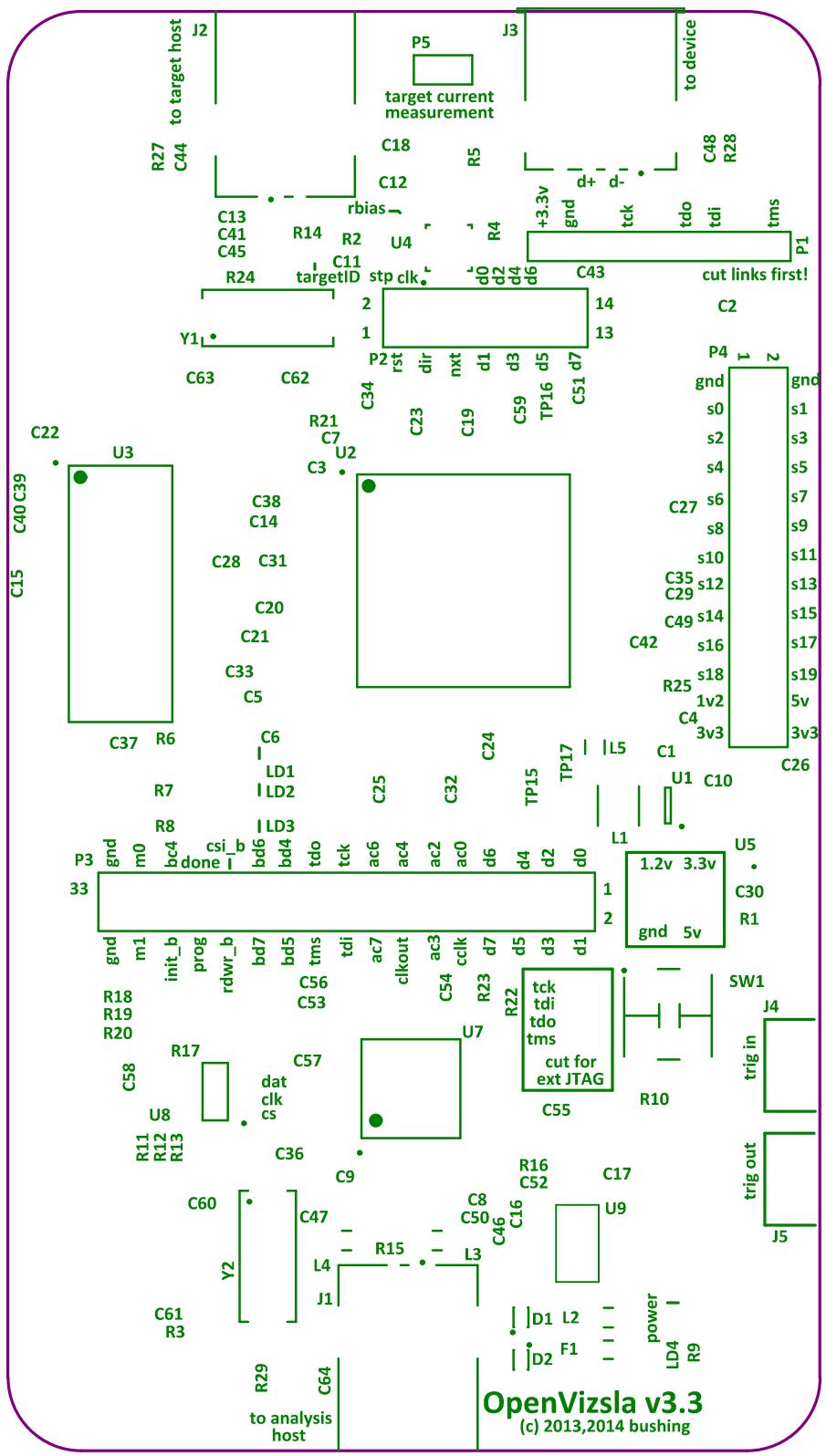












R26 -  
measuring current for  
each current source  
cut trace for

	Apns	D+	D-	Bug	Vnsps
cut links first!					
10	41	39	42	29	38
11	42	38	41	28	39
12	43	37	40	27	34
13	44	36	38	26	35
14	45	35	39	25	33
15	46	34	37	24	32
16	47	33	36	23	31
17	48	32	35	22	30
18	49	31	34	21	29
19	50	30	33	20	28
20	51	29	32	19	27
21	52	28	31	18	26
22	53	27	30	17	25
23	54	26	29	16	24
24	55	25	28	15	23
25	56	24	27	14	22
26	57	23	26	13	21
27	58	22	25	12	20
28	59	21	24	11	19
29	60	20	23	10	18
30	61	19	22	9	17
31	62	18	21	8	16
32	63	17	20	7	15
33	64	16	19	6	14
34	65	15	18	5	13
35	66	14	17	4	12
36	67	13	16	3	11
37	68	12	15	2	10
38	69	11	14	1	9
39	70	10	13		8
40	71	9	12		7
41	72	8	11		6
42	73	7	10		5
43	74	6	9		4
44	75	5	8		3
45	76	4	7		2
46	77	3	6		1
47	78	2	5		
48	79	1	4		
49	80		3		
50	81		2		
51	82		1		
52	83				



