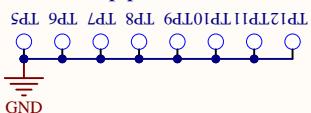
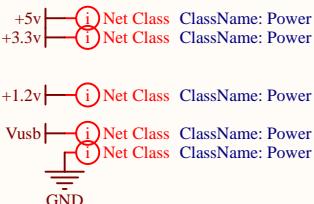
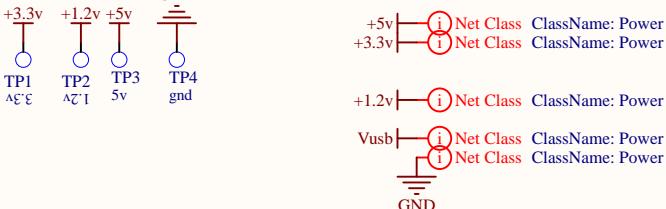
**A****B****C****D**

Ground clip pads

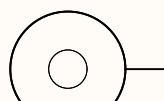
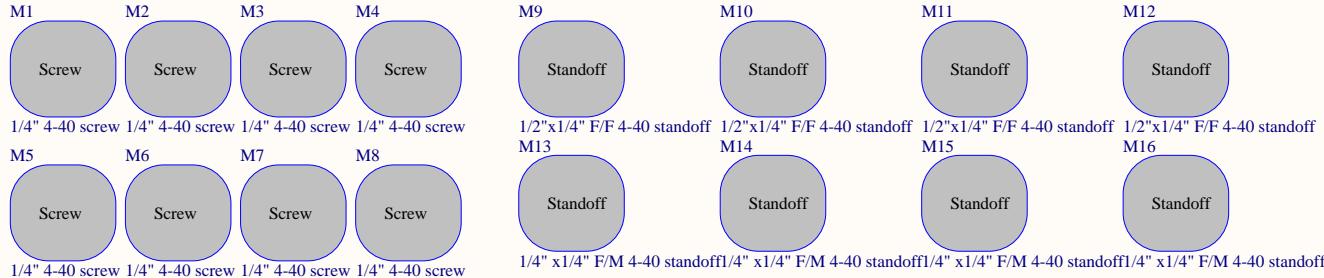


Power supply test points, top side

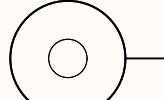


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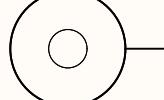
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Size	Number	Revision
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Date:	3/11/2021	Sheet of
File:	C:\Users\...\power.SchDoc	Drawn By:



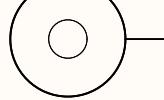
MHole3.2mm



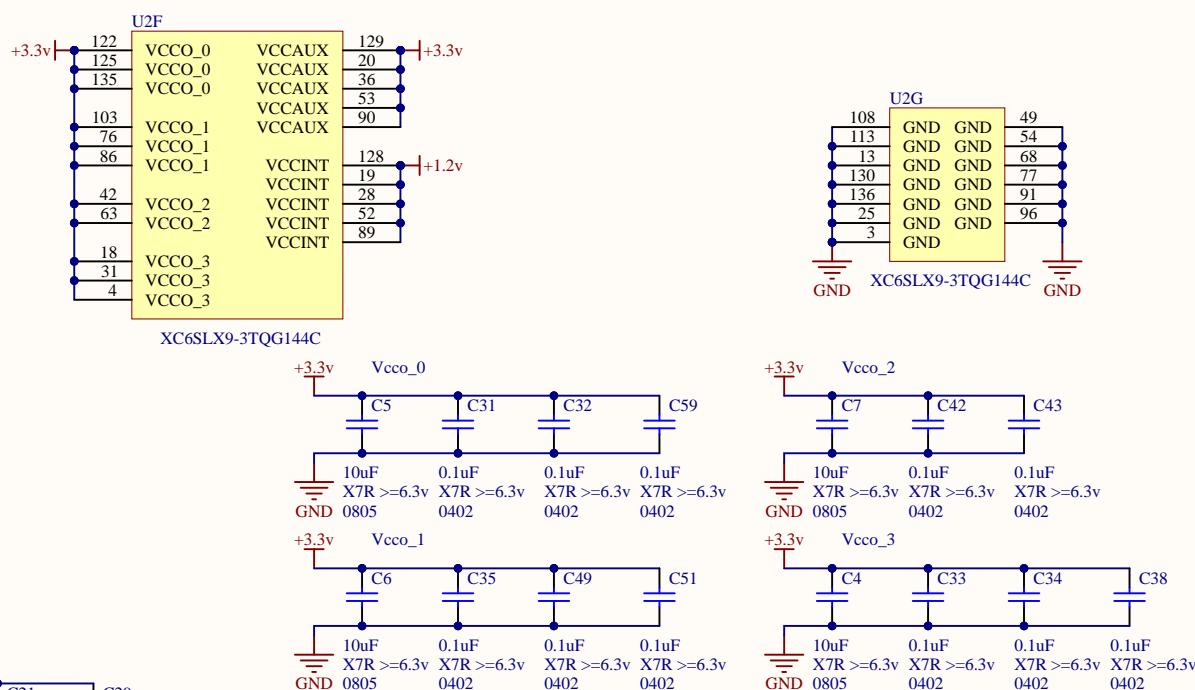
MHole3.2mm



M101CS.ZMM



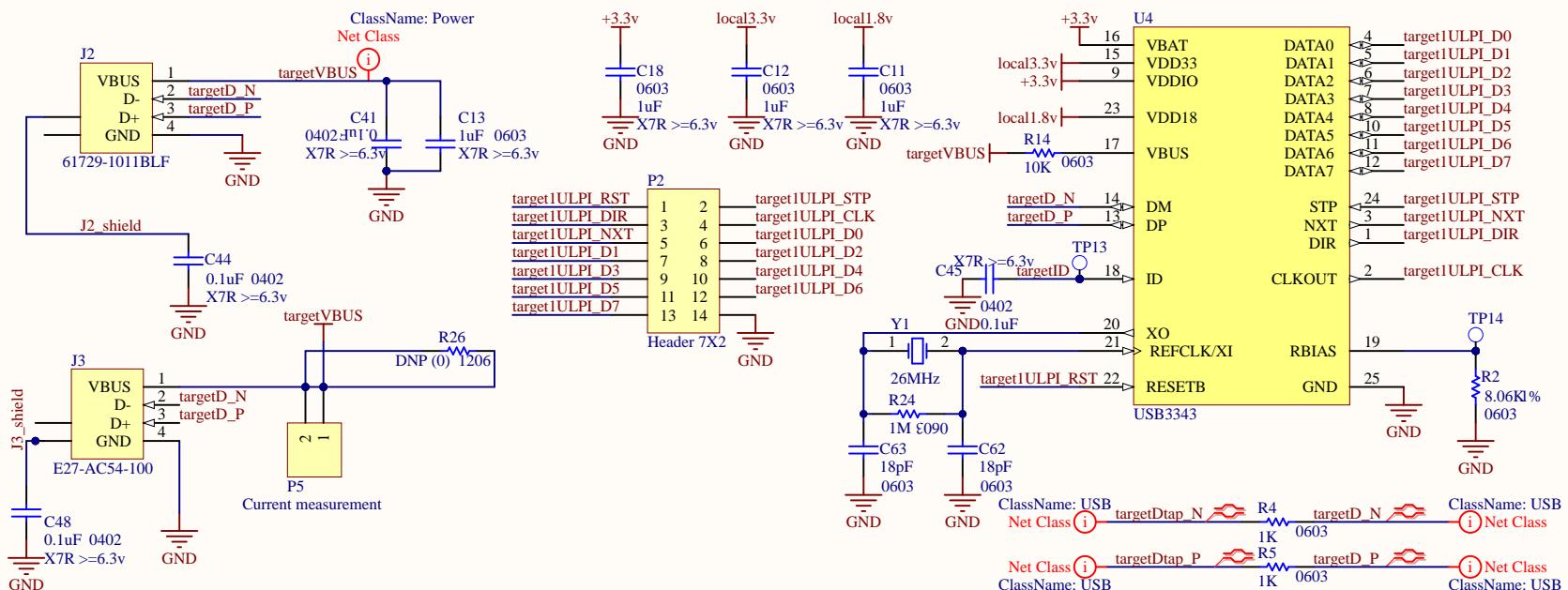
MHole3.2mm



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Date:	3/11/2021	Sheet 2 of
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A

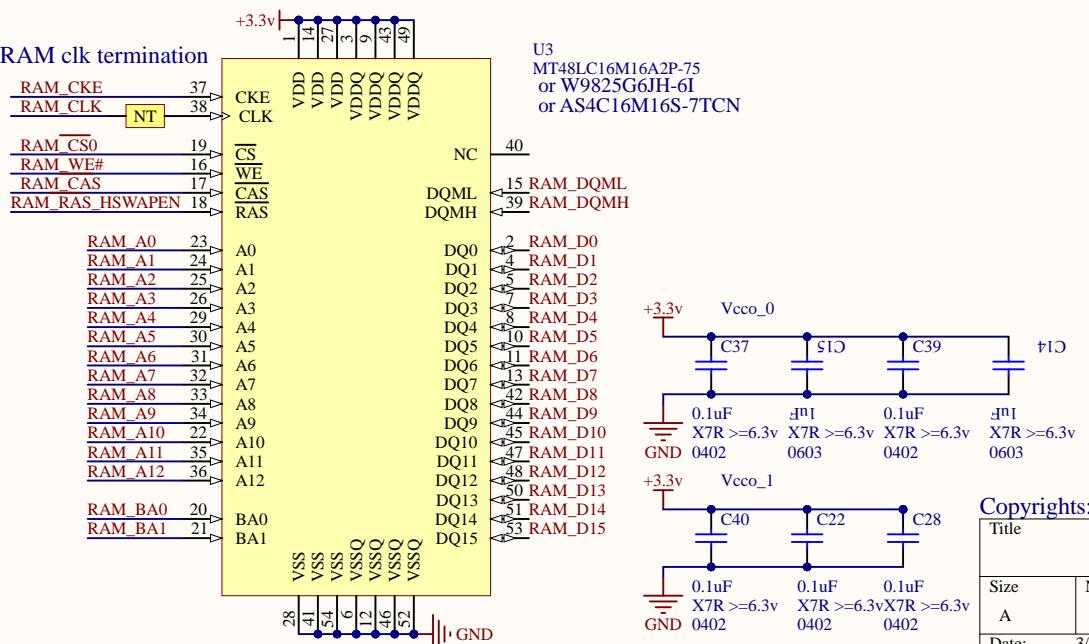


B

A

B

optional RAM clk termination



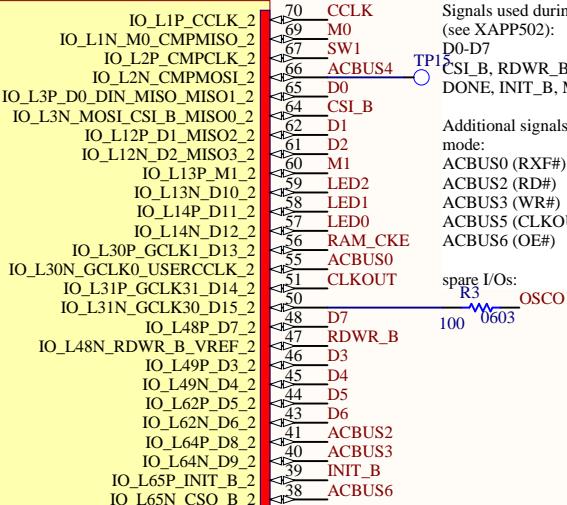
C

C

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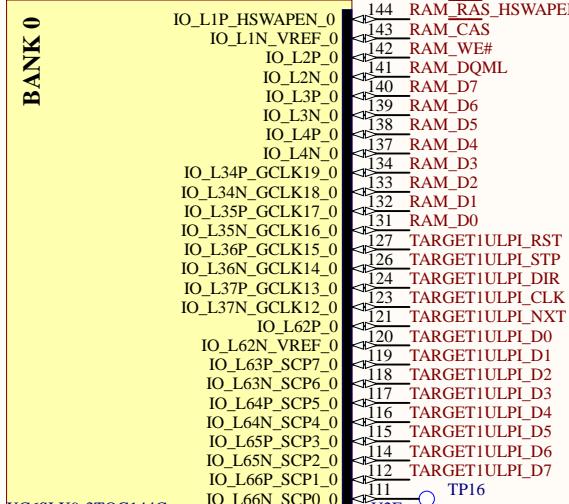
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File: C:\Users\...\RAM and target USB.SchDoc	Drawn By:	

U2C

BANK 2

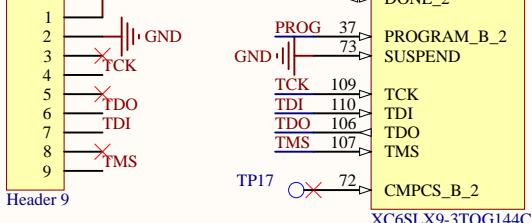
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U2A



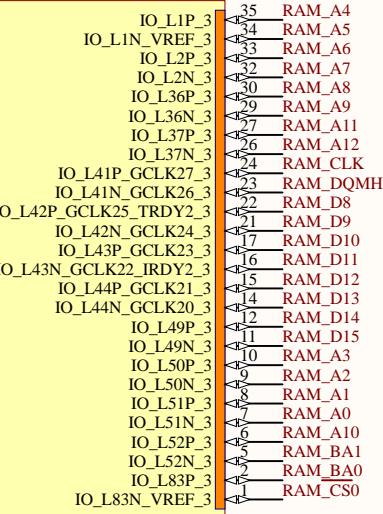
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P1

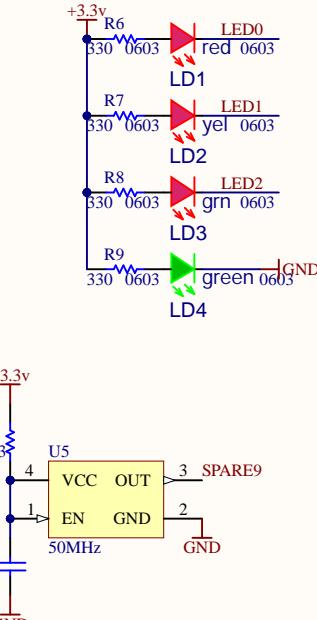


XC6SLX9-3TQG144C

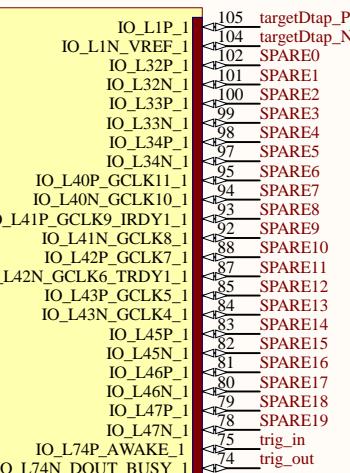
U2D

BANK 3

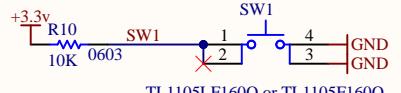
XC6SLX9-3TQG144C



Spare 50MHz clock for bringup

BANK 1

XC6SLX9-3TQG144C

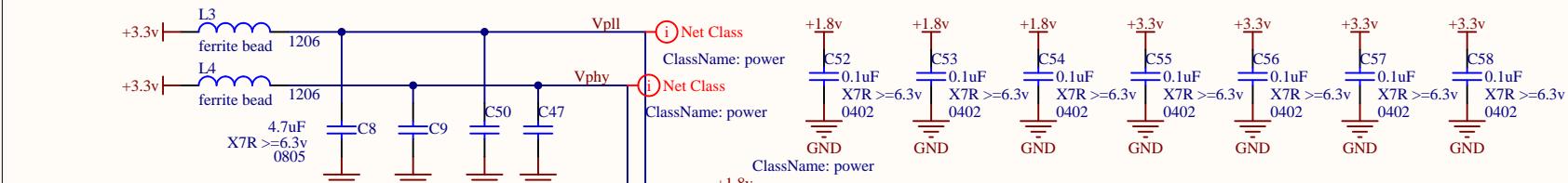


TL1105LF160Q or TL1105F160Q

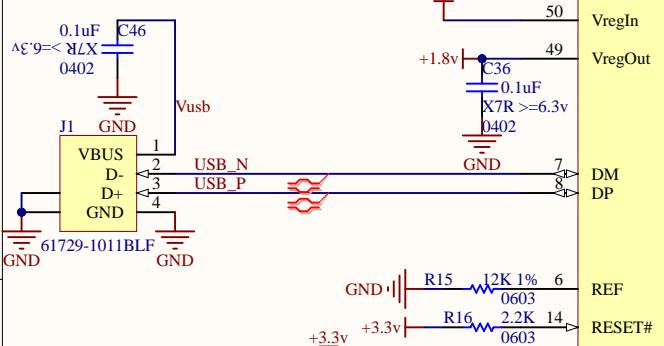
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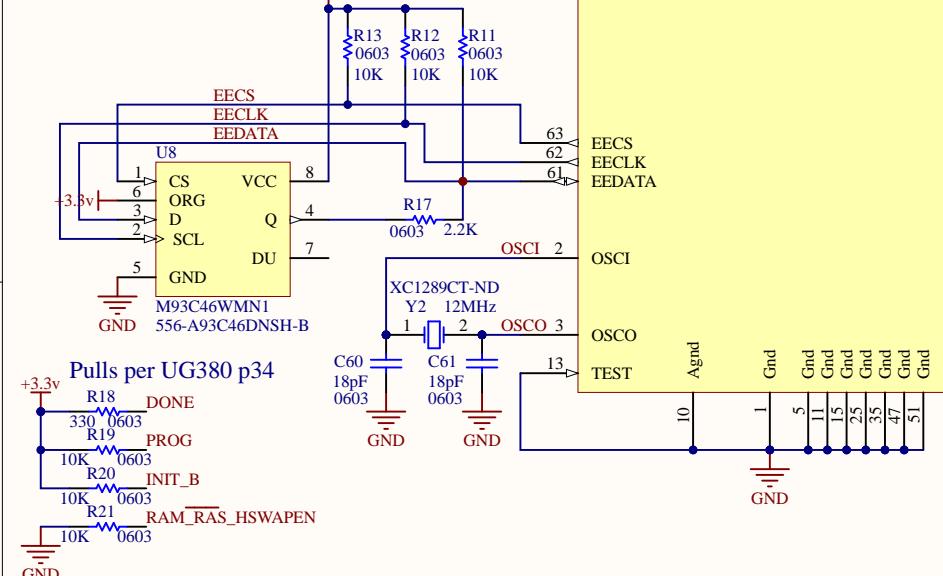
A



B



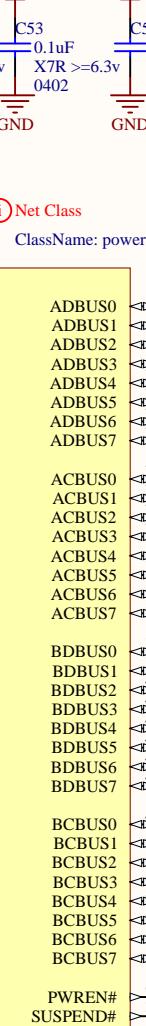
C



Pulls per UG380 p34

+3.3v
R18 DONE
330 0603
R19 PROG
10K 0603
R20 INIT_B
10K 0603
R21 RAM_RAS_HSWAPEN
10K 0603
GND

FT2232H

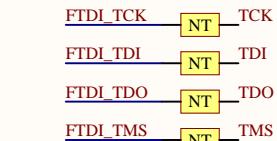
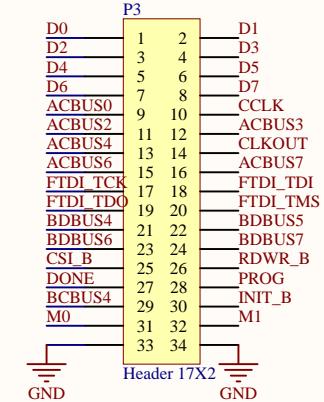


Configuration / FIFO to FPGA

Signals used during FPGA configuration
(see XAPP502):
D0-D7
CSI_B, RDWR_B, CCLK, PROG_B,
DONE, INIT_B, M0, M1

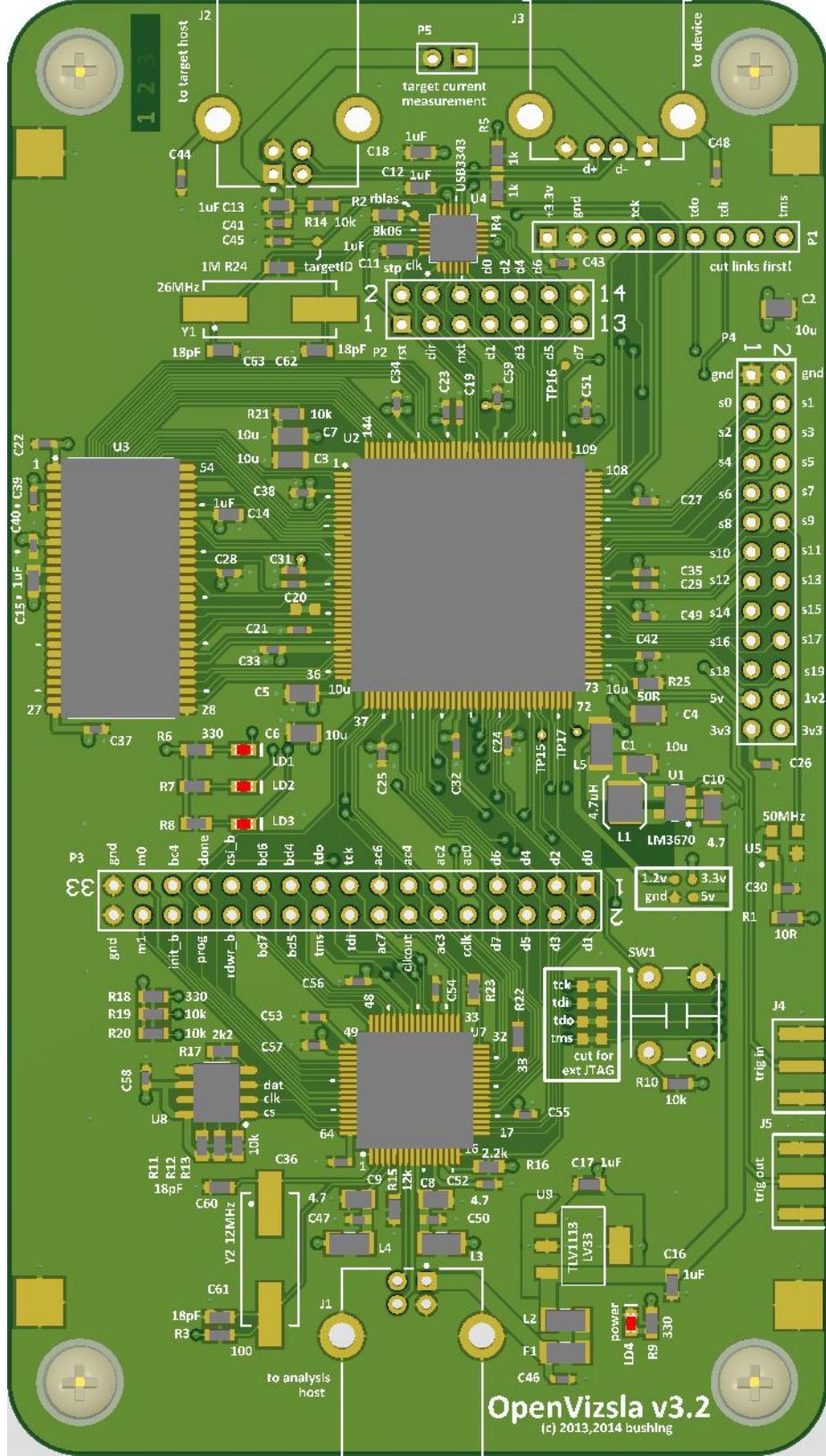
Additional signals used during FIFO mode:
ACBUS0 (RXF#)
ACBUS2 (RD#)
ACBUS3 (WR#)
ACBUSS (CLKOUT)
ACBUS6 (OE#)

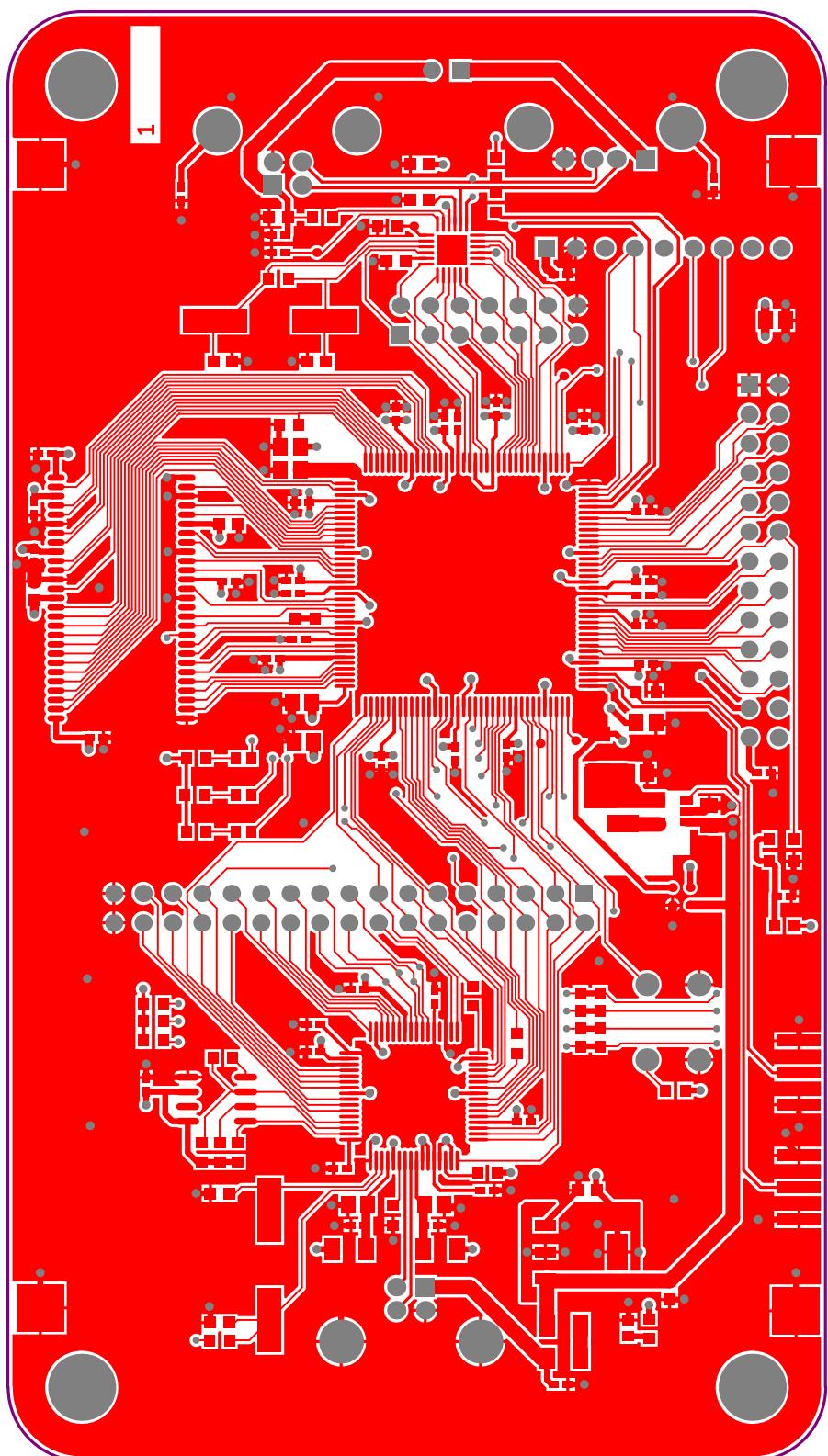
spare I/Os:

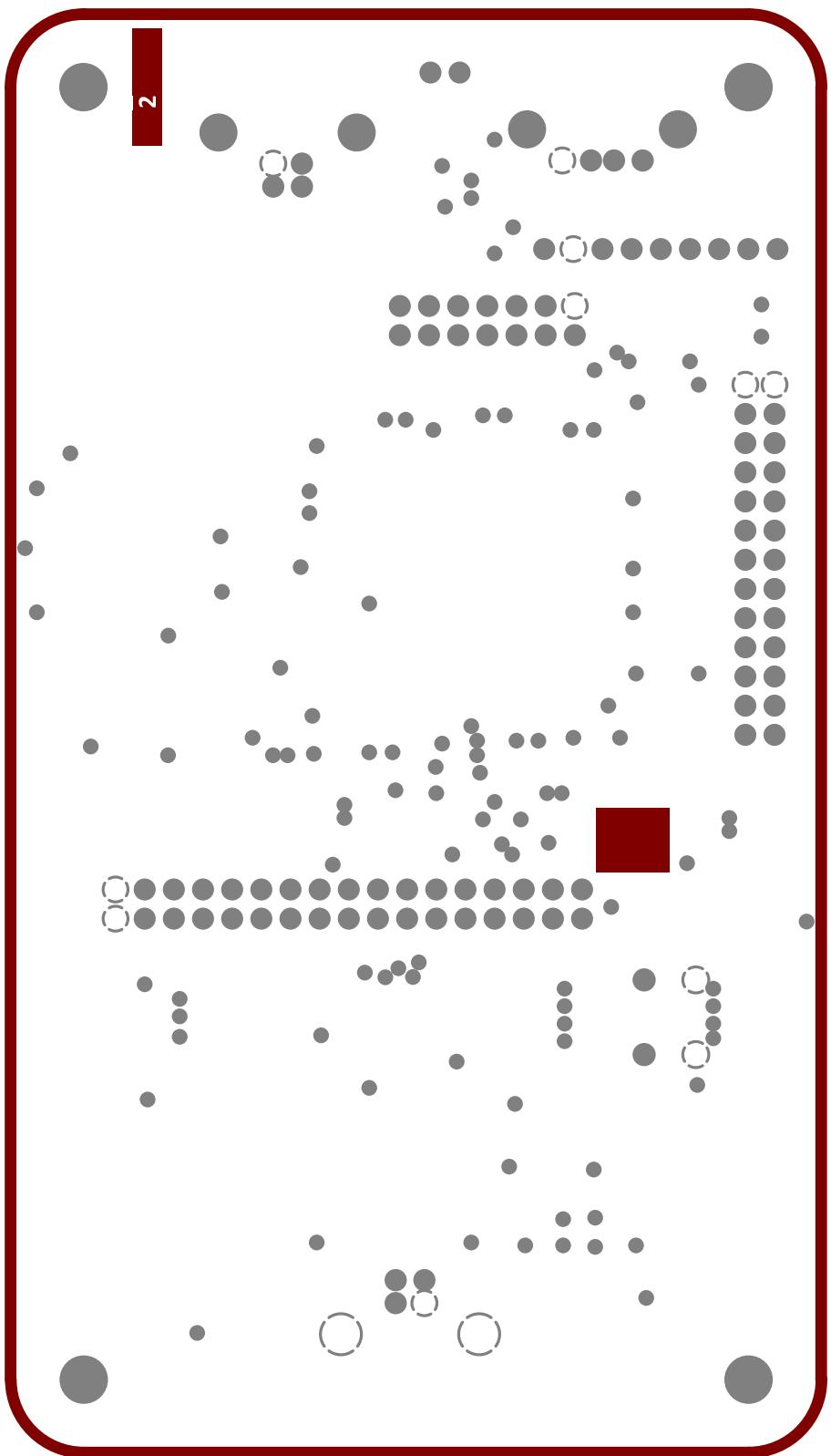


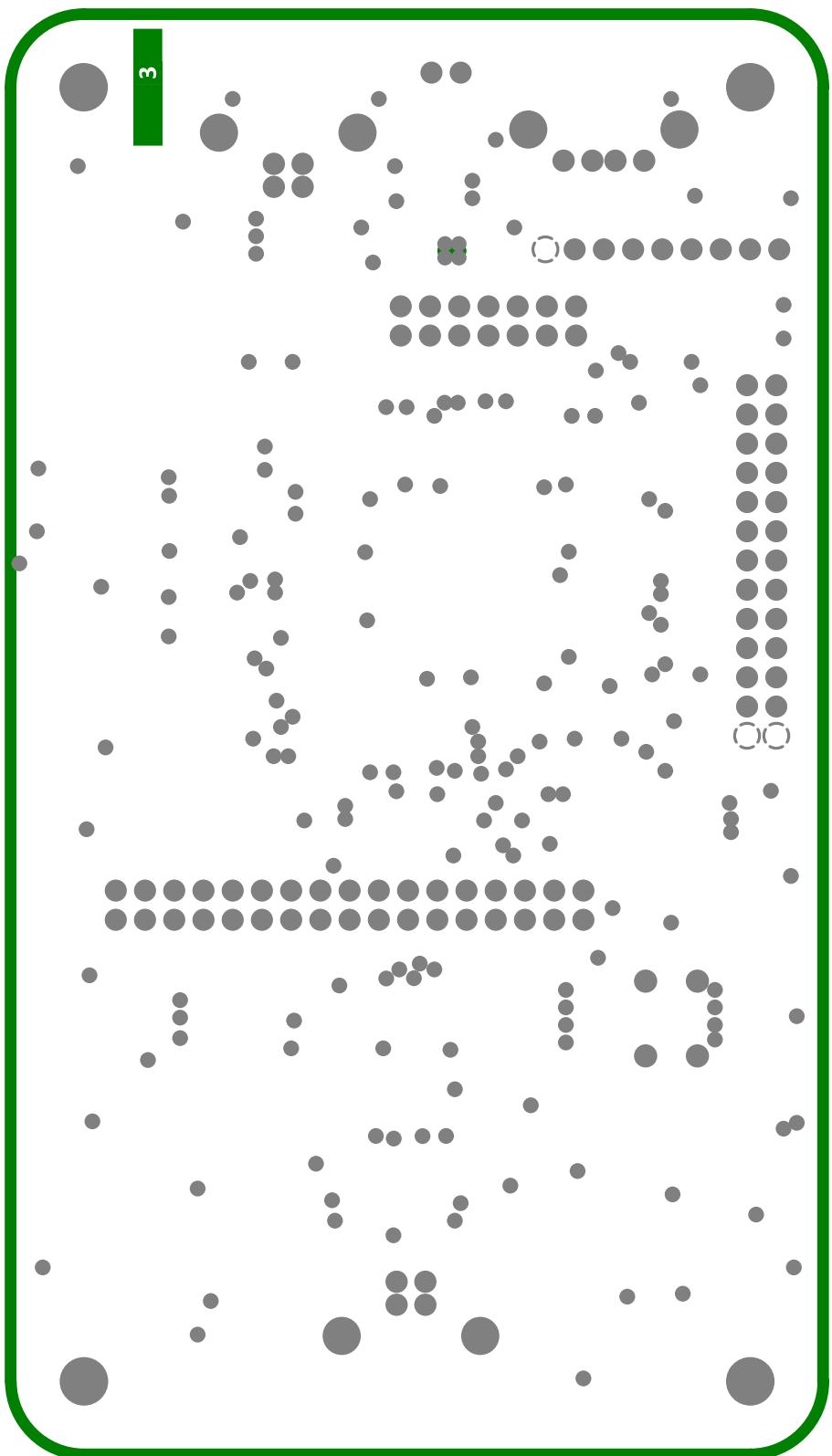
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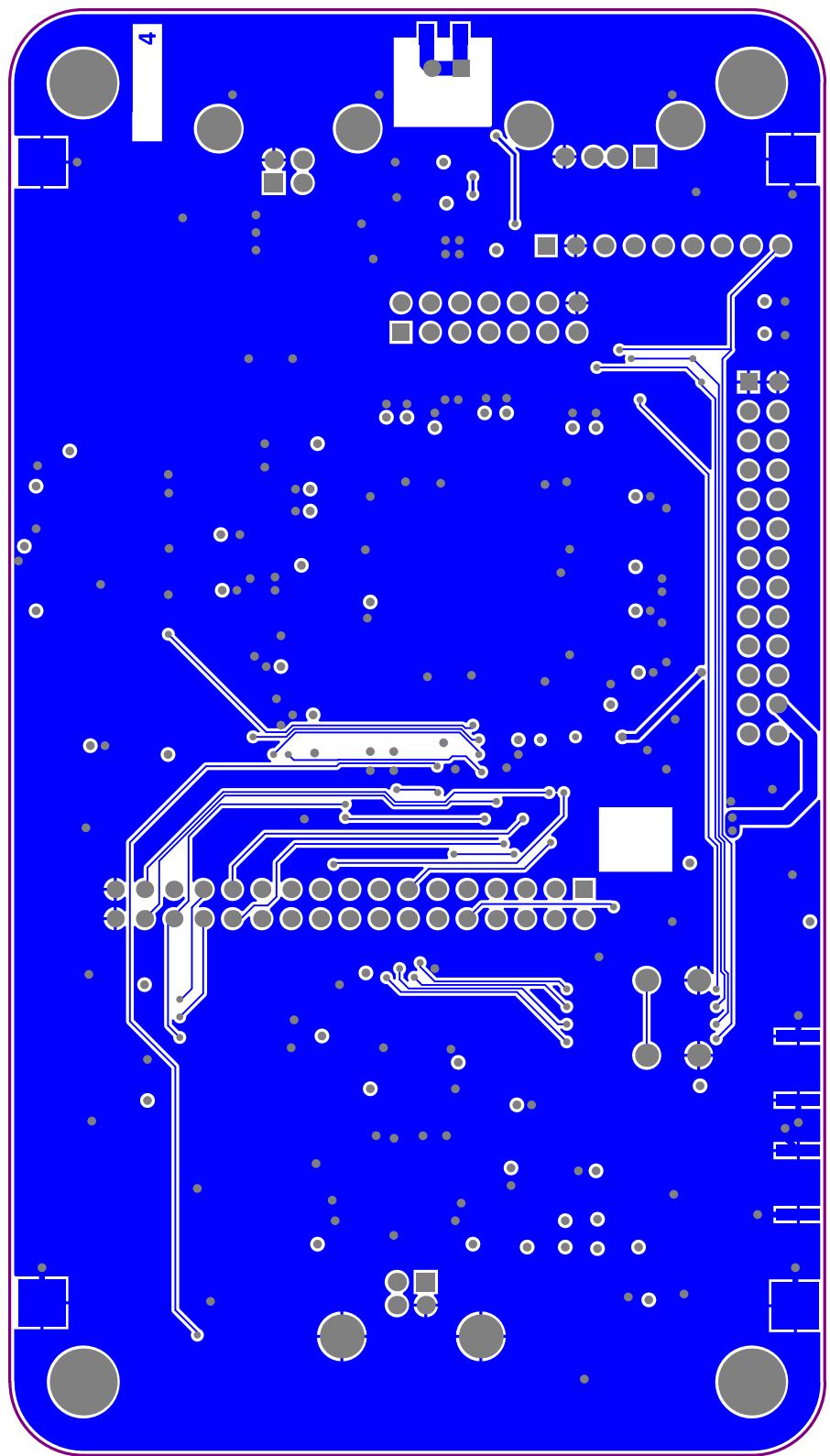
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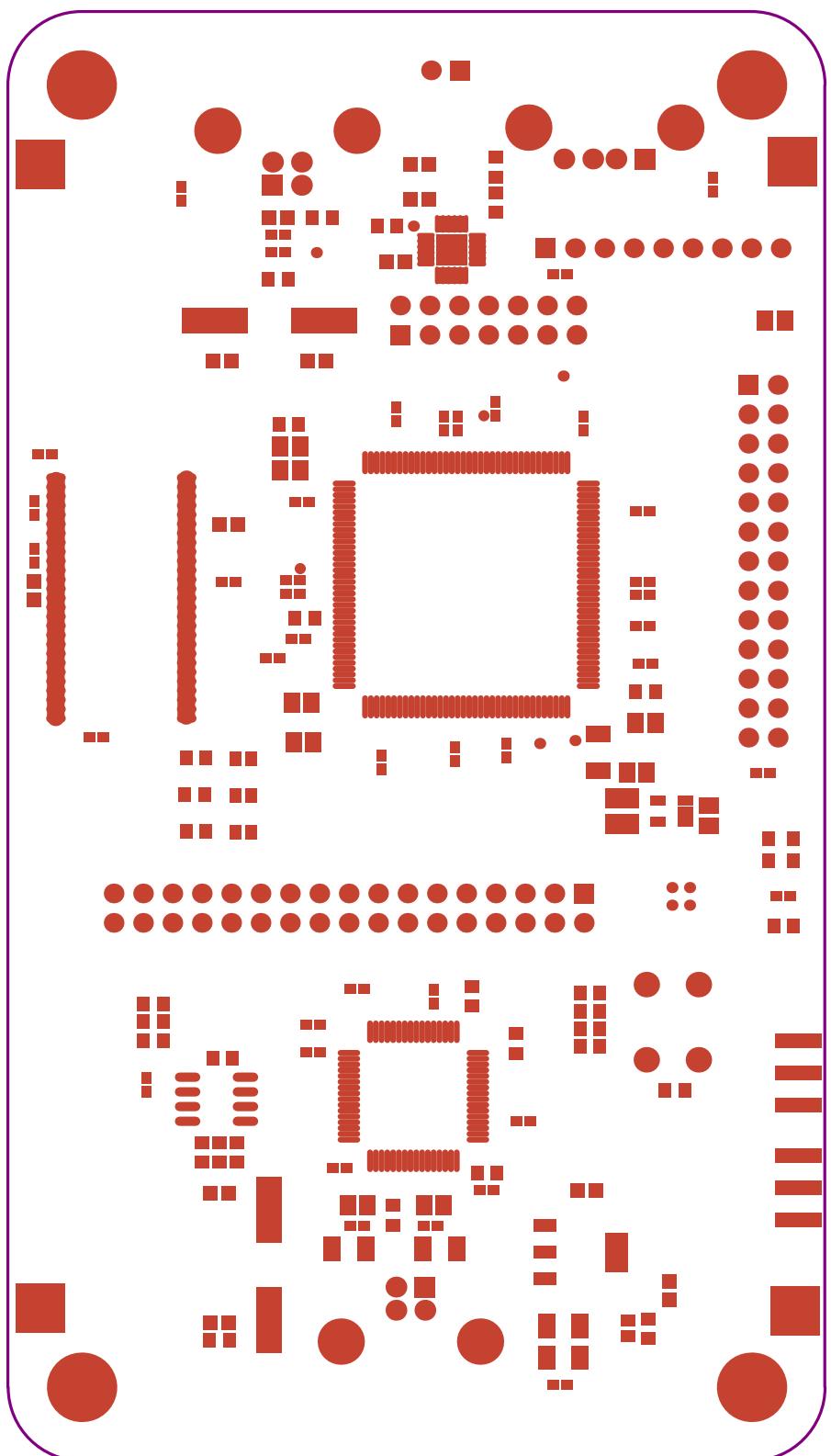


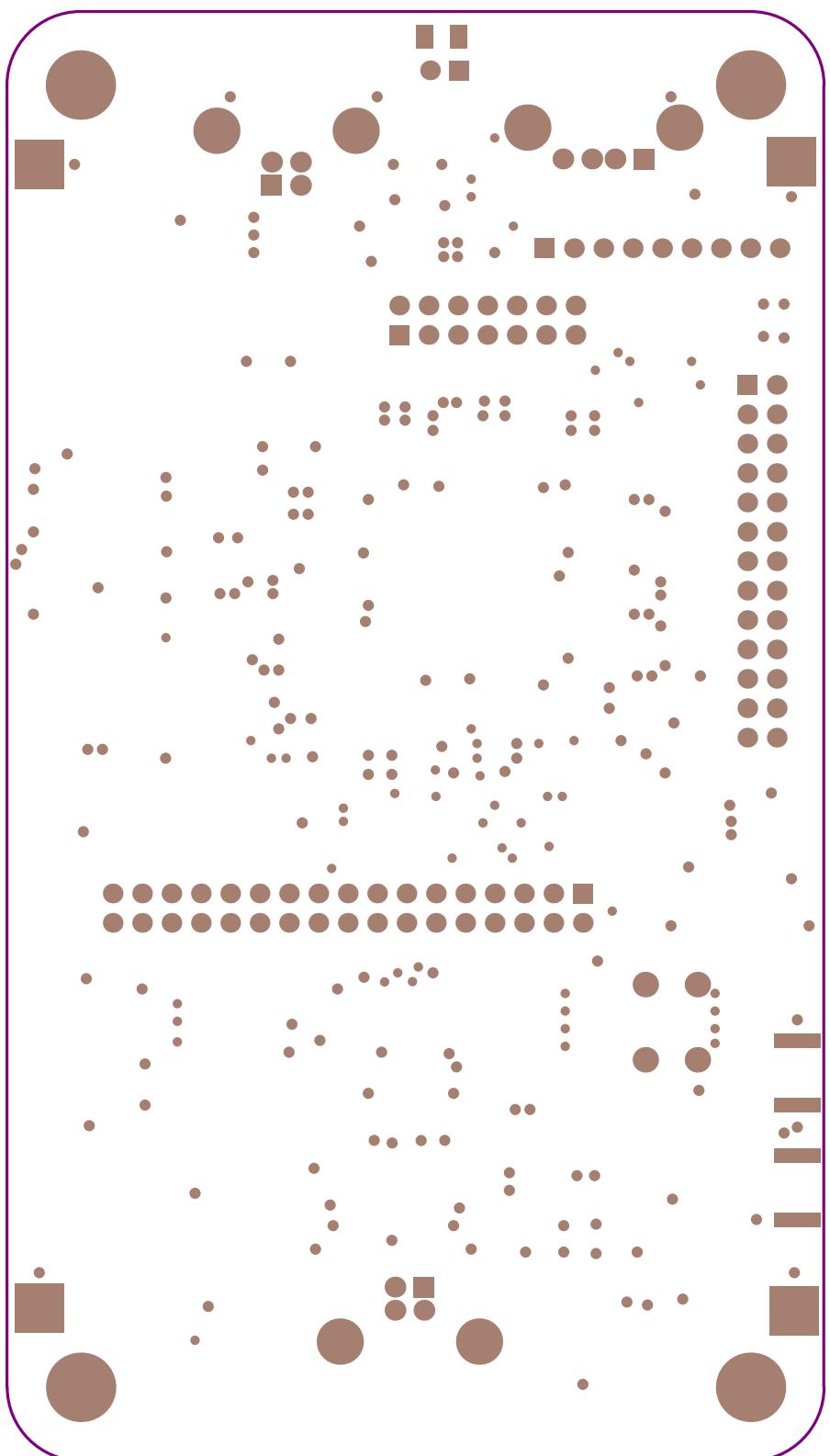


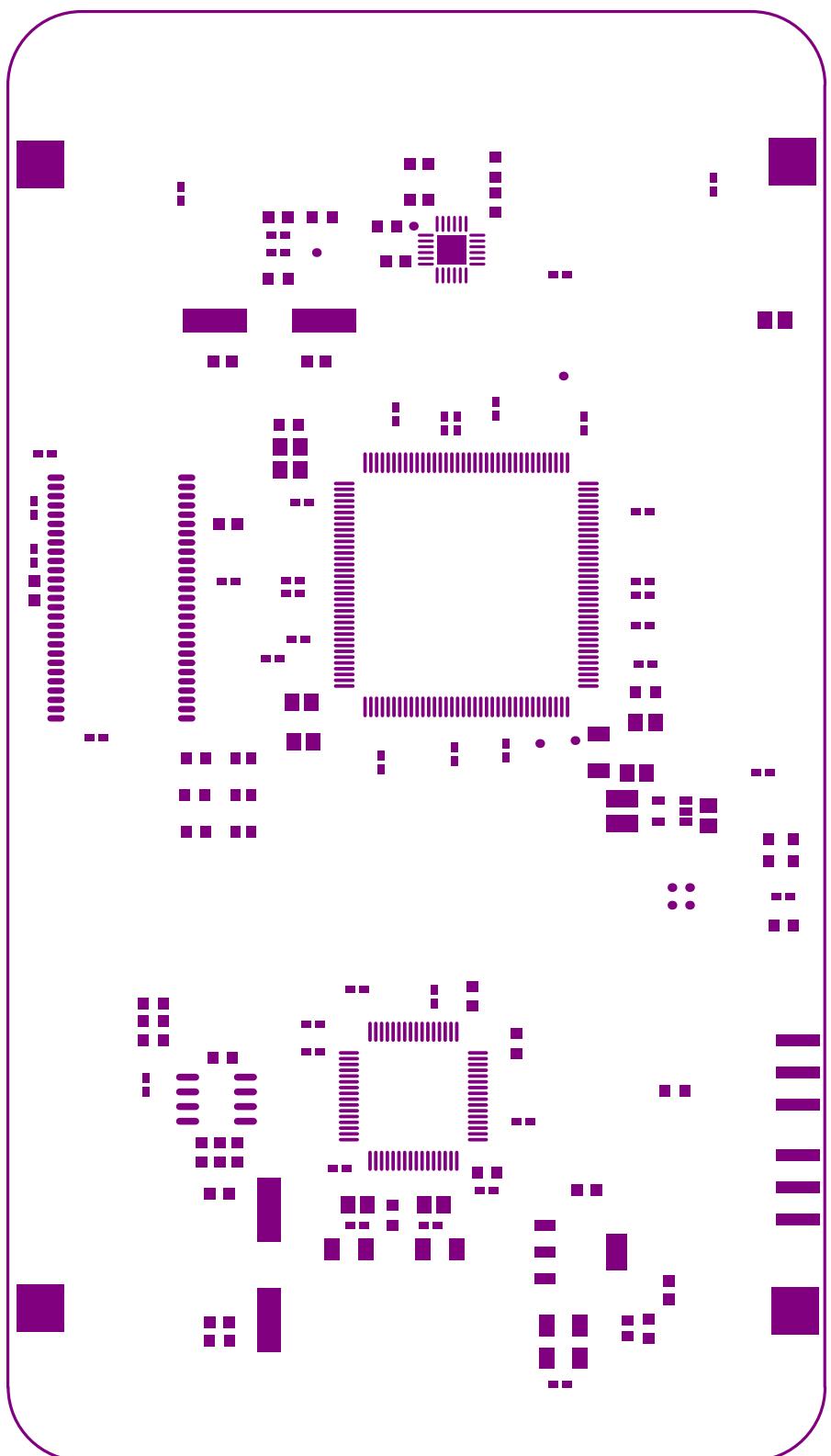


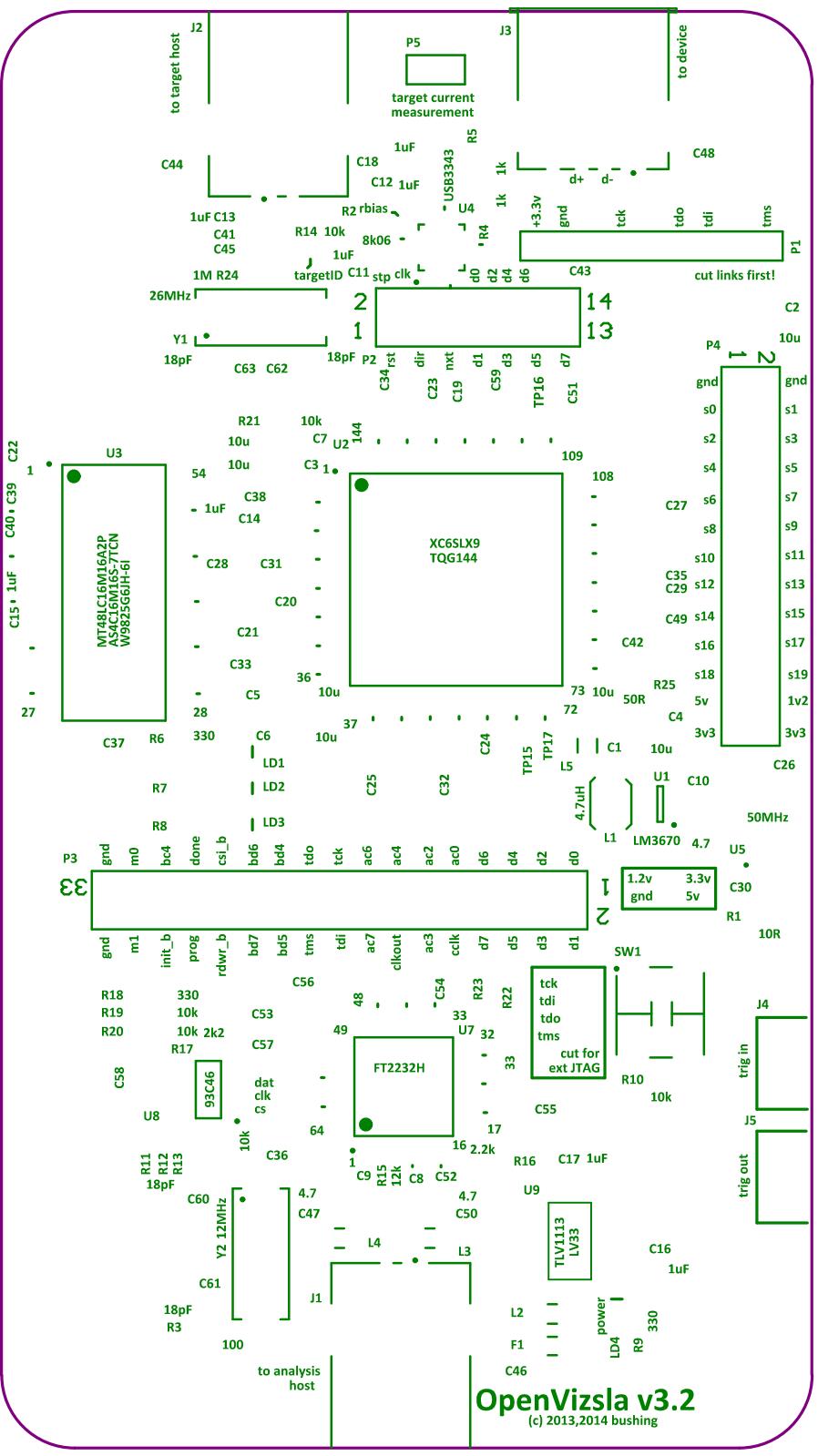












measures must be taken to
ensure that the
target audience
can take full
advantage of
the new measure.

Apns
D-
D+

smf
ibt
obj

q
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k
b
o
d
q

fcjk

bng	bng
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১২	১১
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০১১	১০১
১১১	১১১

9c4	9c5	9c6	9c7	9c8	9c9	9c10
9c11	9c12	9c13	9c14	9c15	9c16	9c17
9c18	9c19	9c20	9c21	9c22	9c23	9c24
9c25	9c26	9c27	9c28	9c29	9c30	9c31
9c32	9c33	9c34	9c35	9c36	9c37	9c38

cikonf

class	classe
clone	clonar
code	código
model	modelo
group	grupo
single	único
multiple	múltiplo
binary	binário
queue	fila
stack	pilha

10



