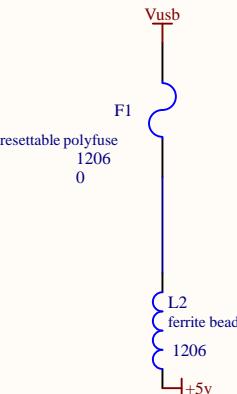
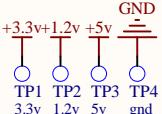


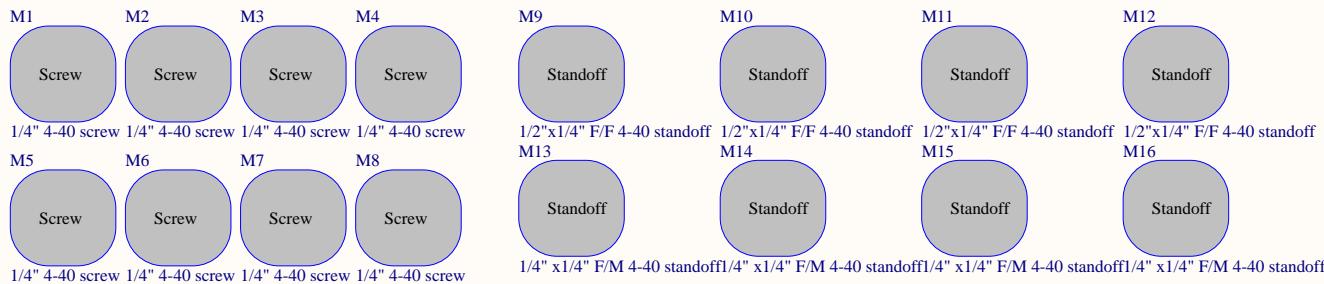
Power supply test points, top side



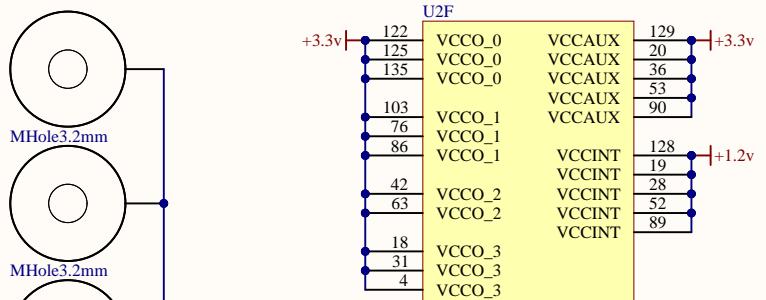
Copyrights: CC-BY-SA 3.0 Patents: Apache 2.0

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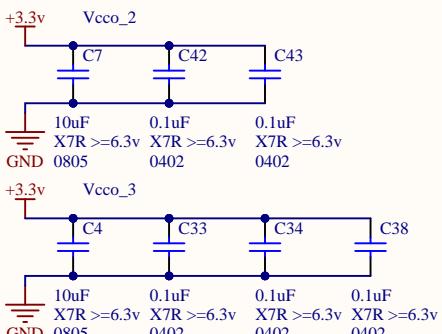
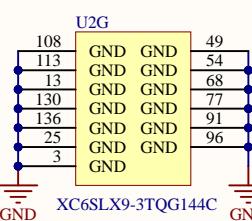
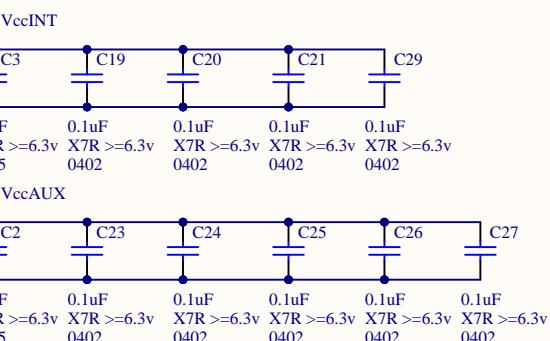
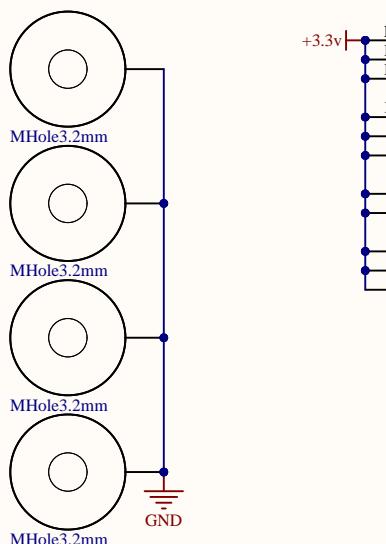
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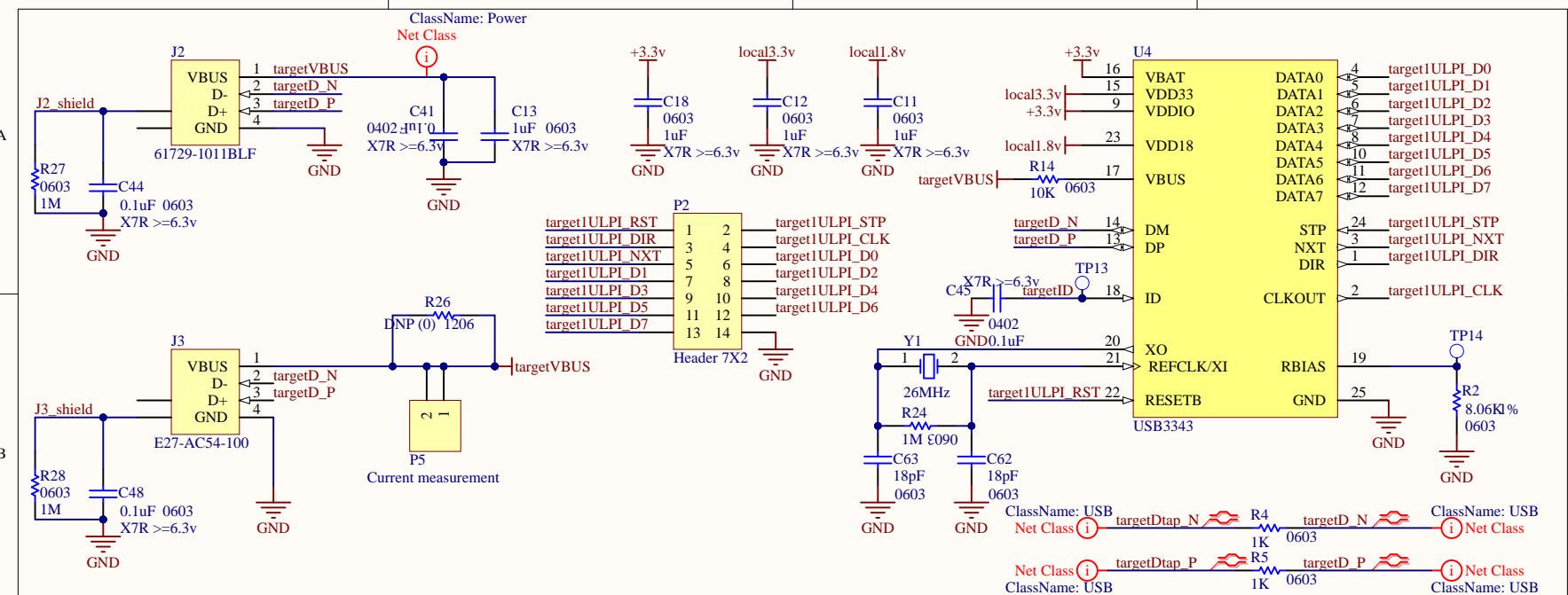


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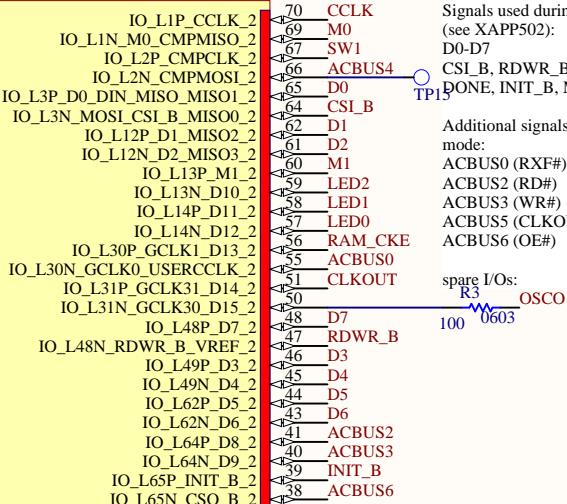
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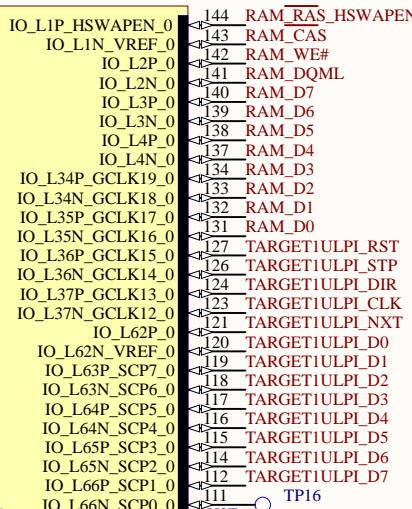
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U2C

**BANK 2**

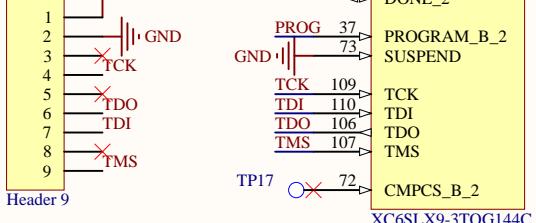
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U2A

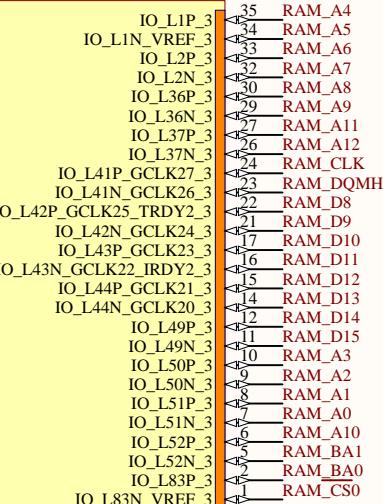


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P1

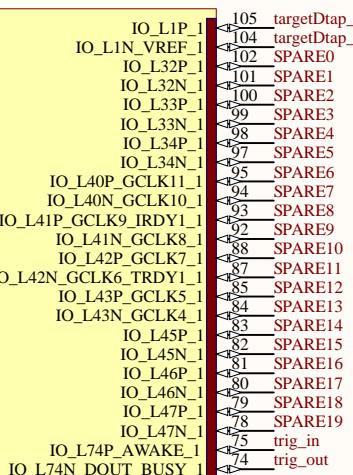


U2D

**BANK 3**

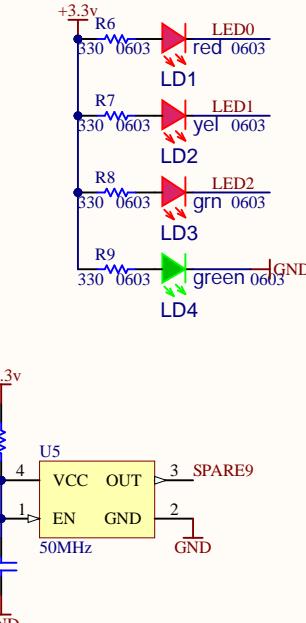
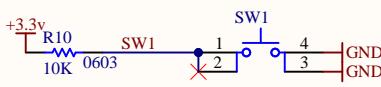
XC6SLX9-3TQG144C

U2B

**BANK 1**

XC6SLX9-3TQG144C

TL1105LF160Q or TL1105F160Q

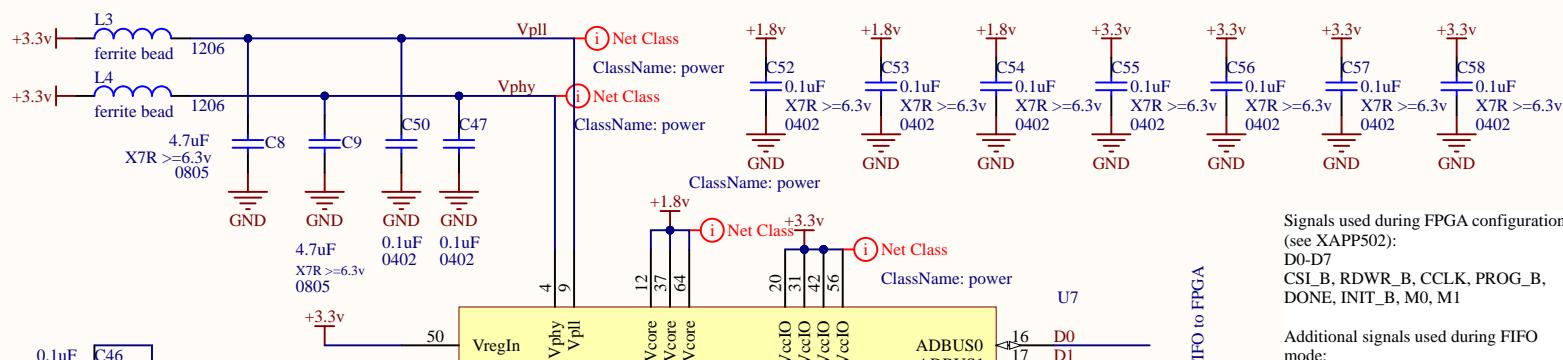


Spare 50MHz clock for bringup

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Title		Revision
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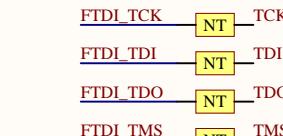
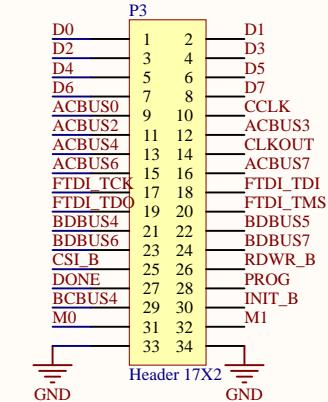
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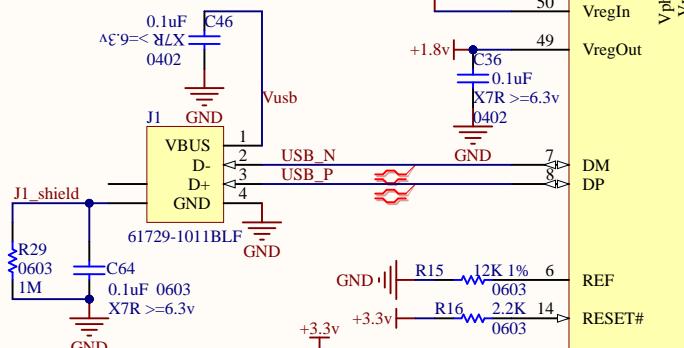
Signals used during FPGA configuration  
(see XAPP502):  
D0-D7  
CSI\_B, RDWR\_B, CCLK, PROG\_B,  
DONE, INIT\_B, M0, M1

Additional signals used during FIFO mode:  
ACBUS0 (RXF#)  
ACBUS2 (RD#)  
ACBUS3 (WR#)  
ACBU5 (CLKOUT)  
ACBUS6 (OE#)

spare I/Os:

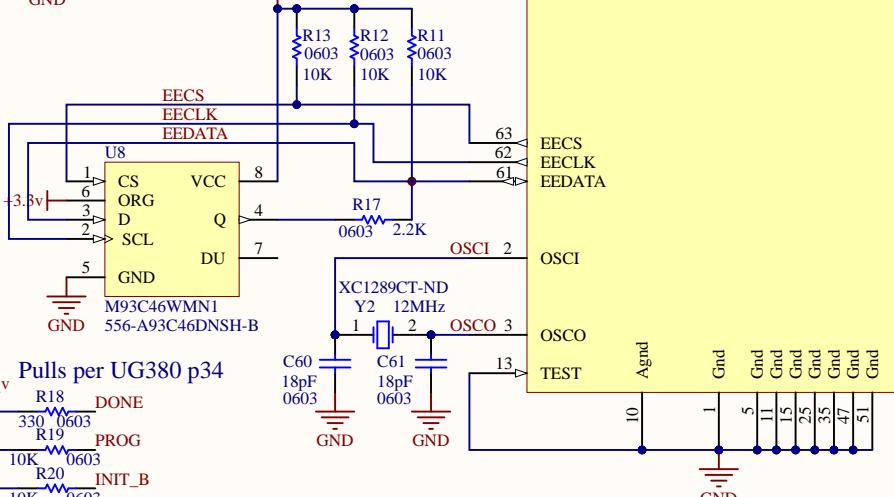


B



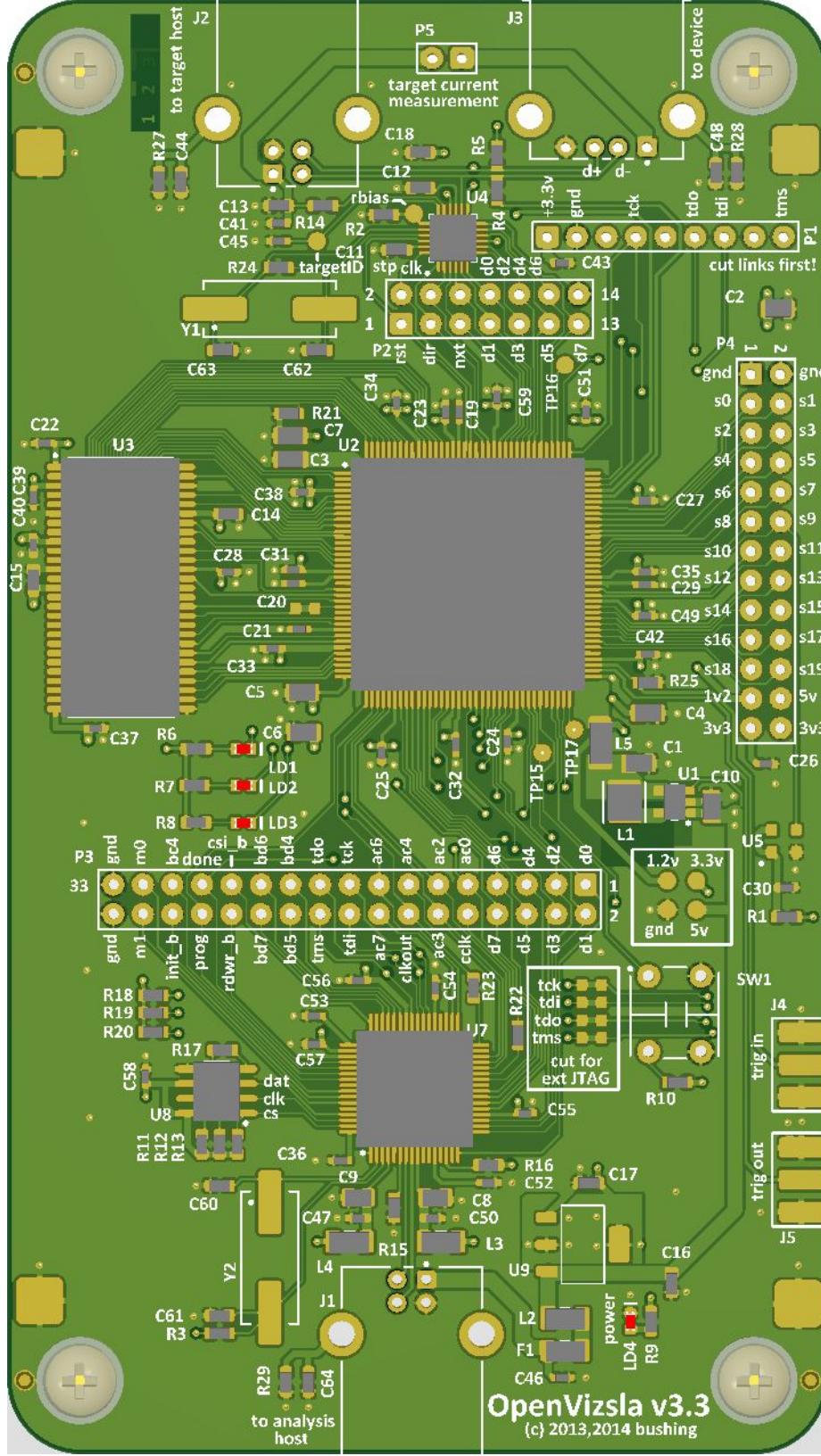
FT2232H

C

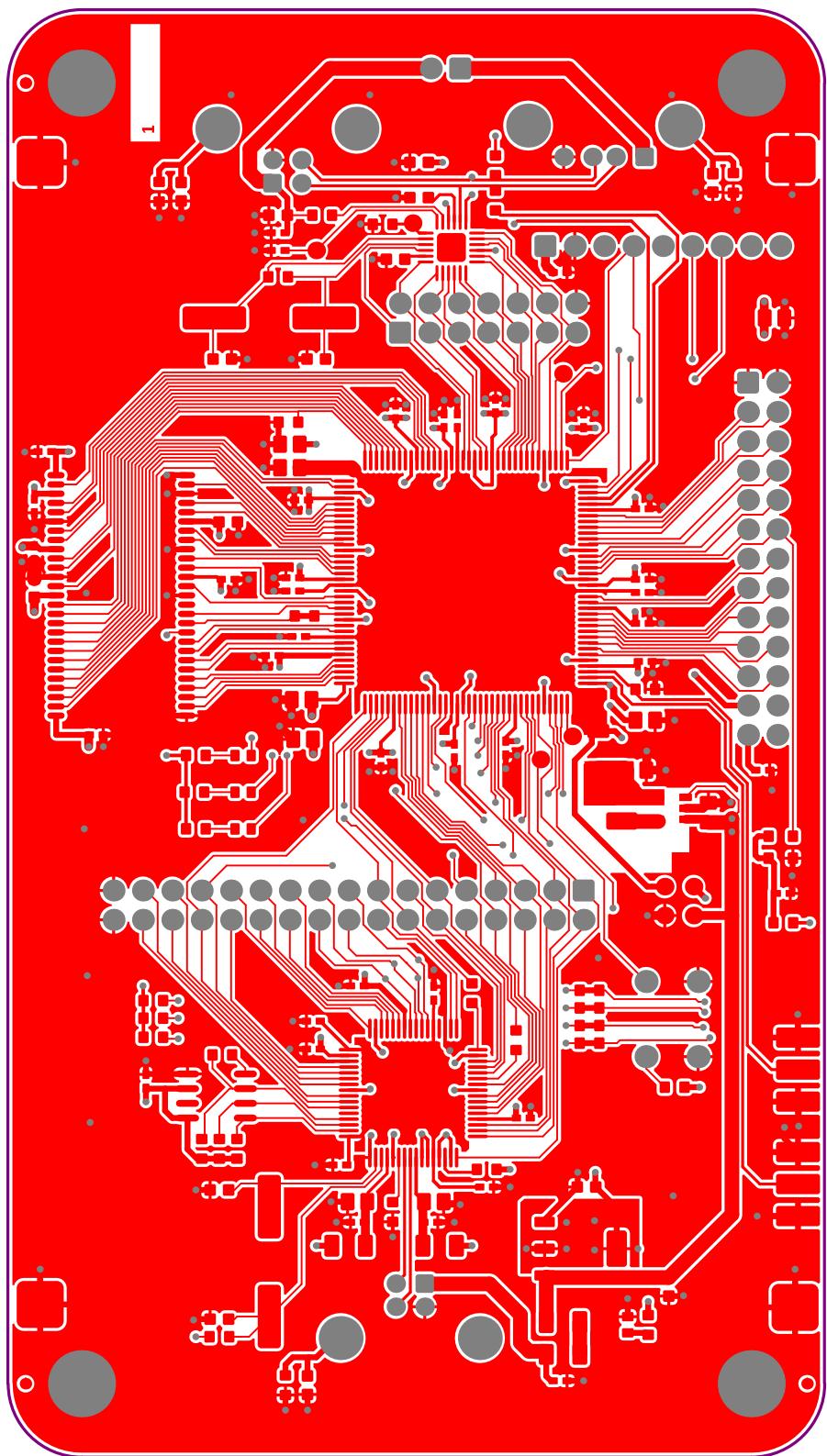


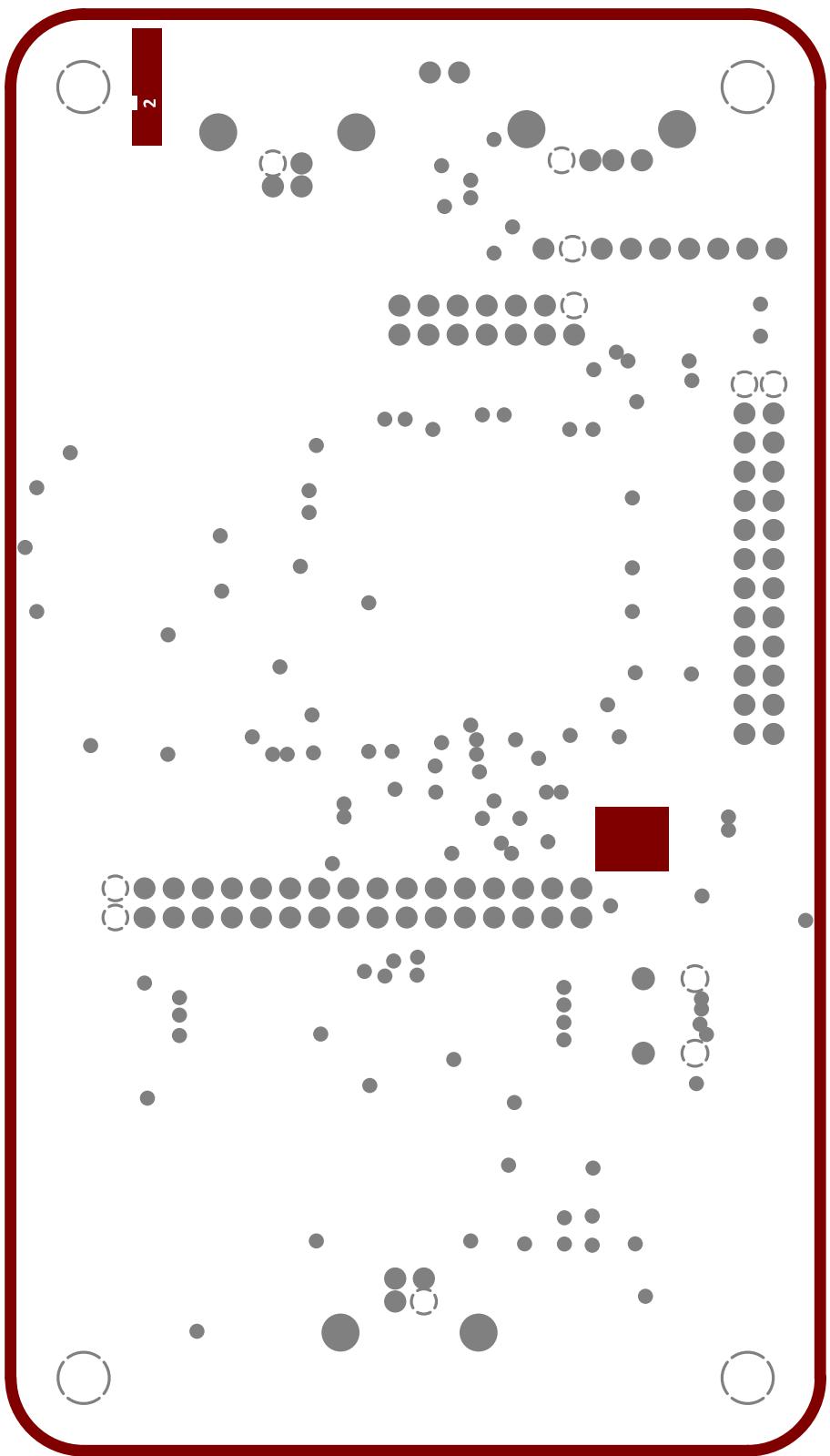
Copyrights: CC-BY-SA 3.0 Patents: Apache 2.0

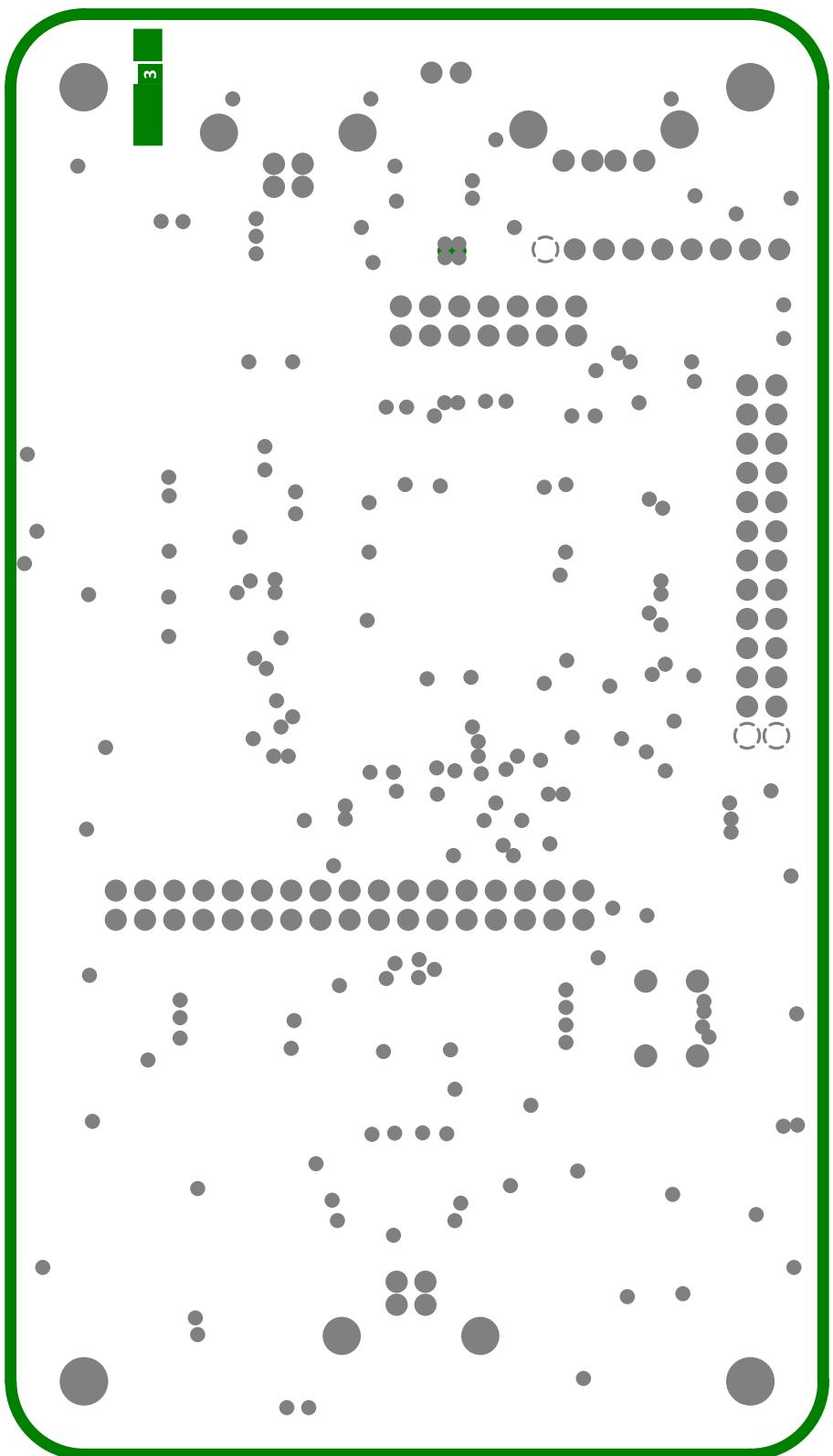
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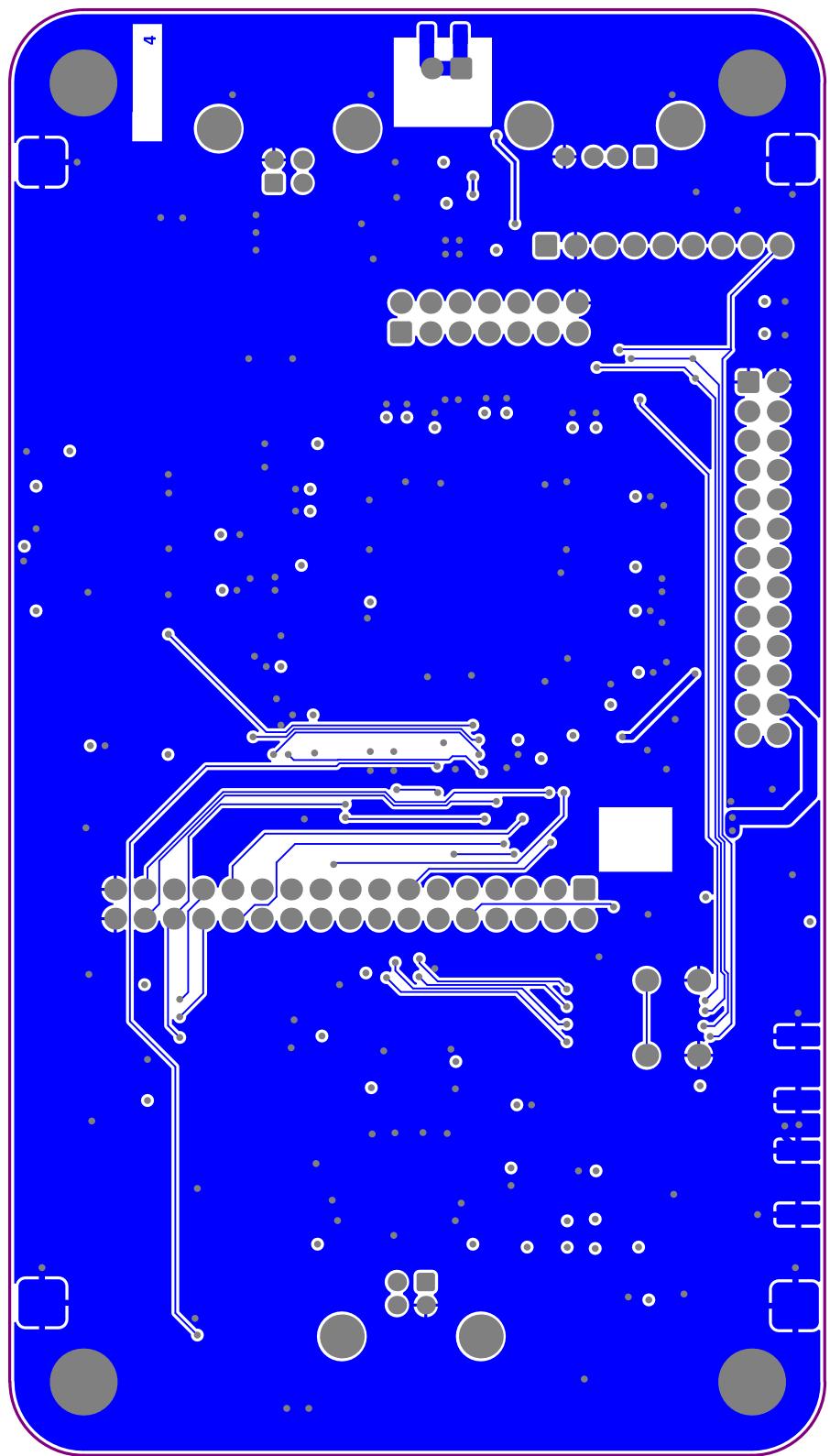


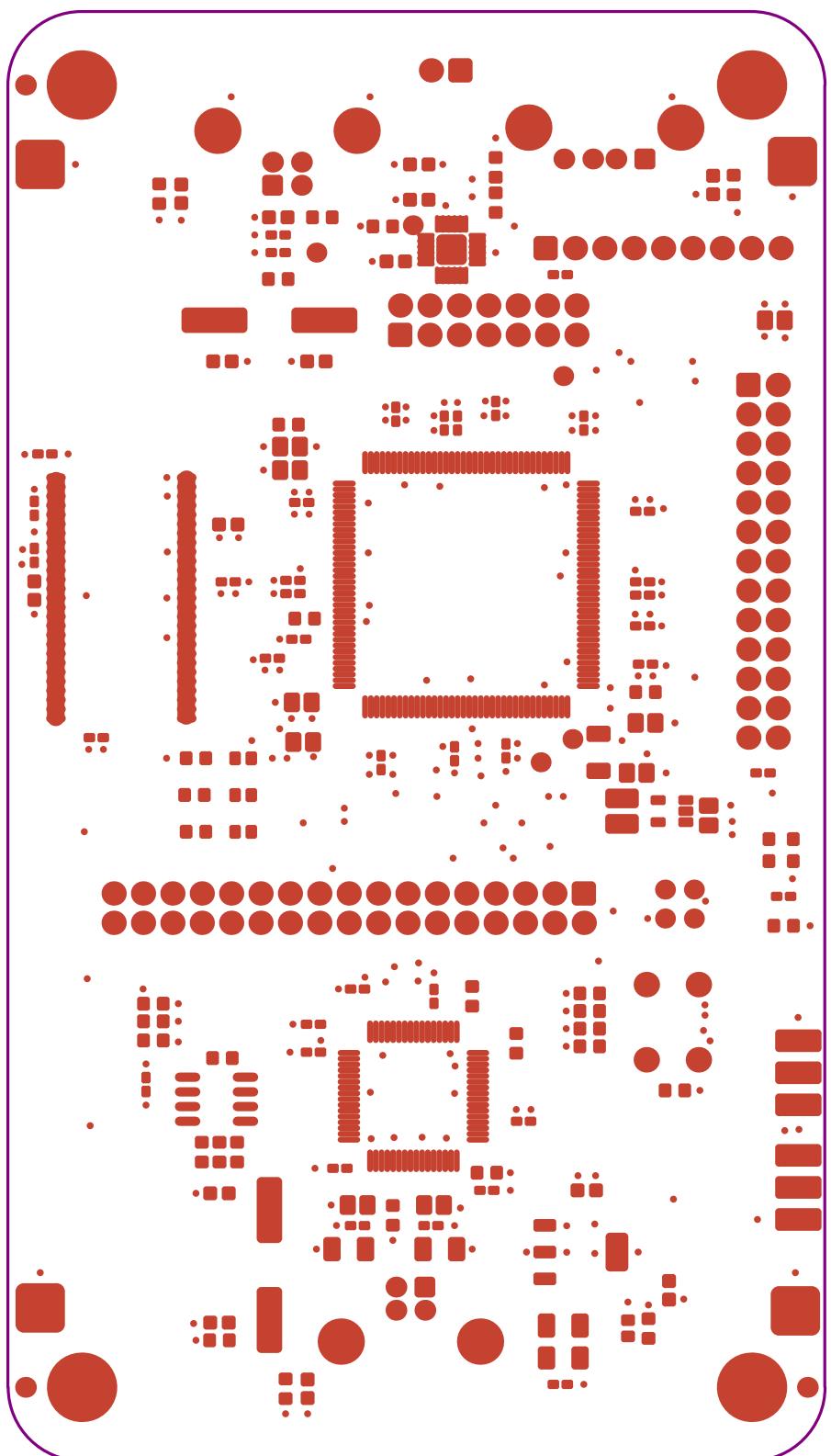
**OpenVizsla v3.3**  
(c) 2013,2014 bushing

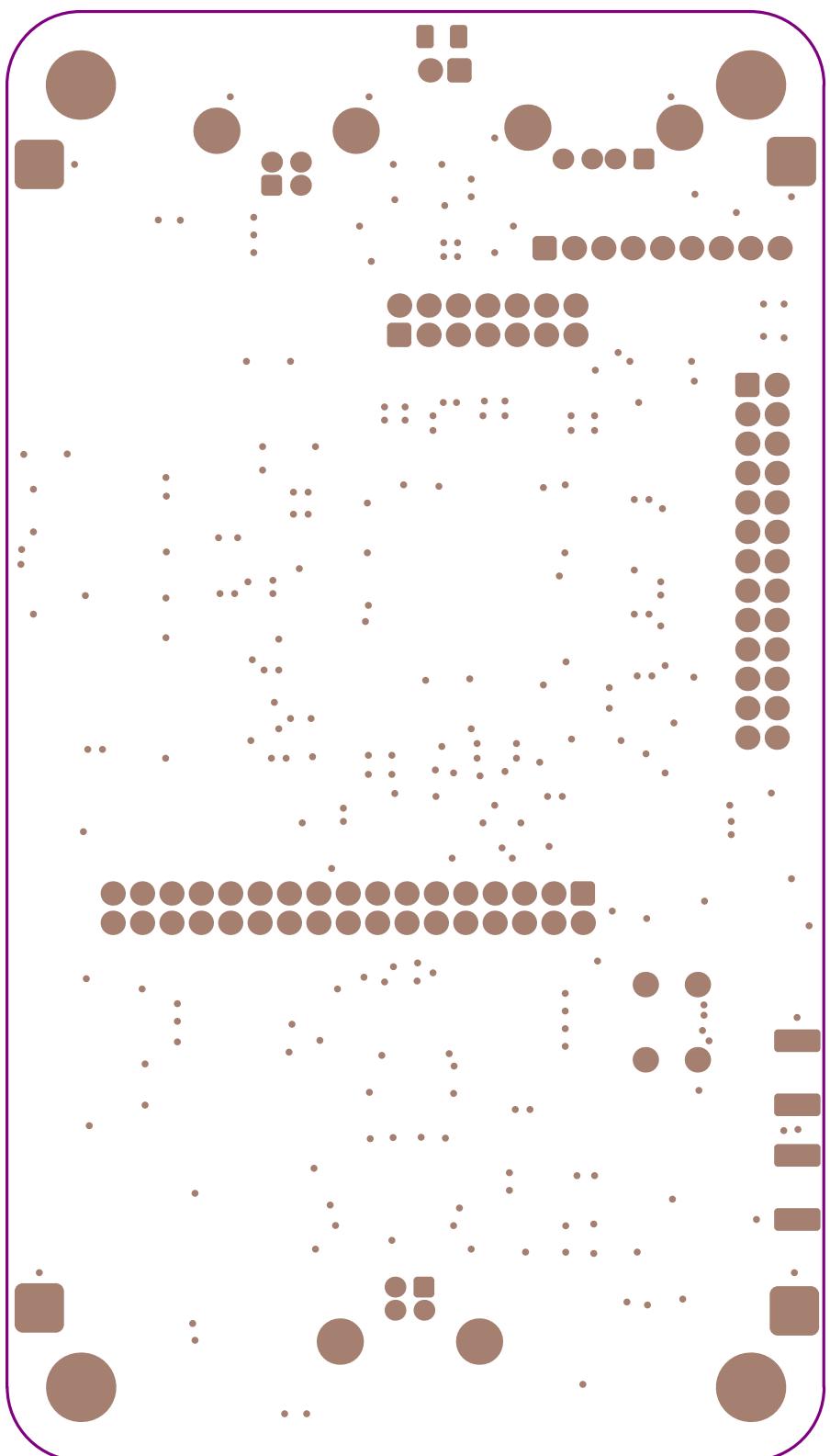


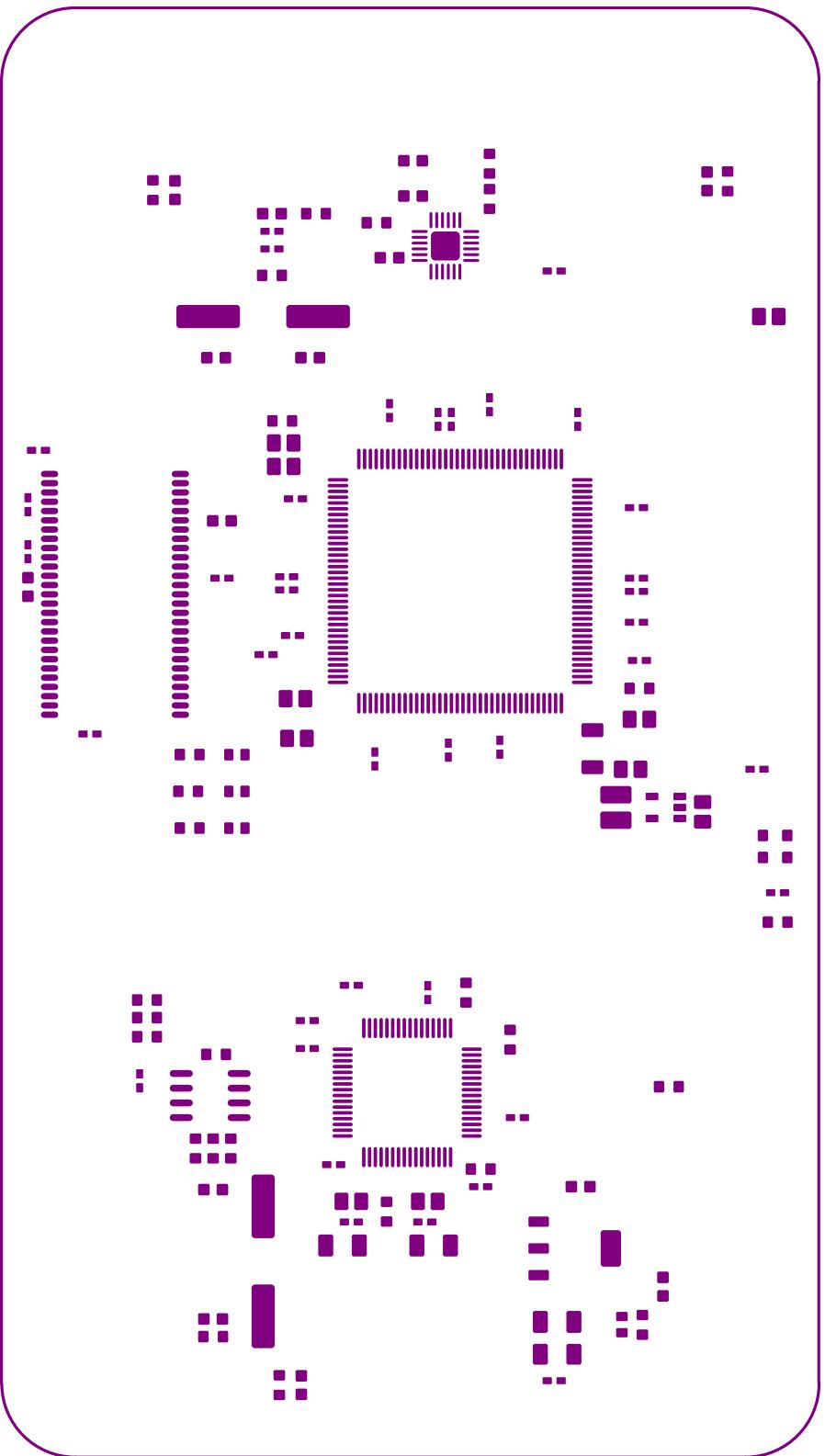


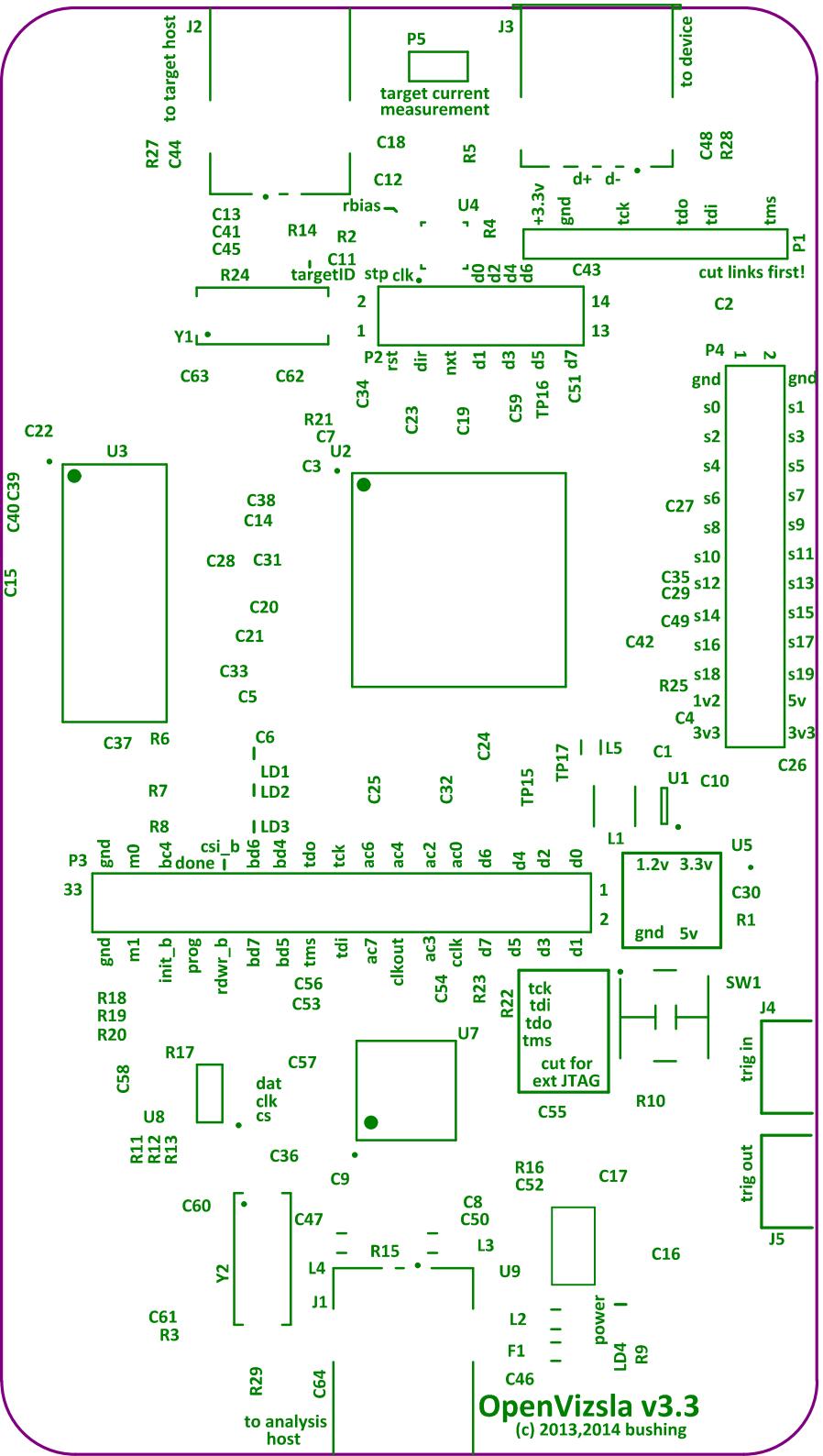












cut links first!  
measure current  
forget current  
- trace cut for



R26 -  
measure current  
forget current  
- trace cut for

Vans D+ D- Buq Buq



