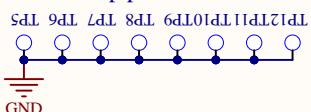
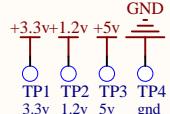


Ground clip pads



Power supply test points, top side



+3.3v +1.2v +5v
Net Class ClassName: Power
Net Class ClassName: Power

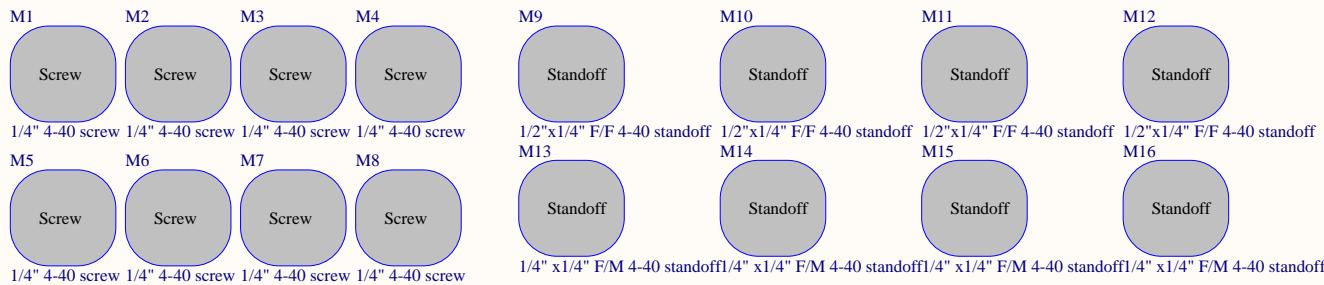
+1.2v
Net Class ClassName: Power

Vusb
Net Class ClassName: Power
Net Class ClassName: Power
GND

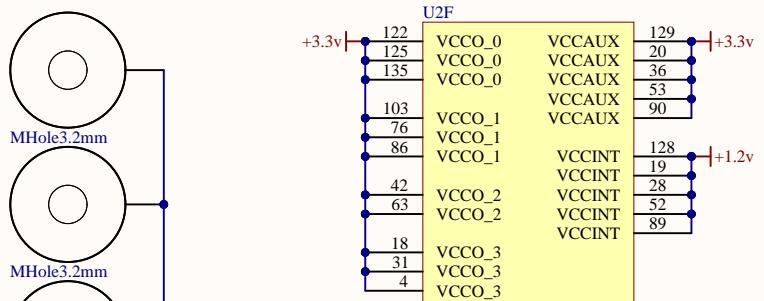
Copyrights: CC-BY-SA 3.0 Patents: Apache 2.0

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File:	C:\Users\...\power.SchDoc	Drawn By:

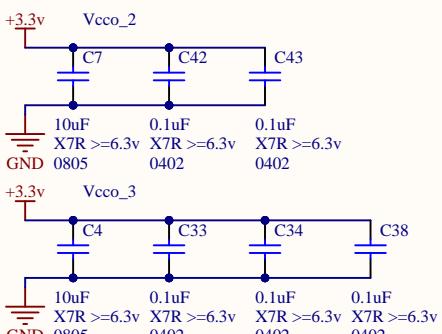
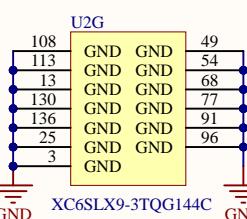
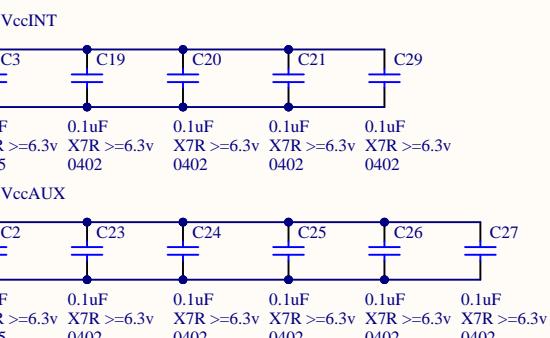
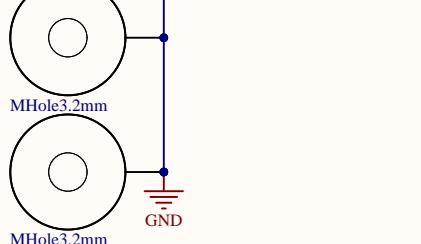
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B

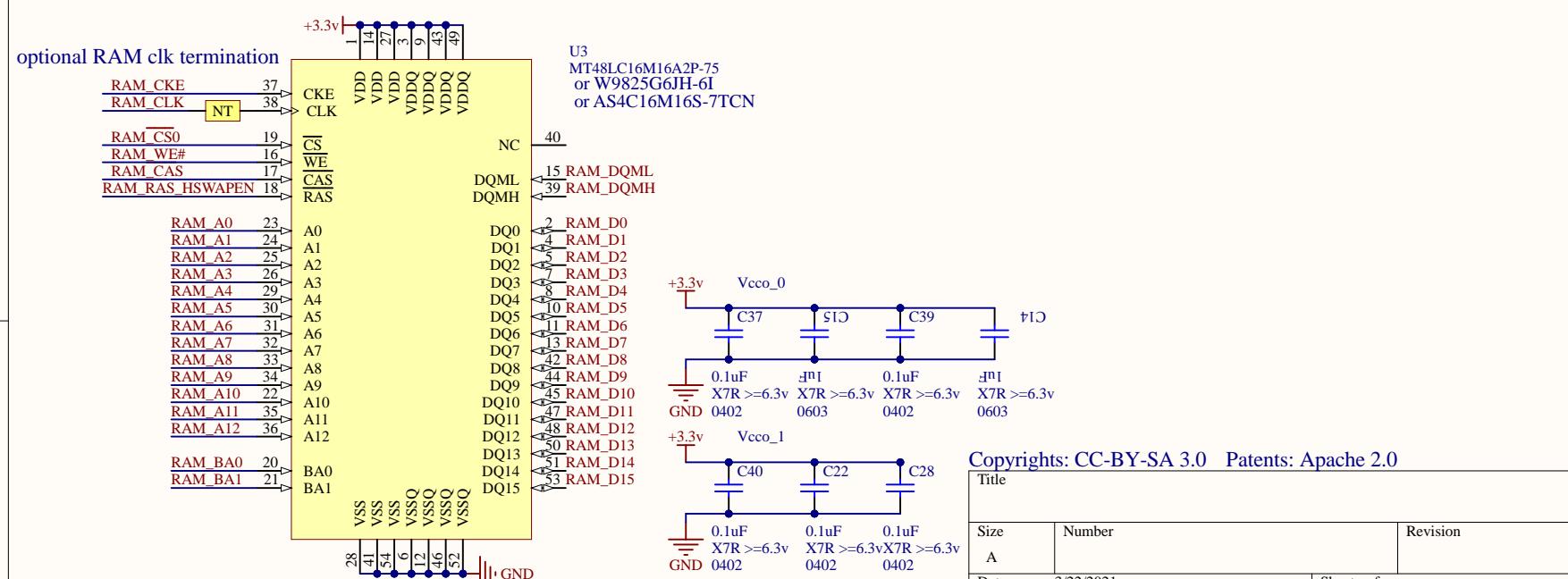
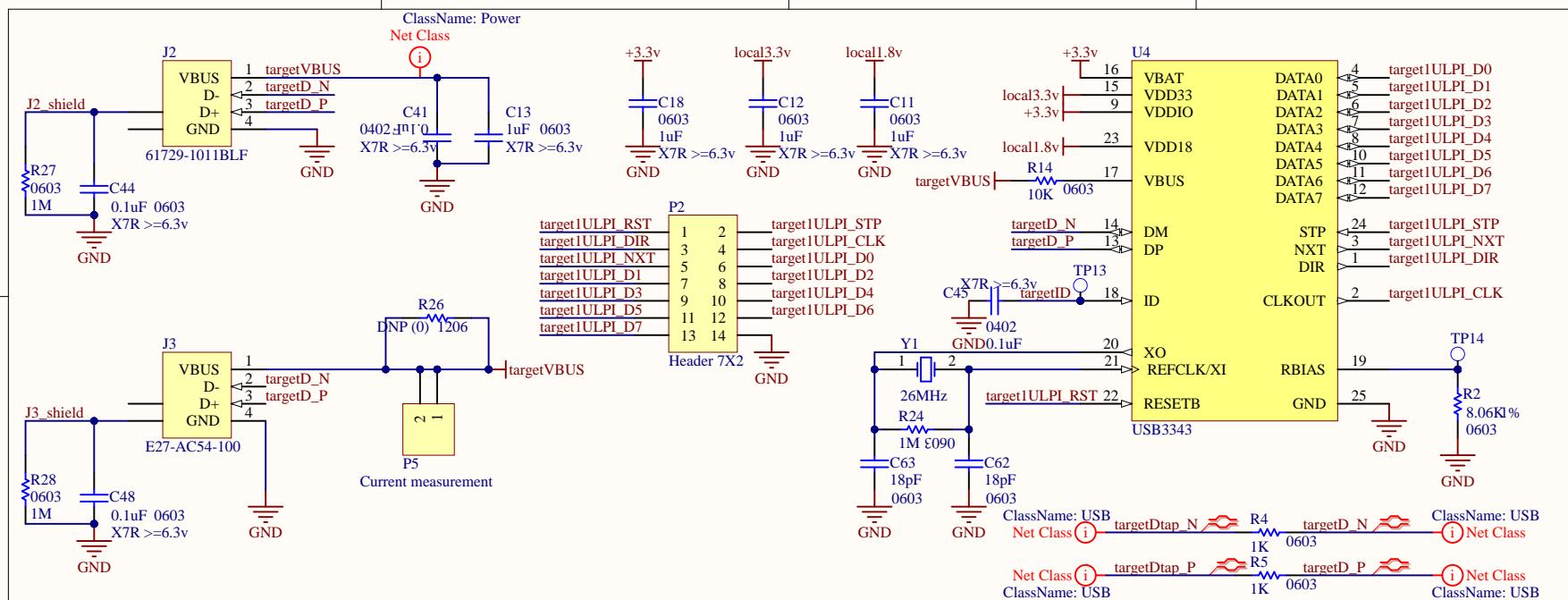


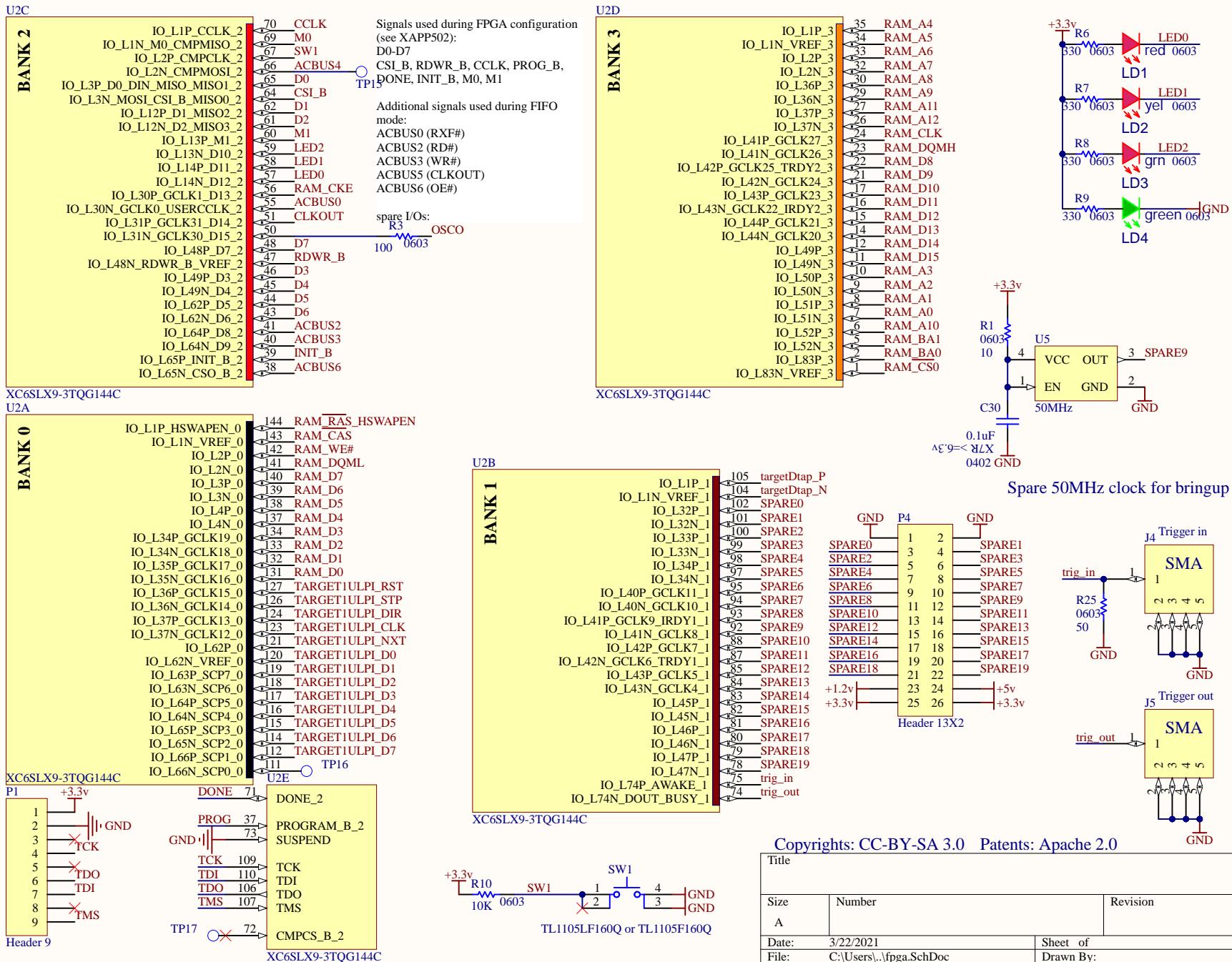
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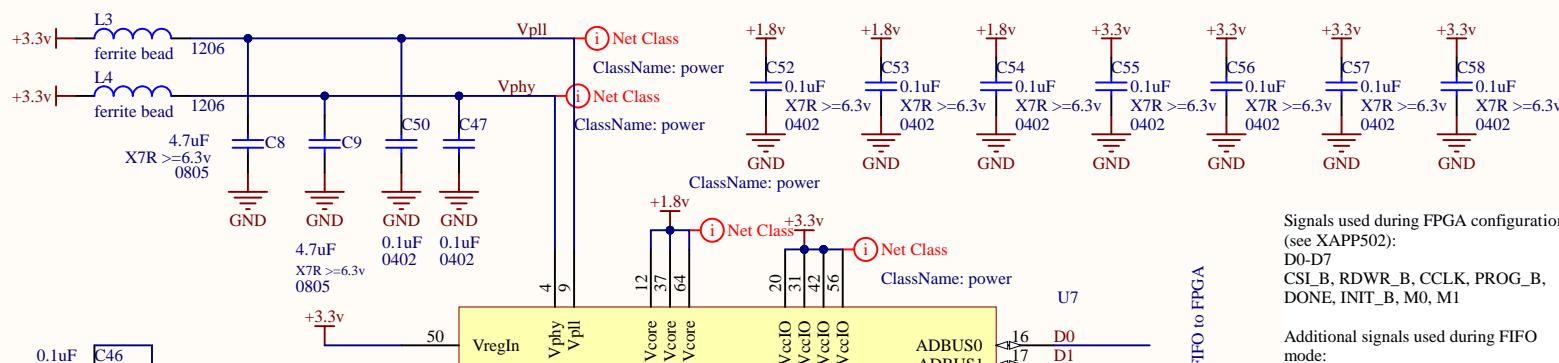
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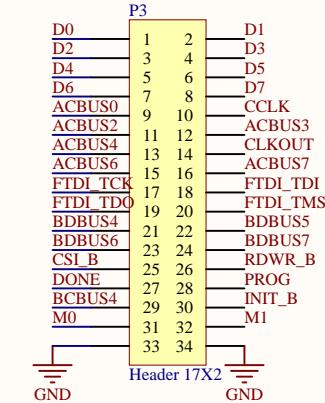
A



Signals used during FPGA configuration
(see XAPP502):
D0-D7
CSI_B, RDWR_B, CCLK, PROG_B,
DONE, INIT_B, M0, M1

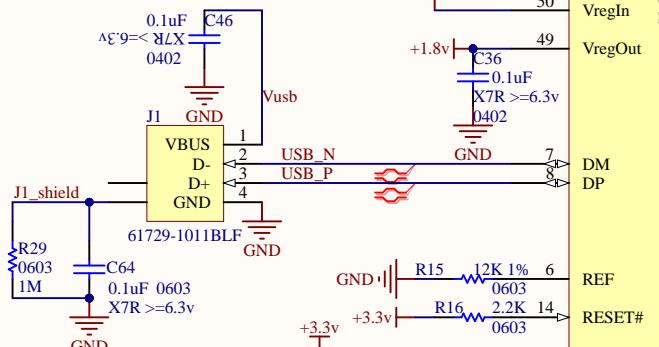
Additional signals used during FIFO mode:
ACBUS0 (RXF#)
ACBUS2 (RD#)
ACBUS3 (WR#)
ACBUSS (CLKOUT)
ACBUS6 (OE#)

spare I/Os:

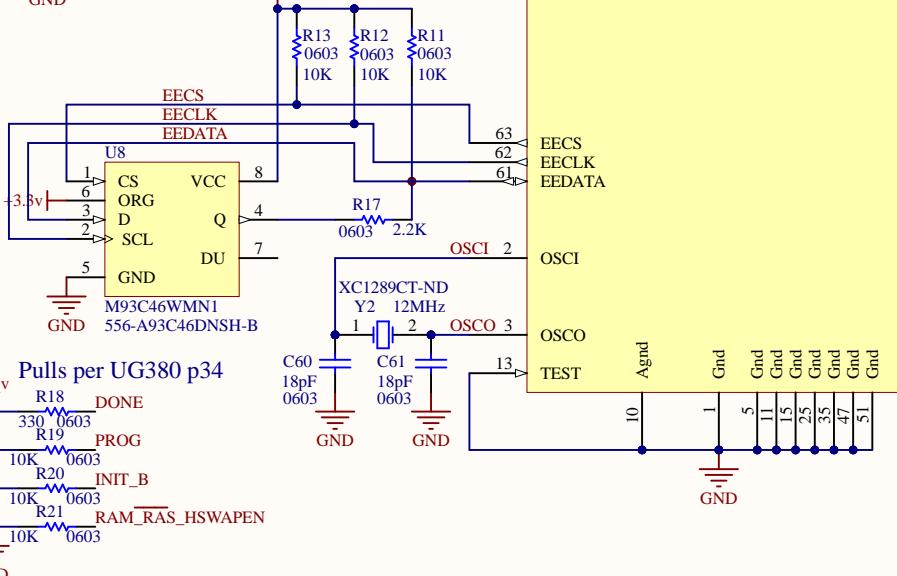


FT2232H

B



C



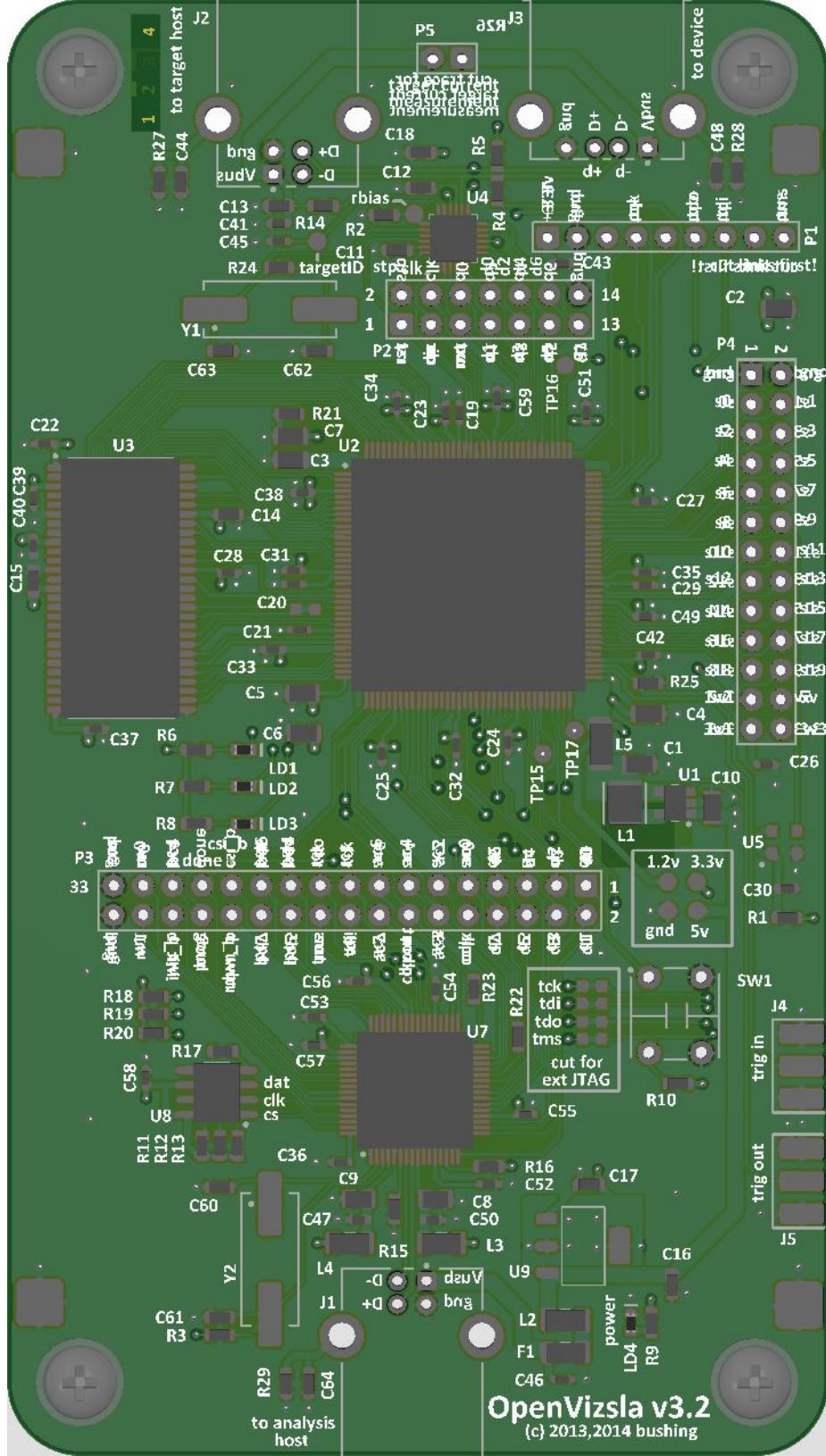
D

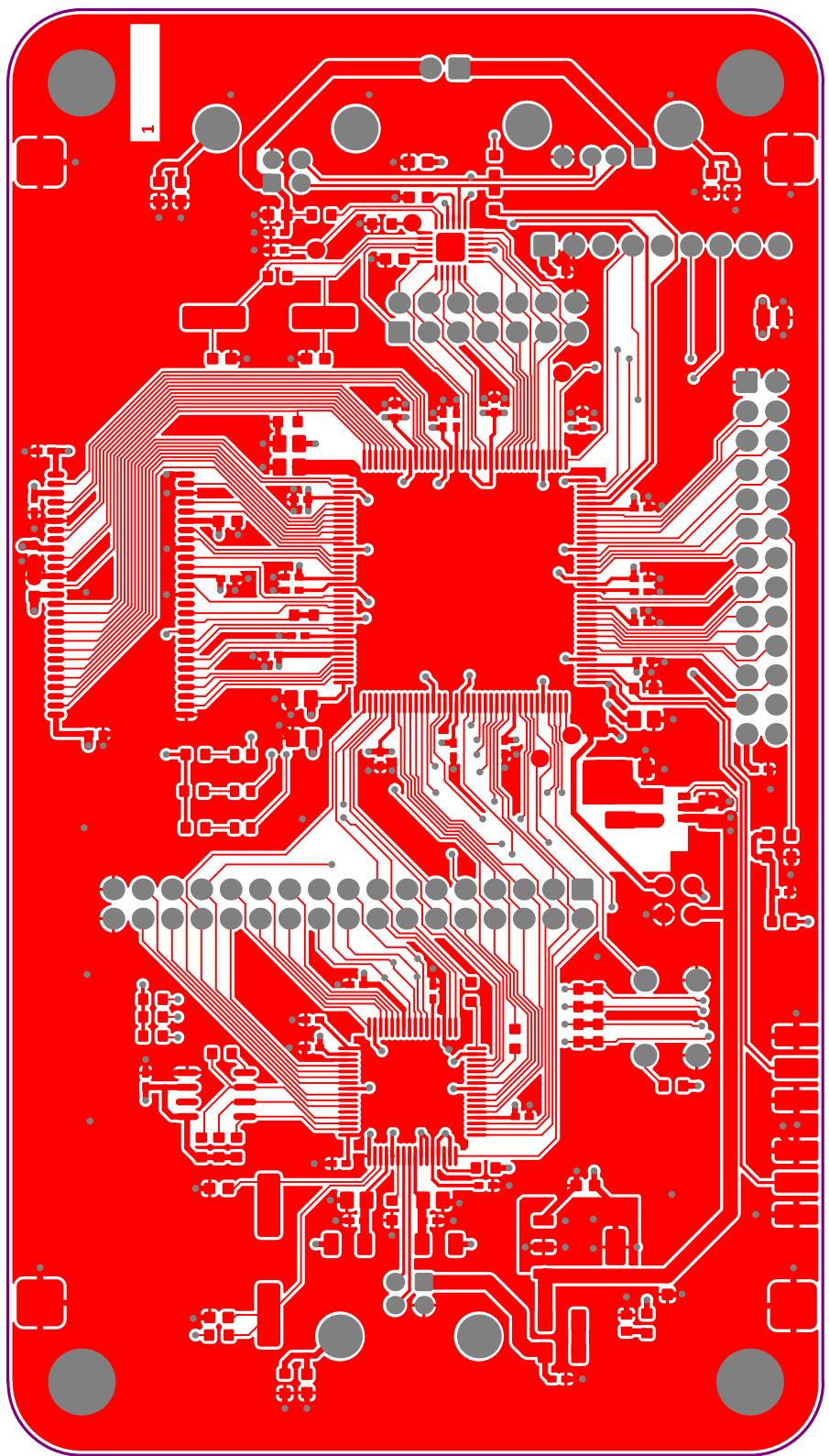
Pulls per UG380 p34

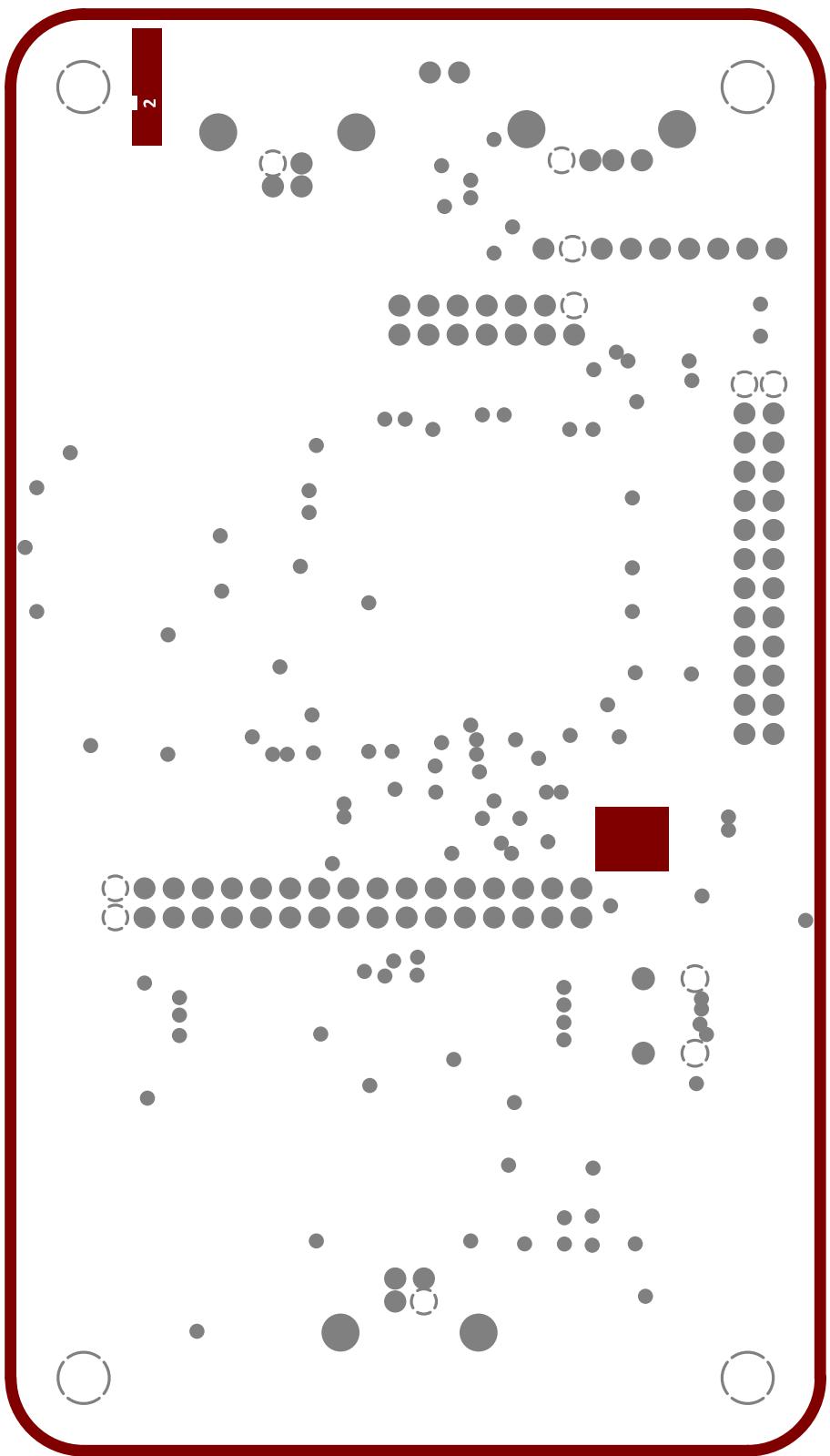
+3.3v R18 DONE
 330 0603
 R19 PROG
 10K 0603
 R20 INIT_B
 10K 0603
 R21 RAM_RAS_HSWAPEN
 10K 0603
 GND

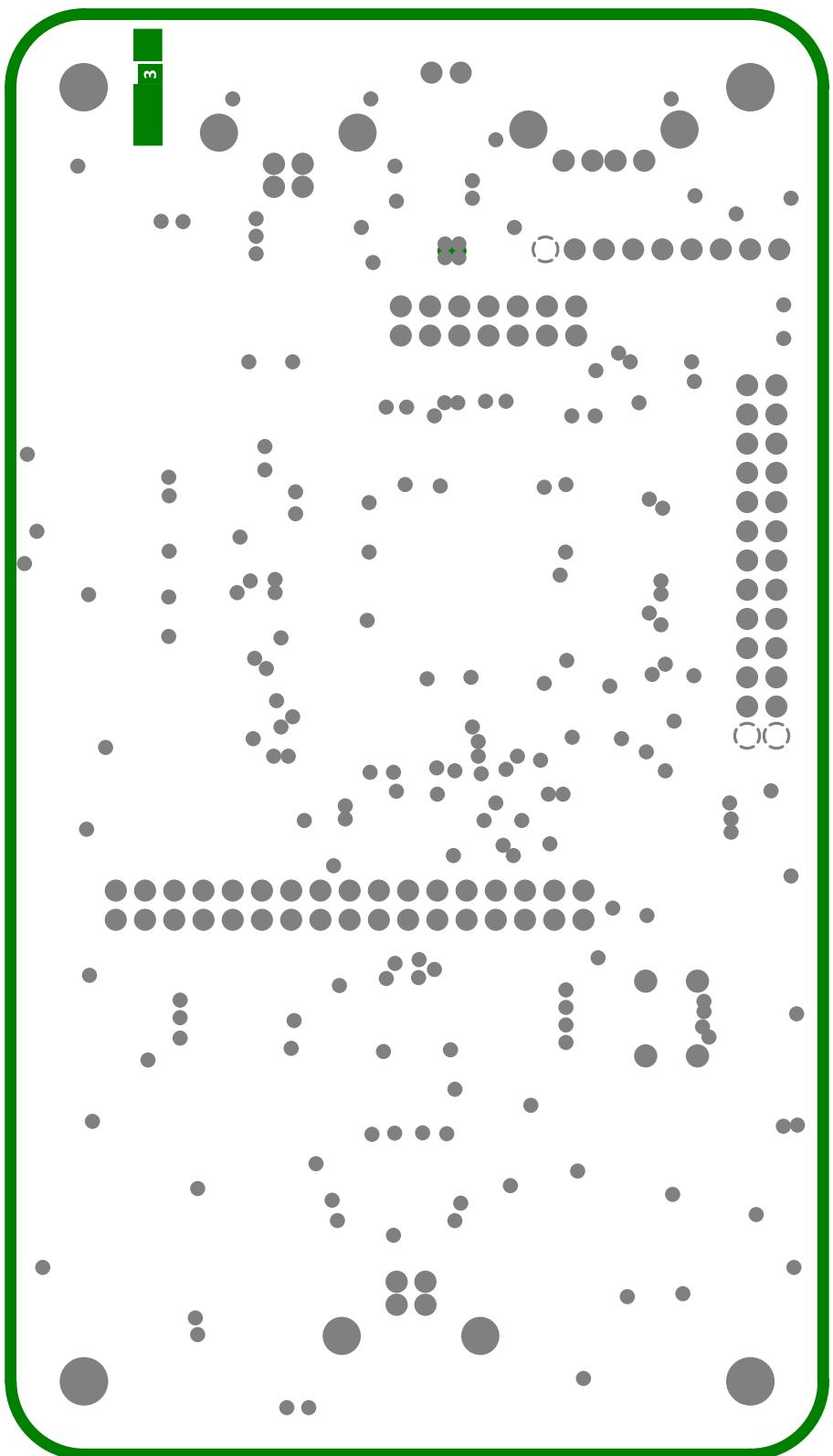
Copyrights: CC-BY-SA 3.0 Patents: Apache 2.0

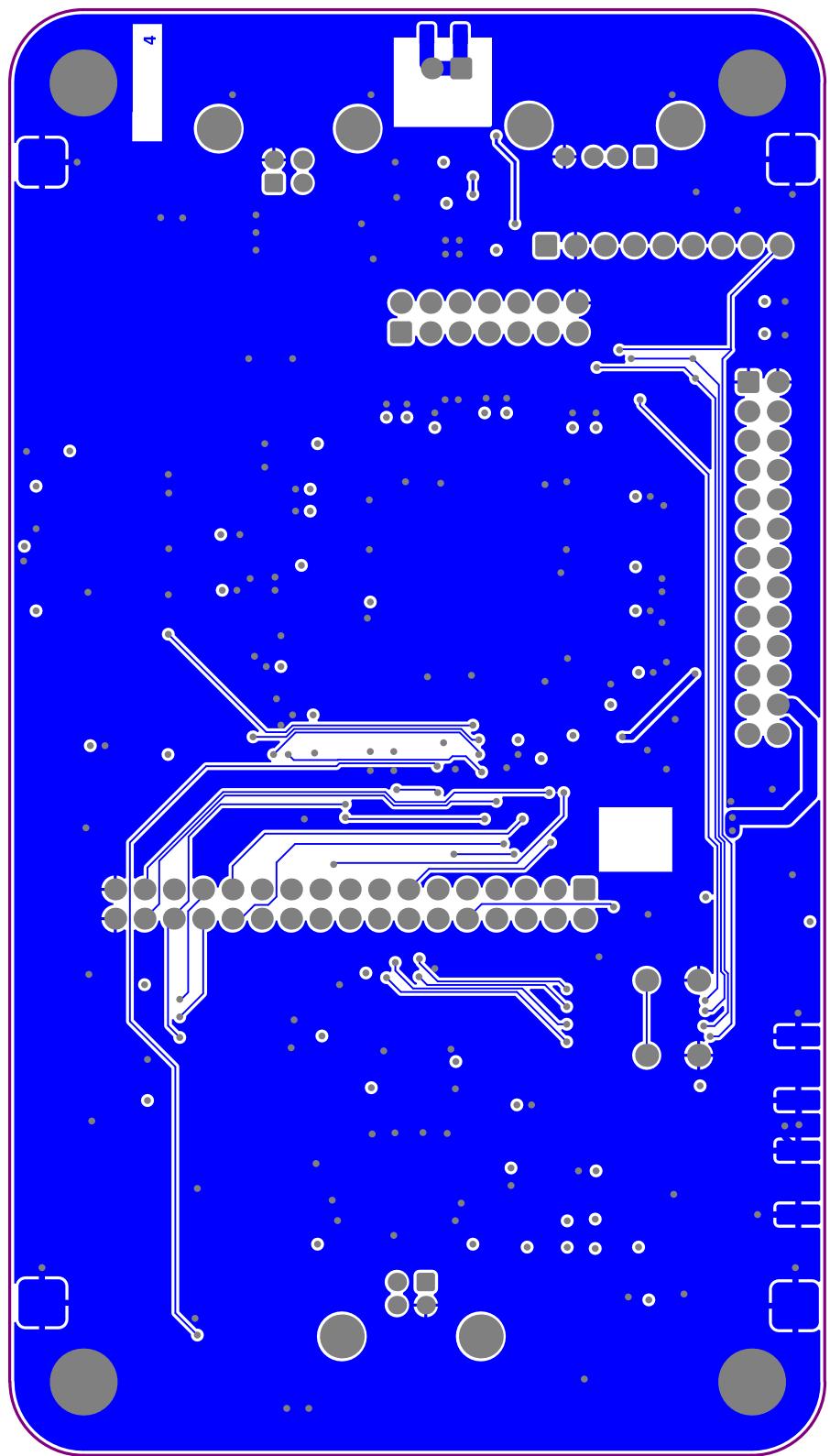
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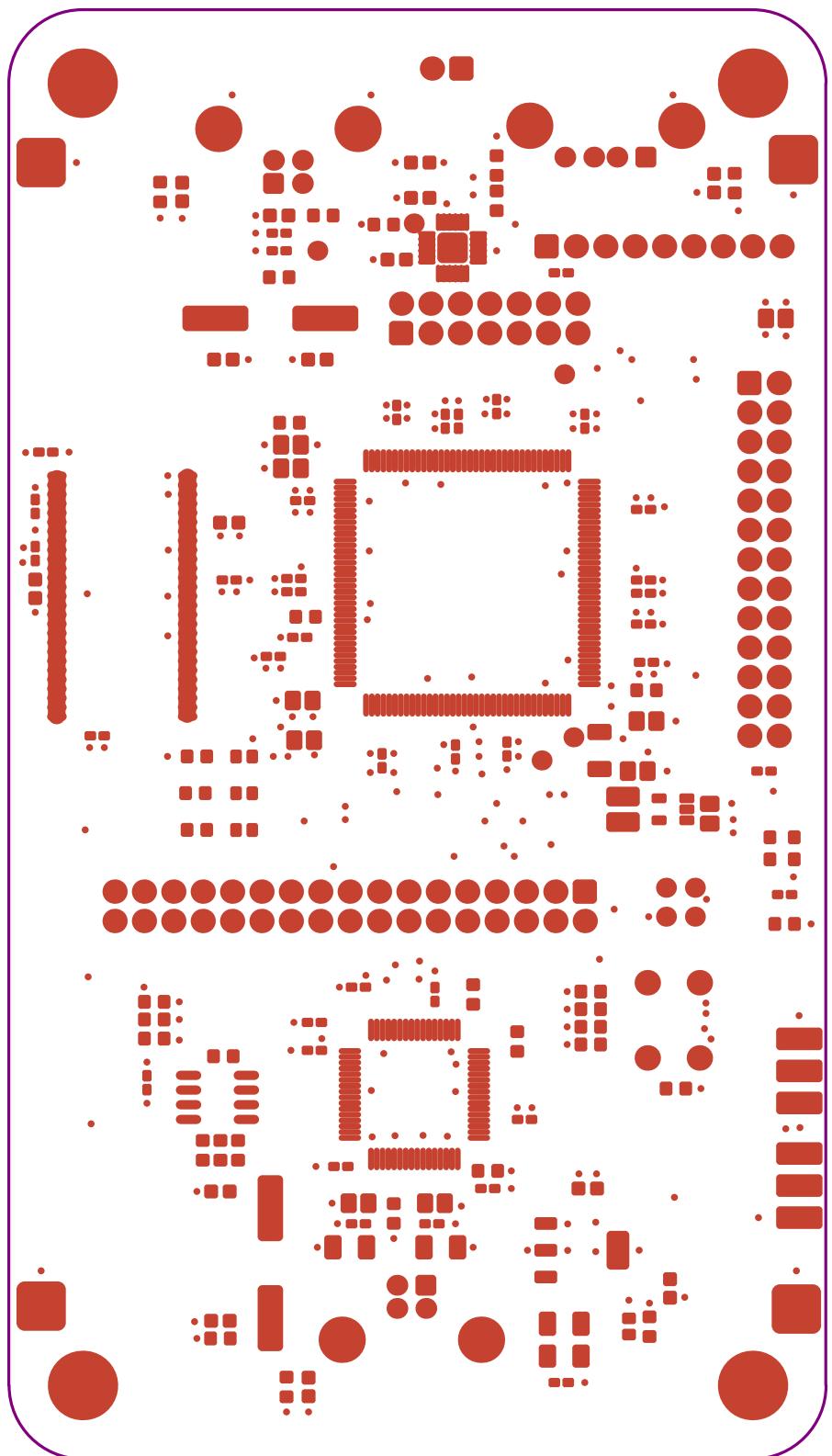


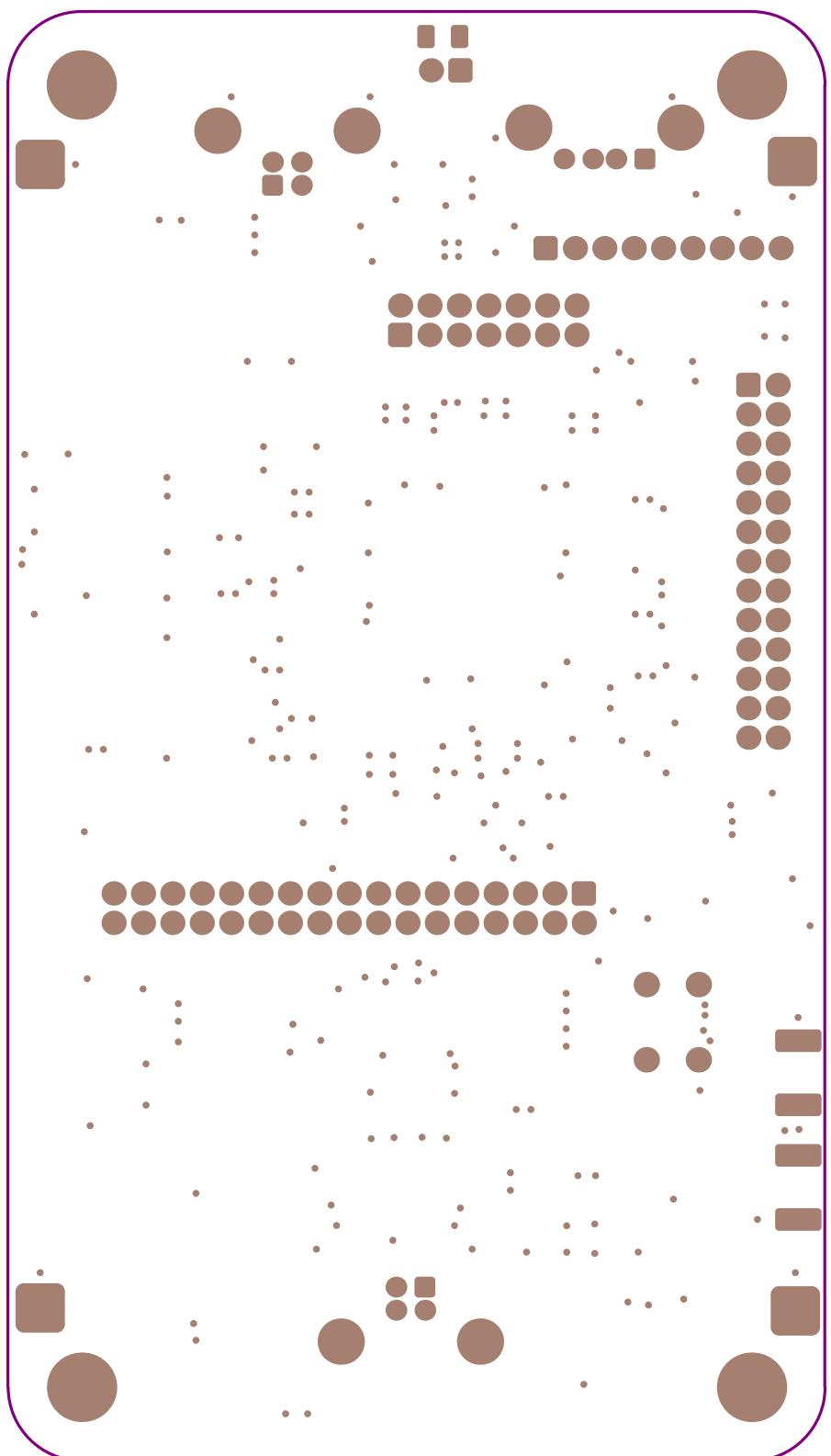


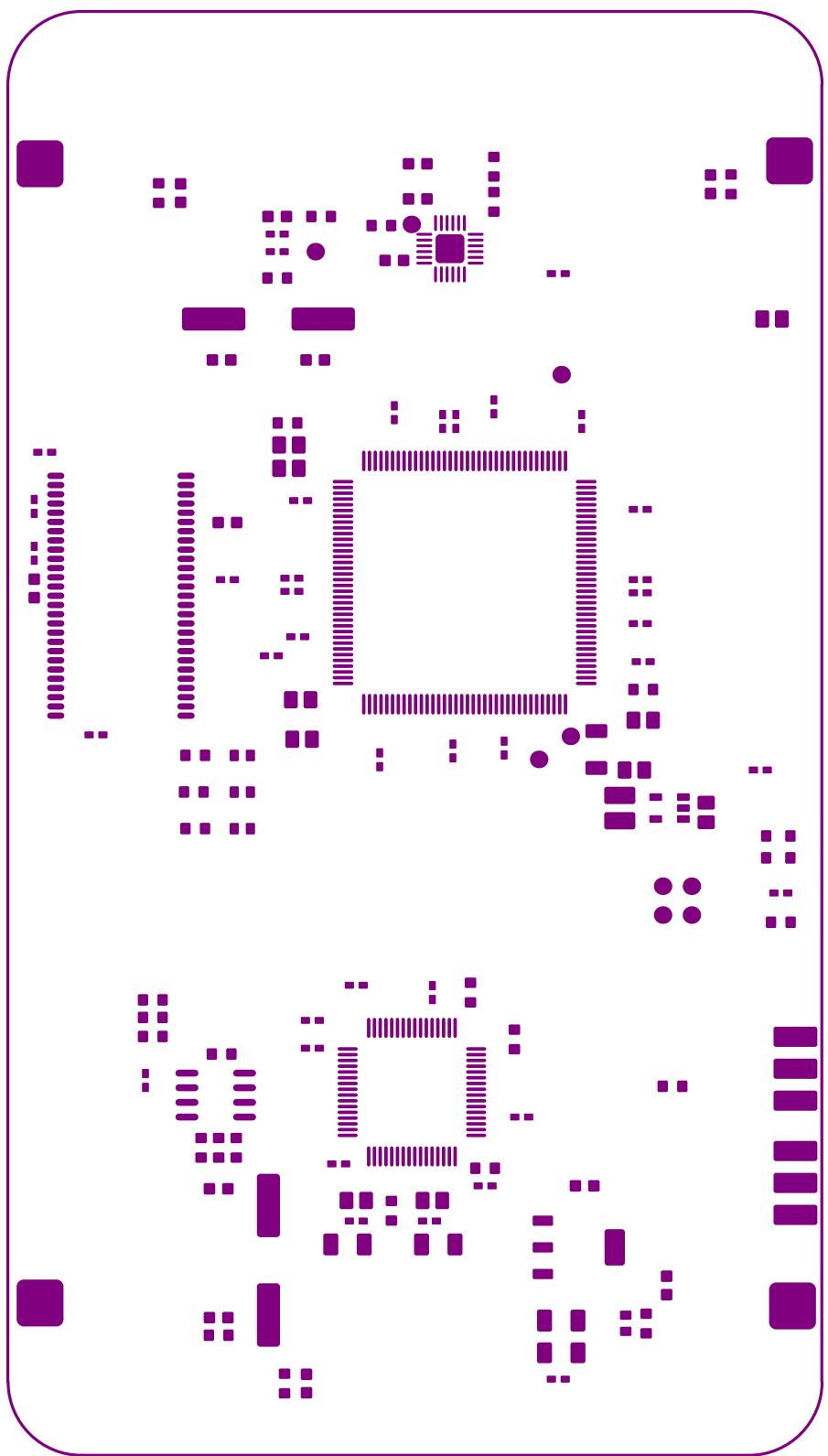


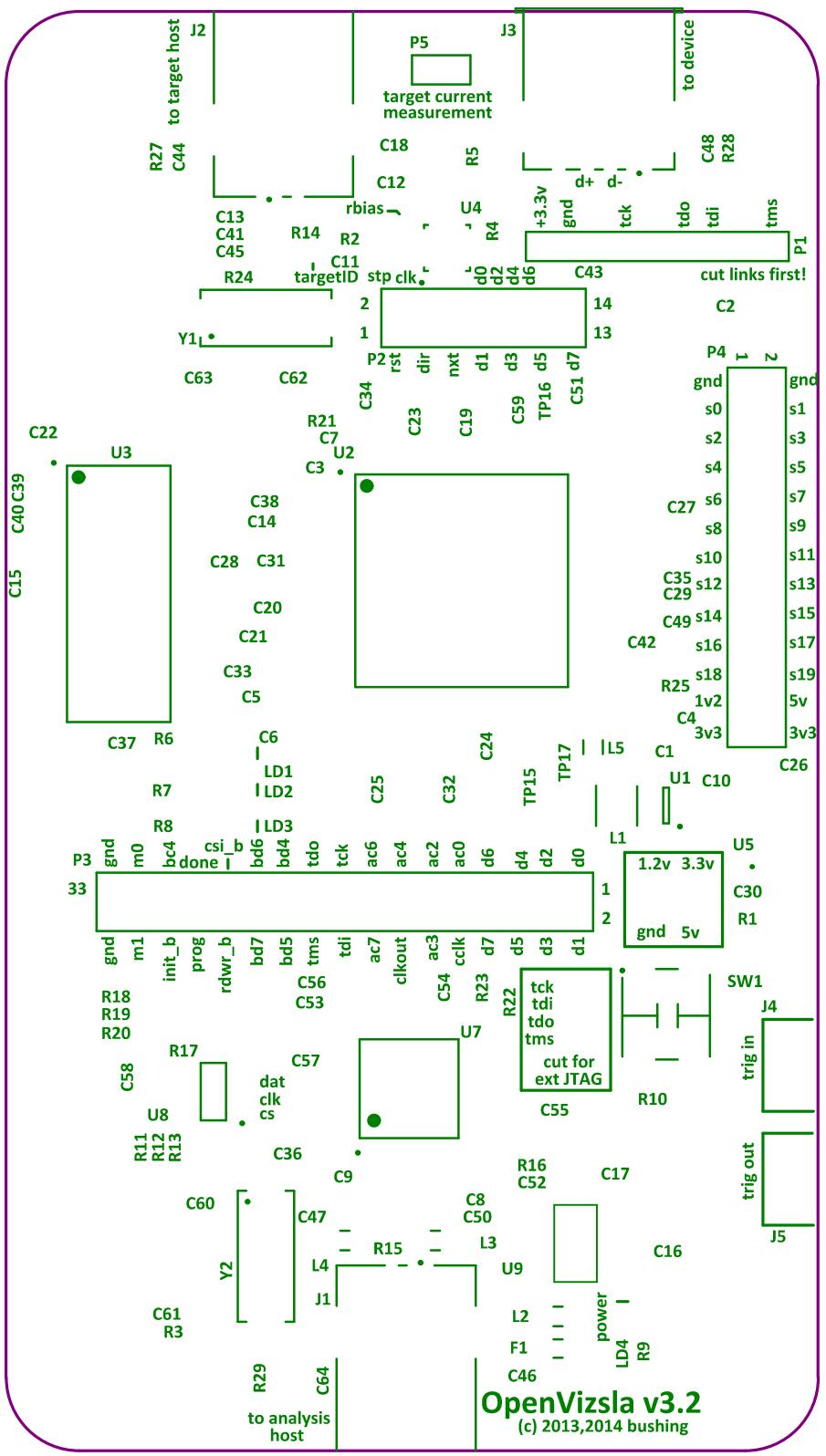












OpenVizsla v3.2
(c) 2013,2014 bushing

- 65 -

cut trace for
target current
measurement

លេខ	ឈ្មោះ
០២	តែន
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៥២៣	ស៊ុន
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៨២៣	ស៊ុន
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1b
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bt
but
dil
list

D-
D+
Aplus
Bplus
Cplus

q1	bug
q2	bug
q3	bug
q4	bug
q5	bug
q6	bug
q7	bug
q8	bug
q9	bug
q10	bug
q11	bug
q12	bug
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q36	bug
q37	bug
q38	bug
q39	bug
q40	bug

Vnsb
Bud



