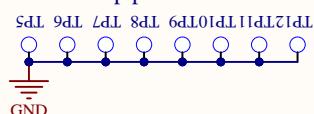
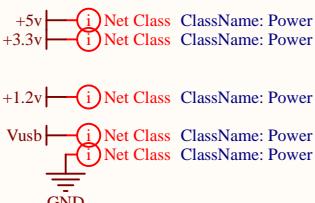
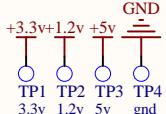
**C**

Ground clip pads



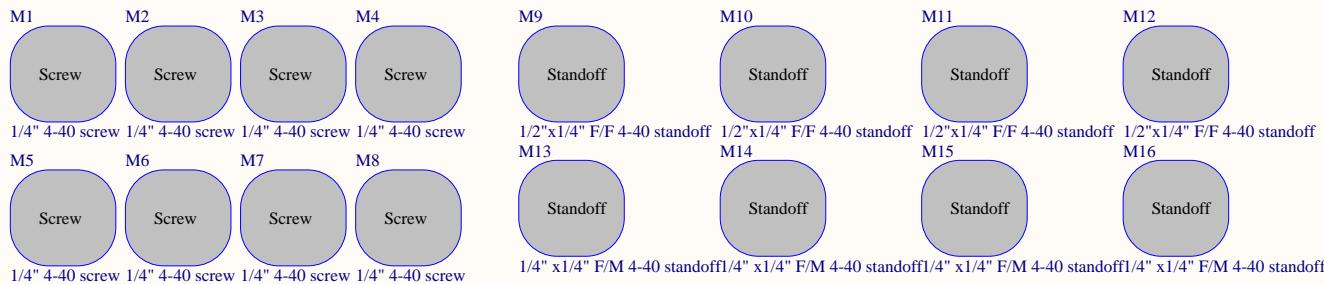
Power supply test points, top side



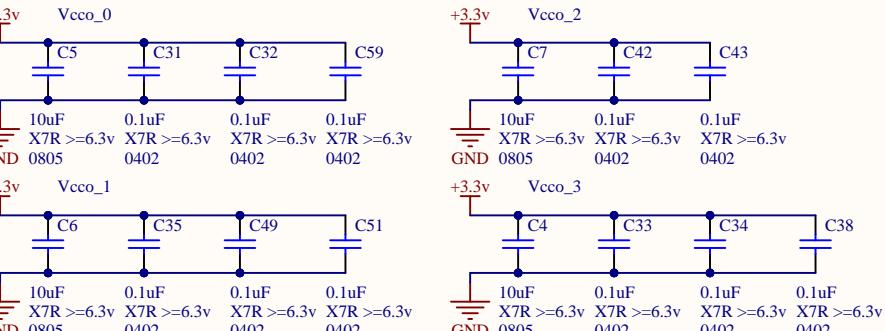
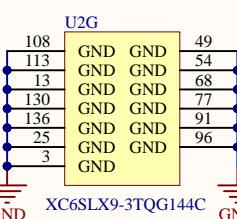
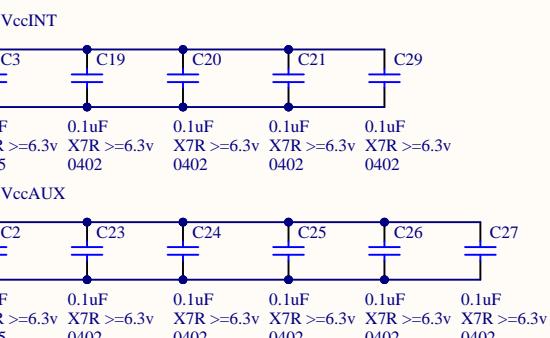
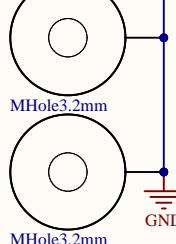
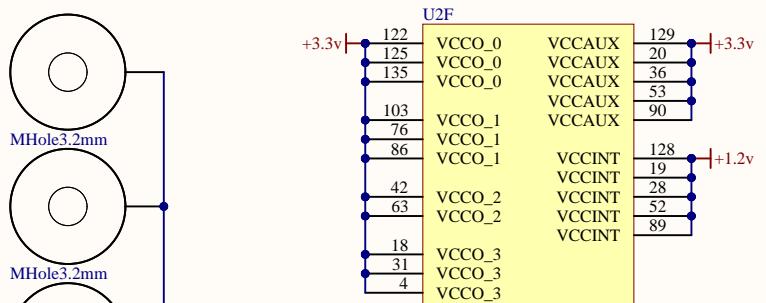
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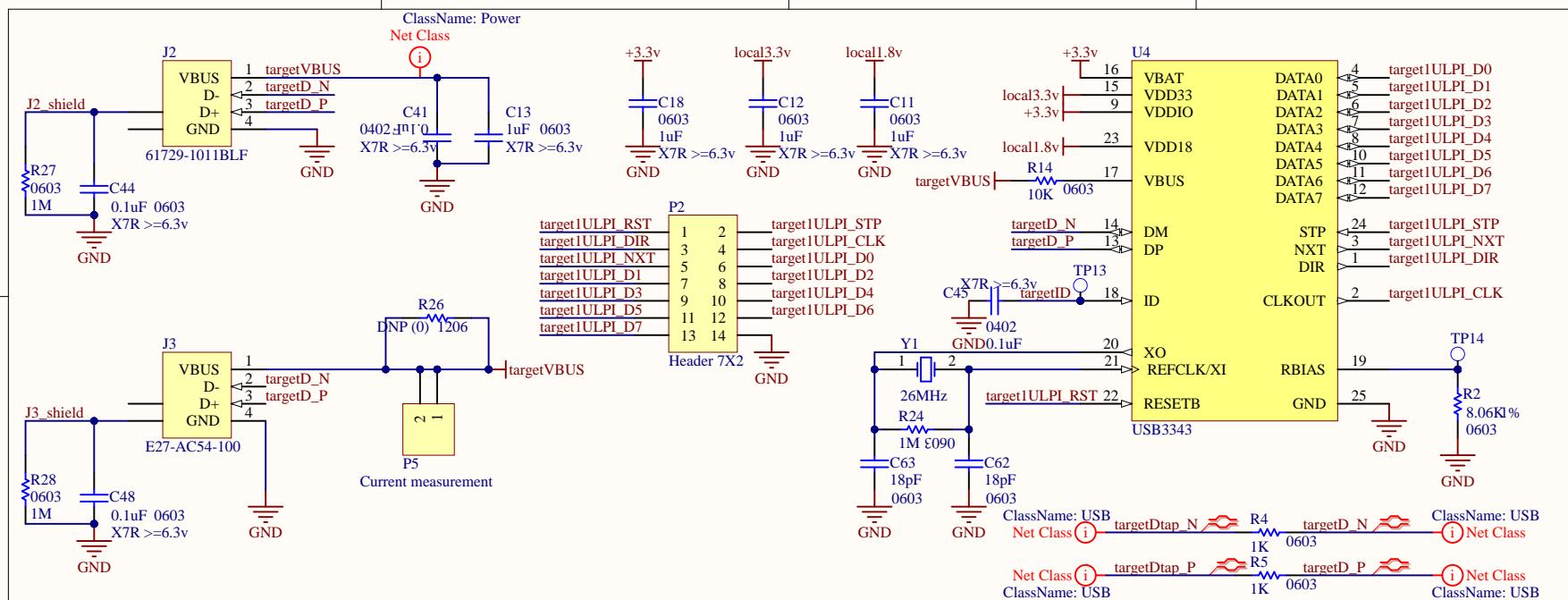


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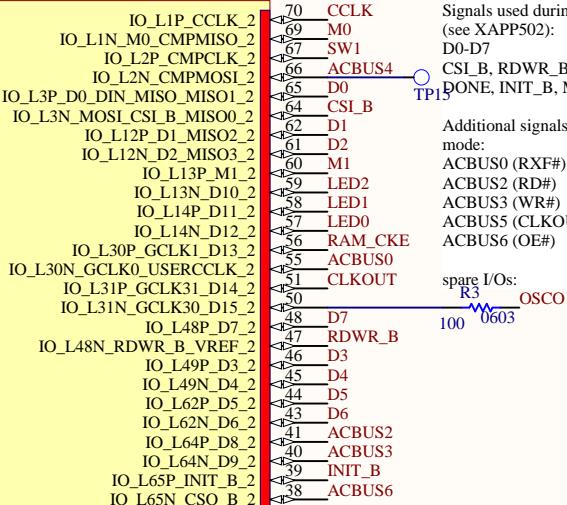


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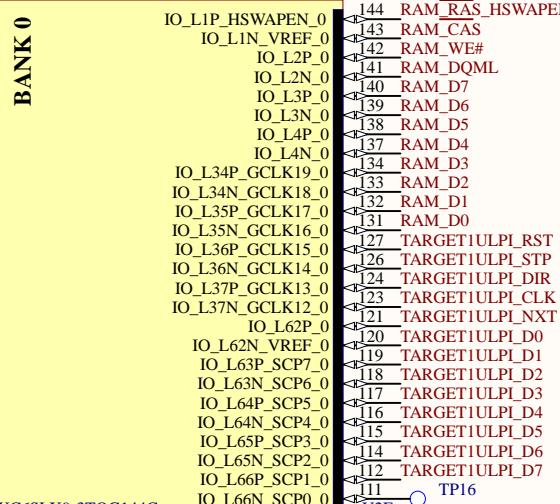


U2C

BANK 2

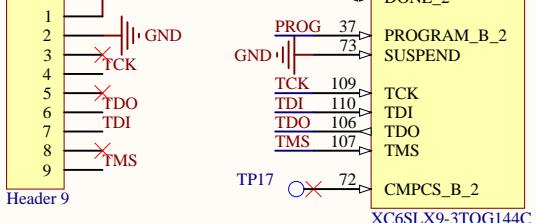
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U2A

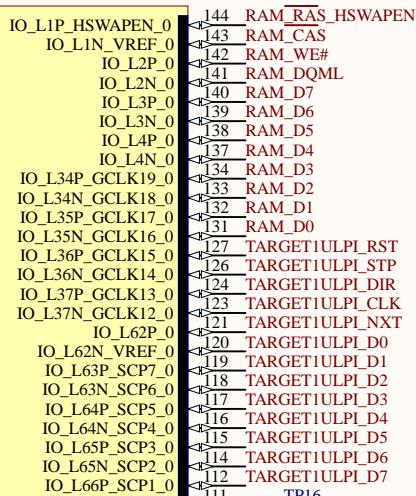
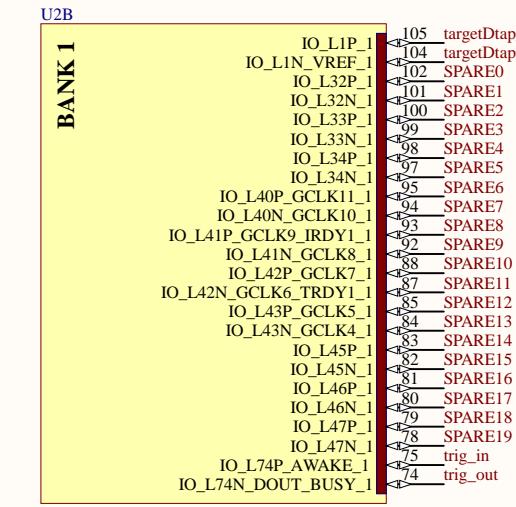


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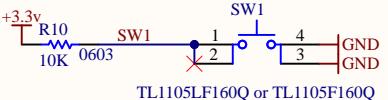
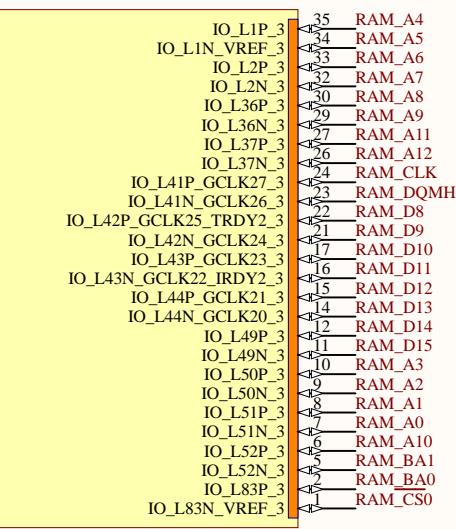
P1



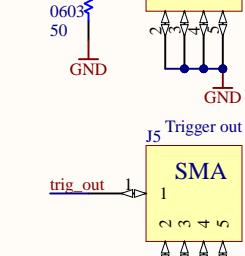
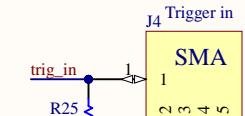
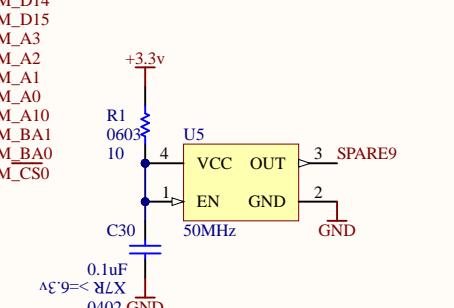
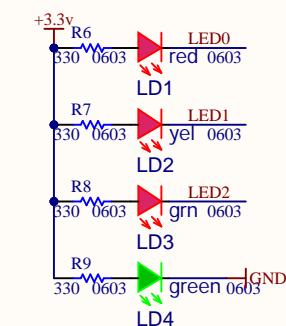
U2D

BANK 0**BANK 1**

XC6SLX9-3TQG144C

**BANK 3**

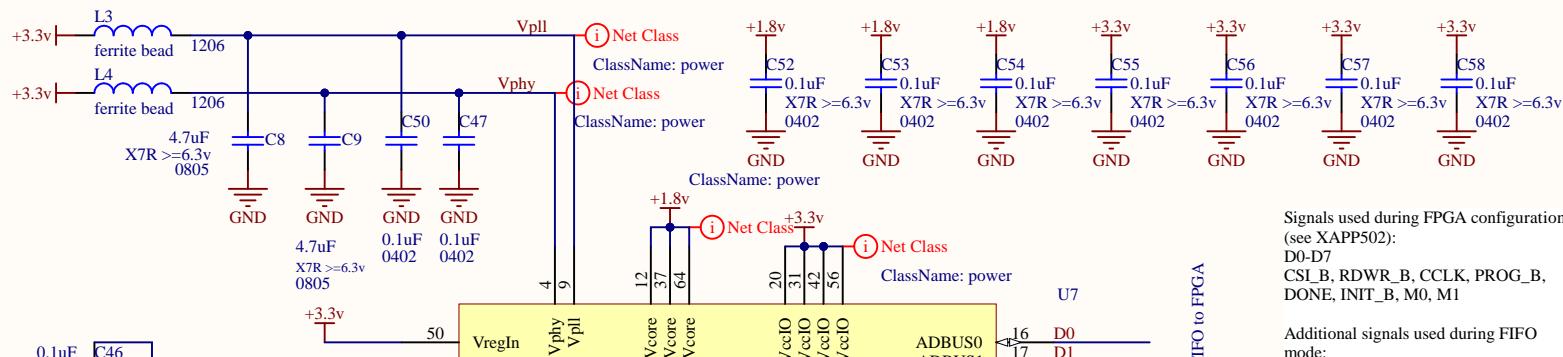
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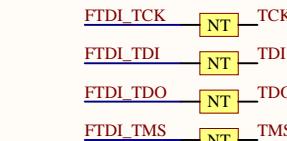
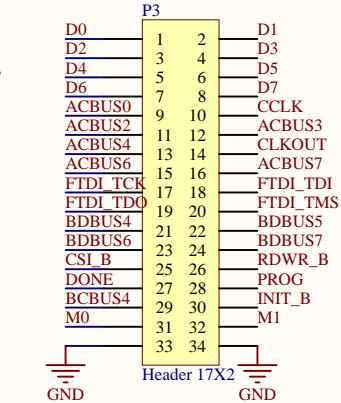
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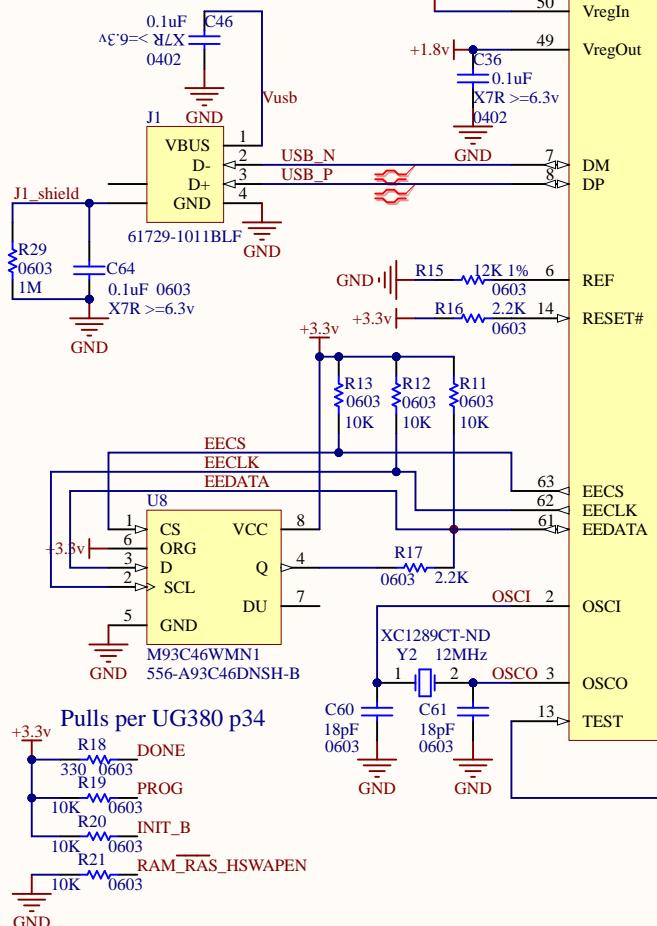
Signals used during FPGA configuration
(see XAPP502):
D0-D7
CSI_B, RDWR_B, CCLK, PROG_B,
DONE, INIT_B, M0, M1

Additional signals used during FIFO mode:
ACBUS0 (RXF#)
ACBUS2 (RD#)
ACBUS3 (WR#)
ACBUSS (CLKOUT)
ACBUS6 (OE#)

spare I/Os:



B



FT2232H

C

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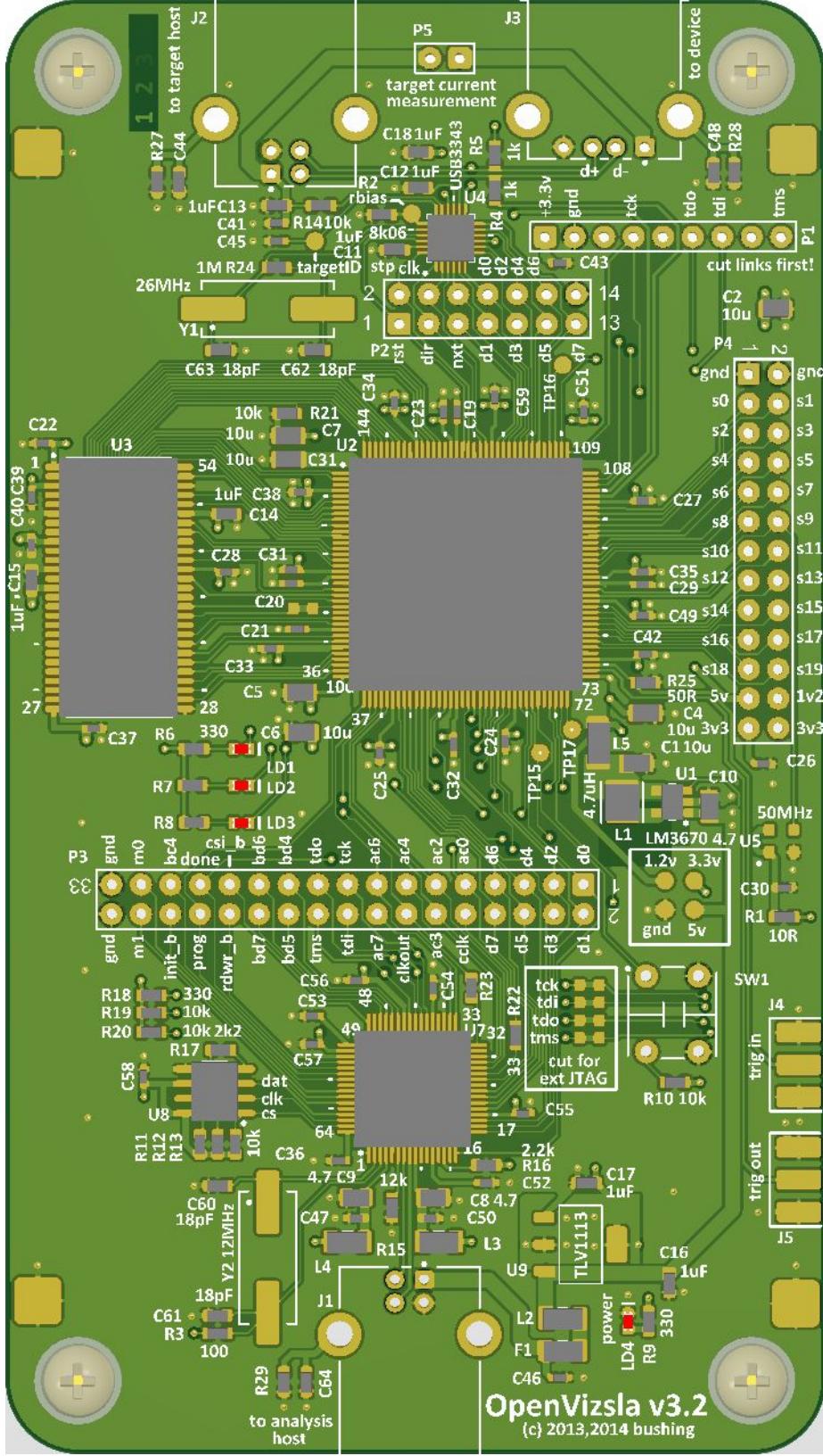
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D

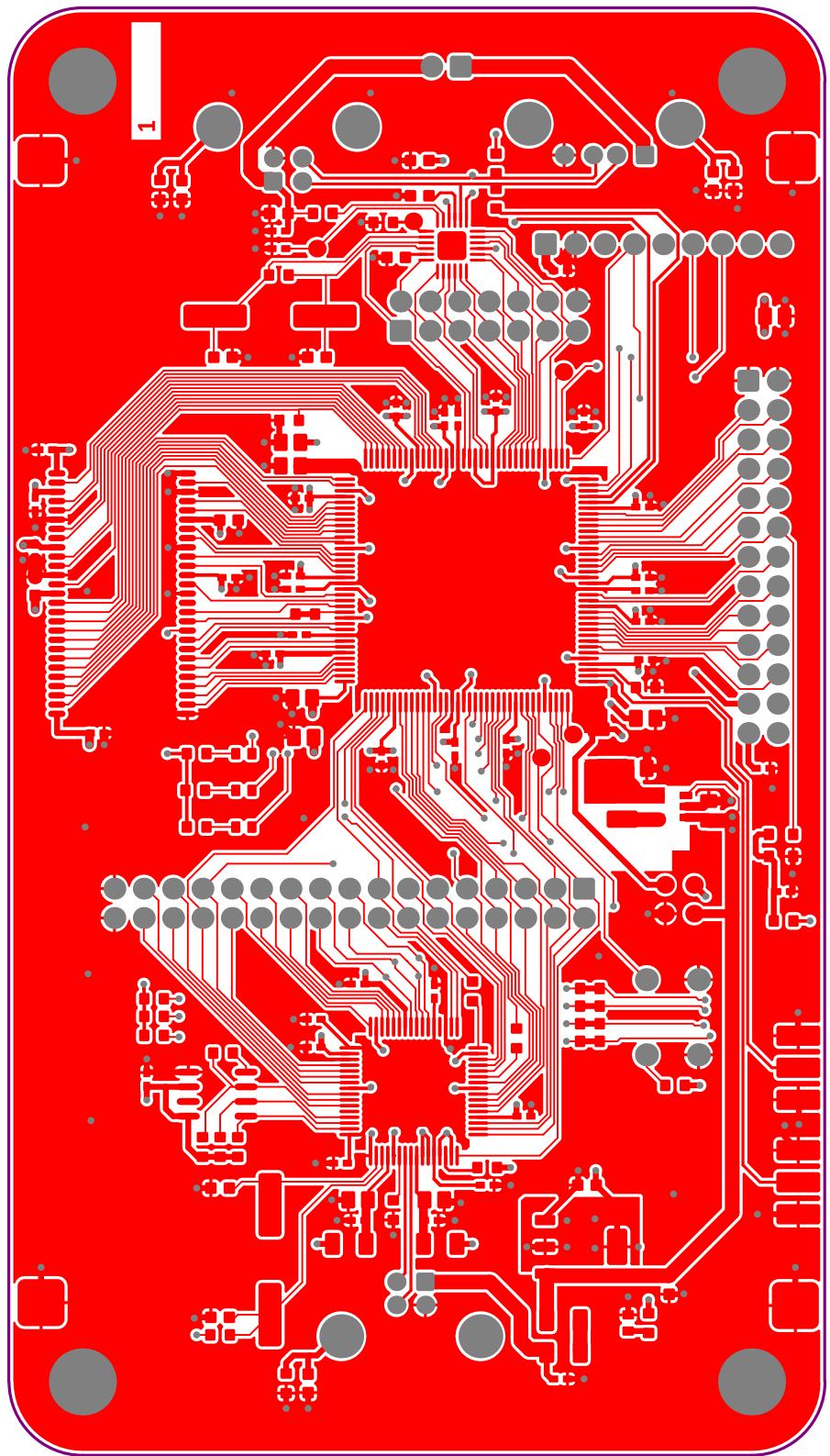
Pulls per UG380 p34

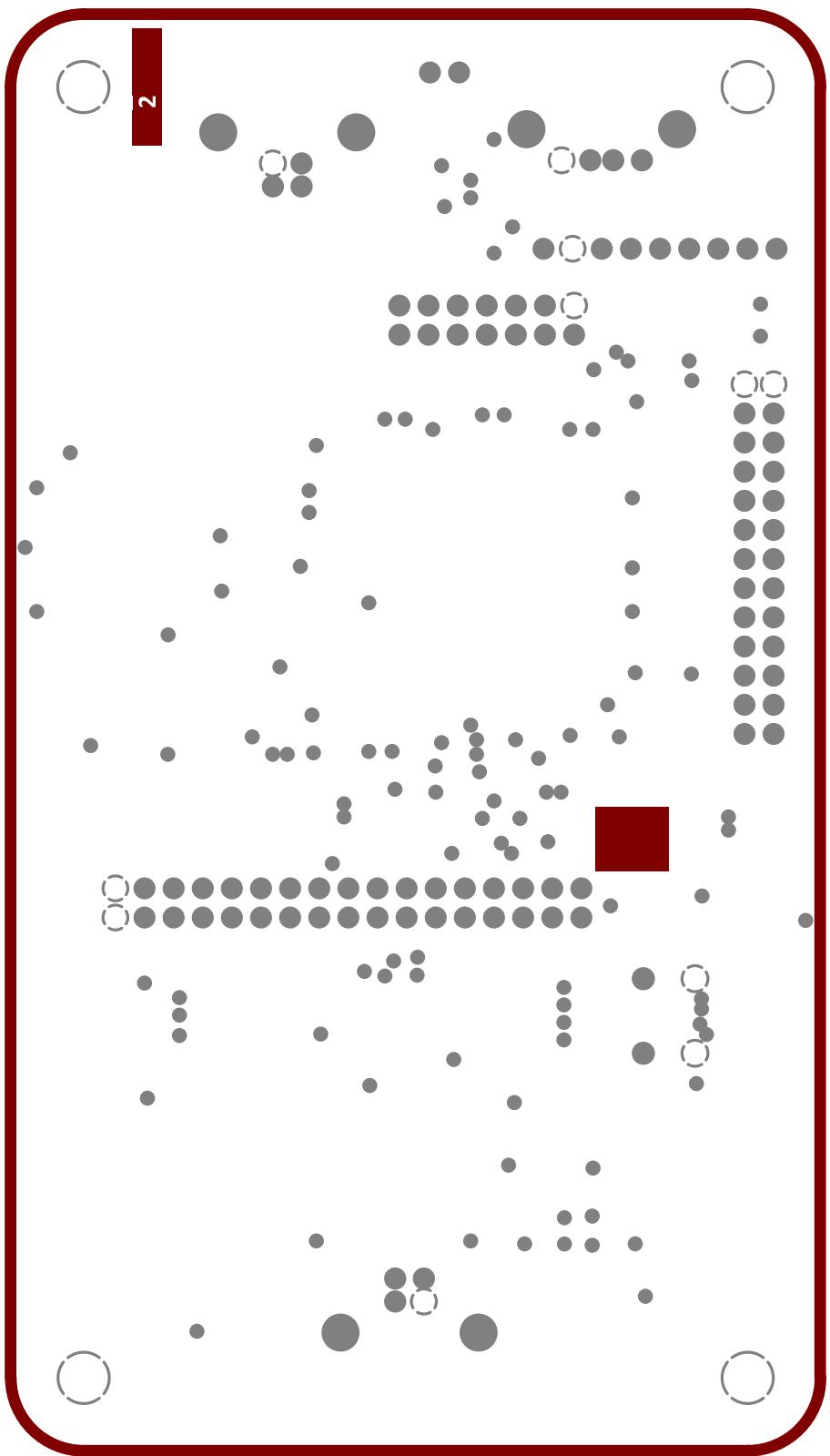
- +3.3v → DONE (330Ω 0603)
- +3.3v → PROG (10kΩ 0603)
- +3.3v → INIT_B (10kΩ 0603)
- +3.3v → RAM_RAS_HSWAPEN (10kΩ 0603)

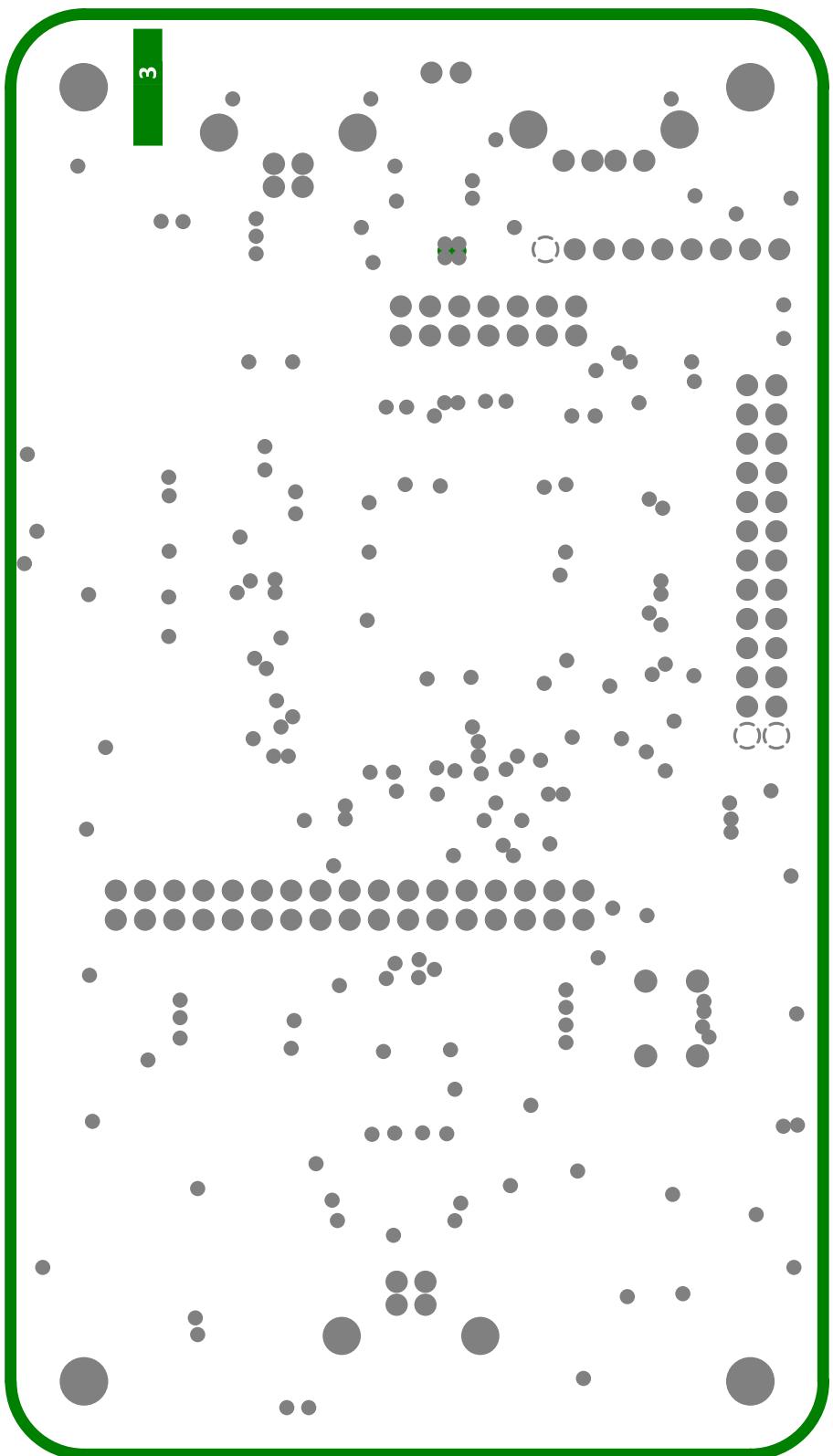
GND

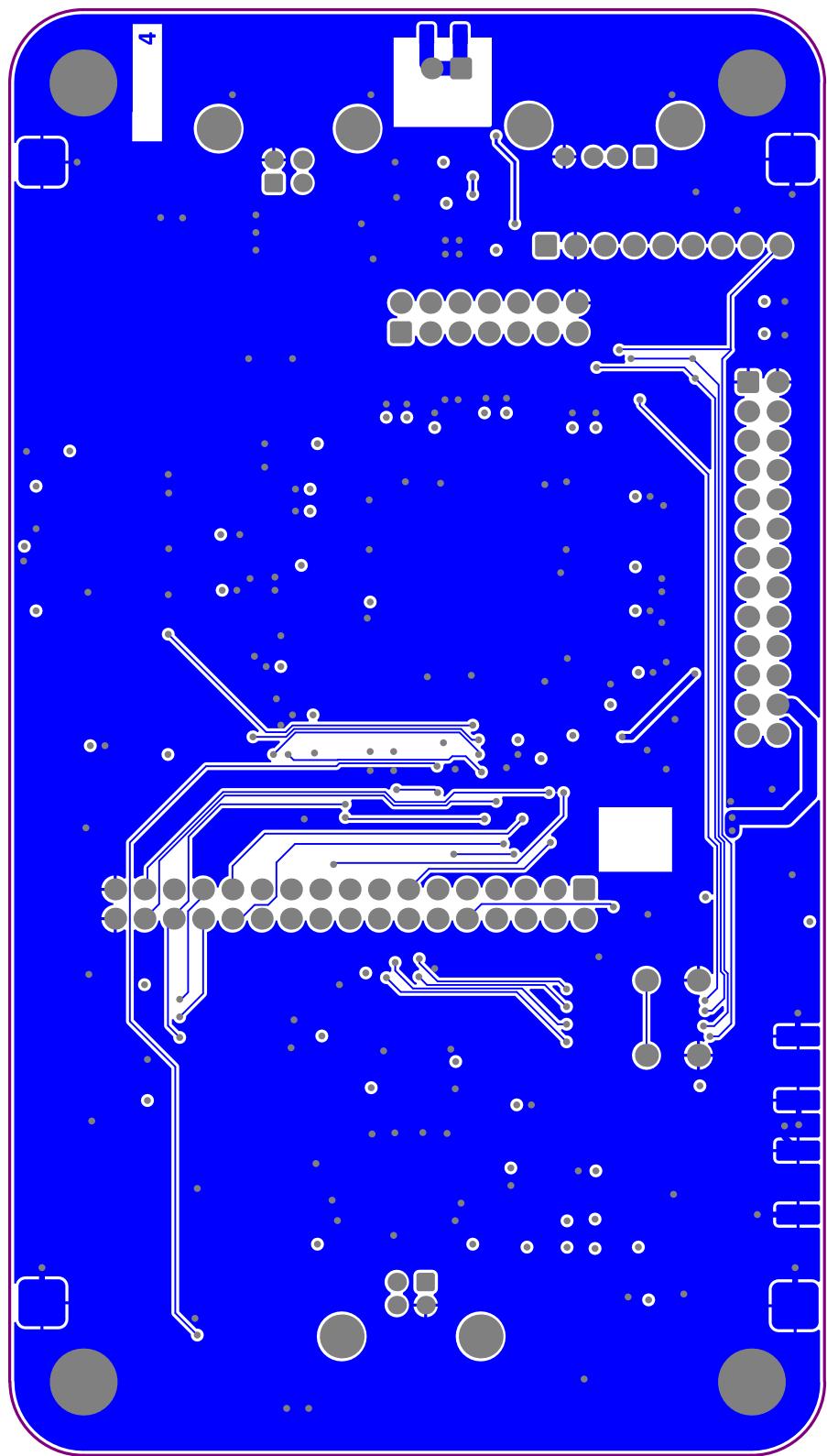


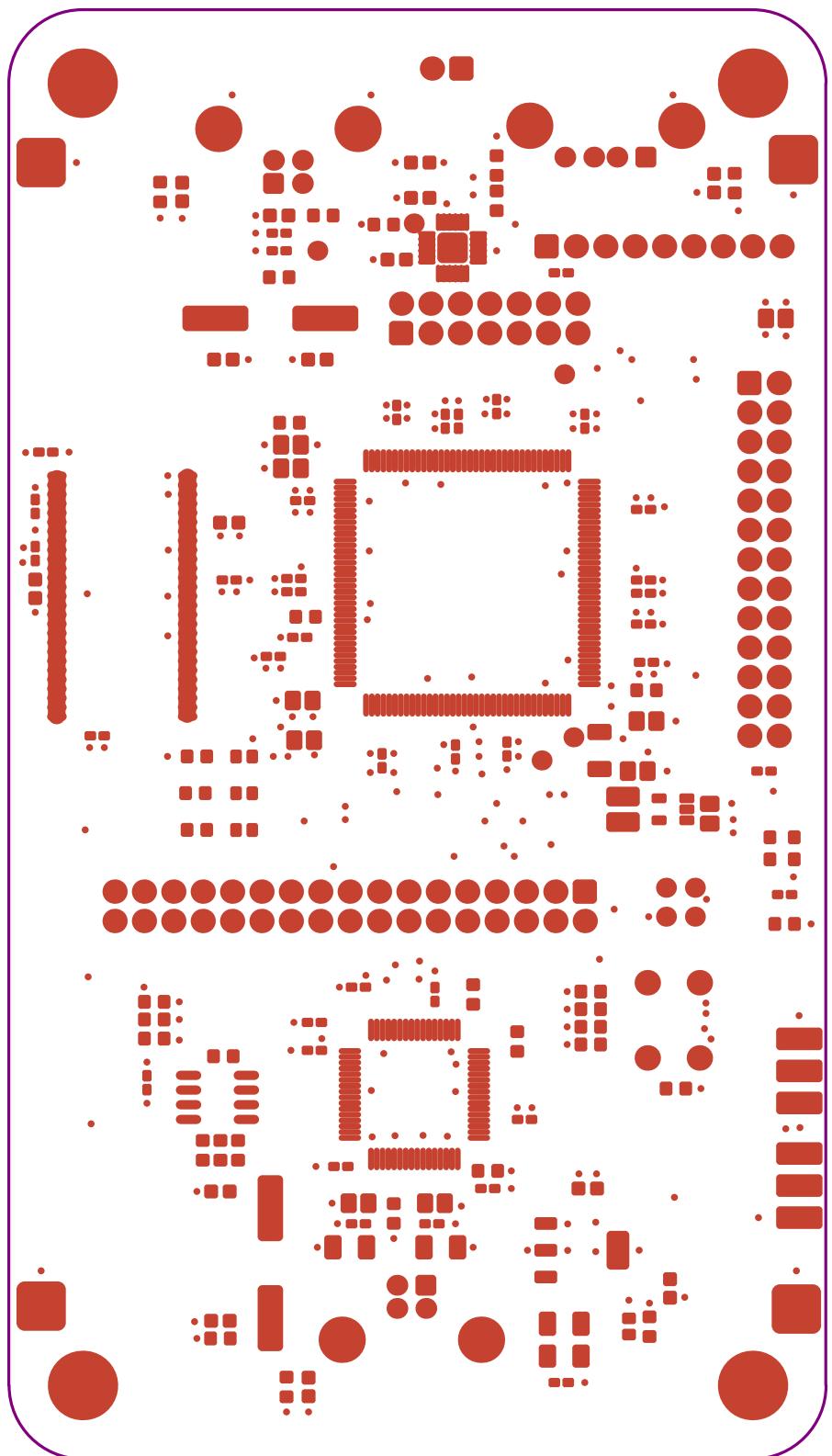
OpenVizsla v3.2
(c) 2013,2014 bushing

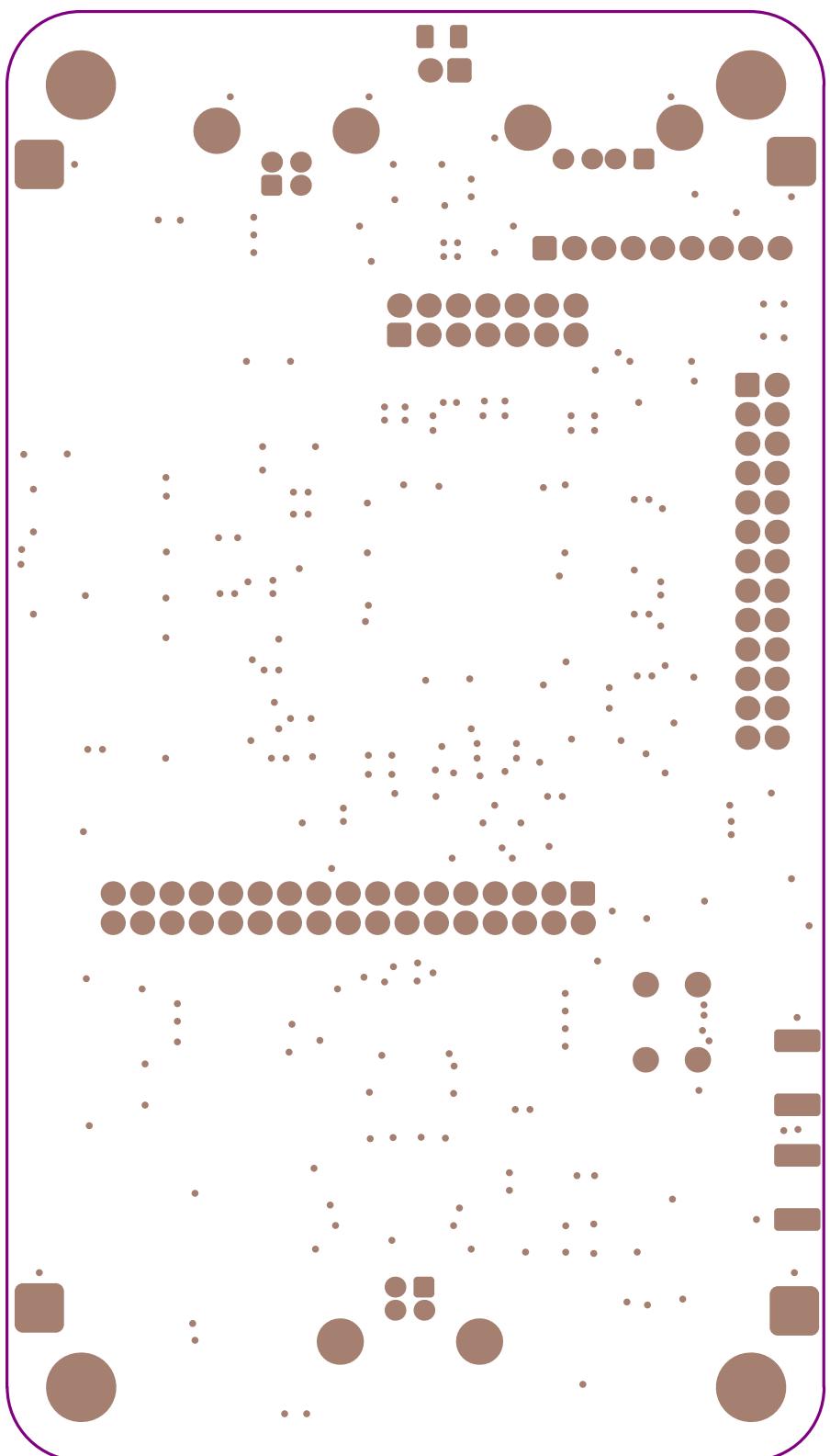


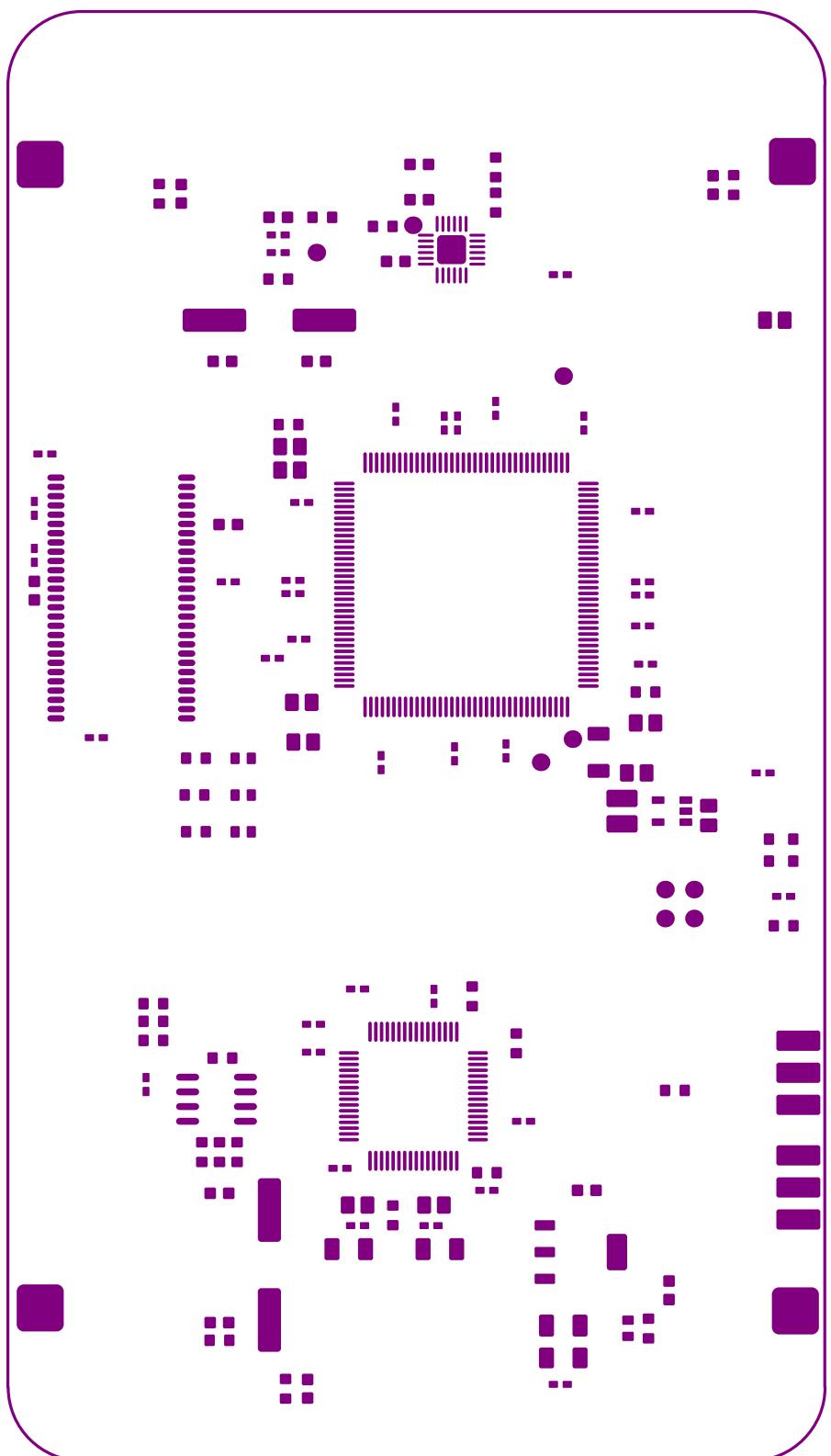


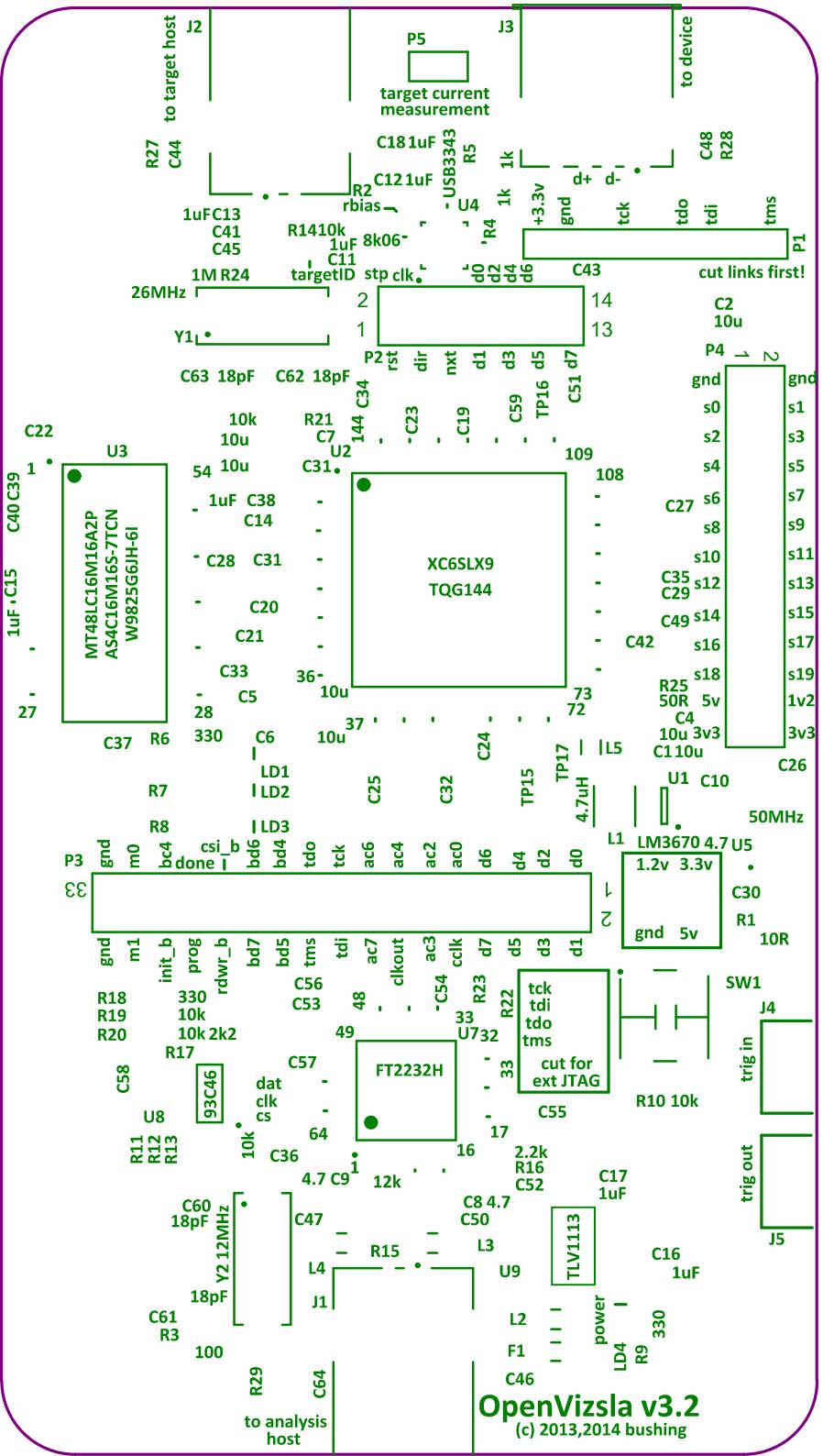












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