

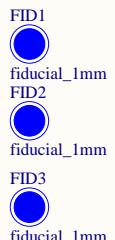
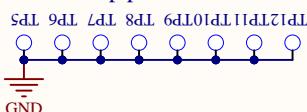
A

B

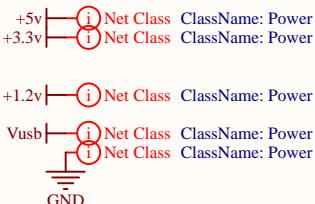
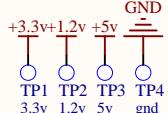
C

D

Ground clip pads



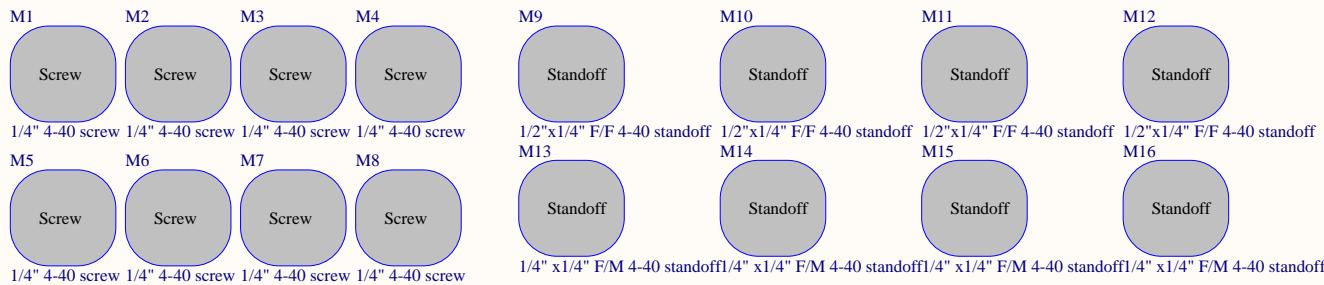
Power supply test points, top side



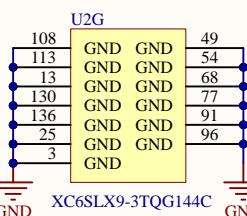
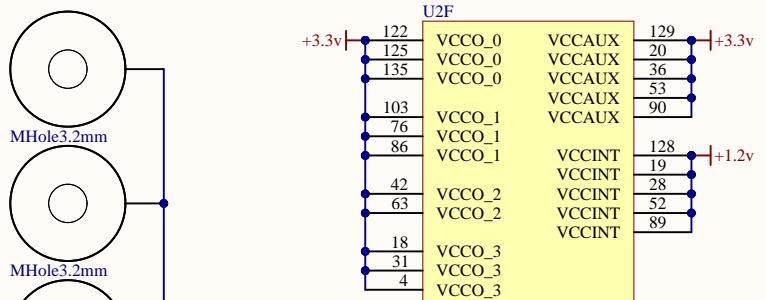
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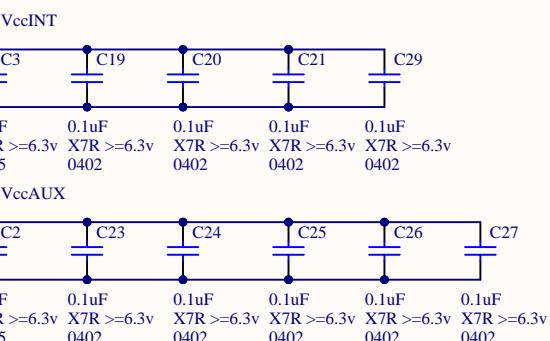
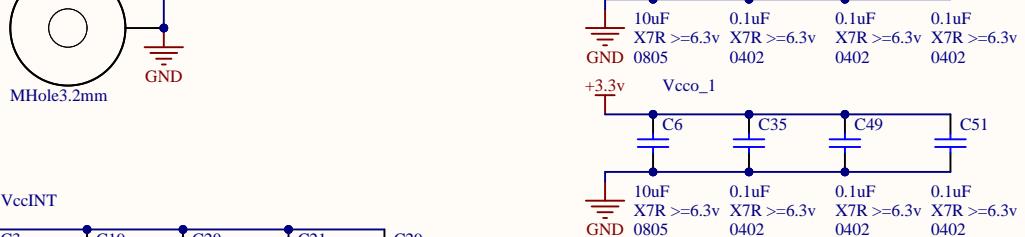
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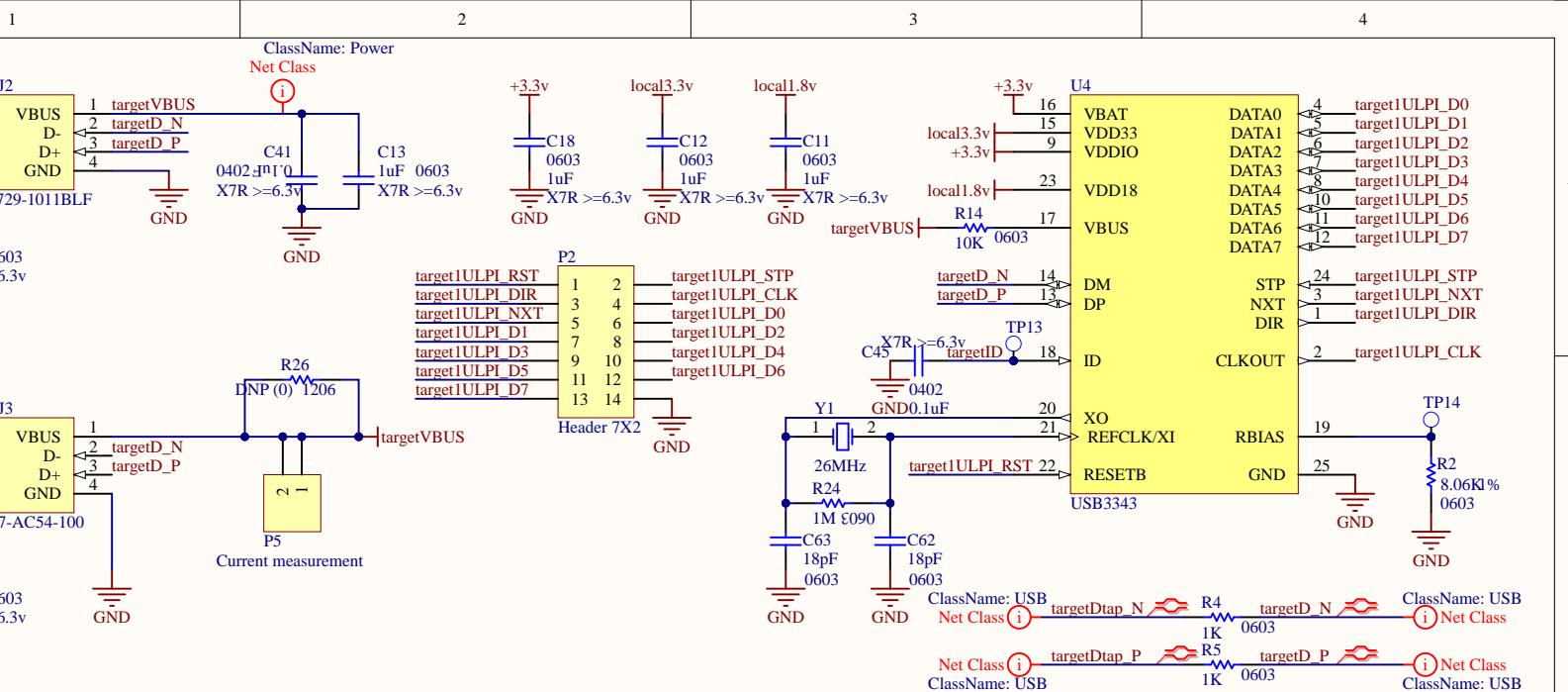


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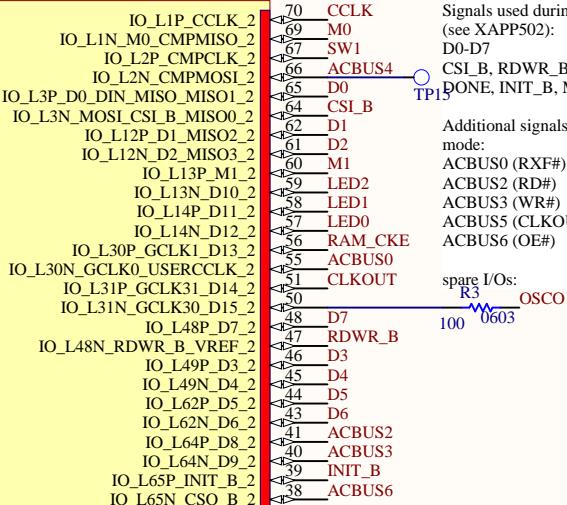


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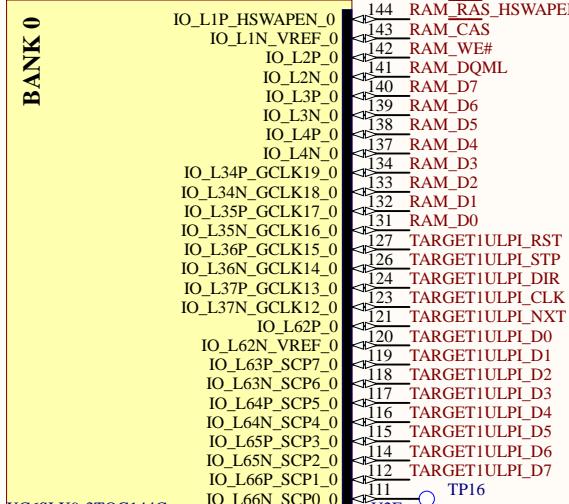


U2C

BANK 2

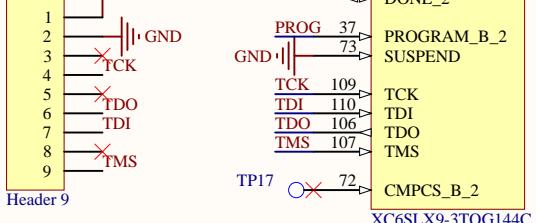
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U2A



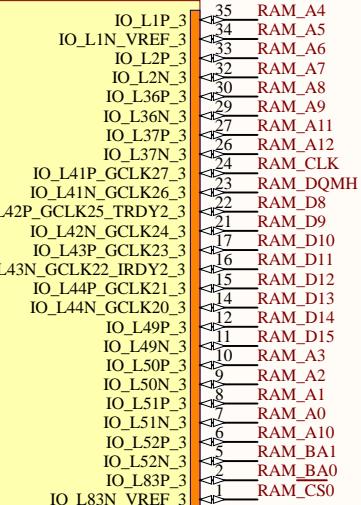
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P1

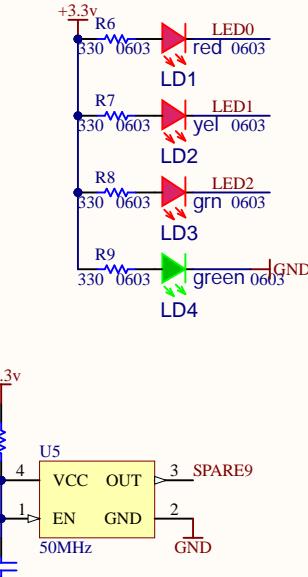
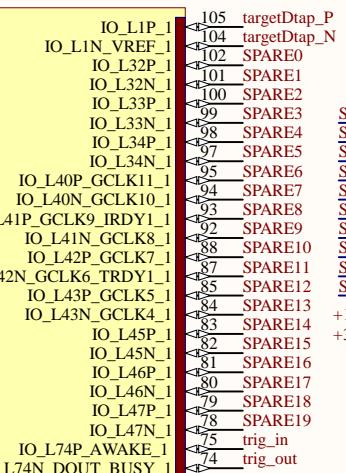


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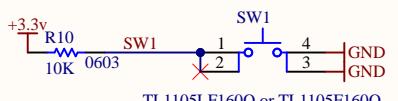
U2D

BANK 3

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**BANK 1**

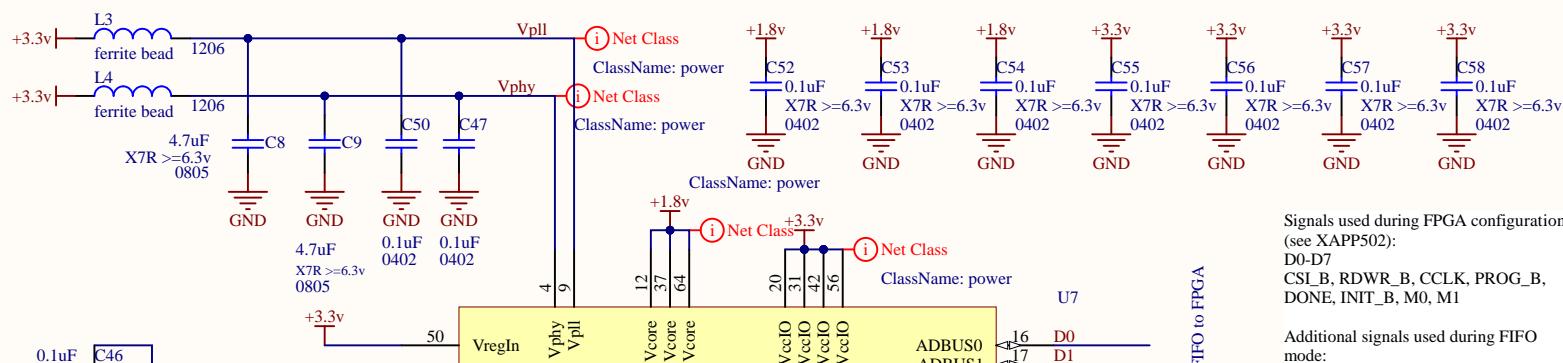
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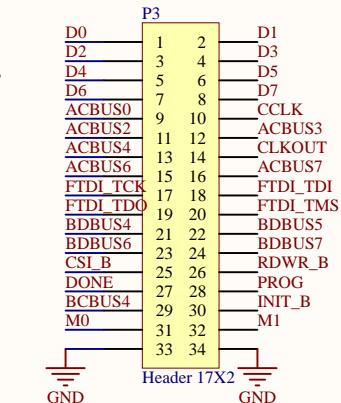
A



Signals used during FPGA configuration
(see XAPP502):
D0-D7
CSI_B, RDWR_B, CCLK, PROG_B,
DONE, INIT_B, M0, M1

Additional signals used during FIFO mode:
ACBUS0 (RXF#)
ACBUS2 (RD#)
ACBUS3 (WR#)
ACBUSS (CLKOUT)
ACBUS6 (OE#)

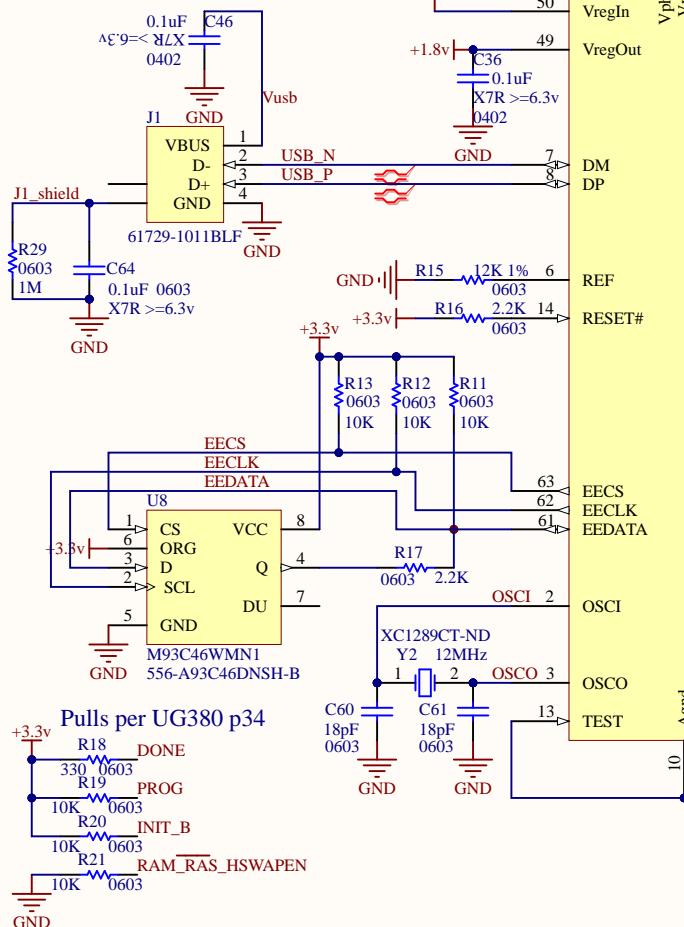
spare I/Os:



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Title		Revision
Size	Number	
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Date:	3/24/2021	Sheet of
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B

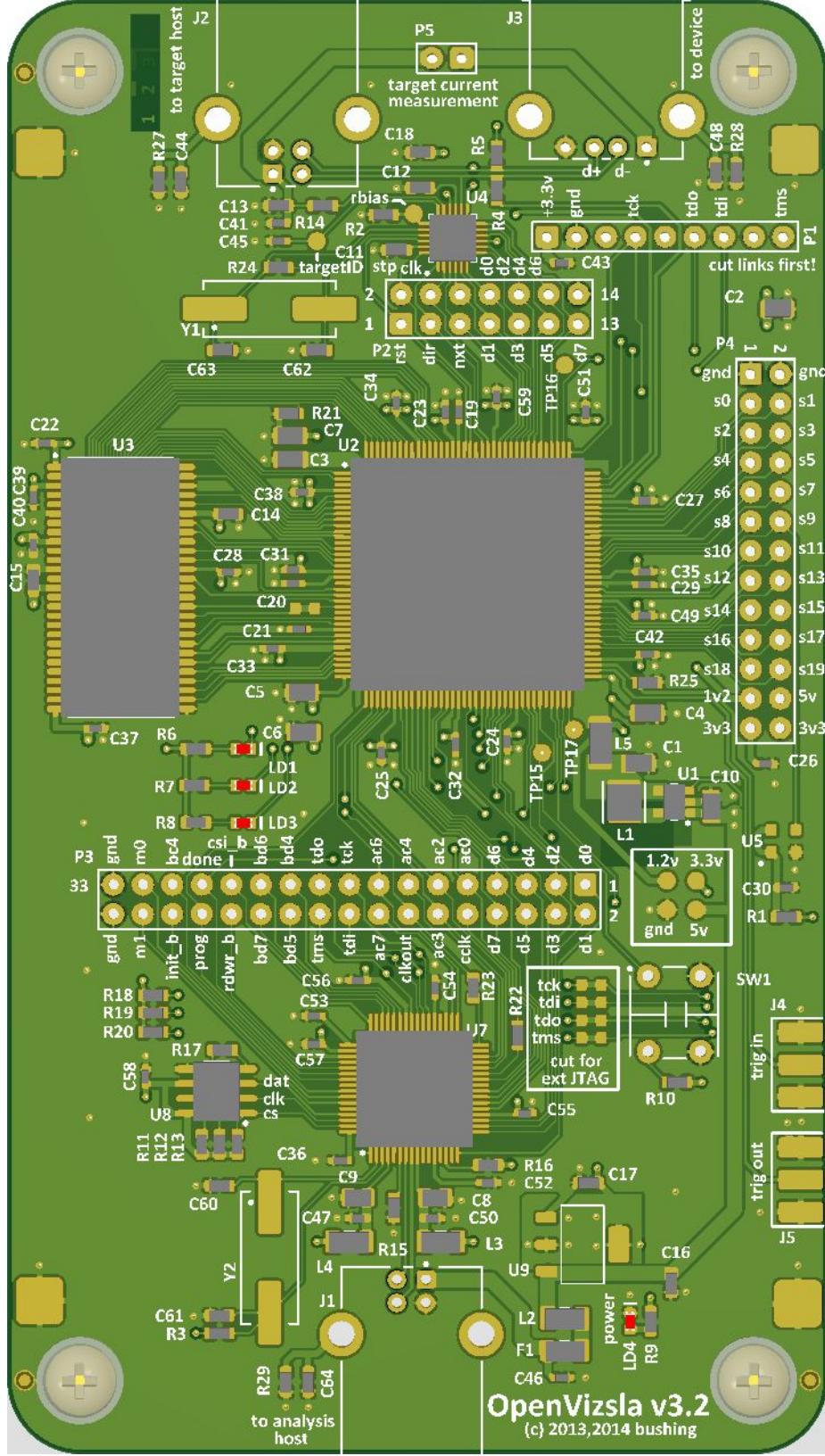


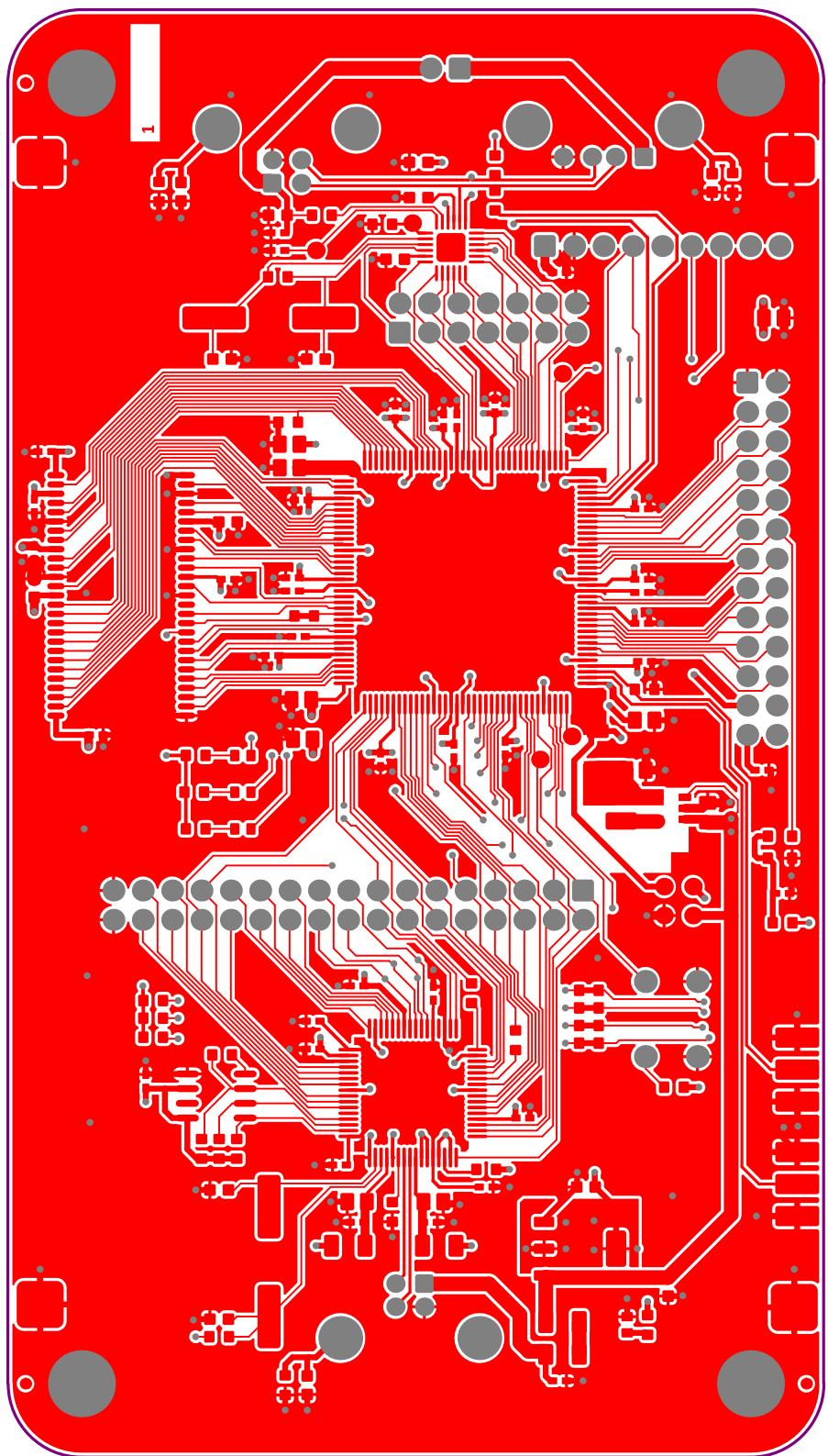
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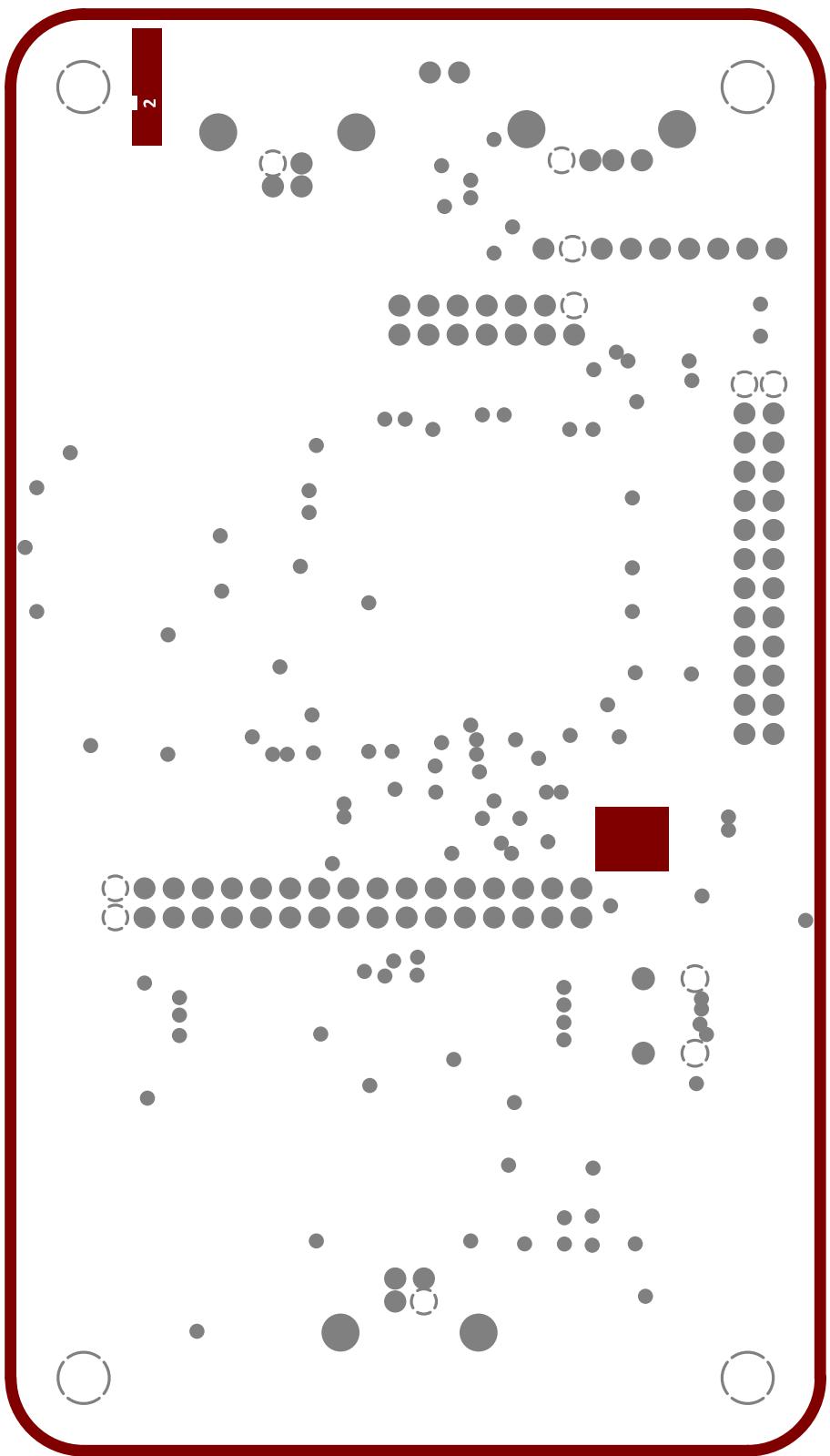
Pulls per UG380 p34

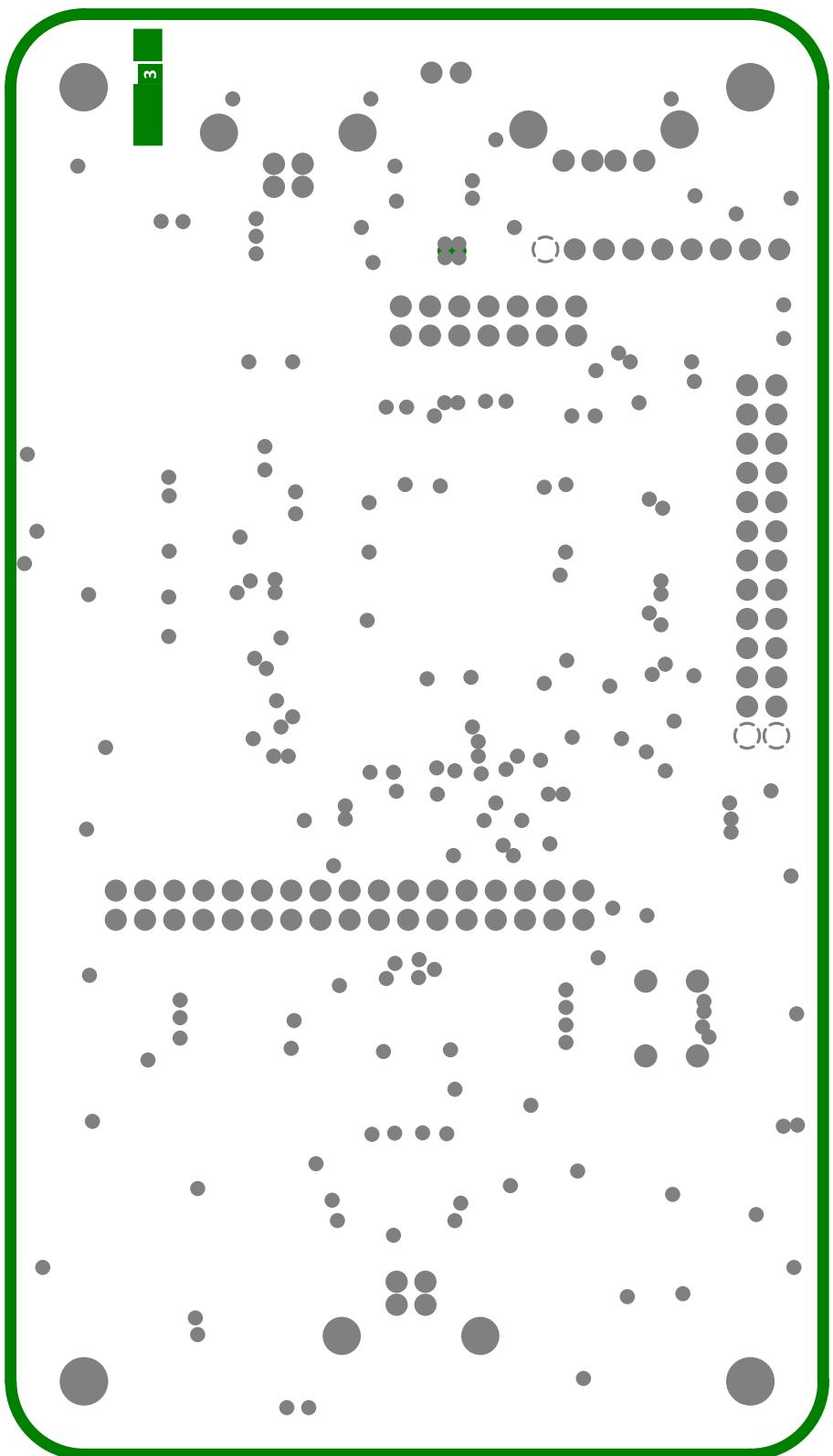
- +3.3v → R18 (DONE)
- 330 0603 → R19 (PROG)
- 10K 0603 → R20 (INIT_B)
- 10K 0603 → R21 (RAM_RAS_HSWAPEN)
- 10K 0603 → GND

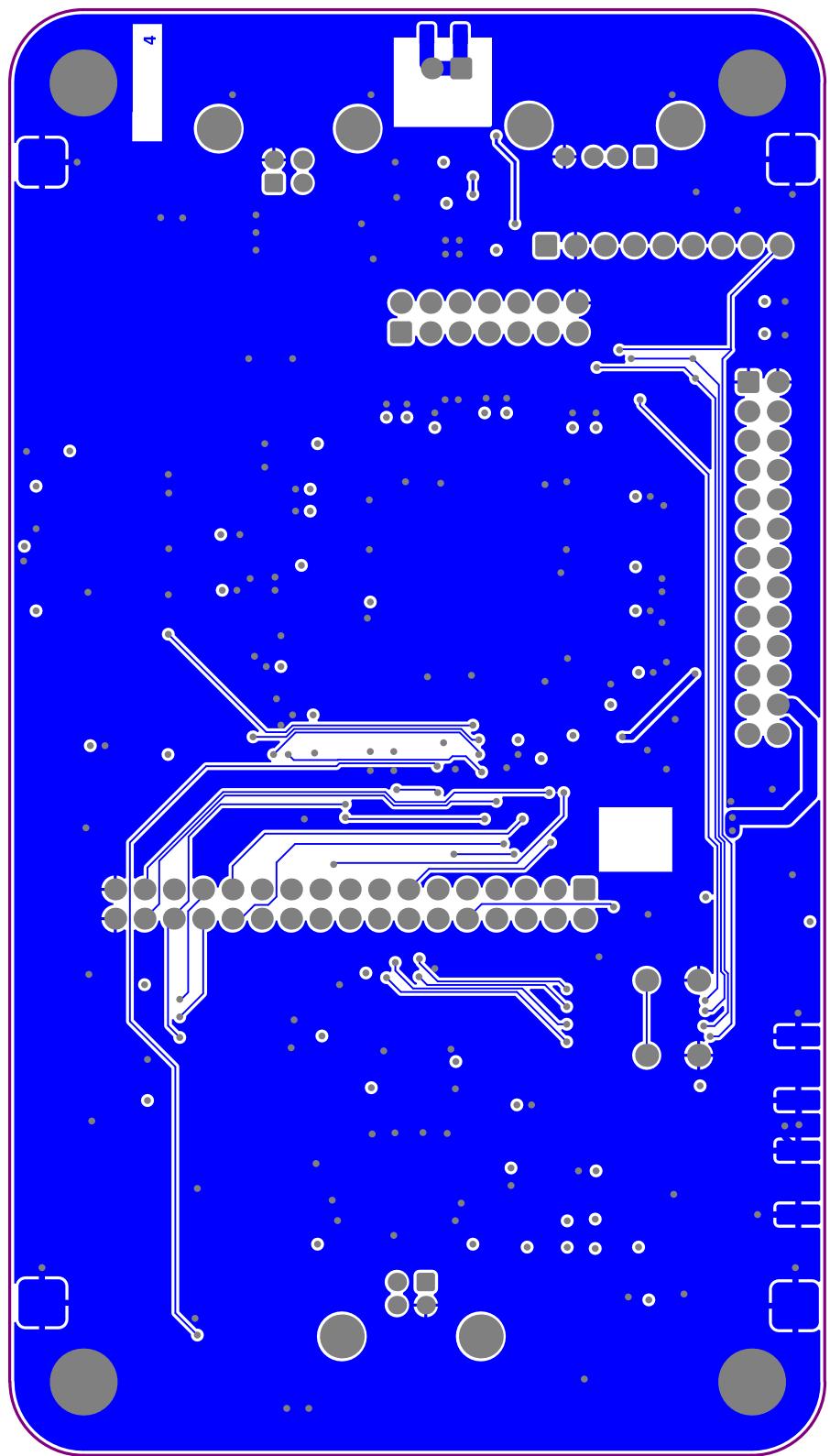
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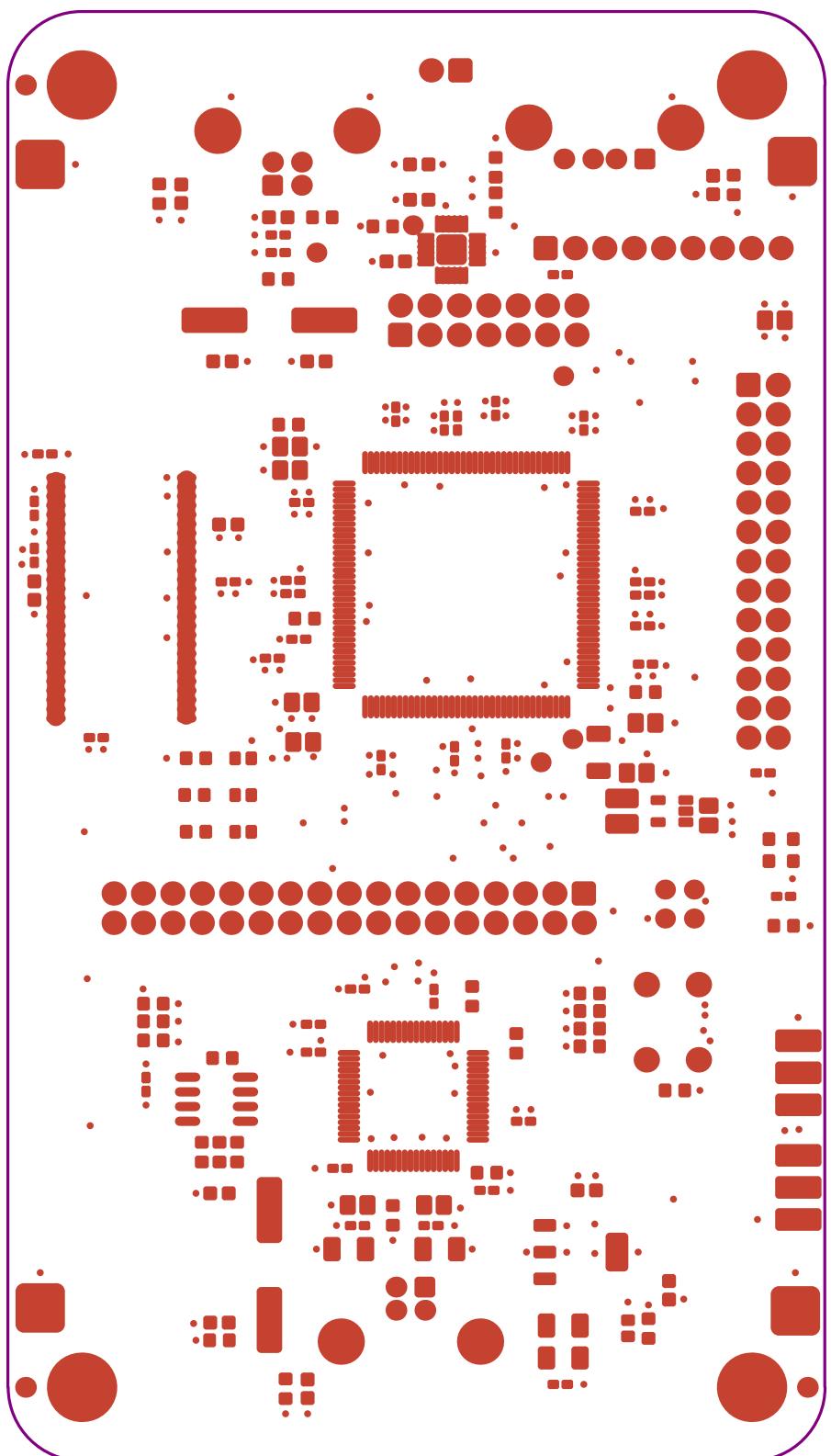


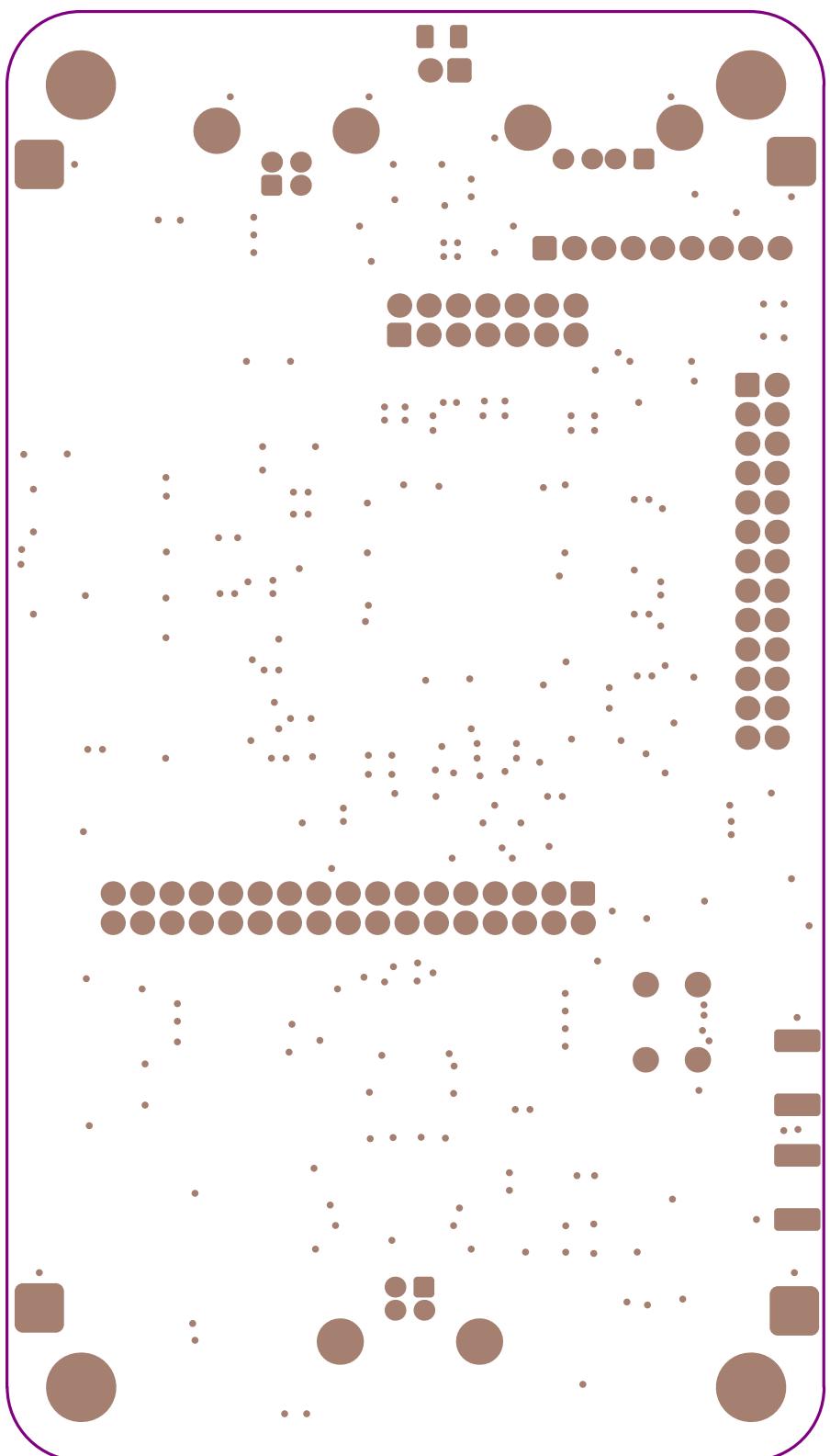


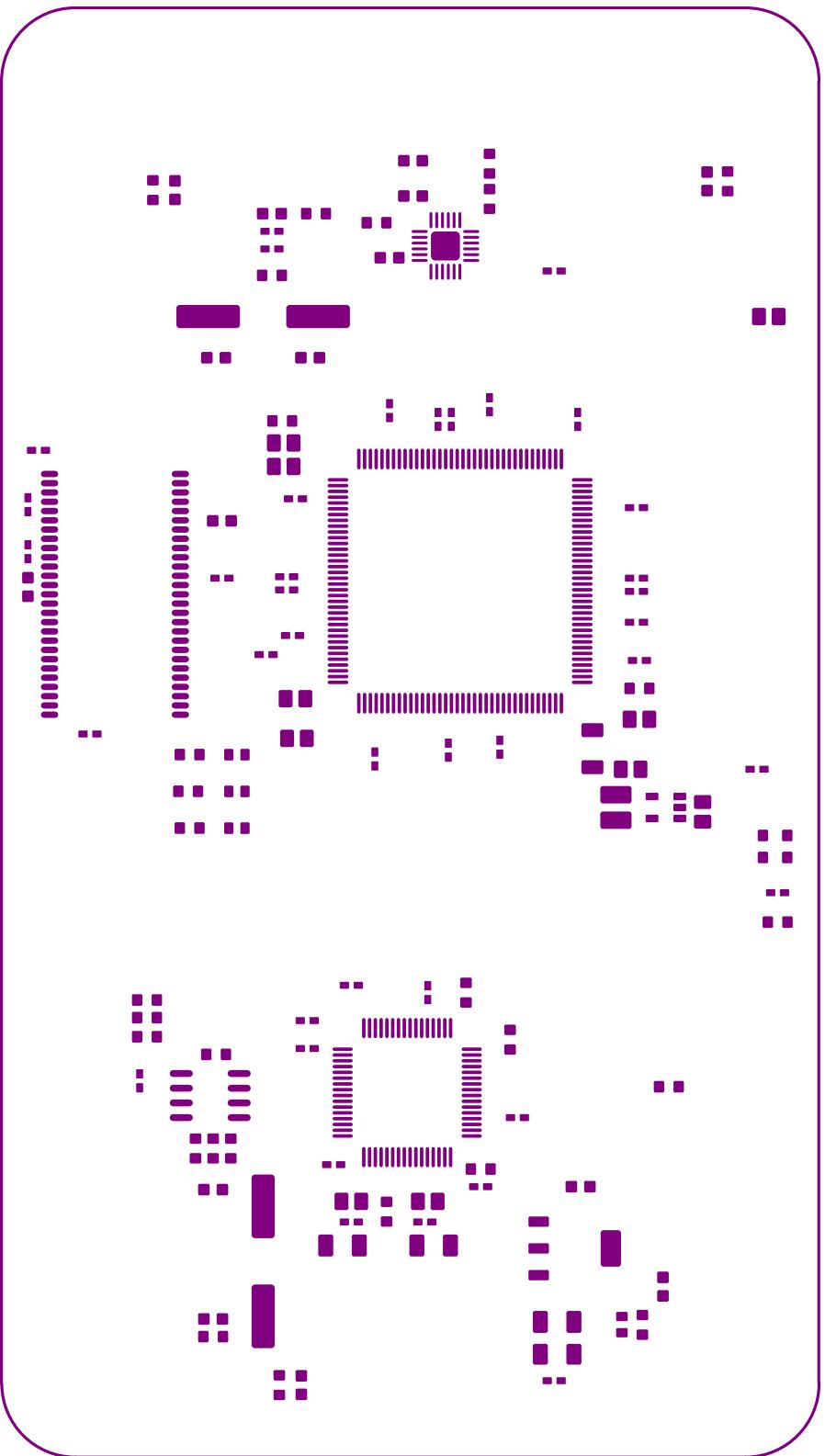


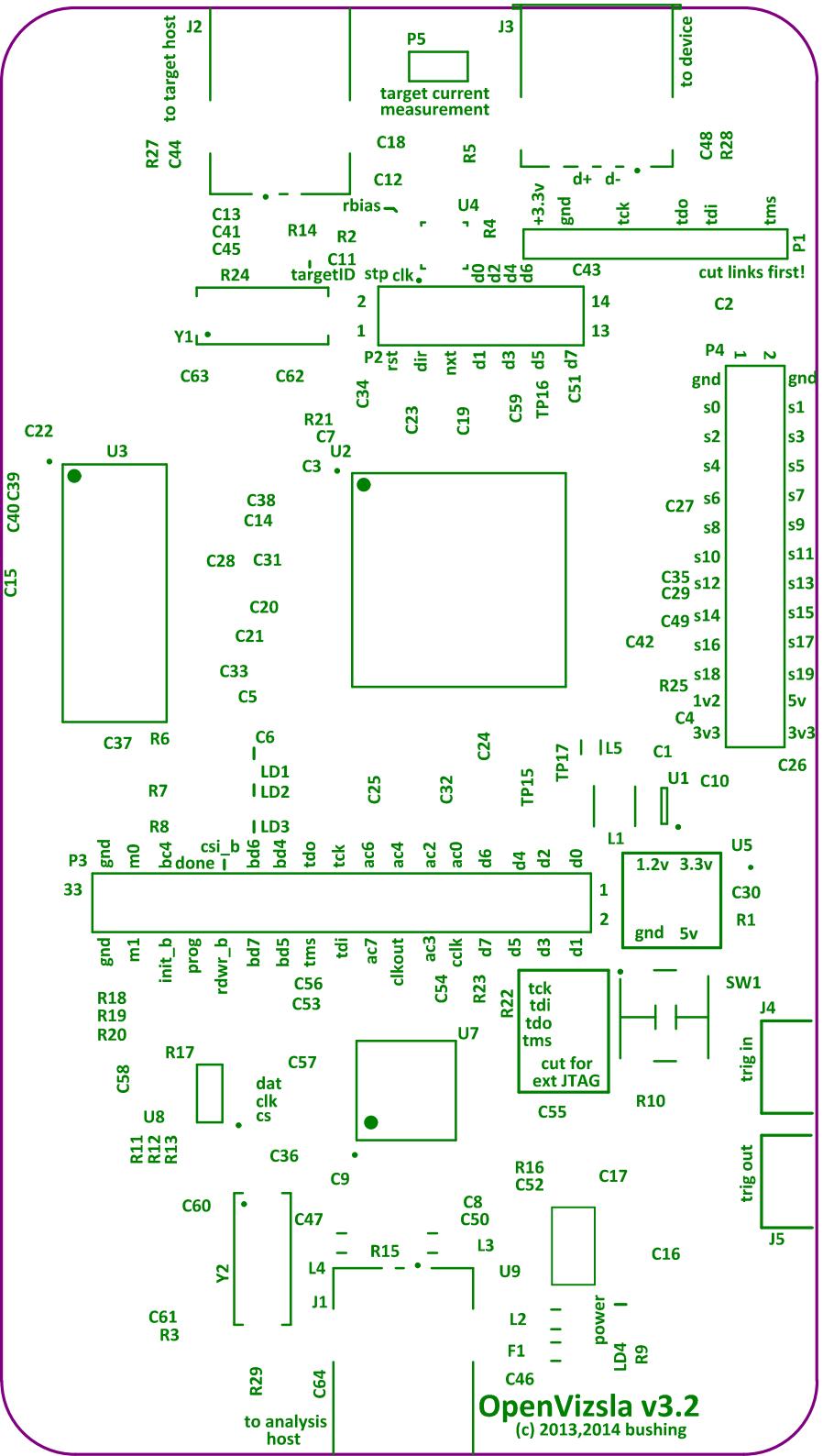












- 65 -

cut trace for
target current
measurement

cut links first	long	long
0s	1s	
2s	3s	
4s	5s	
6s	7s	
8s	9s	
0t1s	1t1s	
1t1s	2t1s	
4t1s	5t1s	
6t1s	7t1s	
8t1s	9t1s	
2v1s	v1s	
4v1s	5v1s	

D-
D+
Aplus
Bplus

q1	bl
q2	blng
q3	blng
q4	blng
q5	blng
q6	blng
q7	blng
q8	blng
q9	blng
q10	blng
q11	blng
q12	blng
q13	blng
q14	blng
q15	blng
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q96	blng
q97	blng
q98	blng
q99	blng
q100	blng

Vnsb
Bud



