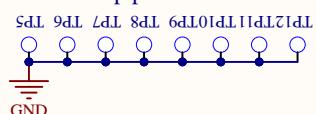
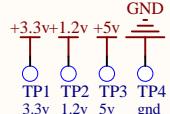


B

Ground clip pads



Power supply test points, top side



+5v
+3.3v
+1.2v
TP1 TP2 TP3 TP4
3.3v 1.2v 5v gnd

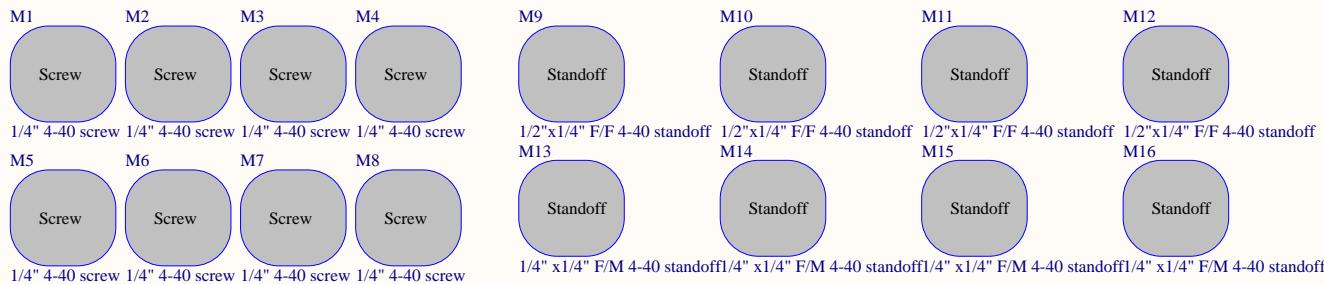
+5v Net Class
+3.3v Net Class
+1.2v Net Class
Vusb Net Class
GND

ClassName: Power
ClassName: Power

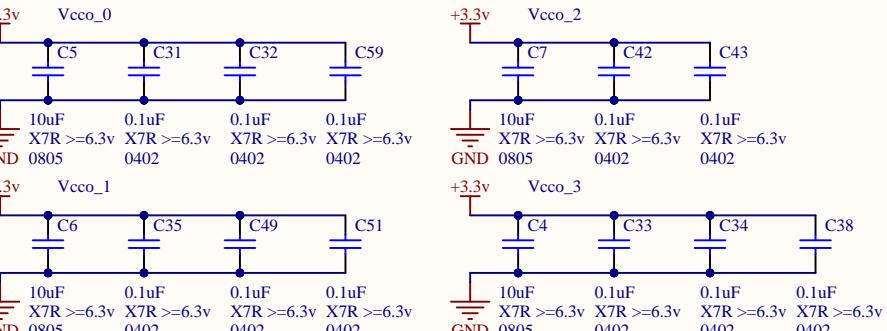
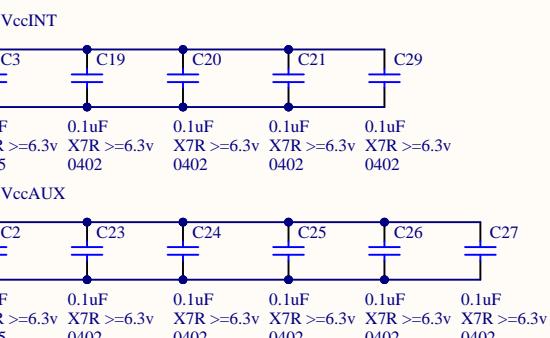
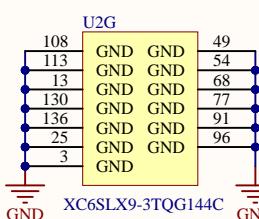
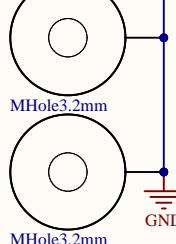
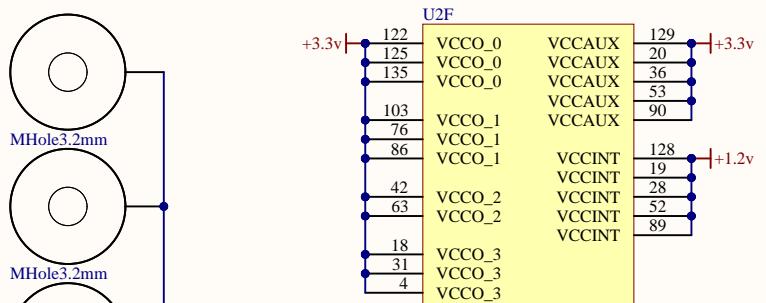
Copyrights: CC-BY-SA 3.0 Patents: Apache 2.0

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A

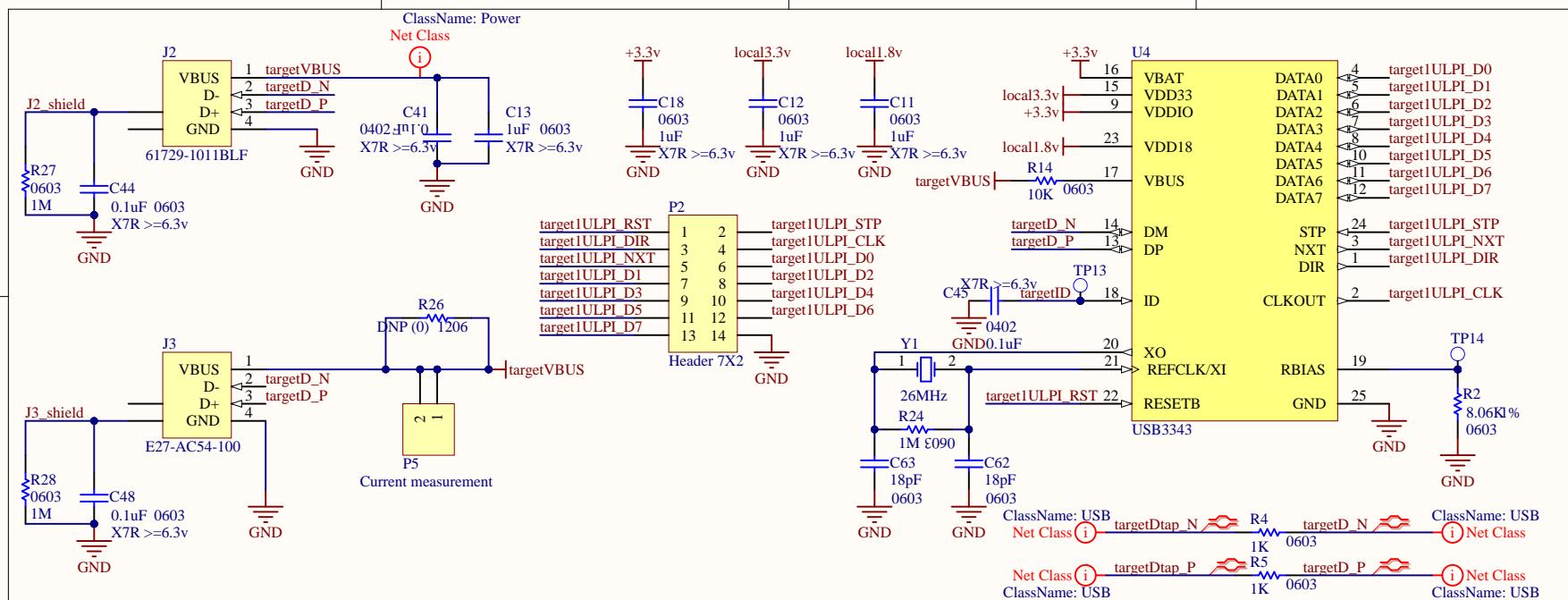


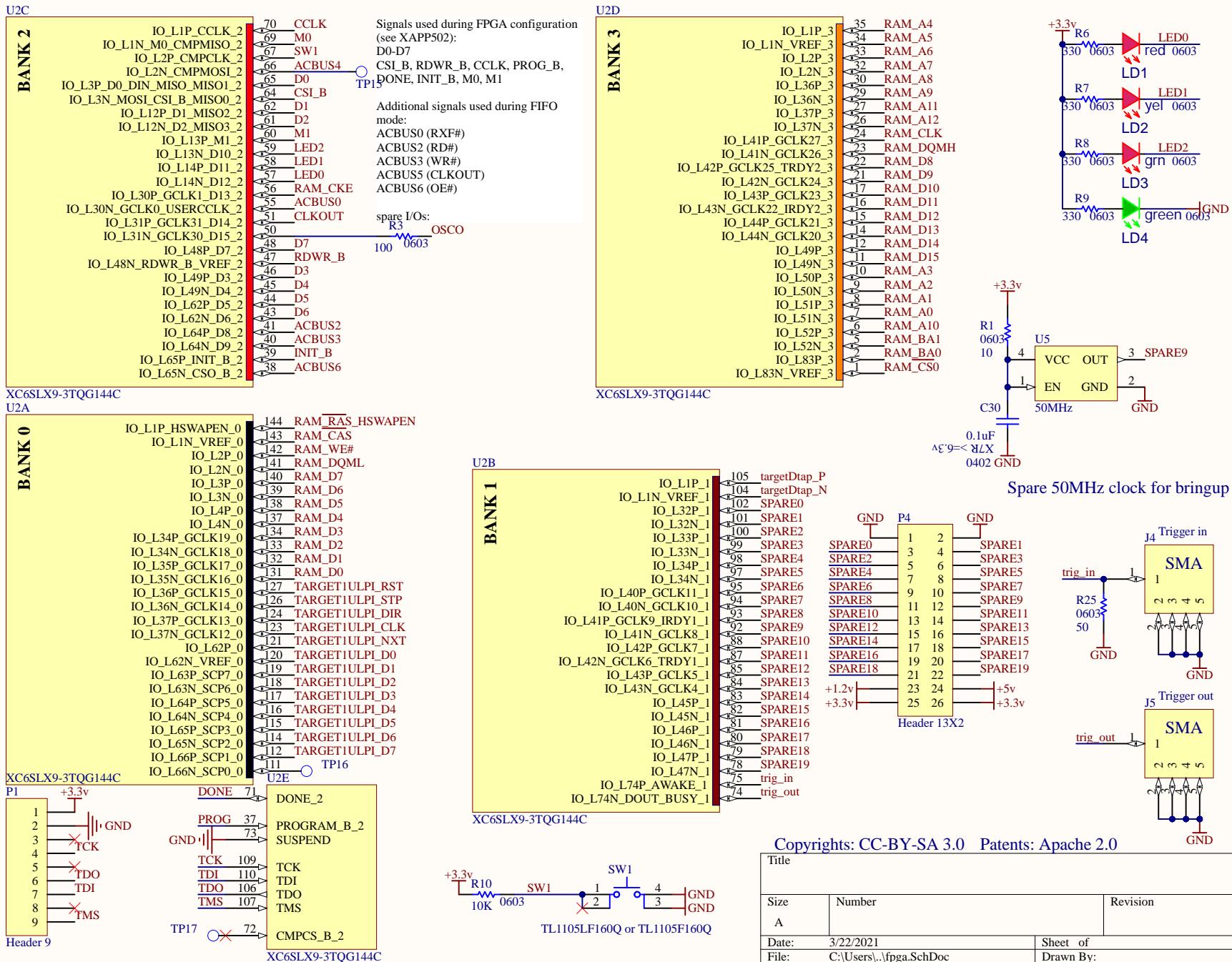
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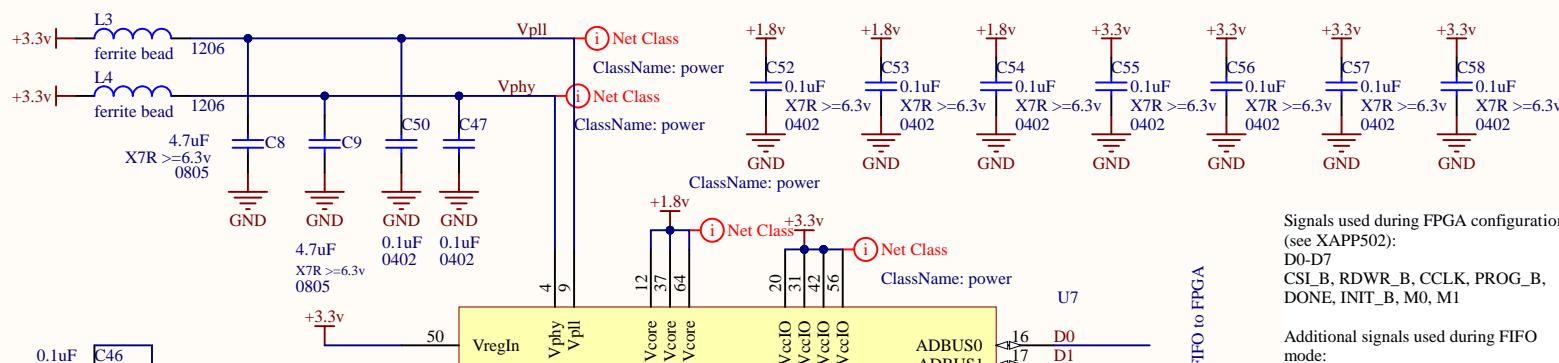
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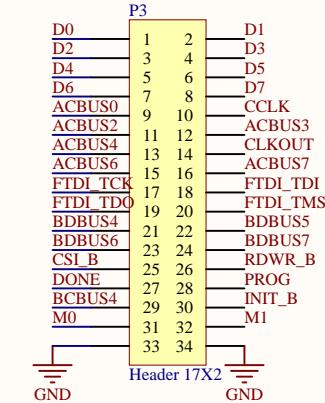
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Signals used during FPGA configuration
(see XAPP502):
D0-D7
CSI_B, RDWR_B, CCLK, PROG_B,
DONE, INIT_B, M0, M1

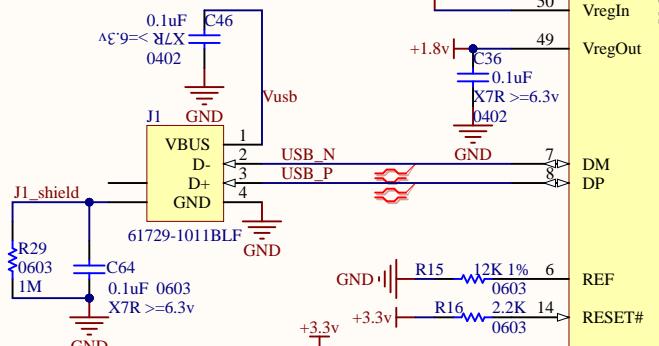
Additional signals used during FIFO mode:
ACBUS0 (RXF#)
ACBUS2 (RD#)
ACBUS3 (WR#)
ACBUSS (CLKOUT)
ACBUS6 (OE#)

spare I/Os:

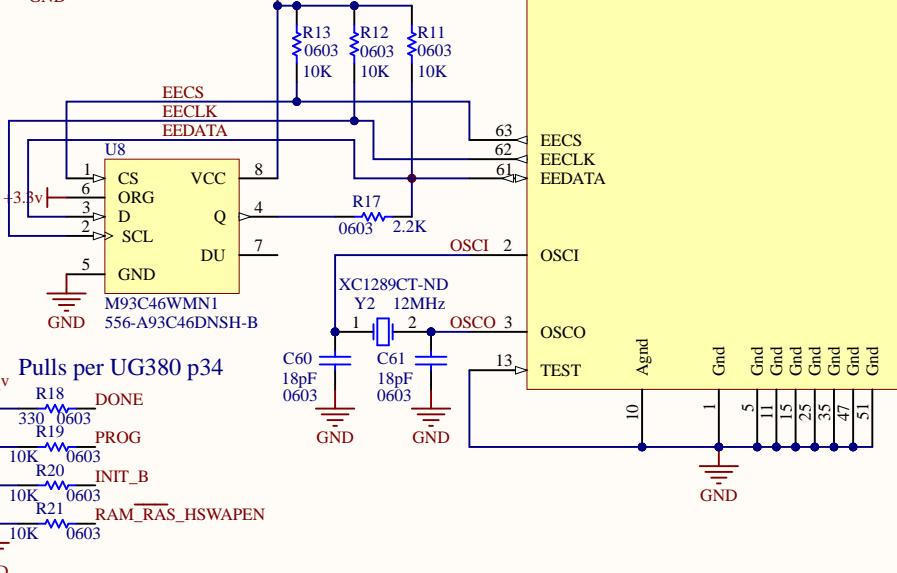


FT2232H

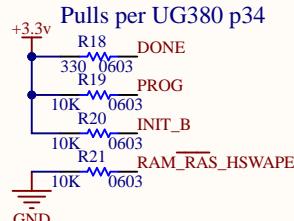
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C

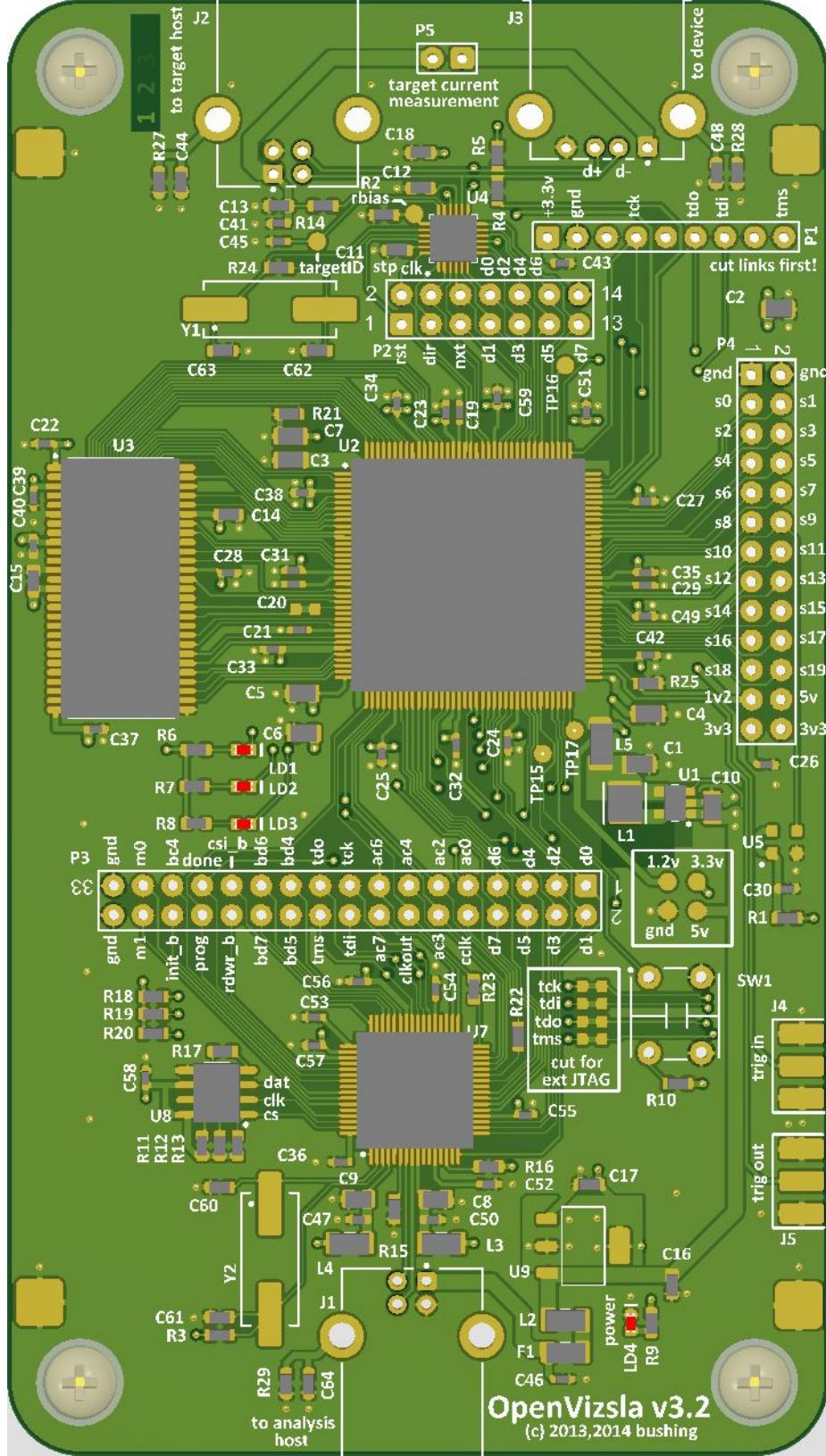


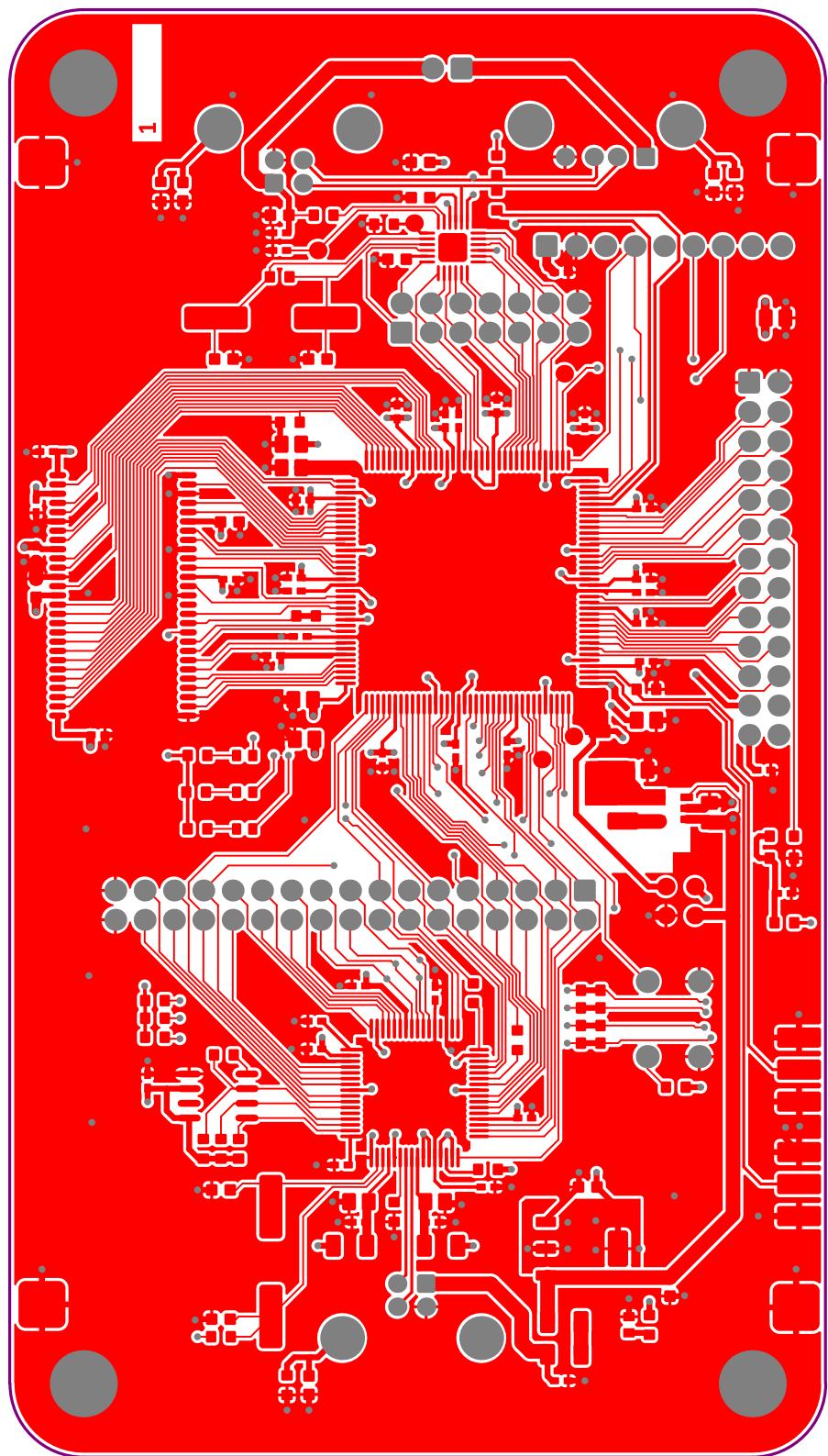
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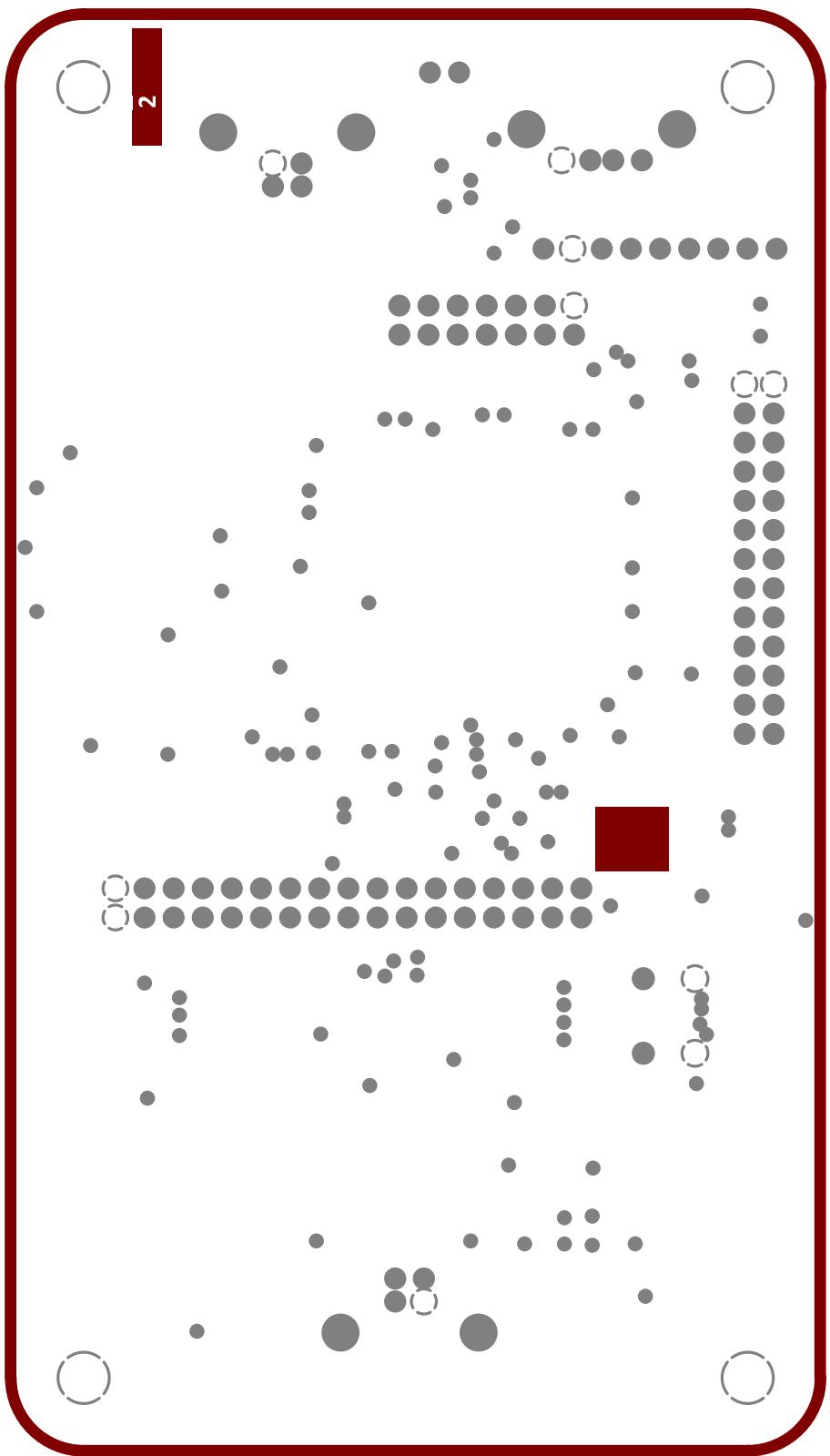


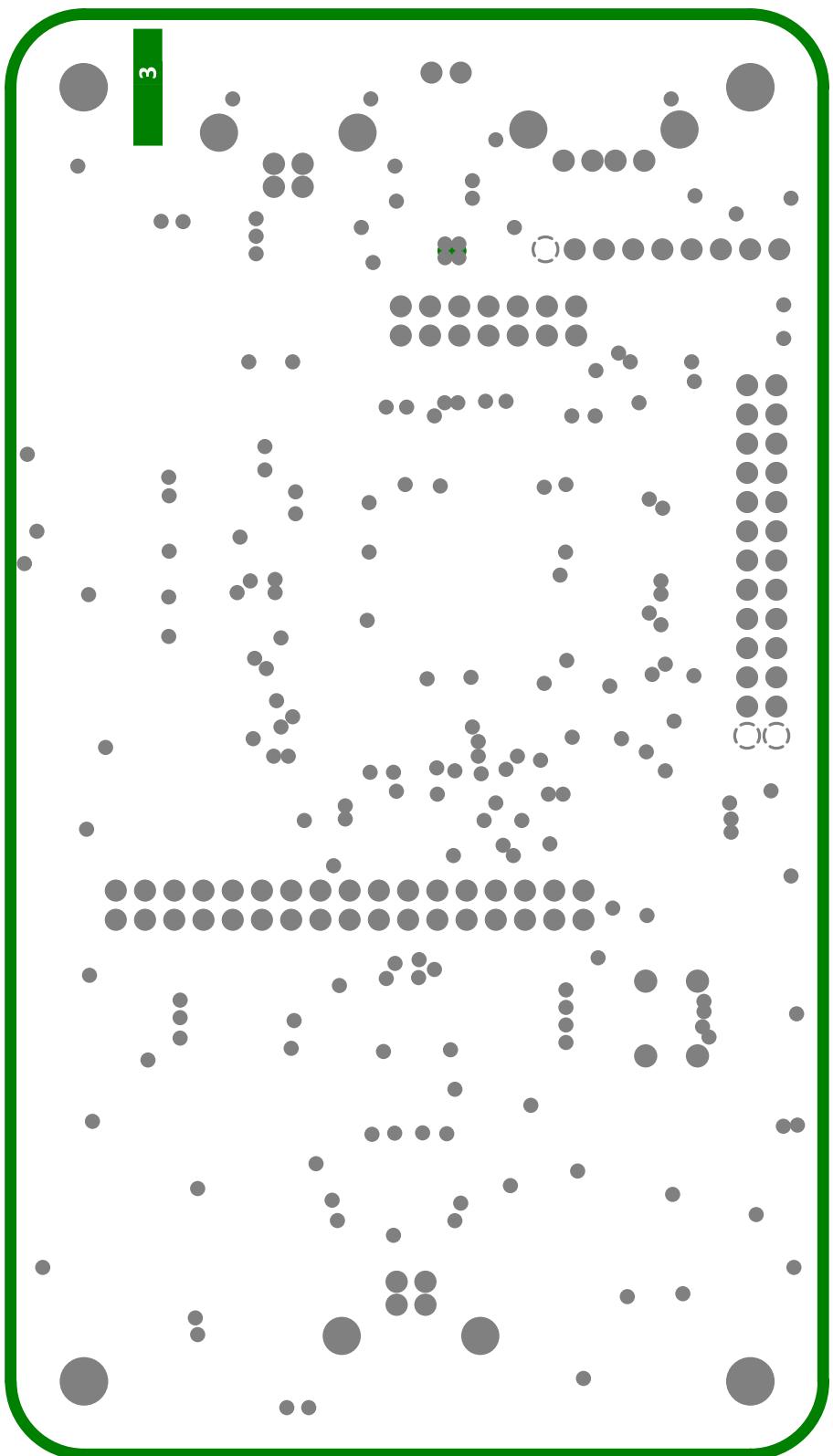
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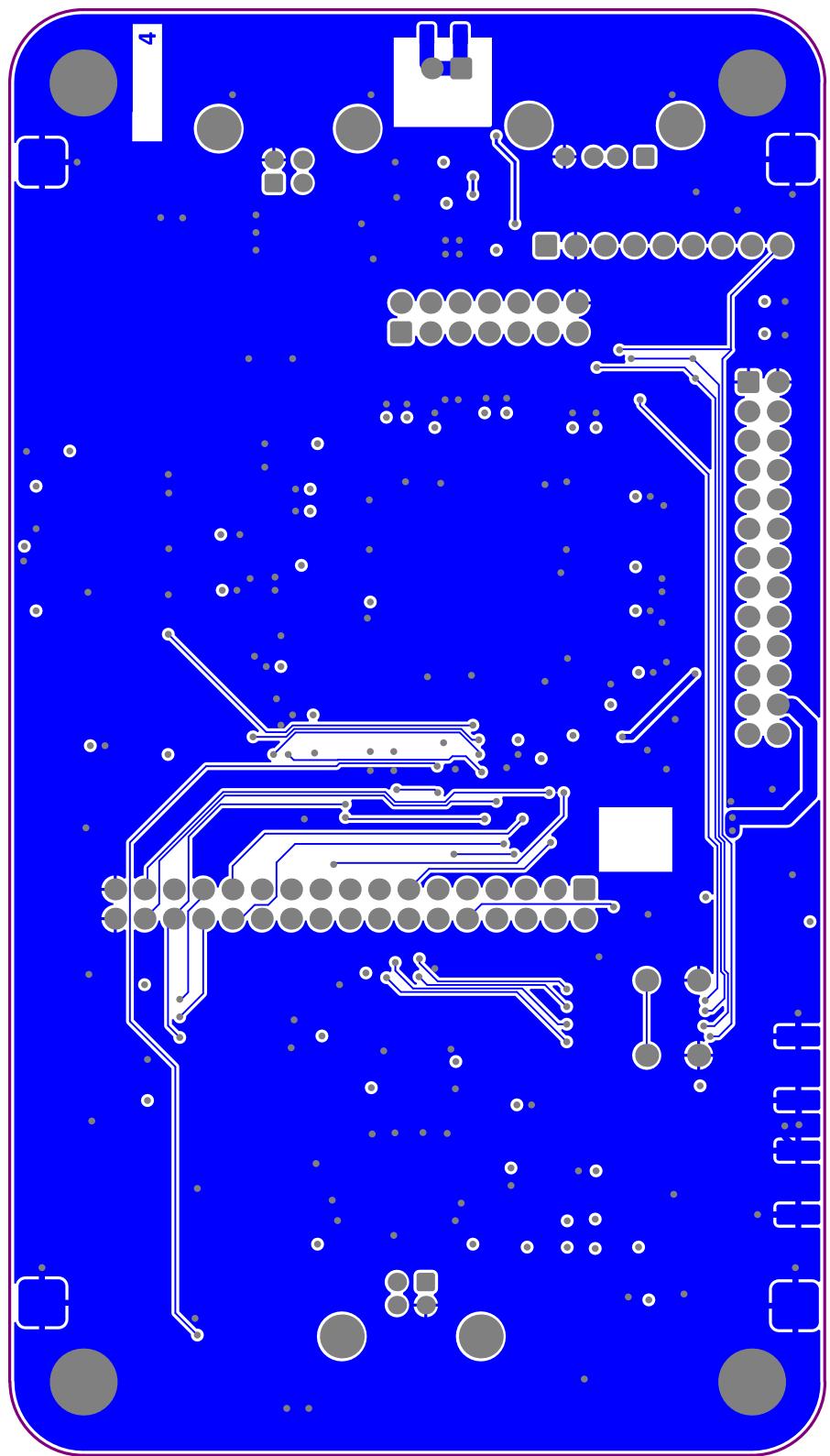
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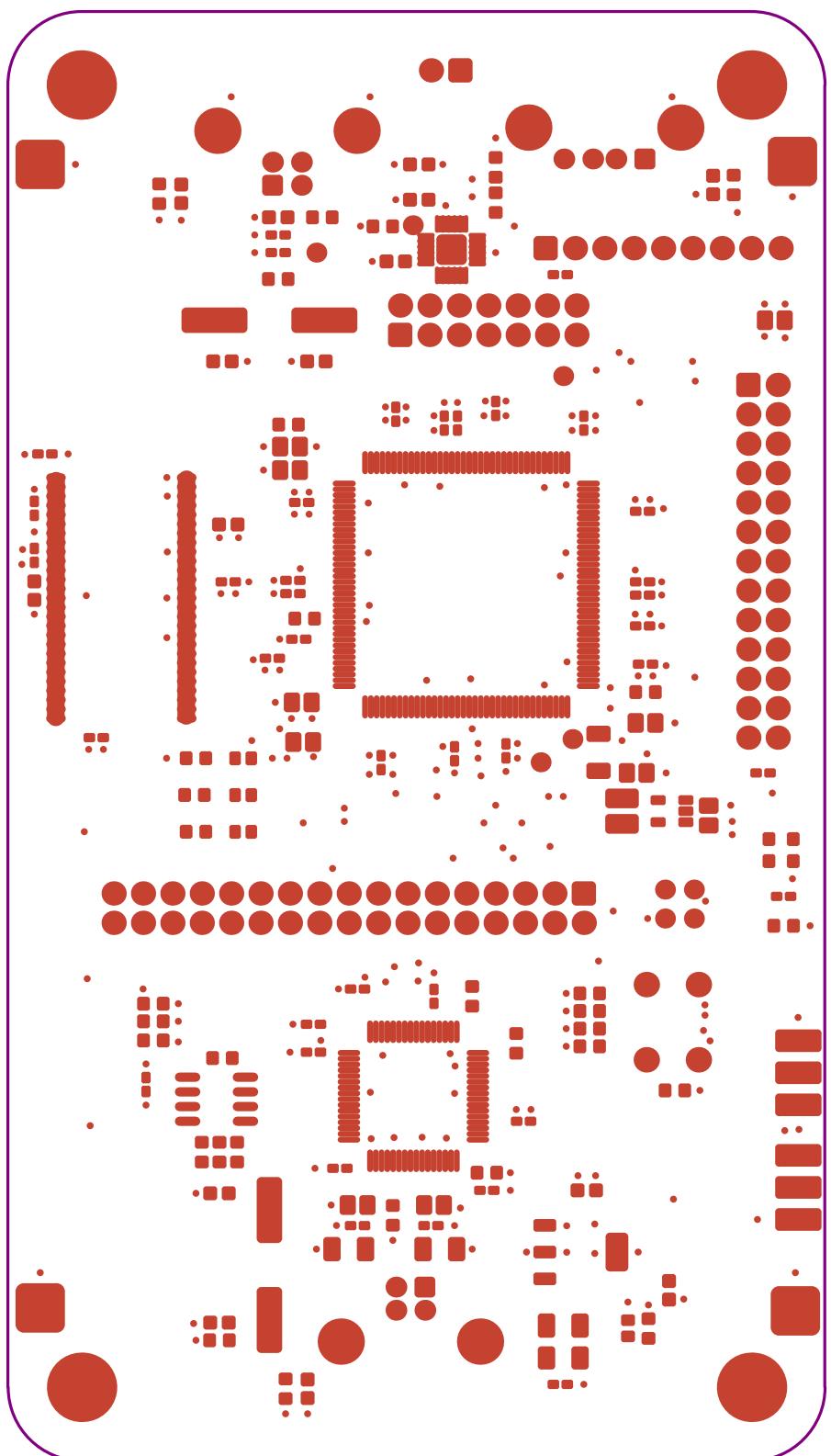


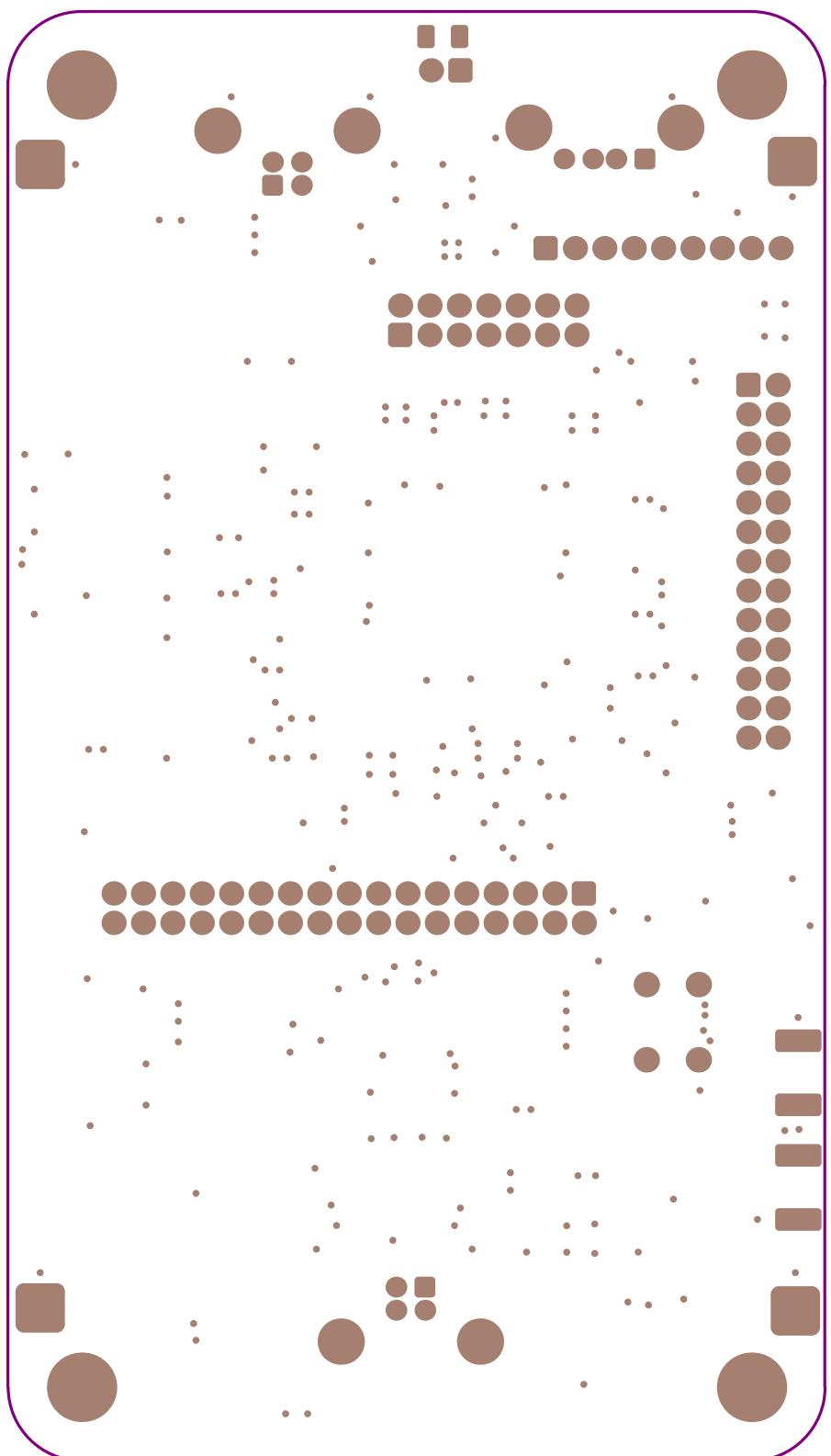


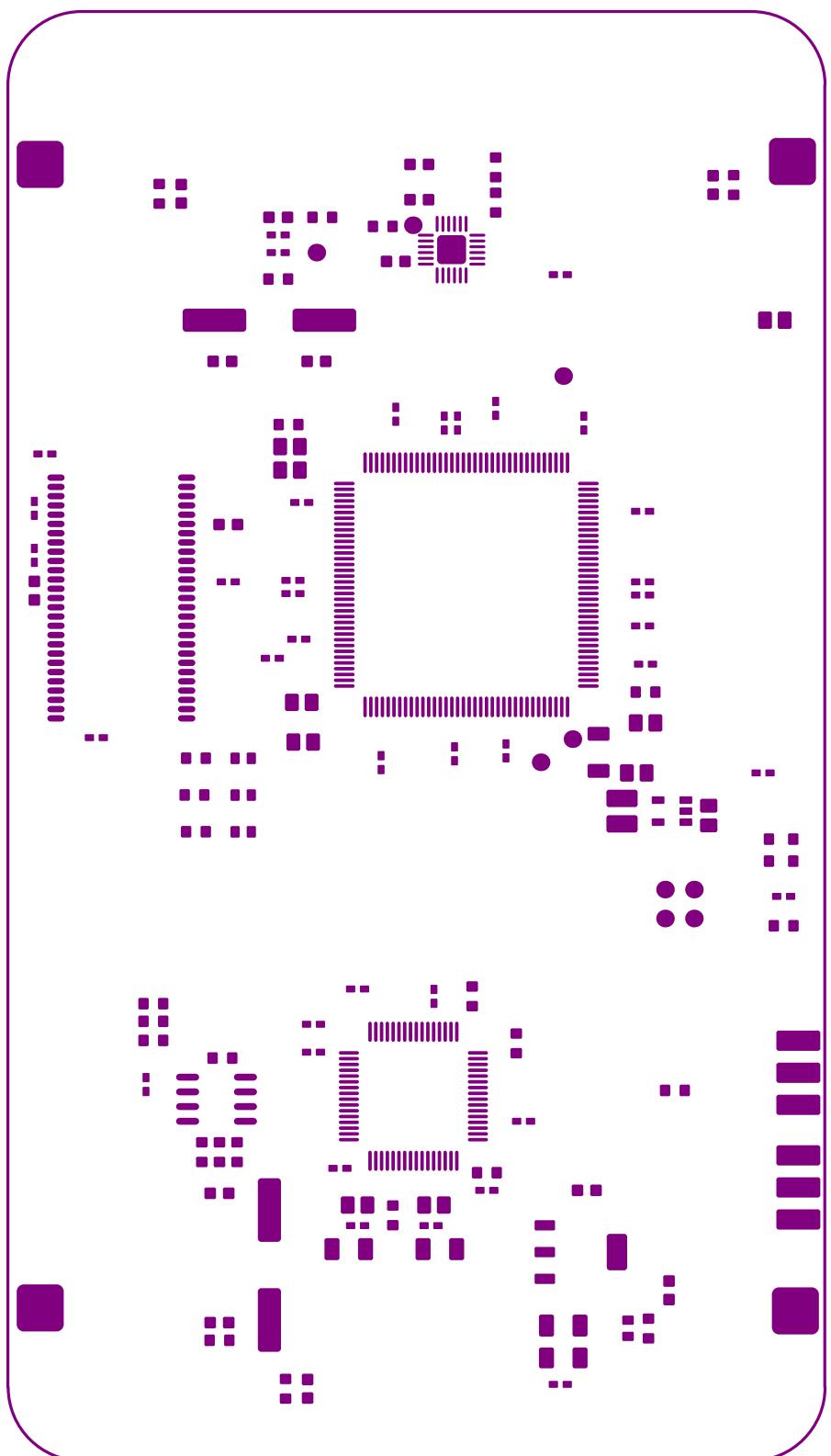


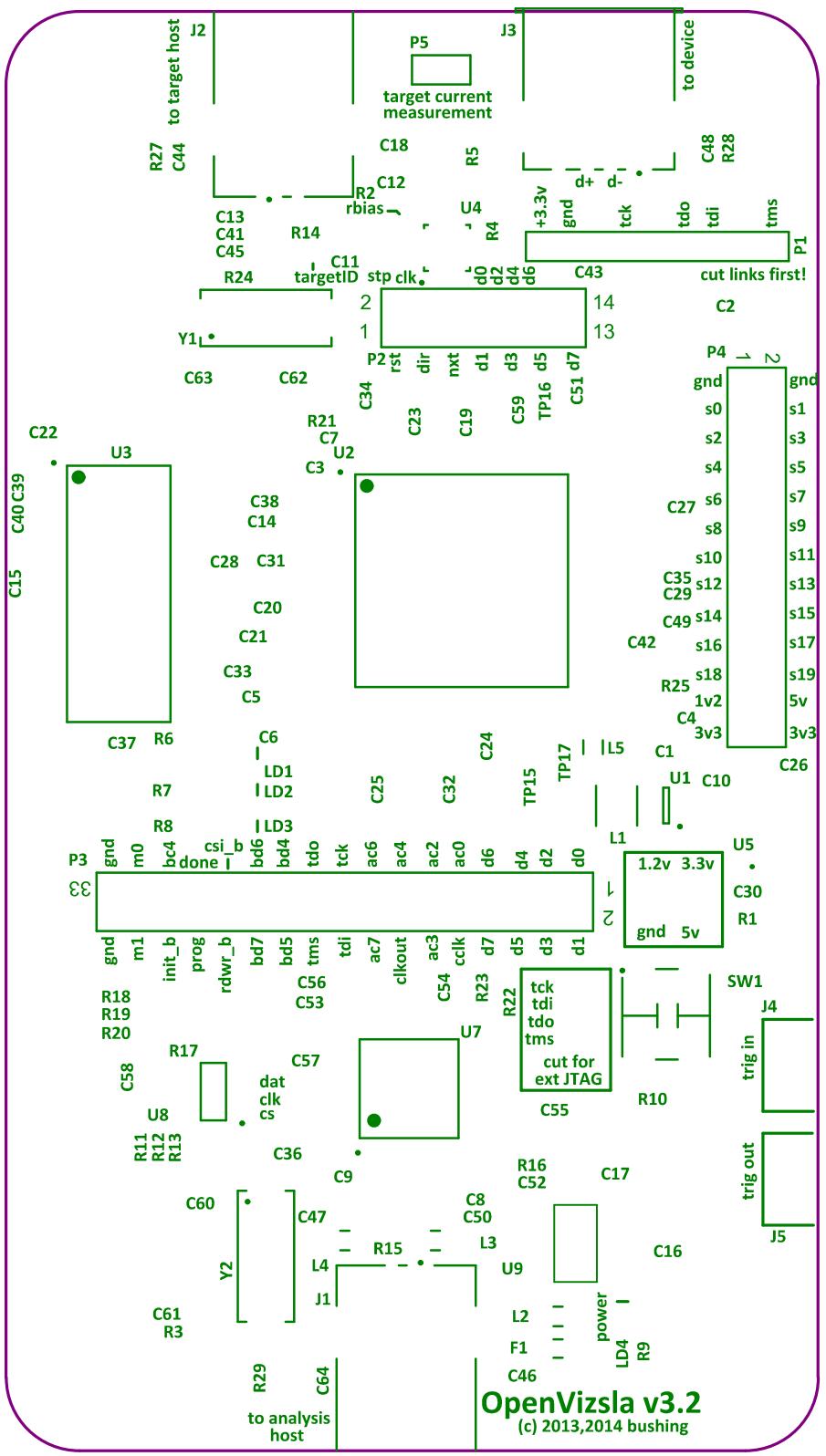












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cut links first!
measure current
forget current
- trace cut



R26 -

cut trace for
measure current
forget current
- trace cut



