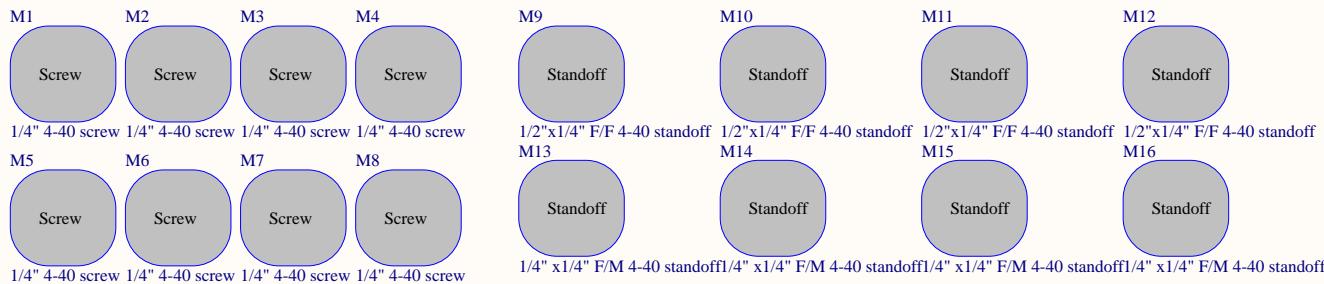


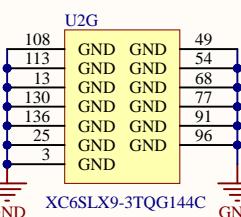
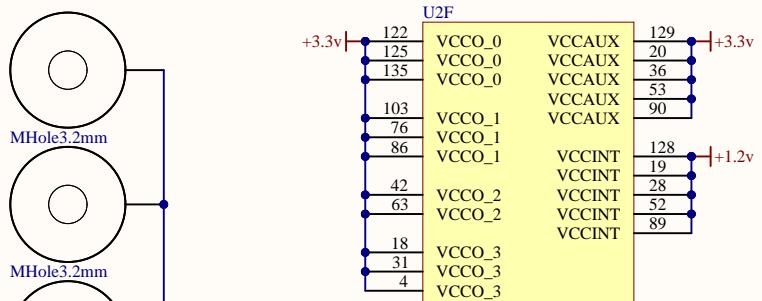
Copyrights: CC-BY-SA 3.0 Patents: Apache 2.0

Title		
Size	Number	Revision
A		
Date:	3/15/2021	Sheet of
File:	C:\Users\...\power.SchDoc	Drawn By:

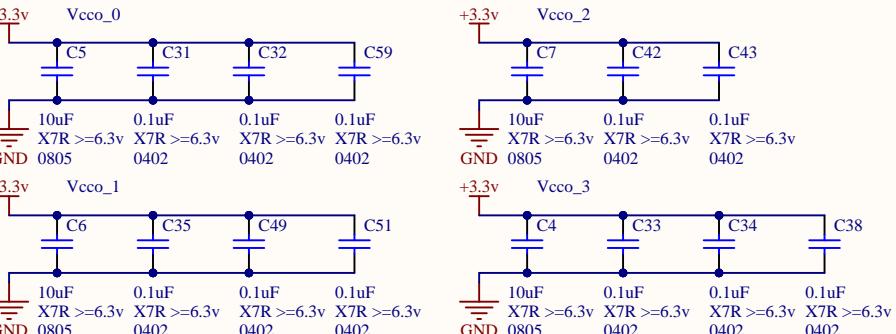
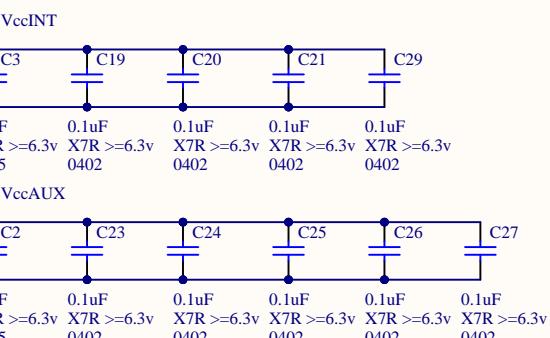
A



B



C



Copyrights: CC-BY-SA 3.0 Patents: Apache 2.0

Title

Size

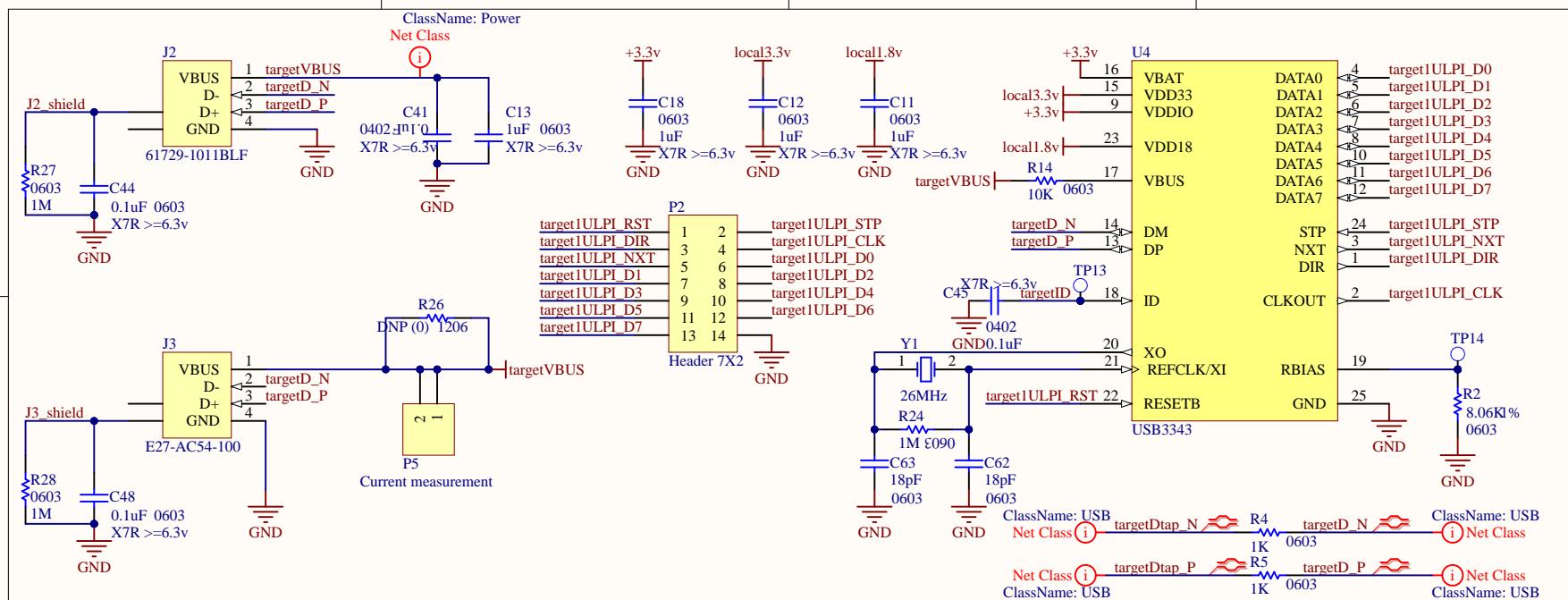
A

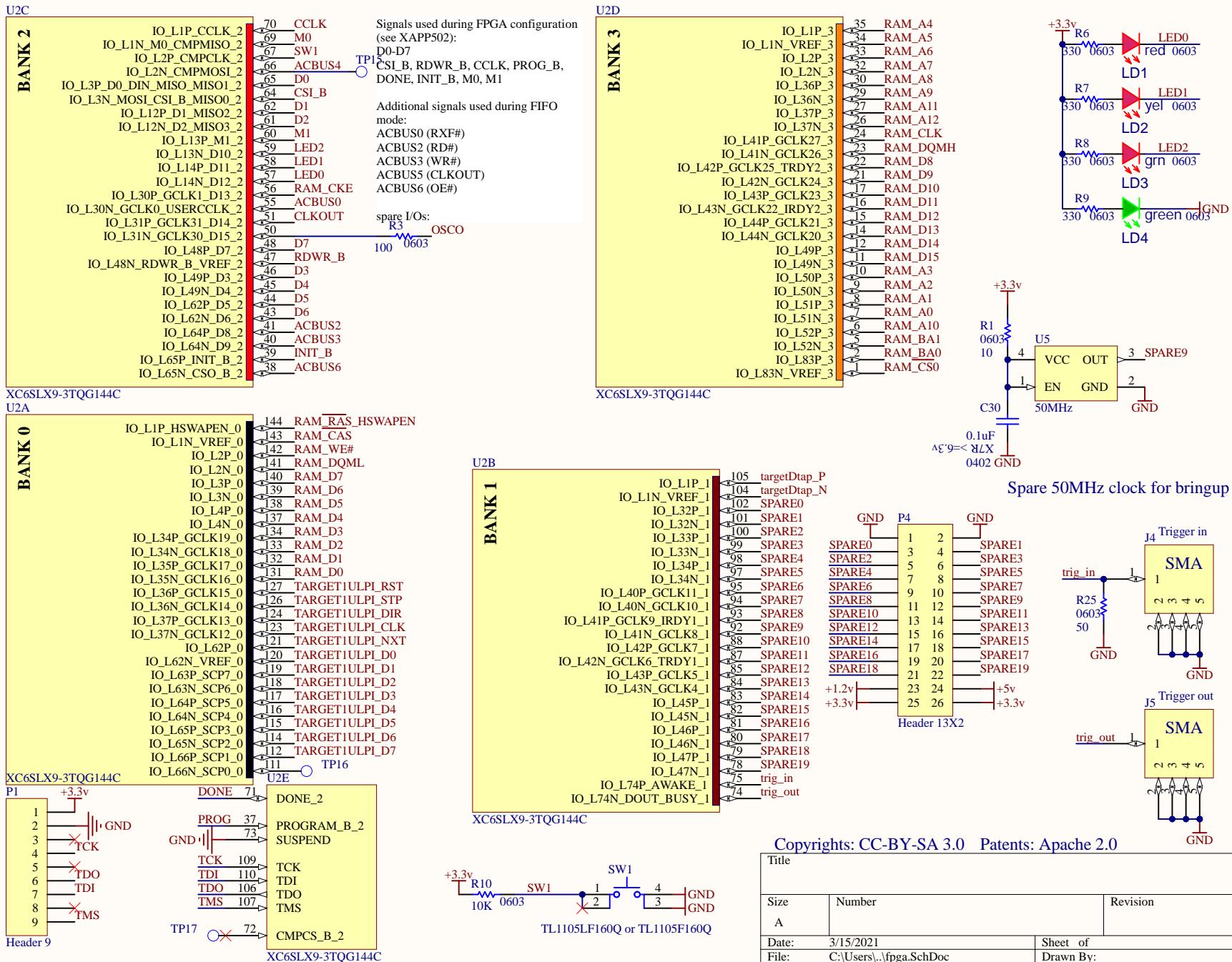
Number

Revision

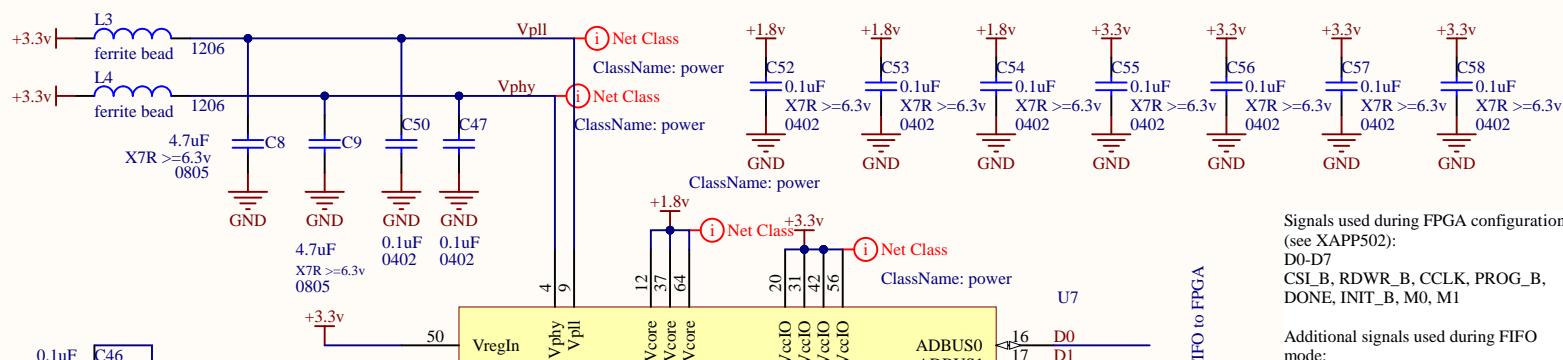
Date: 3/15/2021 Sheet 2 of

File: C:\Users\...\FPGA power v3.SchDoc Drawn By:





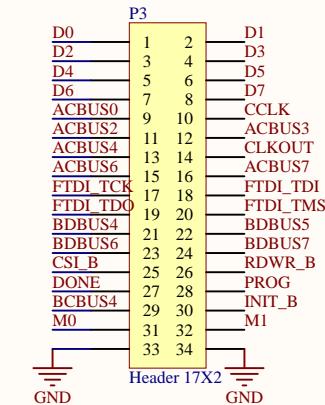
A



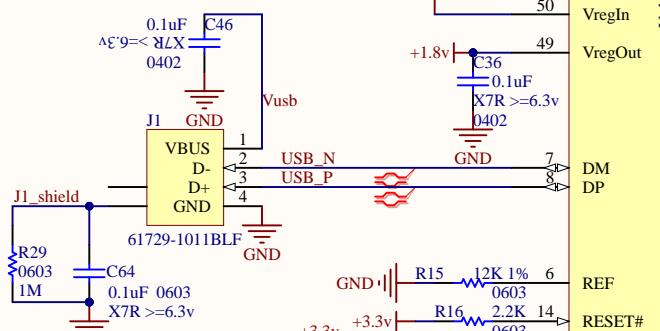
Signals used during FPGA configuration
(see XAPP502):
D0-D7
CSI_B, RDWR_B, CCLK, PROG_B,
DONE, INIT_B, M0, M1

Additional signals used during FIFO mode:
ACBUS0 (RXF#)
ACBUS2 (RD#)
ACBUS3 (WR#)
ACBUSS (CLKOUT)
ACBUS6 (OE#)

spare I/Os:

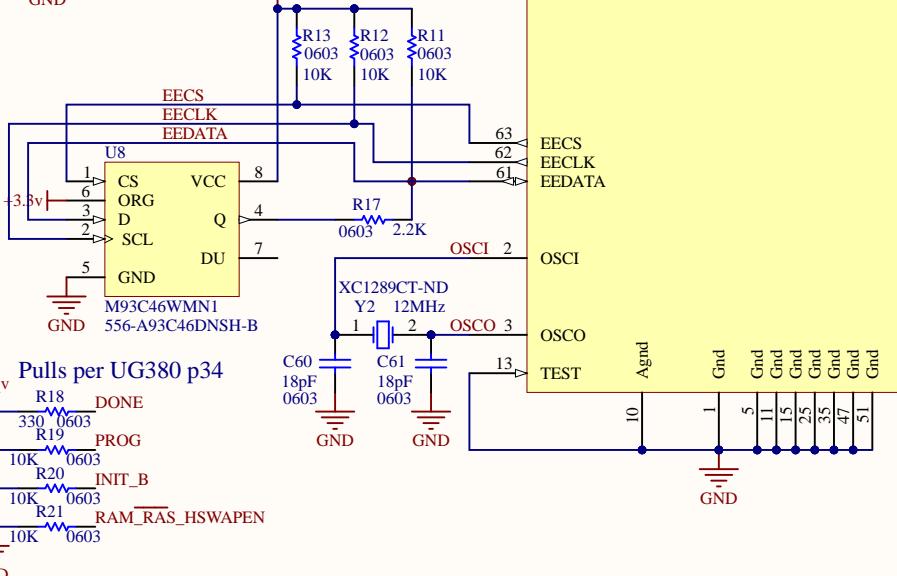


B



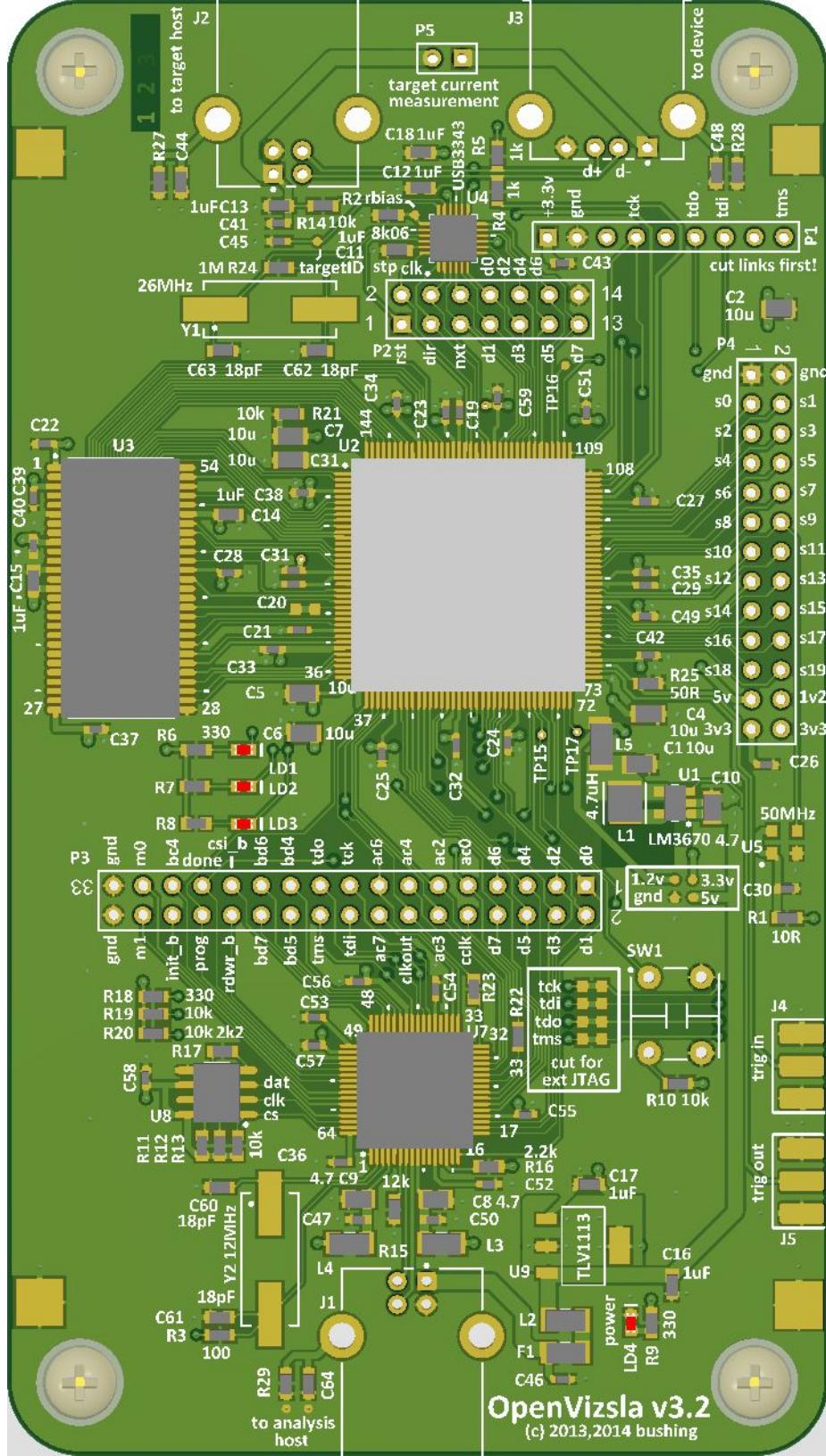
FT2232H

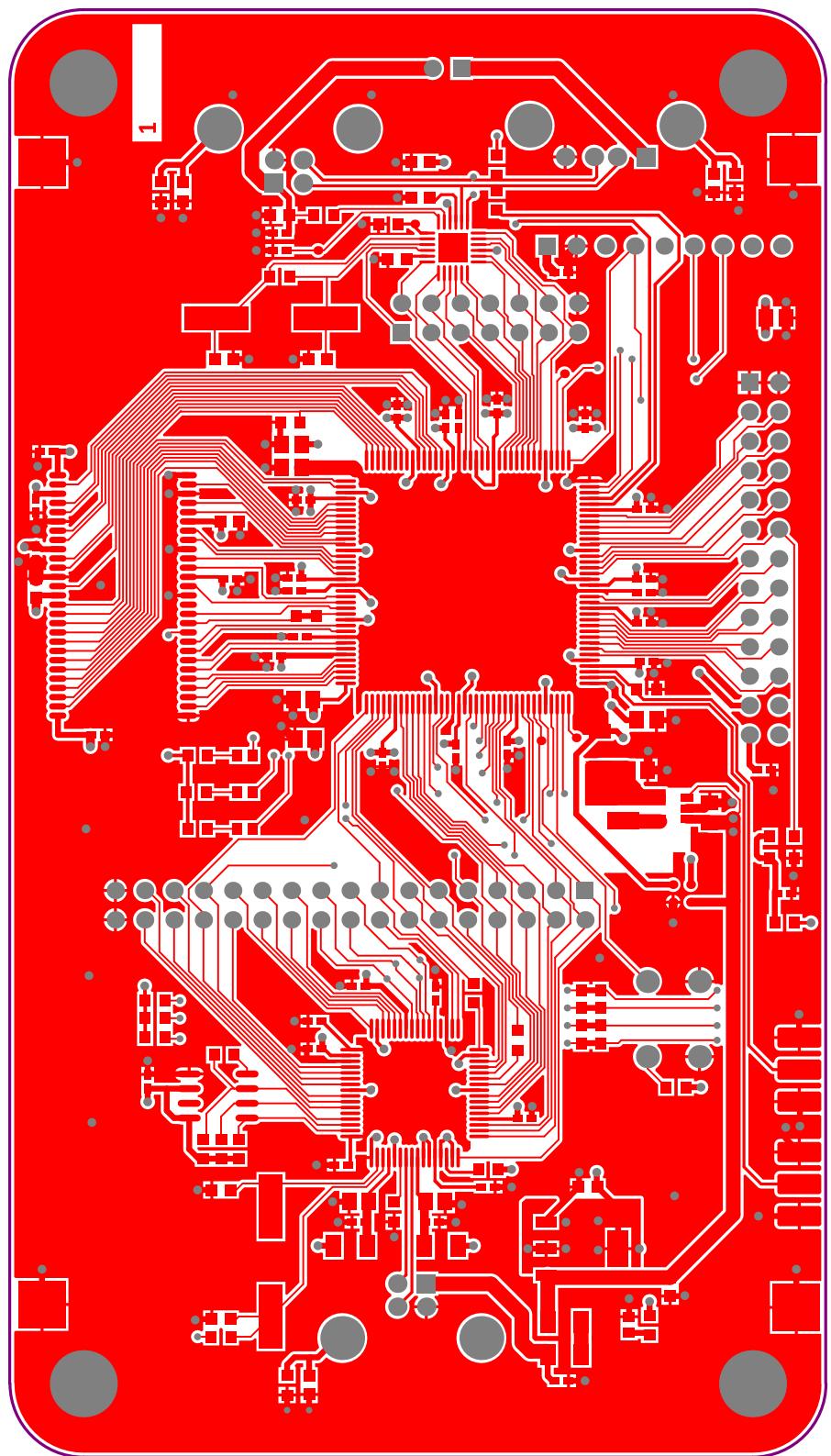
C

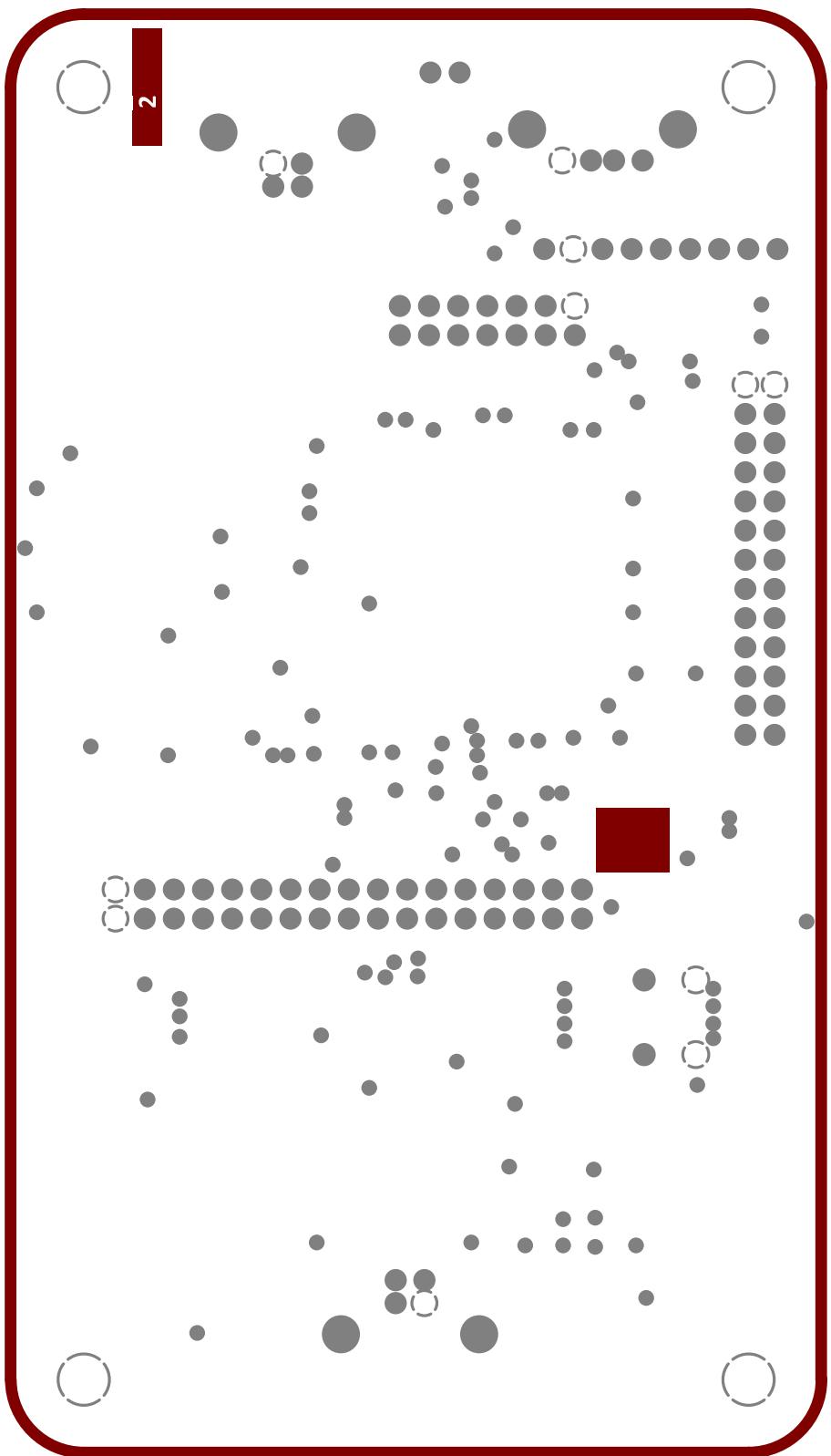


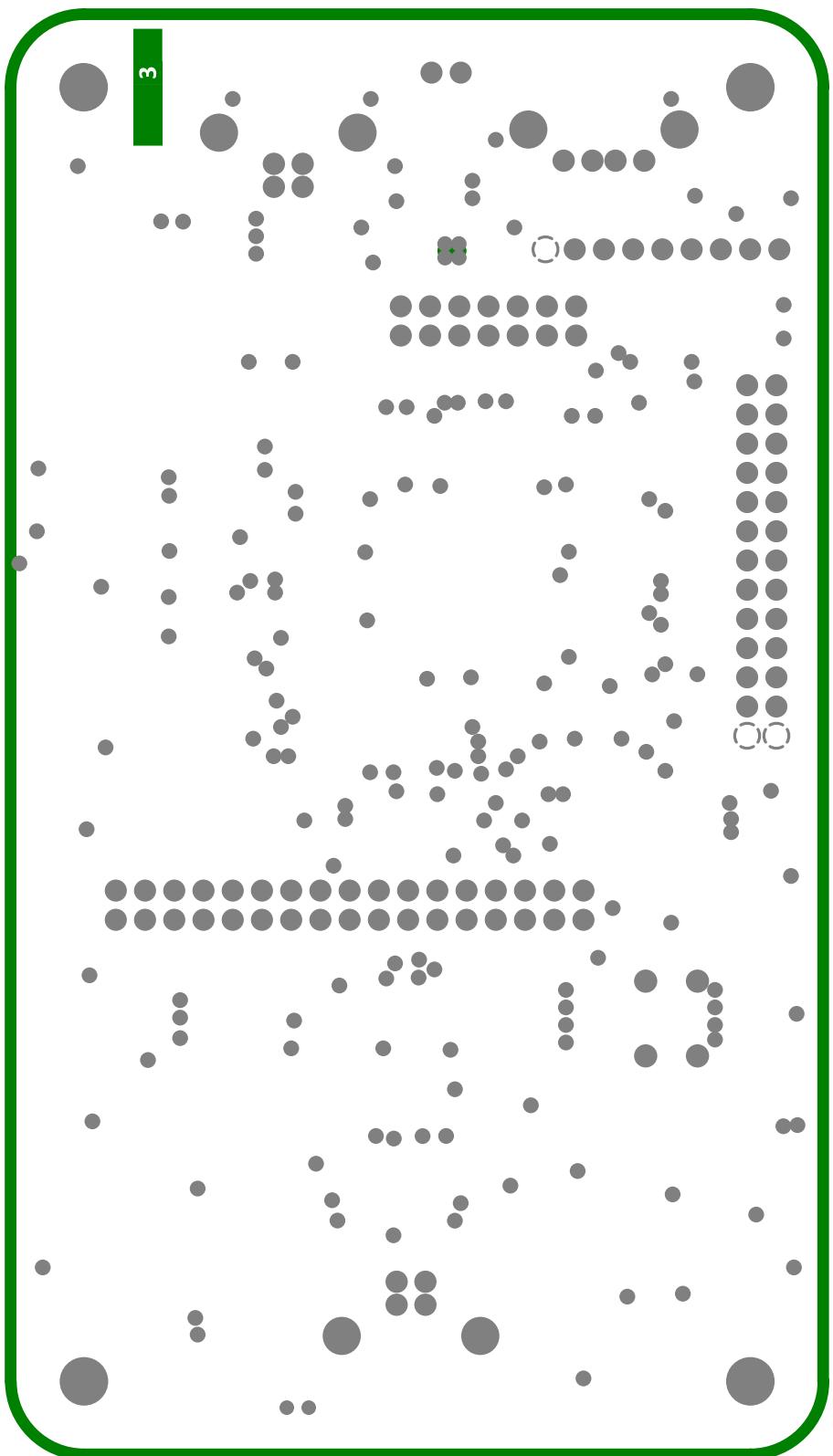
Copyrights: CC-BY-SA 3.0 Patents: Apache 2.0

Title		Revision
Size	Number	
A		
Date:	3/15/2021	Sheet of
File:	C:\Users\...\usb.SchDoc	Drawn By:

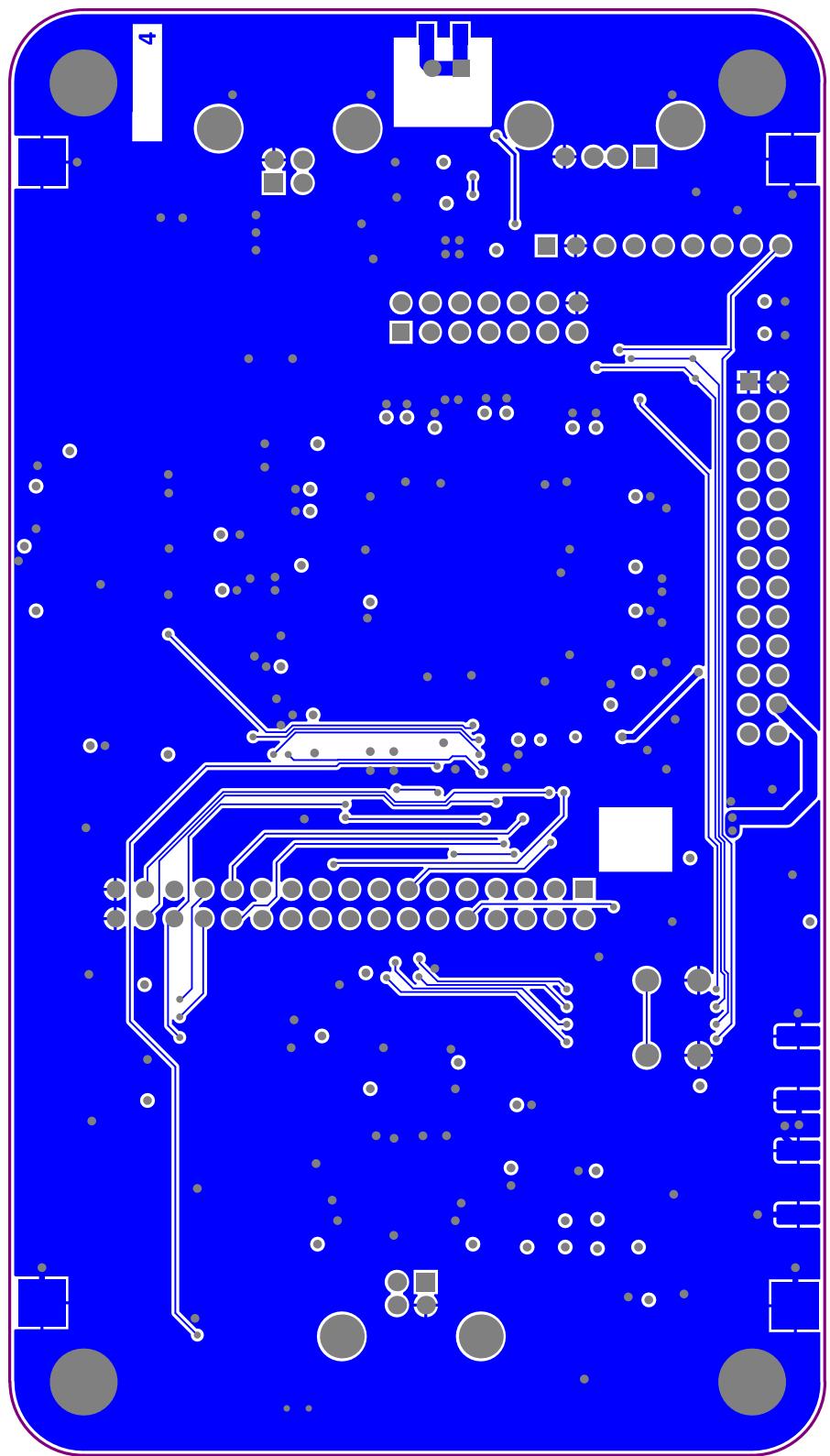


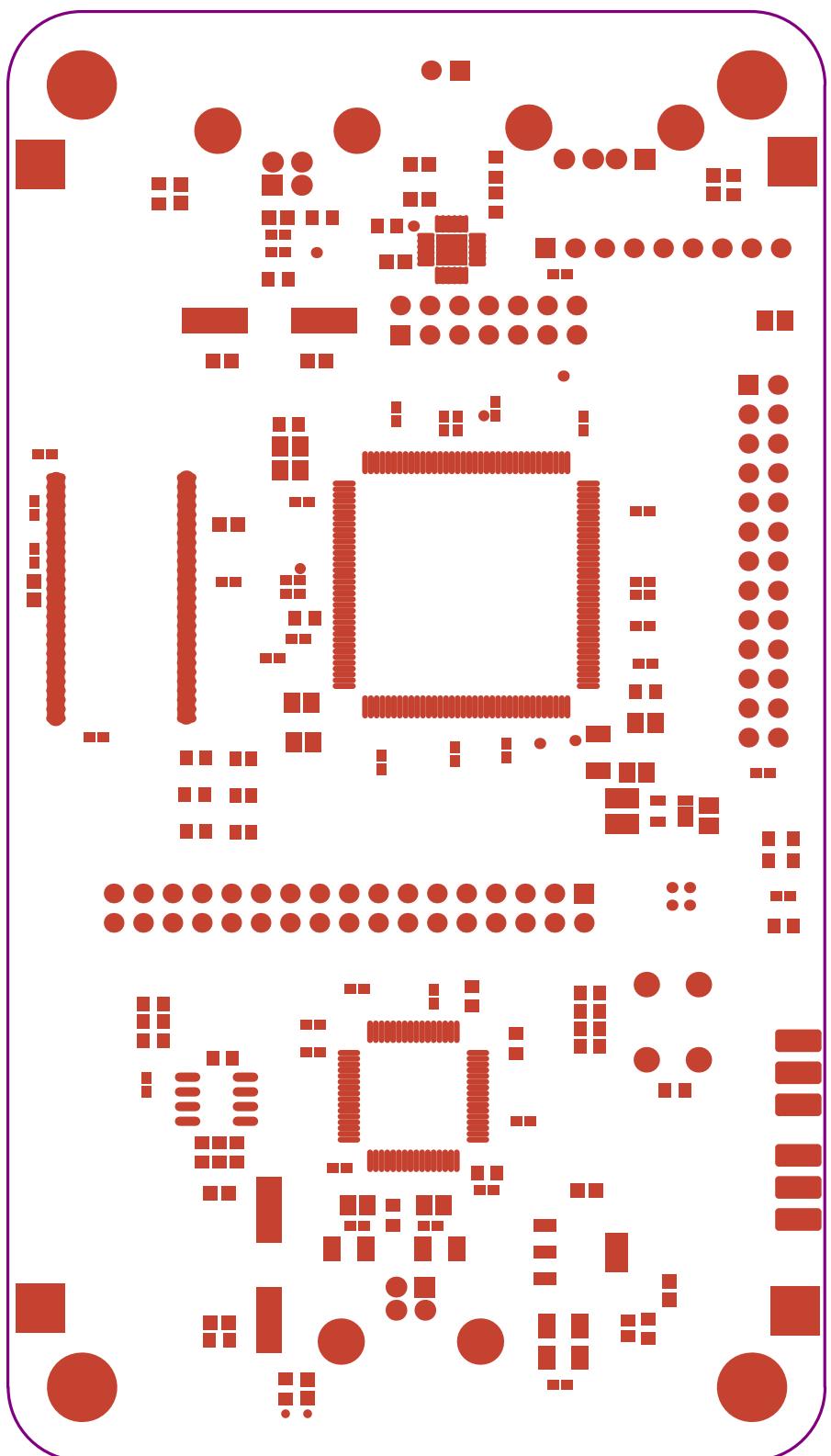


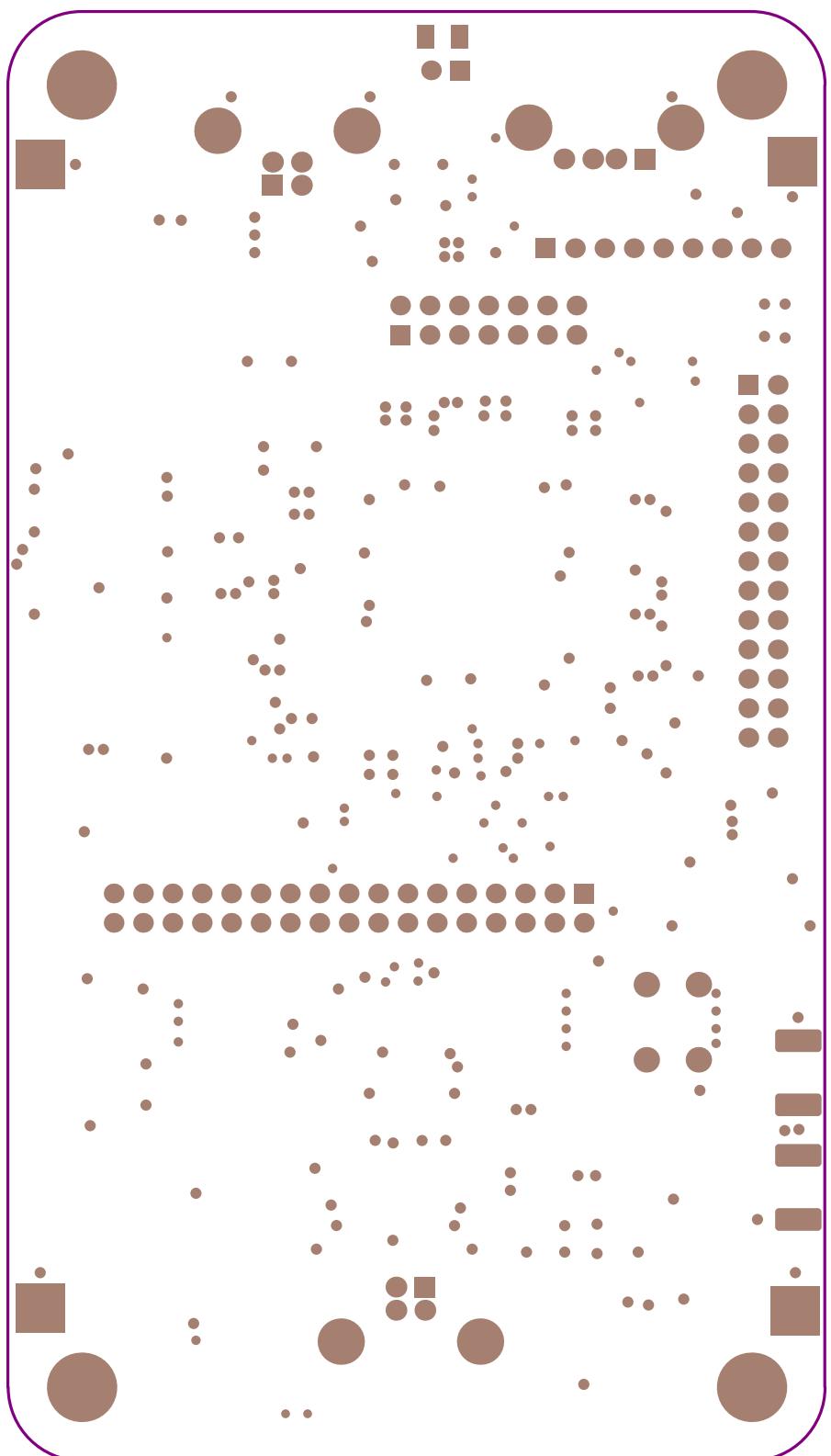


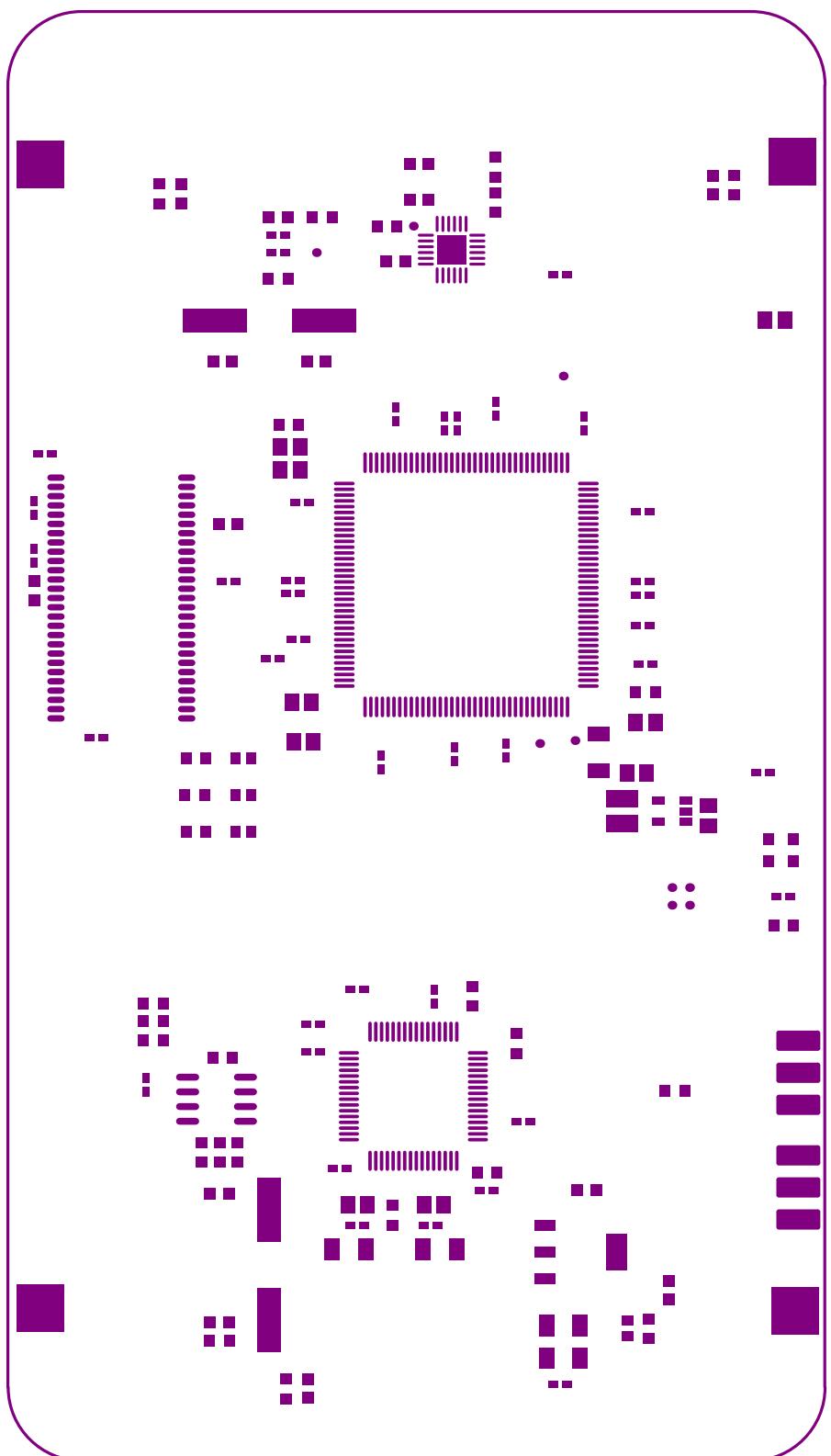


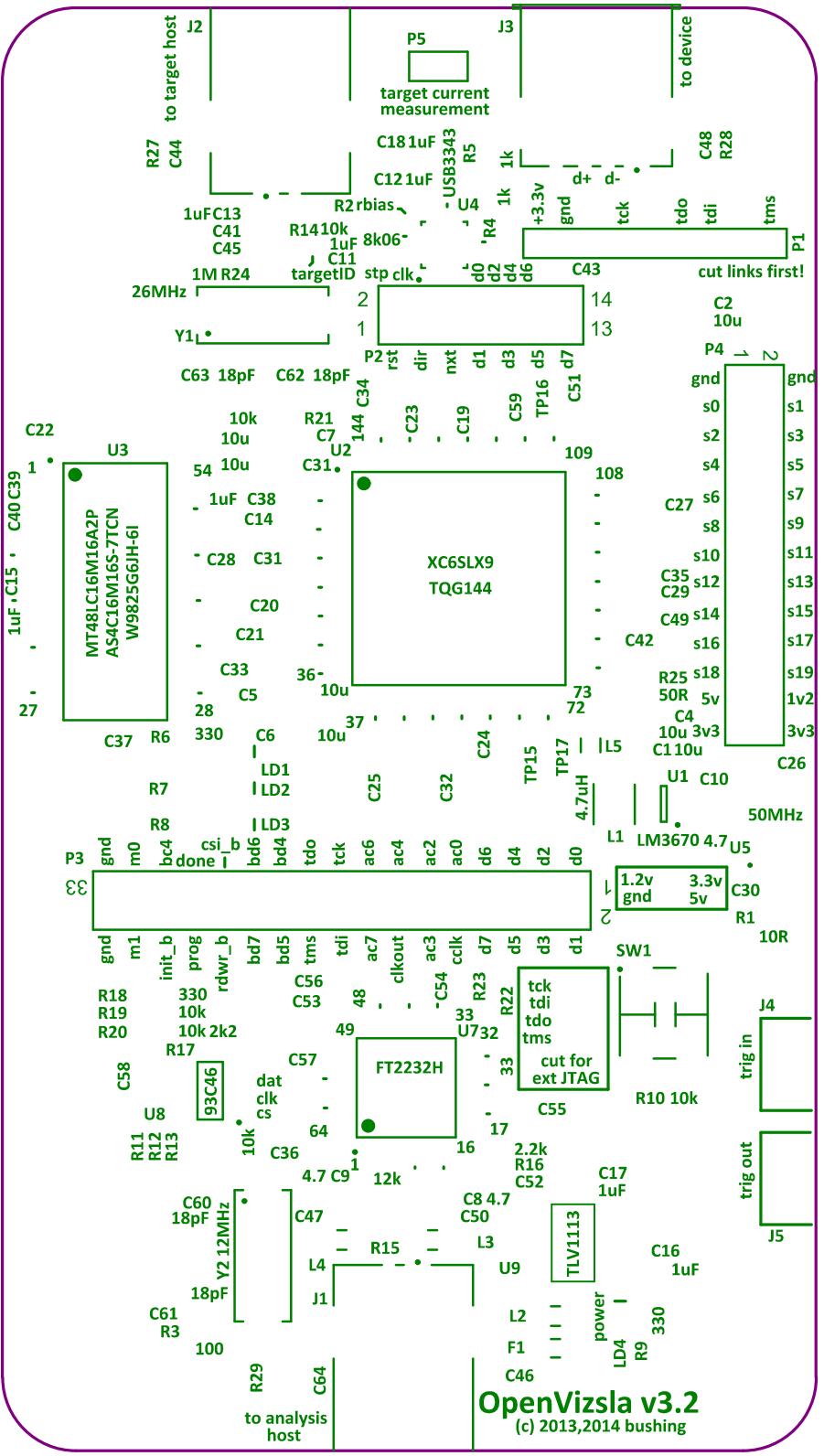
3











OpenVizsla v3.2
(c) 2013,2014 bushing

dsv
brg

D-
D+

clout
gC1

436

九

9

10
תְּהִלָּה

class_p
queue
bitop
PcA
0m
bng
bng

100

cut 1
tuna

