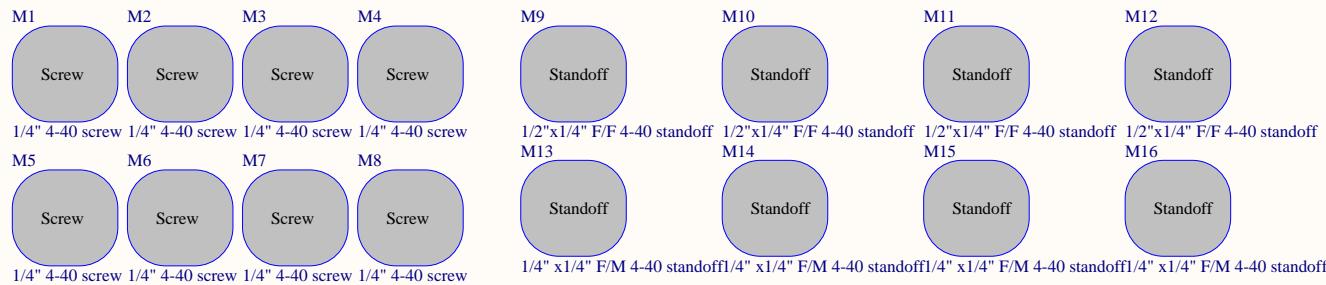


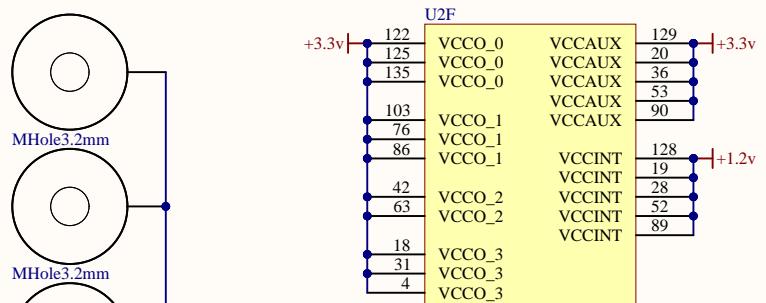
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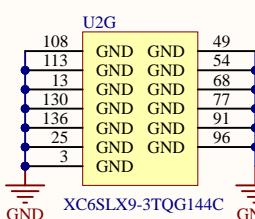
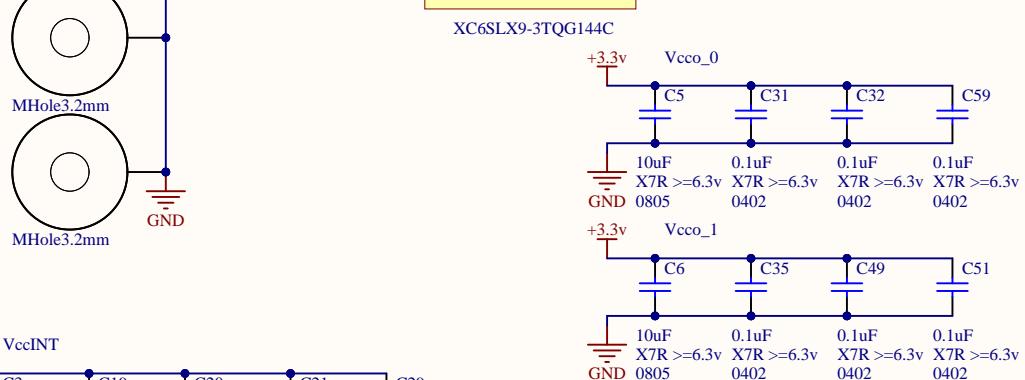
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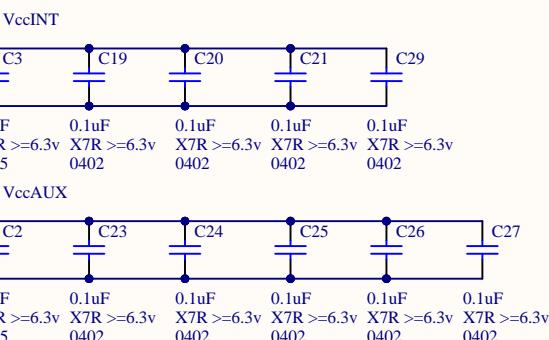
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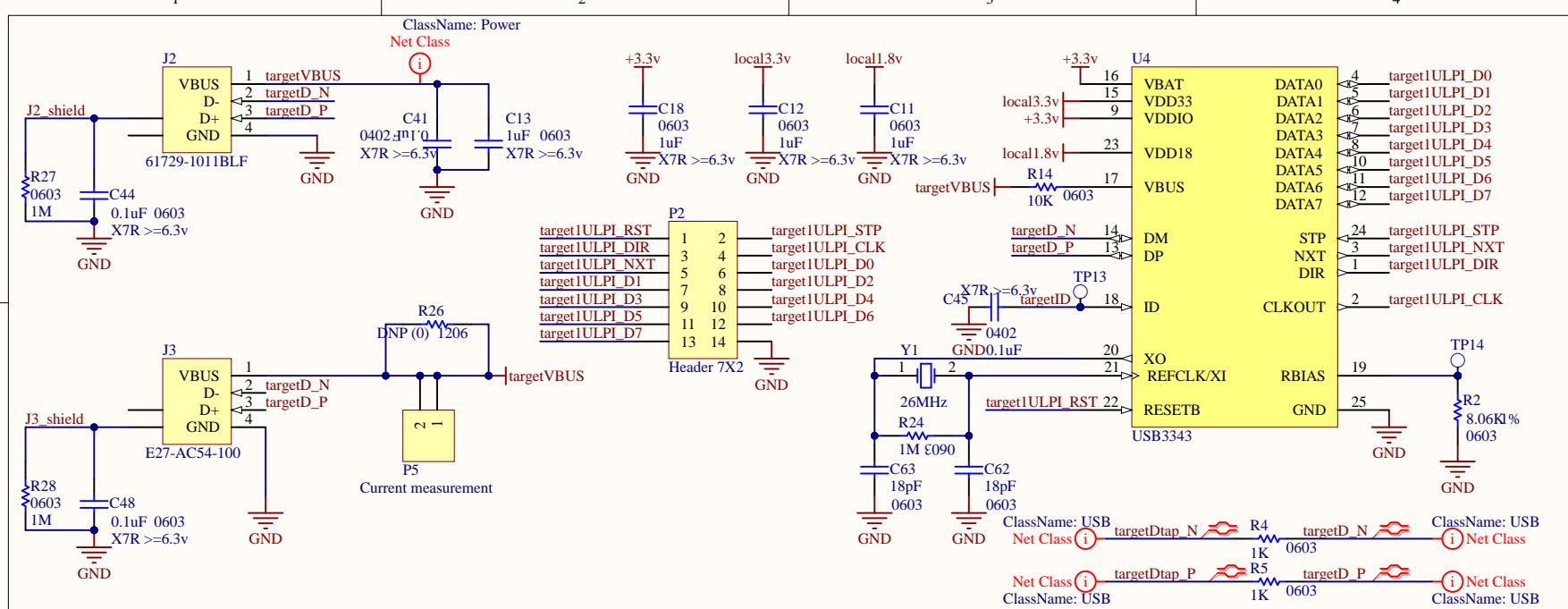


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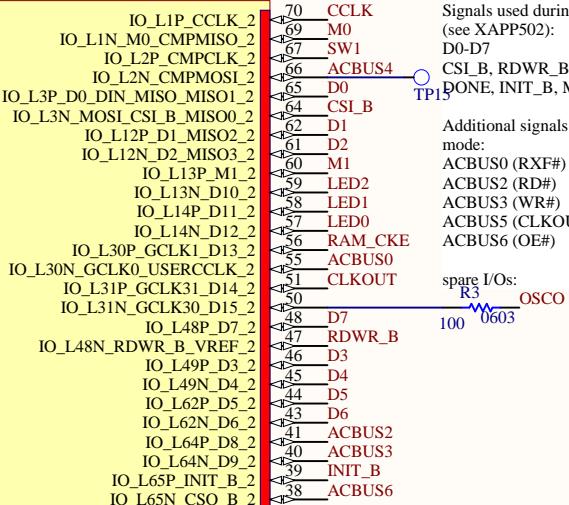


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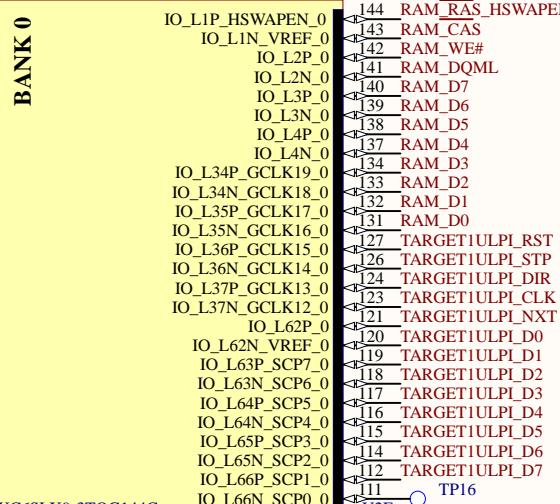


U2C

**BANK 2**

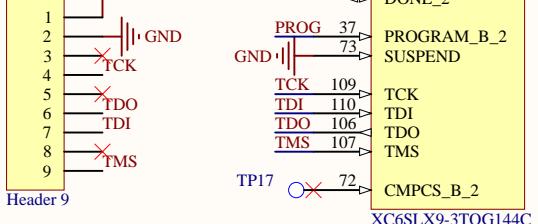
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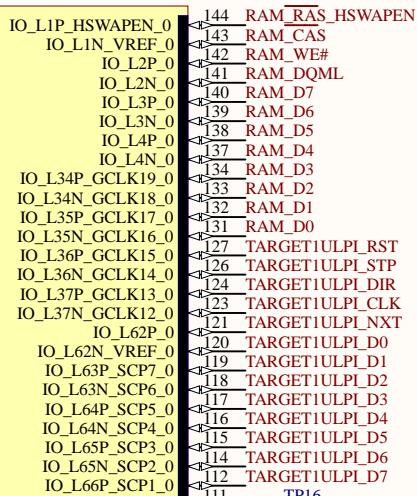
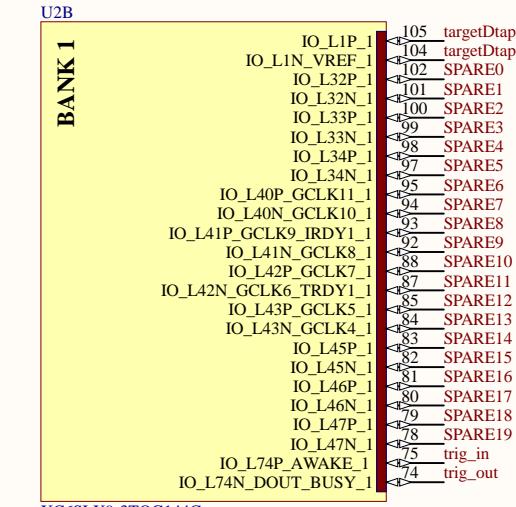


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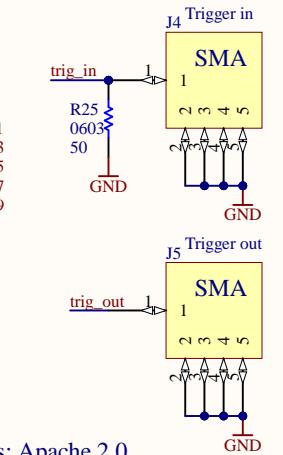
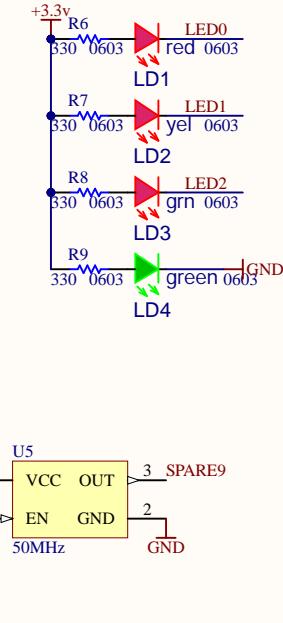
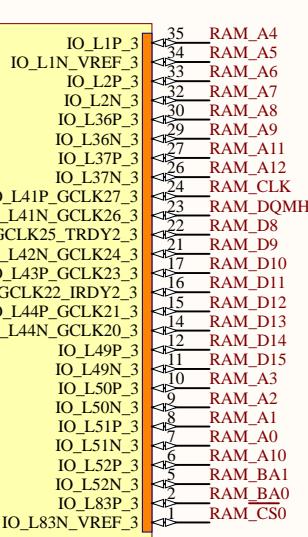
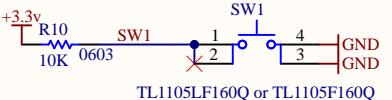
P1



U2D

**BANK 0****BANK 1**

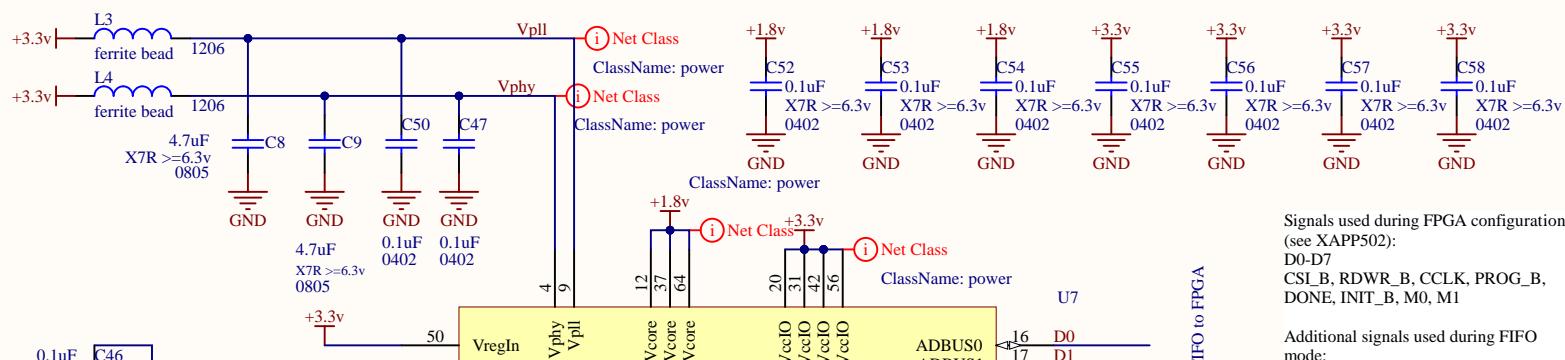
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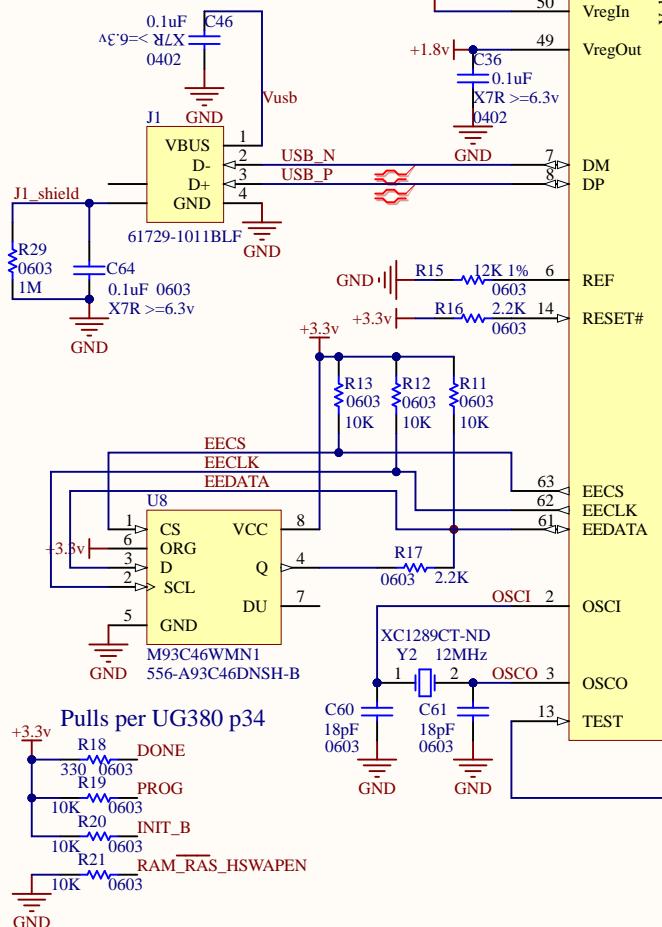
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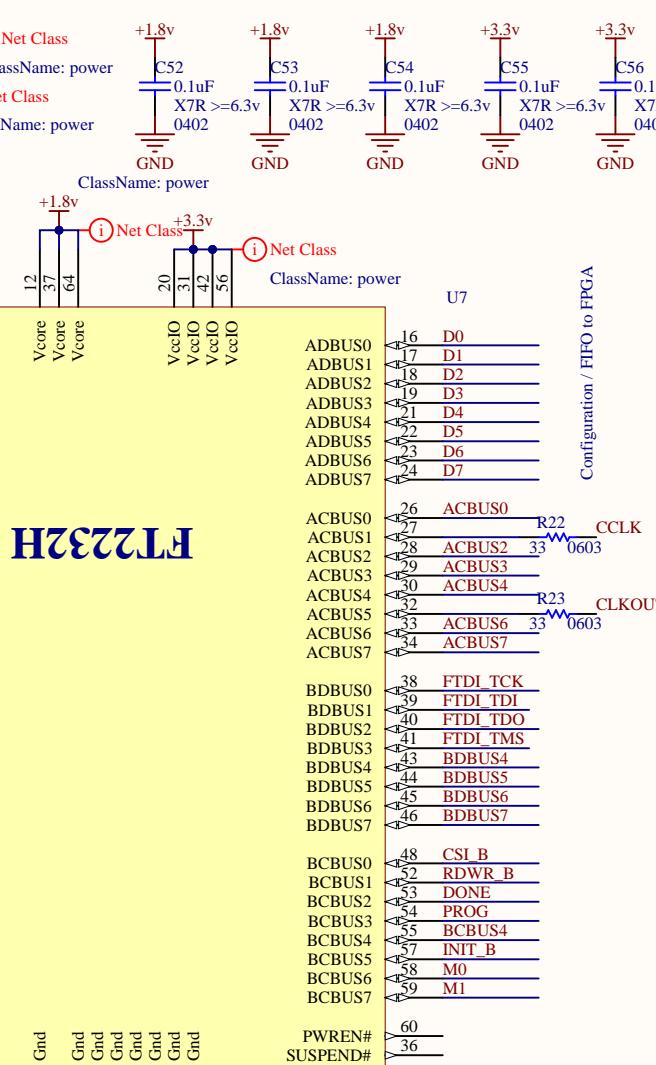


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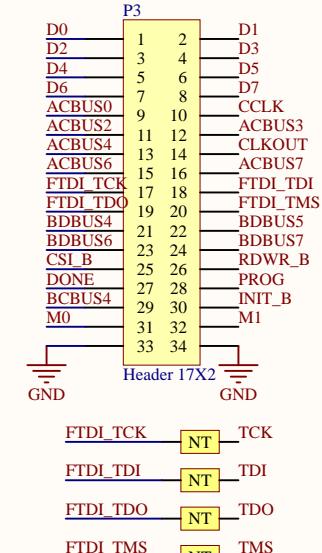
FT2232H



Signals used during FPGA configuration (see XAPP502):  
D0-D7  
CSI\_B, RDWR\_B, CCLK, PROG\_B, DONE, INIT\_B, M0, M1

Additional signals used during FIFO mode:  
ACBUS0 (RXF#)  
ACBUS2 (RD#)  
ACBUS3 (WR#)  
ACBUSS (CLKOUT)  
ACBUS6 (OE#)

spare I/Os:



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