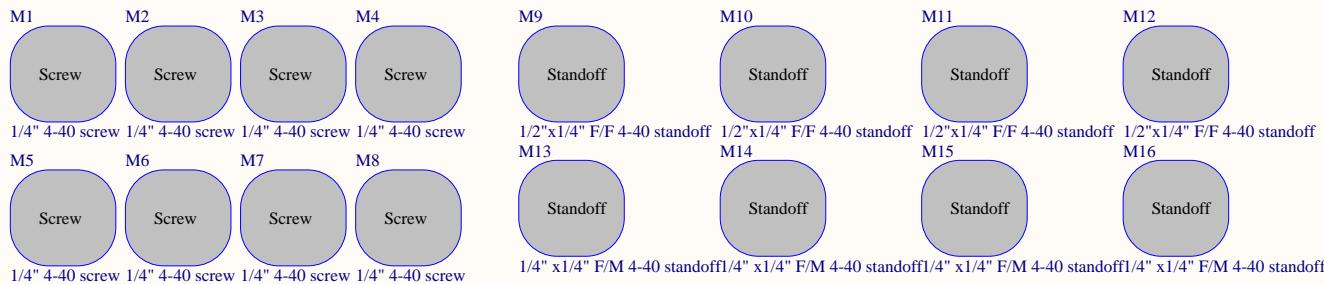


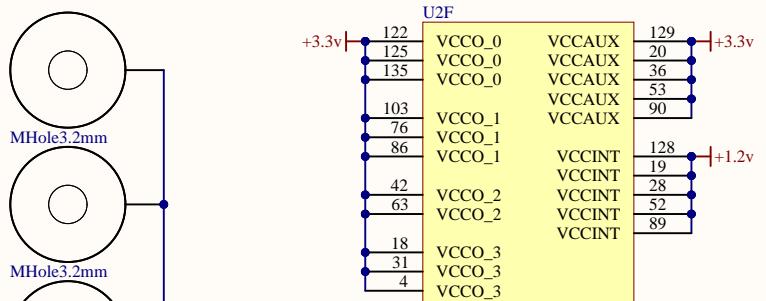
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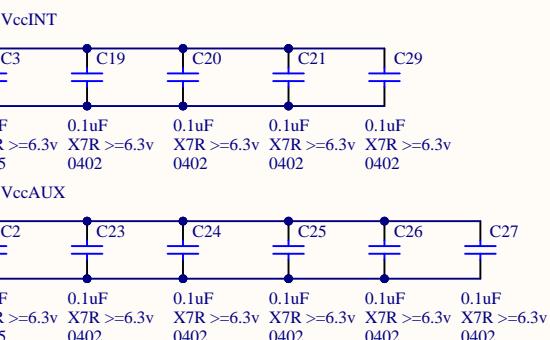
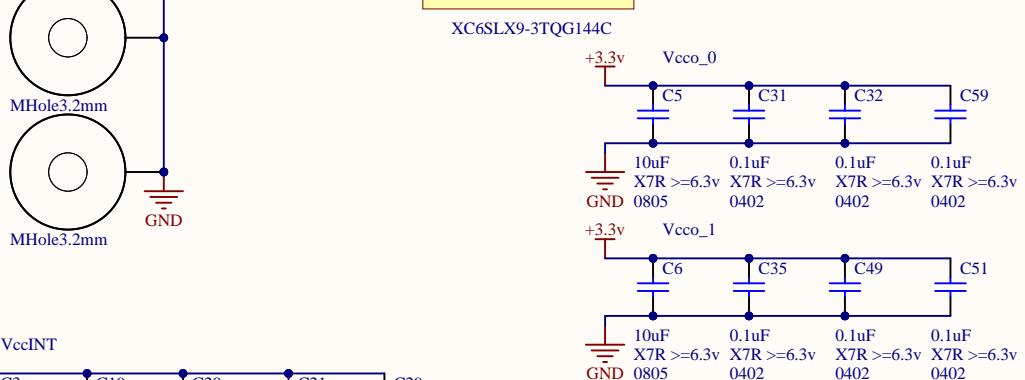
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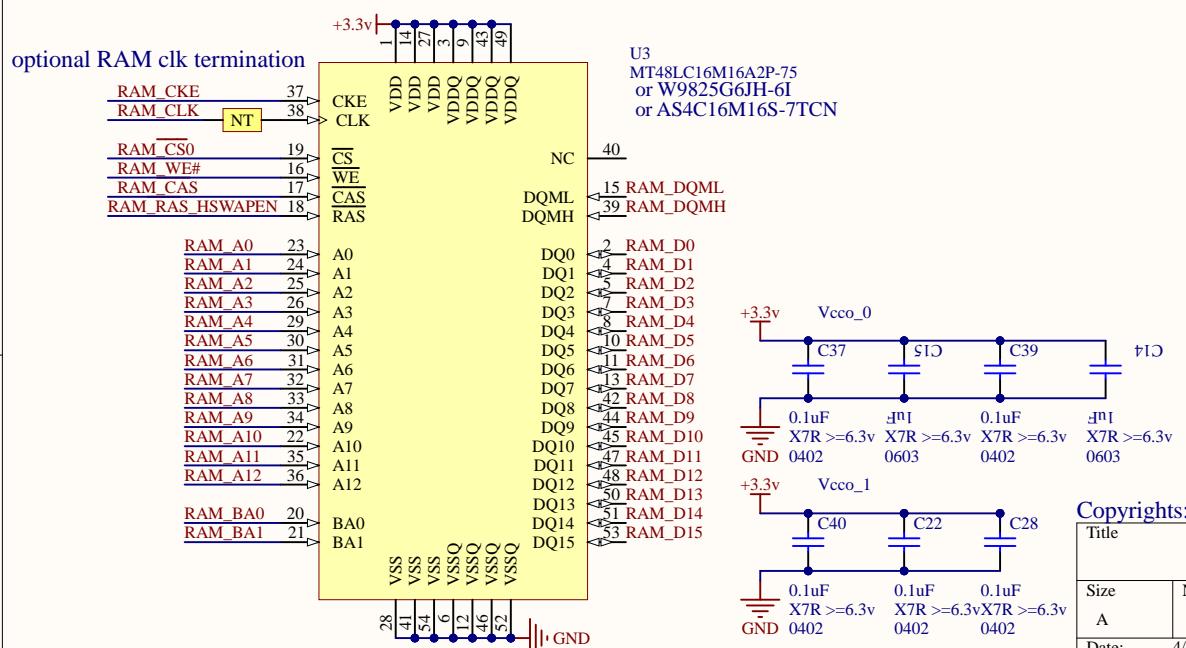
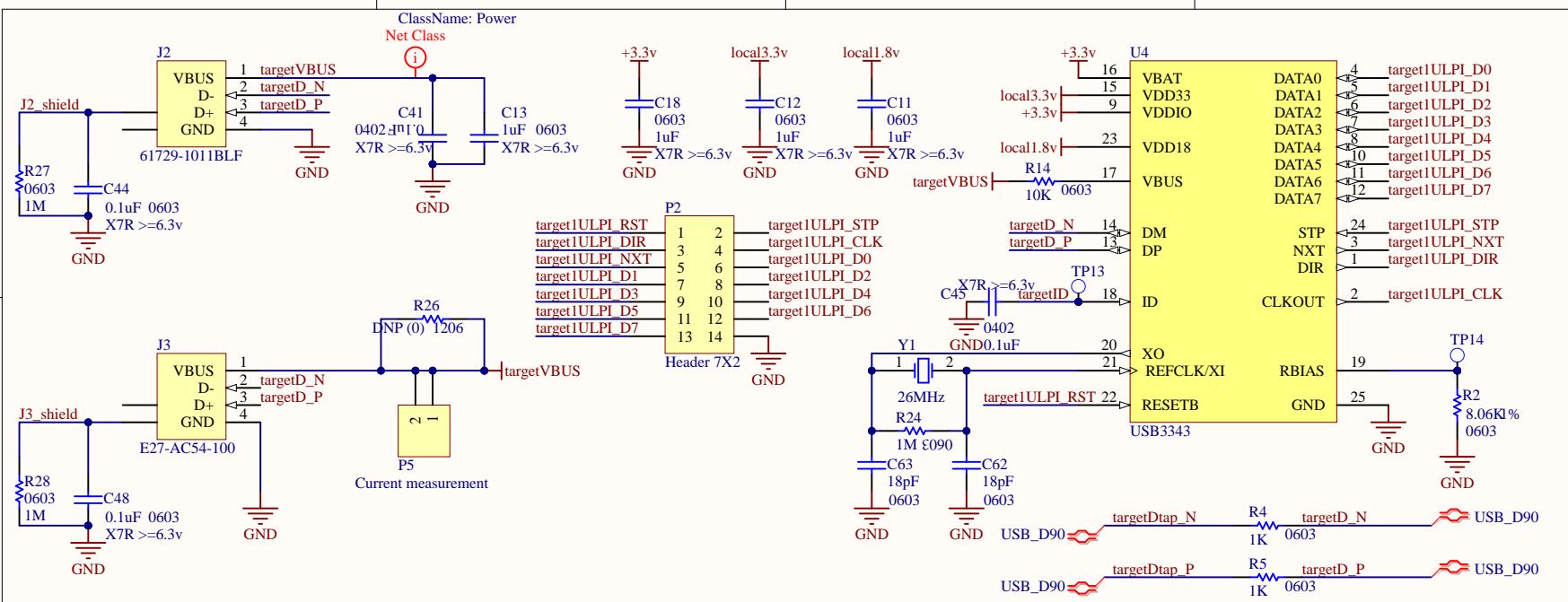


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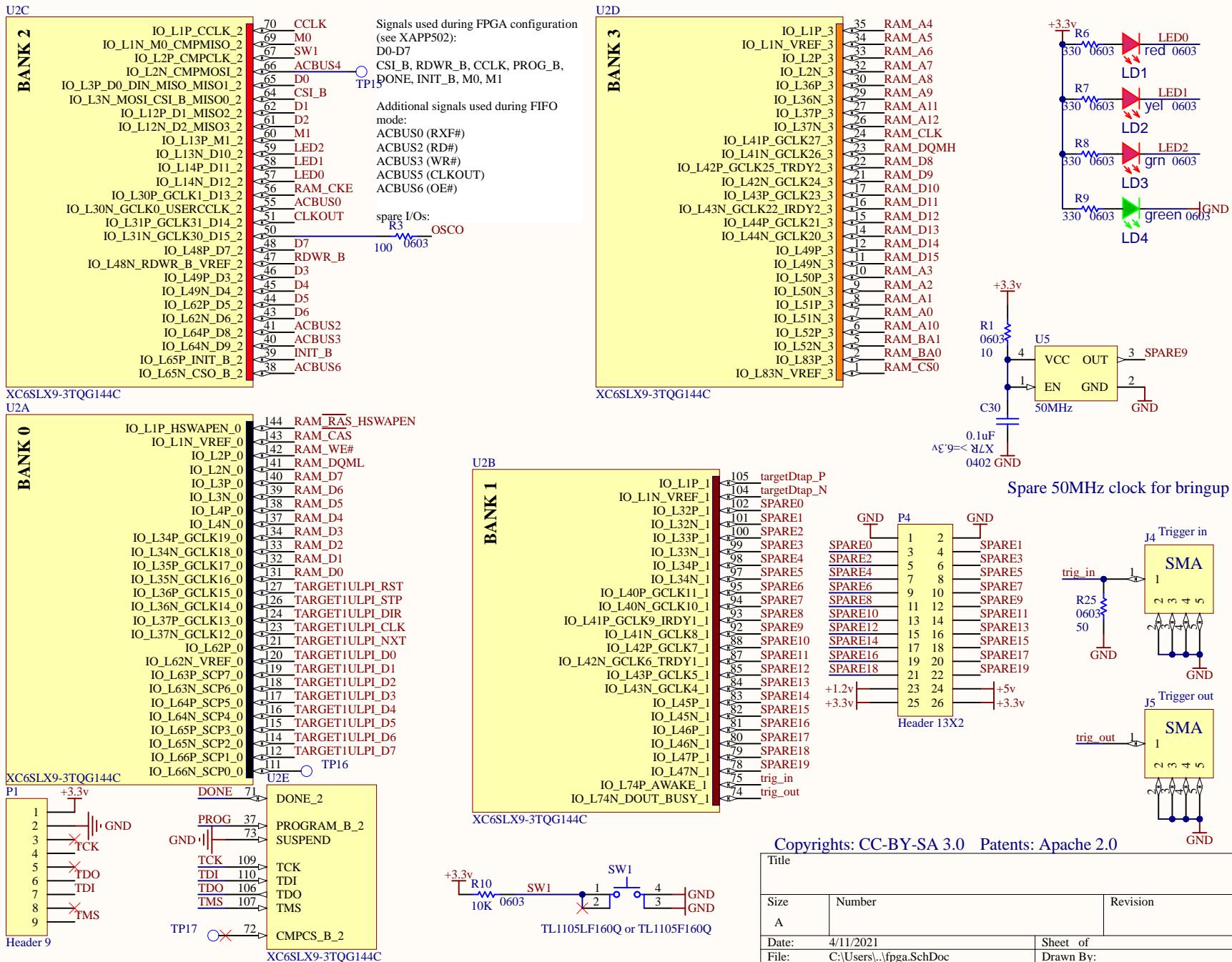


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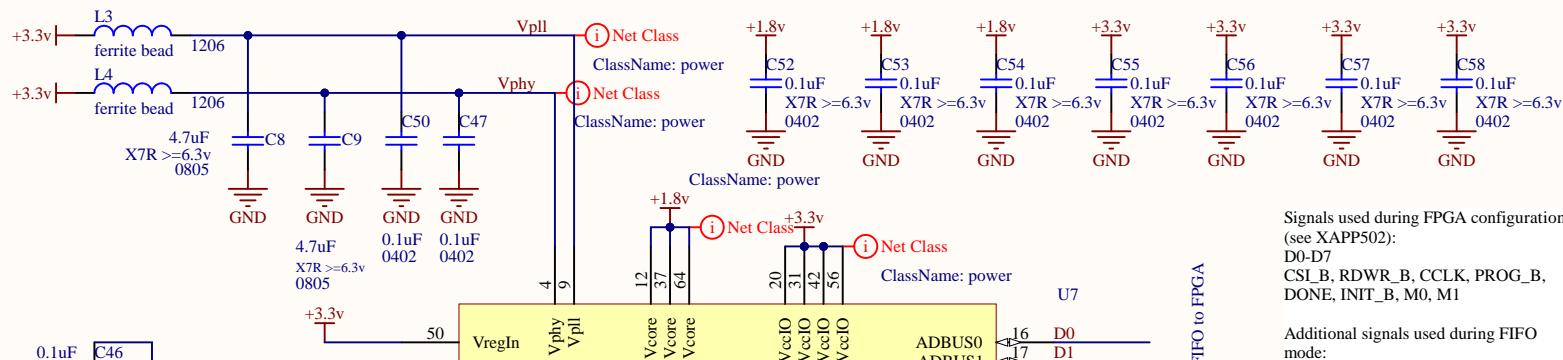
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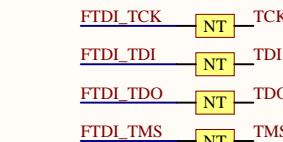
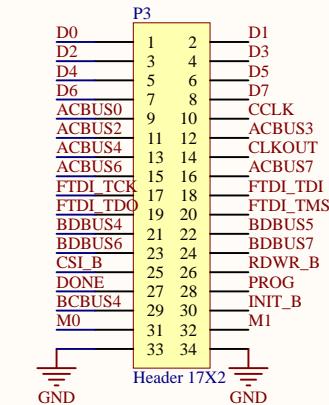
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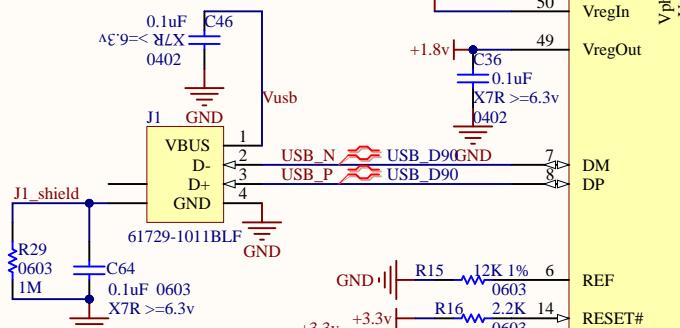
Signals used during FPGA configuration (see XAPP502):
D0-D7
CSI_B, RDWR_B, CCLK, PROG_B,
DONE, INIT_B, M0, M1

Additional signals used during FIFO mode:
ACBUS0 (RXF#)
ACBUS2 (RD#)
ACBUS3 (WR#)
ACBUSS (CLKOUT)
ACBUS6 (OE#)

spare I/Os:

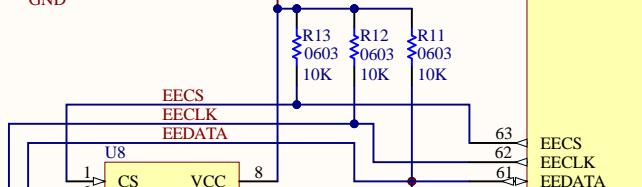


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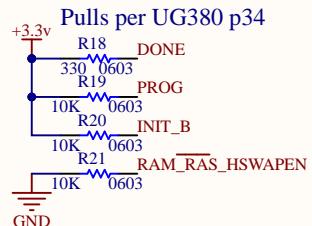


FT2232H

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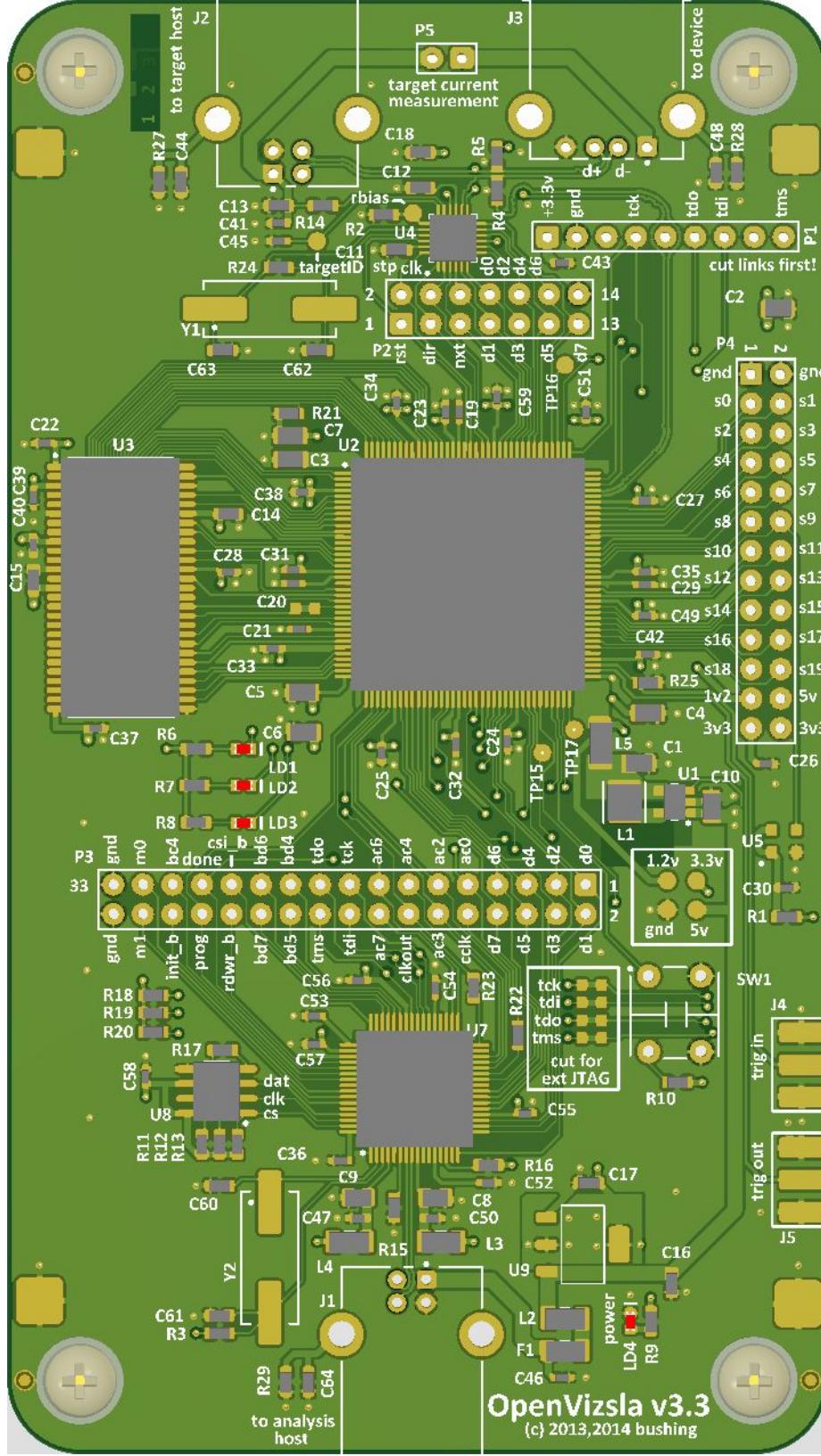


D

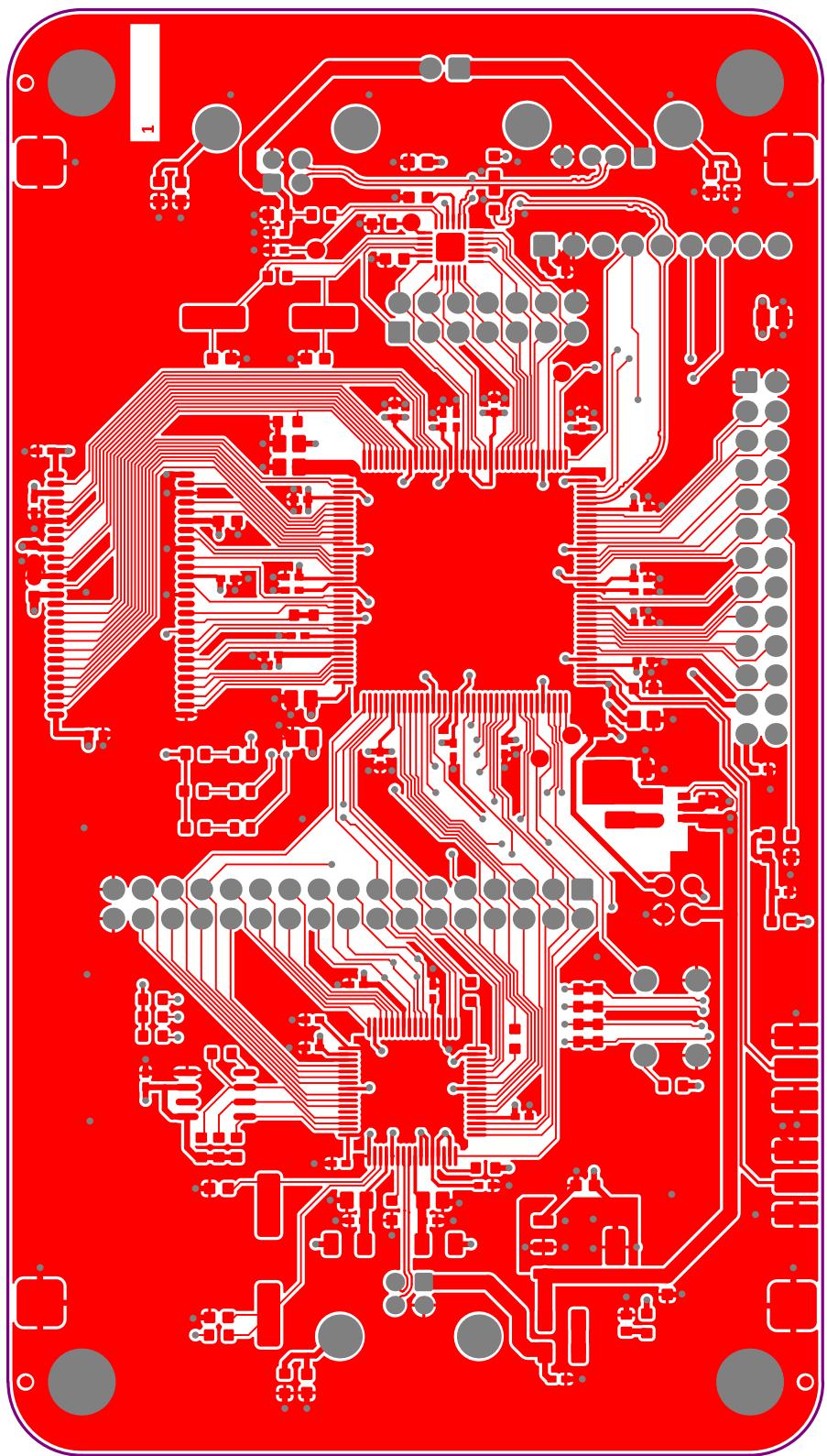


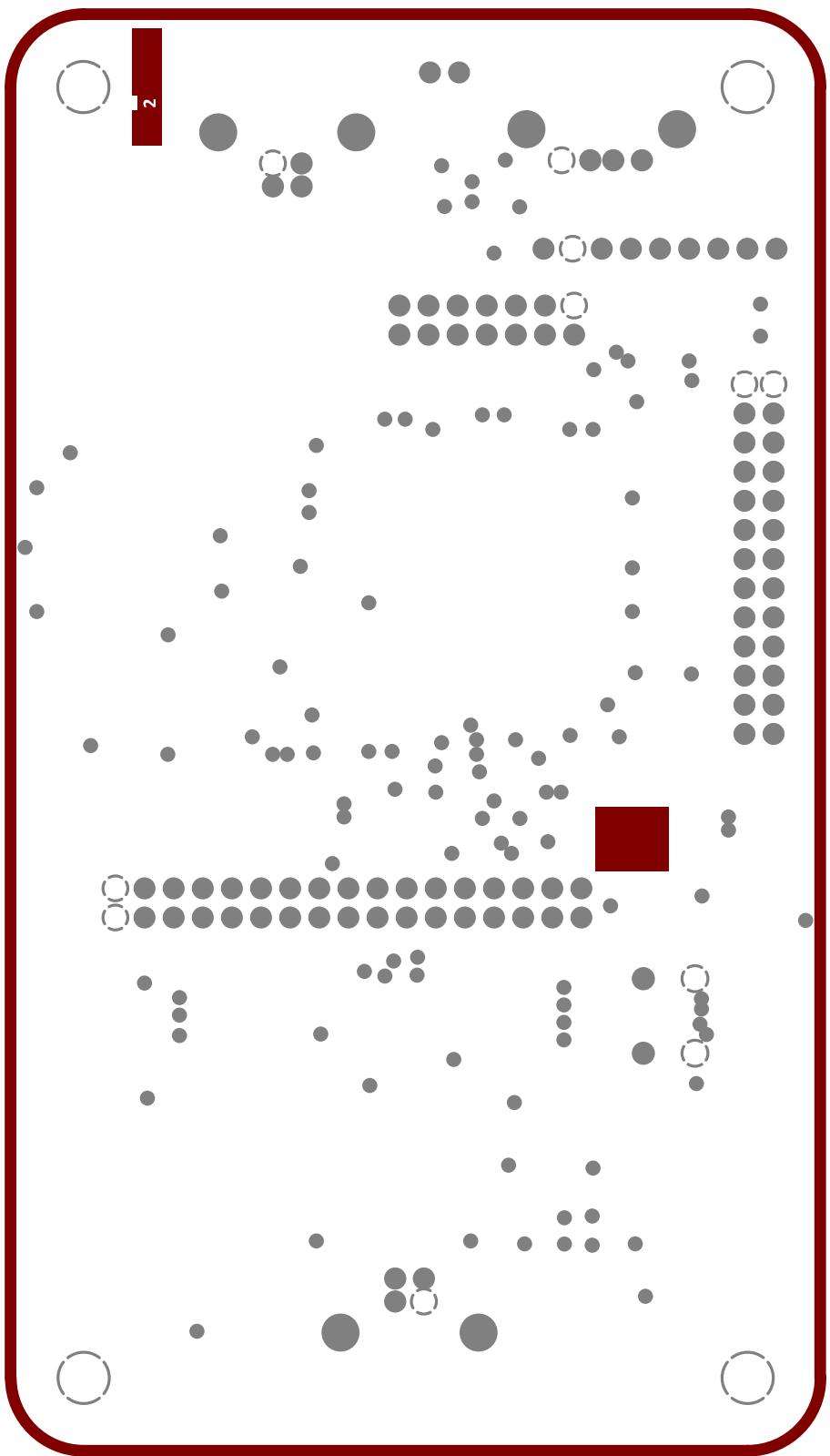
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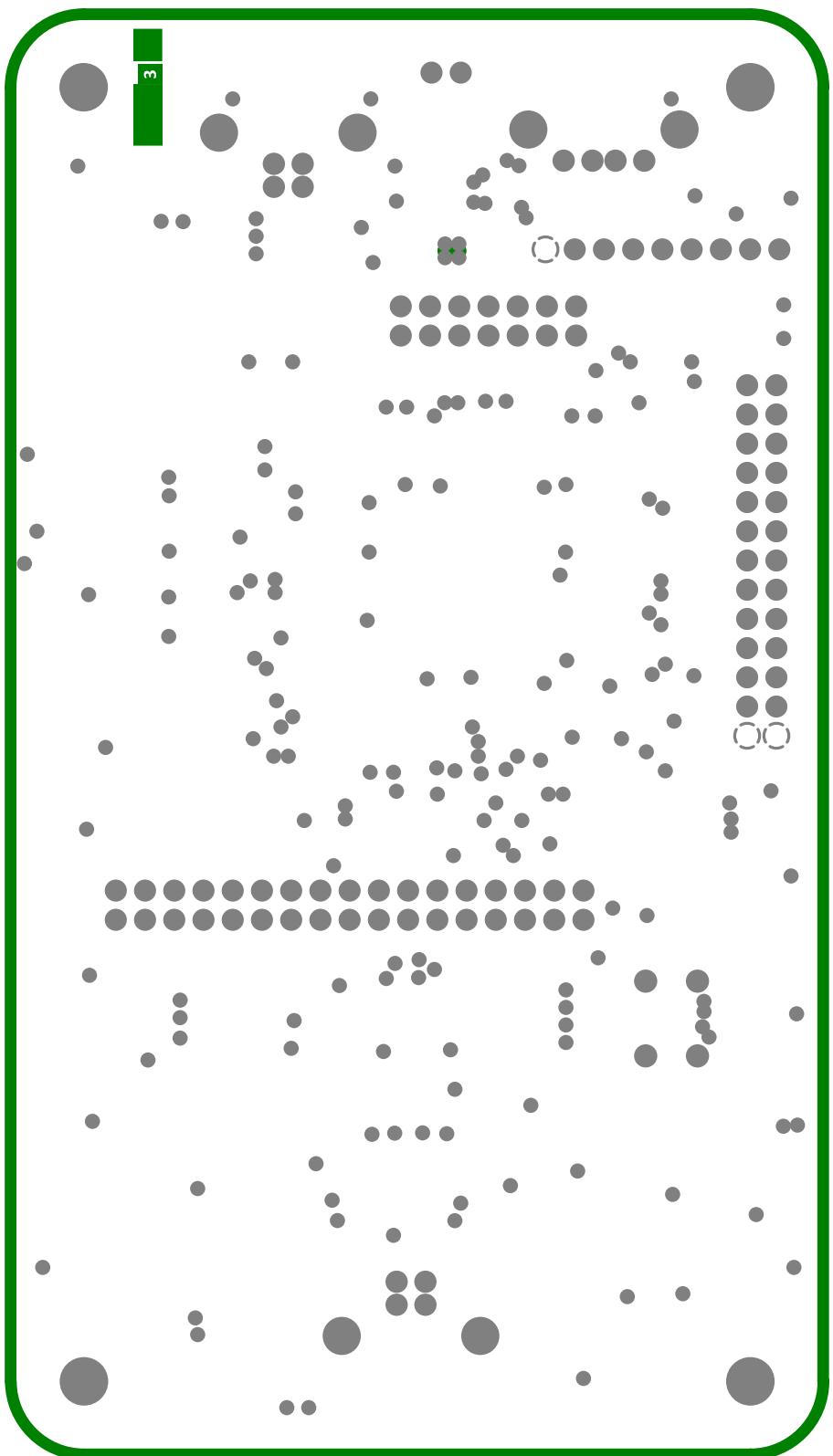
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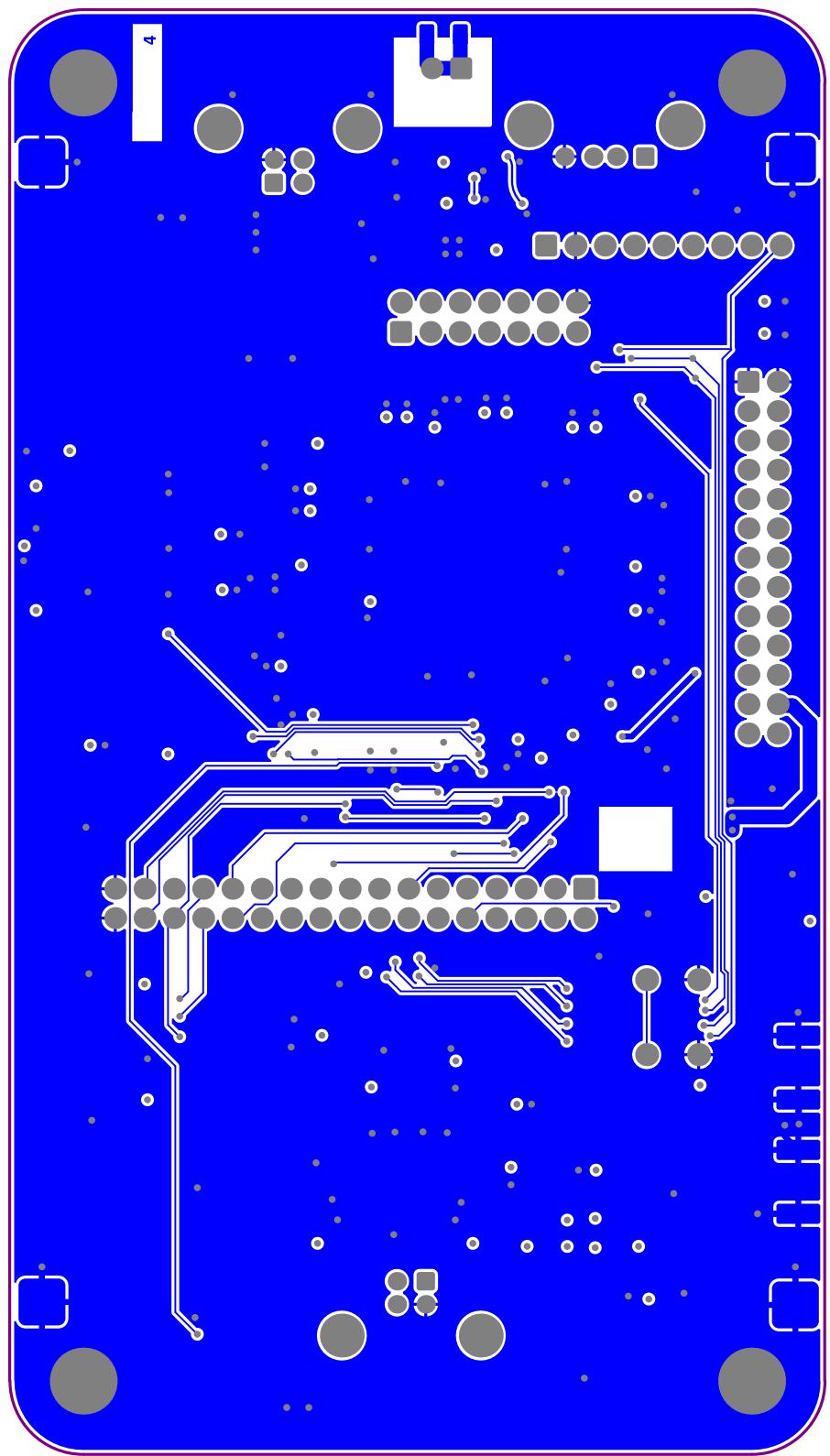


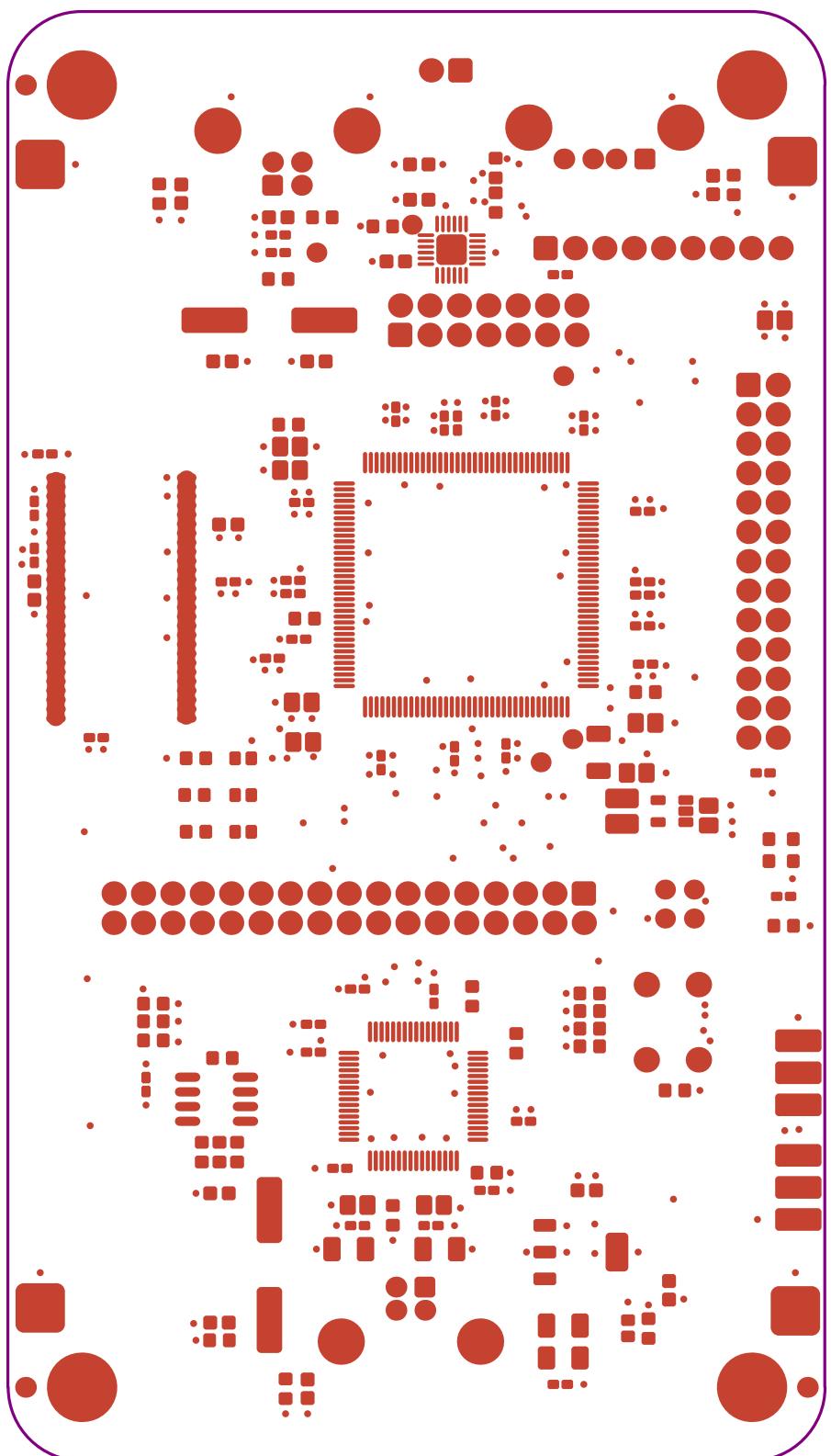
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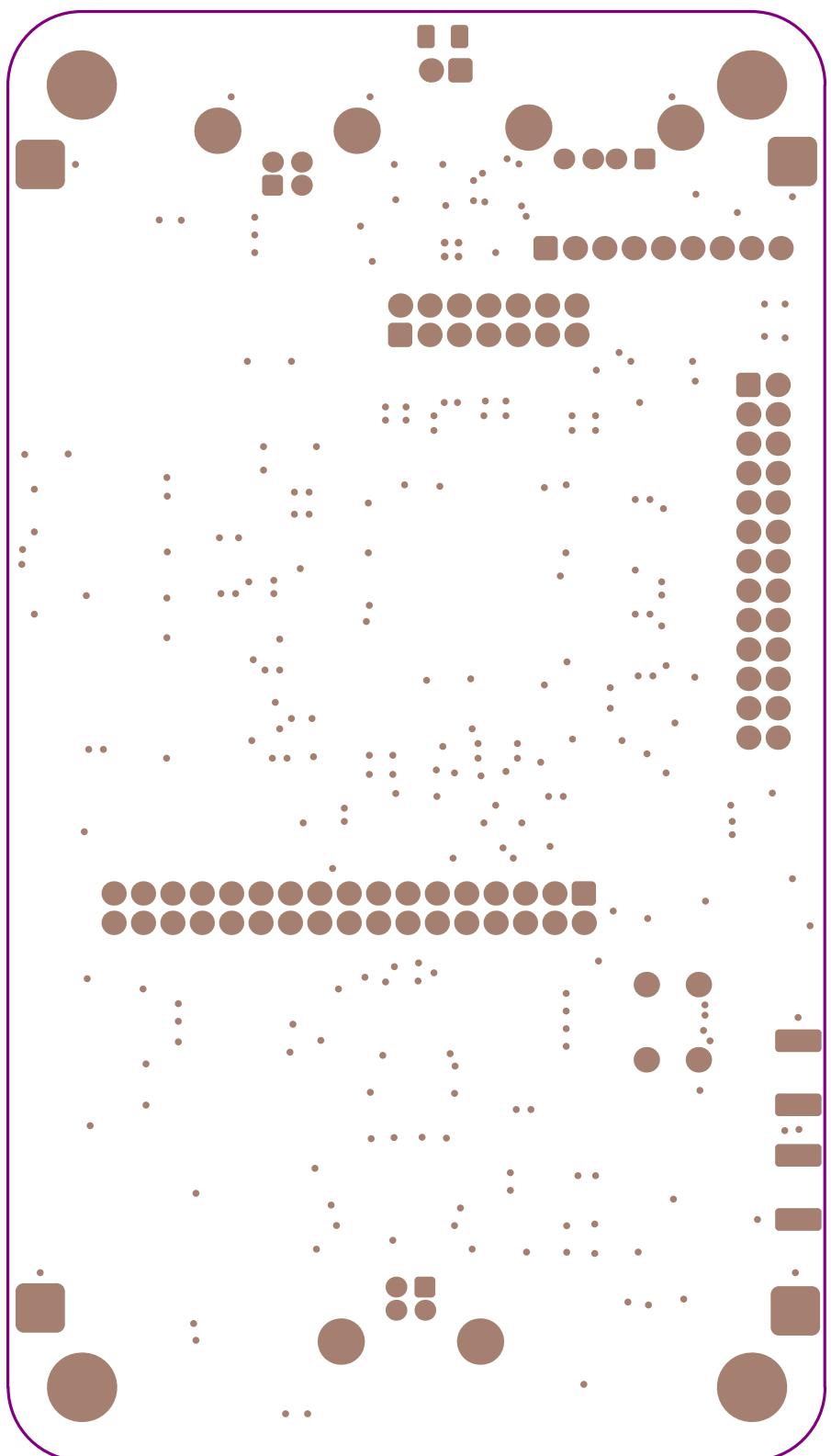


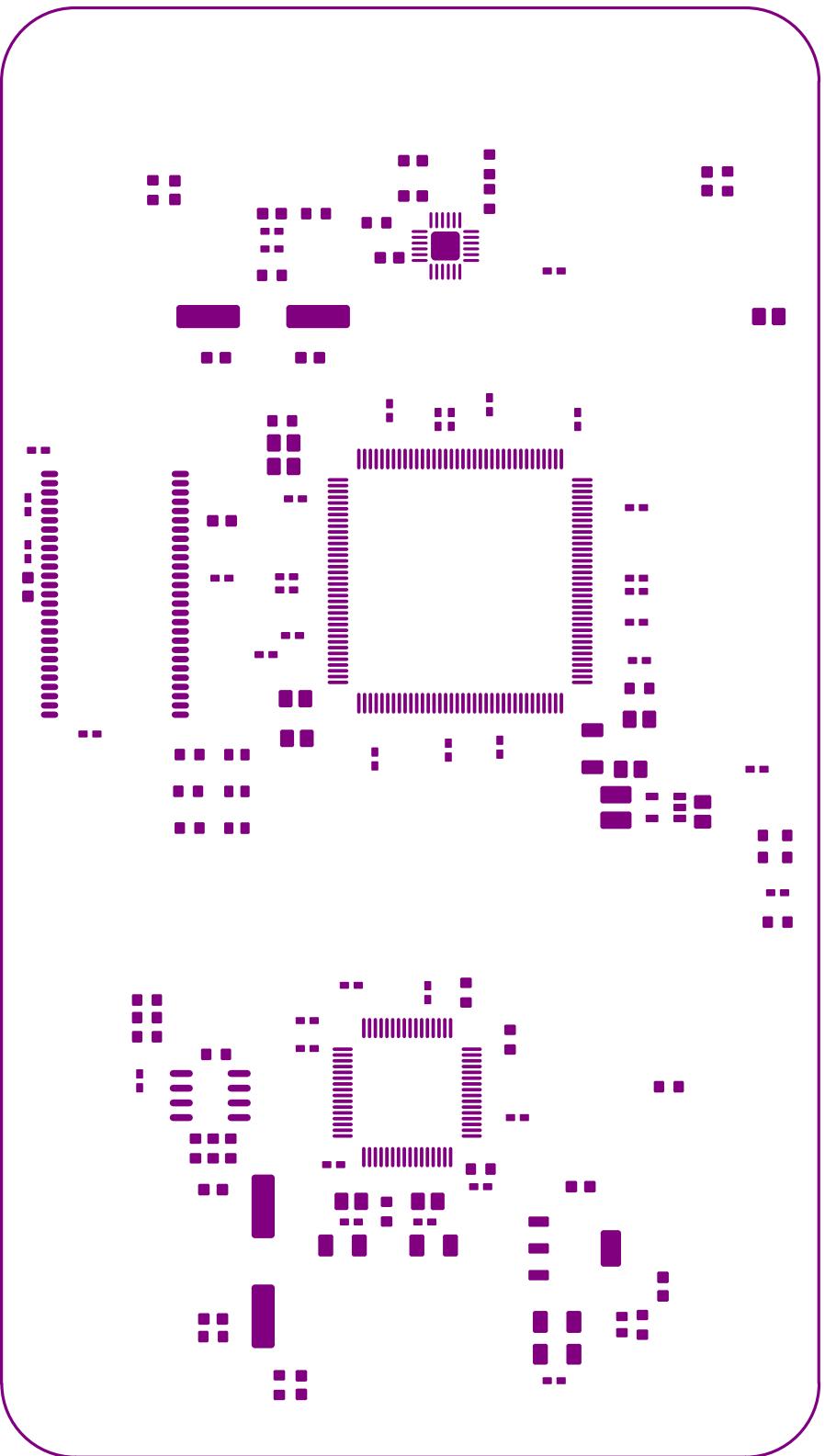


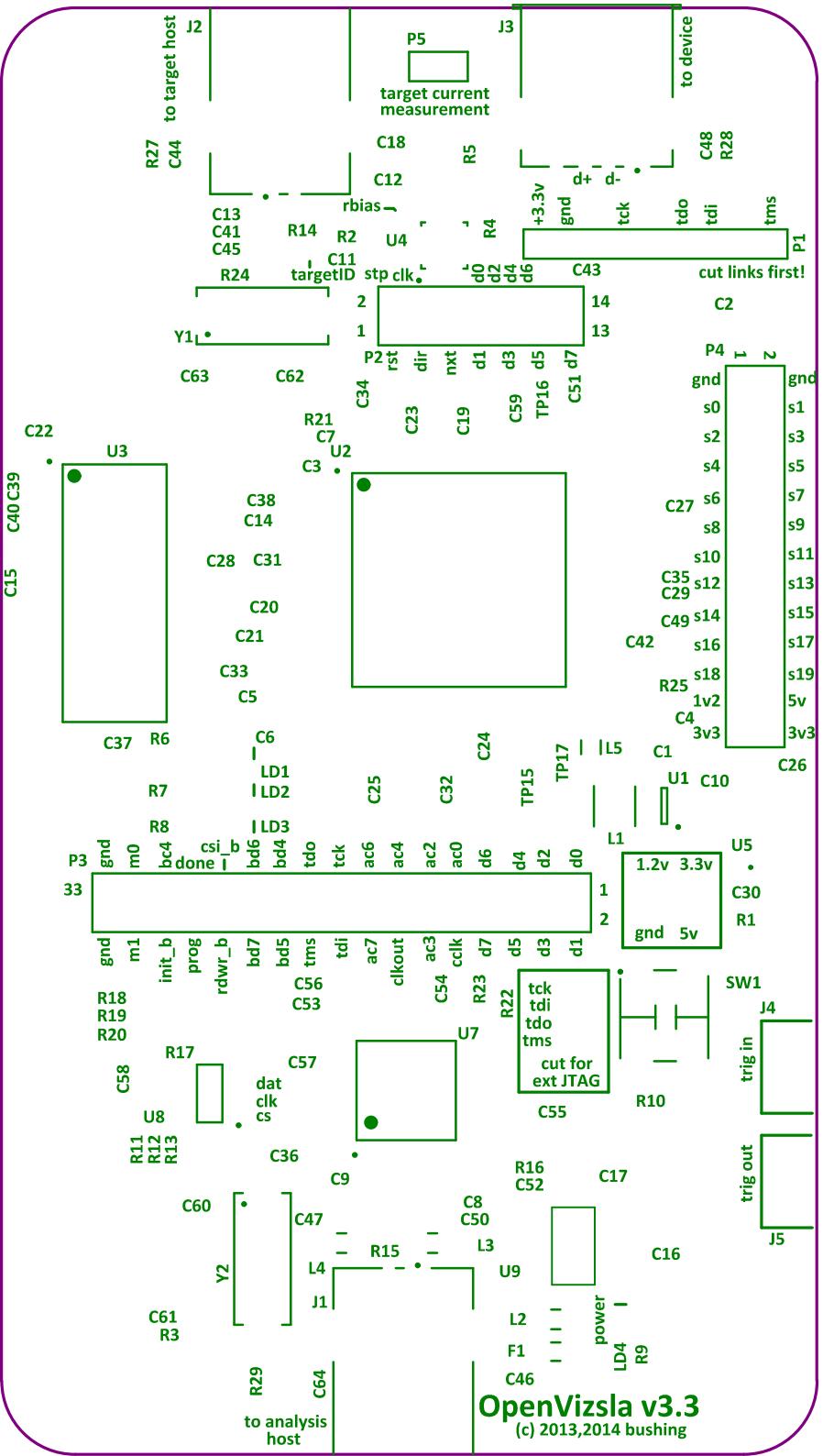












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