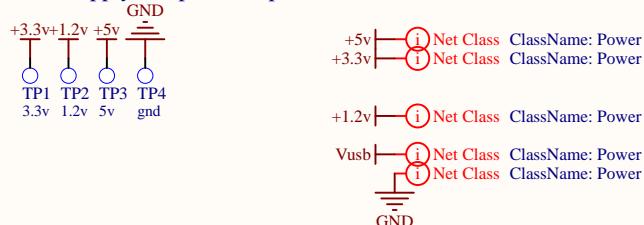


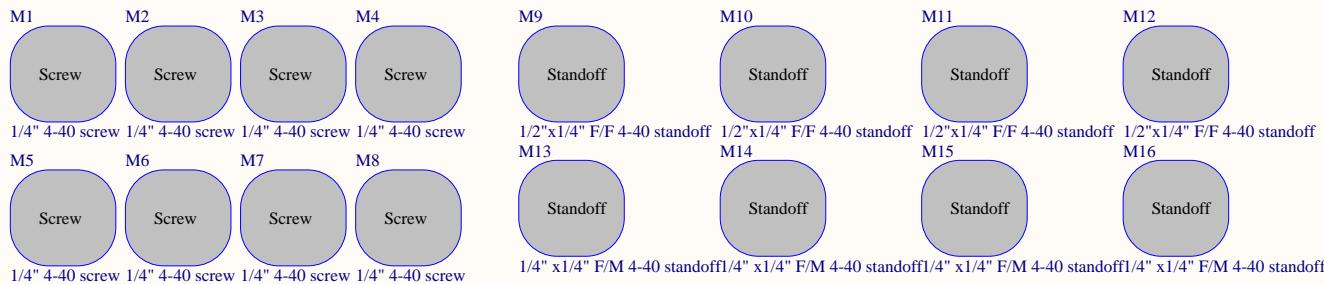
Power supply test points, top side



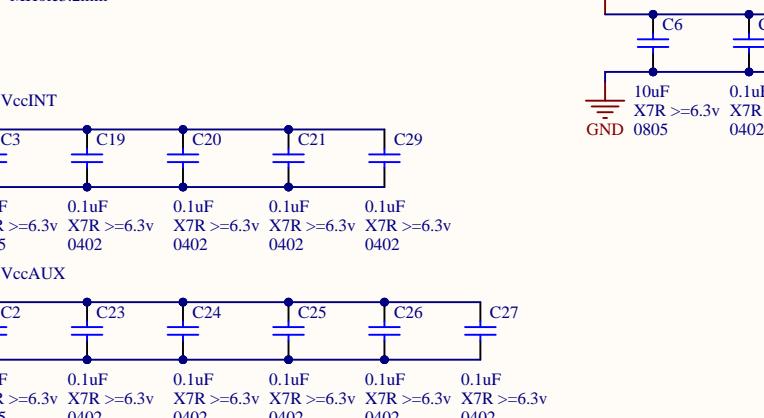
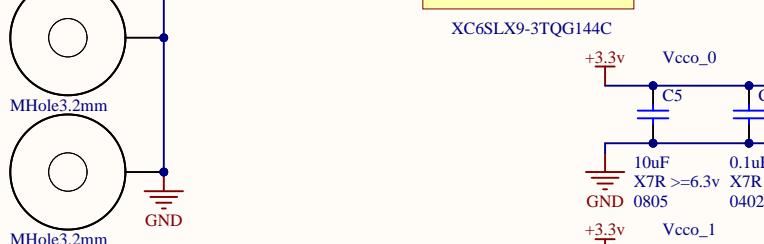
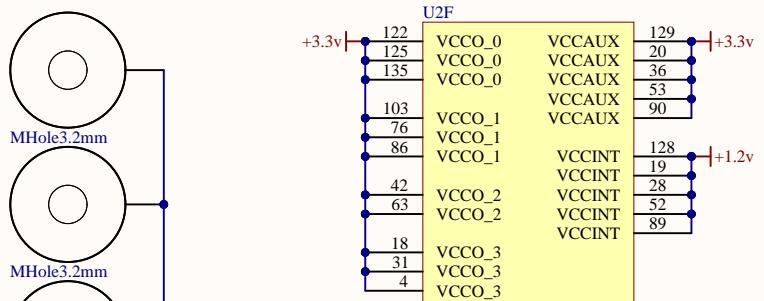
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Date:	3/22/2021	Sheet of
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A

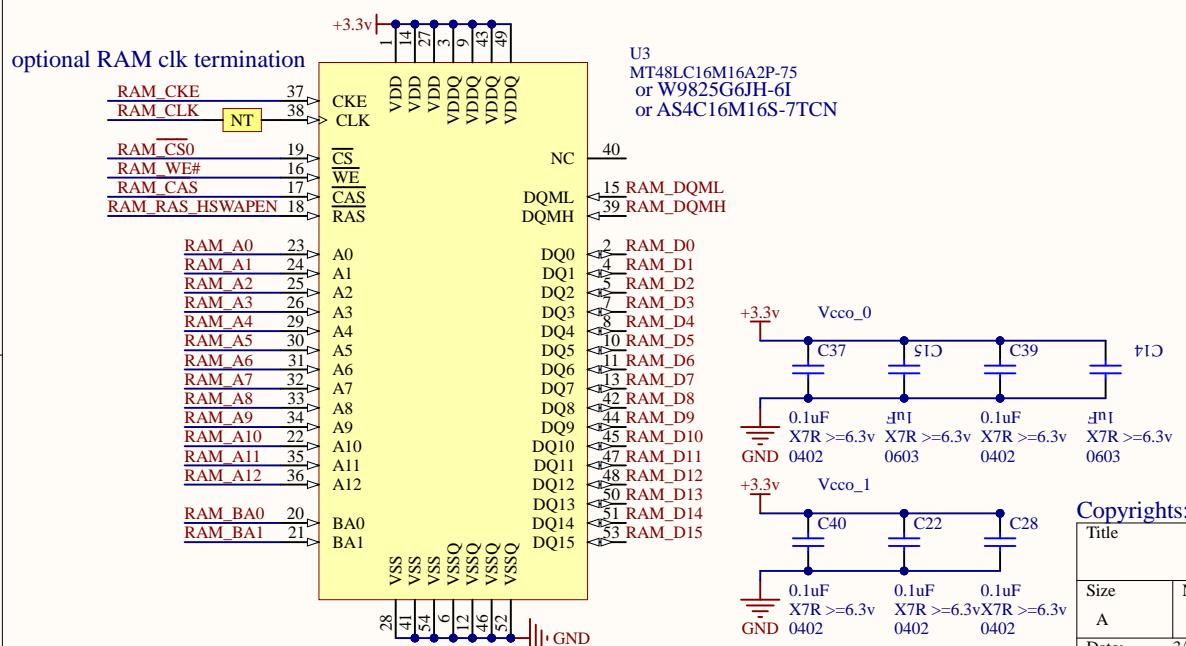
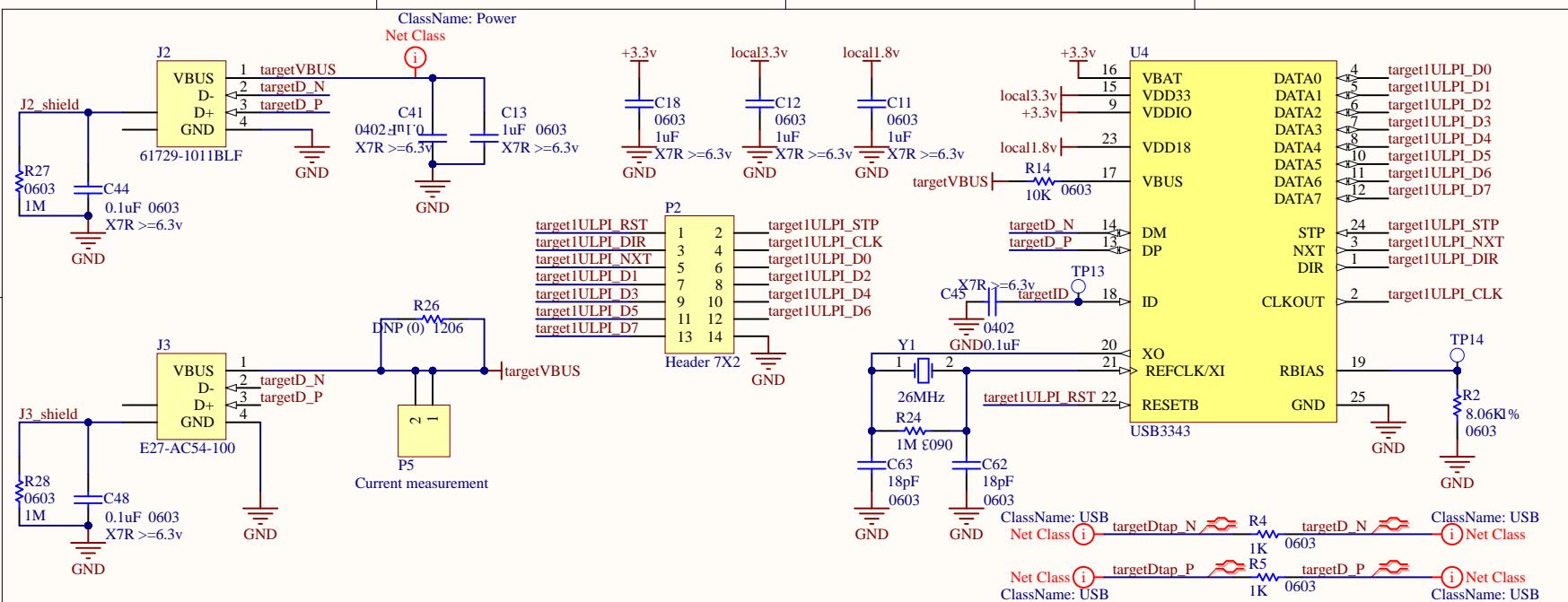


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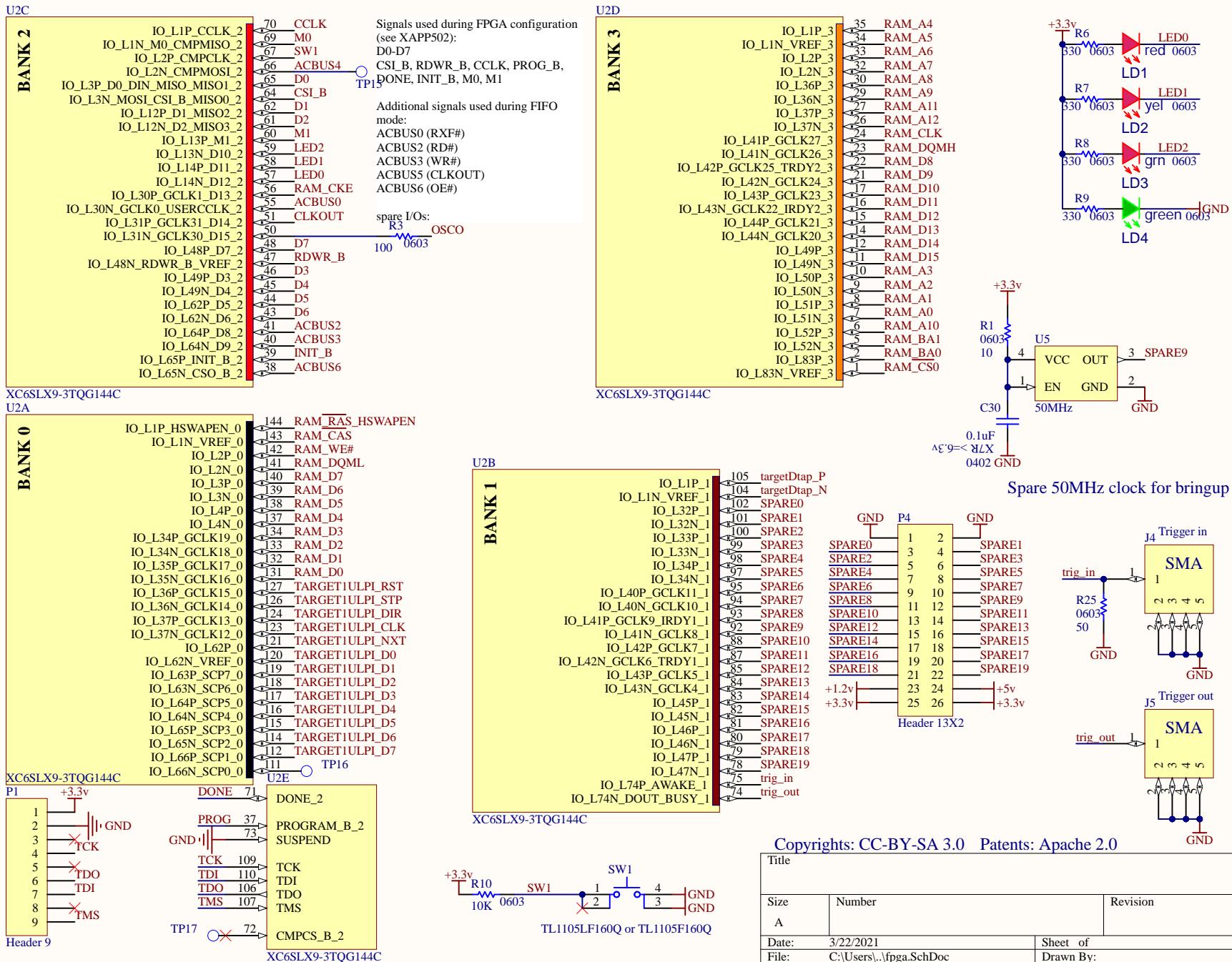


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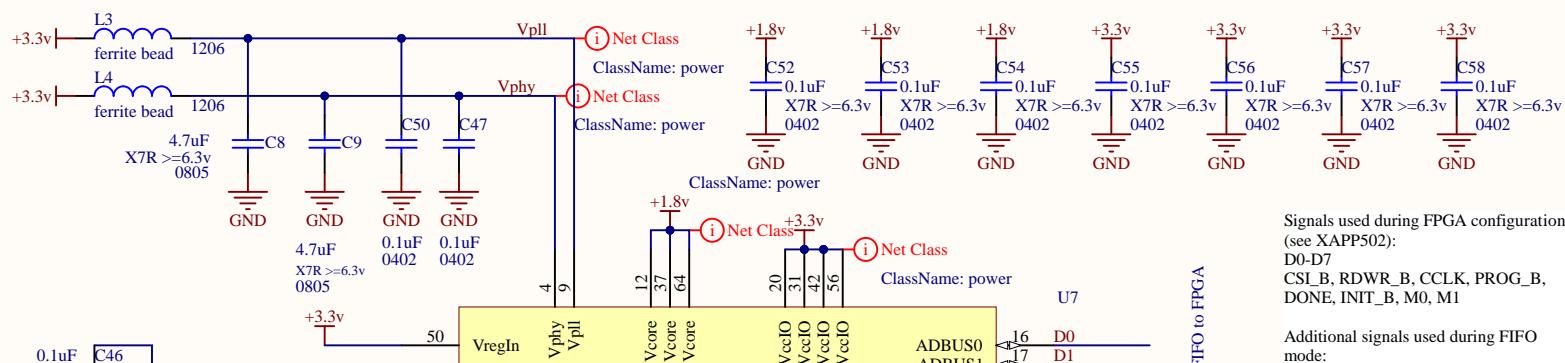
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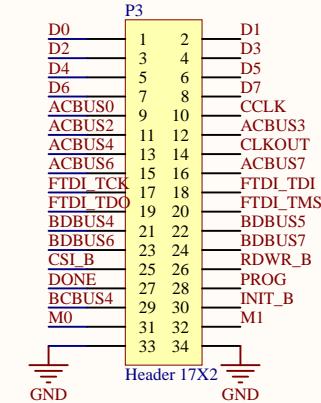
A



Signals used during FPGA configuration
(see XAPP502):
D0-D7
CSI_B, RDWR_B, CCLK, PROG_B,
DONE, INIT_B, M0, M1

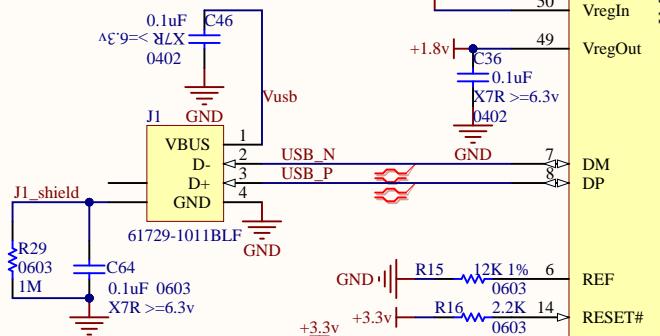
Additional signals used during FIFO mode:
ACBUS0 (RXF#)
ACBUS2 (RD#)
ACBUS3 (WR#)
ACBUSS (CLKOUT)
ACBUS6 (OE#)

spare I/Os:

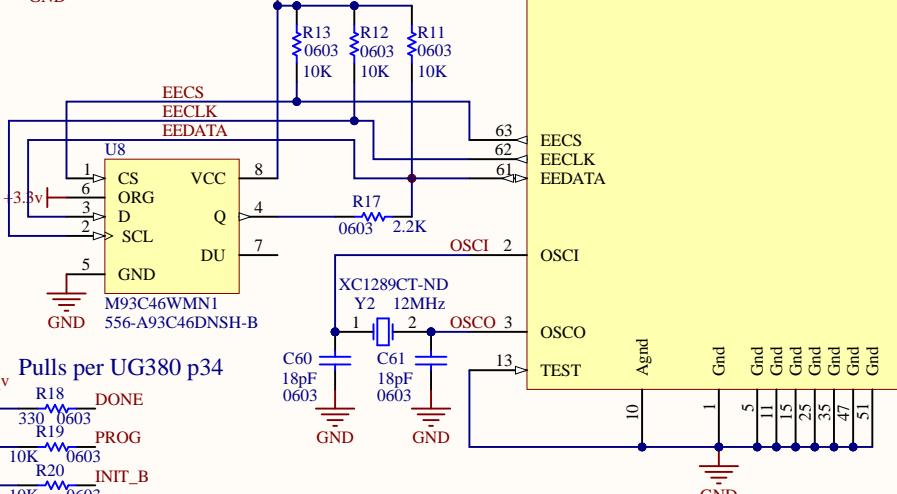


FT2232H

B



C

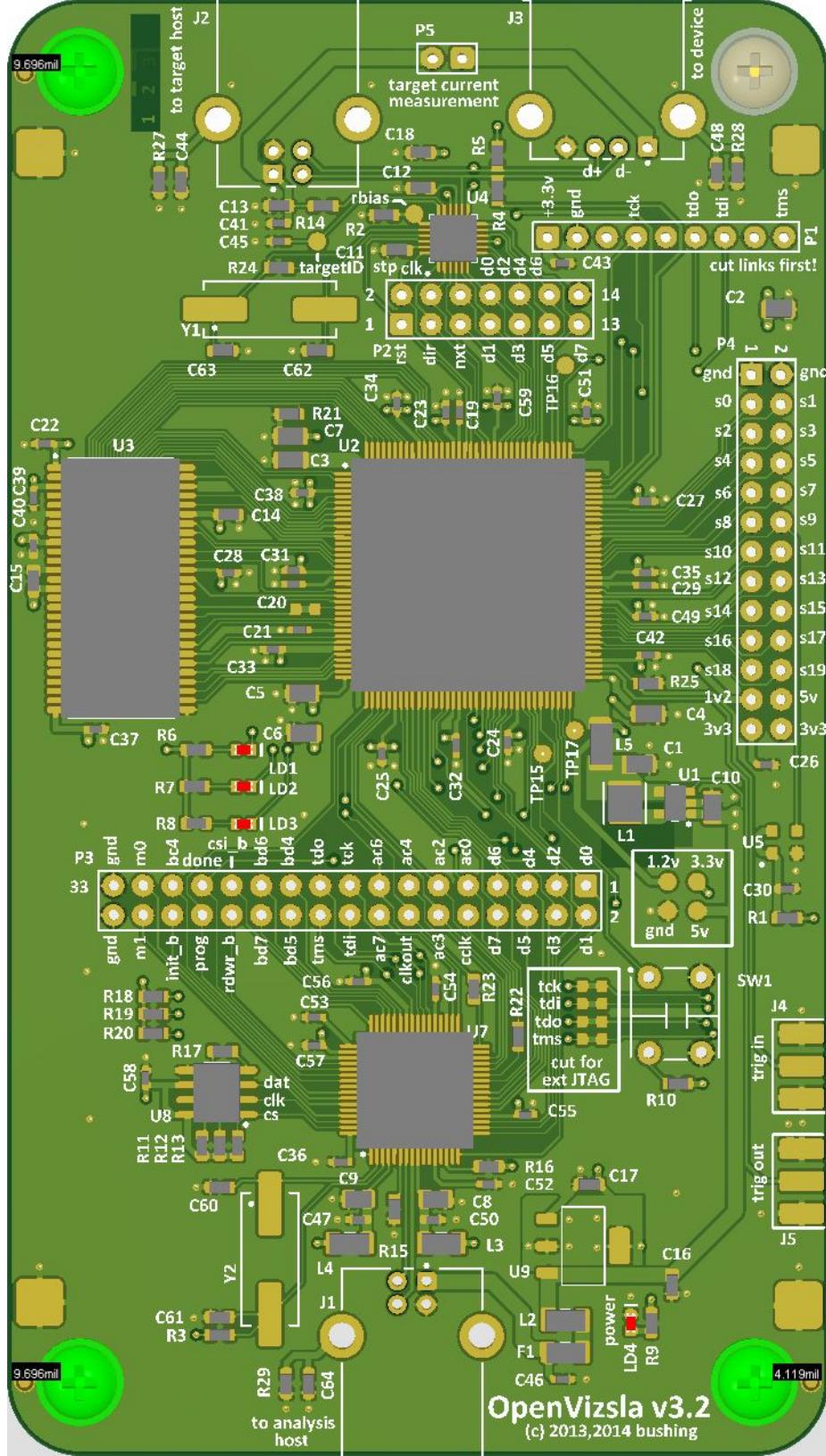


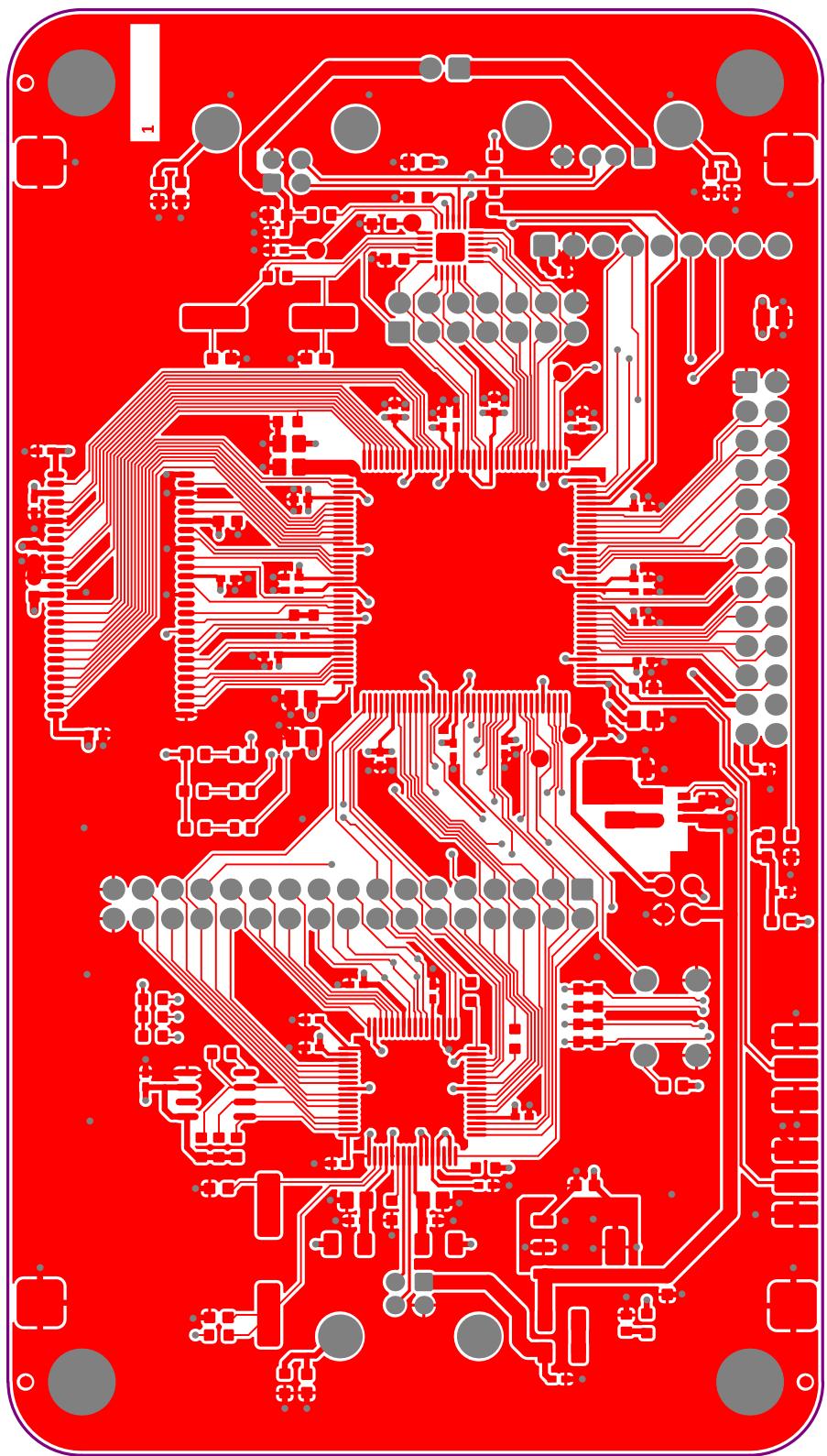
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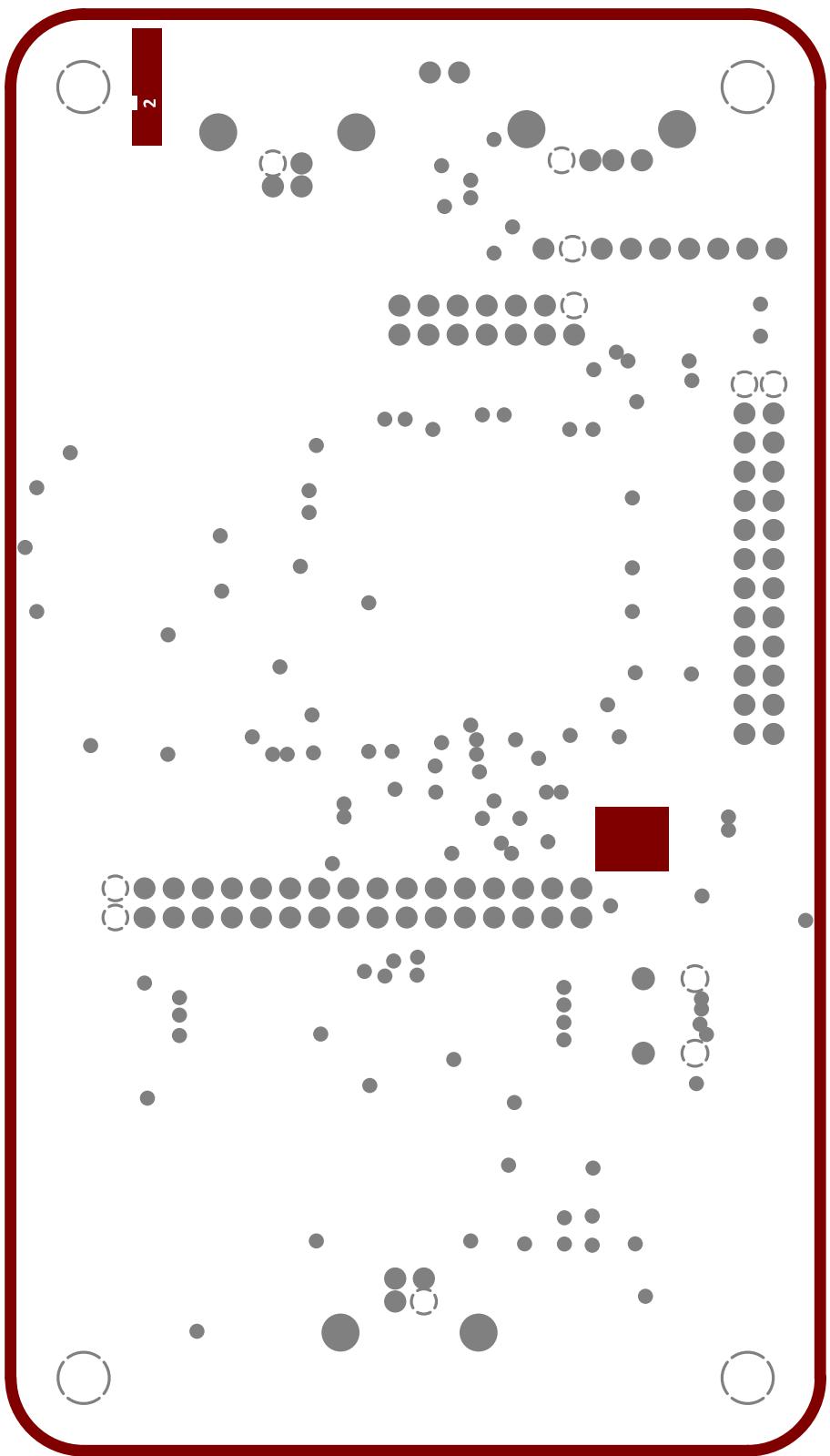


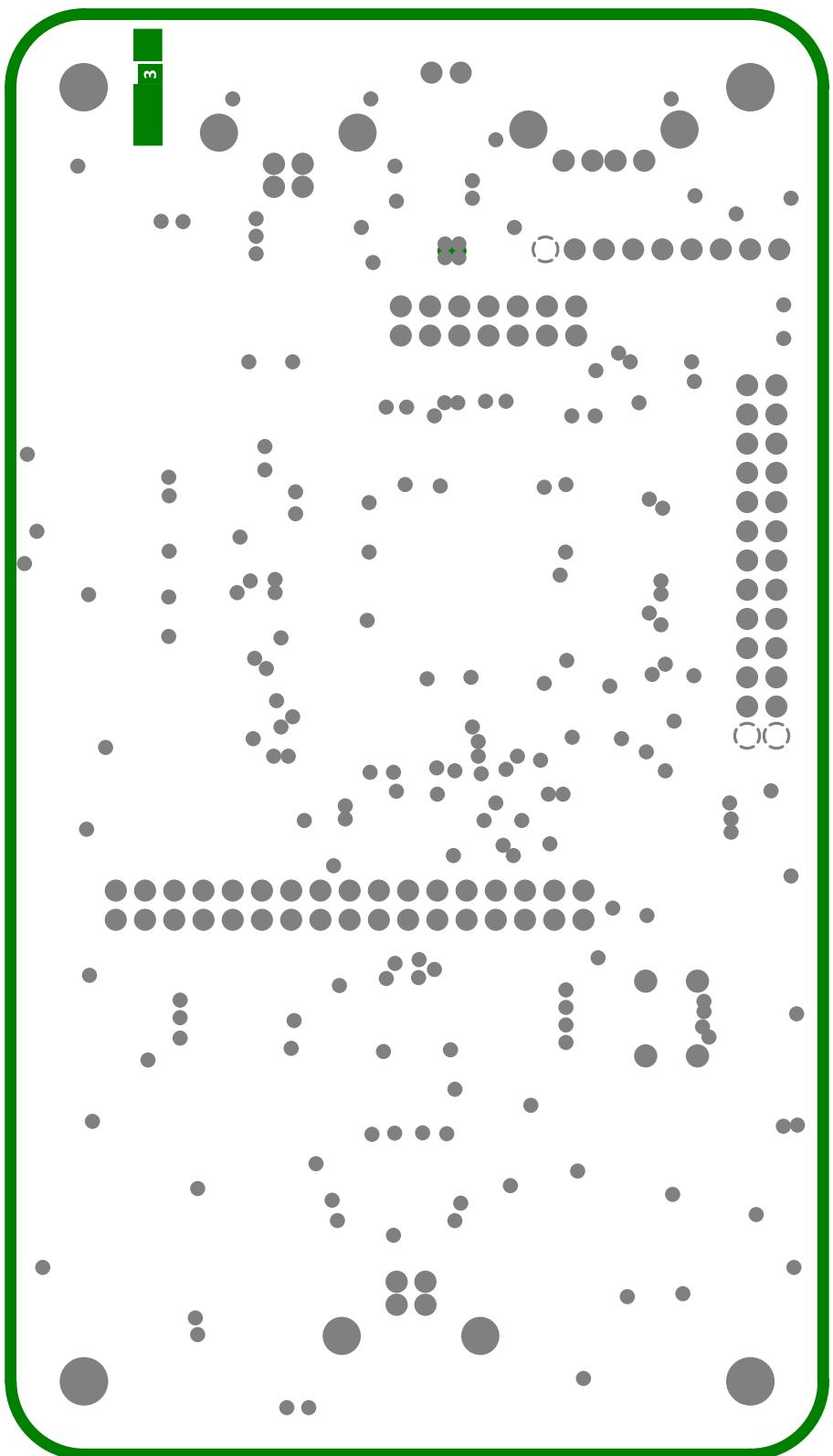
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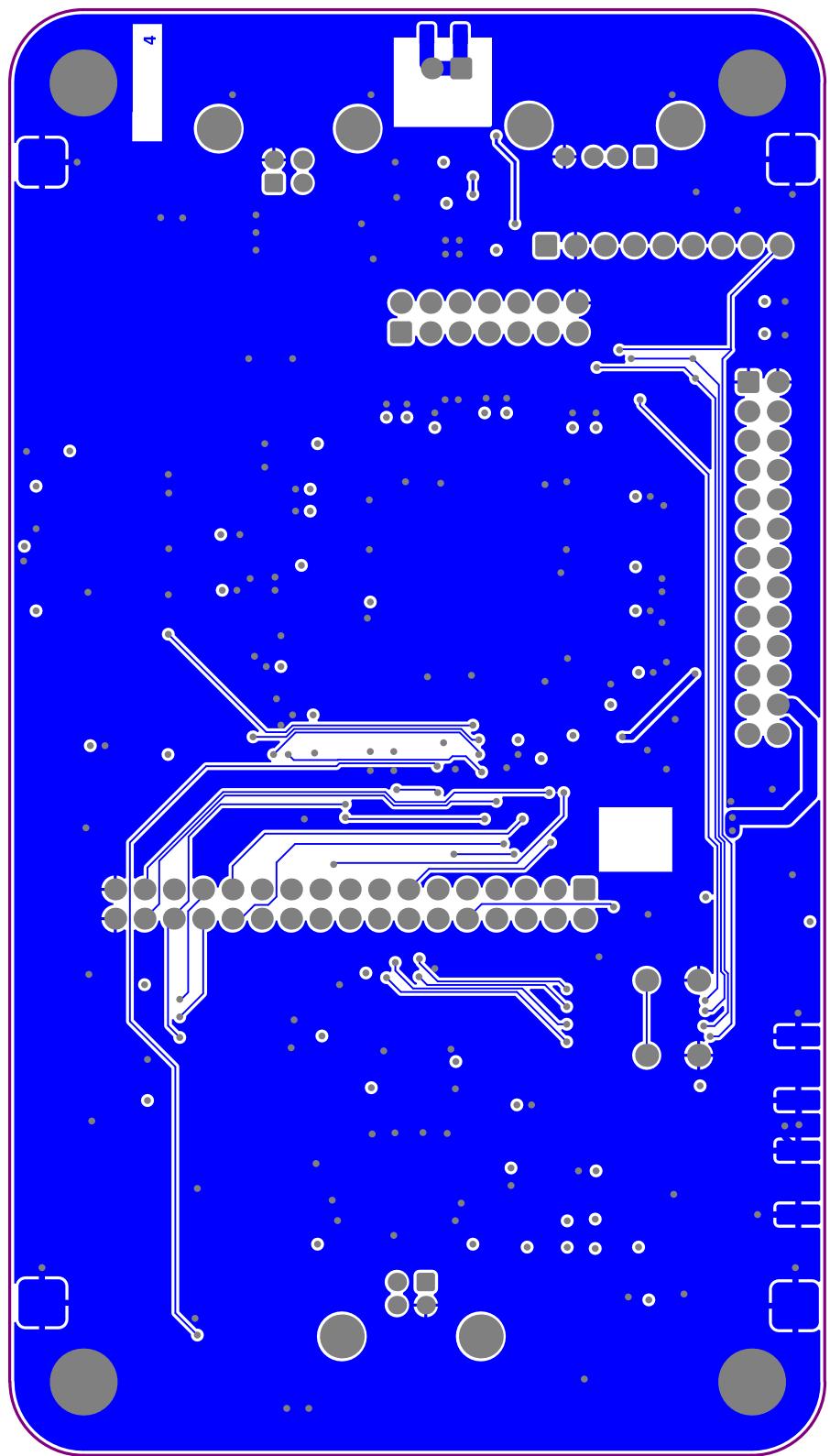
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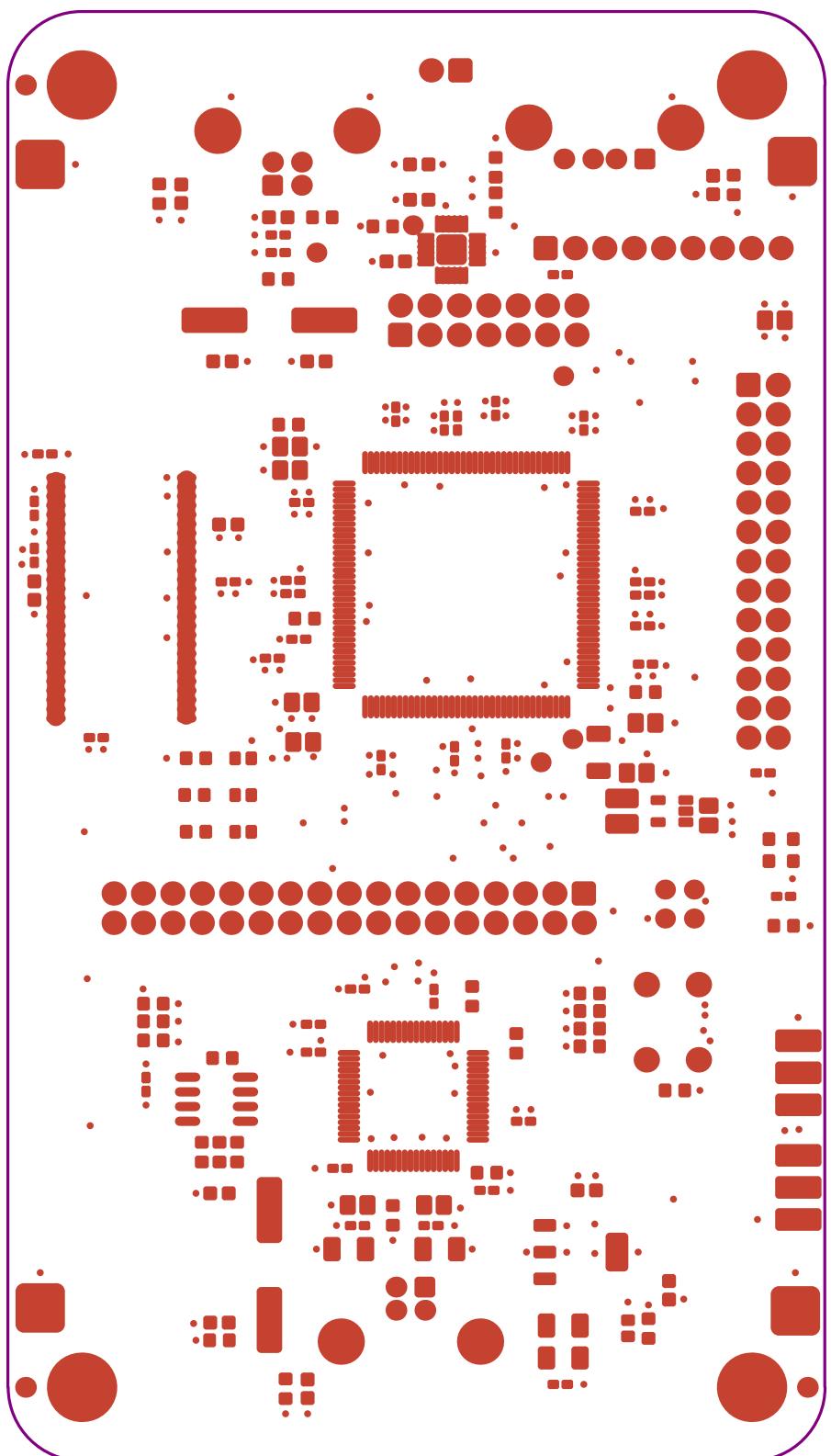


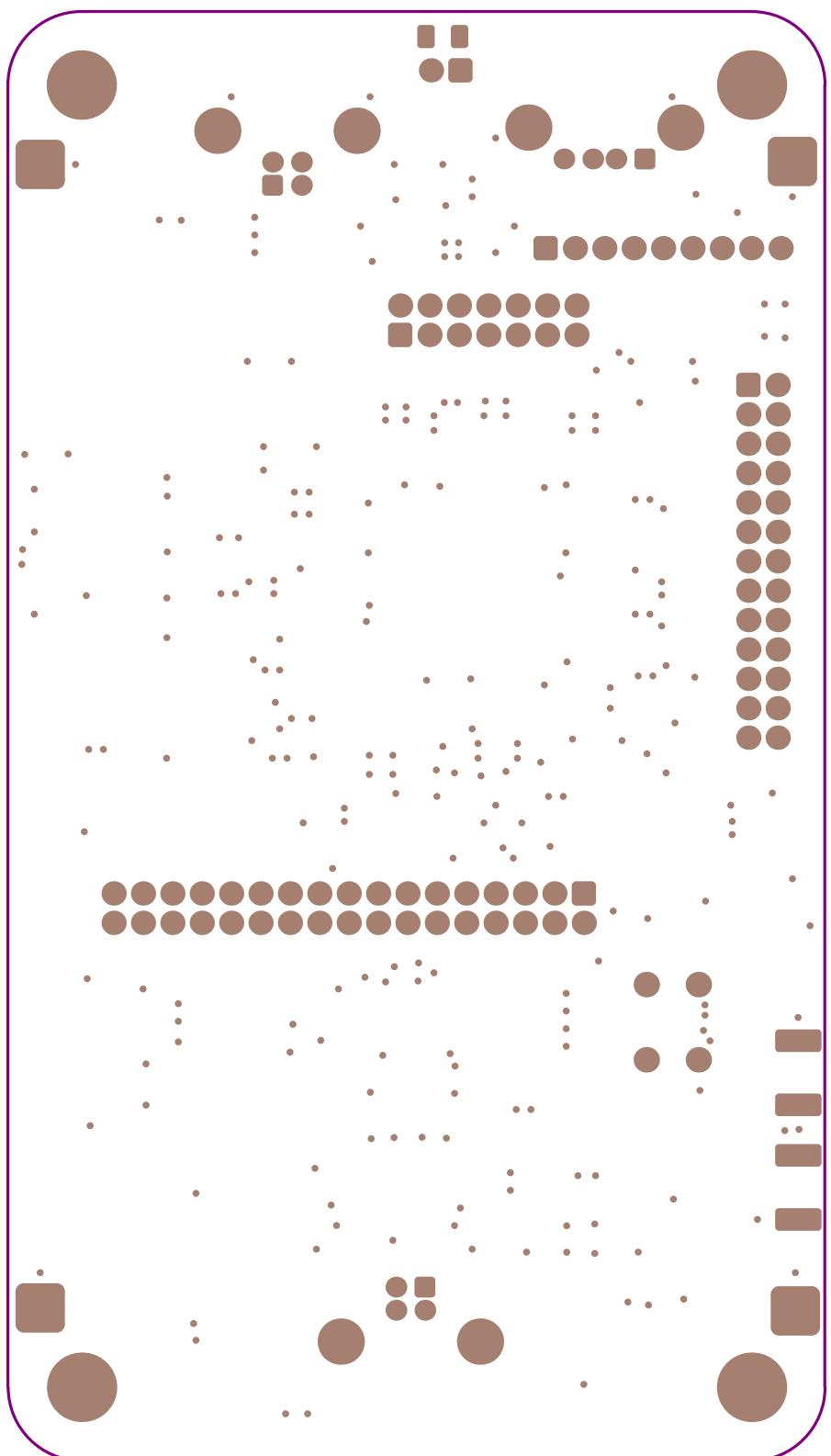


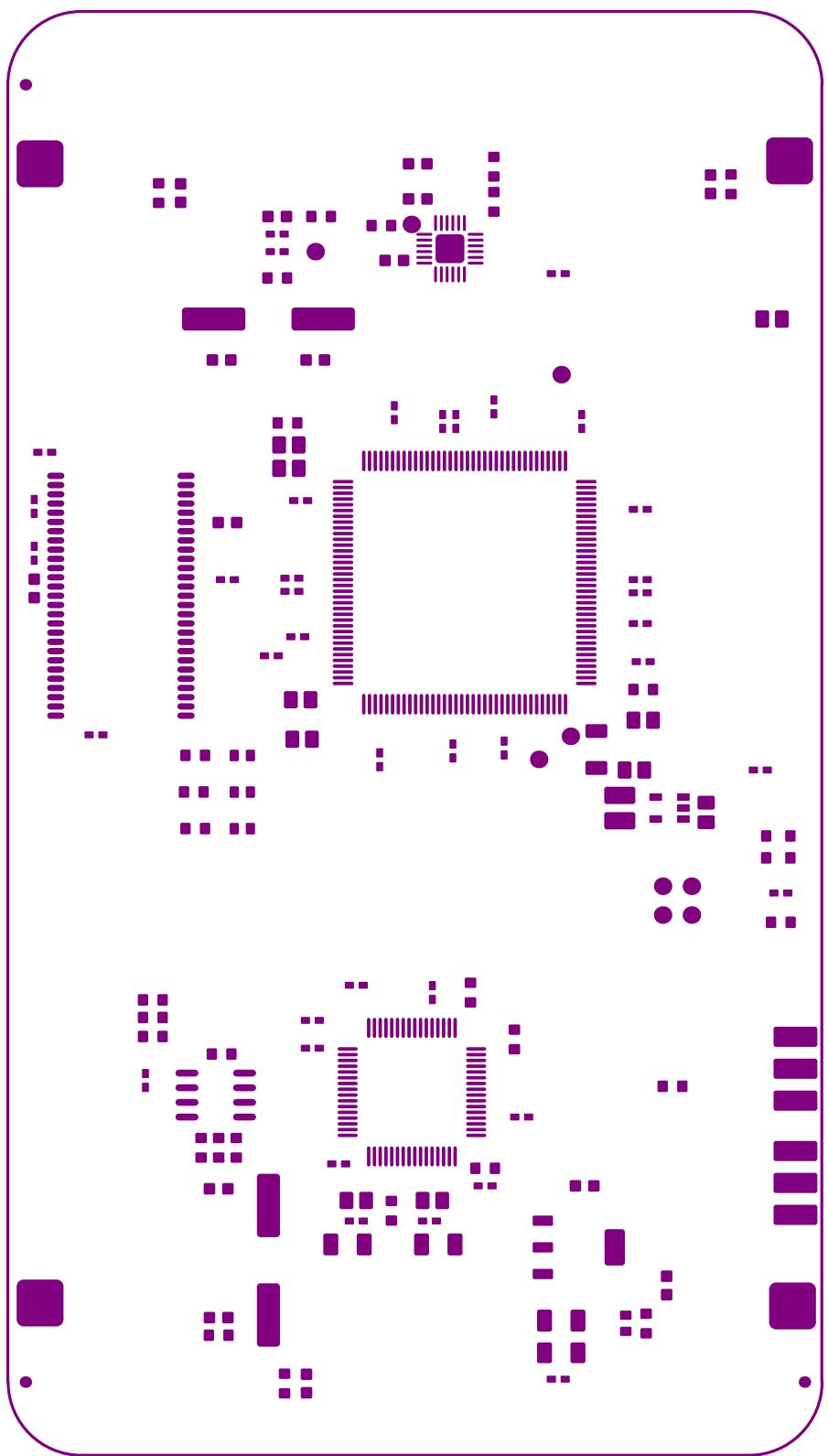


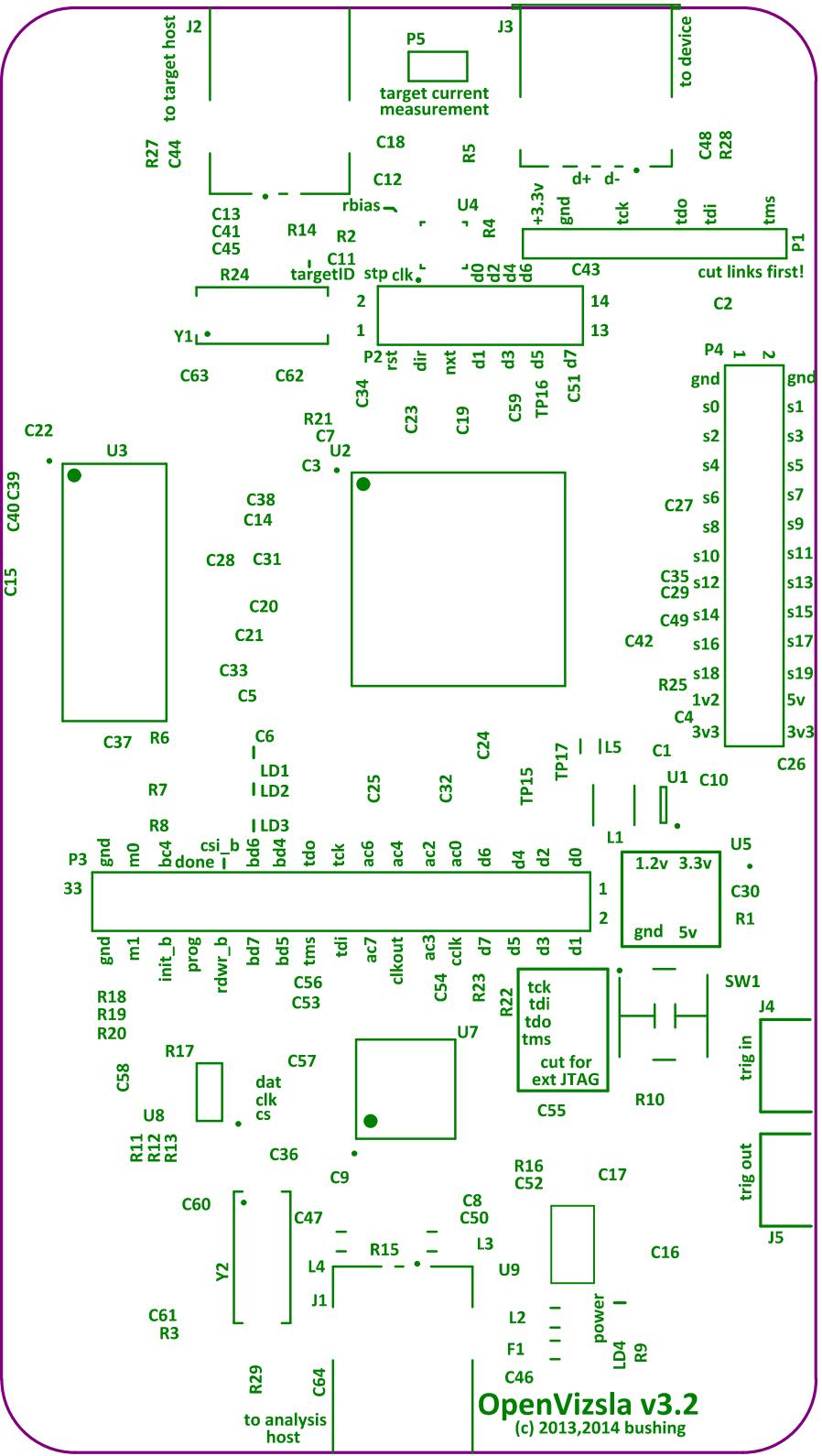












cut links first!
measure current
forget current
- trace cut



R26 -

cut trace for
measure current
forget current
- trace cut

Vans
D+
D-
Bng



