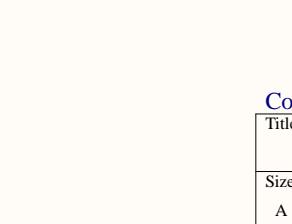
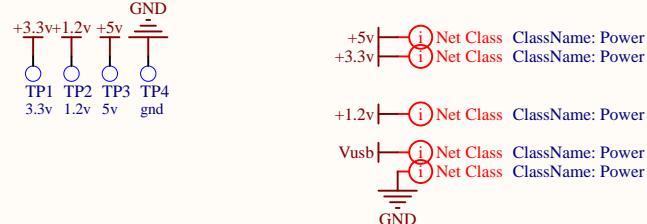


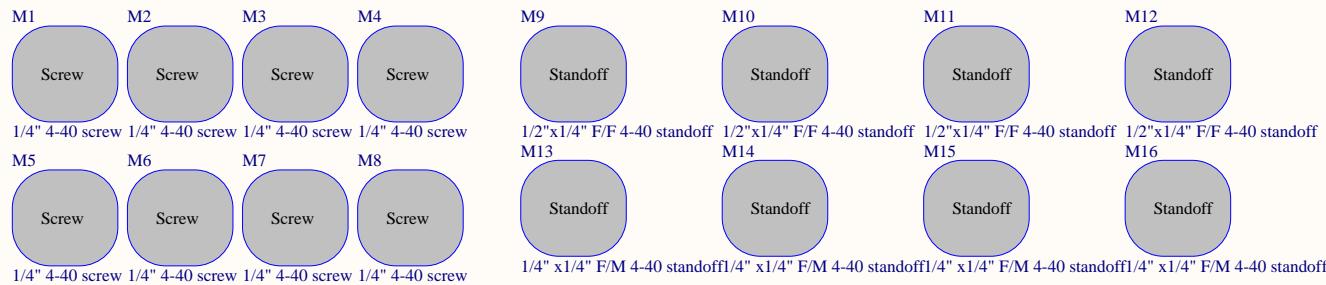
Power supply test points, top side



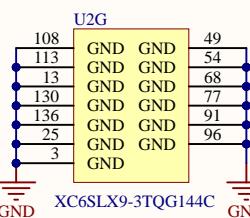
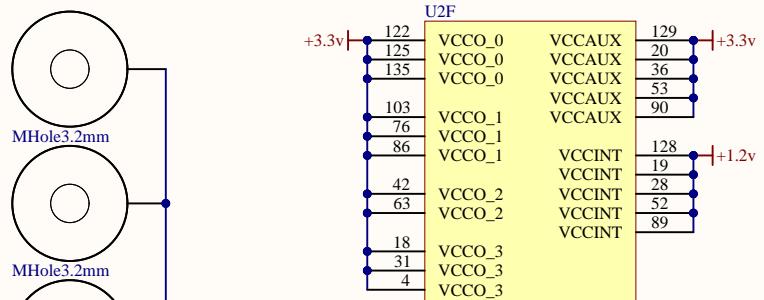
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Title		
Size	Number	Revision
A		
Date:	4/10/2021	Sheet of
File:	C:\Users\...\power.SchDoc	Drawn By:

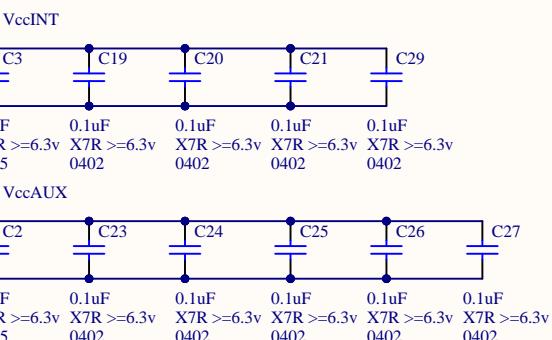
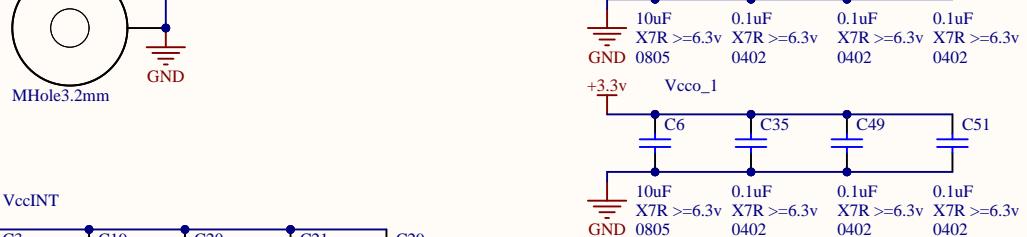
A



B

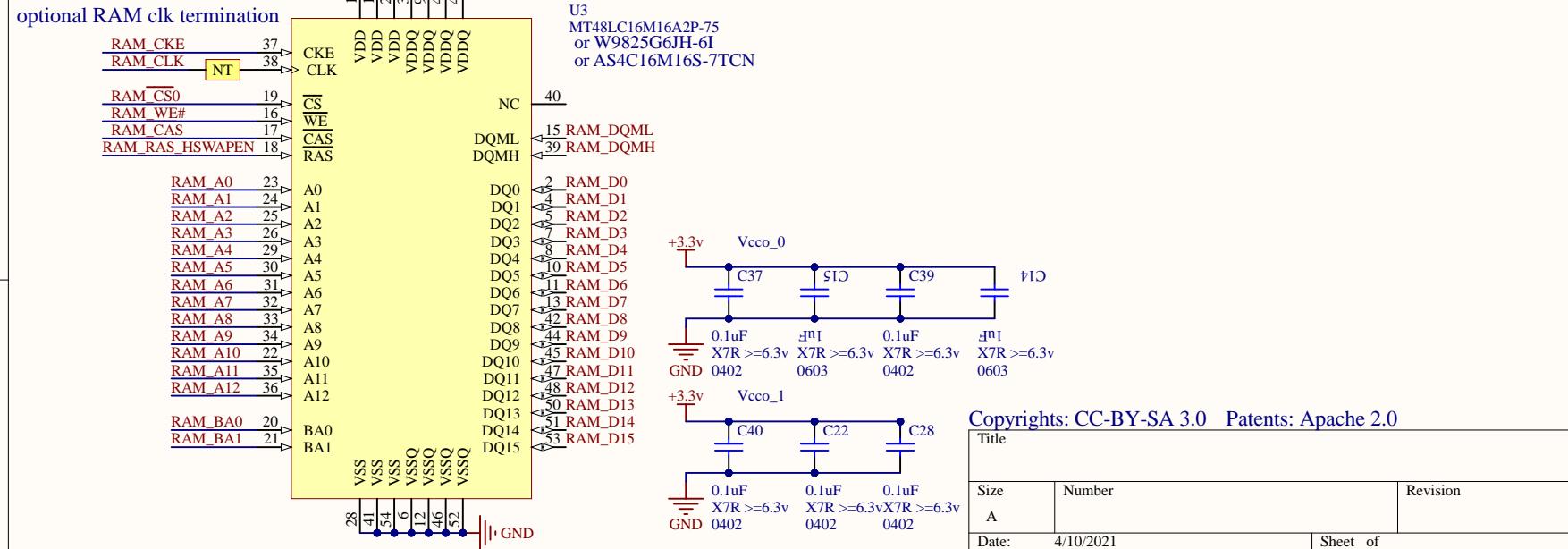
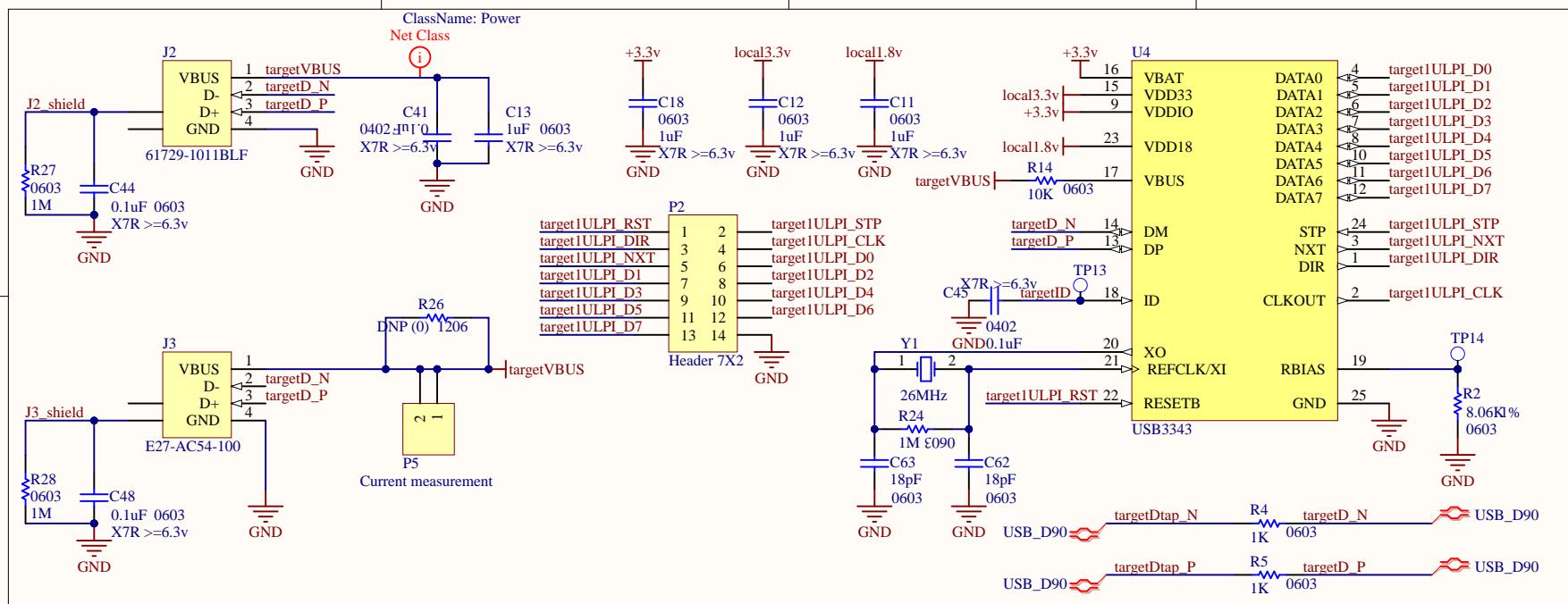


C

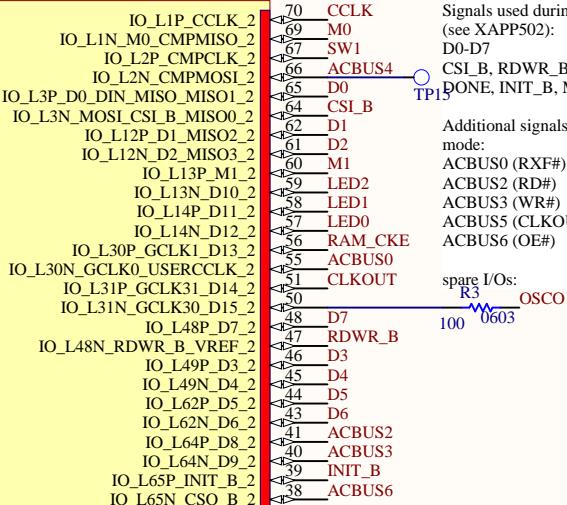


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Title		
Size	Number	Revision
A		
Date:	4/10/2021	Sheet 2 of
File:	C:\Users\...\FPGA power v3.SchDoc	Drawn By:

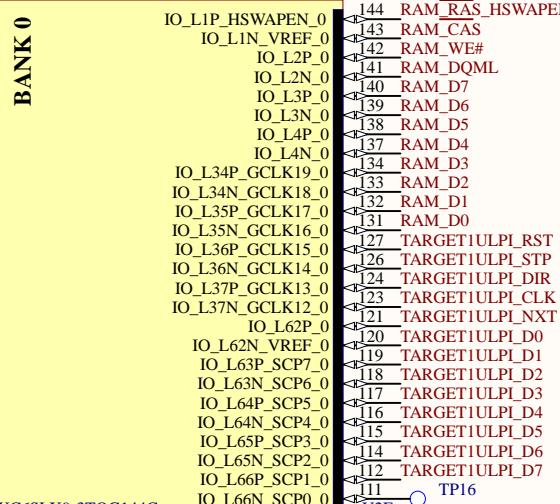


U2C

BANK 2

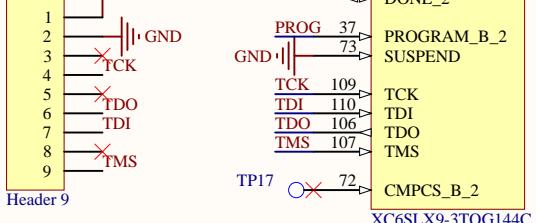
XC6SLX9-3TQG144C

U2A



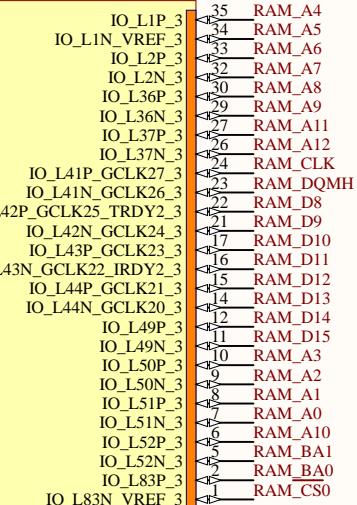
XC6SLX9-3TQG144C

P1

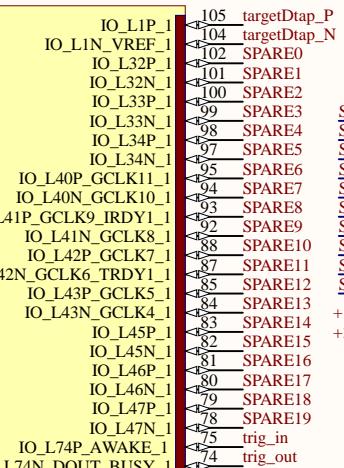


XC6SLX9-3TQG144C

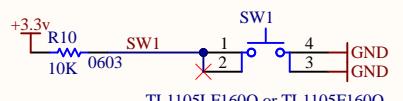
U2D

BANK 3

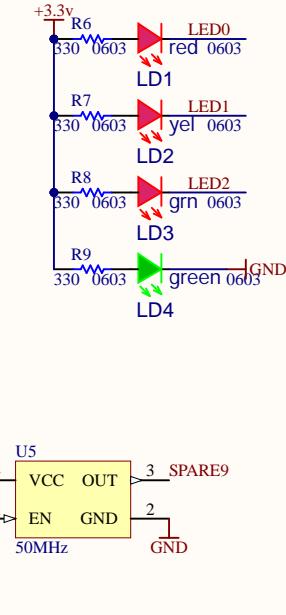
XC6SLX9-3TQG144C

BANK 1

XC6SLX9-3TQG144C



TL1105LF160Q or TL1105F160Q

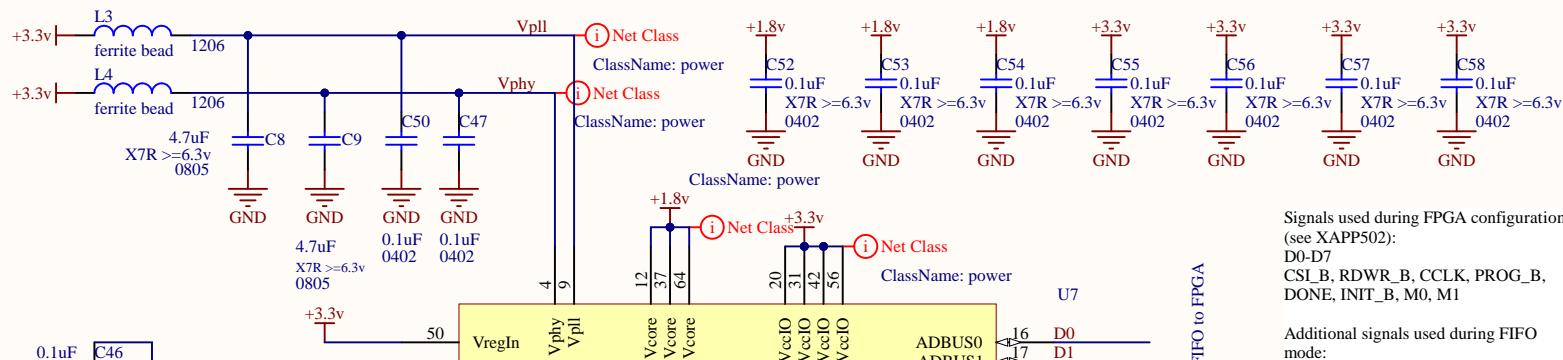


Spare 50MHz clock for bringup

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Title		
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Date:	4/10/2021	Sheet of
File:	C:\Users\.\fpga.SchDoc	Drawn By:

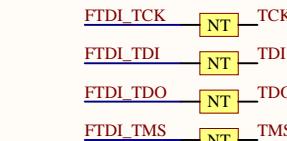
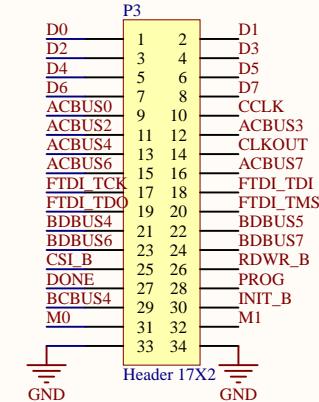
A



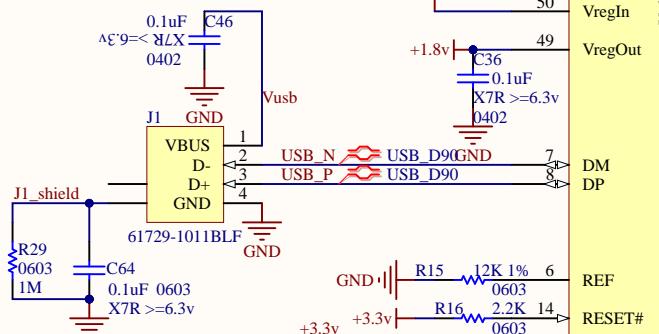
Signals used during FPGA configuration (see XAPP502):
D0-D7
CSI_B, RDWR_B, CCLK, PROG_B,
DONE, INIT_B, M0, M1

Additional signals used during FIFO mode:
ACBUS0 (RXF#)
ACBUS2 (RD#)
ACBUS3 (WR#)
ACBUSS (CLKOUT)
ACBUS6 (OE#)

spare I/Os:

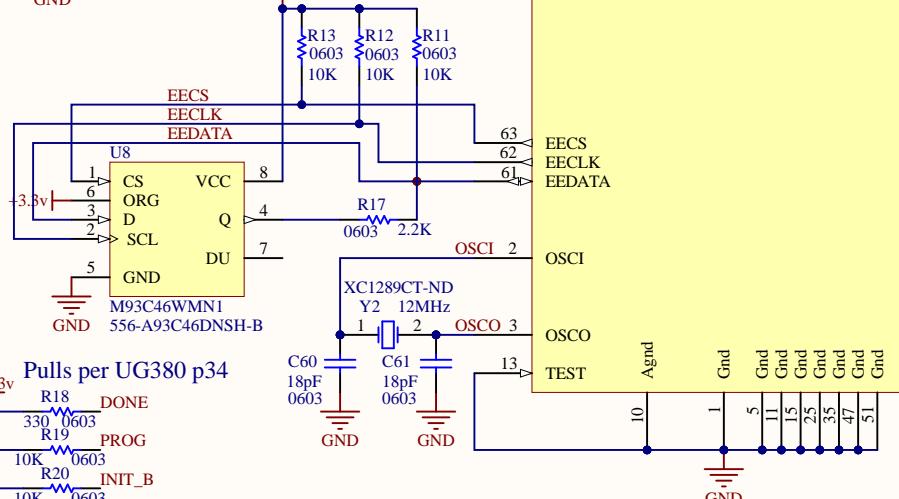


B

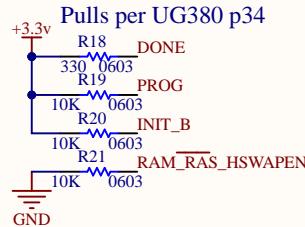


FT2232H

C



D



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