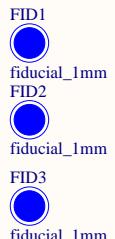
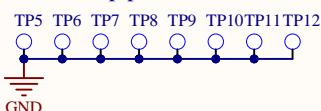
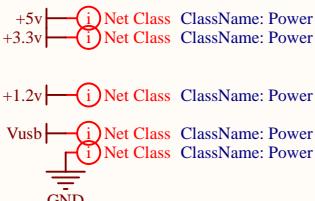
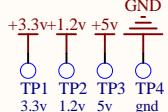


### Ground clip pads



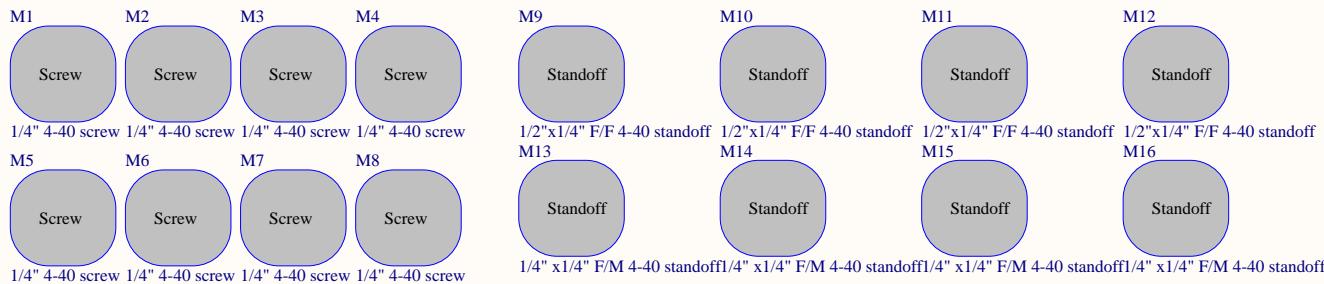
### Power supply test points, top side



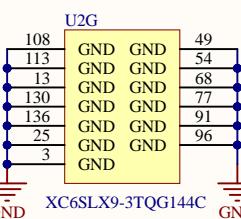
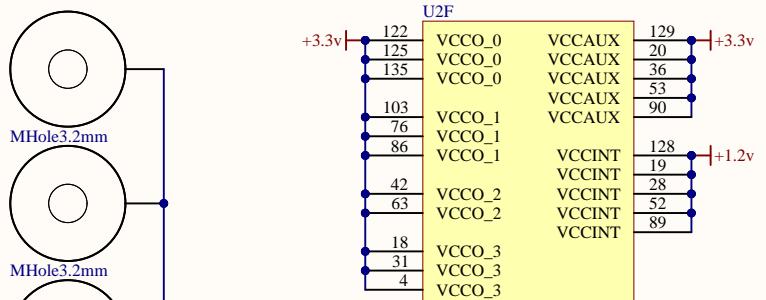
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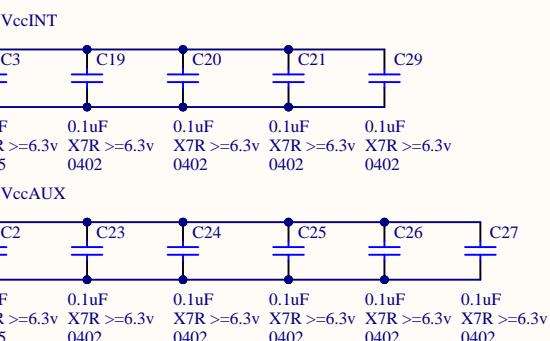
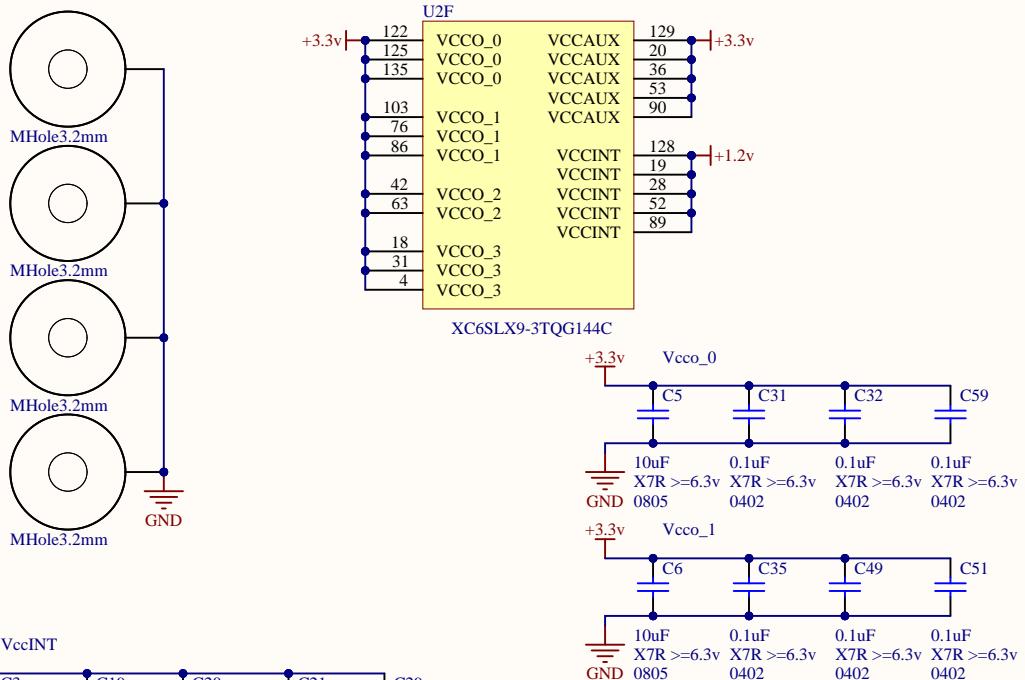
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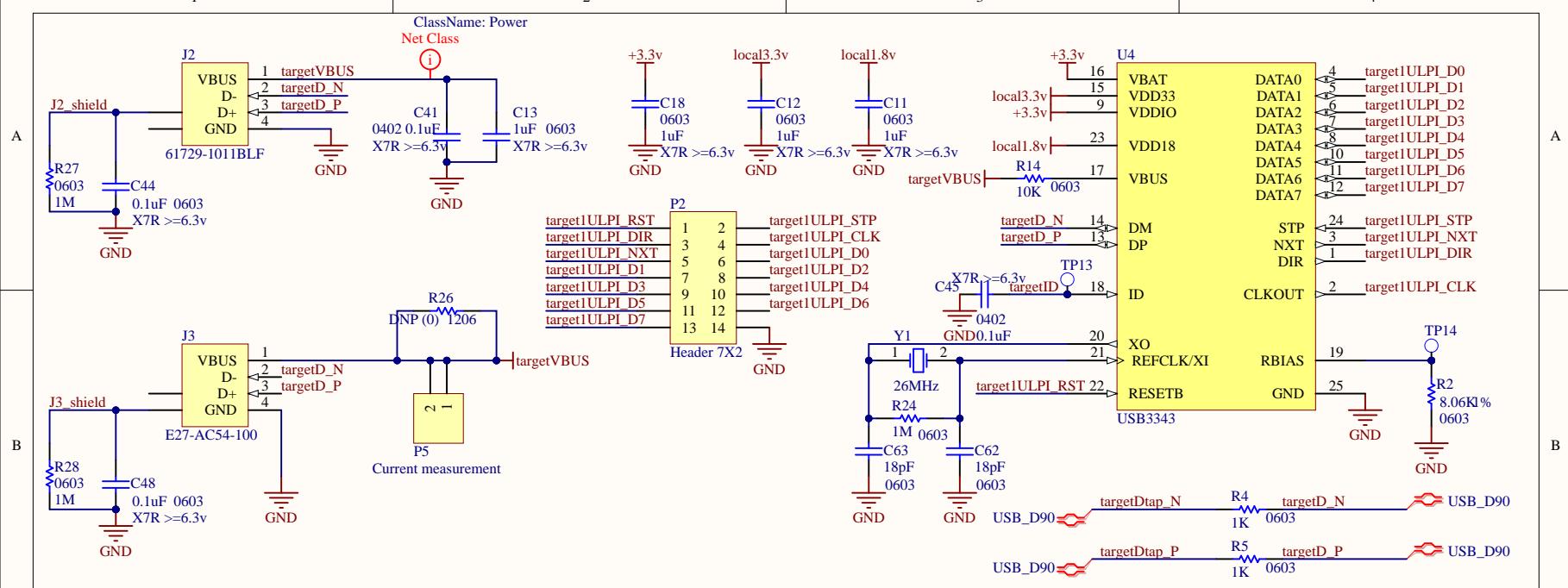


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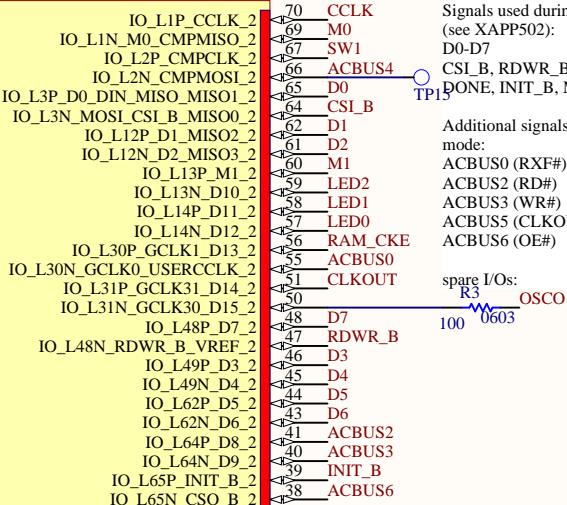


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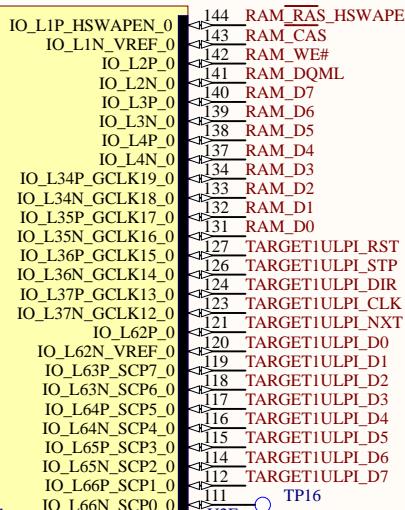


U2C

**BANK 2**

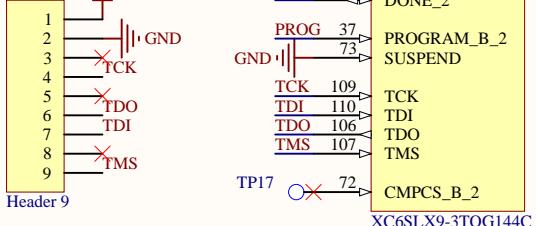
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U2A

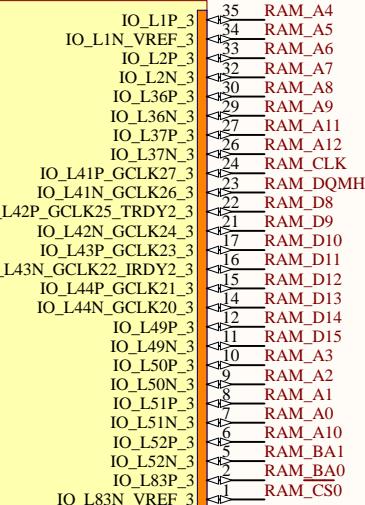


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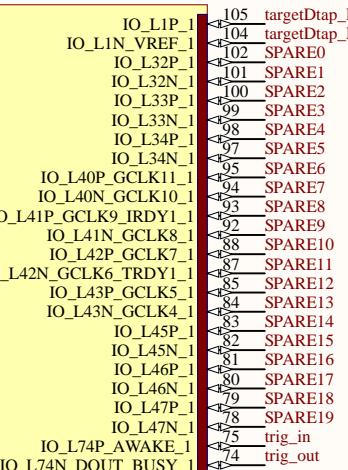
P1



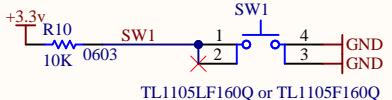
U2D

**BANK 3**

XC6SLX9-3TQG144C

**BANK 1**

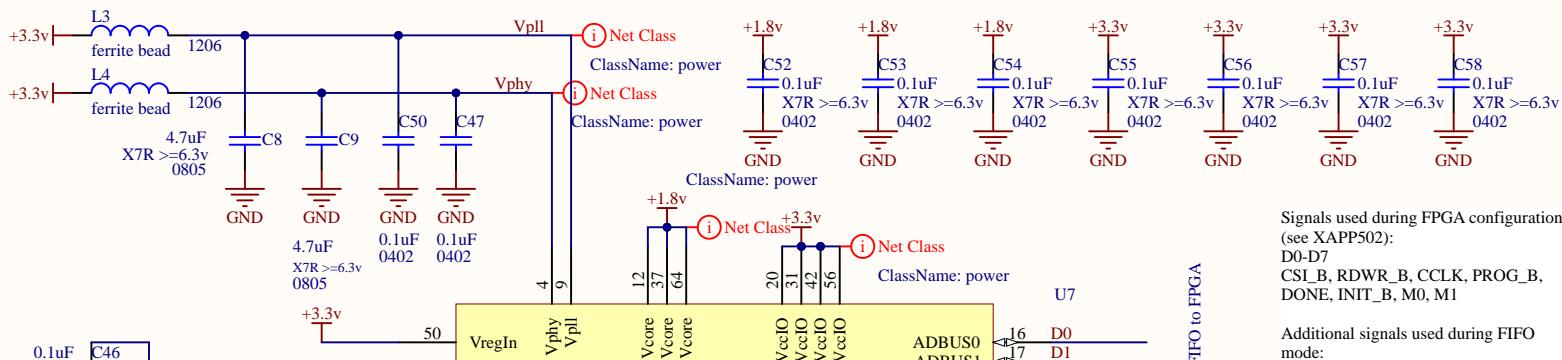
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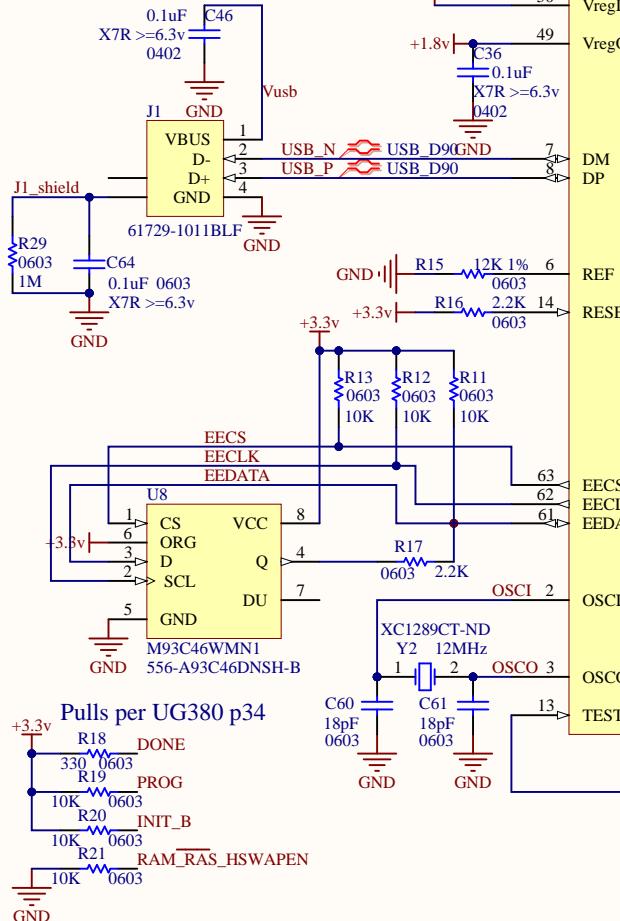
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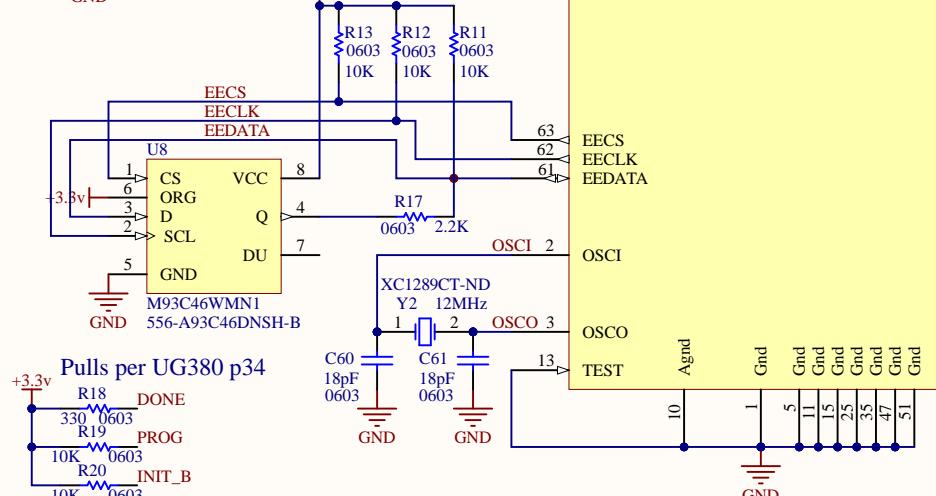
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B



C



D



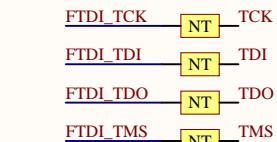
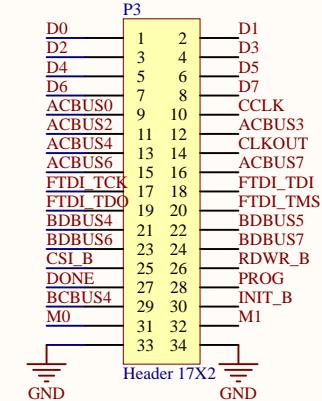
## FT2232H

Configuration / FIFO to FPGA

Signals used during FPGA configuration (see XAPP502):  
D0-D7  
CSI\_B, RDWR\_B, CCLK, PROG\_B,  
DONE, INIT\_B, M0, M1

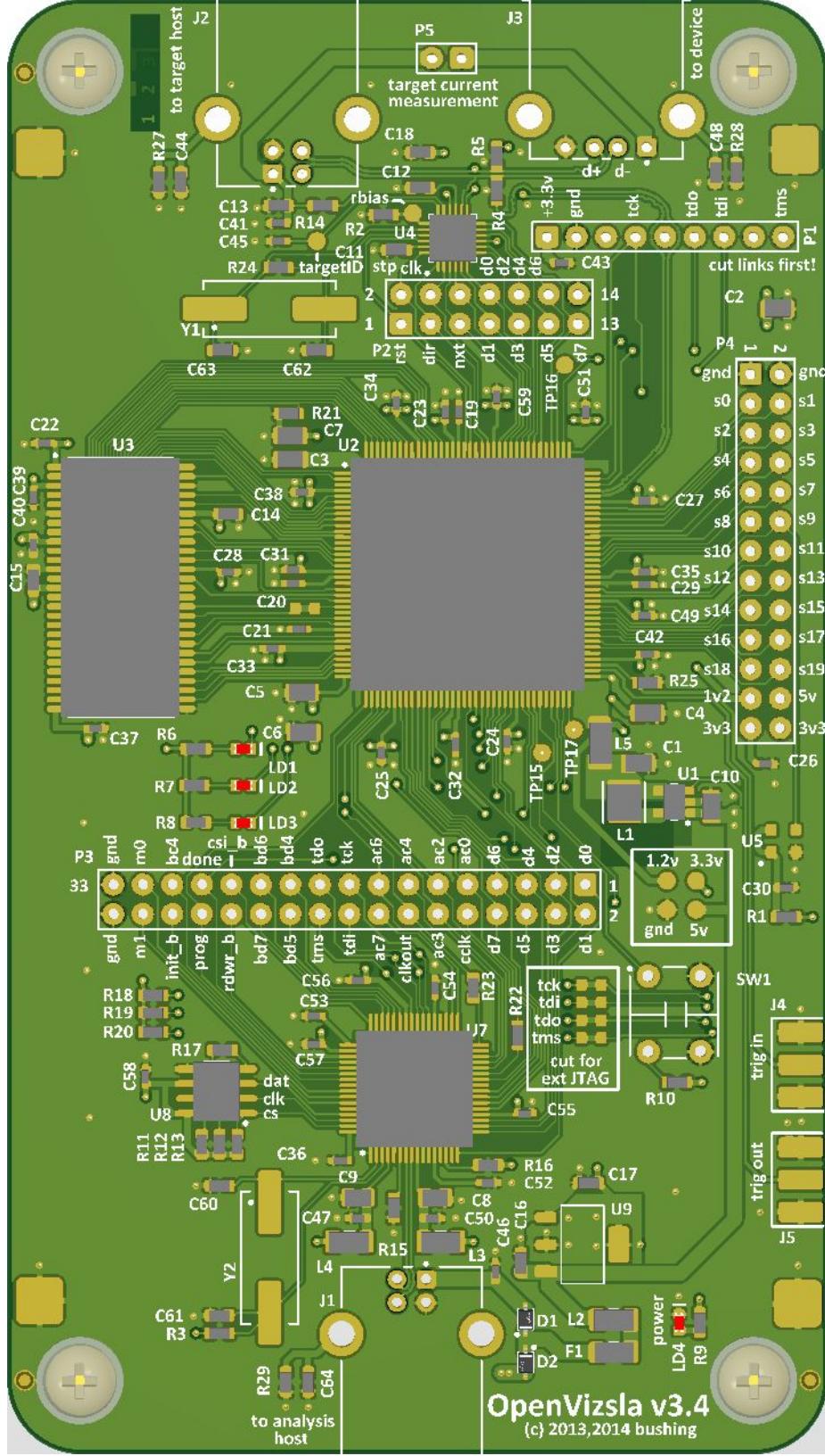
Additional signals used during FIFO mode:  
ACBUS0 (RXF#)  
ACBUS2 (RD#)  
ACBUS3 (WR#)  
ACBUSS (CLKOUT)  
ACBUS6 (OE#)

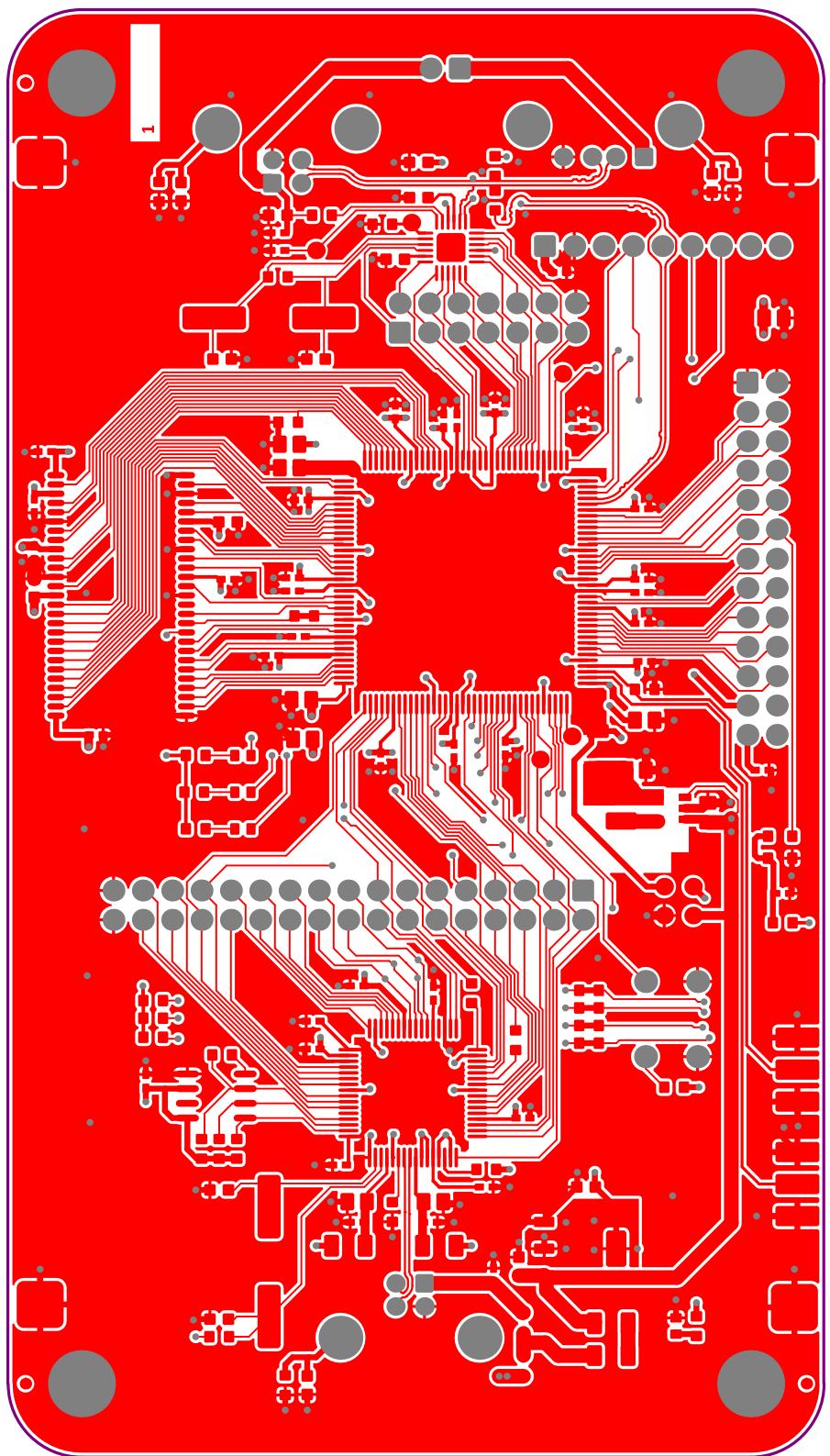
spare I/Os:

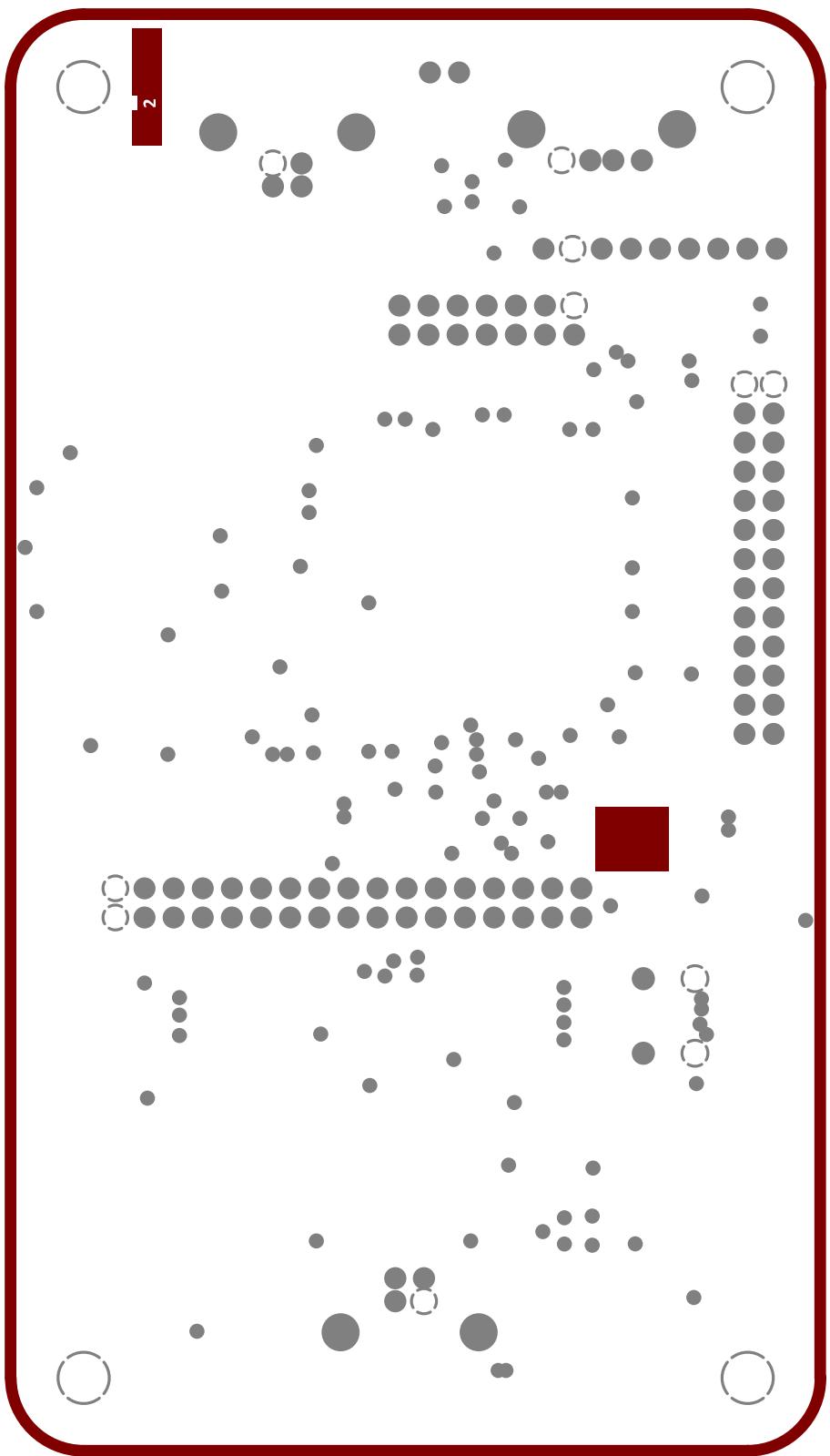


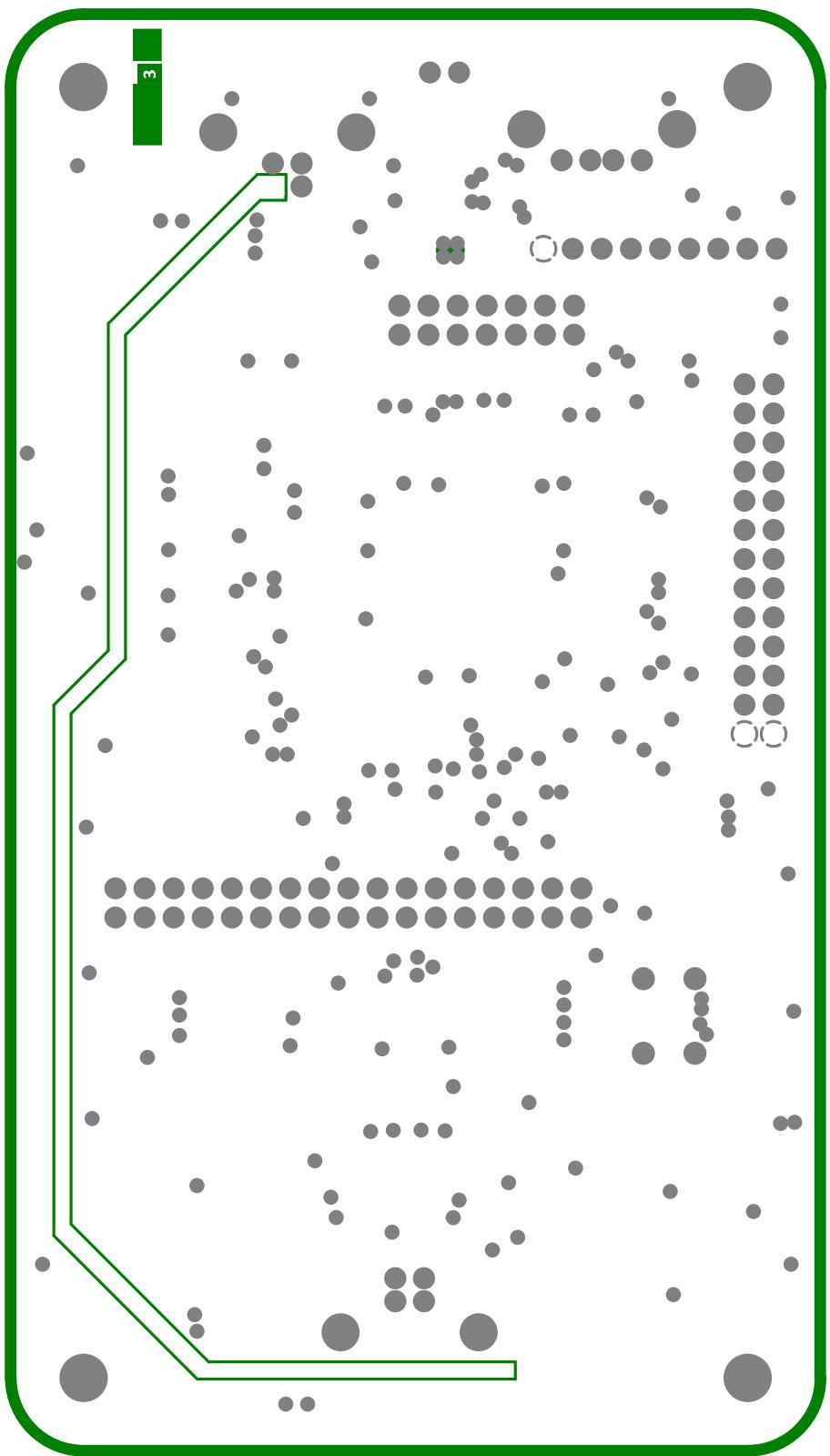
Copyrights: CC-BY-SA 3.0 Patents: Apache 2.0

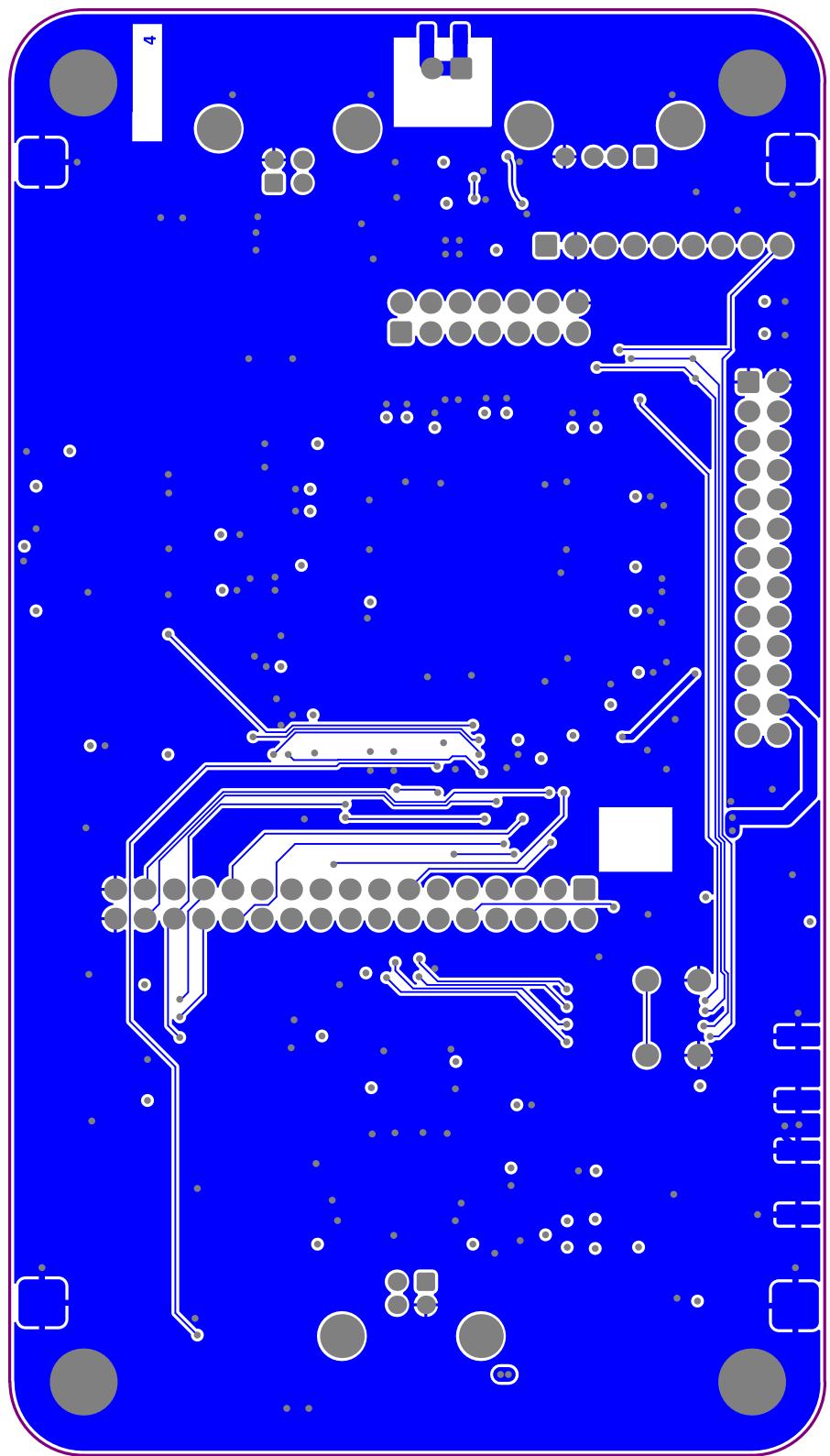
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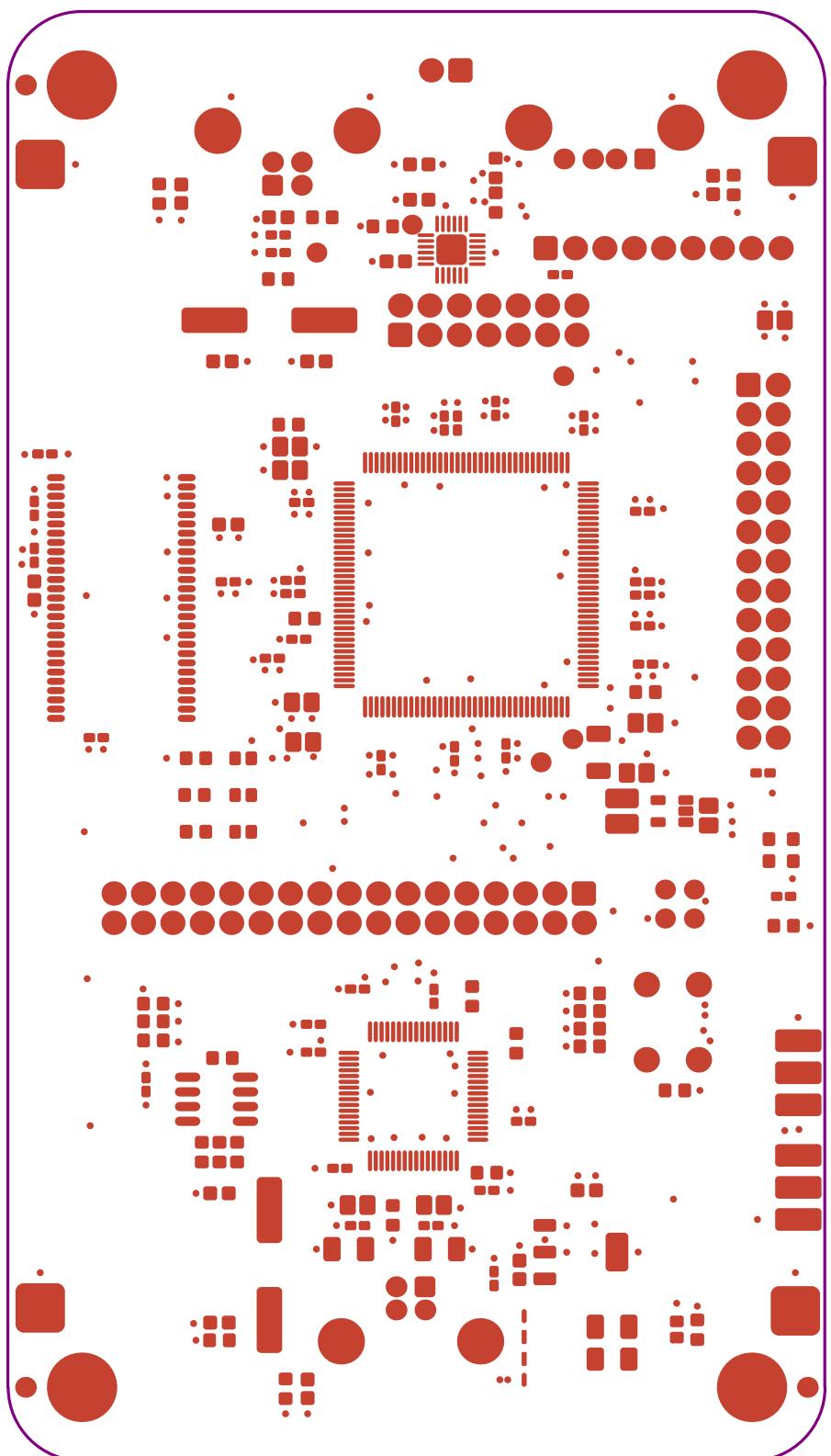


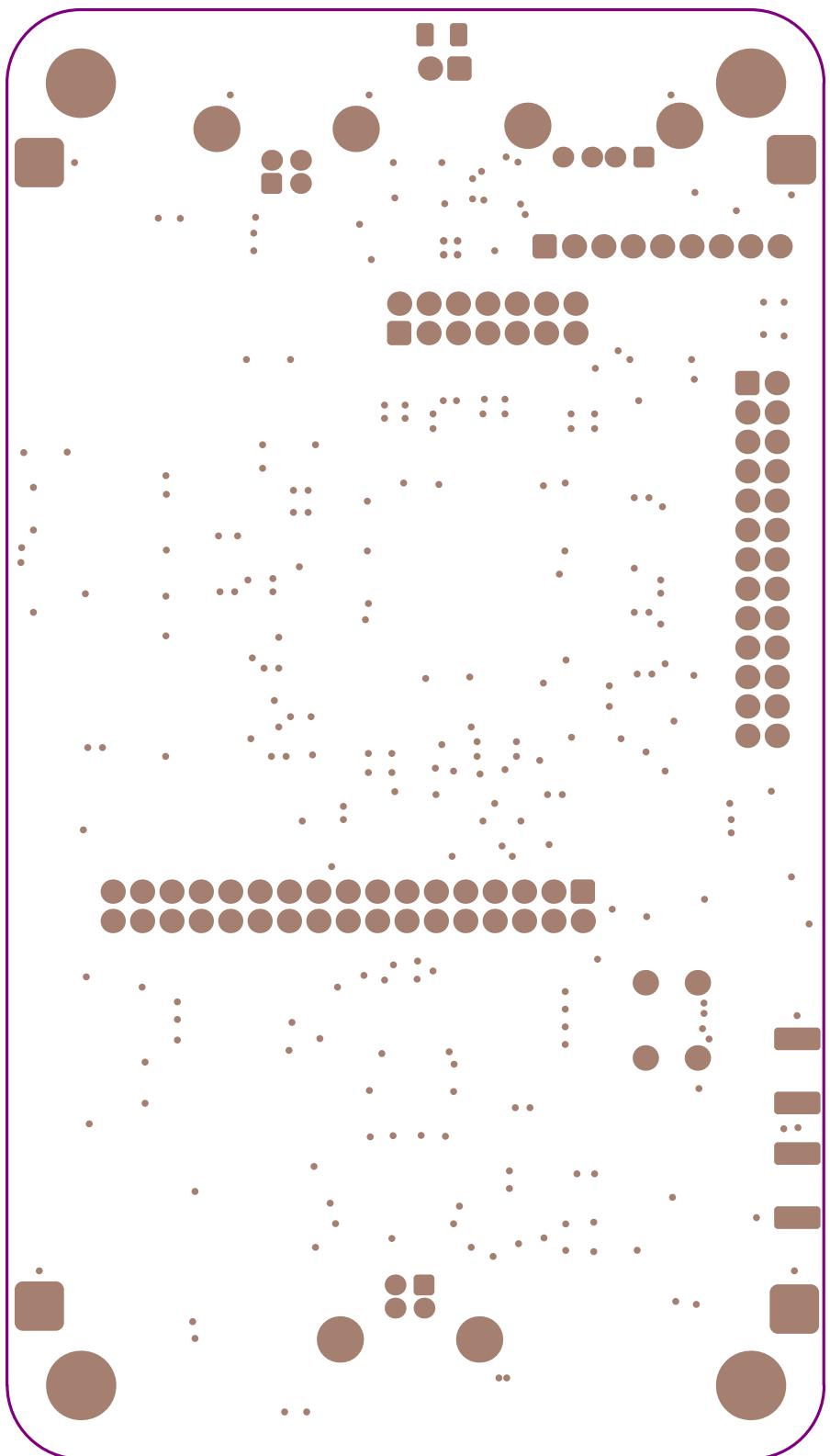


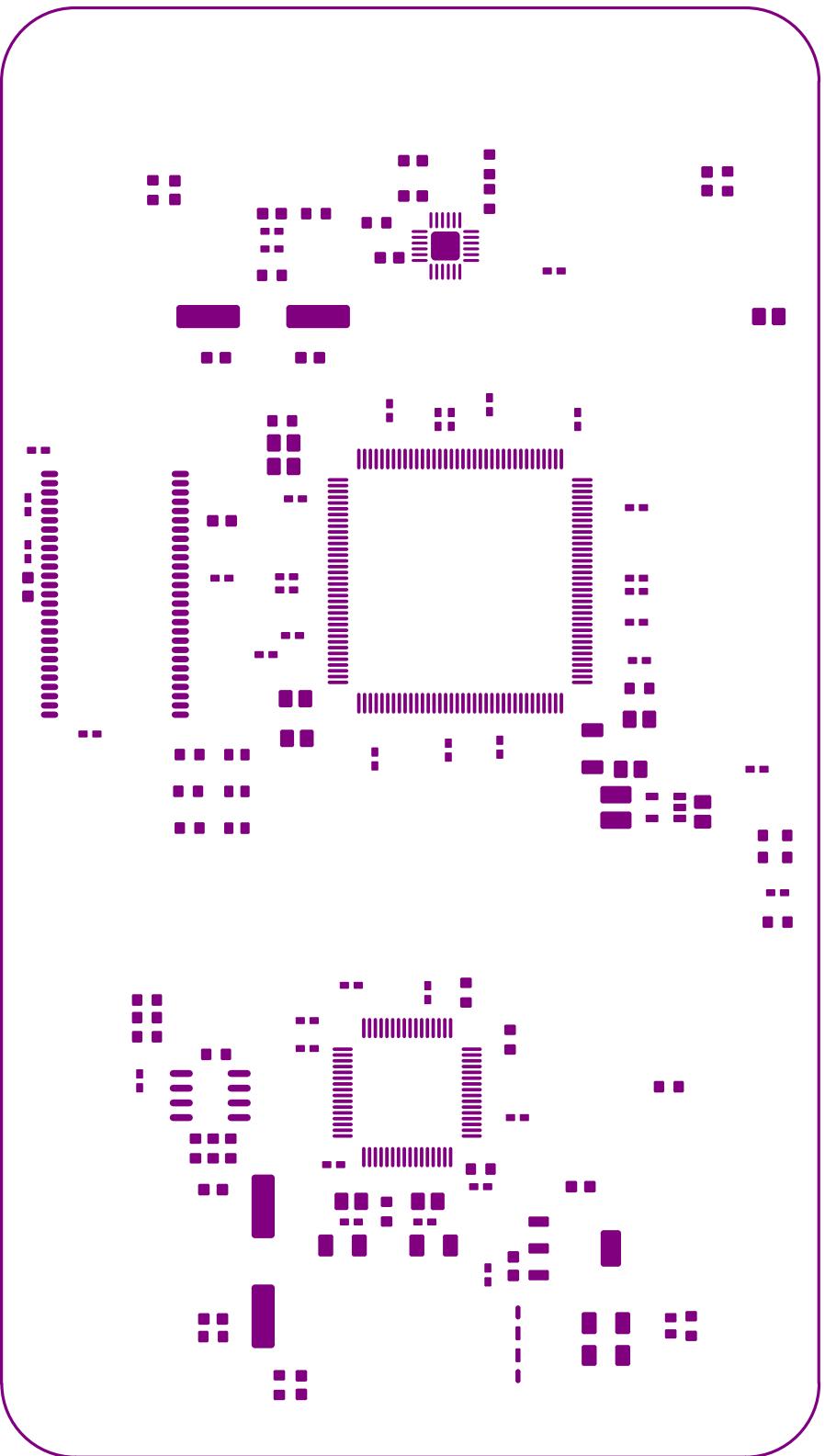


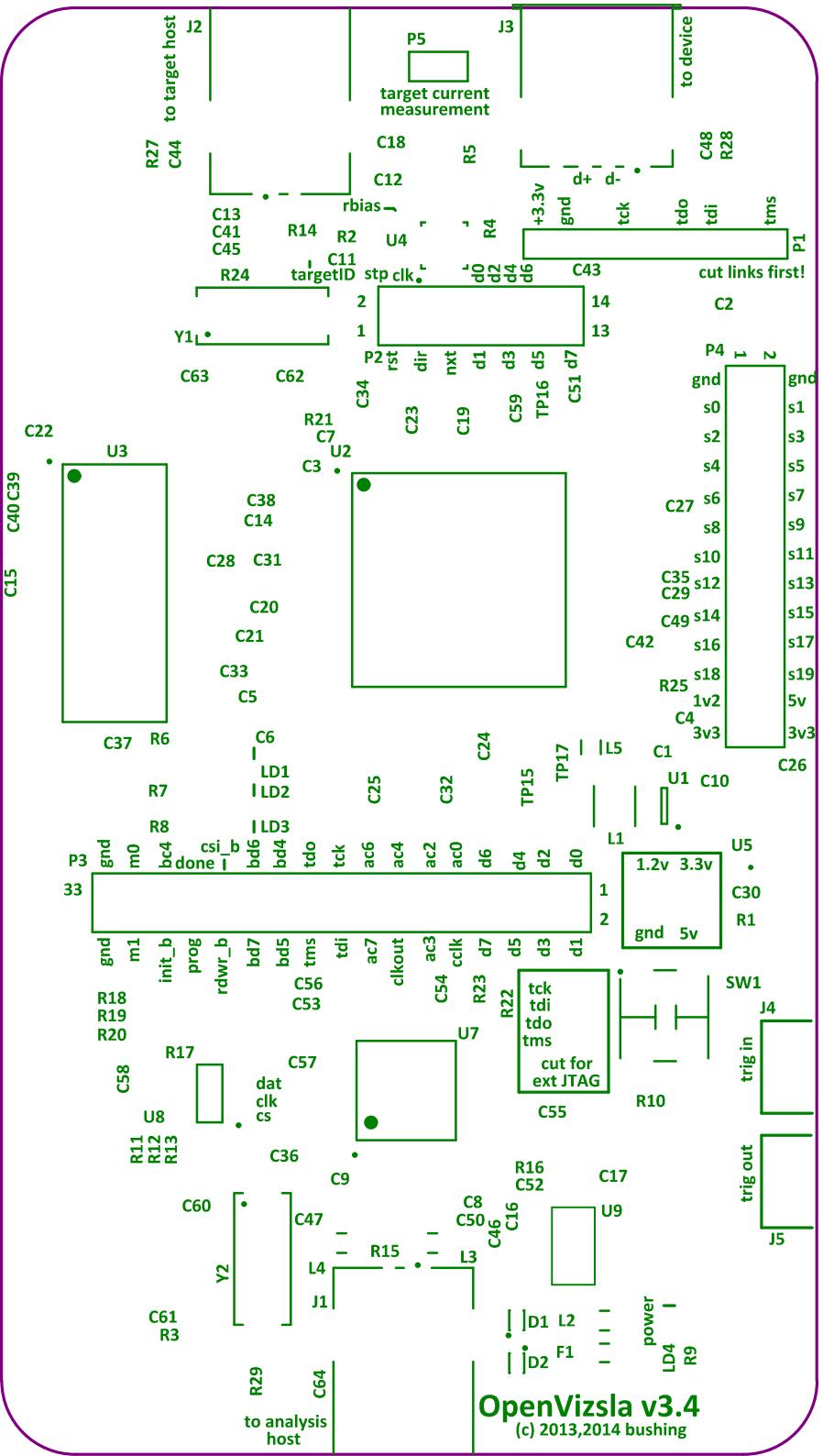












cut links first!  
measure current  
forget current  
D- D+ bugs

cut links first!  
measure current  
forget current  
D- D+ bugs

Vans  
D-  
D+ bugs

R26 -  
cut trace for  
measure current  
forget current  
D- D+ bugs

cut links first!  
measure current  
forget current  
D- D+ bugs

cut links first!  
measure current  
forget current  
D- D+ bugs

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forget current  
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