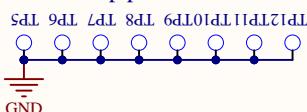
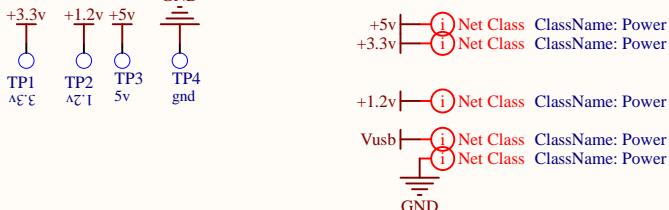


### Ground clip pads



### Power supply test points, top side



+5v  
+3.3v  
Net Class  
ClassName: Power  
Net Class  
ClassName: Power

+1.2v  
Net Class  
ClassName: Power

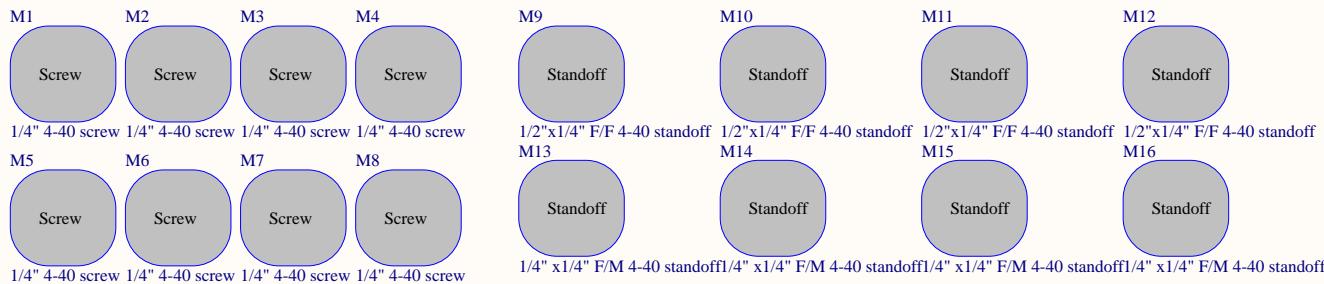
Vusb  
Net Class  
ClassName: Power  
Net Class  
ClassName: Power

GND

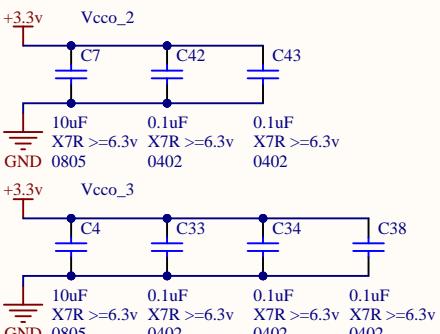
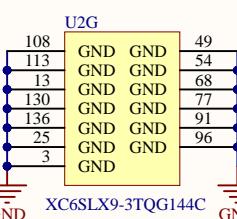
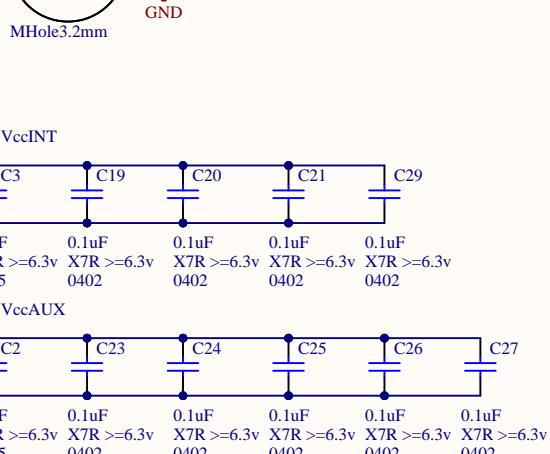
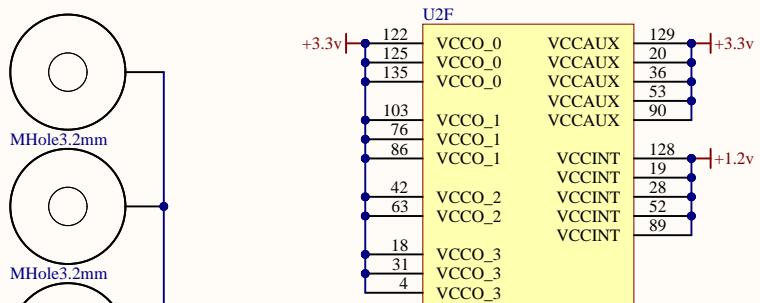
Copyrights: CC-BY-SA 3.0 Patents: Apache 2.0

Title		
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File:	C:\Users\...\power.SchDoc	Drawn By:

A



B



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Title

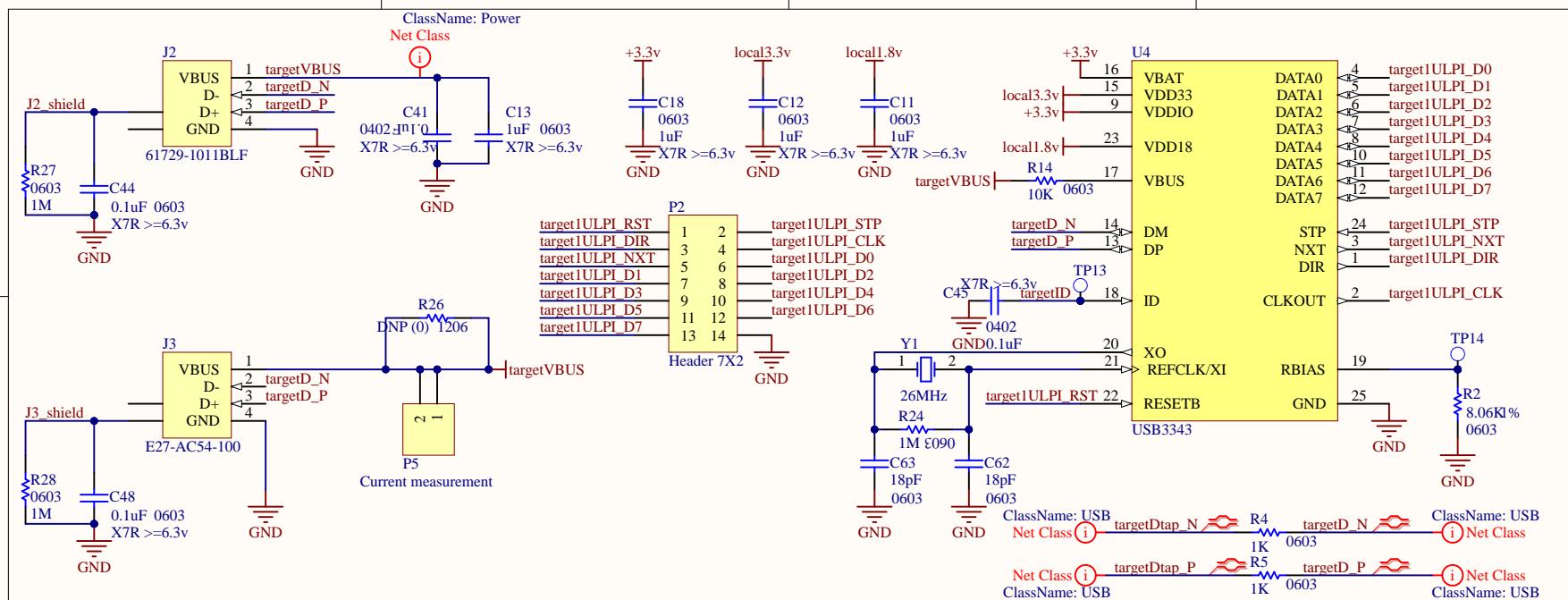
Size

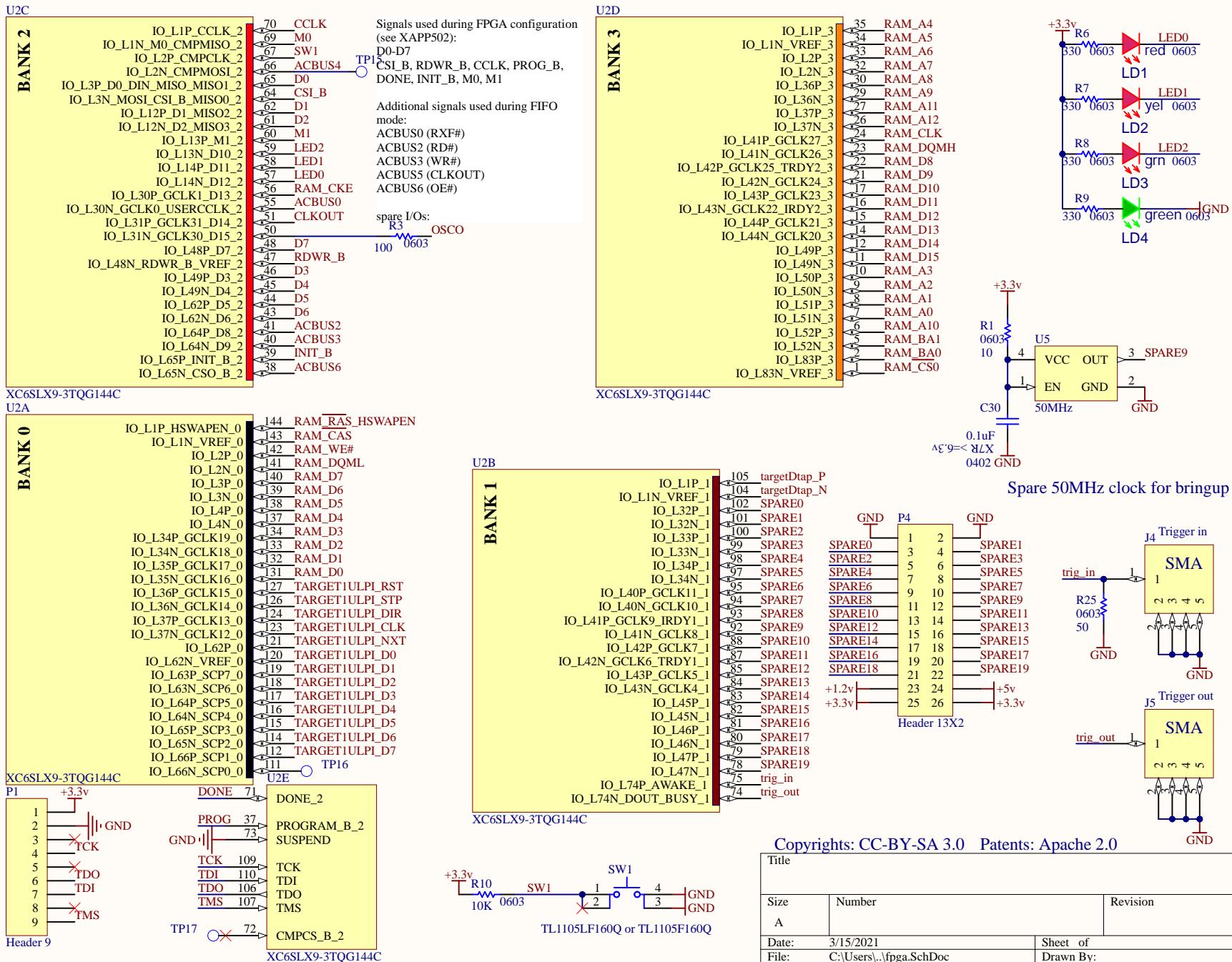
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Number

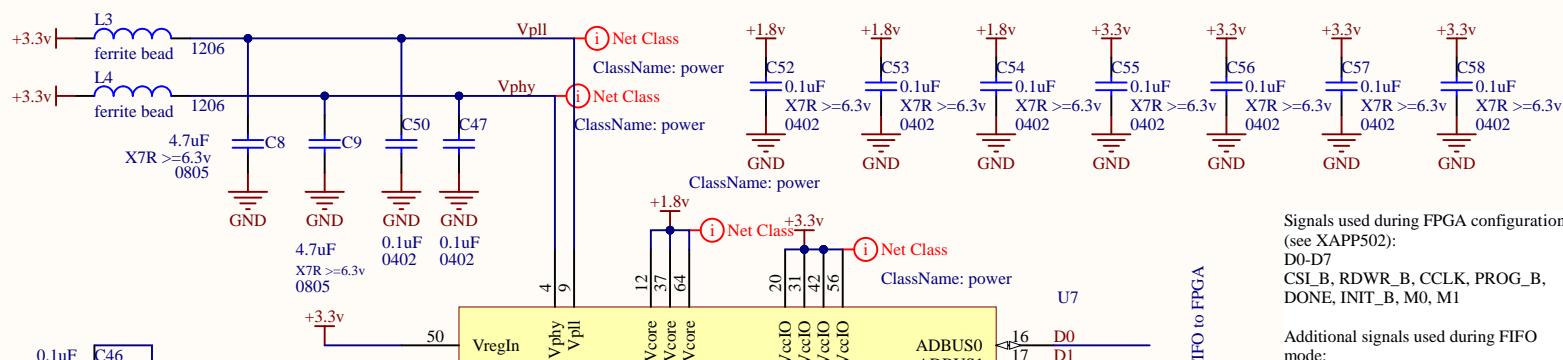
Revision

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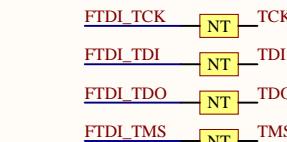
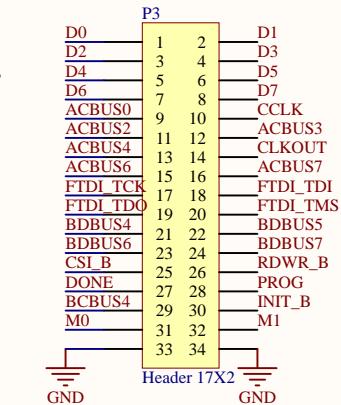
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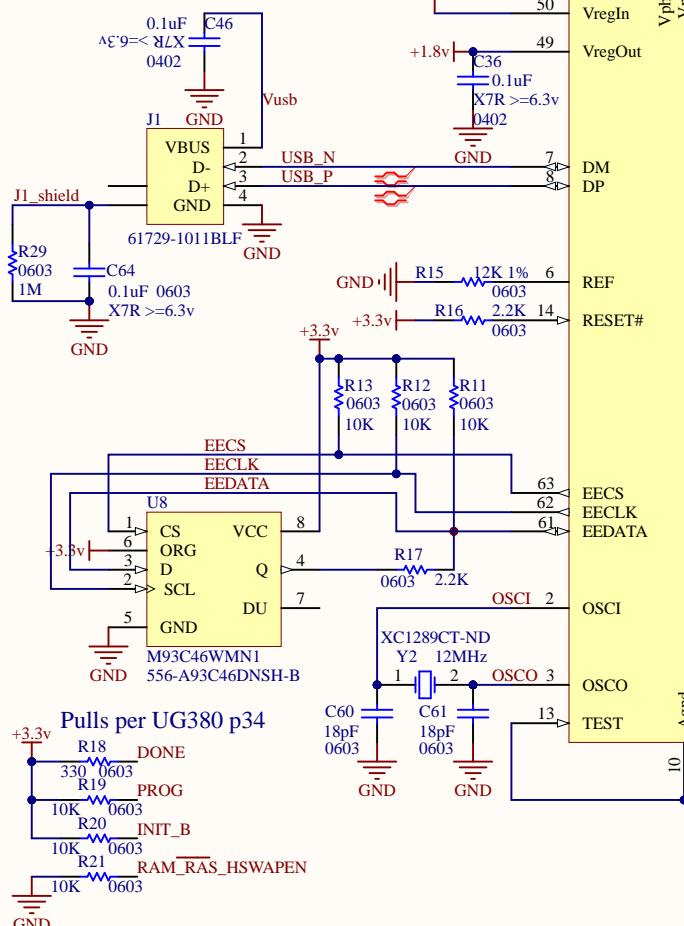
Signals used during FPGA configuration (see XAPP502):  
D0-D7  
CSI\_B, RDWR\_B, CCLK, PROG\_B,  
DONE, INIT\_B, M0, M1

Additional signals used during FIFO mode:  
ACBUS0 (RXF#)  
ACBUS2 (RD#)  
ACBUS3 (WR#)  
ACBUSS (CLKOUT)  
ACBUS6 (OE#)

spare I/Os:



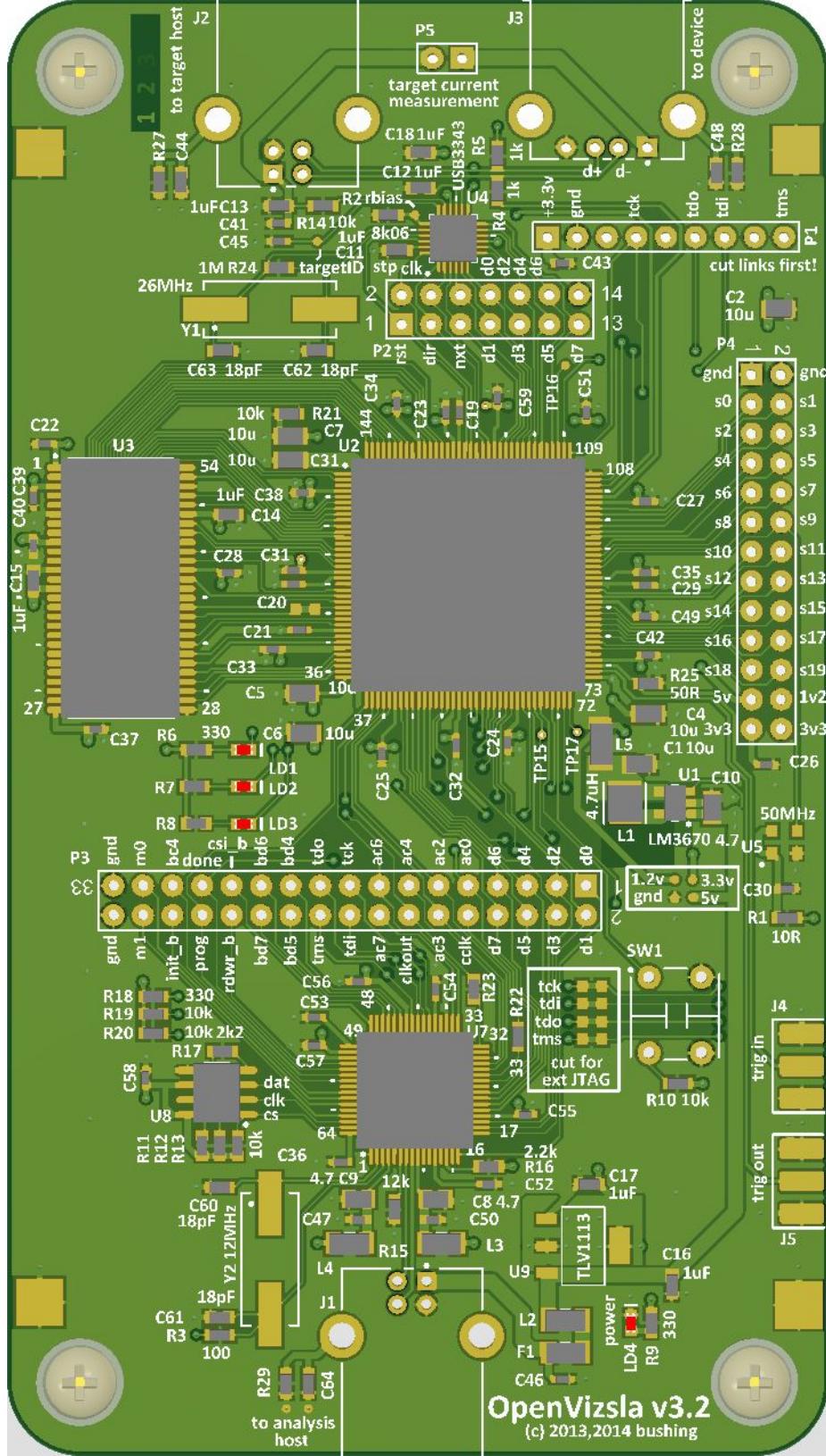
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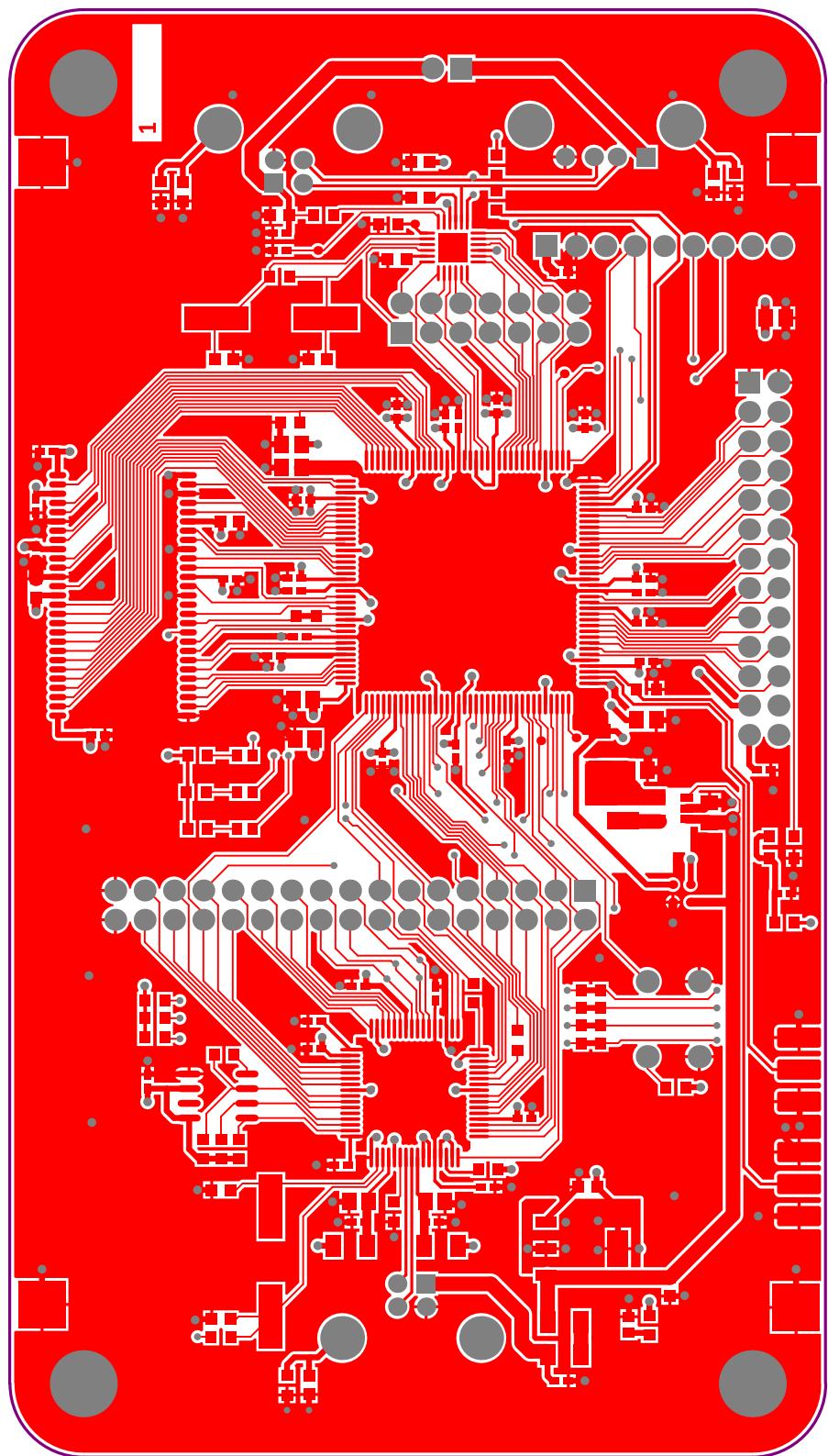


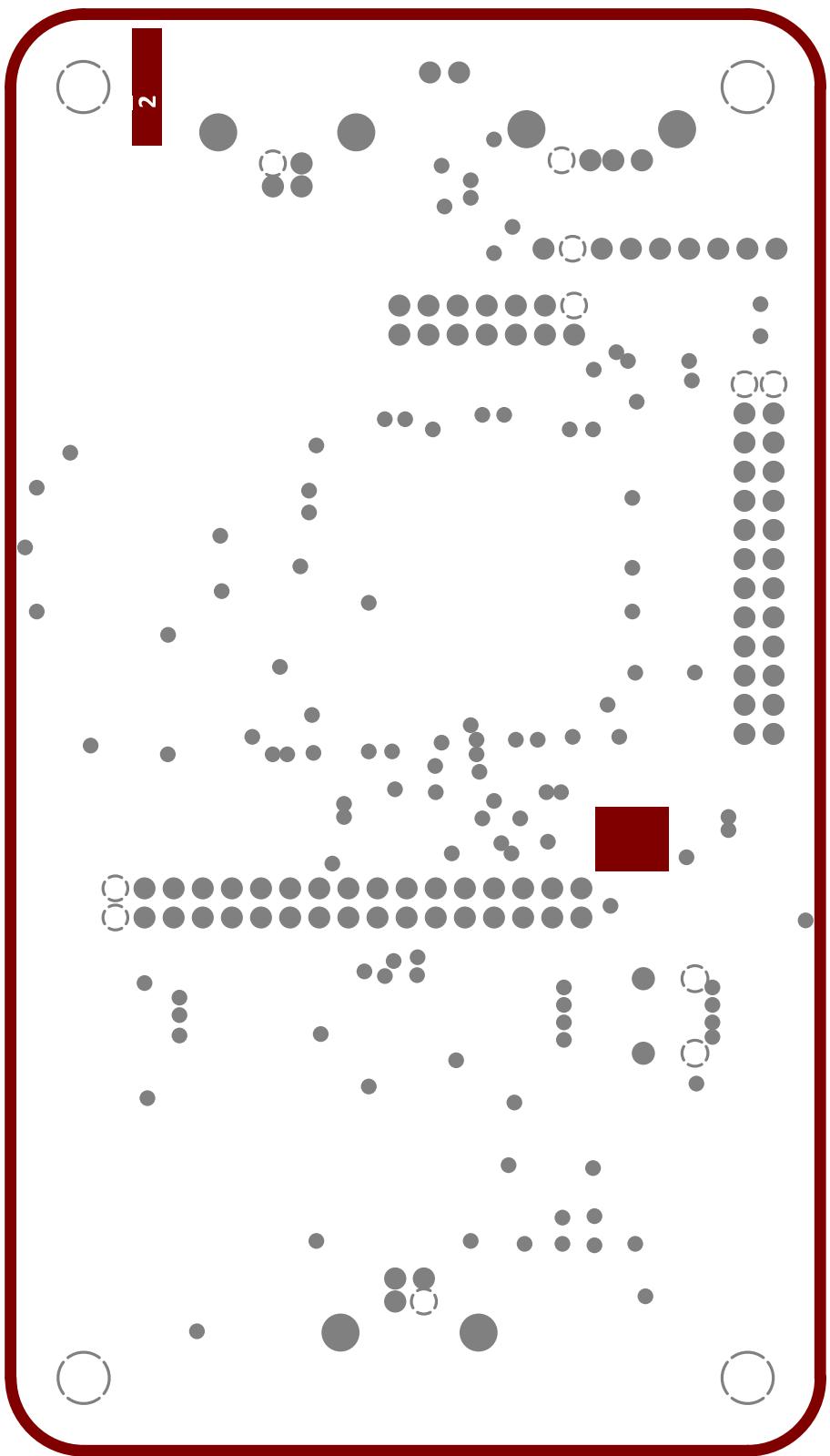
FT2232H

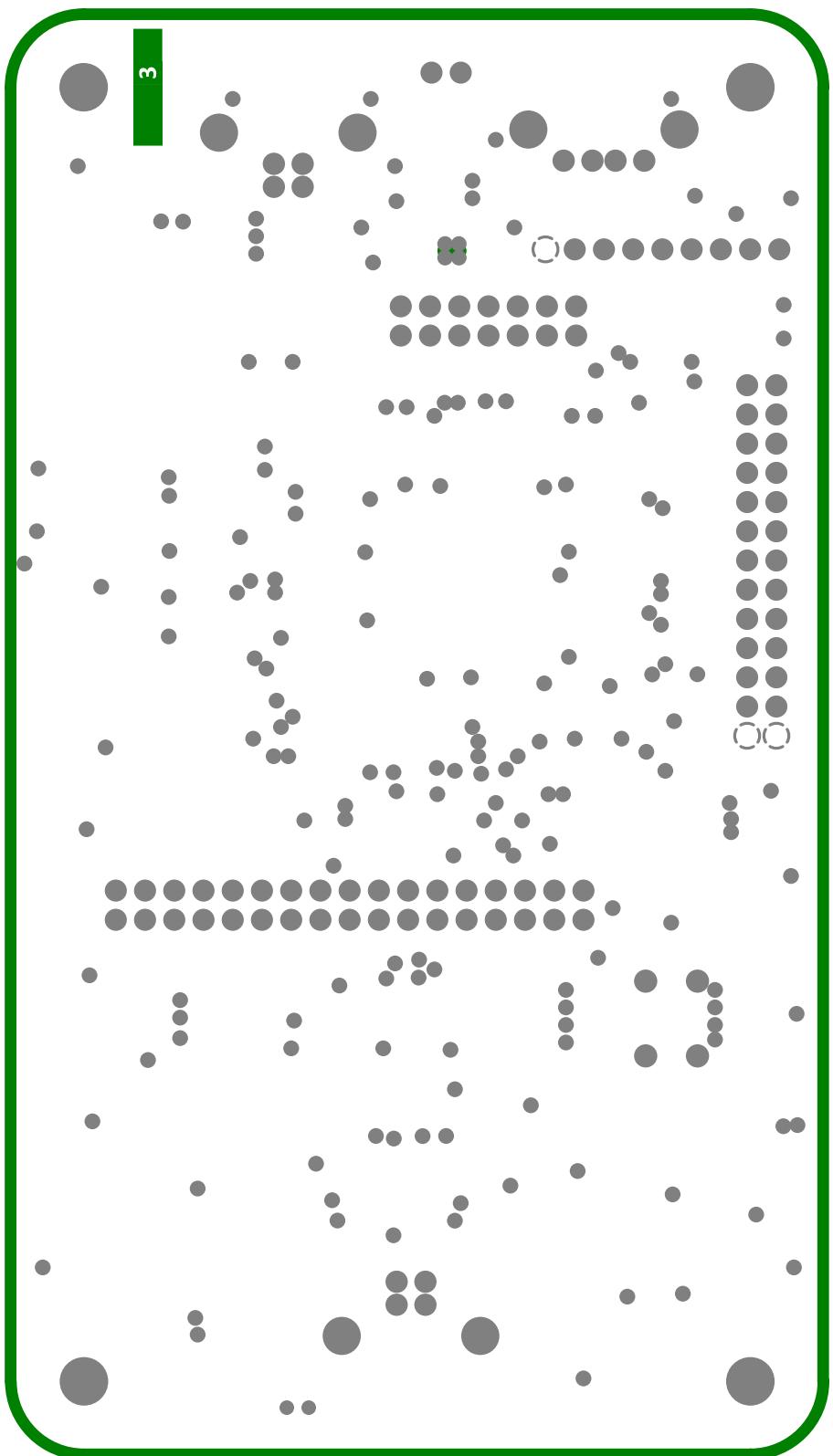
Copyrights: CC-BY-SA 3.0 Patents: Apache 2.0

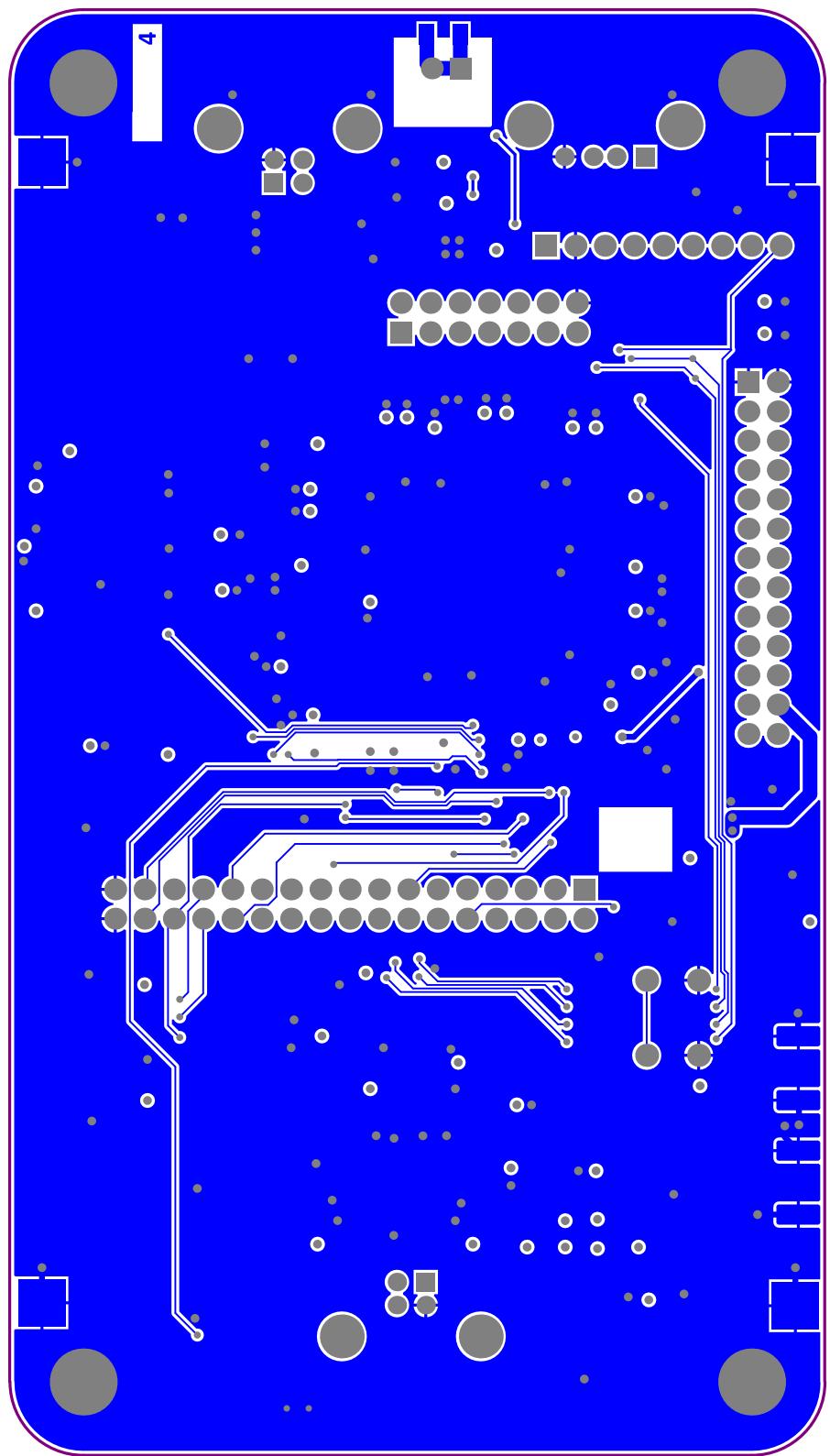
Title		Revision
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A		
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File:	C:\Users\...\usb.SchDoc	Drawn By:

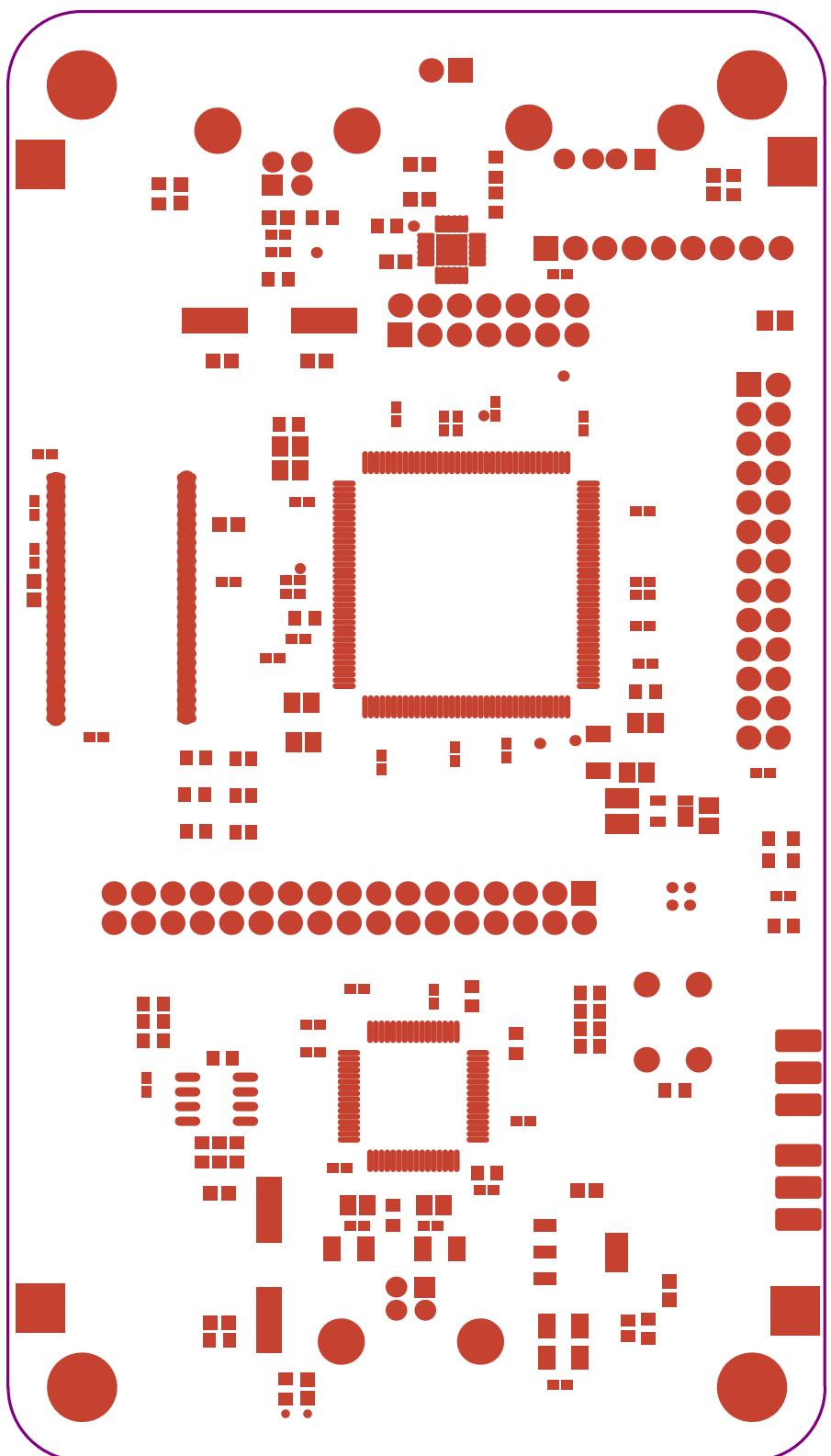


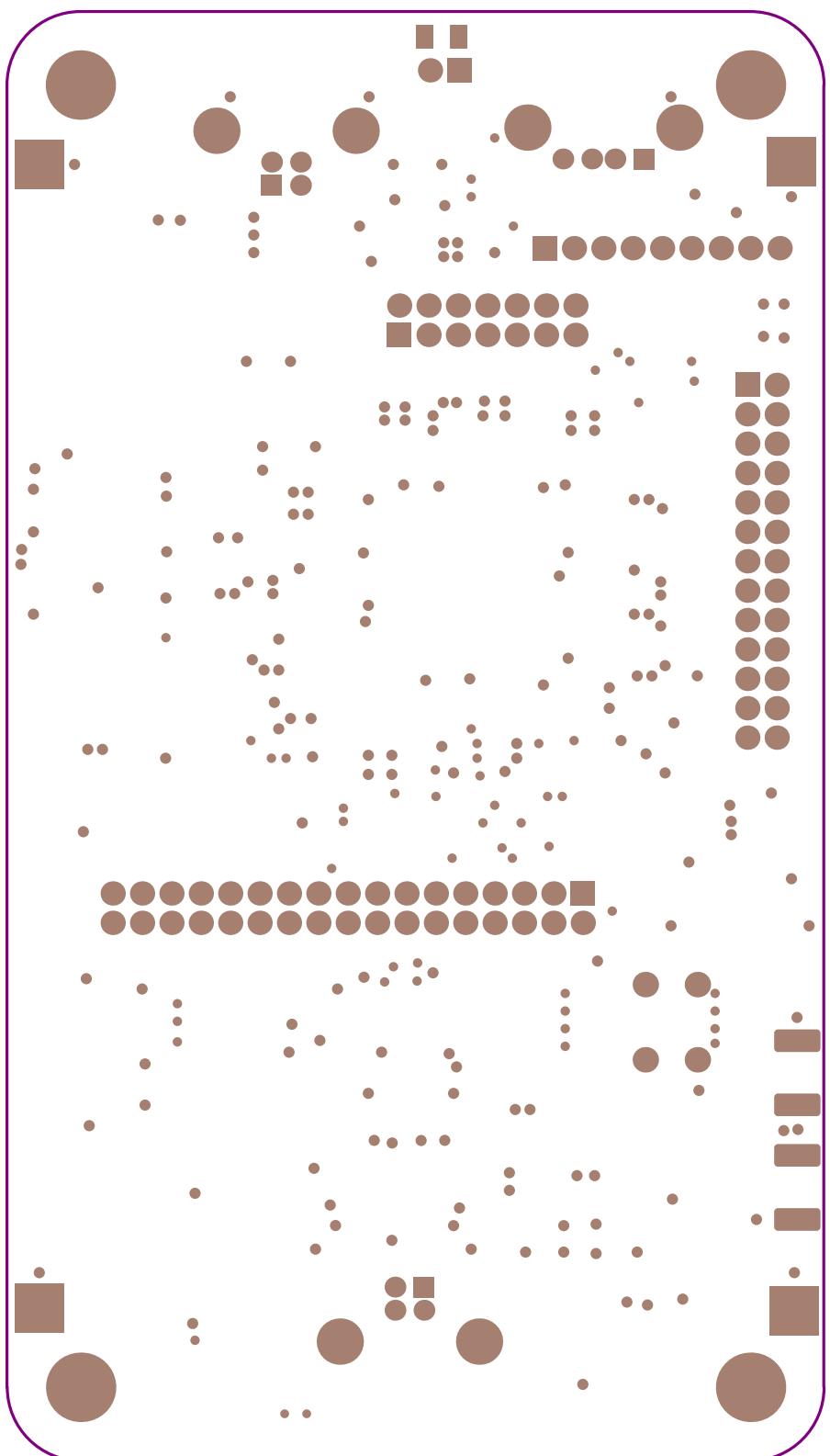


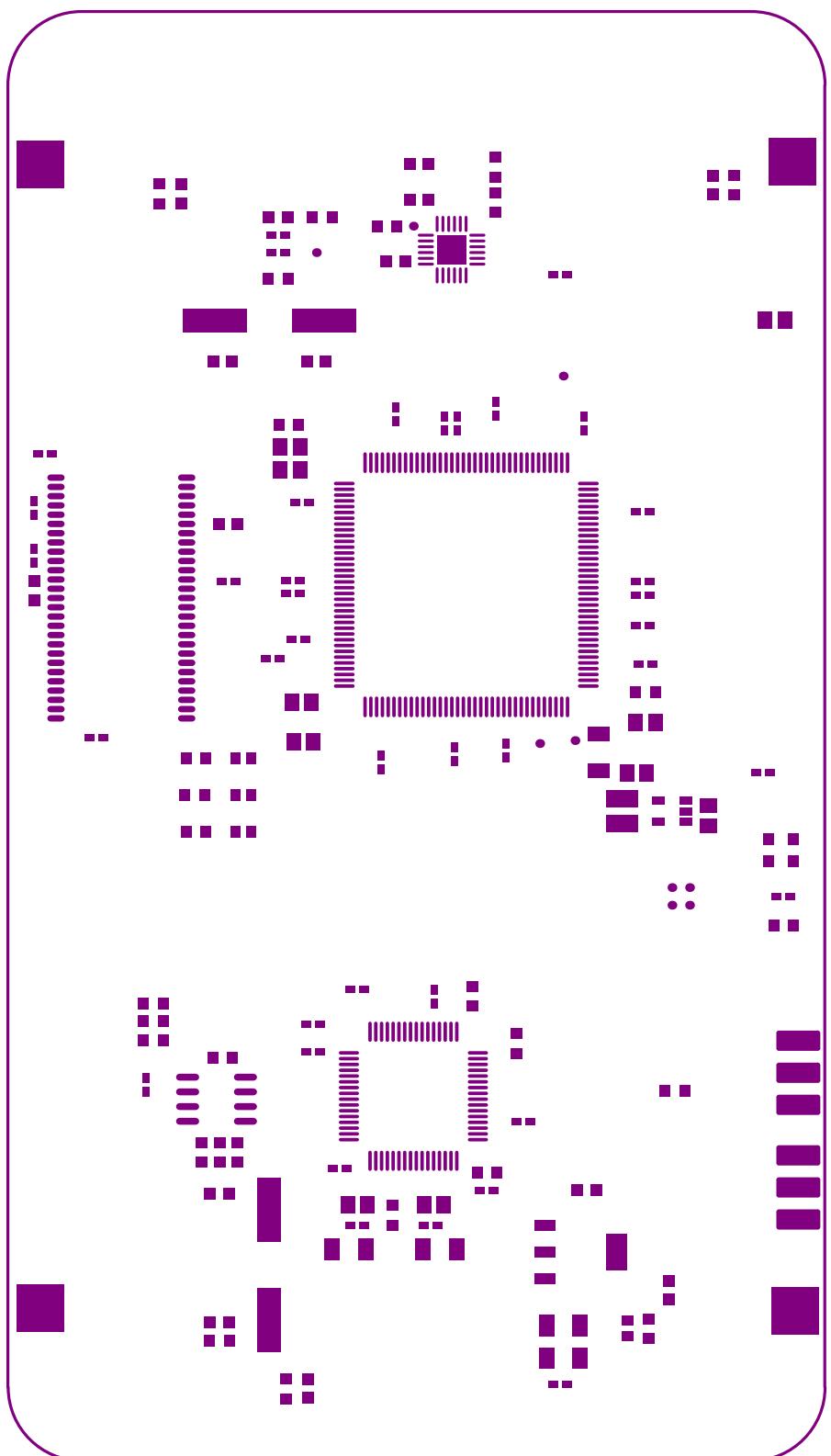


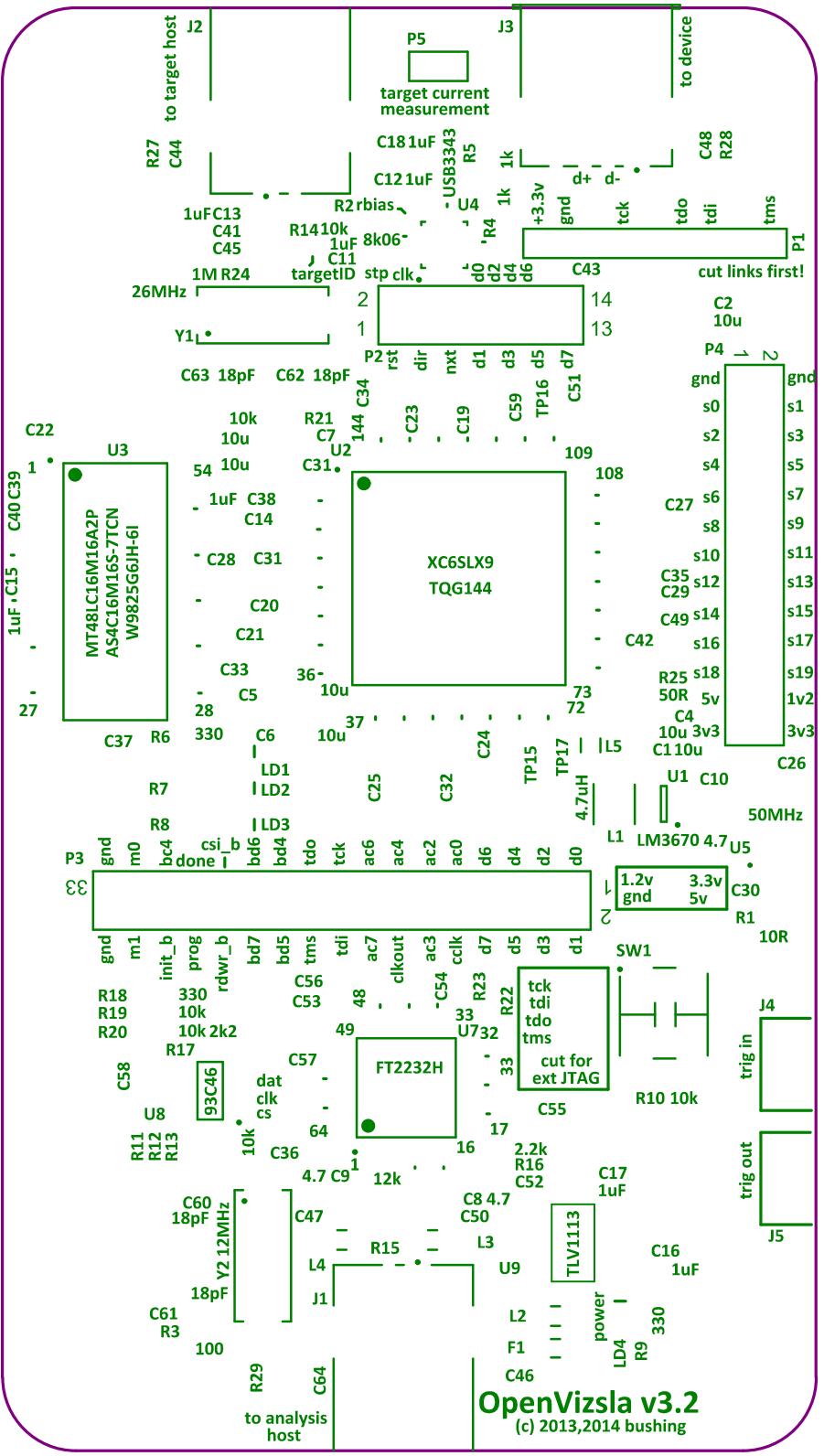












**OpenVizsla v3.2**  
(c) 2013,2014 bushing

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