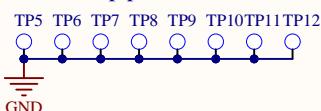
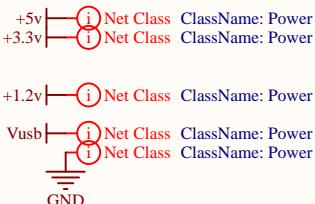
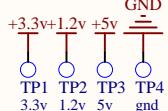


#### Ground clip pads



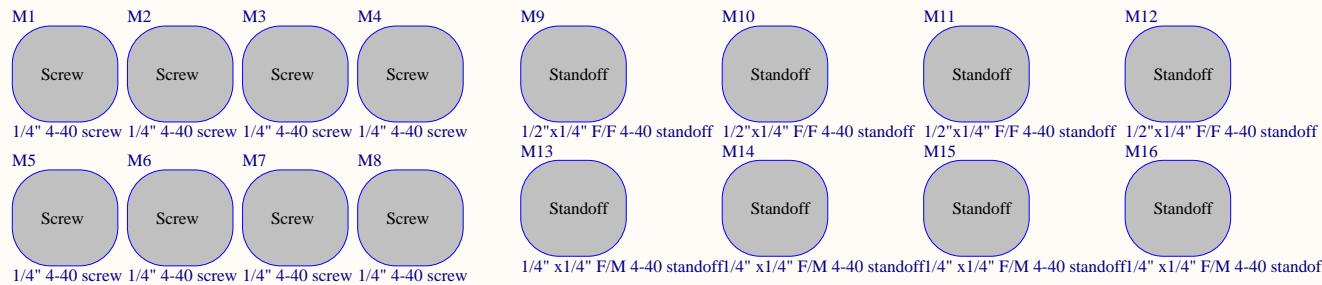
#### Power supply test points, top side



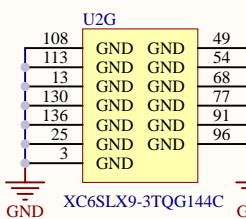
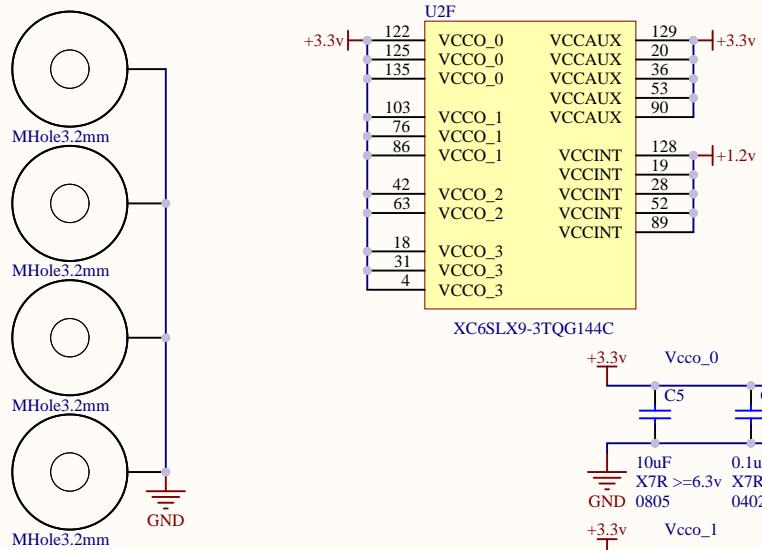
**Copyrights: CC-BY-SA 3.0 Patents: Apache 2.0**

Title		
Size	Number	Revision
A		
Date:	4/14/2021	Sheet of
File:	C:\Users\...\power.SchDoc	Drawn By:

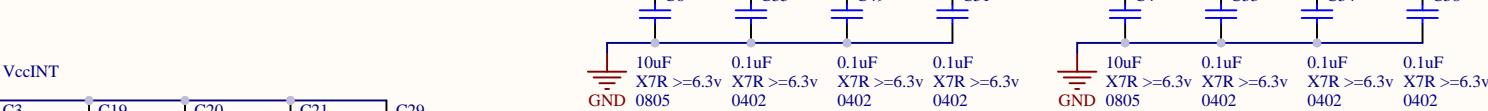
A



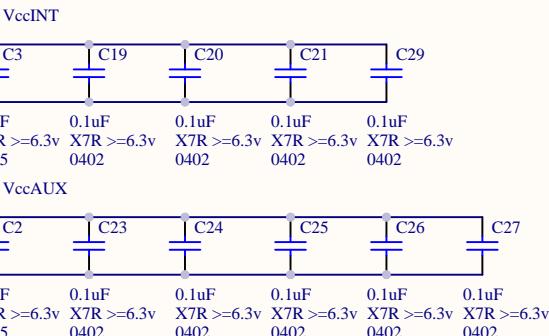
B



C

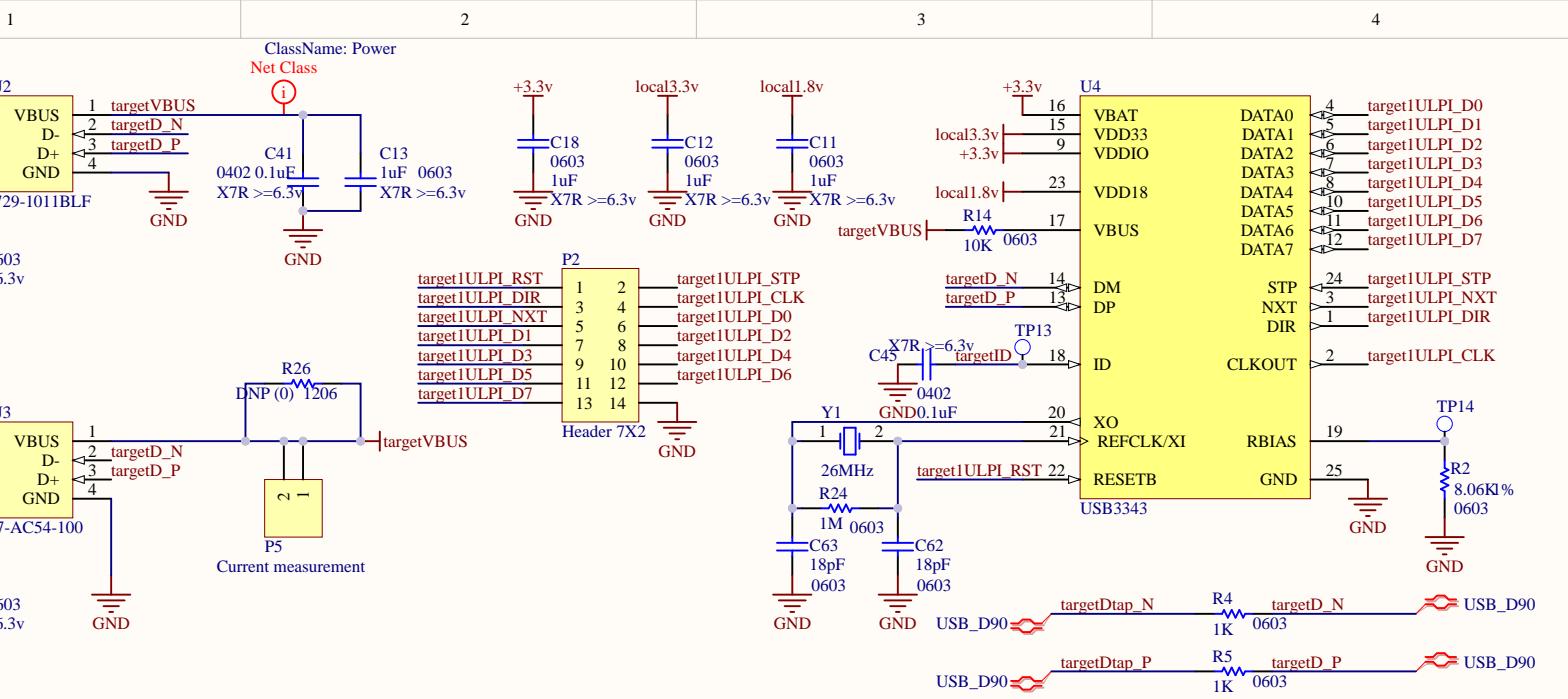


D

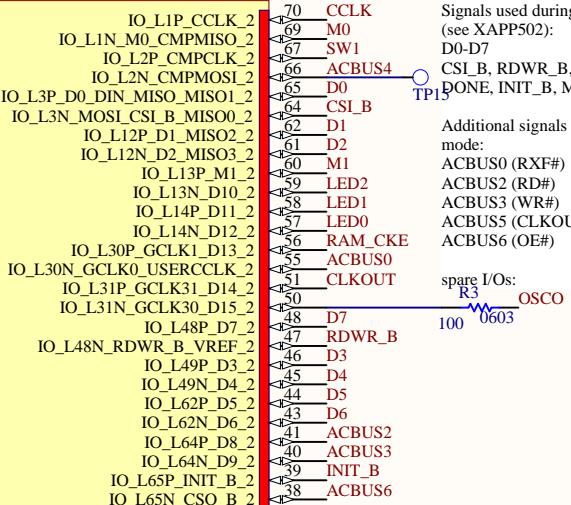


Copyrights: CC-BY-SA 3.0 Patents: Apache 2.0

Title		
Size	Number	Revision
A		
Date:	4/14/2021	Sheet 2 of
File:	C:\Users...\FPGA power v3.SchDoc	Drawn By:

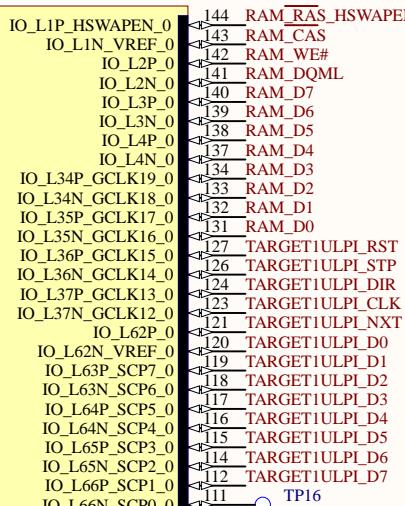


U2C

**BANK 2**

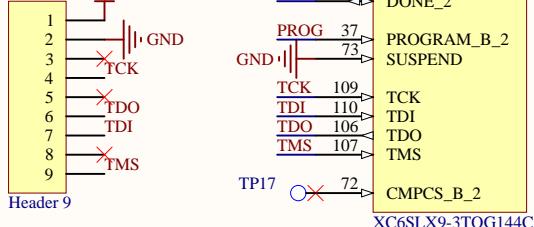
XC6SLX9-3TQG144C

U2A



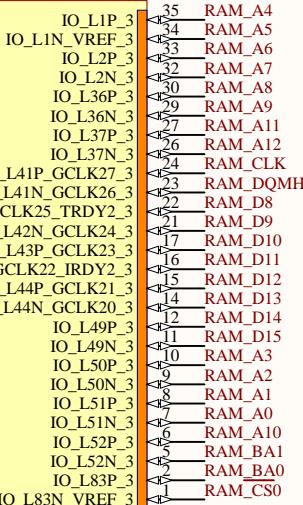
XC6SLX9-3TQG144C

P1

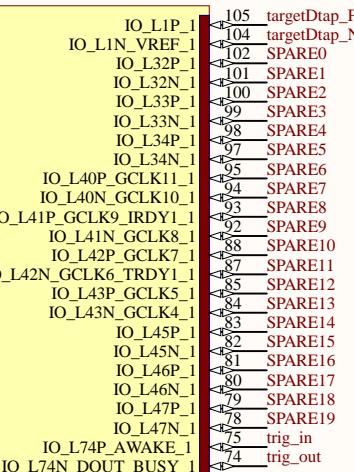


Header 9

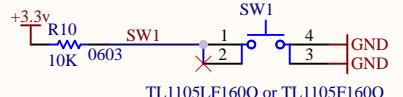
U2D



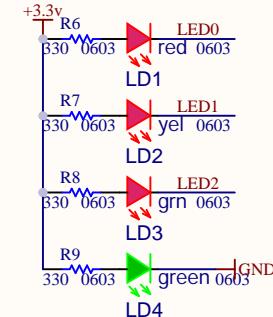
XC6SLX9-3TQG144C

**BANK 1**

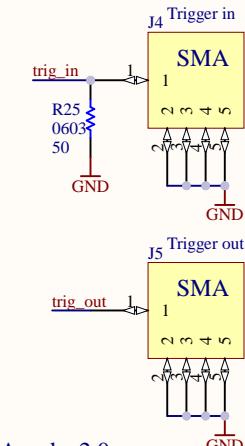
XC6SLX9-3TQG144C



TL1105LF160Q or TL1105F160Q



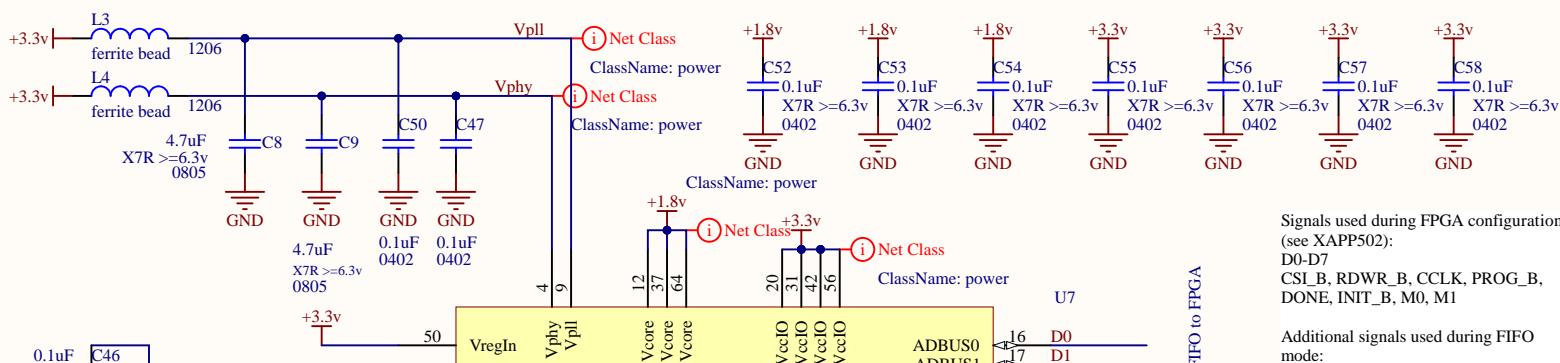
Spare 50MHz clock for bringup



Copyrights: CC-BY-SA 3.0 Patents: Apache 2.0

Title		Revision
Size	Number	
A		
Date:	4/14/2021	Sheet of
File:	C:\Users...\fpga.SchDoc	Drawn By:

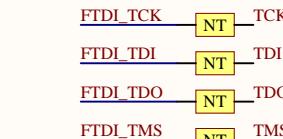
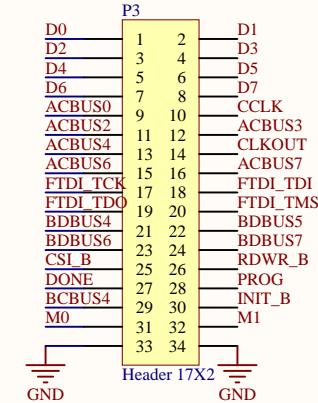
A



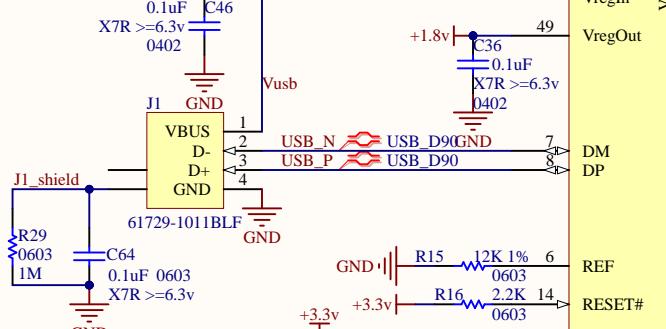
Signals used during FPGA configuration (see XAPP502):  
D0-D7  
CSI\_B, RDWR\_B, CCLK, PROG\_B,  
DONE, INIT\_B, M0, M1

Additional signals used during FIFO mode:  
ACBUS0 (RXF#)  
ACBUS2 (RD#)  
ACBUS3 (WR#)  
ACBUSS (CLKOUT)  
ACBUS6 (OE#)

spare I/Os:

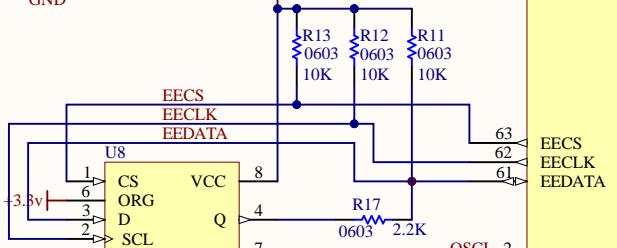


B

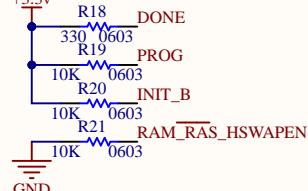


FT2232H

C



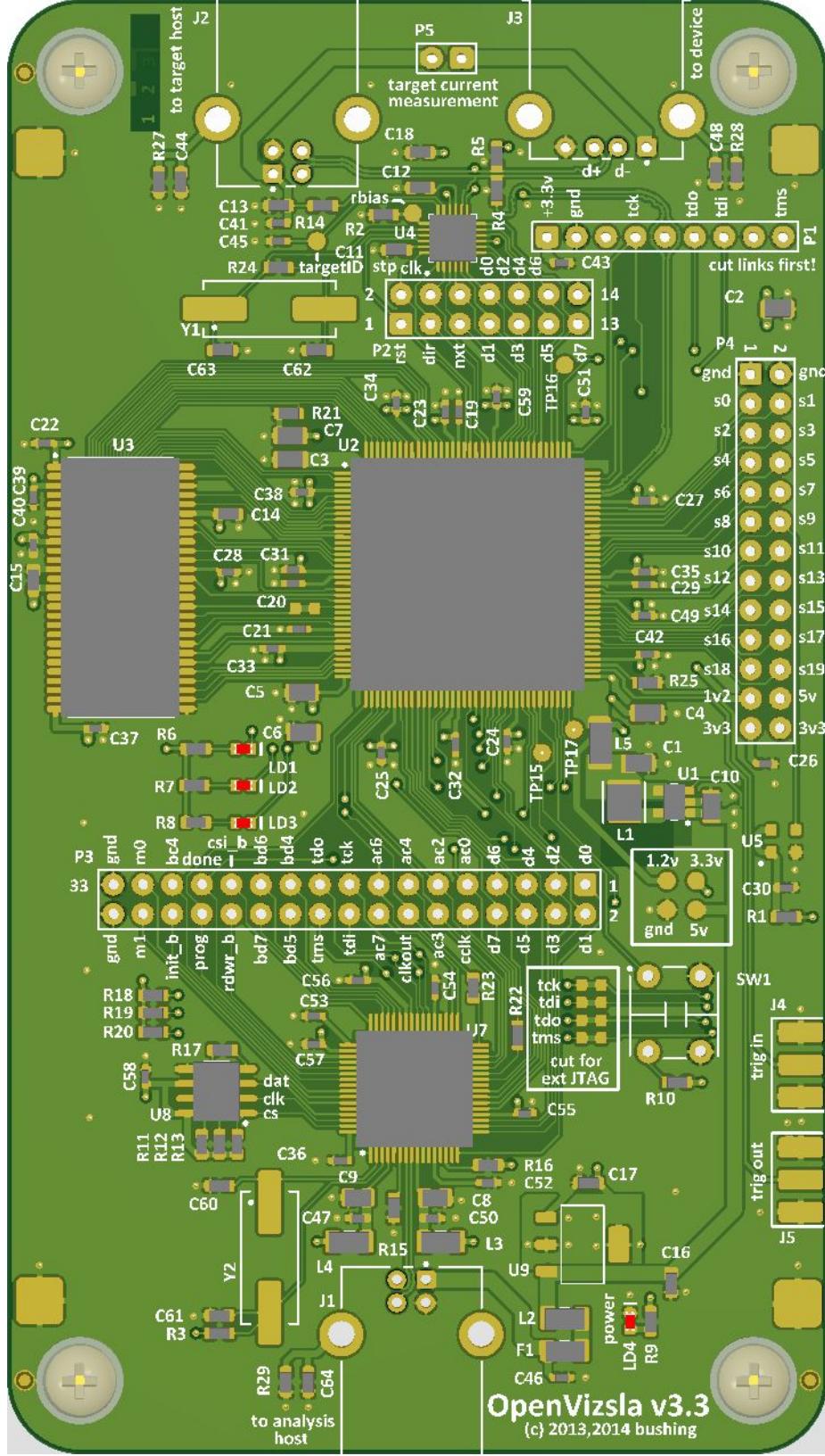
Pulls per UG380 p34



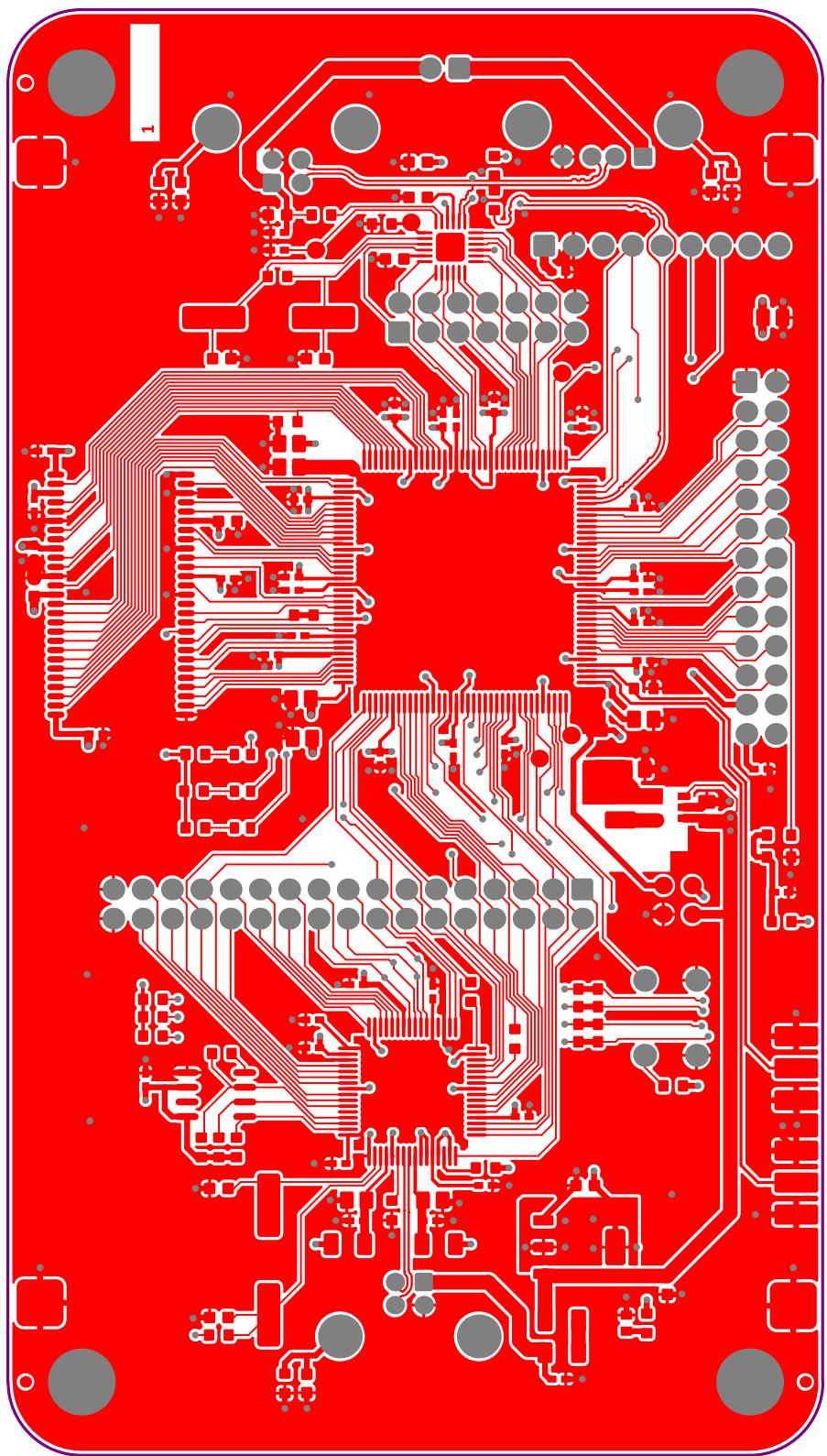
D

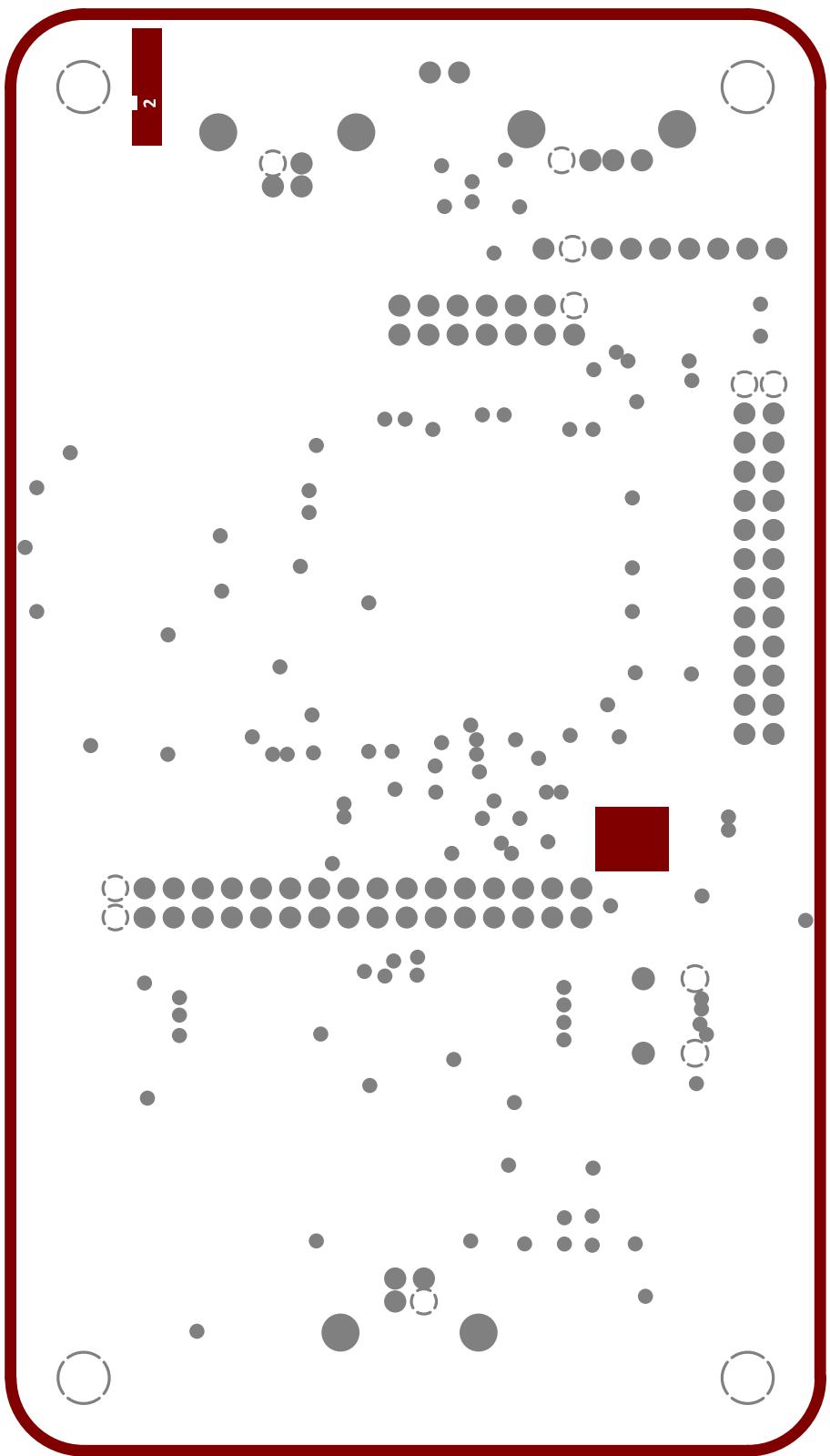
Copyrights: CC-BY-SA 3.0 Patents: Apache 2.0

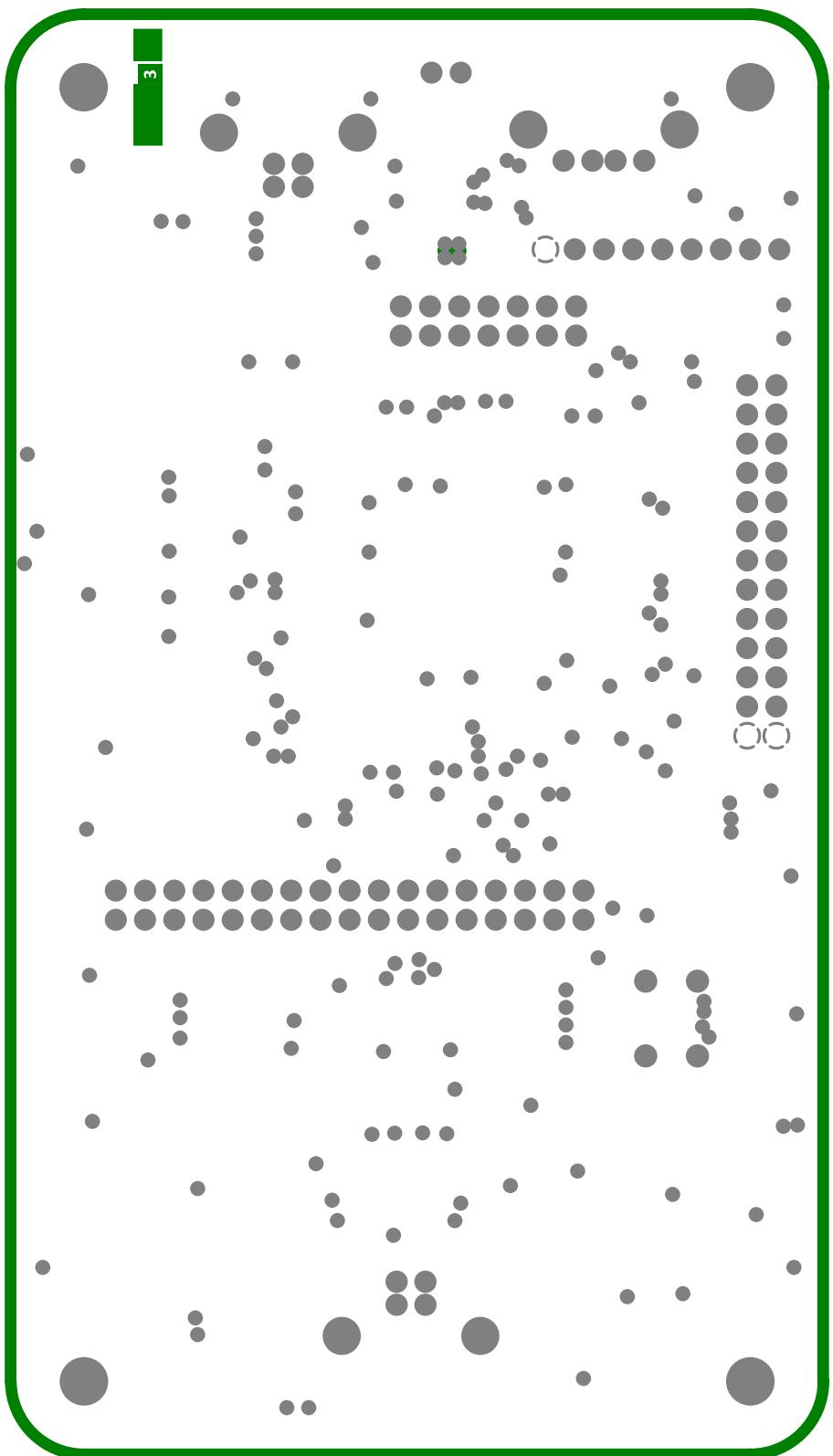
Title		Revision
Size	Number	
A		
Date:	4/14/2021	Sheet of
File:	C:\Users\...\usb.SchDoc	Drawn By:

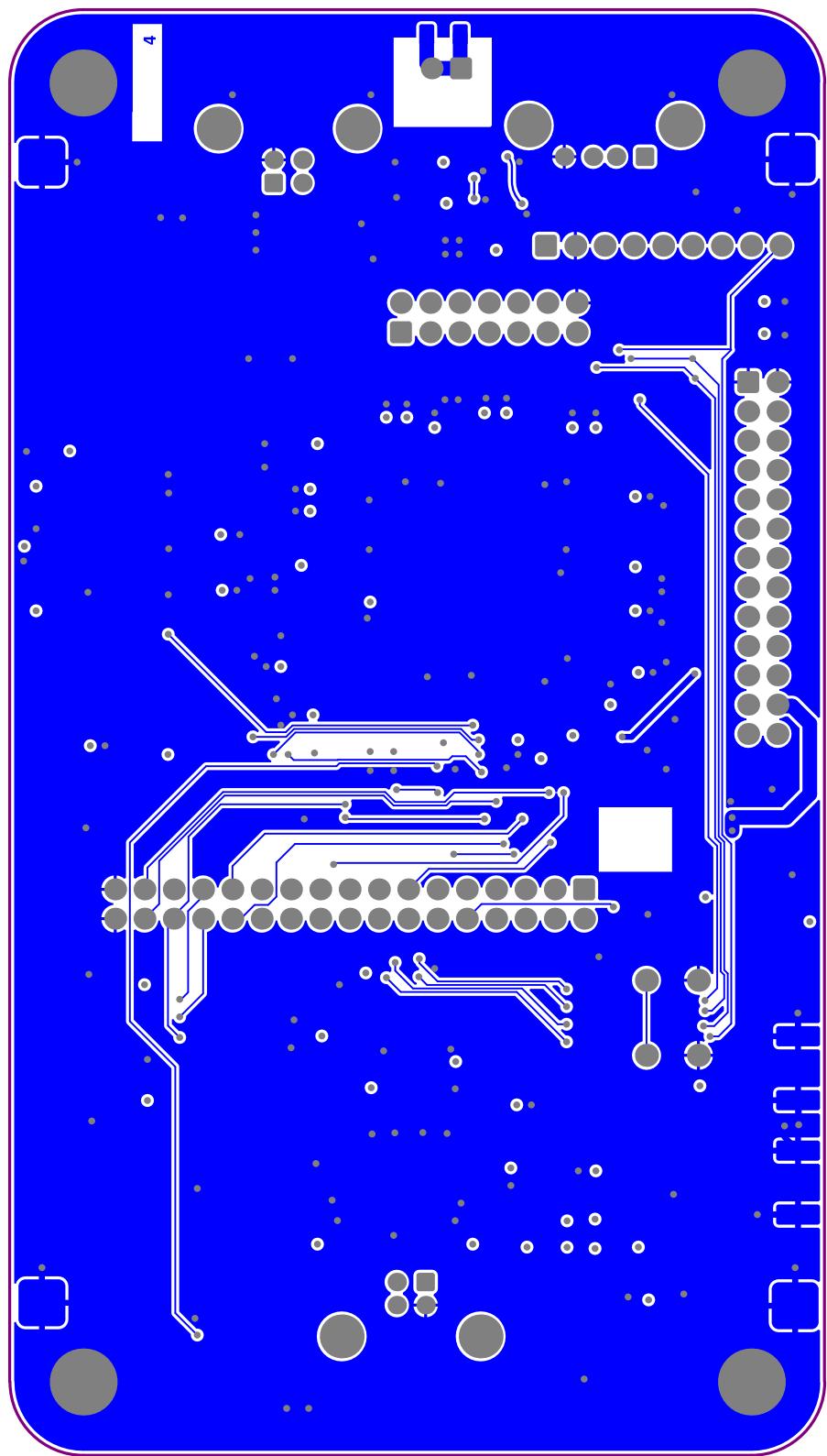


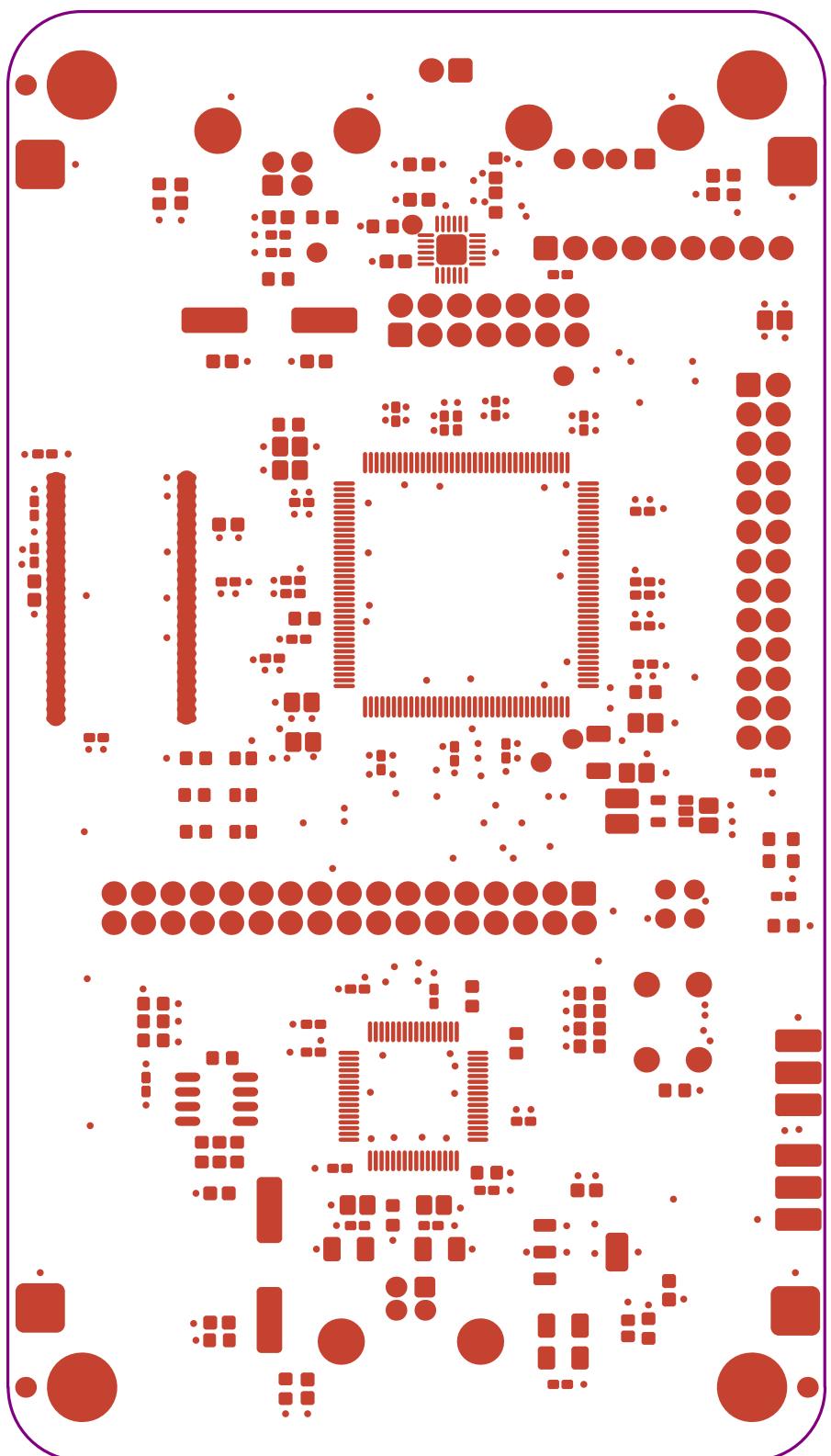
OpenVizsla v3.3  
(c) 2013,2014 bushing

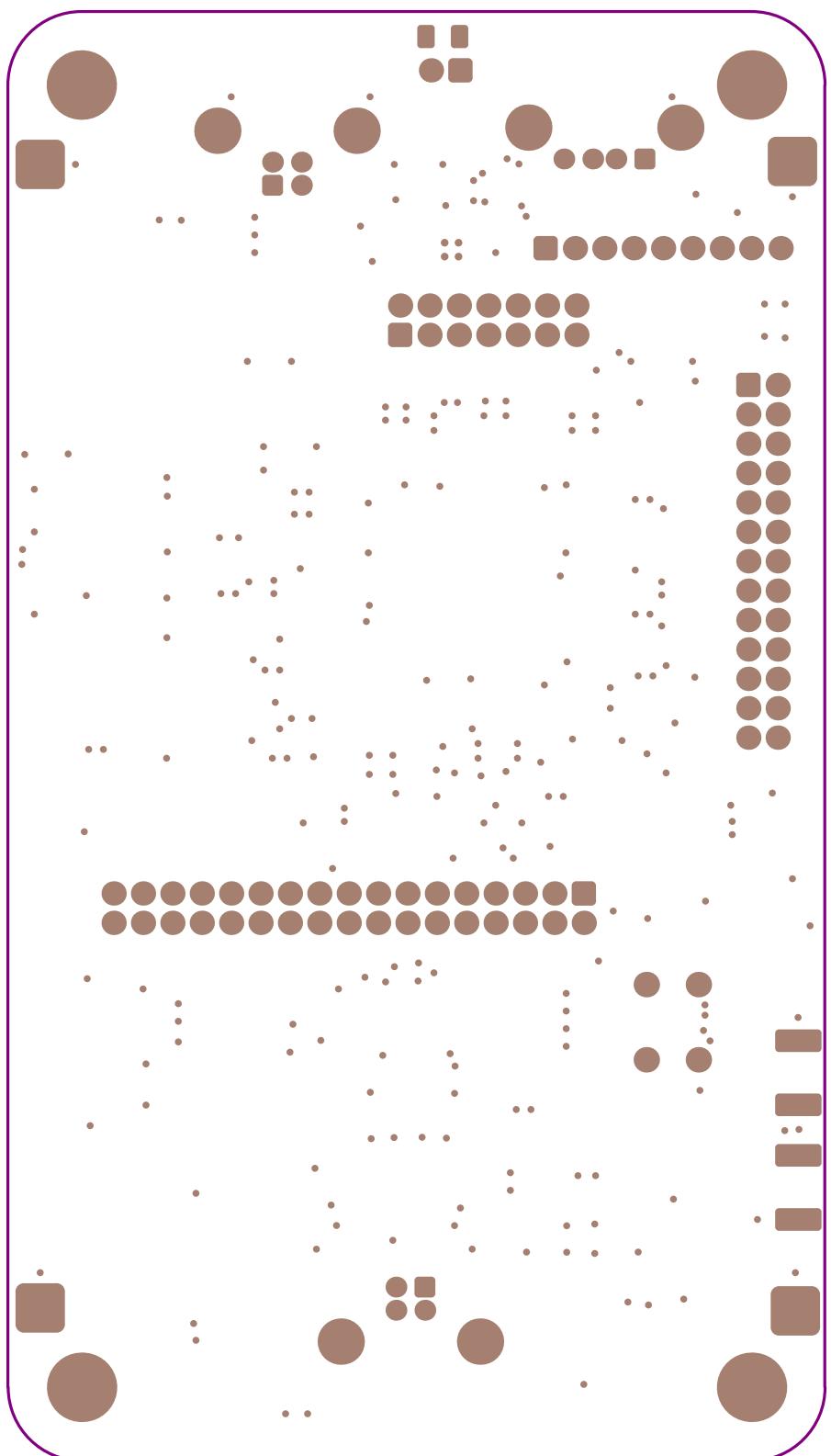


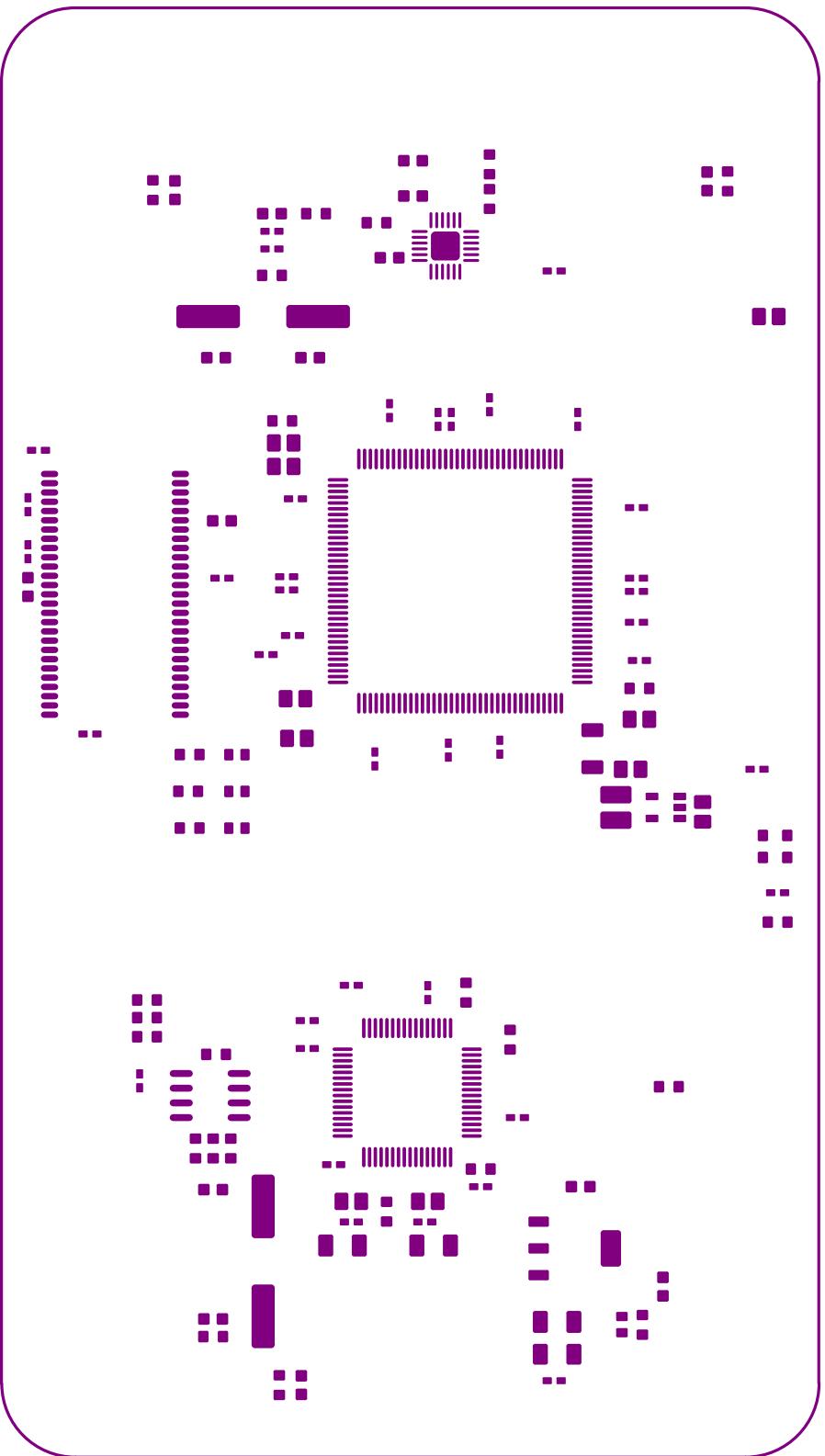


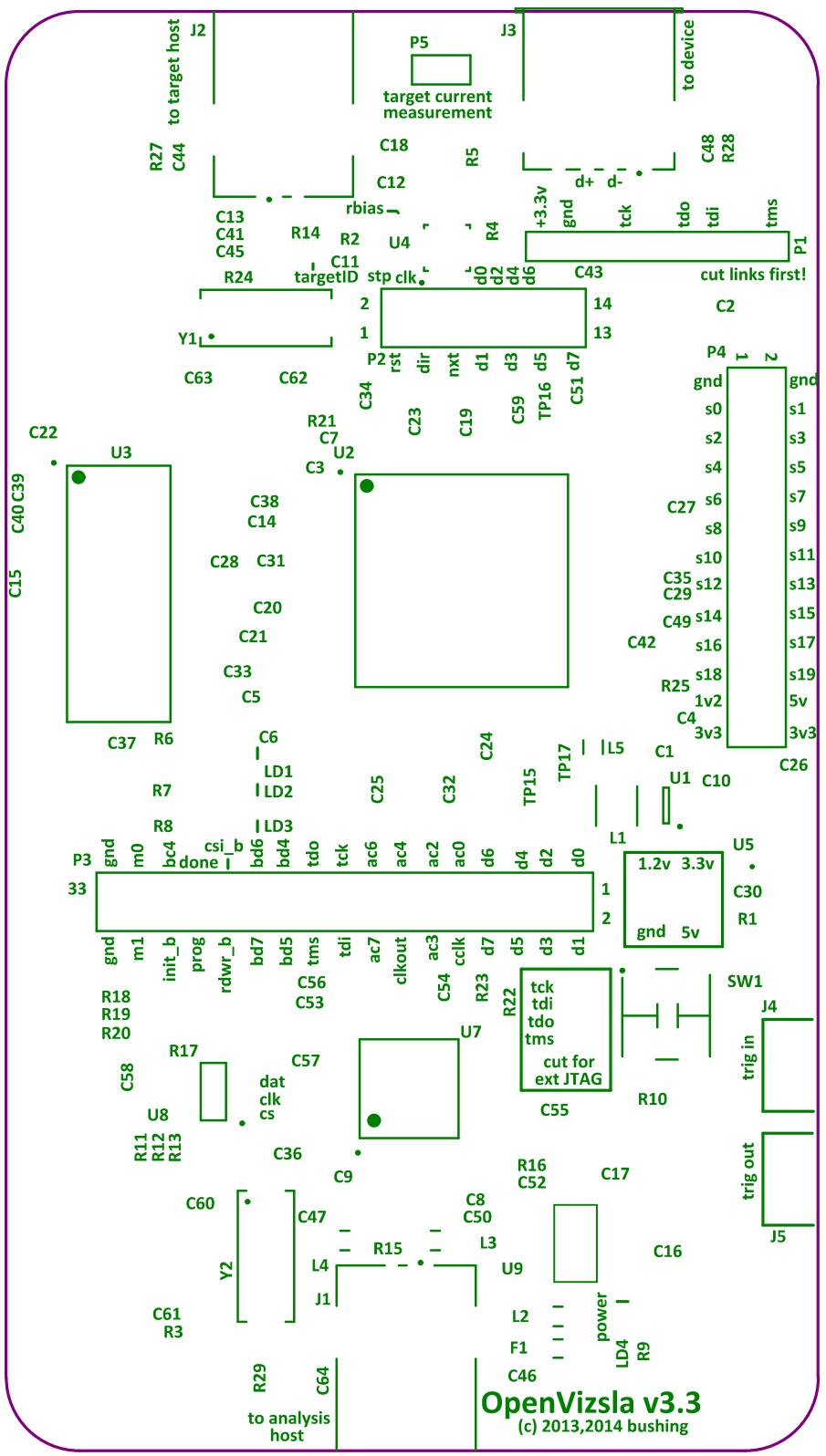












**OpenVizsla v3.3**  
(c) 2013,2014 bushing



