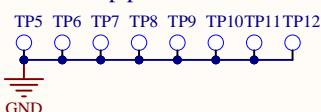
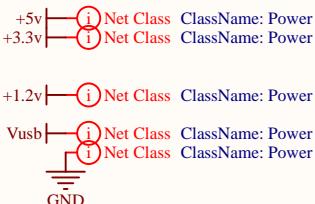
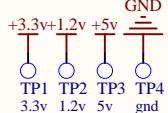


Ground clip pads



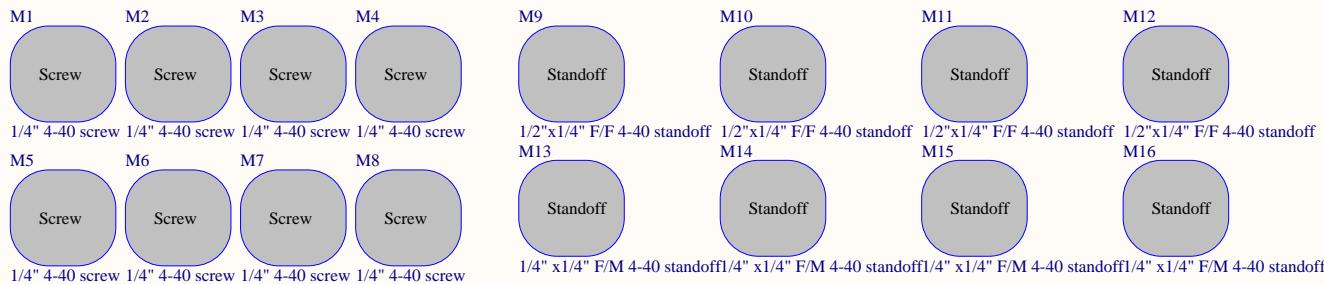
Power supply test points, top side



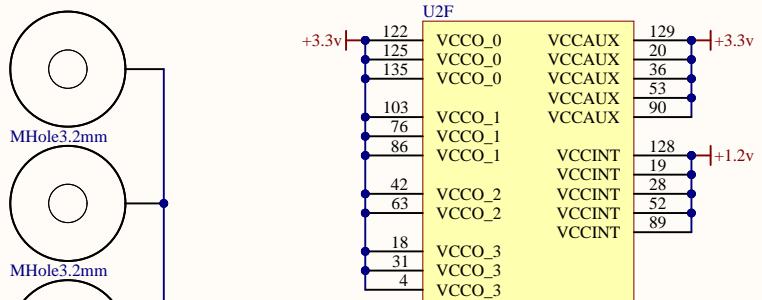
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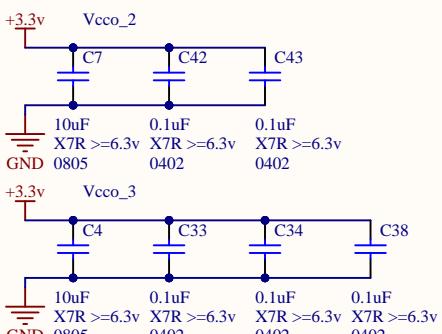
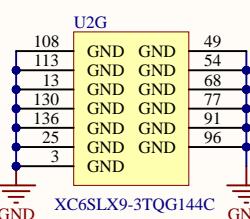
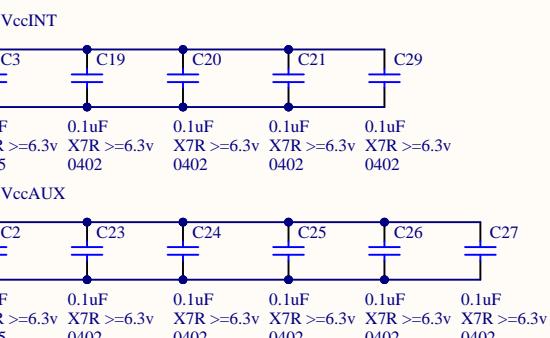
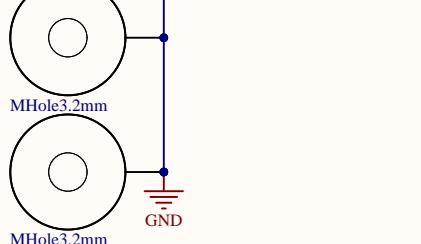
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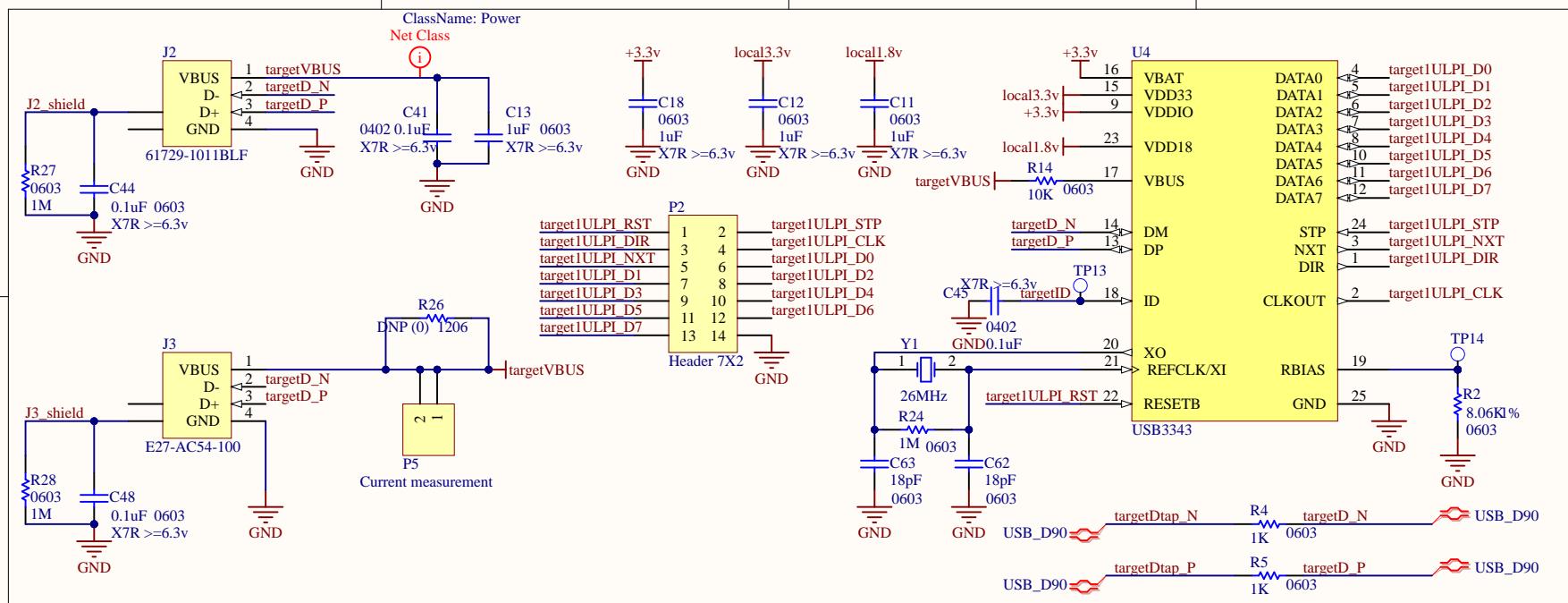


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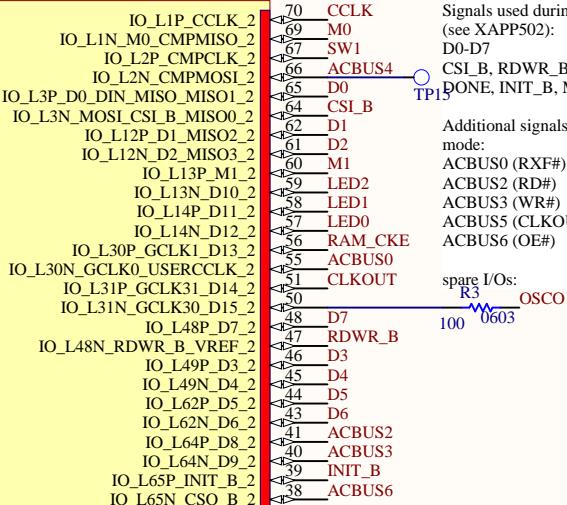
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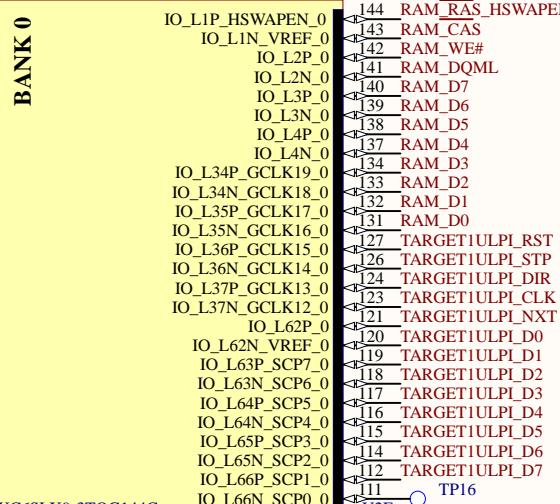
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U2C

BANK 2

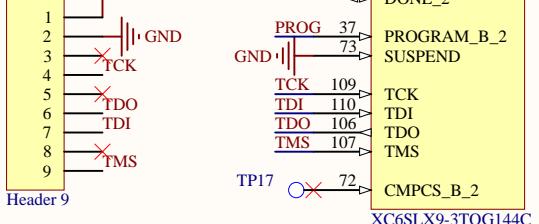
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U2A



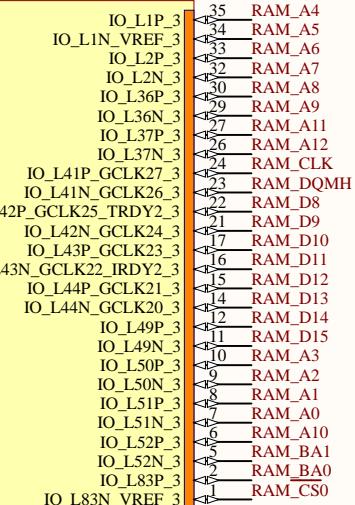
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P1

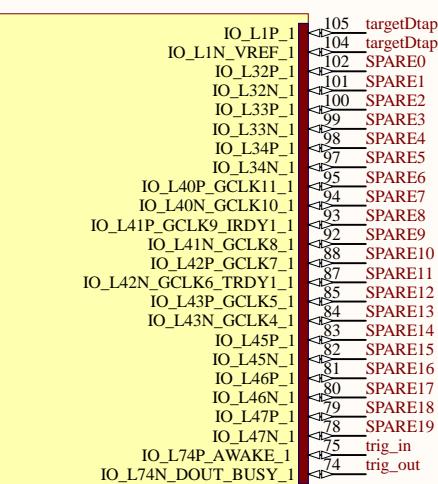


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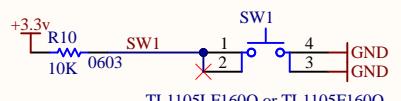
U2D

BANK 3

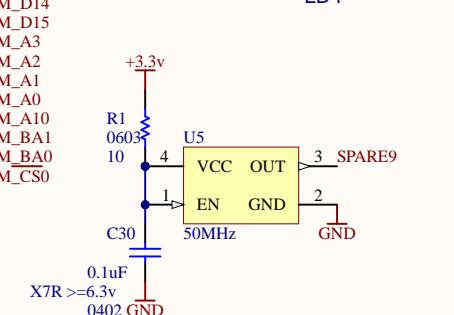
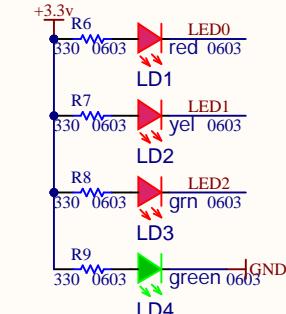
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BANK 1

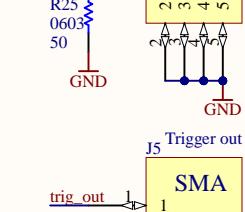
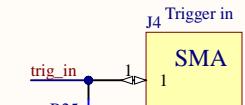
XC6SLX9-3TQG144C



TL1105LF160Q or TL1105F160Q



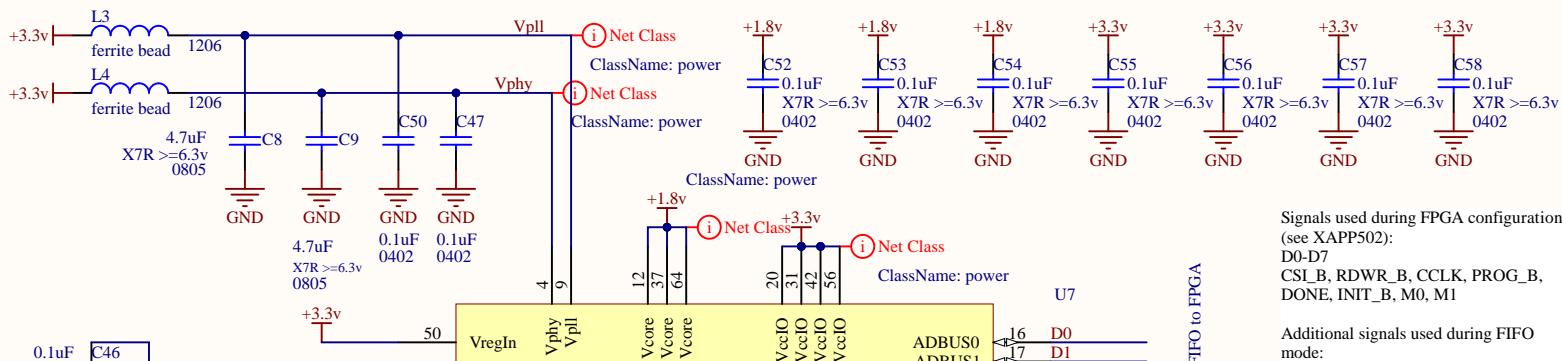
Spare 50MHz clock for bringup



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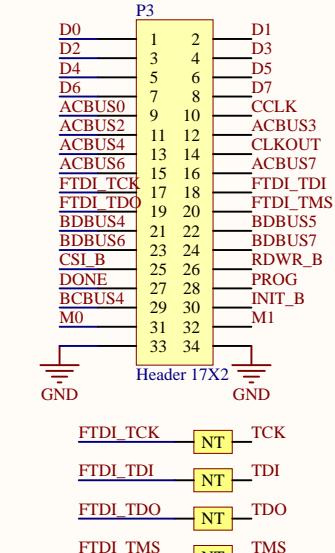
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Signals used during FPGA configuration
(see XAPP502):
D0-D7
CSI_B, RDWR_B, CCLK, PROG_B,
DONE, INIT_B, M0, M1

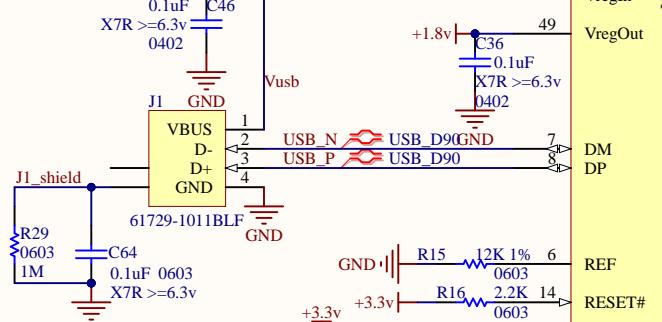
Additional signals used during FIFO mode:
ACBUS0 (RXF#)
ACBUS2 (RD#)
ACBUS3 (WR#)
ACBUSS (CLKOUT)
ACBUS6 (OE#)

spare I/Os:

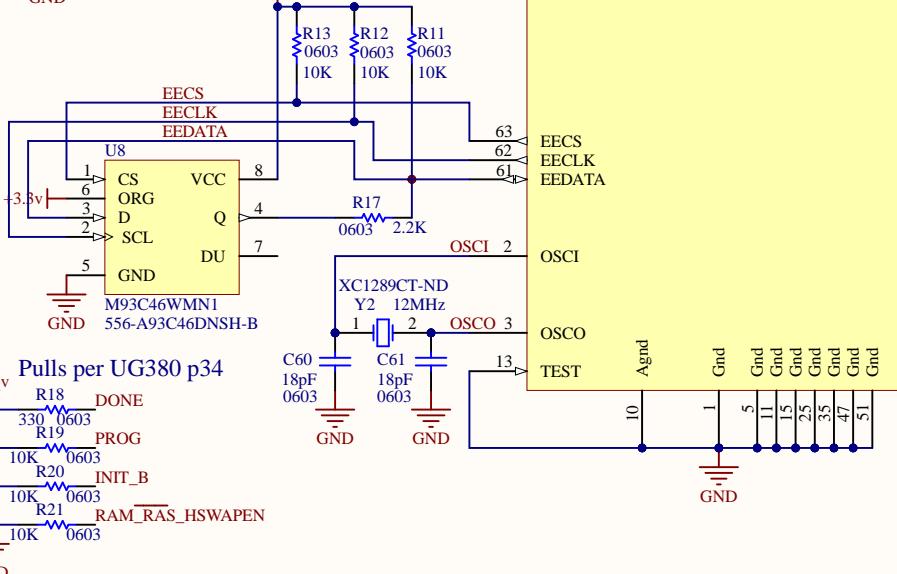


FT2232H

B

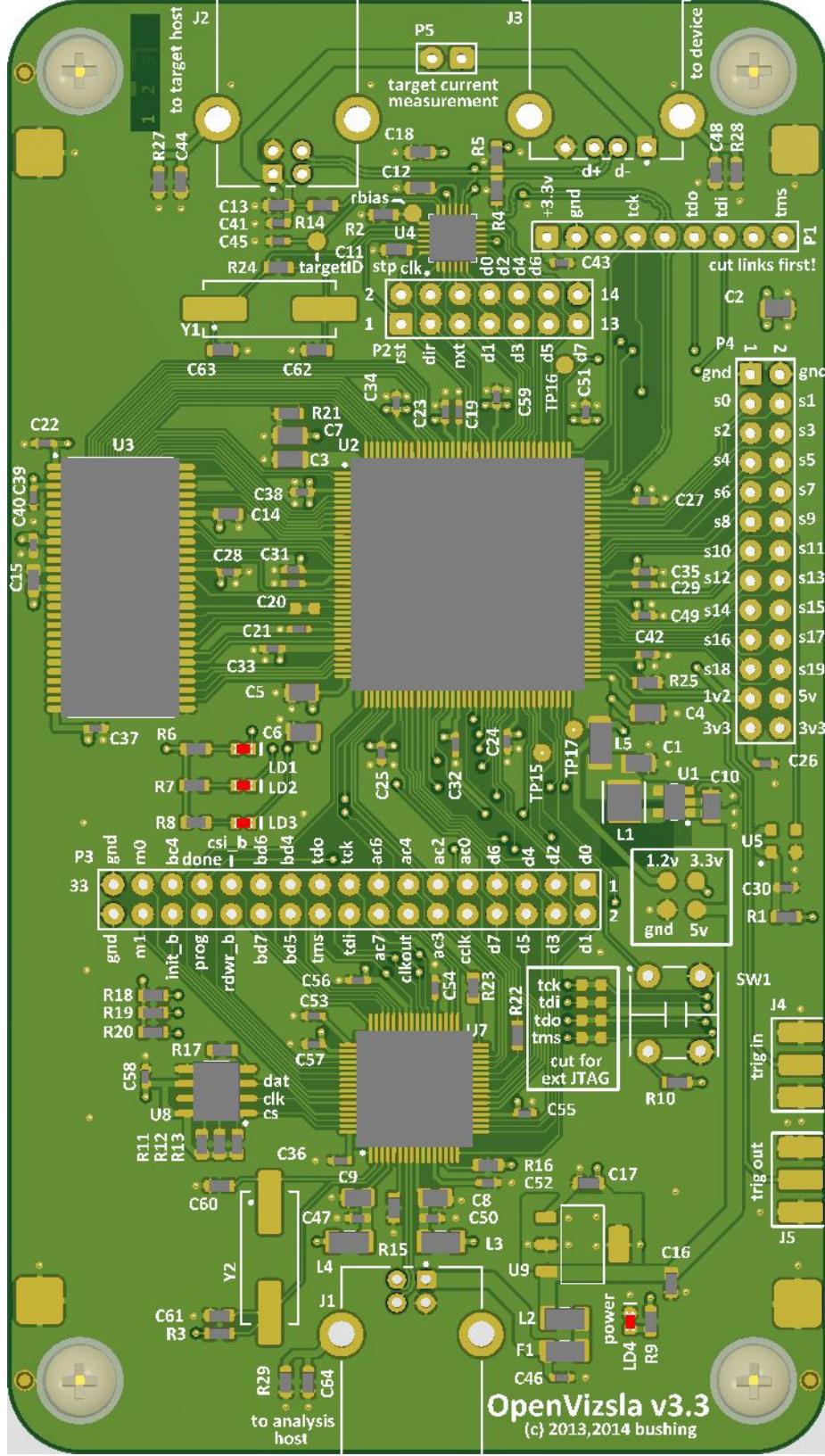


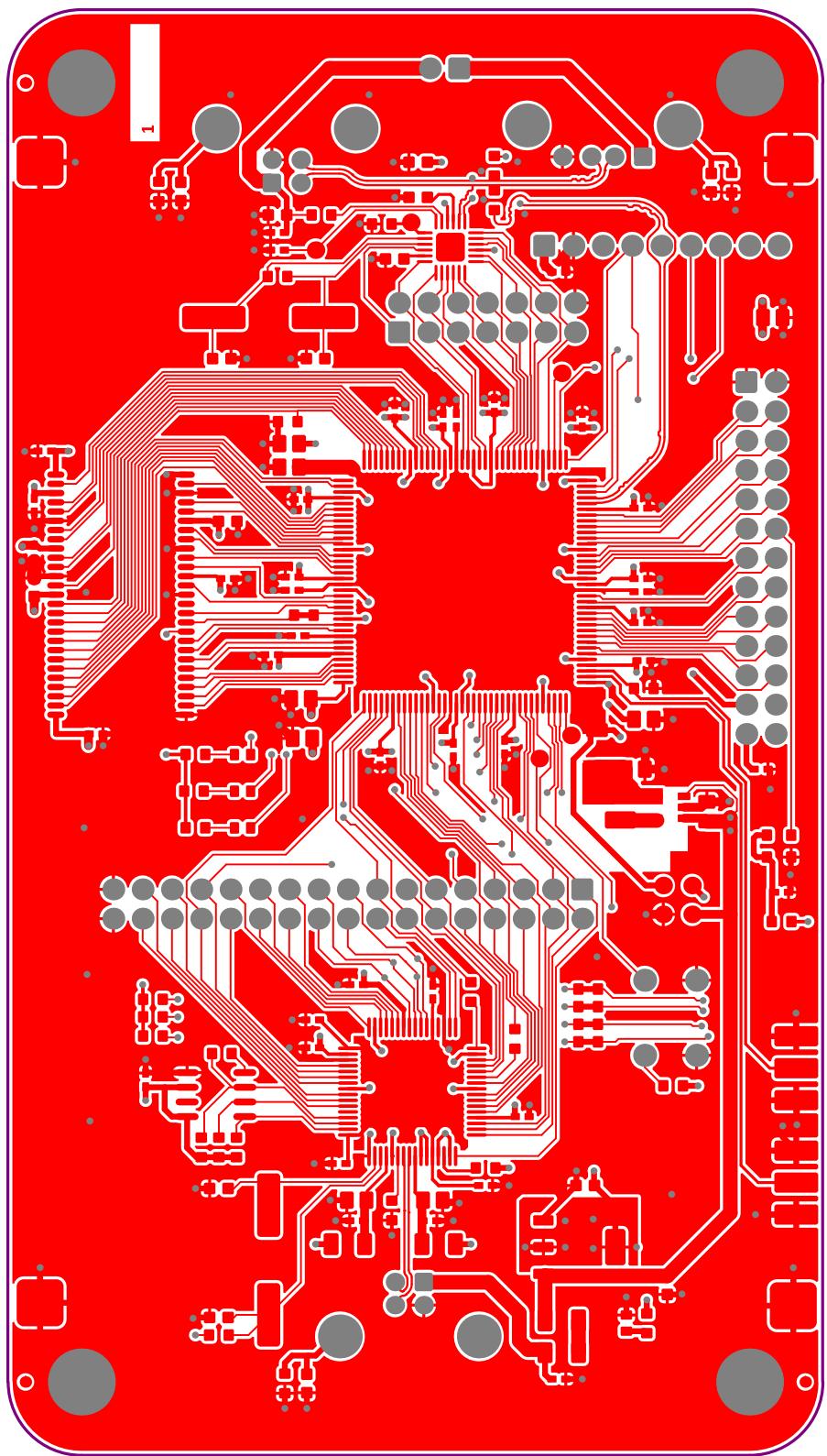
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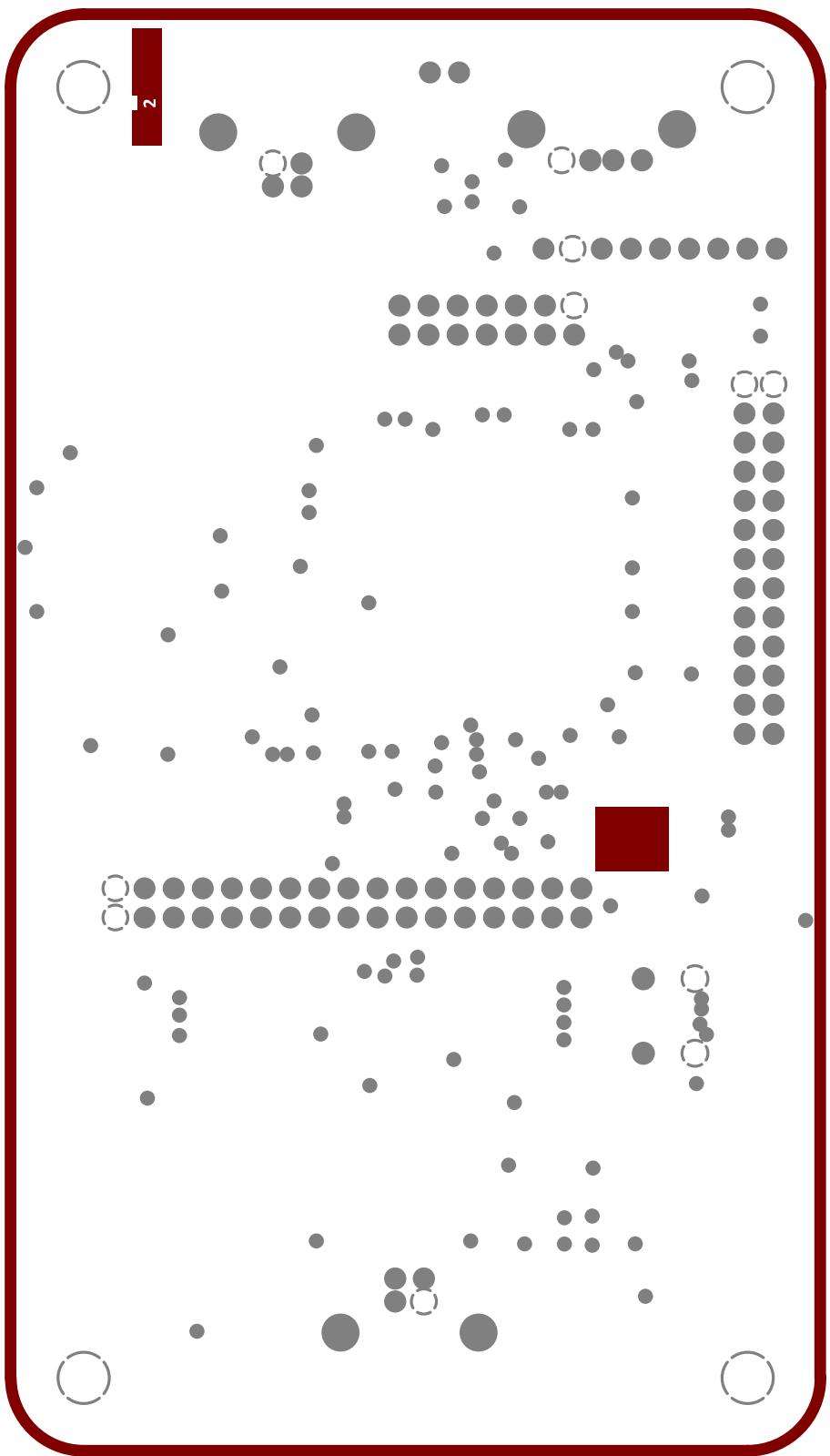


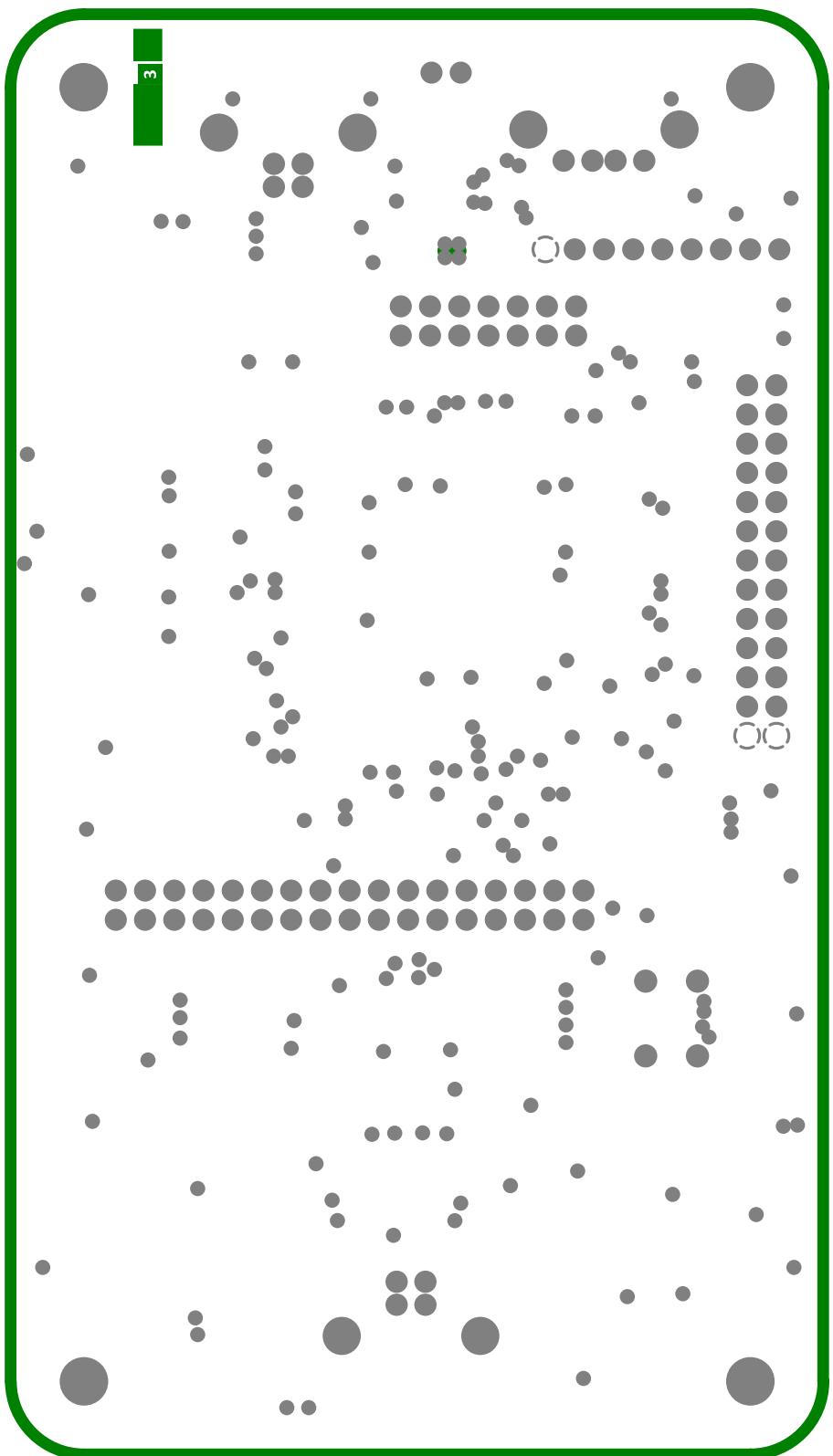
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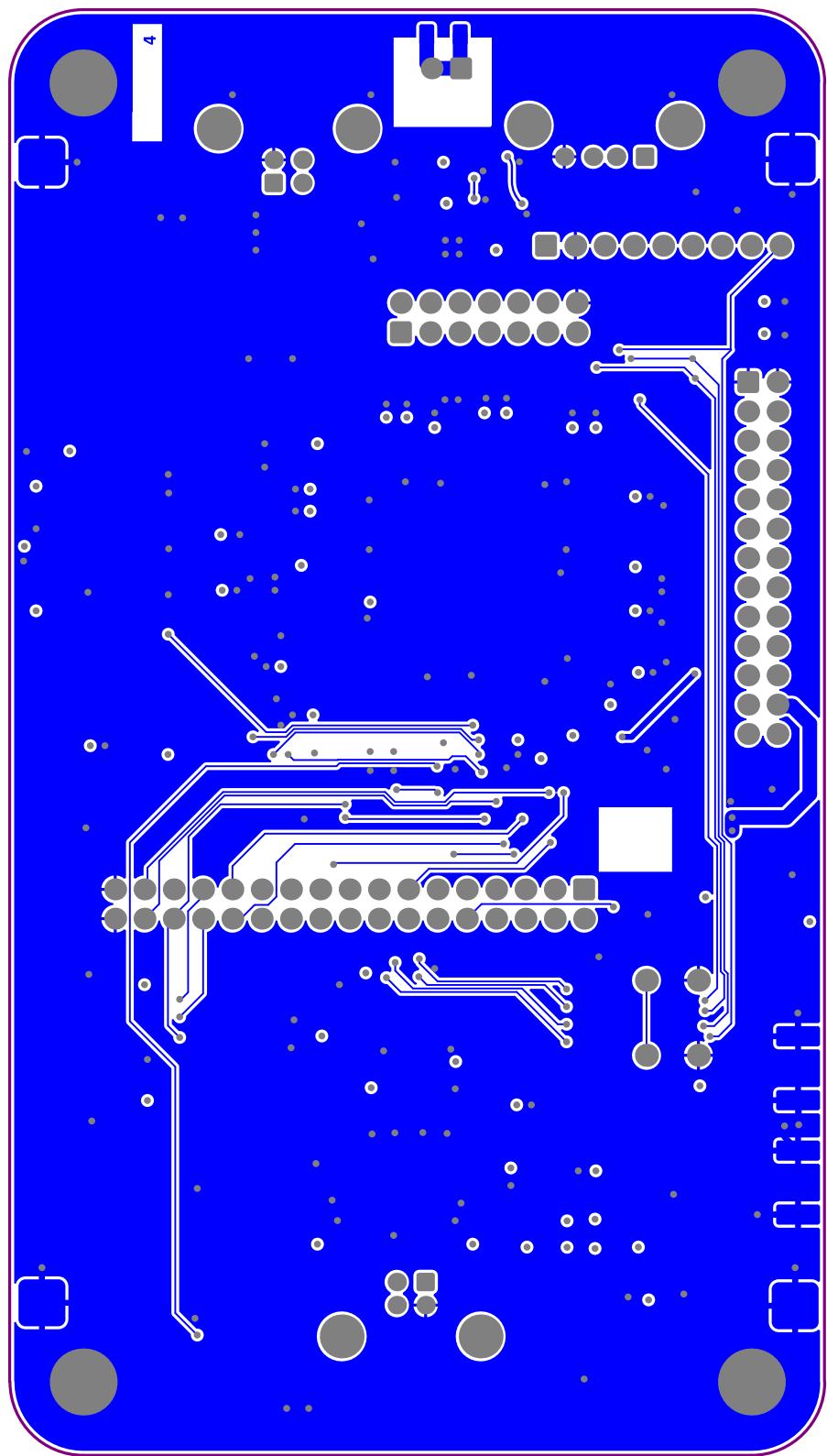
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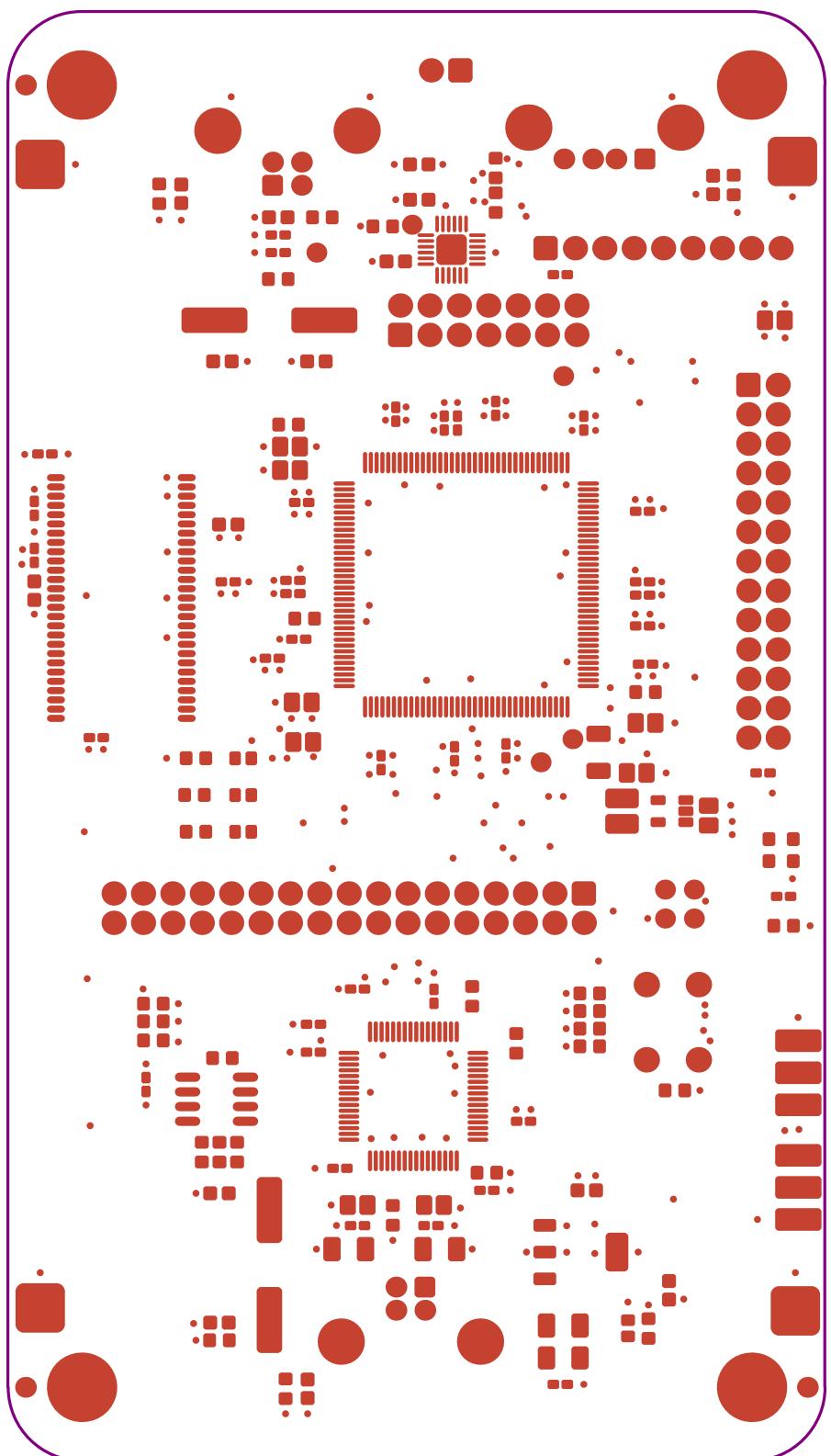


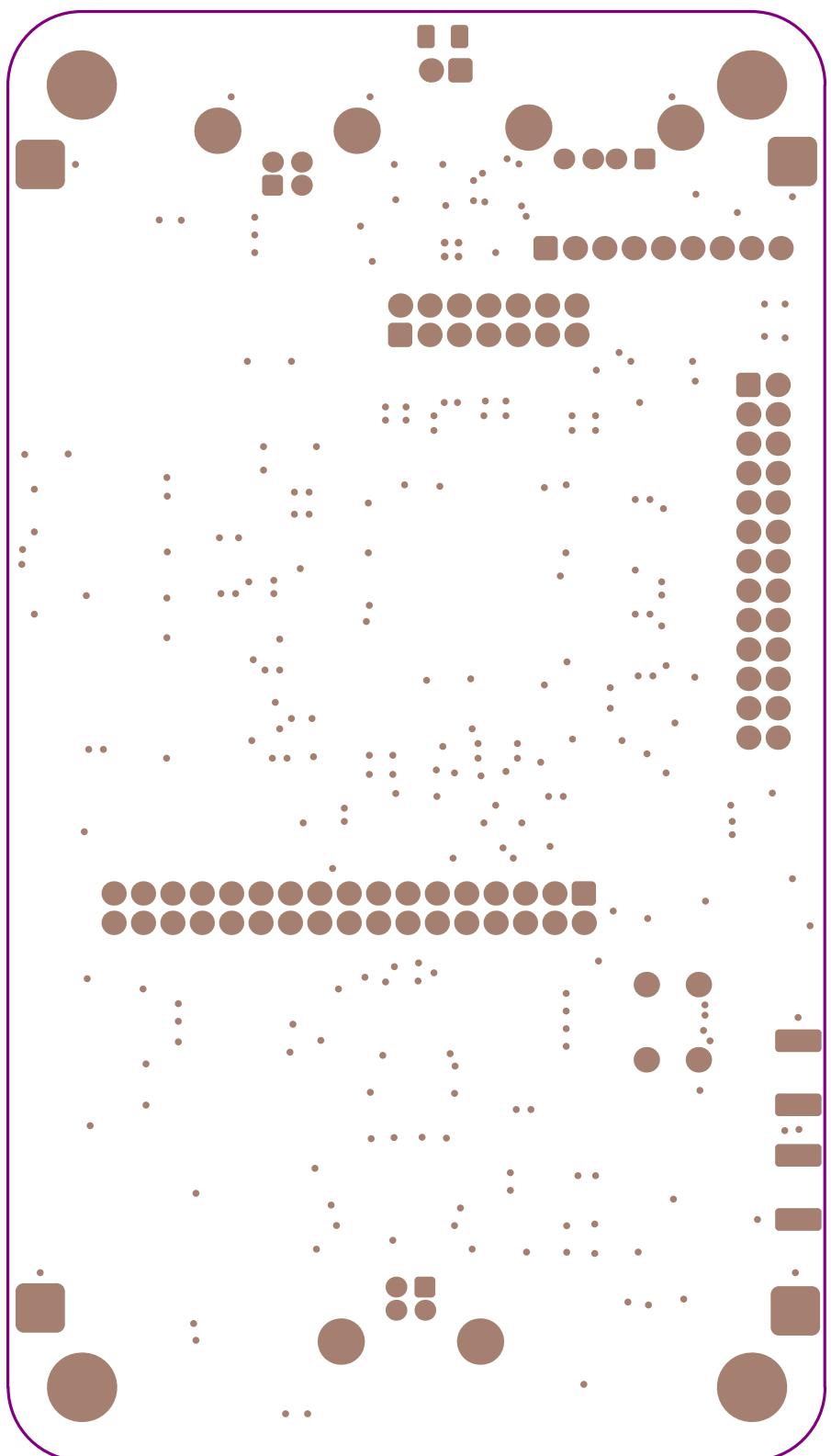


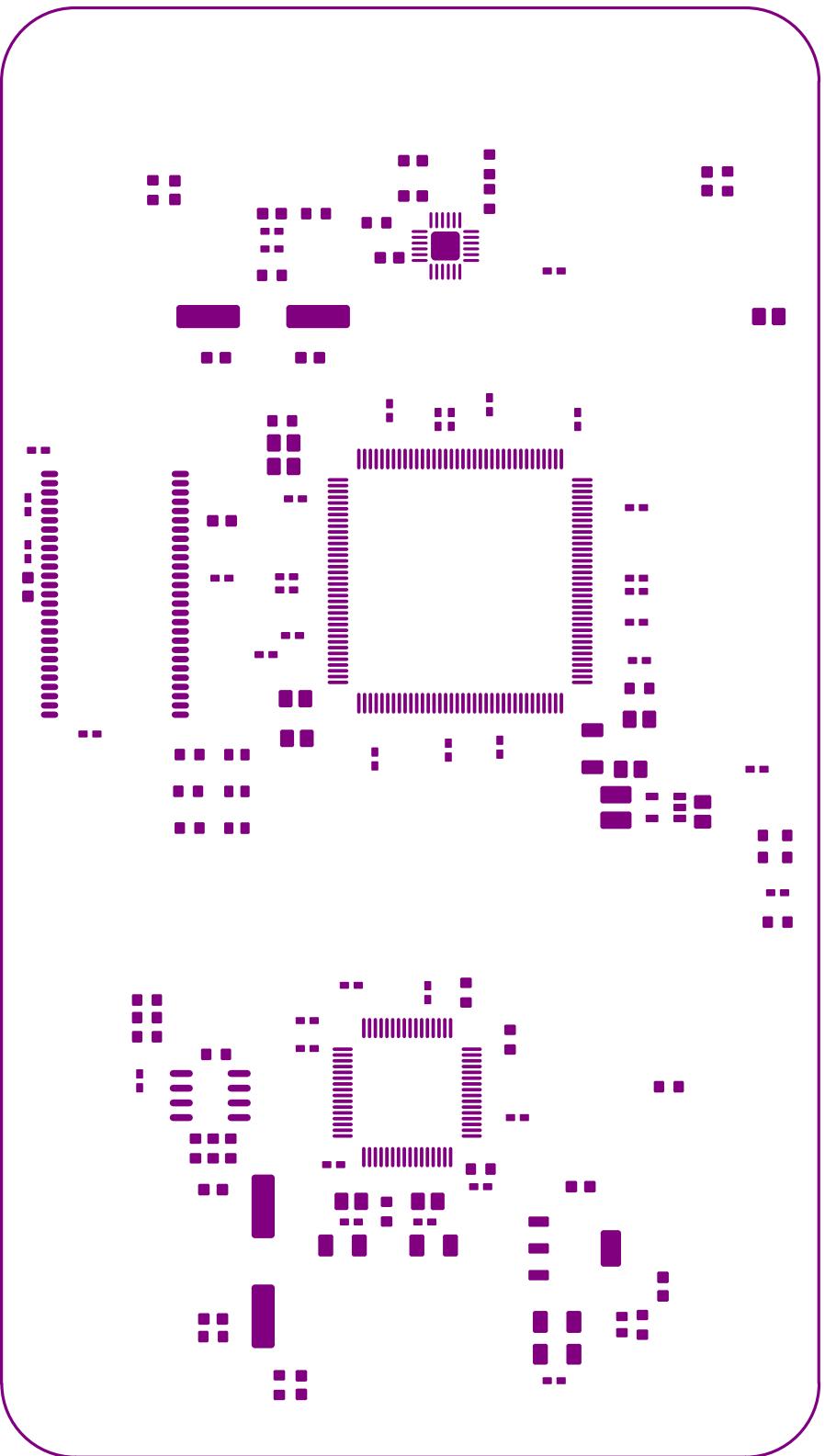


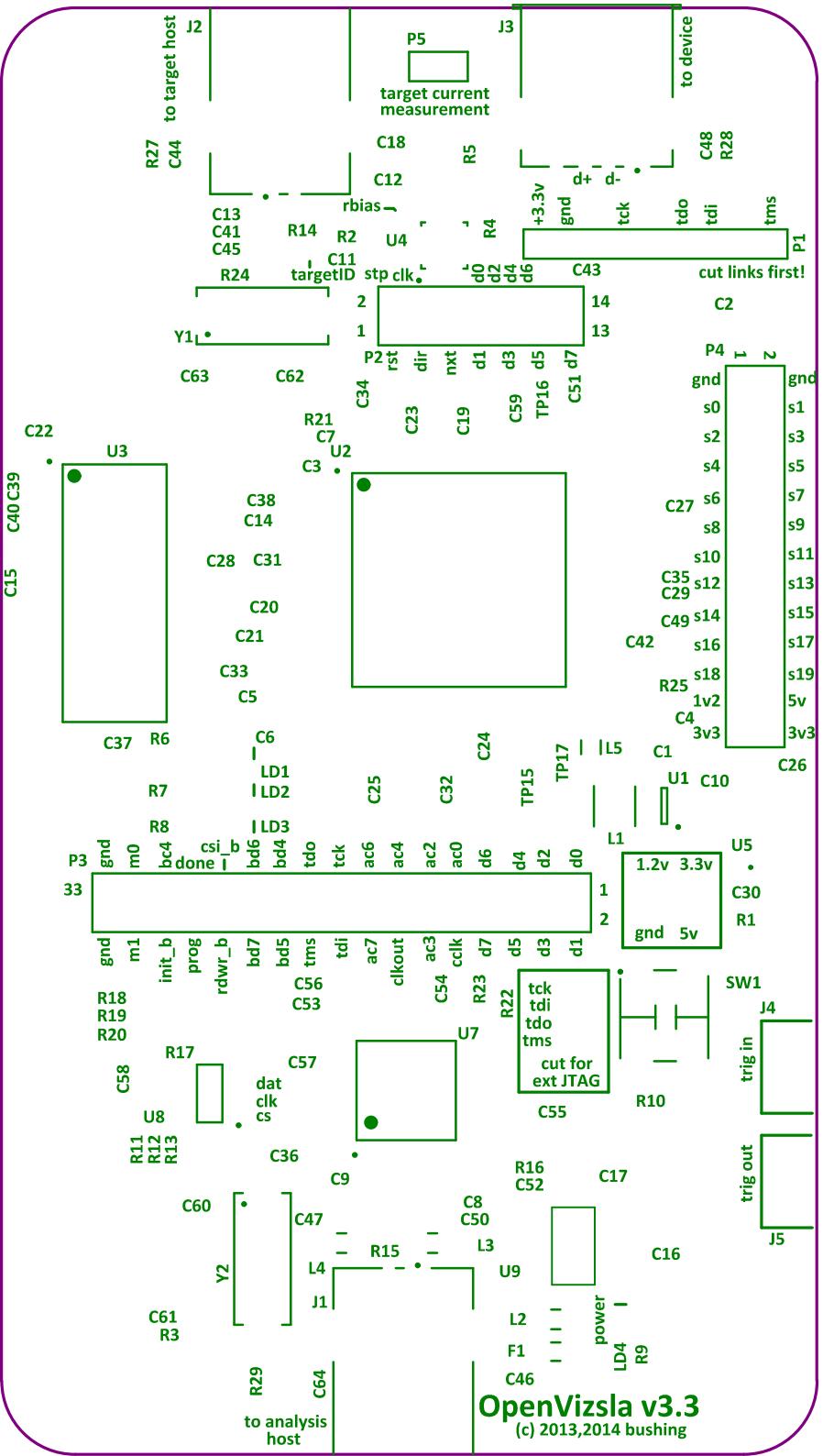












cut links first!
measure current
forget current
D- D+ bugs

cut links first!
measure current
forget current
D- D+ bugs

Vans
D- D+ bugs

R26 -

cut trace for
measure current
forget current
D- D+ bugs

cut links first!
measure current
forget current
D- D+ bugs



