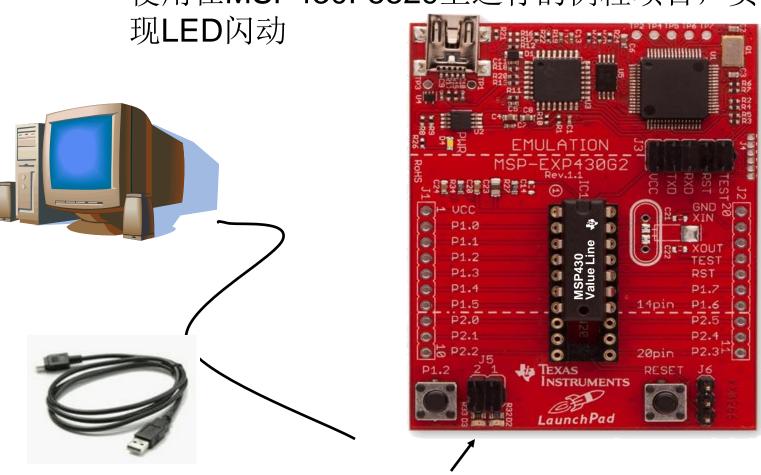
Lab_0: 闪动LED

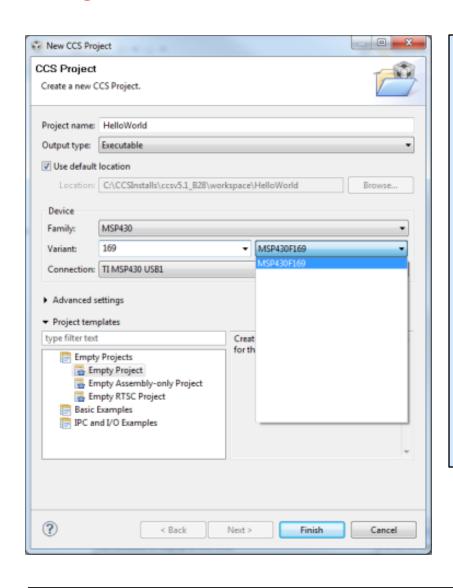
• 使用在MSP430F5529上运行的例程项目,实



LED1闪烁!



Project 创建向导



- 一步完成工程的创建,满足大多数情况的需求
 - 当NEXT按钮可用时,提醒需要进一 步的选择
- 包括Debugger的设置
 - 在选择了芯片后,可以选择所用的连接方式,环境会自动生成一个 ccxml 文件,在后续可以在该文件中对配置进行修改
- 使用默认配置
 - 大多数情况下,使用默认配置可以满足要求。其余,如Compiler version,endianness... 在 advanced 中可进行配置

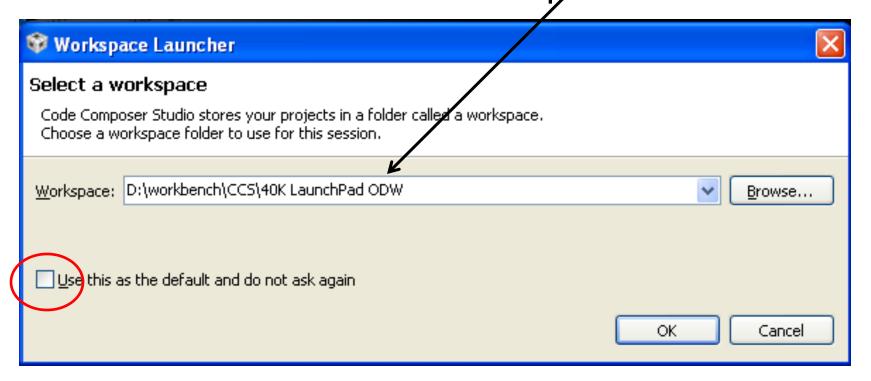
NSTRUMENTS

Step 1: 新建 CCS workspace

• 双击图标, 启动 CCS v5

*尽量避免中文字符(桌面?)

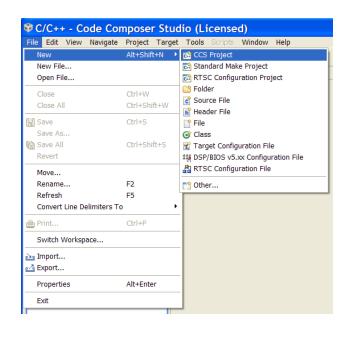
• 若未选择默认路径,设置 "Workspace" 路径

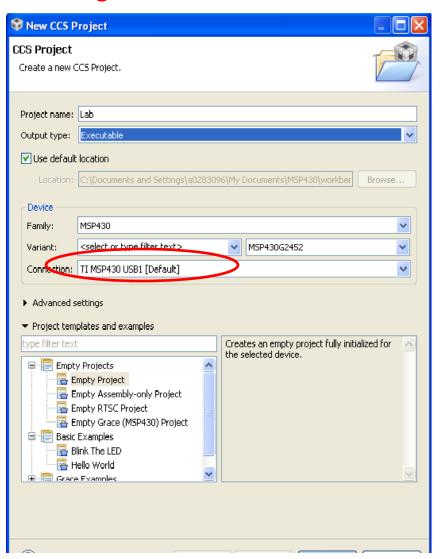




Step 2: 创建 CCS Project

- File > New > CCS Project
- Project 名称: Lab1
- Device>Family: MSP430
- Variant: MSP430F5529
- Project templates and example

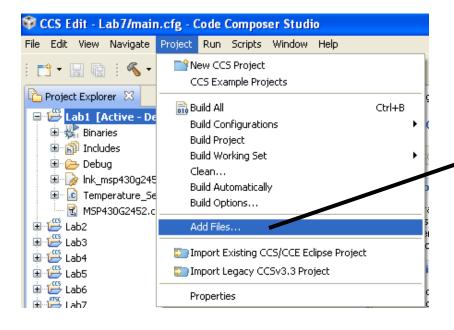


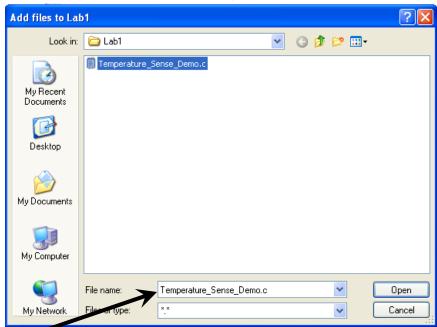


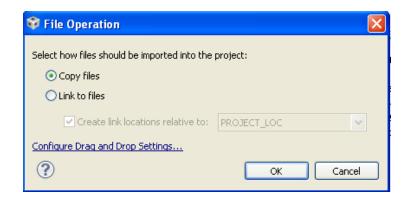


Step 3: 在CCS Project中添加文件

- Project > Add Files
- Navigate to Lab source folder
- And select : Temperature_Sense_Demo.c

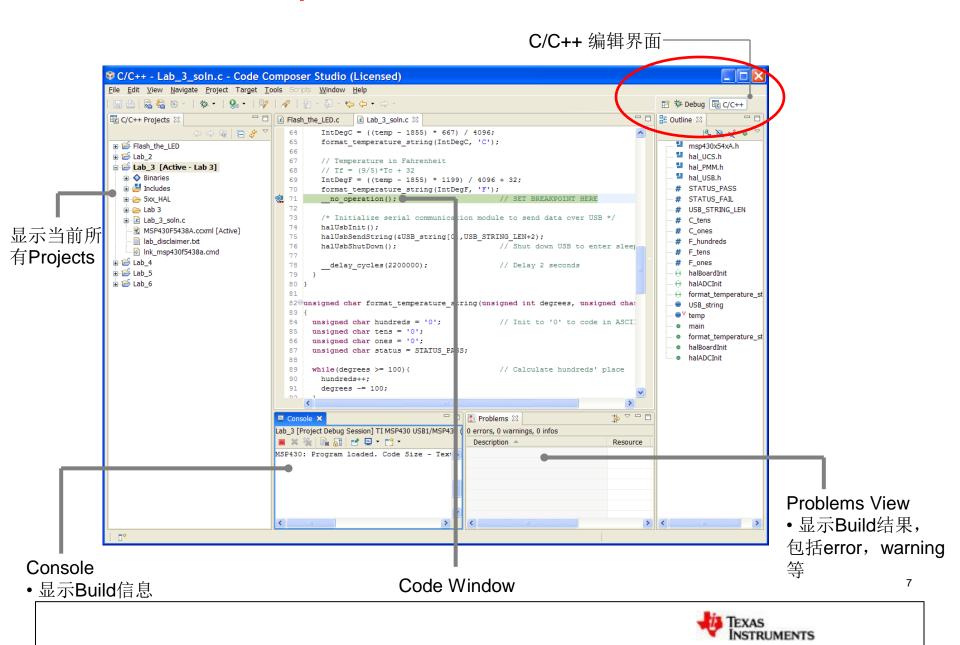




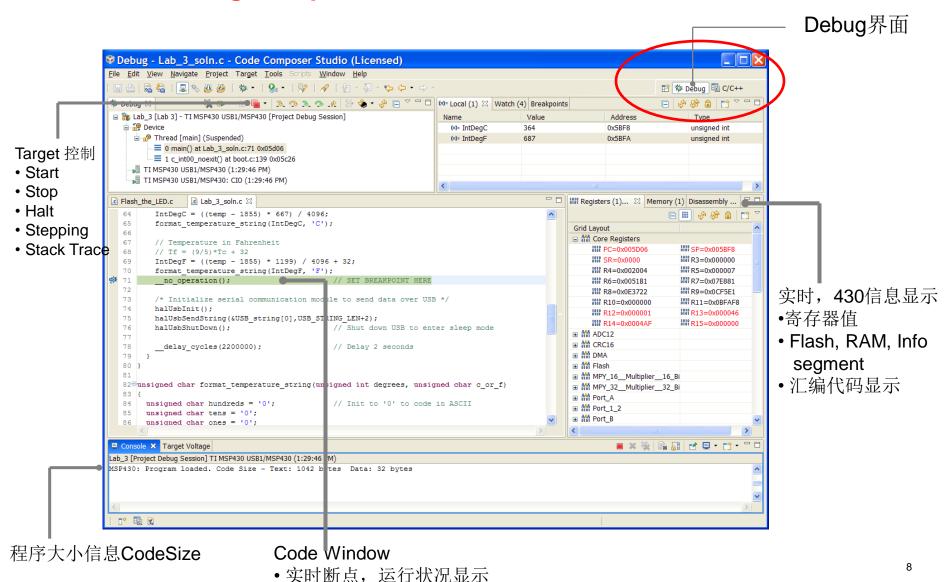




CCS 界面 – C/C++ Perspective Overview

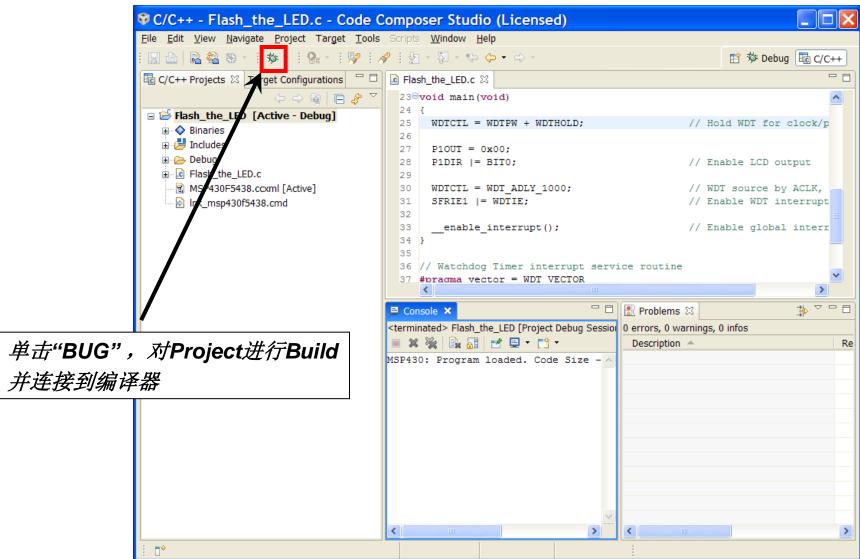


CCS 界面 – Debug Perspective Overview



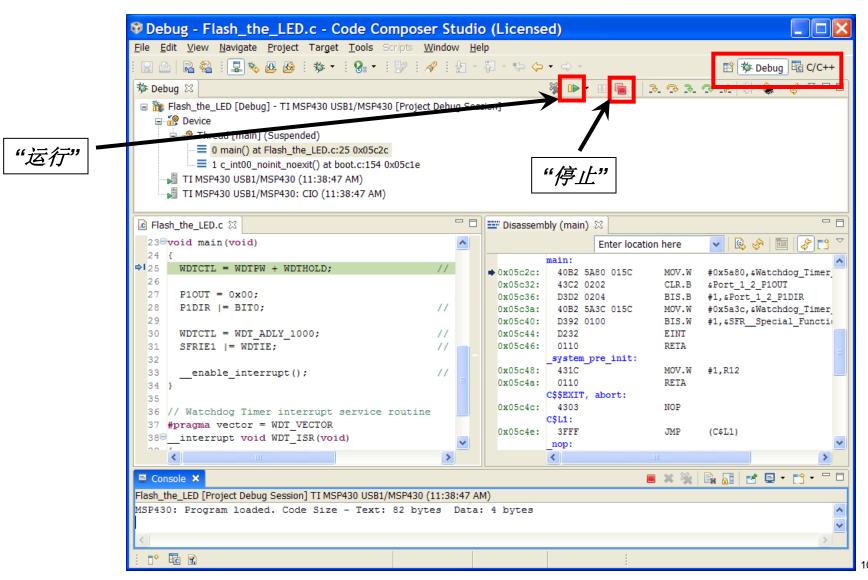
TEXAS INSTRUMENTS

Step 4: Build & Debug a CCS Project





Step 5: 运行,终止 CCS Project





I/O引脚寄存器

1. 方向寄存器PxDIR

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
PxDIR.7	PxDIR.6	PxDIR.5	PxDIR.4	PxDIR.3	PxDIR.2	PxDIR.1	PxDIR.0

Bit = 0: The port pin is switched to input direction

Bit = 1: The port pin is switched to output direction

2. 输出寄存器PxOUT

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
PxOUT.7	PxOUT.6	PxOUT.5	PxOUT.4	PxOUT.3	PxOUT.2	PxOUT.1	PxOUT.0

Bit = 0: The output is low

Bit = 1: The output is high

其他常用寄存器包括P1IN、P1SEL、P1REN、P1IFG、P1IE等,详见User's Guide第8章节。



I/O口常用操作

1. 将特定bit置1

2. 将特定bit置0

PxOUT
$$\&= \sim (BIT1 + BIT6);$$

3. 特定bit取反

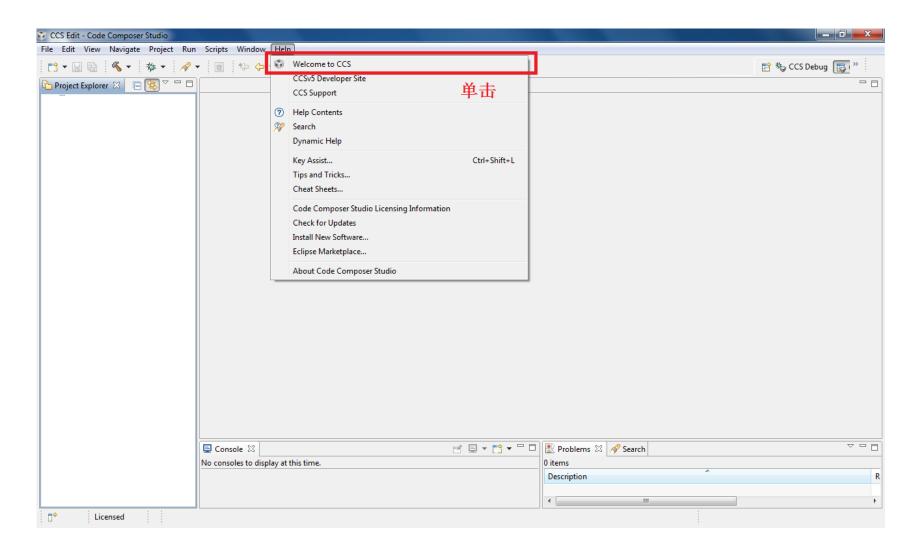


Lab_0: 闪动LED _code

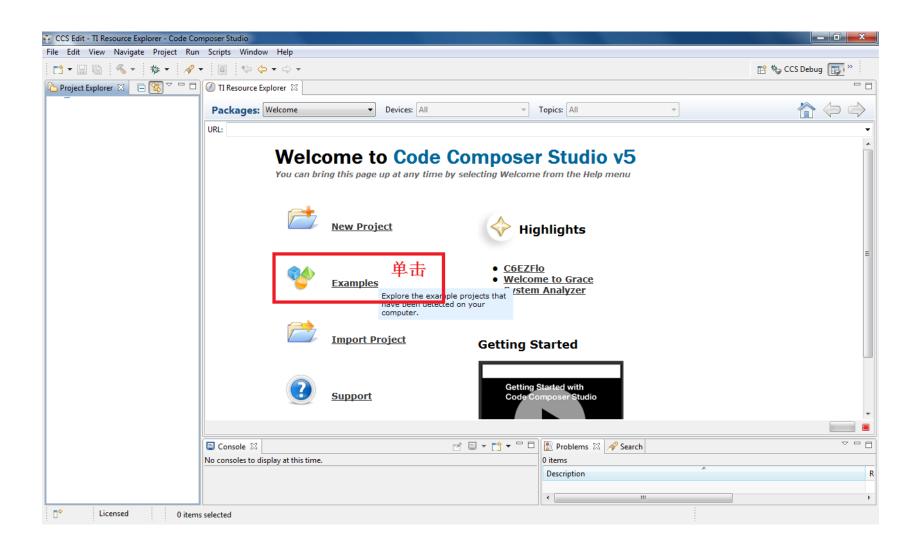
```
#include <msp430.h>
int main(void)
 WDTCTL = WDTPW + WDTHOLD; // Stop watchdog timer
 P1DIR |= 0x01;
                                    // Set P1.0 to output direction
 for (;;)
   volatile unsigned int i;  // volatile to prevent optimization
   P10UT ^= 0x01;
                                     // Toggle P1.0 using exclusive-OR
   i = 10000;
                                     // SW Delay
   do i--:
   while (i != 0);
```

这段代码为什么不够好?

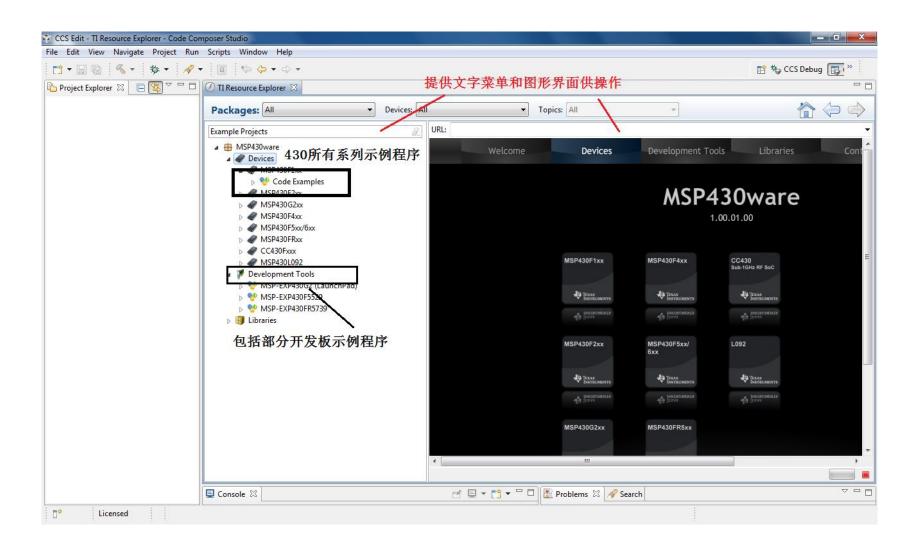




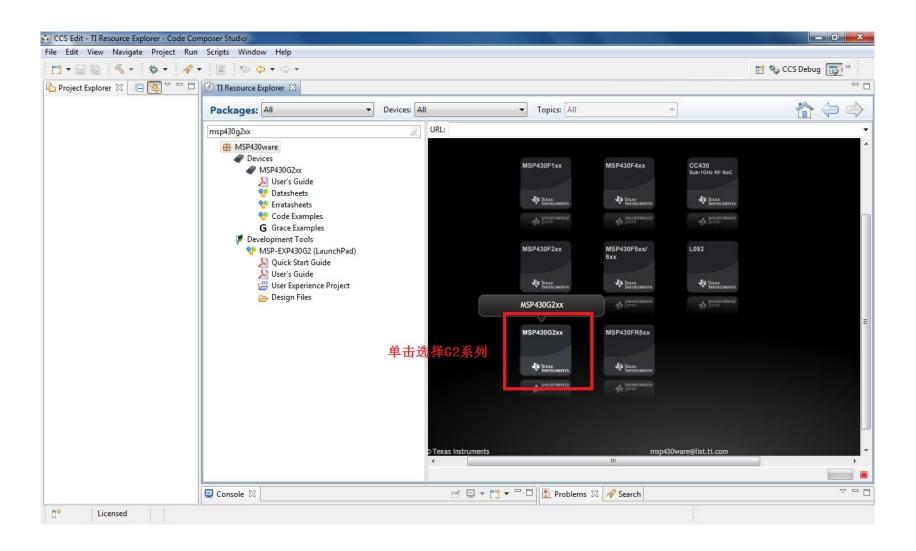




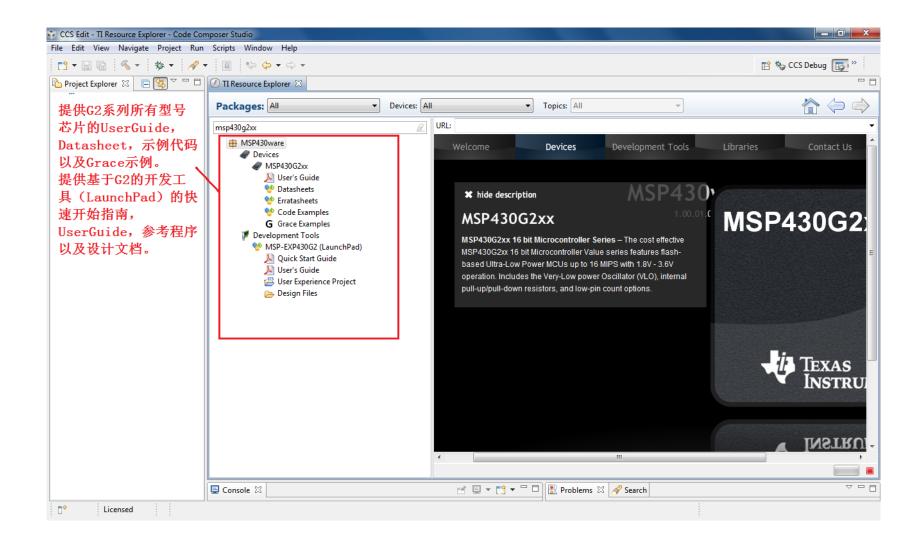




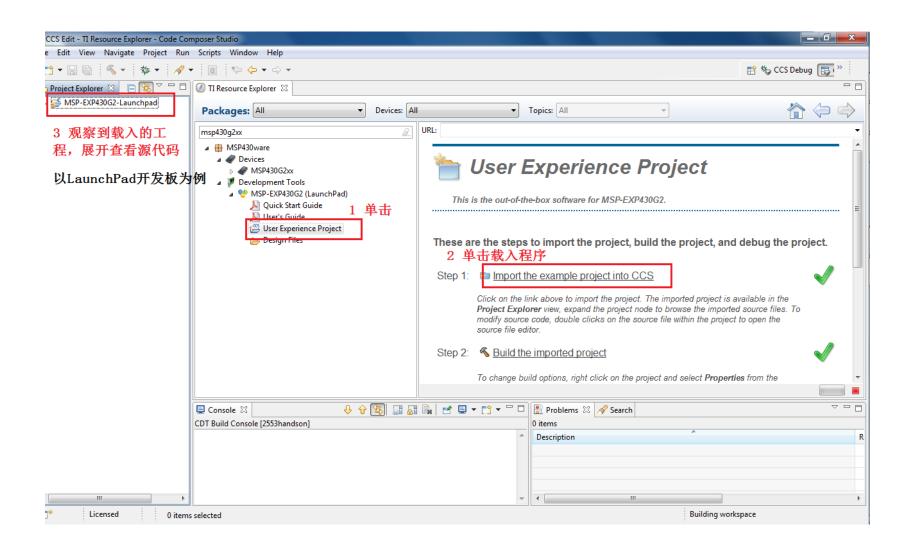




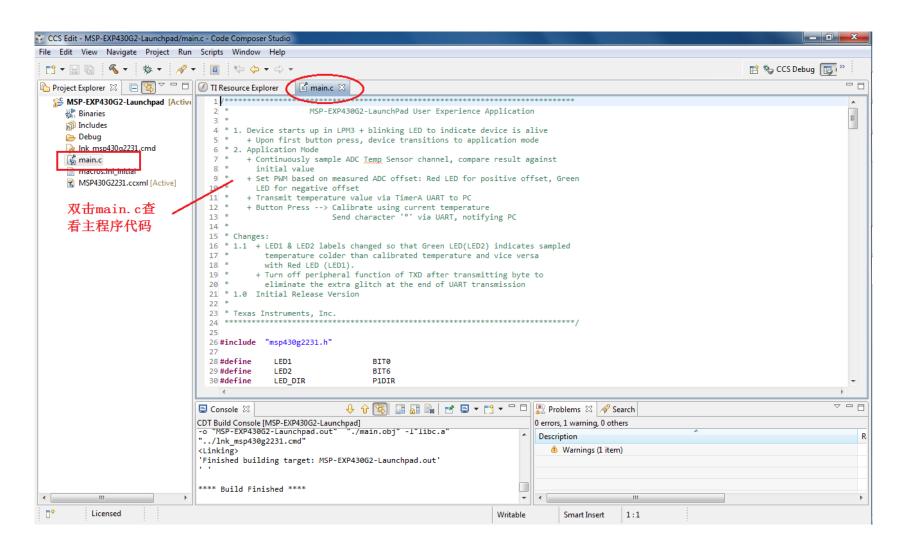








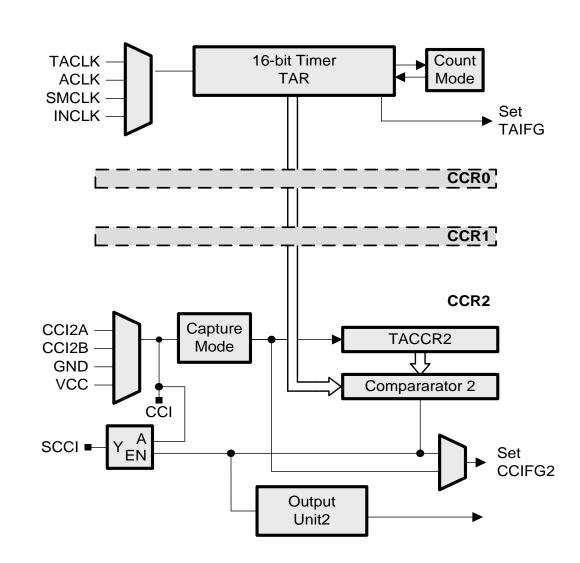






计时器_A

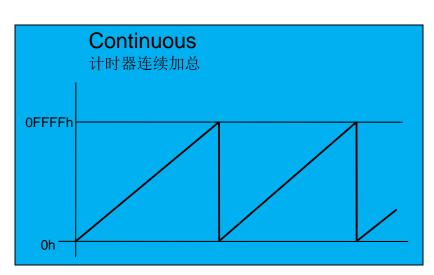
- 异步16-Bit计时器/计 数器
- 连续的、自上而下的 up count模式
- 多次捕获/比较寄存器
- PWM输出
- 中断矢量寄存器,以 便快速解码
- 可以触发DMA转移
- 可用于所有MSP430 产品

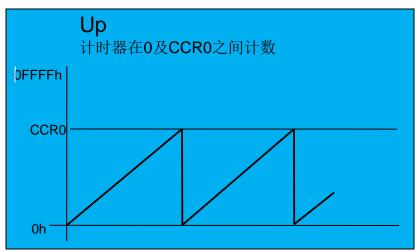


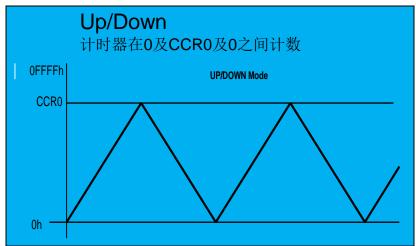


计时器_A 计数模式









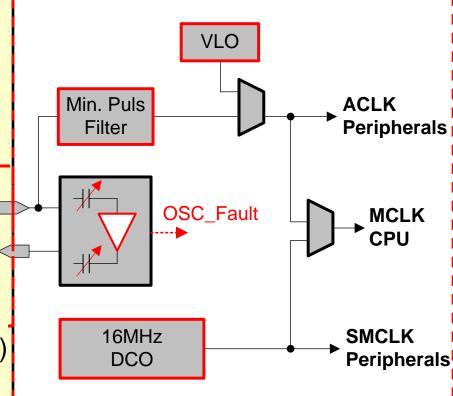
CCR - 计数比较寄存器



时钟系统



- Very Low Power/Low Frequency Oscillator (VLO)
 - 4 20kHz (典型值12kHz)
 - 500nA 待机流耗
 - 0.5%/° C and 4%/V 漂移
- 外接晶体振荡器(LFXT1, 低频)
 - 片内可编程电容
 - 故障保护 OSC_Fault
 - 脉冲滤波器
- Digitally Controlled Oscillator (DCO)
 - 0-to-16MHz
 - ± 3% 容差
 - 出厂校准(Flash I.M.)



上电后:

- •MCLK 和 SMCLK 由DCOCLK 提供(~1.1 MHz)
- •ACLK 由 LFXT1CLK 提供(LF 模式,6pF内部负载电容)



基本时钟控制寄存器



5.3.3 BCSCTL2, Basic Clock System Control Register 2

7	6		5	4	3	2	1	0
	SELMx		DIV	Mx	SELS	DIV	/Sx	DCOR ⁽¹⁾⁽²⁾
rw-0	rw-(0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0
SELMx	Bits 7-6	Sele	ct MCLK. These b	its select the MC	LK source.			
		00	DCOCLK					
		01	DCOCLK					
		10	XT2CLK when 2 on-chip.	XT2 oscillator pre	esent on-chip. LFX	T1CLK or VLOCLI	K when XT2 osci	llator not present
		11	LFXT1CLK or V	LOCLK				
DIVMx	Bits 5-4	Divid	ler for MCLK					
		00	/1					
		01	/2					
		10	/4					
		11	/8					
SELS	Bit 3	Sele	ct SMCLK. This bi	t selects the SM0	CLK source.			
		0	DCOCLK					
		1	XT2CLK when 2	XT2 oscillator pre	esent. LFXT1CLK	or VLOCLK when 2	XT2 oscillator not	t present
DIVSx	Bits 2-1	Divid	ler for SMCLK					
		00	/1					
		01	/2					
		10	/4					
		11	/8					
DCOR	Bit 0	DCO	resistor select. N	ot available in all	devices. See the	device-specific dat	ta sheet.	
		0	Internal resistor					
		1	External resisto	r				



TimerA输出模式

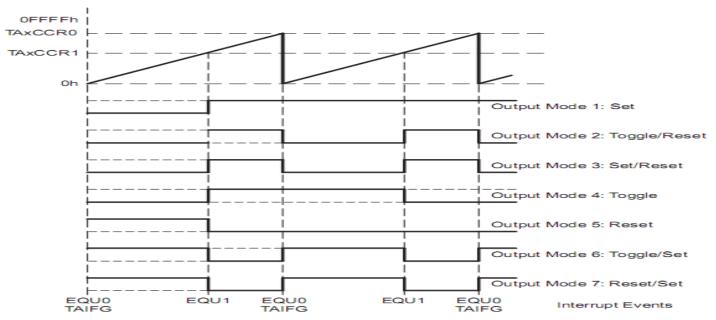


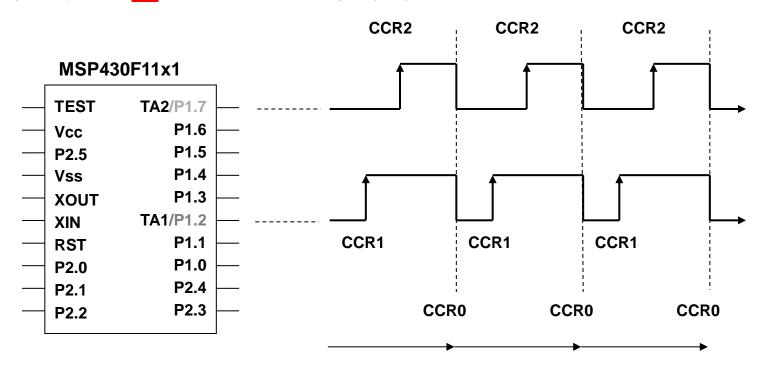
Figure 15-12. Output Example - Timer in Up Mode

Table 15-2. Output Modes

OUTMODx	Mode	Description
000	Output	The output signal OUTn is defined by the OUT bit. The OUTn signal updates immediately when OUT is updated.
001	Set	The output is set when the timer counts to the TAxCCRn value. It remains set until a reset of the timer, or until another output mode is selected and affects the output.
010	Toggle/Reset	The output is toggled when the timer counts to the TAxCCRn value. It is reset when the timer counts to the TAxCCR0 value.
011	Set/Reset	The output is set when the timer counts to the TAxCCRn value. It is reset when the timer counts to the TAxCCR0 value.
100	Toggle	The output is toggled when the timer counts to the TAxCCRn value. The output period is double the timer period.
101	Reset	The output is reset when the timer counts to the TAxCCRn value. It remains reset until another output mode is selected and affects the output.
110	Toggle/Set	The output is toggled when the timer counts to the TAxCCRn value. It is set when the timer counts to the TAxCCR0 value.
111	Reset/Set	The output is reset when the timer counts to the TAxCCRn value. It is set when the timer counts to the TAxCCR0 value.



计时器_APWM示例





- ◆ 可以为每一个CCR生成不同工作周期的独立频率
- ◆ MSP430网站提供代码示例

完全自动











