BUCK稳压器反馈补偿

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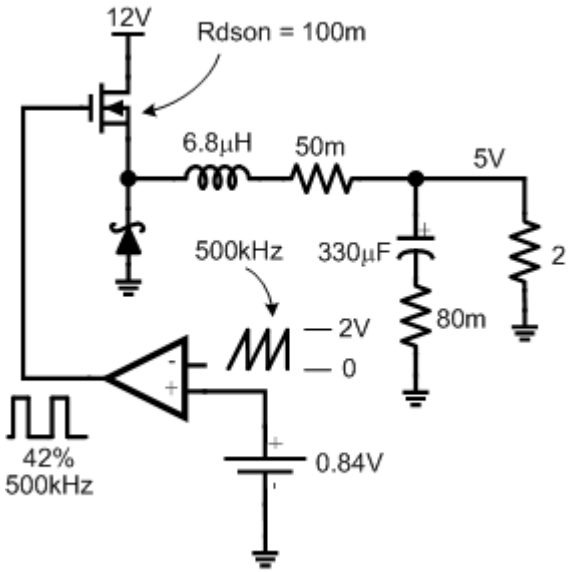
Why Do We Need Feedback Control In A Switcher

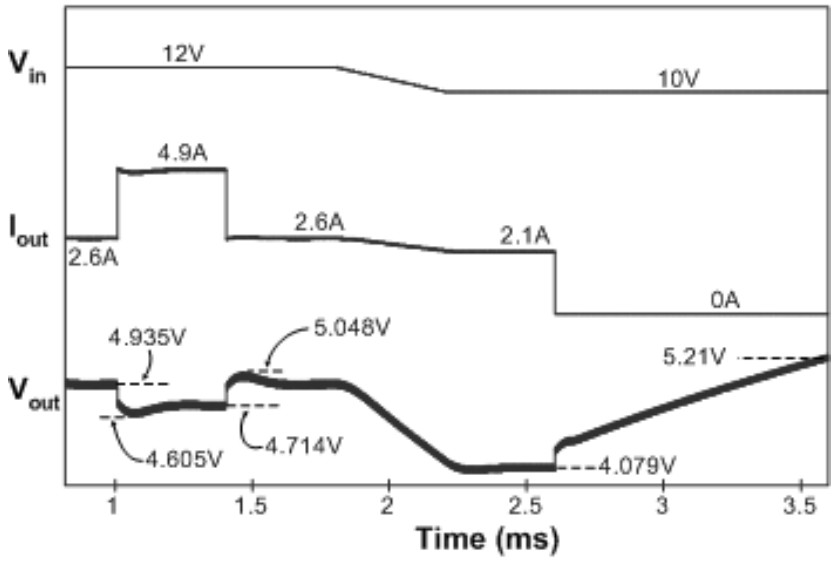
- For most DC/DC conversions, it is desirable to have a tightly regulated output voltage rail, independent of variations in the input voltage or the load current. In the case of a buck regulator, it is possible to run the circuit open-loop as shown in the figure below.

- A 0.8V fixed voltage is compared with a 500kHz saw tooth to generate a pulse train with a 42% duty cycle. The pulse train is used to control the on and off state of the MOSFET switch. Therefore, with an input voltage of 12V and the MOSFET being turned on for 42% of the time, the output voltage will be appoximately 5V.



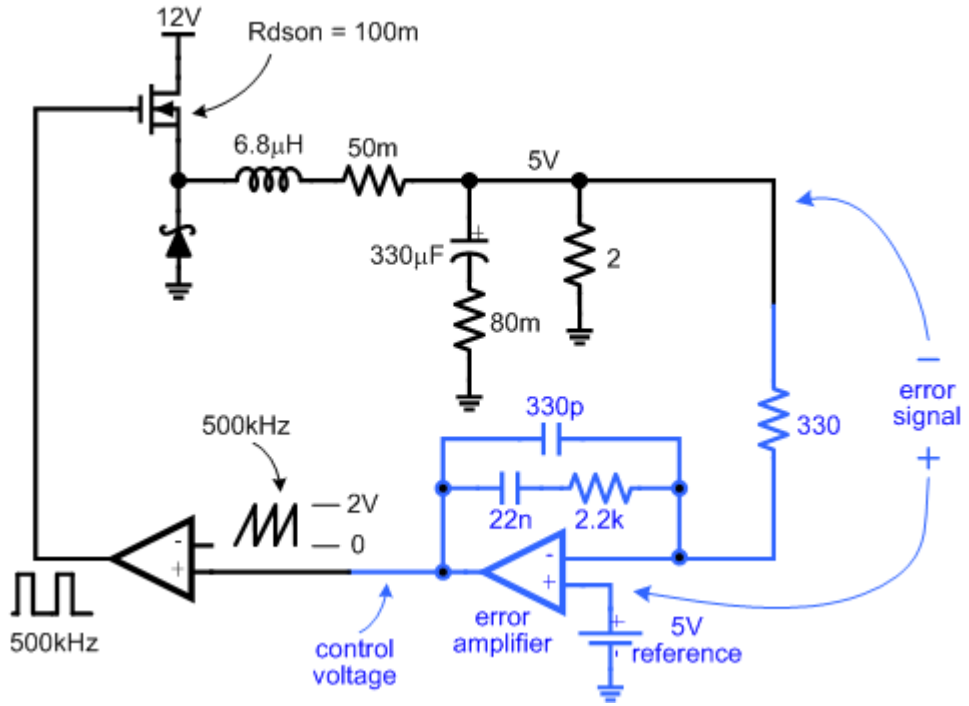
Why Do We Need Feedback Control In A Switcher

- In reality, the load is usually not so constant. The input voltage can sometimes change significantly. The figure below shows that when the input voltage and load current change, the output voltage also changes, sometimes significantly.



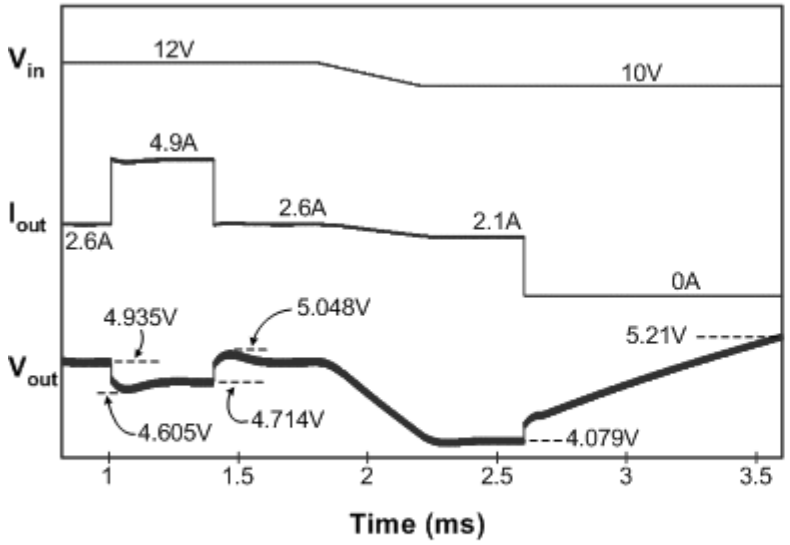
Why Do We Need Feedback Control In A Switcher

- By replacing the 0.8V fixed voltage source with an active RC network connected to the output, a "closed loop" is created.

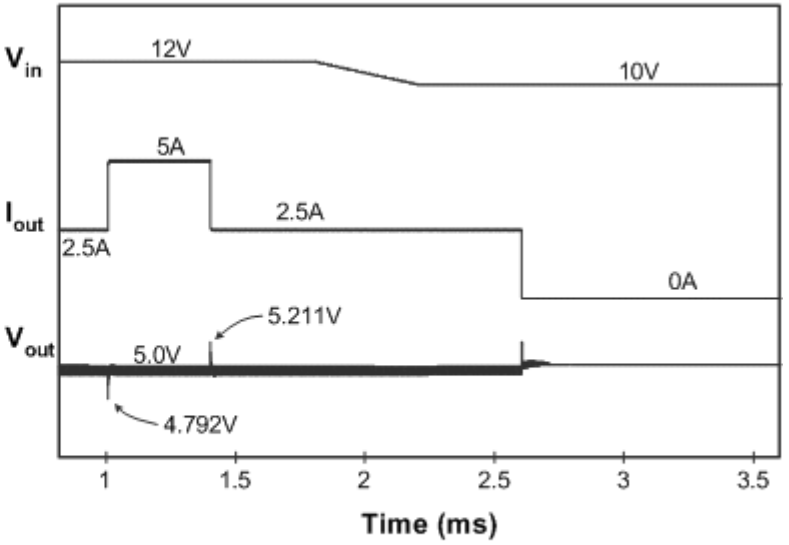


Why Do We Need Feedback Control In A Switcher

- The diagrams below compare the reponses of an open loop buck regulator and a closed loop buck regulator to the same transients. The closed-loop load transient response is totally different - Vout quickly settles back to the target value (5V) instead of gradually to a lower value. The closed-loop response to the change in Vin is even better with almost no change to Vout.



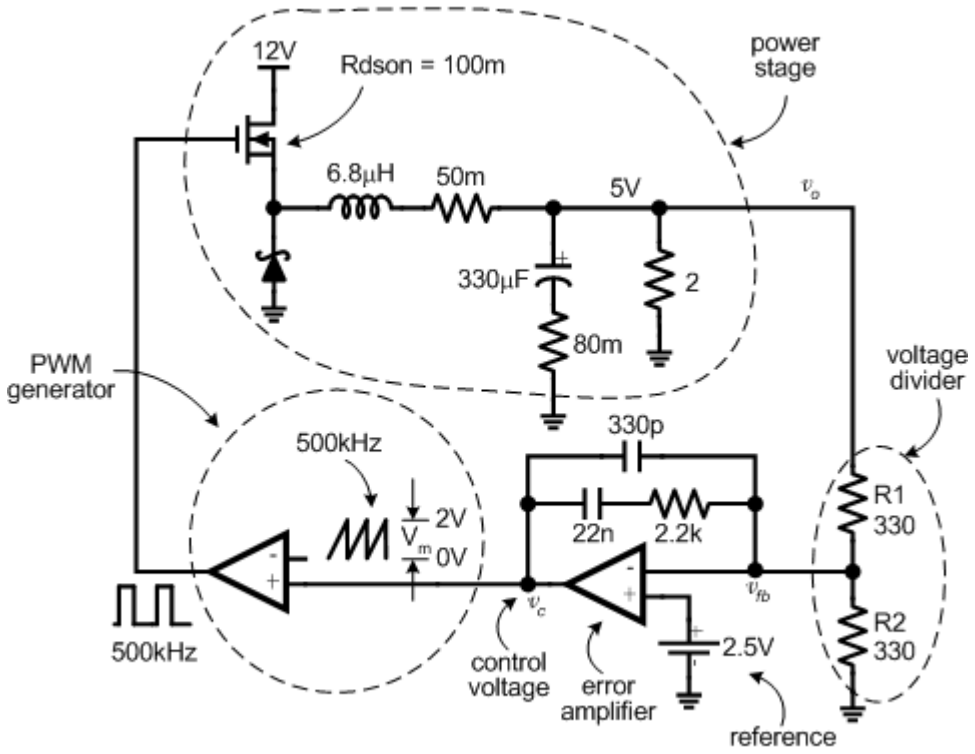
Open Loop



Closed Loop

Main Elements In A Closed-Loop Buck Regulator

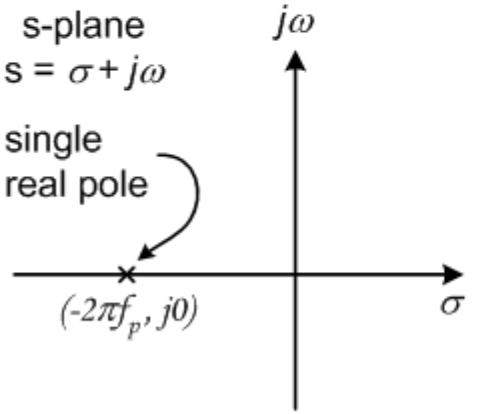
- In a voltage-mode PWM buck regulator, there are four main elements. The voltage divider, the error amplifier, the PWM generator and the power stage.

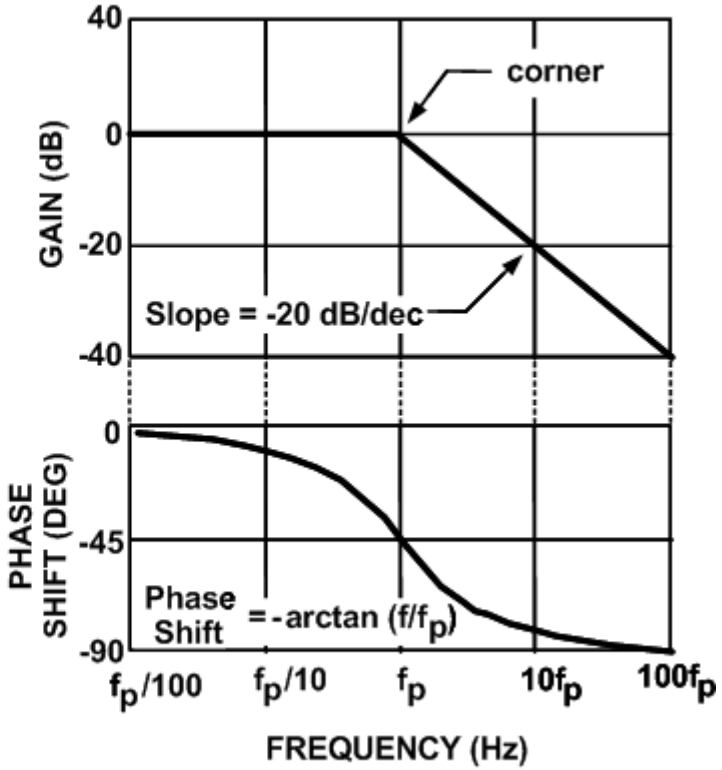


Review Of Poles And Zeros

- A pole is a root of a transfer function's denominator when the latter is made equal to zero.
- A single pole always has -45 degrees phase shift at its corner frequency. The total phase lag caused by a single pole is always less than 90 degrees.

transfer function containing a pole $\dfrac{1}{1+\dfrac{s}{2\pi \cdot f_p}}$

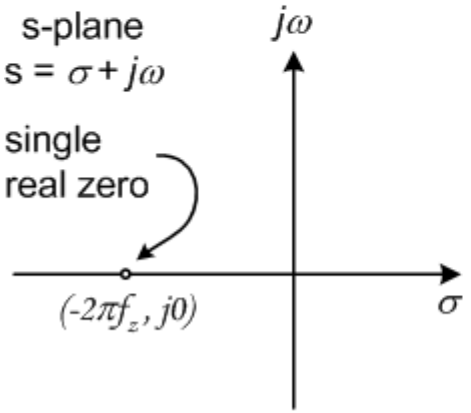


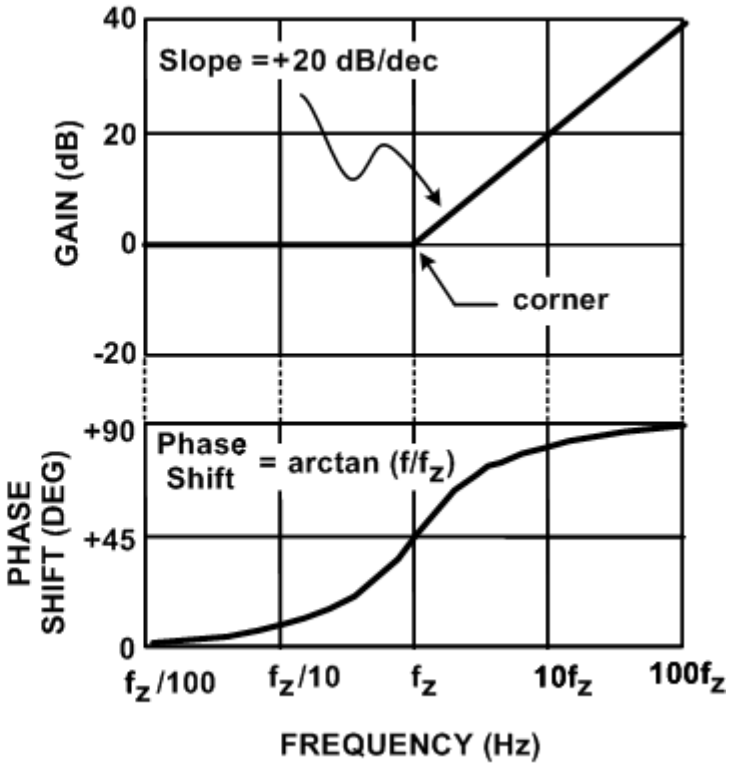


Review Of Poles And Zeros

- A zero is a root of a transfer function's numerator when the latter is made equal to zero.
- A single zero always has +45 degrees phase shift at its corner frequency. The total phase lead caused by a single zero is always less than 90 degrees.

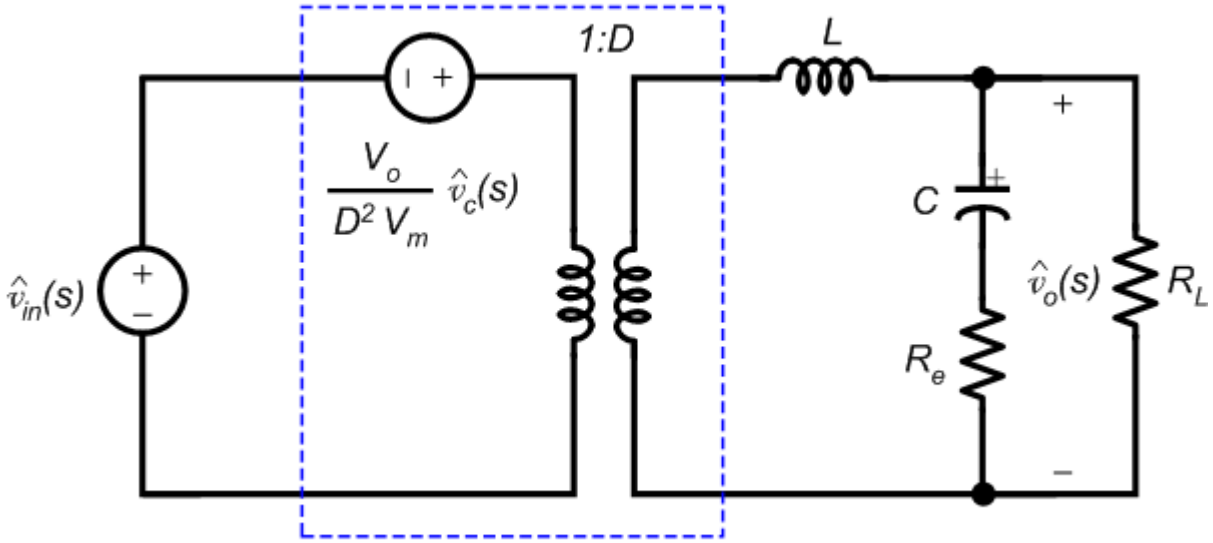
transfer function containing a zero $1+\frac{s}{2\pi \cdot f_z}$





Small-signal Model Of A Buck Regulator

- This model basically turns the power switches (i.e. the power MOSFET and diode) into a two-port network that consists of a voltage source and an ideal transformer, as indicated by the box in the figure. The rest of the circuit remains the same as it appeared in the original circuit diagram.
- From this small-signal model, we can immediately obtain two important transfer functions. (see next page)



Small-signal Model Of A Buck Regulator

- Control-to-output transfer function. This is obtained by fixing the input voltage and allowing the control voltage to vary.

$$G_c(s) = \frac{\hat{v}_o(s)}{\hat{v}_c(s)} = \frac{V_{in}(1+sCR_e)}{s^2LC(1+\frac{R_e}{R_L})+s(\frac{L}{R_L}+CR_e)+1} \cdot \frac{1}{V_m}$$

- Line-to-output transfer function. This is obtained by fixing the control voltage and allowing the input voltage to vary.

$$G_a(s) = \frac{\hat{v}_o(s)}{\hat{v}_{in}(s)} = \frac{D(1+sCR_e)}{s^2LC(1+\frac{R_e}{R_L})+s(\frac{L}{R_L}+CR_e)+1}$$

- The two transfer functions have the same zero and poles. They are only different by a coefficient.

Small-signal Model Of A Buck Regulator

- The zero is often called the "ESR zero" since it only exists when output capacitors have a finite ESR (Equivalent Series Resistance). The corner frequency of the ESR zero is:

$$f_z = \frac{1}{2\pi \cdot CR_e}$$

So the ESR zero frequency is inversely proportional to the output capacitance and to the ESR.

Small-signal Model Of A Buck Regulator

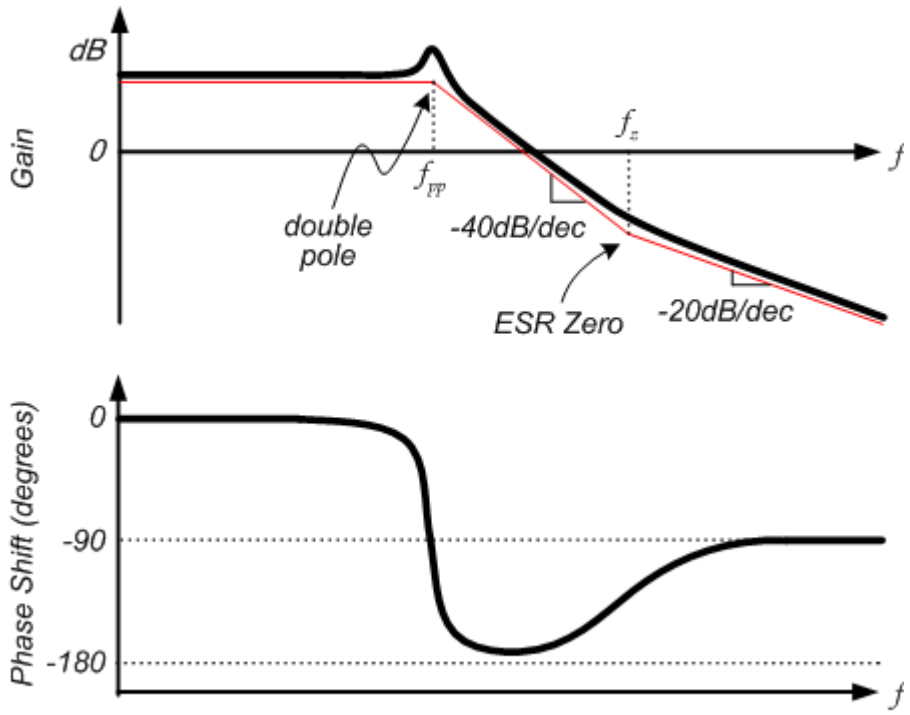
- The poles in the two transfer functions are complex conjugates in the s-plane and are often called a "double pole." Notice that a double pole is not two poles having the same corner frequency in the Bode plot. In our case, the double pole is the result of the LC filter at the output stage. A double pole has a "damping factor" characteristic. A smaller damping factor will cause at the corner frequency more peaking in the gain plot and more rapid increase of phase delay, making it more difficult to stabilize the loop.

- The corner frequency of the double pole is:

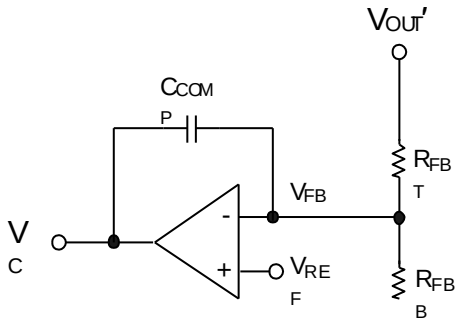
$$f_{pp} = \frac{1}{2\pi\sqrt{LC(1+\frac{R_e}{R_L})}} \approx \frac{1}{2\pi\sqrt{LC}}$$

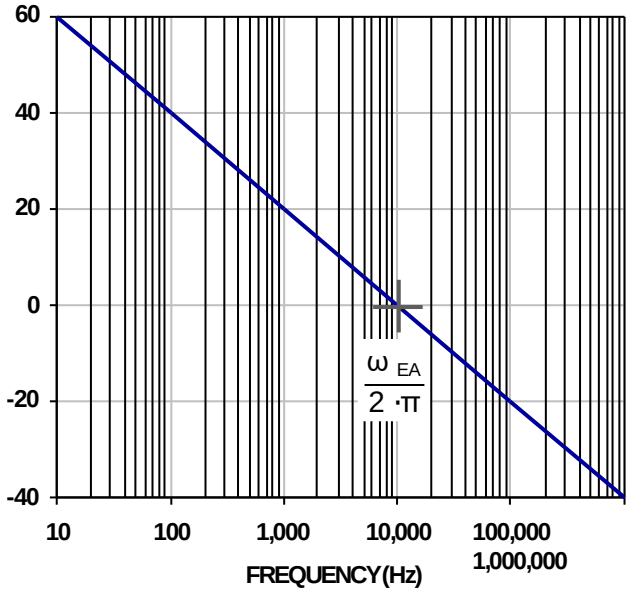
Small-signal Model Of A Buck Regulator

- The Bode plot of the control-to-output transfer function is:



Type I 误差放大器

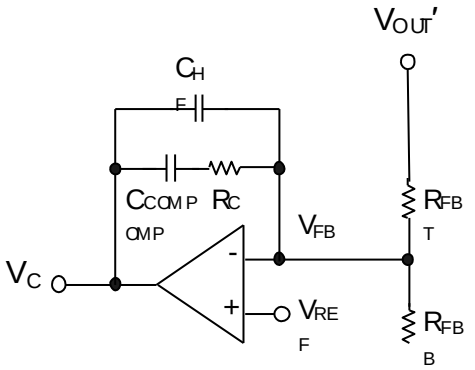


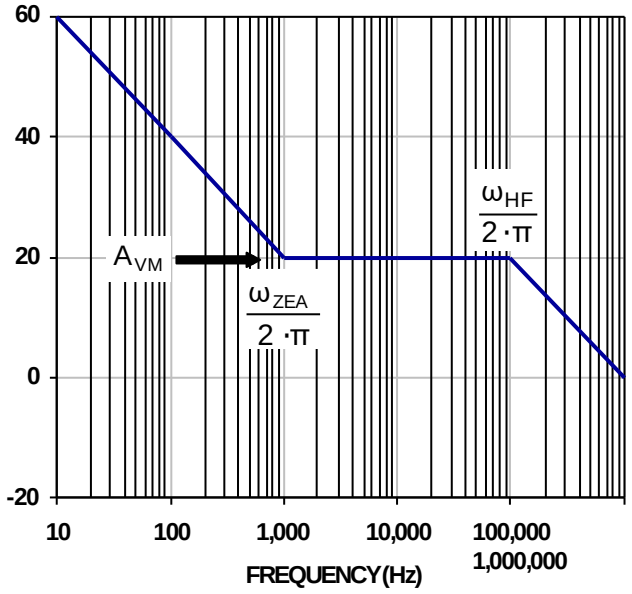


$$\omega_{EA} = \frac{1}{R_{FBT} \cdot C_{COMP}}$$

$$\frac{\hat{v}_C}{\hat{v}_{OUT}'} \approx -\frac{\omega_{EA}}{s}$$

Type II 误差放大器





$$A_{VM} \approx \frac{R_{COMP}}{R_{FBT}}$$

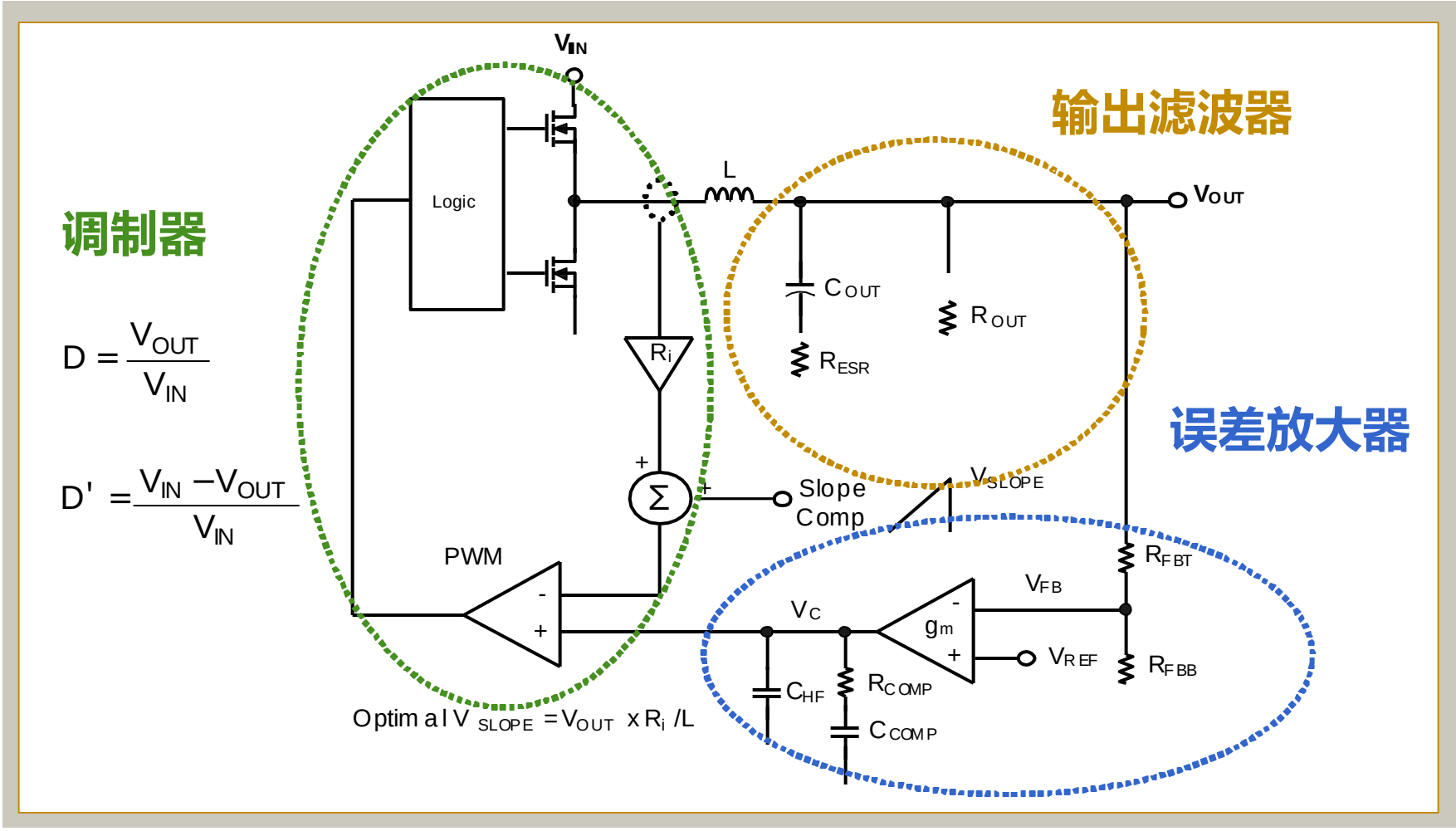
$$\omega_{ZEA} = \frac{1}{R_{COMP} \cdot C_{COMP}}$$

$$\omega_{HF} \approx \frac{1}{R_{COMP} \cdot C_{HF}}$$

假设 $C_{COMP} >> C_{HF}$

$$\frac{\hat{v}_C}{\hat{v}_{OUT}} \approx -A_{VM} \cdot \frac{1 + \frac{\omega_{ZEA}}{s}}{1 + \frac{s}{\omega_{HF}}}$$

电流模式降压模型



电流模式降压 – Type II 补偿

- 选择一个大的 R_{FBT} 阻值，介于 2 kΩ 和 200 kΩ 之间
- 找出调制器跨导（单位： A/V）
- 选择一个目标带宽，通常为 $F_{SW}/10$
- 设定中频段增益 A_{VM} 以实现目标带宽： $\omega_C = 2 \cdot \pi \cdot F_C$
- 设定 $\omega_{ZEA} = 1/10$ 目标交越频率： $\omega_{ZEA} = \omega_C/10$
- 设定 $\omega_{HF} =$ ESR 零点频率：$\omega_{HF} = \omega_Z$

$$G_m(mod) = \frac{1}{R_i} \qquad A_{VM} = \frac{\omega_C \cdot C_O}{G_m(mod)}$$

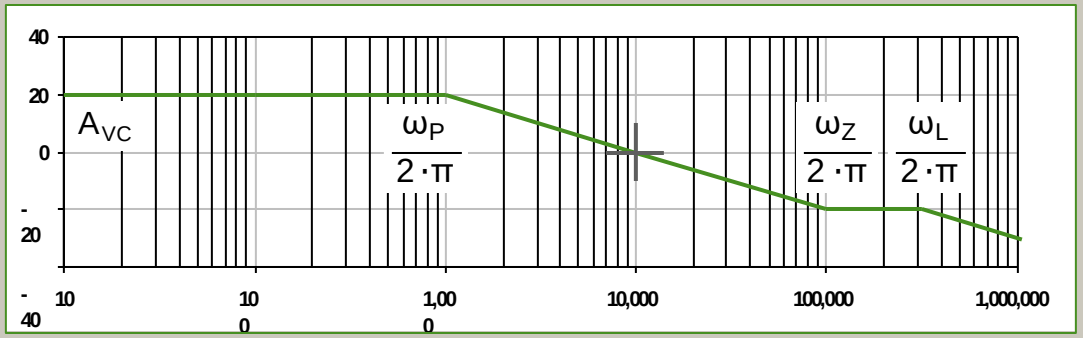
$$R_{COMP} = A_{VM} \cdot R_{FBT} \qquad \text{或：} \qquad R_{COMP} = \frac{A_{VM}}{g_m \cdot K_{FB}}$$

$$C_{COMP} = \frac{1}{\omega_{ZEA} \cdot R_{COMP}} \qquad C_{HF} = \frac{1}{\omega_{HF} \cdot R_{COMP}}$$

电流模式降压控制环路

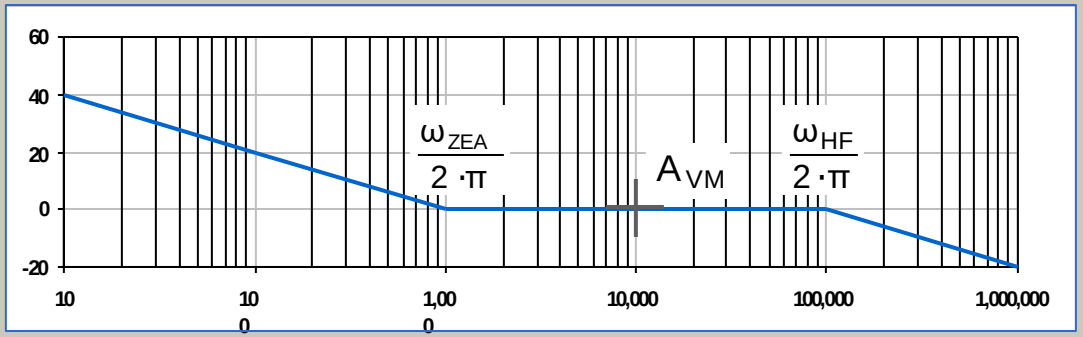
功率级

$$\frac{\hat{v}_{OUT}}{\hat{v}_C} \approx A_{VC} \cdot \frac{1+\frac{s}{\omega_Z}}{\left(1+\frac{s}{\omega_P}\right)\cdot\left(1+\frac{s}{\omega_L}\right)}$$



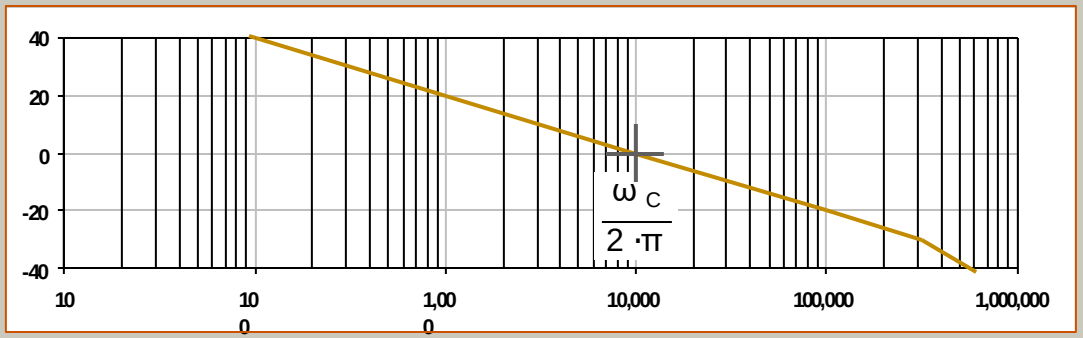
误差放大器

$$\frac{\hat{v}_C}{\hat{v}_{OUT}'} \approx -A_{VM} \cdot \frac{1+\frac{\omega_{ZEA}}{s}}{1+\frac{s}{\omega_{HF}}}$$

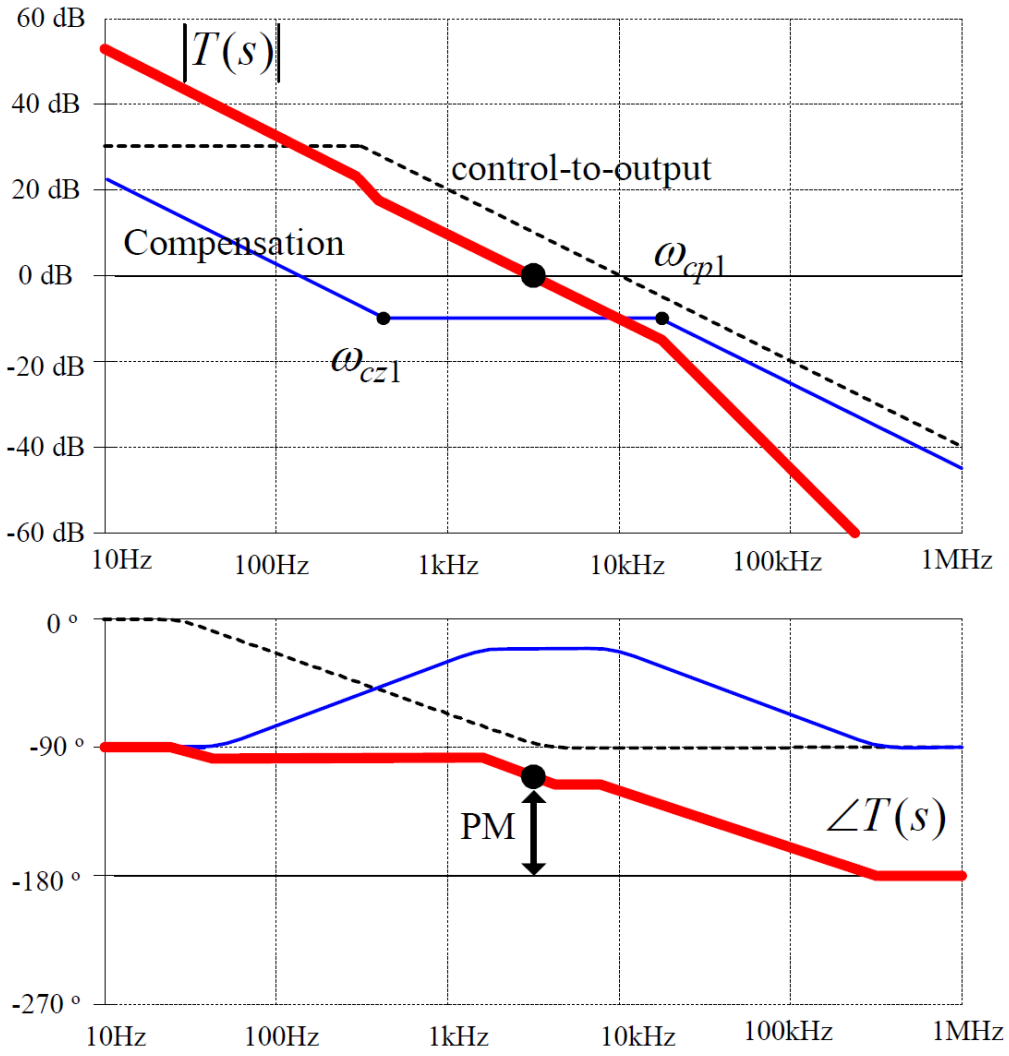


控制环路

$$\frac{\hat{v}_{OUT}}{\hat{v}_{OUT}'} = \frac{\hat{v}_{OUT}}{\hat{v}_C} \cdot \frac{\hat{v}_C}{\hat{v}_{OUT}'}$$



电流模式降压 – Type II 补偿



Control Architecture Summary

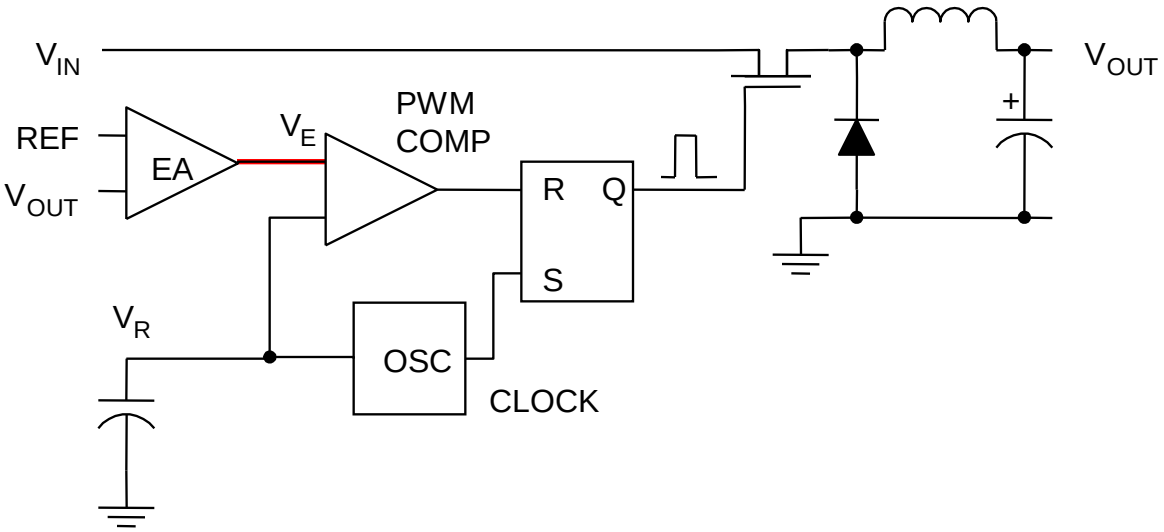
Linear Control Architectures

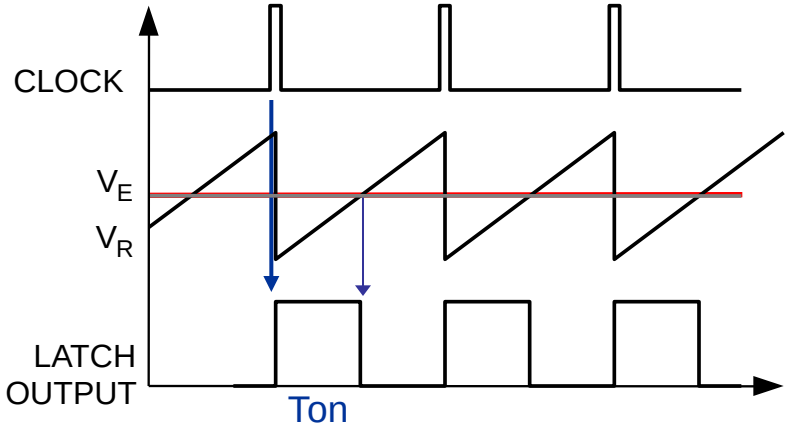
- Voltage Mode
- Voltage Mode with Voltage Feed Forward
- Current Mode
- Emulated Current Mode

Non- Linear Control Architectures

- Hysteretic
- Constant On Time (COT)
- COT with Emulated Ripple Mode
- D-CAP™ (Adaptive On Time)
- D-CAP+™
- D-CAP2™
- DCS™ (Direct Control w/ Seamless transition to Power Save Mode)

Voltage Mode Control





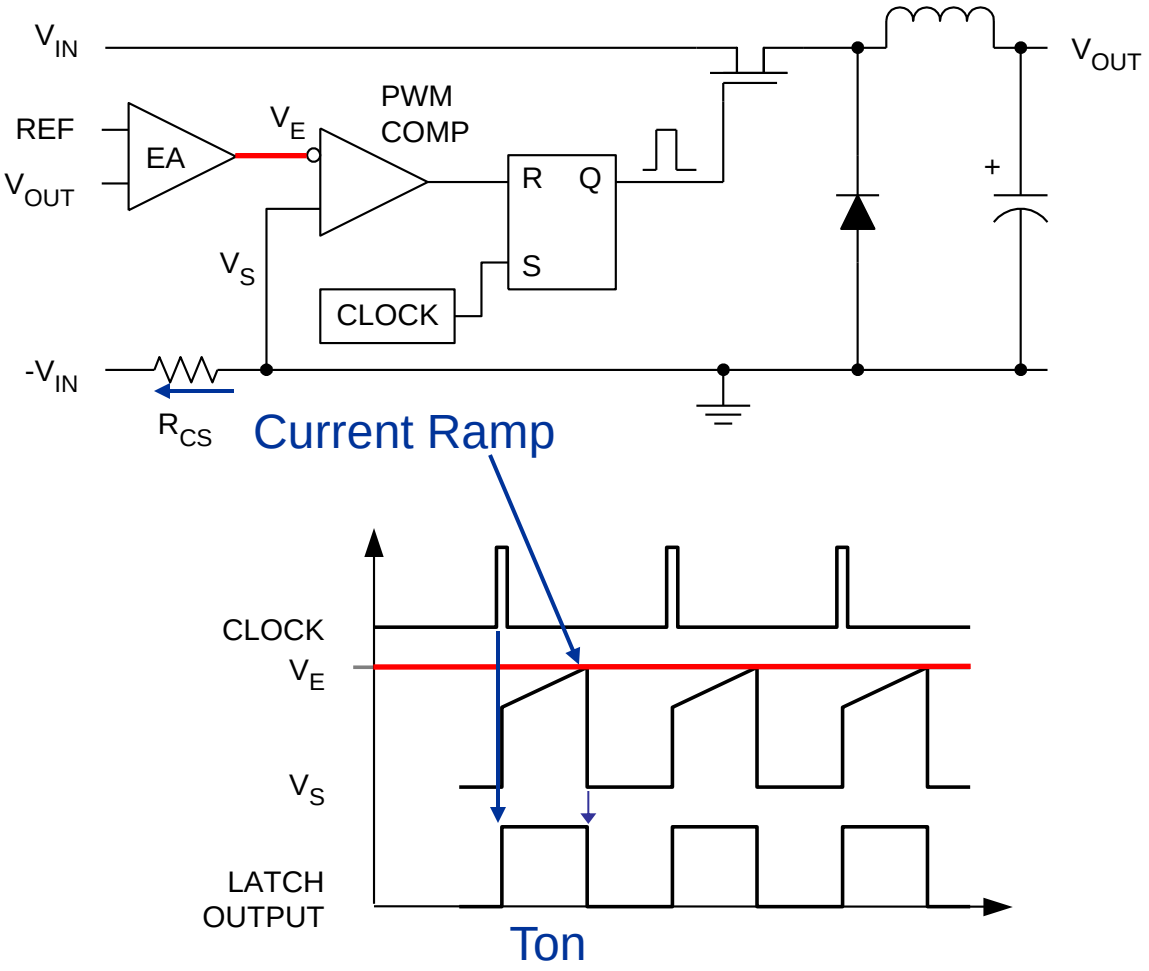
ADVANTAGES

- Single feedback loop
- Good noise margin
- Voltage regulation is independent of current

DISADVANTAGES

- High BW EA required
- More difficult double-pole compensation
- Output caps affect compensation
- V_{IN} affects loop gain

Current Mode Control



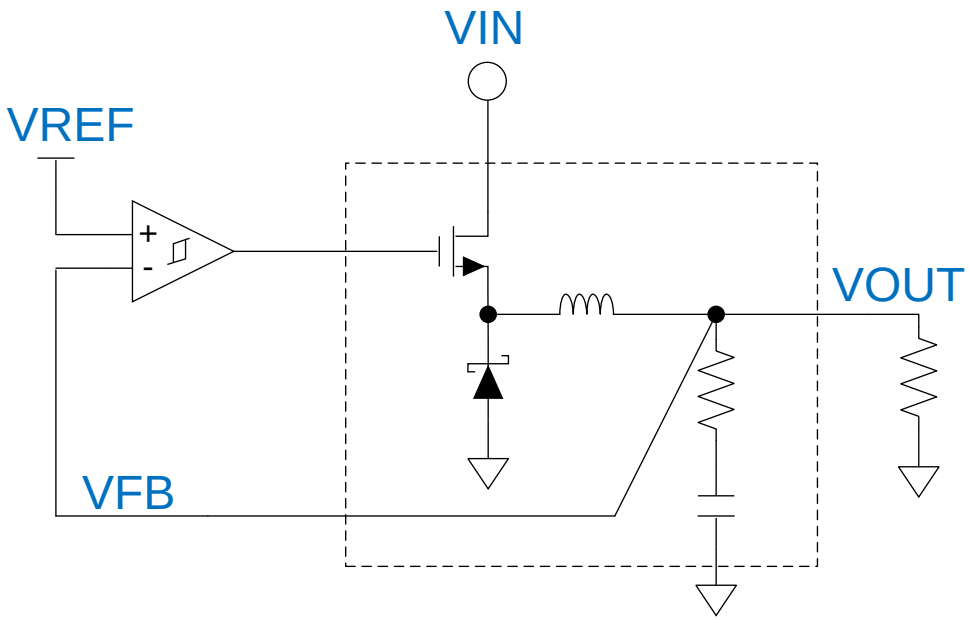
ADVANTAGES

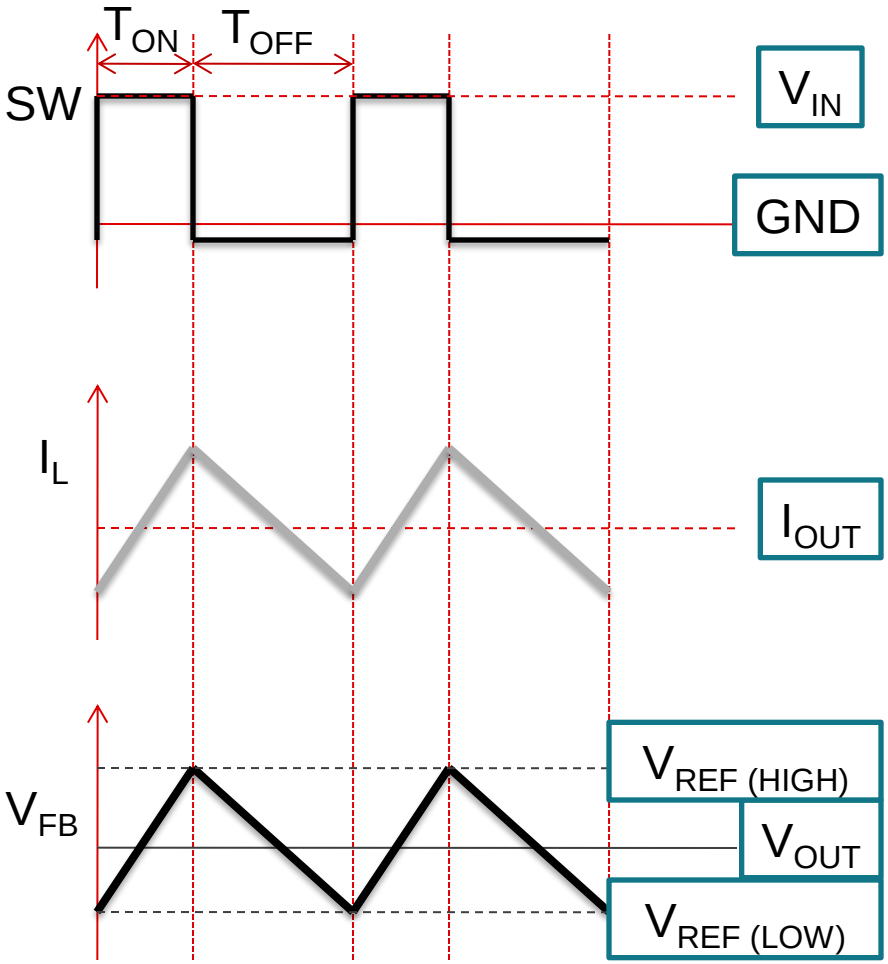
- Fast response to output current changes
- Single-pole compensation
- Inherent current limiting
- Inherent feed forward
- Multiple phase current sharing possible

DISADVANTAGES

- Two feedback loops if a current amplifier is used
- Need for slope compensation
- Current limit “tail”
- Noise sensitivity due to leading edge current spike

Hysteretic Control Scheme





TON - Terminated by VFB > $V_{REF\ (HIGH)}$

TOFF - Terminated by VFB < $V_{REF\ (LOW)}$

Hysteretic Control

ADVANTAGES

- Simple controls - bang/bang system
- No loop compensation
- Fastest response to load changes

DISADVANTAGES

- Variable switching frequency
- Needs protection against magnetic saturation
- Requires some output ripple - ESR
- Sensitive to output noise
- Circuit delays limit maximum frequency