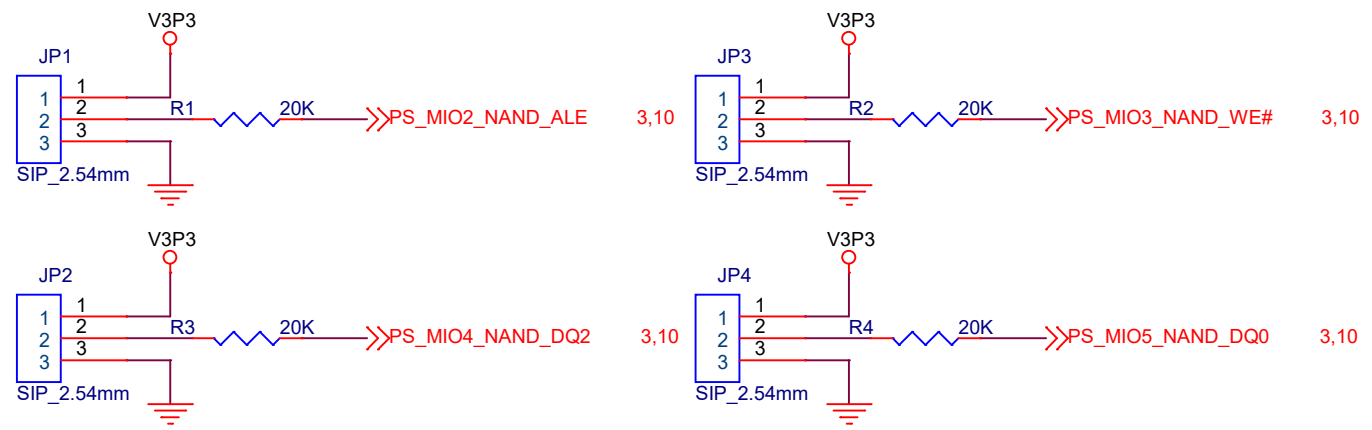
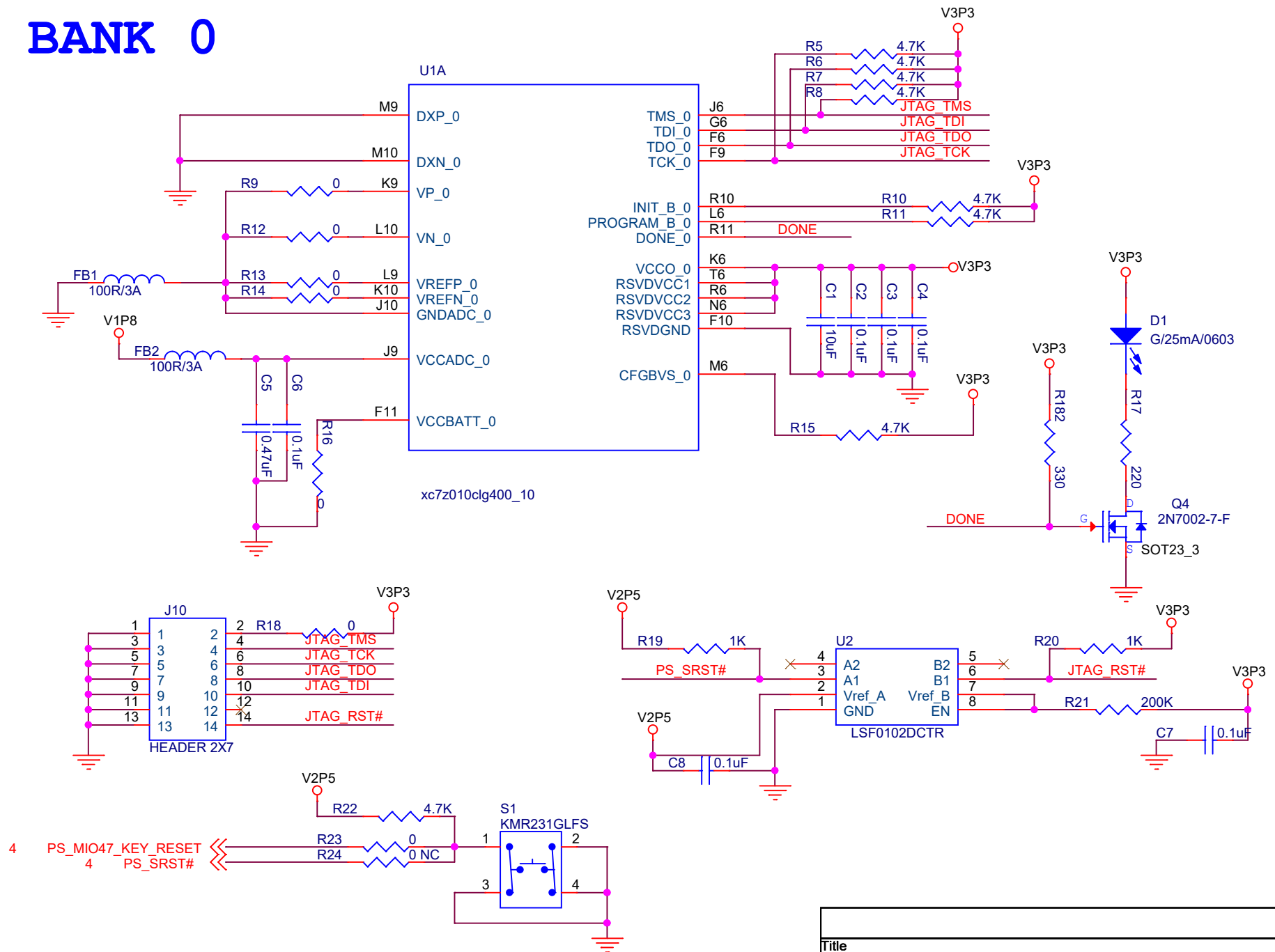


Boot Mode Select



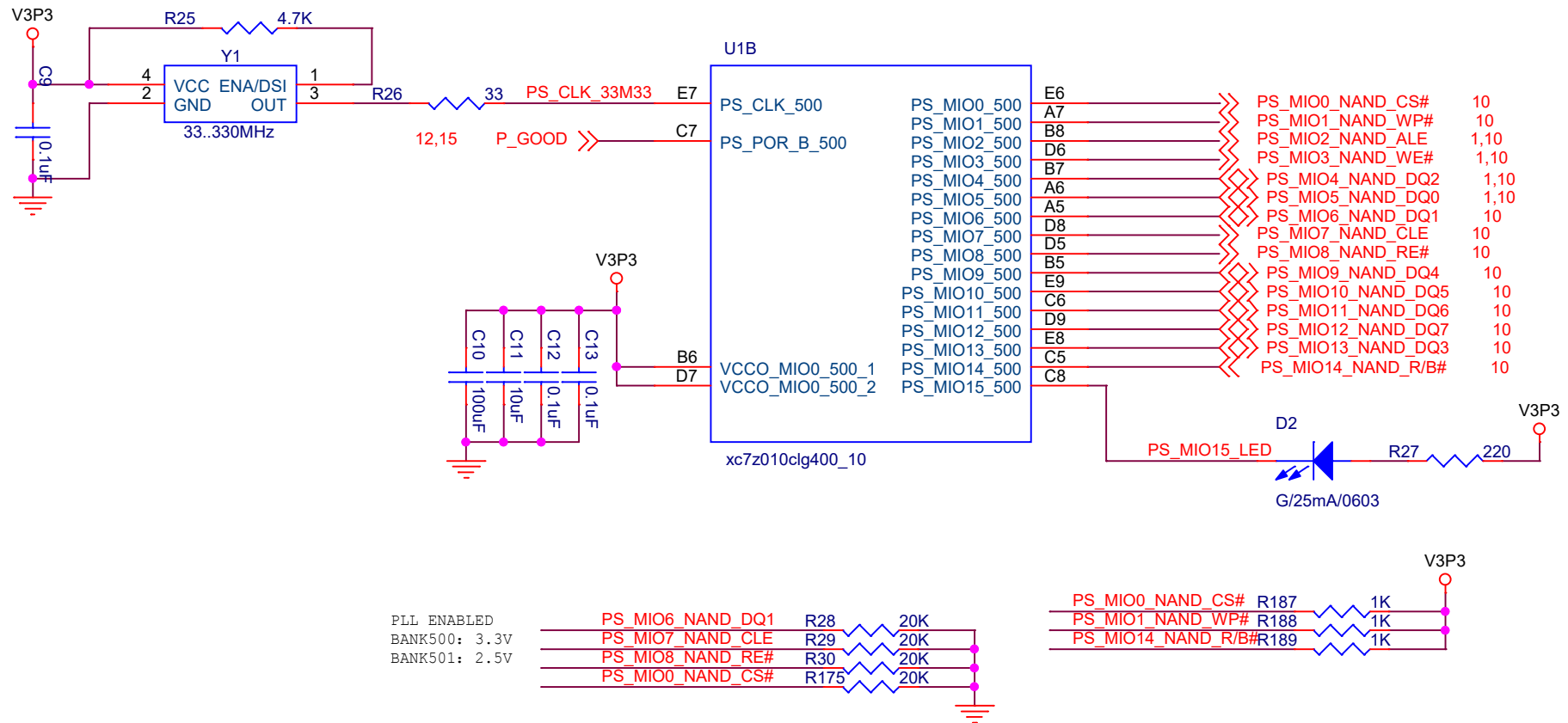
| Boot Mode | JP1 | JP2 | JP3 | JP4 |
|--------------|-----|-----|-----|-----|
| Cascade JTAG | 0 | 0 | 0 | 0 |
| TF Card | 0 | 1 | 0 | 1 |
| QSPI Flash | 0 | 0 | 0 | 1 |
| NOR Flash | 0 | 0 | 1 | 0 |
| NAND Flash | 0 | 1 | 0 | 0 |

BANK 0



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BANK 500

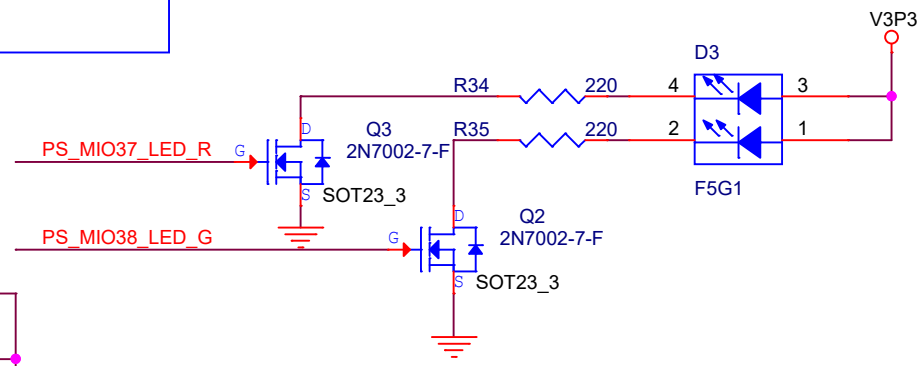
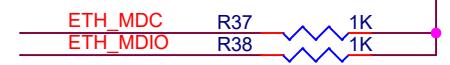
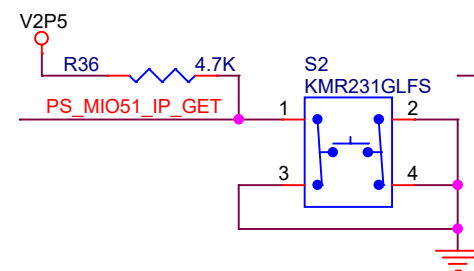
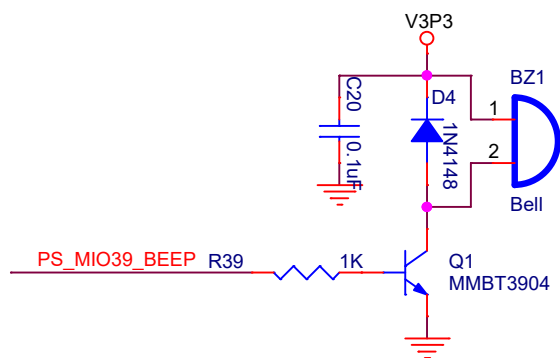
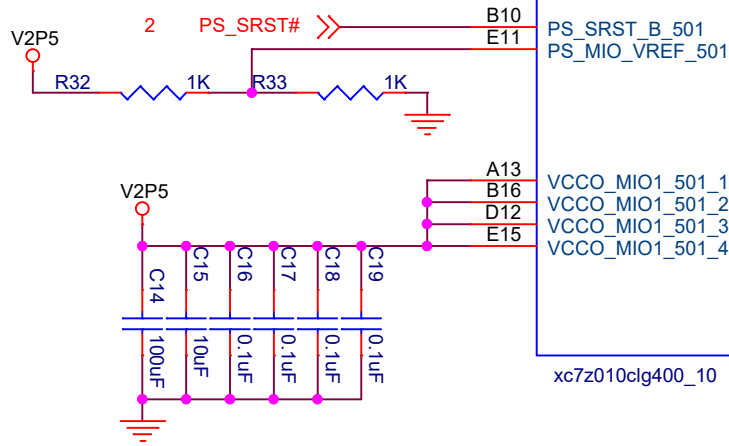
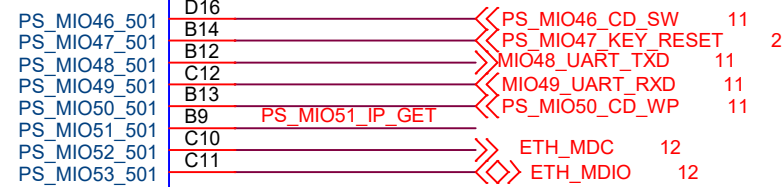
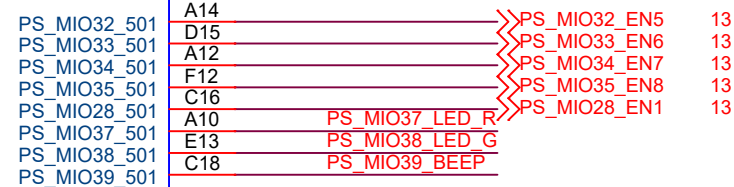
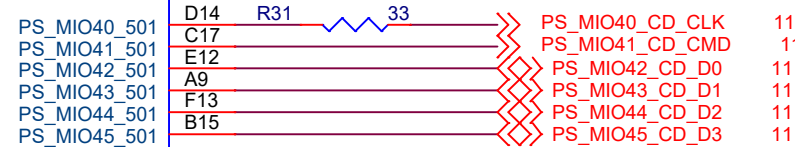
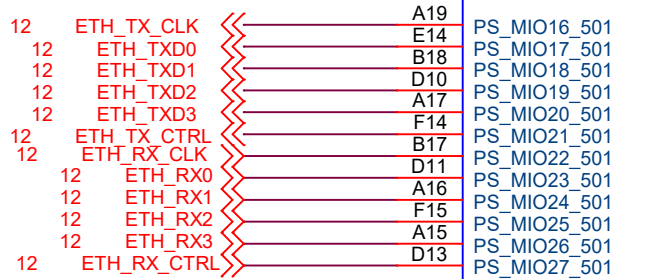


PLL ENABLED
BANK500: 3.3V
BANK501: 2.5V

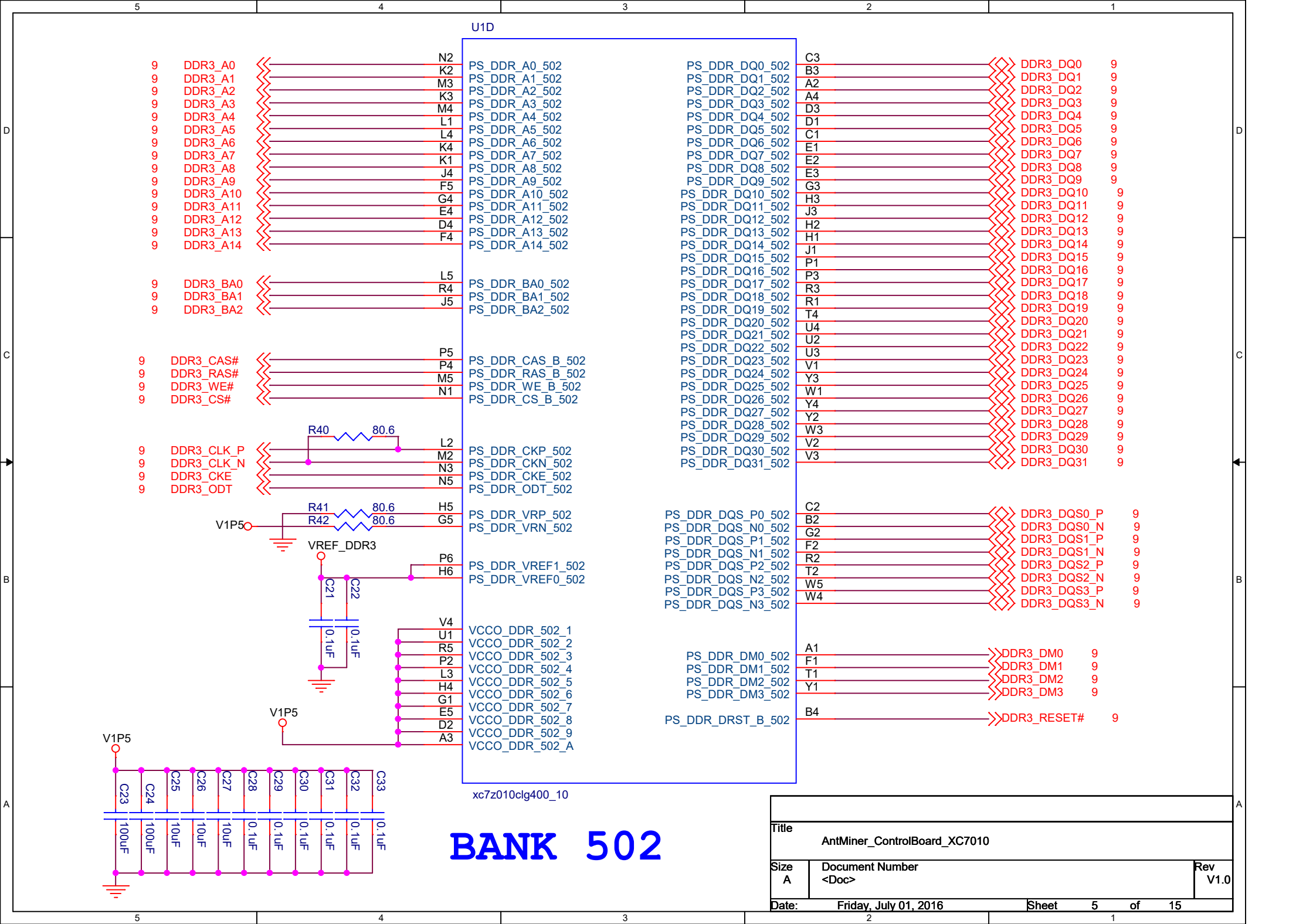
During an SD memory card boot sequence, the BootROM reads the logic level on the MIO pin 0 as an SD Card Detect. MIO pin 0 must be Low during the SDIO boot process.

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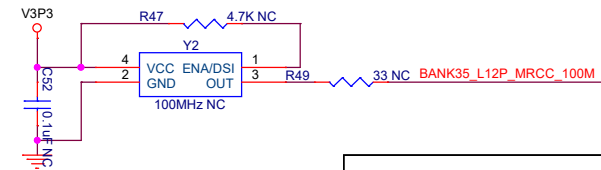
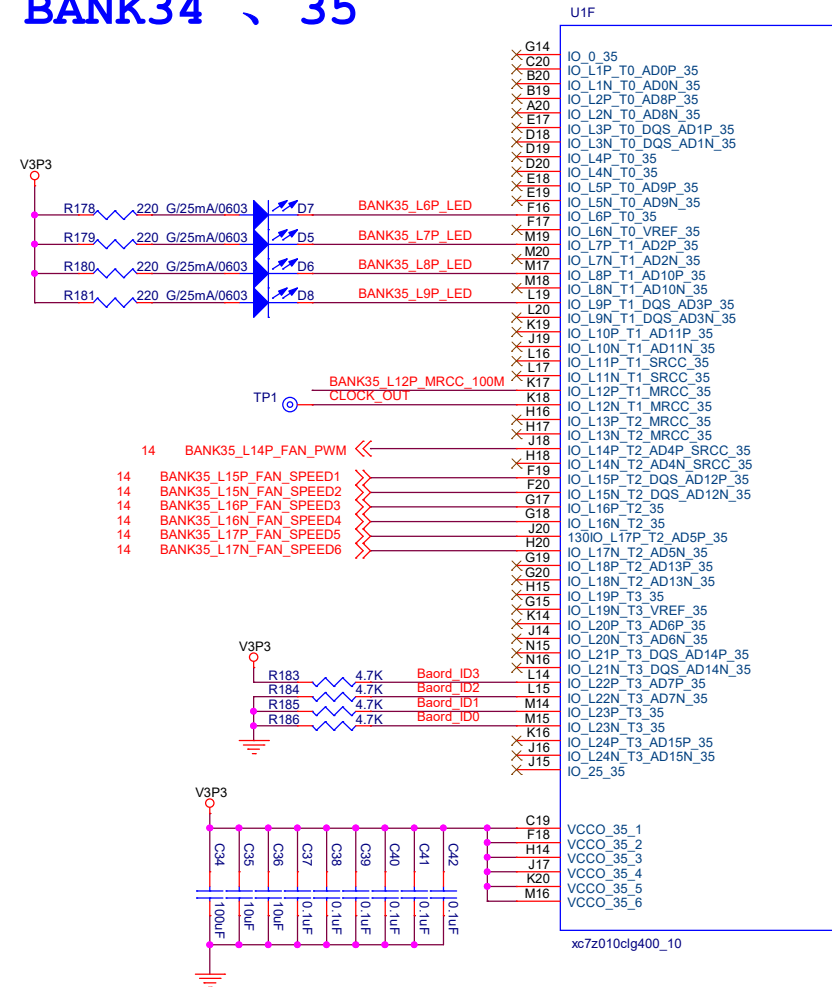
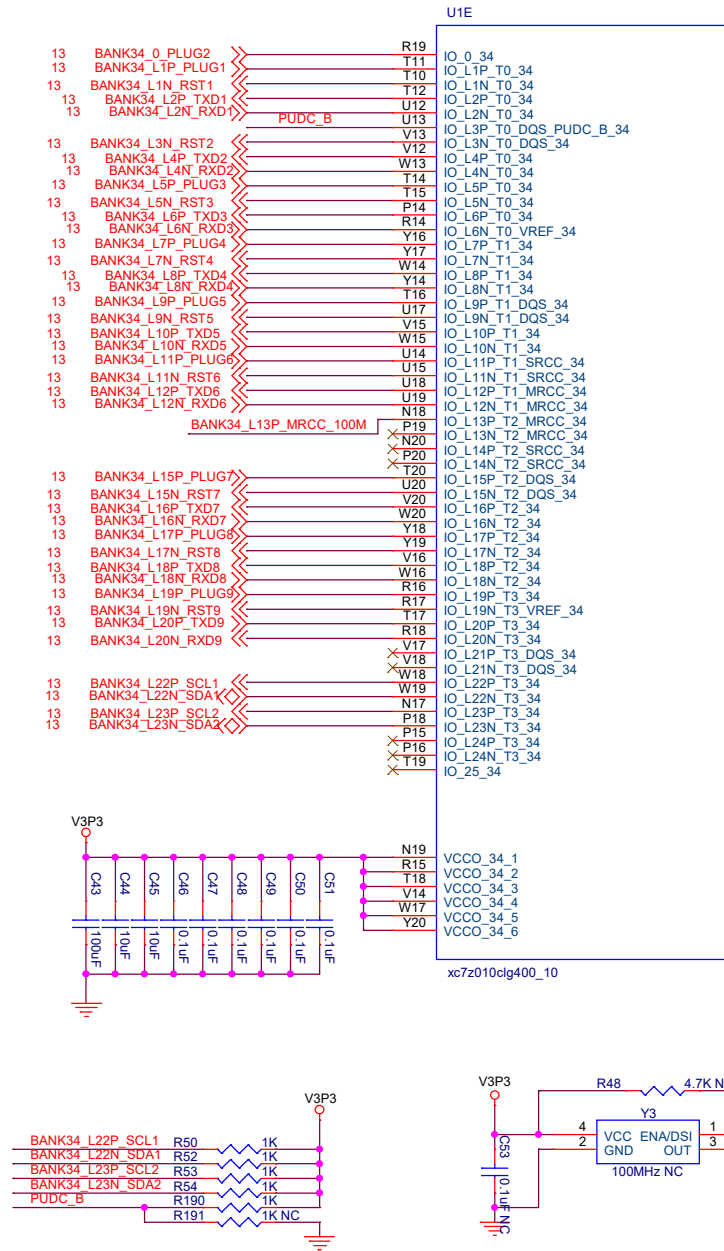
BANK 501



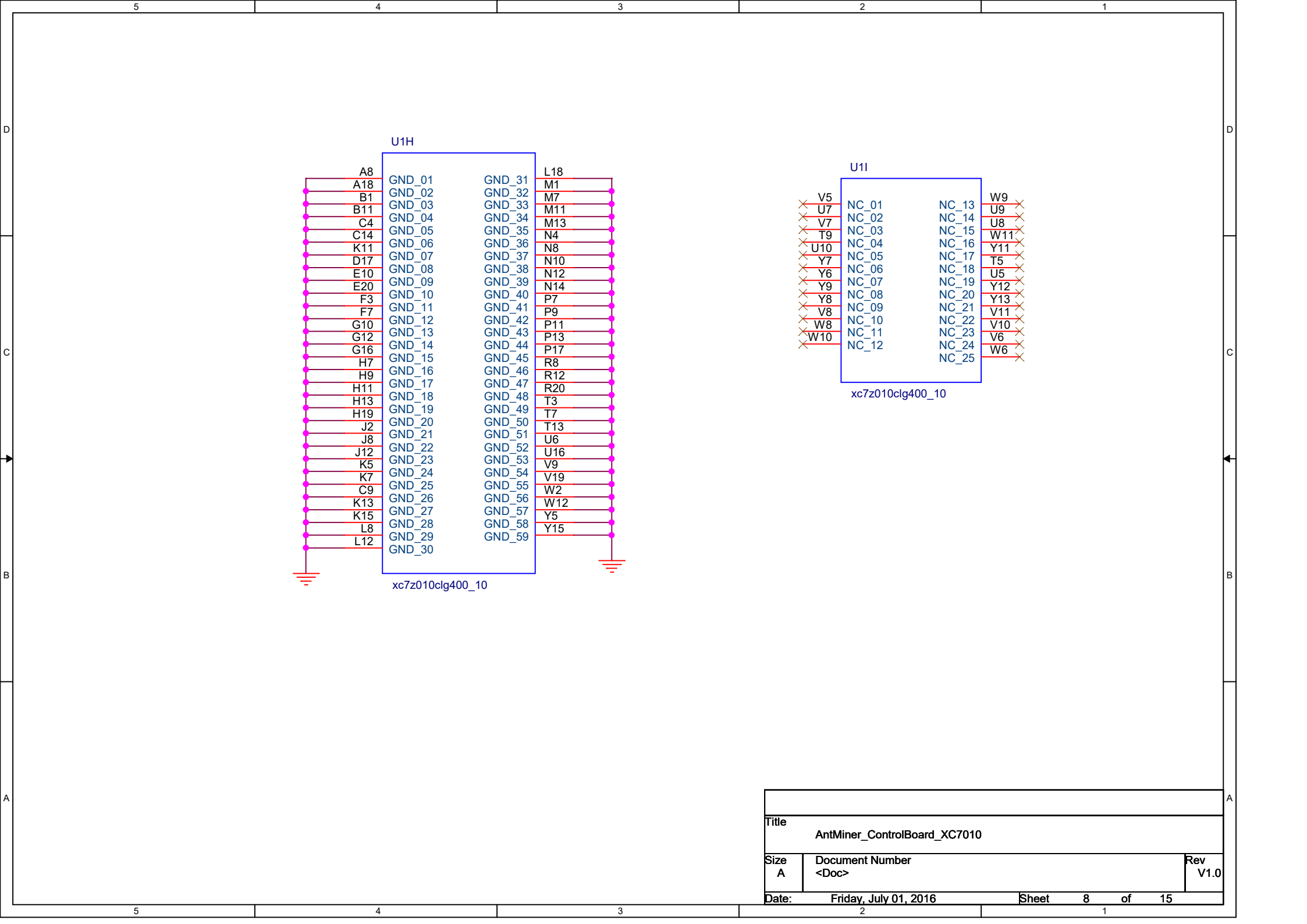
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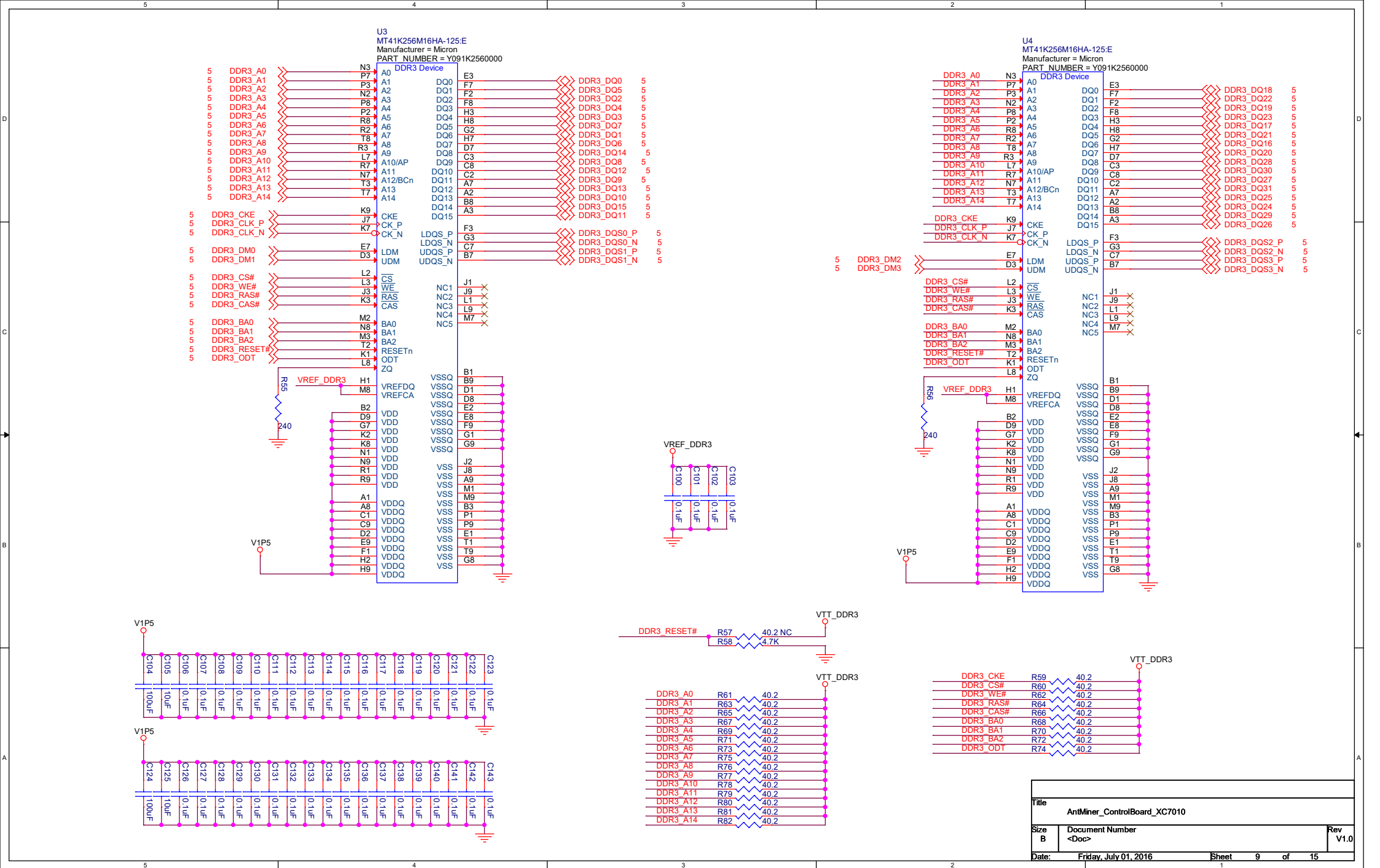
PL BANK34 、 35



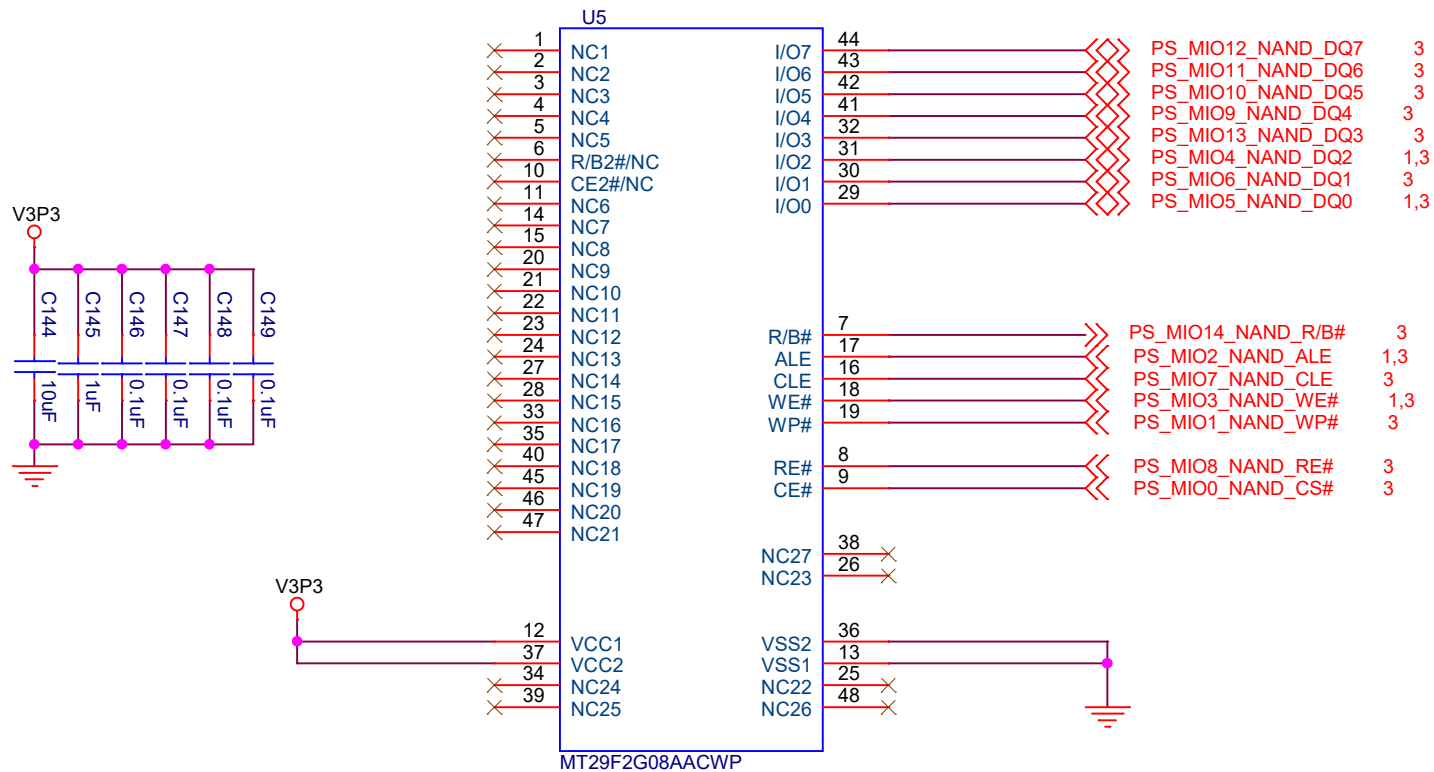
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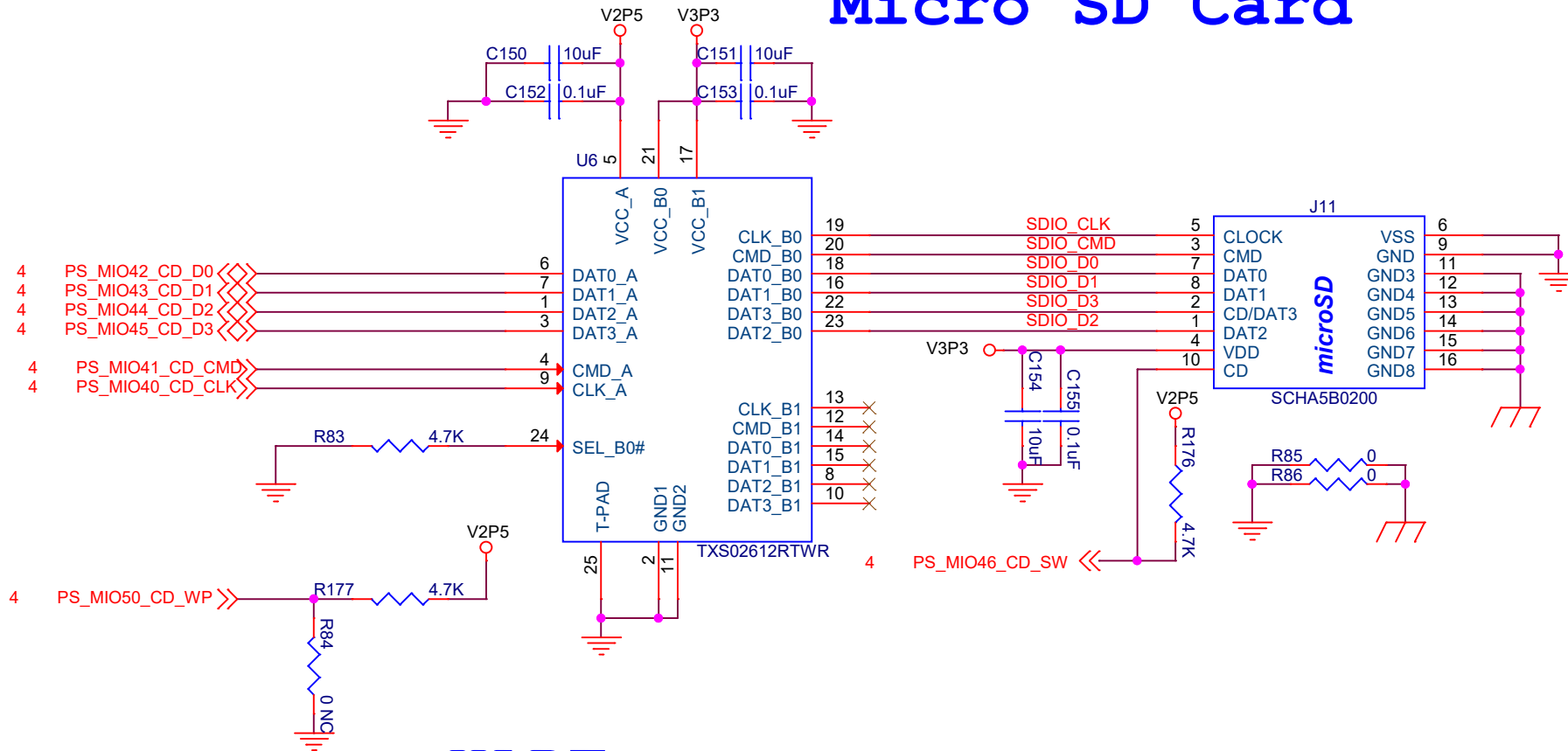


NAND FLASH

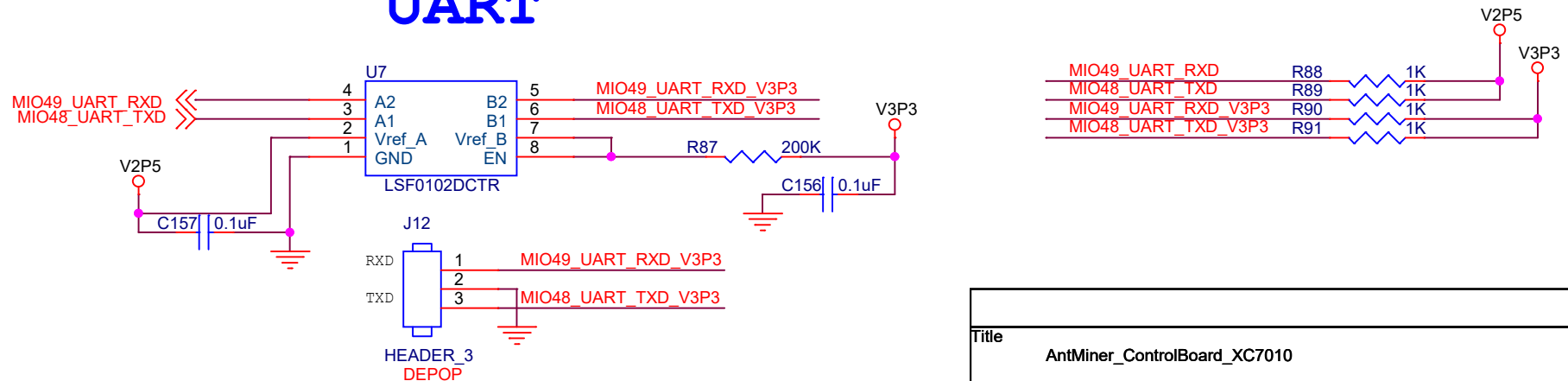


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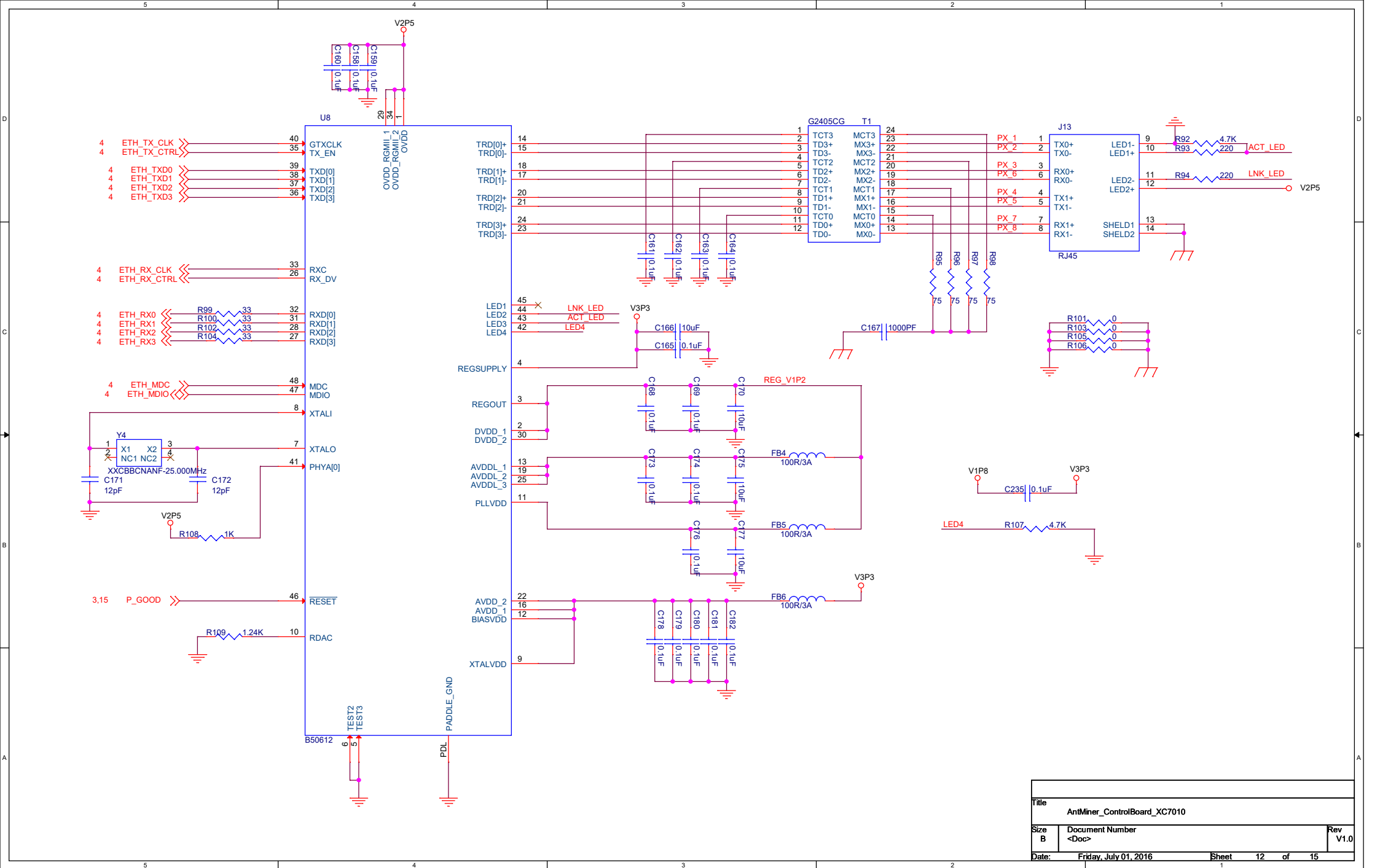
Micro SD Card



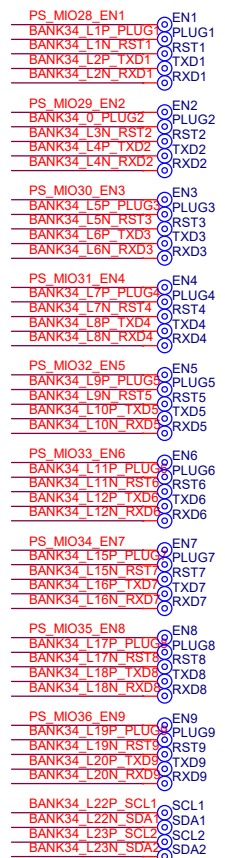
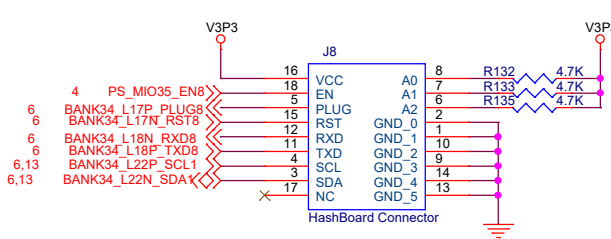
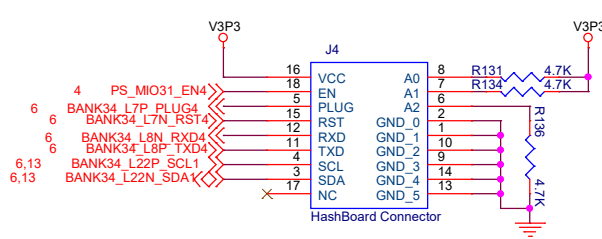
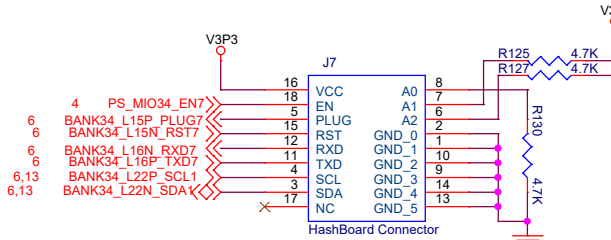
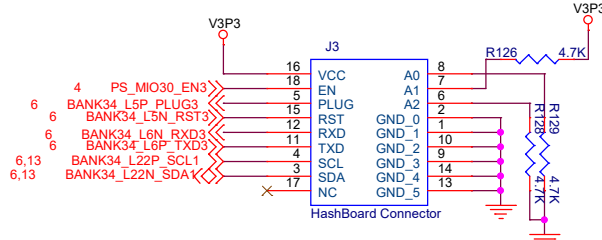
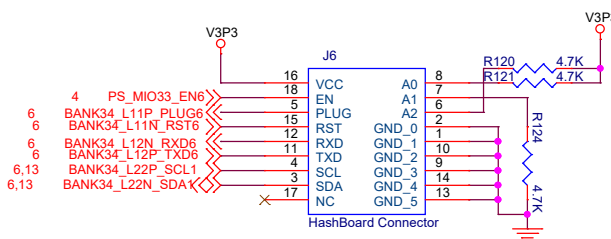
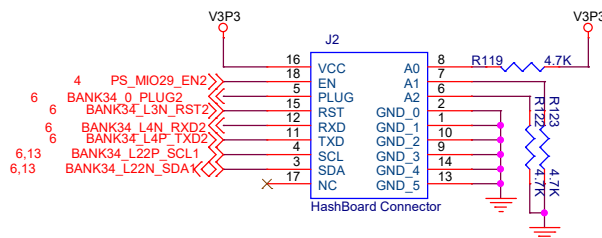
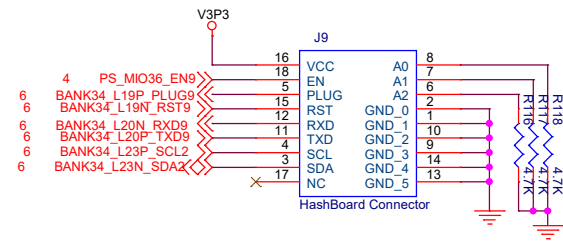
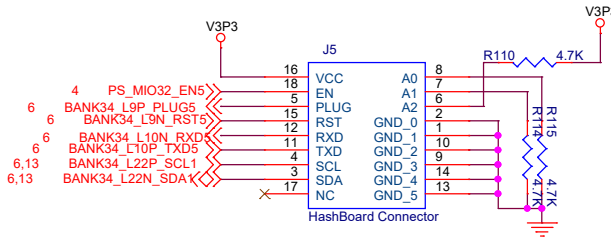
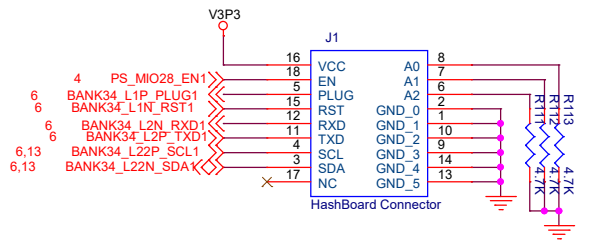
UART



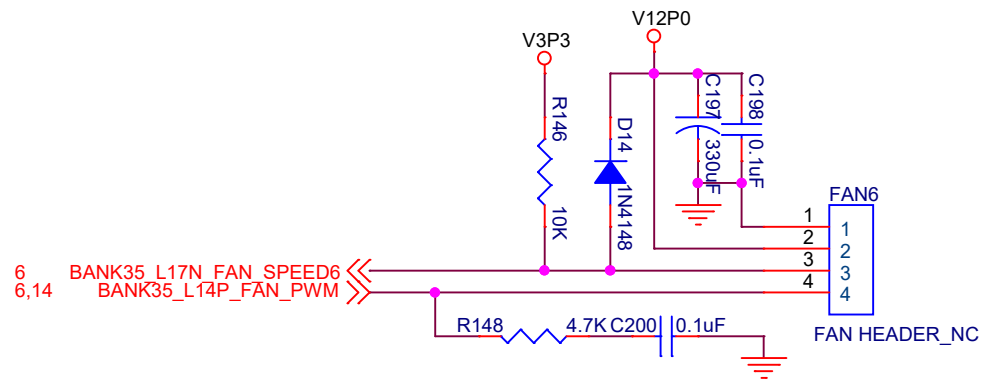
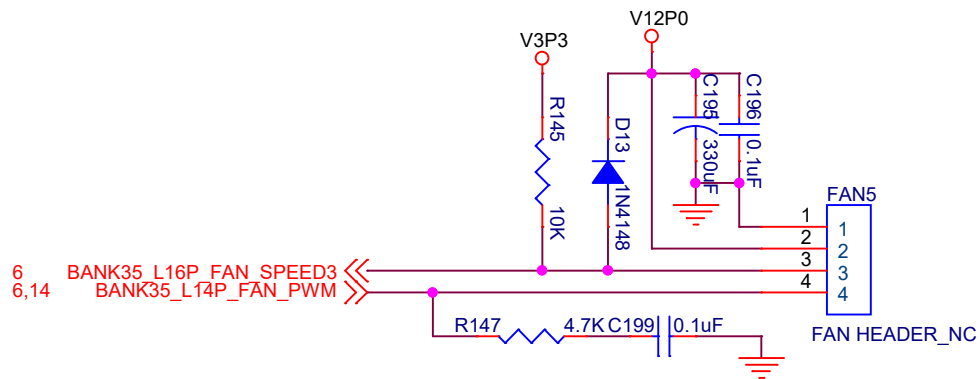
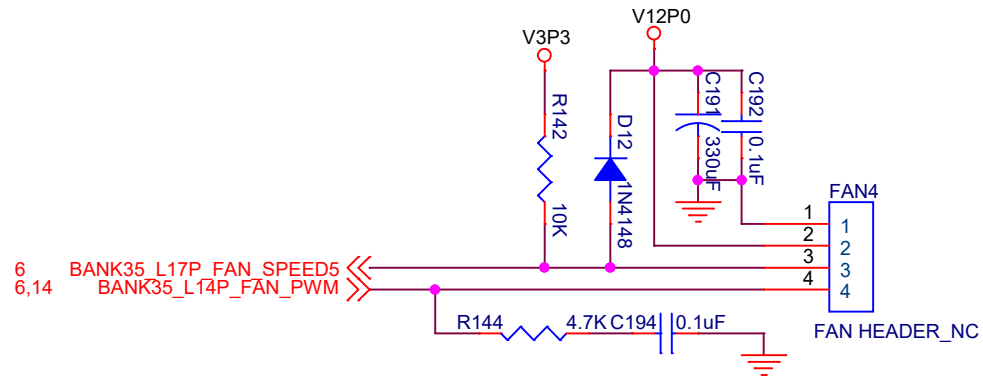
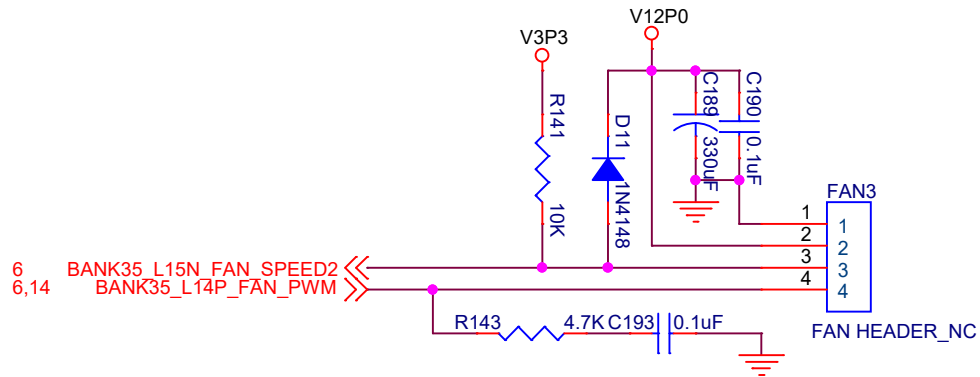
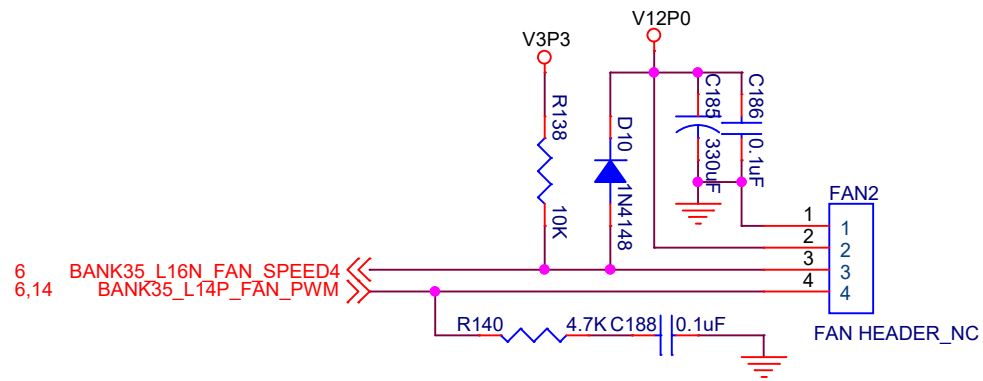
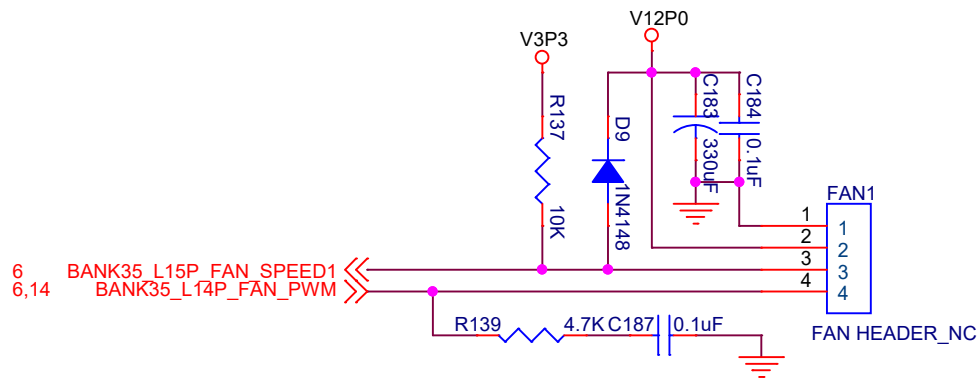
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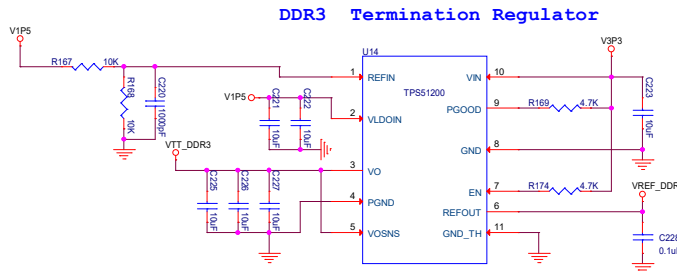
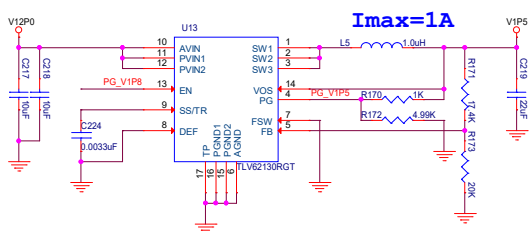
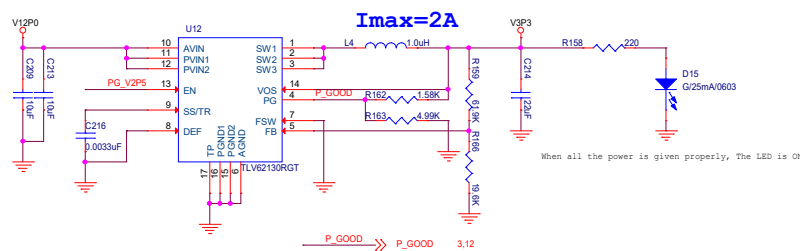
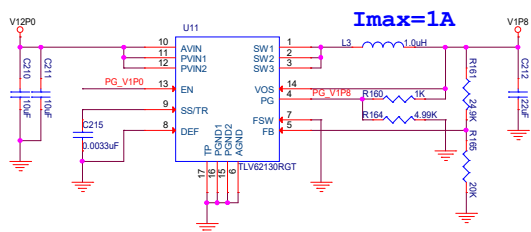
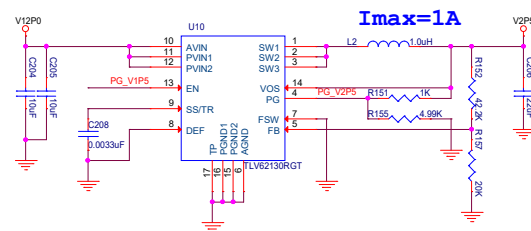
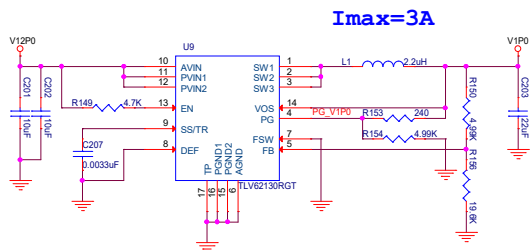
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12V Power CONN

