
STM32
CubeMX

1. Description

1.1. Project

Project Name	cube
Board Name	custom
Generated with:	STM32CubeMX 6.8.1
Date	05/15/2023

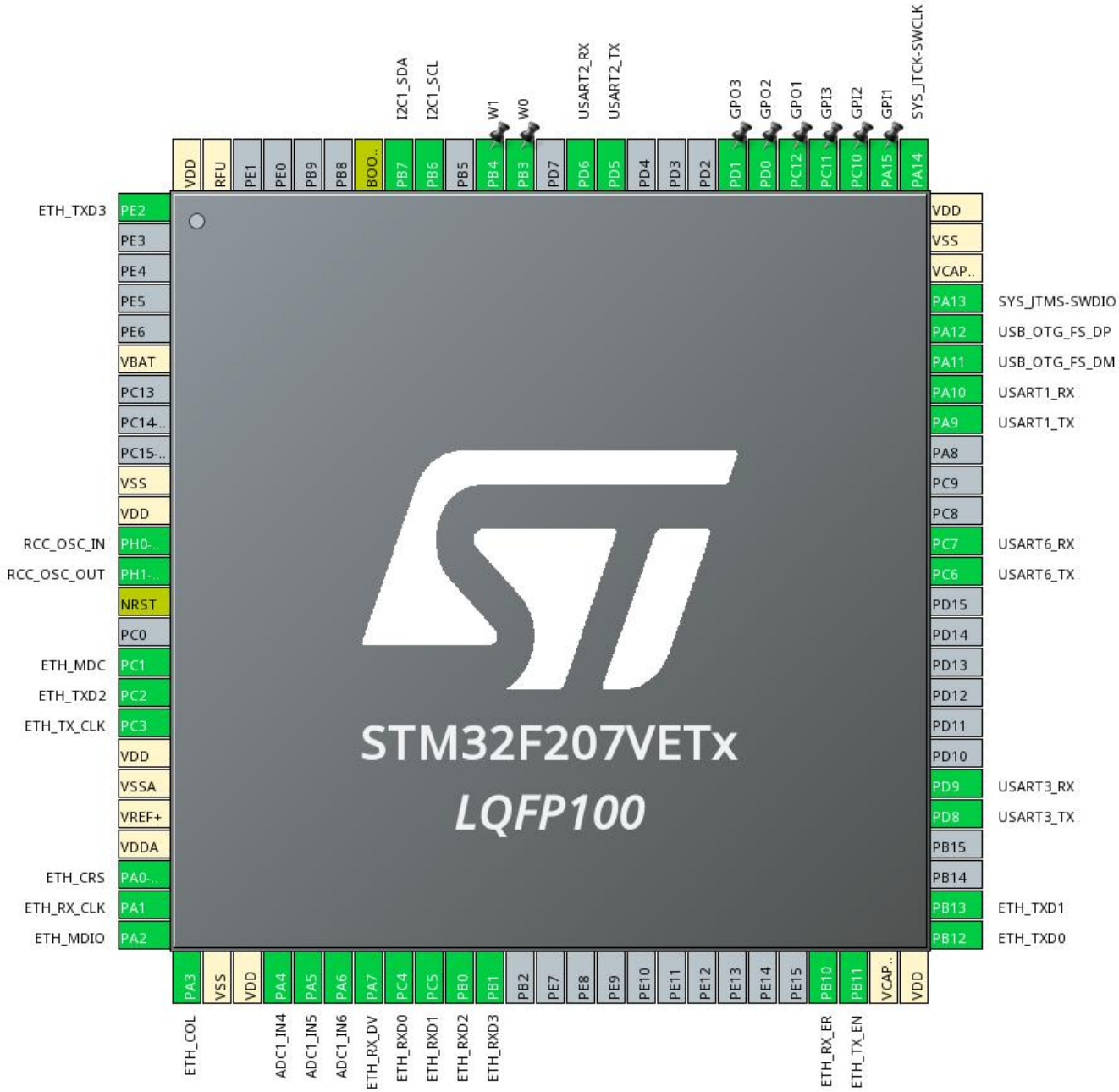
1.2. MCU

MCU Series	STM32F2
MCU Line	STM32F2x7
MCU name	STM32F207VETx
MCU Package	LQFP100
MCU Pin number	100

1.3. Core(s) information

Core(s)	Arm Cortex-M3

2. Pinout Configuration



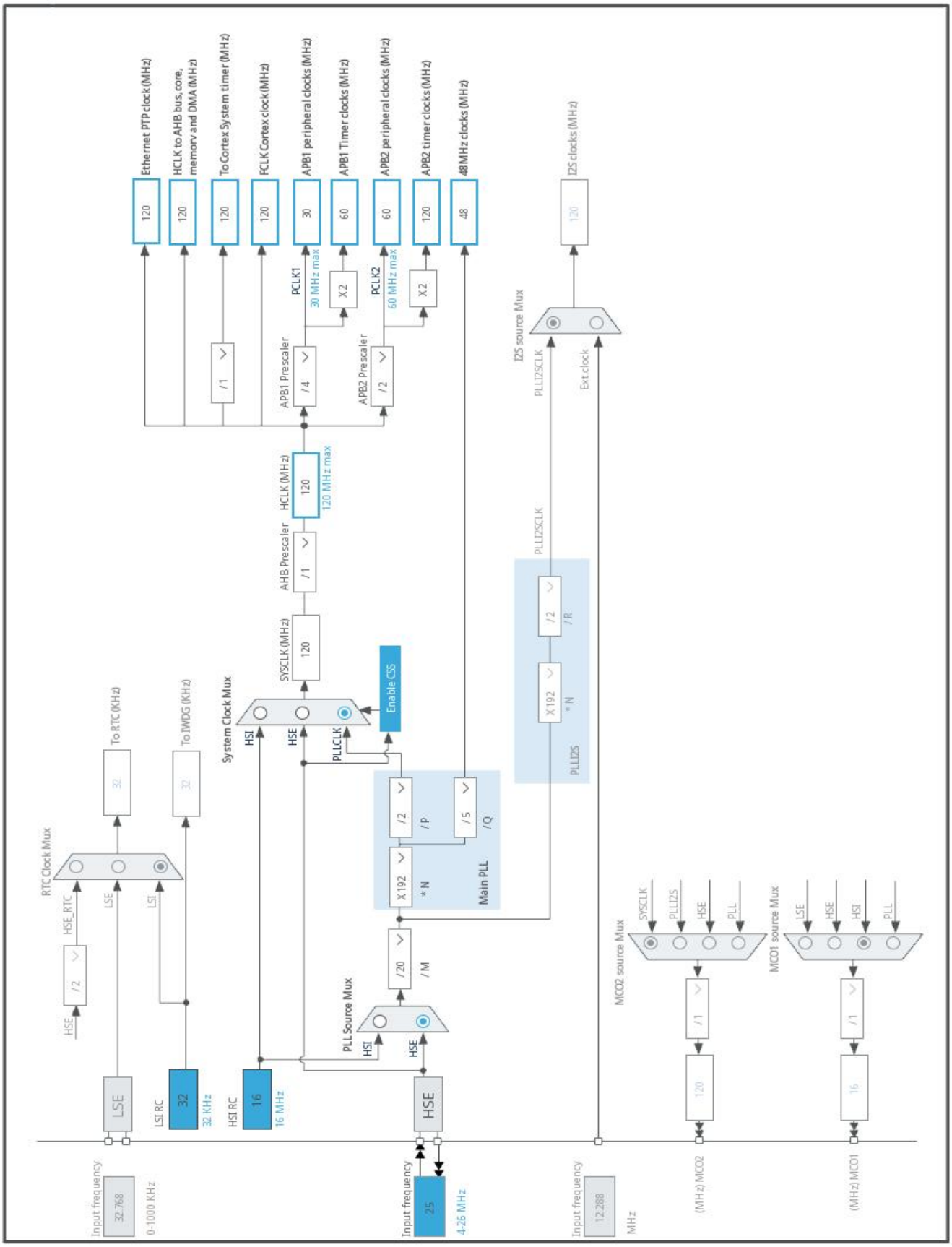
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	ETH_TXD3	
6	VBAT	Power		
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
16	PC1	I/O	ETH_MDC	
17	PC2	I/O	ETH_TXD2	
18	PC3	I/O	ETH_TX_CLK	
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	ETH_CRS	
24	PA1	I/O	ETH_RX_CLK	
25	PA2	I/O	ETH_MDIO	
26	PA3	I/O	ETH_COL	
27	VSS	Power		
28	VDD	Power		
29	PA4	I/O	ADC1_IN4	
30	PA5	I/O	ADC1_IN5	
31	PA6	I/O	ADC1_IN6	
32	PA7	I/O	ETH_RX_DV	
33	PC4	I/O	ETH_RXD0	
34	PC5	I/O	ETH_RXD1	
35	PB0	I/O	ETH_RXD2	
36	PB1	I/O	ETH_RXD3	
47	PB10	I/O	ETH_RX_ER	
48	PB11	I/O	ETH_TX_EN	
49	VCAP_1	Power		
50	VDD	Power		
51	PB12	I/O	ETH_TXD0	
52	PB13	I/O	ETH_TXD1	
55	PD8	I/O	USART3_TX	
56	PD9	I/O	USART3_RX	

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
63	PC6	I/O	USART6_TX	
64	PC7	I/O	USART6_RX	
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
70	PA11	I/O	USB_OTG_FS_DM	
71	PA12	I/O	USB_OTG_FS_DP	
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
77	PA15 *	I/O	GPIO_Input	GPI1
78	PC10 *	I/O	GPIO_Input	GPI2
79	PC11 *	I/O	GPIO_Input	GPI3
80	PC12 *	I/O	GPIO_Output	GPO1
81	PD0 *	I/O	GPIO_Output	GPO2
82	PD1 *	I/O	GPIO_Output	GPO3
86	PD5	I/O	USART2_TX	
87	PD6	I/O	USART2_RX	
89	PB3 *	I/O	GPIO_Output	W0
90	PB4 *	I/O	GPIO_Output	W1
92	PB6	I/O	I2C1_SCL	
93	PB7	I/O	I2C1_SDA	
94	BOOT0	Boot		
99	RFU	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	cube
Project Folder	/home/zbigniewo/work/Repositories/pille/cube
Toolchain / IDE	Makefile
Firmware Package Name and Version	STM32Cube FW_F2 V1.9.3
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3	MX_I2C1_Init	I2C1
4	MX_USART1_UART_Init	USART1
5	MX_USART2_UART_Init	USART2
6	MX_USART3_UART_Init	USART3
7	MX_USART6_UART_Init	USART6
8	MX_LWIP_Init	LWIP
9	MX_USB_DEVICE_Init	USB_DEVICE
10	MX_ADC1_Init	ADC1

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F2
Line	STM32F2x7
MCU	STM32F207VETx
Datasheet	DS6329_Rev15

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

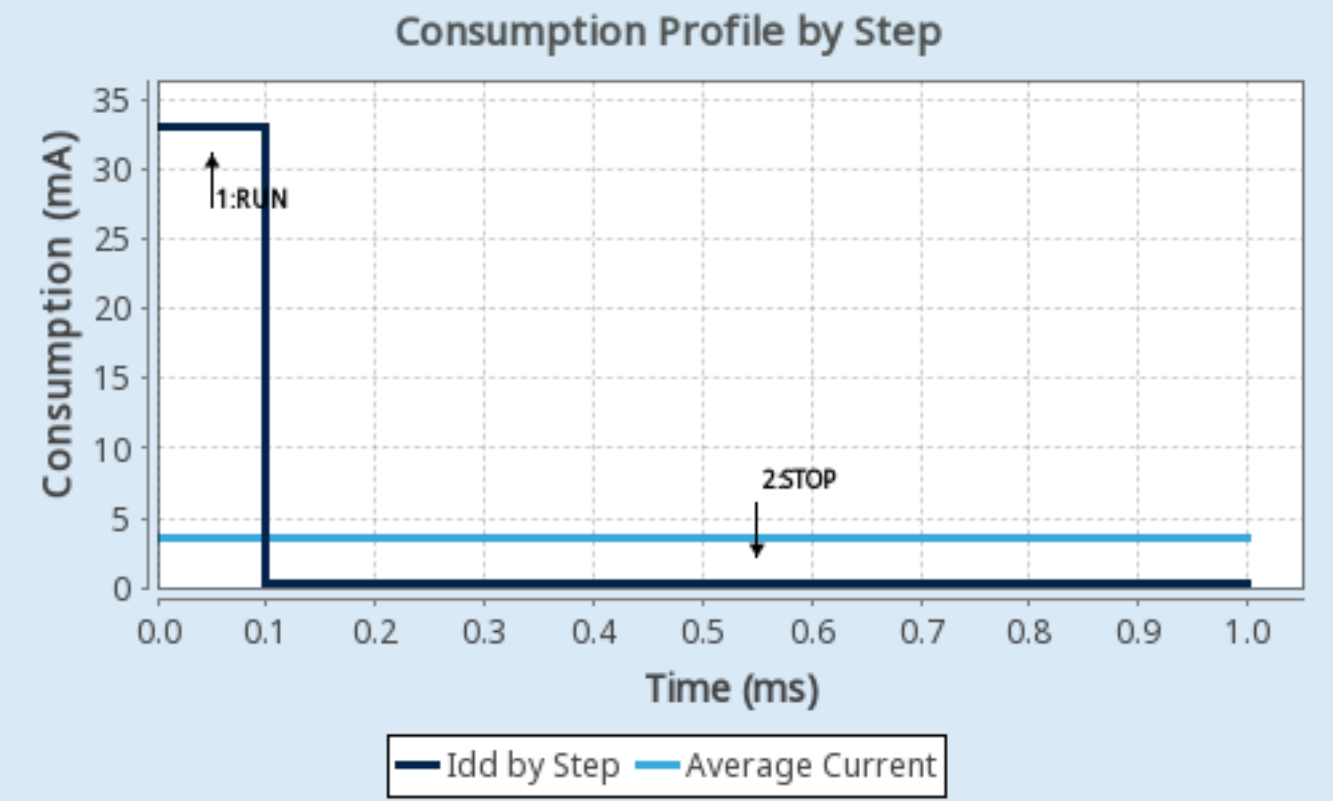
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	No-Scale	No Scale
Fetch Type	FLASH	n/a
CPU Frequency	120 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	33 mA	300 µA
Duration	0.1 ms	0.9 ms
DMIPS	150.0	0.0
Ta Max	99.99	104.95
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	3.57 mA
Battery Life	1 month, 9 days, 5 hours	Average DMIPS	150.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
35
30
25
20
15
10
5
0
1:RUN
2:STOP
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN4

mode: IN5

mode: IN6

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 2
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 4
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. ETH

Mode: MII

mode: Activate Rx Err signal

7.2.1. Parameter Settings:

Advanced : Ethernet Media Configuration:

Auto Negotiation	Enabled

Speed	100 MBits/s
Duplex Mode	Full Duplex

General : Ethernet Configuration:

Ethernet MAC Address	00:80:E1:00:00:00
PHY Address	1

Ethernet Basic Configuration:

Rx Mode	Polling Mode
TX IP Header Checksum Computation	By hardware

7.2.2. Advanced Parameters:

External PHY Configuration:

PHY	DP83848_PHY_ADDRESS
PHY Address Value	1
PHY Reset delay these values are based on a 1 ms Systick interrupt	**0x000000FF ***
PHY Configuration delay	**0x00000FFF ***
PHY Read TimeOut	**0x0000FFFF ***
PHY Write TimeOut	**0x0000FFFF ***

Common : External PHY Configuration:

Transceiver Basic Control Register	**0x00 ***
Transceiver Basic Status Register	**0x01 ***
PHY Reset	**0x8000 ***
Select loop-back mode	**0x4000 ***
Set the full-duplex mode at 100 Mb/s	**0x2100 ***
Set the half-duplex mode at 100 Mb/s	**0x2000 ***
Set the full-duplex mode at 10 Mb/s	**0x0100 ***
Set the half-duplex mode at 10 Mb/s	**0x0000 ***
Enable auto-negotiation function	**0x1000 ***
Restart auto-negotiation function	**0x0200 ***
Select the power down mode	**0x0800 ***
Isolate PHY from MII	**0x0400 ***
Auto-Negotiation process completed	**0x0020 ***
Valid link established	**0x0004 ***
Jabber condition detected	**0x0002 ***

Extended : External PHY Configuration:

PHY special control/status register Offset	**0x10 ***
MII Interrupt Control Register	**0x11 ***

MII Interrupt Status and Misc. Control Register	**0x12 ***
PHY Link mask	**0x0001 ***
PHY Speed mask	**0x0002 ***
PHY Duplex mask	**0x0004 ***
PHY Enable interrupts	**0x0002 ***
PHY Enable output interrupt events	**0x0001 ***
Enable Interrupt on change of link status	**0x0020 ***
PHY link status interrupt mask	**0x2000 ***

7.3. I2C1

I2C: I2C

7.3.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

7.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	3 WS (4 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100

LSE Startup Timout Value (ms)	5000

7.5. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.6. USART1

Mode: Asynchronous

7.6.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.7. USART2

Mode: Asynchronous

7.7.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.8. USART3

Mode: Asynchronous

7.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.9. USART6

Mode: Asynchronous

7.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.10. USB_OTG_FS

Mode: Device_Only

7.10.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Low power	Disabled
VBUS sensing	Disabled
Signal start of frame	Disabled

7.11. LWIP

mode: Enabled

Advanced parameters are not listed except if modified by user.

7.11.1. General Settings:

LwIP Version:	
LwIP Version (Version of LwIP supported by CubeMX ** CubeMX specific **)	2.0.3
IPv4 - DHCP Options:	
LWIP_DHCP (DHCP Module)	Enabled
RTOS Dependency:	
WITH_RTOS (Use FREERTOS ** CubeMX specific **)	Disabled
RTOS_USE_NEWLIB_REENTRANT (FREERTOS USE_NEWLIB_REENTRANT 2)	0
Protocols Options:	
LWIP_ICMP (ICMP Module Activation)	Enabled
LWIP_IGMP (IGMP Module)	Disabled
LWIP_DNS (DNS Module)	Disabled
LWIP_UDP (UDP Module)	Enabled
MEMP_NUM_UDP_PCB (Number of UDP Connections)	4
LWIP_TCP (TCP Module)	Enabled
MEMP_NUM_TCP_PCB (Number of TCP Connections)	5

7.11.2. Key Options:

Infrastructure - OS Awarness Option:	
NO_SYS (OS Awarness)	OS Not Used
Infrastructure - Timers Options:	
LWIP_TIMERS (Use Support For sys_timeout)	Enabled
Infrastructure - Core Locking and MPU Options:	
SYS_LIGHTWEIGHT_PROT (Memory Functions Protection)	Disabled
Infrastructure - Heap and Memory Pools Options:	
MEM_SIZE (Heap Memory Size)	1600
Infrastructure - Internal Memory Pool Sizes:	
MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs)	16
MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks)	4
MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections)	8
MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued)	16
MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List)	1
Pbuf Options:	
PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool)	16
PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool)	592

IPv4 - ARP Options:

LWIP_ARP (ARP Functionality)	Enabled

Callback - TCP Options:

TCP_TTL (Number of Time-To-Live Used by TCP Packets)	255
TCP_WND (TCP Receive Window Maximum Size)	2144
TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets)	Enabled
TCP_MSS (Maximum Segment Size)	536
TCP_SND_BUF (TCP Sender Buffer Space)	1072
TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender)	9

Network Interfaces Options:

LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes)	Disabled
LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes)	Enabled

NETIF - Loopback Interface Options:

LWIP_NETIF_LOOPBACK (NETIF Loopback)	Disabled

Thread Safe APIs - Socket Options:

LWIP_SOCKET (Socket API)	Disabled

7.11.3. PPP:

PPP Options:

PPP_SUPPORT (PPP Module)	Disabled

7.11.4. IPv6:

IPv6 Options:

LWIP_IPV6 (IPv6 Protocol)	Disabled

7.11.5. HTTPD:

HTTPD Options:

LWIP_HTTPD (LwIP HTTPD Support ** CubeMX specific **)	Disabled

7.11.6. SNMP:

SNMP Options:

LWIP_SNMP (LwIP SNMP Agent)	Disabled

7.11.7. SNTP:

SNTP Options:

LWIP_SNTP (LWIP SNTP Support ** CubeMX specific **)	Disabled

7.11.8. MDNS/TFTP:

MDNS Options:

LWIP_MDNS (Multicast DNS Support ** CubeMX specific **)	Disabled

TFTP Options:

LWIP_TFTP (TFTP Support ** CubeMX specific **)	Disabled

7.11.9. Perf/Checks:

Sanity Checks:

LWIP_DISABLE_TCP_SANITY_CHECKS (TCP Sanity Checks)	Disabled
LWIP_DISABLE_MEMP_SANITY_CHECKS (MEMP Sanity Checks)	Disabled

Performance Options:

LWIP_PERF (Performace Testing for LwIP)	Disabled

7.11.10. Statistics:

Debug - Statistics Options:

LWIP_STATS (Statictics Collection)	Disabled

7.11.11. Checksum:

Infrastructure - Checksum Options:

CHECKSUM_BY_HARDWARE (Hardware Checksum ** CubeMX specific **)	Enabled
LWIP_CHECKSUM_CTRL_PER_NETIF (Generate/Check Checksum per Netif)	Disabled
CHECKSUM_GEN_IP (Generate Software Checksum for Outgoing IP Packets)	Disabled
CHECKSUM_GEN_UDP (Generate Software Checksum for Outgoing UDP Packets)	Disabled
CHECKSUM_GEN_TCP (Generate Software Checksum for Outgoing TCP Packets)	Disabled
CHECKSUM_GEN_ICMP (Generate Software Checksum for Outgoing ICMP Packets)	Disabled
CHECKSUM_GEN_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets)	Disabled
CHECKSUM_CHECK_IP (Generate Software Checksum for Incoming IP Packets)	Disabled
CHECKSUM_CHECK_UDP (Generate Software Checksum for Incoming UDP Packets)	Disabled
CHECKSUM_CHECK_TCP (Generate Software Checksum for Incoming TCP Packets)	Disabled
CHECKSUM_CHECK_ICMP (Generate Software Checksum for Incoming ICMP Packets)	Disabled

CHECKSUM_CHECK_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets)	Disabled

7.11.12. Debug:

LwIP Main Debugging Options:

LWIP_DBG_MIN_LEVEL (Minimum Level)	All

7.12. USB_DEVICE
Class For FS IP: Communication Device Class (Virtual Port Com)

7.12.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	**5 ***
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message

Class Parameters:

USB CDC Rx Buffer Size	2048
USB CDC Tx Buffer Size	2048

7.12.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

Device Descriptor FS:

PID (Product IDentifier)	22336
PRODUCT_STRING (Product Identifier)	STM32 Virtual ComPort
CONFIGURATION_STRING (Configuration Identifier)	CDC Config
INTERFACE_STRING (Interface Identifier)	CDC Interface

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	
	PA5	ADC1_IN5	Analog mode	No pull-up and no pull-down	n/a	
	PA6	ADC1_IN6	Analog mode	No pull-up and no pull-down	n/a	
ETH	PE2	ETH_TXD3	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PC2	ETH_TXD2	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PC3	ETH_TX_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA0-WKUP	ETH_CRS	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA1	ETH_RX_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA3	ETH_COL	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA7	ETH_RX_DV	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PB0	ETH_RXD2	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PB1	ETH_RXD3	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PB10	ETH_RX_ER	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PB11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	**High ***	
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	**High ***	
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
USART2	PD5	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PD6	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
USART3	PD8	USART3_TX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PD9	USART3_RX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
USART6	PC6	USART6_TX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PC7	USART6_RX	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
USB_OTG_FS	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
GPIO	PA15	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	GPI1
	PC10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	GPI2
	PC11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	GPI3
	PC12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPO1
	PD0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPO2
	PD1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	GPO3
	PB3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	W0
	PB4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	W1

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
USB On The Go FS global interrupt	true	0	0
PVD interrupt through EXTI line16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
USART1 global interrupt	unused		
USART2 global interrupt	unused		
USART3 global interrupt	unused		
Ethernet global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
USART6 global interrupt	unused		

8.3.2. NVIC Code generation

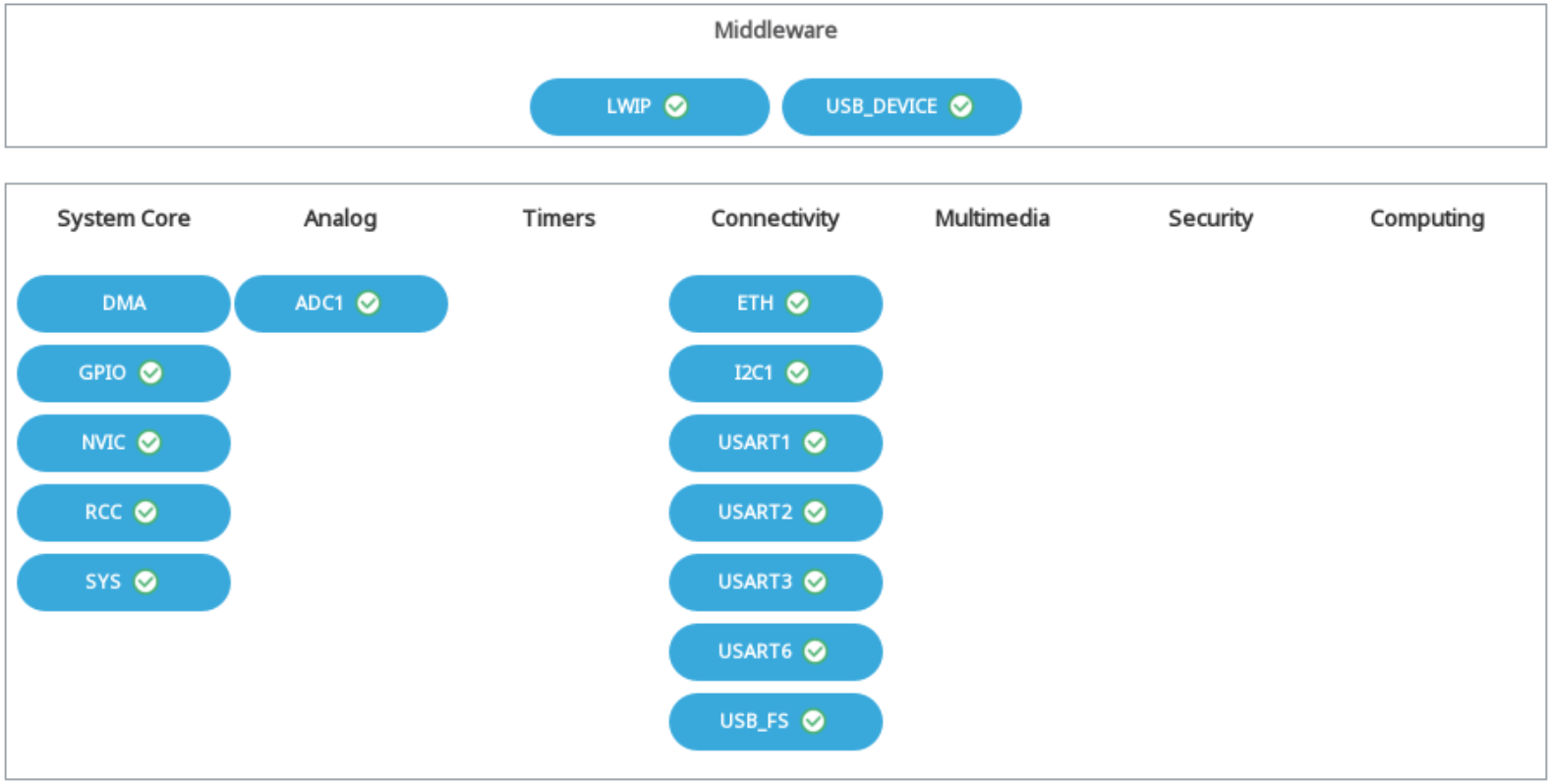
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
USB On The Go FS global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
BSDL files	https://www.st.com/resource/en/bsdl_model/stm32f2_bsdl.zip
IBIS models	https://www.st.com/resource/en/ibis_model/stm32f2_ibis.zip
System View Description	https://www.st.com/resource/en/svd/stm32f2_svd.zip
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