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Verdin Computer Module

Carrier Board Design Guide

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October 16, 2020	V0.91	Correct position of standoff holes in carrier board land pattern drawing (Figure 93) Remove additional notches from the drawings of the module
October 28, 2020	V0.92	Correction of CTRL_SLEEP_MOCI# signal type from open drain to CMOS Correction of standoff hole position in Figure 3 Section 2.6: add information to DSI display adapters
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June 14, 2021	V1.1	Updated the PHY status LED signal names according to the 1.3 version of the Verdin Family Specification throughout the whole document

Contents

1 Introduction

1.1 Overview

This document guides users through the development of a customized carrier board for the Verdin System-on-Module (SoM) family. It describes the different interfaces of those modules and provides reference schematics as well. The document highlights standardized features of Verdin SoMs (compatible between different modules). "Module-specific" interfaces, features, and alternate functions are not detailed in this document. These interfaces are detailed in the respective datasheets of Verdin SoMs. Some Verdin modules do not feature the complete set of the "Reserved" interfaces. It is strongly recommended always to read the datasheet of the module that is intended to be used with an off-the-shelf or a custom carrier board.

Verdin modules feature new high-speed interfaces such as PCI Express, HDMI, MIPI CSI, and DSI, requiring special layout considerations regarding trace impedance and length matching. Please read the Toradex Layout Design Guide carefully for additional information on the routing of these interfaces.

1.2 Additional Documents

1.2.1 Layout Design Guide

This document contains layout requirement specifications for high-speed signals and helps to avoid issues related to layout.

https://developer.toradex.com/carrier-board-design

1.2.2 Verdin Module Datasheets

For every Verdin Module, there is a datasheet available. Among other things, this document describes the "Module-specific" interfaces and secondary functionalities of pins. Before starting the development of a customized carrier board, please check these documents to verify if the required interfaces are available on the selected modules.

https://www.toradex.com/computer-on-modules/verdin-arm-family

1.2.3 Verdin Module Definition

This document describes the Verdin Module standard. It provides information on the mechanical and electrical properties of Verdin modules, in addition to functionalities and interfaces provided by those modules.

The document is available soon.

1.2.4 Toradex Developer Center

You can find a lot of additional information in the Toradex Developer Center, which is updated with the latest product support information regularly.

Please note that the Developer Center is common for all Toradex products. You should always check to ensure if the information is valid or relevant to the Verdin modules.

https://developer.toradex.com/

1.2.5 Verdin Reference Designs

Schematic files, assembly drawings, bills of material, and the complete Altium project files for the Verdin reference carrier boards are available for download for free. There is also an online viewer available, convenient for customers without a license for Altium.

https://developer.toradex.com/carrier-board-design/reference-designs

1.2.6 Pinout Designer

The Toradex Pinout Designer is a powerful tool for evaluating different pin multiplexing options for Verdin, Apalis, and Colibri Modules. Defining the pin multiplexing configuration to use or design for is a vital step in the process of designing a custom carrier board.

The tool allows comparing interfaces across different modules as well.

http://developer.toradex.com/knowledge-base/pinout-designer

1.3 Abbreviations

Abbreviation	Explanation
ADC	Analog to Digital Converter
AGND	Analog Ground, separate ground for analog signals
Auto-MDIX	Automatically Medium Dependent Interface Crossing, a PHY with Auto-MDIX can detect whether RX and TX need to be crossed (MDI or MDIX)
BSP	Board Support Package
CAD	Computer-Aided Design, in this document is referred to PCB Layout tools
CAN	Controller Area Network, a bus that is mainly used in the automotive and industrial environment
CAN FD	Controller Area Network Flexible Data-Rate, an extension to the original CAN bus protocol, allows higher data rates and larger message sizes.
CEC	Consumer Electronic Control, HDMI feature that allows controlling CEC compatible devices
CPU	Central Processor Unit
CSI	Camera Serial Interface
DAC	Digital to Analog Converter
DDC	Display Data Channel, interface for reading out the capability of a monitor, in this document DDC2B (based on I^2C) is always meant
DFP	Downstream Facing Port, USB Type-C port that acts as a host
DRC	Design Rule Check, a tool for checking whether all design rules are satisfied in a CAD tool
DRD	Dual-Role Data, USB Type-C port that can act as host or device
DRP	Dual-Role Port, USB Type-C port that can operate as power sink and source
DSI	Display Serial Interface
DVI	Digital Visual Interface, digital signals are electrically compatible with HDMI
DVI-A	Digital Visual Interface Analog only, signals are compatible with VGA
DVI-D	Digital Visual Interface Digital only, signals are electrically compatible with HDMI
DVI-I	Digital Visual Interface Integrated, combines digital and analog video signals in one connector
EDA	Electronic Design Automation, software for schematic capture and PCB layout (CAD or ECAD)
EDID	Extended Display Identification Data, timing setting information provided by the display in a PROM
EMI	Electromagnetic Interference, high-frequency disturbances
eMMC	Embedded Multi Media Card, flash memory combined with MMC interface controller in a BGA package, used as internal flash memory
ESD	Electrostatic Discharge, high voltage spike or spark that can damage electrostatic- sensitive devices
FPD-Link	Flat Panel Display Link, high-speed serial interface for liquid crystal displays. In this document, it is also called the LVDS interface.
GBE	Gigabit Ethernet, Ethernet interface with a maximum data rate of 1000Mbit/s
GMII	Gigabit Media-Independent Interface, an interface between Ethernet MAC and PHY for up to 1Gb/s

Abbreviation	Explanation
GND	Ground
GPI	General Purpose Input
GPIO	General Purpose Input/Output, pin that can be configured as an input or output
GPO	General Purpose Output
GSM	Global System for Mobile Communications
HDA	High Definition Audio (HD Audio), a digital audio interface between CPU and audio codec
HDCP	High-Bandwidth Digital Content Protection, copy protection system that is used by HDMI beside others
HDMI	High-Definition Multimedia Interface, combines audio and video signal for connecting monitors, TV sets or Projectors, electrical compatible with DVI-D
I^2C	Inter-Integrated Circuit, a two-wire interface for connecting low-speed peripherals
I^2S	Integrated Interchip Sound, serial bus for connecting PCM audio data between two devices
IrDA	Infrared Data Association, an infrared interface for connecting peripherals
JTAG	Joint Test Action Group, widely used debug interface
LCD	Liquid Crystal Display
LSB	Least Significant Bit
LVDS	Low-Voltage Differential Signaling, an electrical interface standard that can transport high-speed signals over twisted-pair cables. Many interfaces like PCIe or SATA use this interface. Since the first successful application was the Flat Panel Display Link, LVDS became synonymous with this interface. In this document, the term LVDS is used for the FPD-Link interface.
MAC	Medium Access Control is part of the second layer (data link layer) in the Ethernet stack
MII	Media-Independent Interface, an interface between Ethernet MAC and PHY for up to 100Mb/s
MIPI	Mobile Industry Processor Interface Alliance
MDI	Medium Dependent Interface, the physical interface between Ethernet PHY and cable connector
MDIO	Management Data Input/Output, an interface that is used for controlling the Ethernet PHY. The bus consists of the MDC clock and the MDIO bidirectional data signal.
MDIX	Medium Dependent Interface Crossed, an MDI interface with crossed RX and TX interfaces
mini PCIe	PCI Express Mini Card, a card form factor for internal peripherals. The interface features PCIe and USB 2.0 connectivity
MMC	MultiMediaCard, flash memory card
MSB	Most Significant Bit
mSATA	Mini-SATA, a standardized form factor for small solid-state drive, similar dimensions as mini PCIe
MXM3	Mobile PCI Express Module (second generation), graphic card standard for a mobile device, the Apalis form factor uses the physical connector but not the pin-out and the PCB dimensions of the MXM3 standard.
N/A	Not Available
N/C	Not Connected
OD	Open-Drain
OTG	USB On-The-Go, a USB host interface that can also act as a USB client when connected to another host interface
OWR	One Wire (1-Wire), a low-speed interface that needs just one data wire plus ground
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect, parallel computer expansion bus for connecting peripherals
PCIe	PCI Express, a high-speed serial computer expansion bus, replaces the PCI bus
PCM	Pulse-Code Modulation, digitally representation of analog signals, standard interface for digital audio
PD	Pull-Down Resistor
PHY	Physical Layer of the OSI model
PMIC	Power Management IC, an integrated circuit that manages amongst others the power sequence of a system
PU	Pull-up Resistor
PWM	Pulse-Width Modulation
QSPI	Quad SPI, SPI interface with four bidirectional data signals
RGB	Red Green Blue, color channels in common display interfaces
RGMII	Reduced Gigabit Media-Independent Interface, an interface between Ethernet MAC and PHY for up to 1Gb/s
RJ45	Registered Jack, common name for the 8P8C modular connector that is used for Ethernet wiring

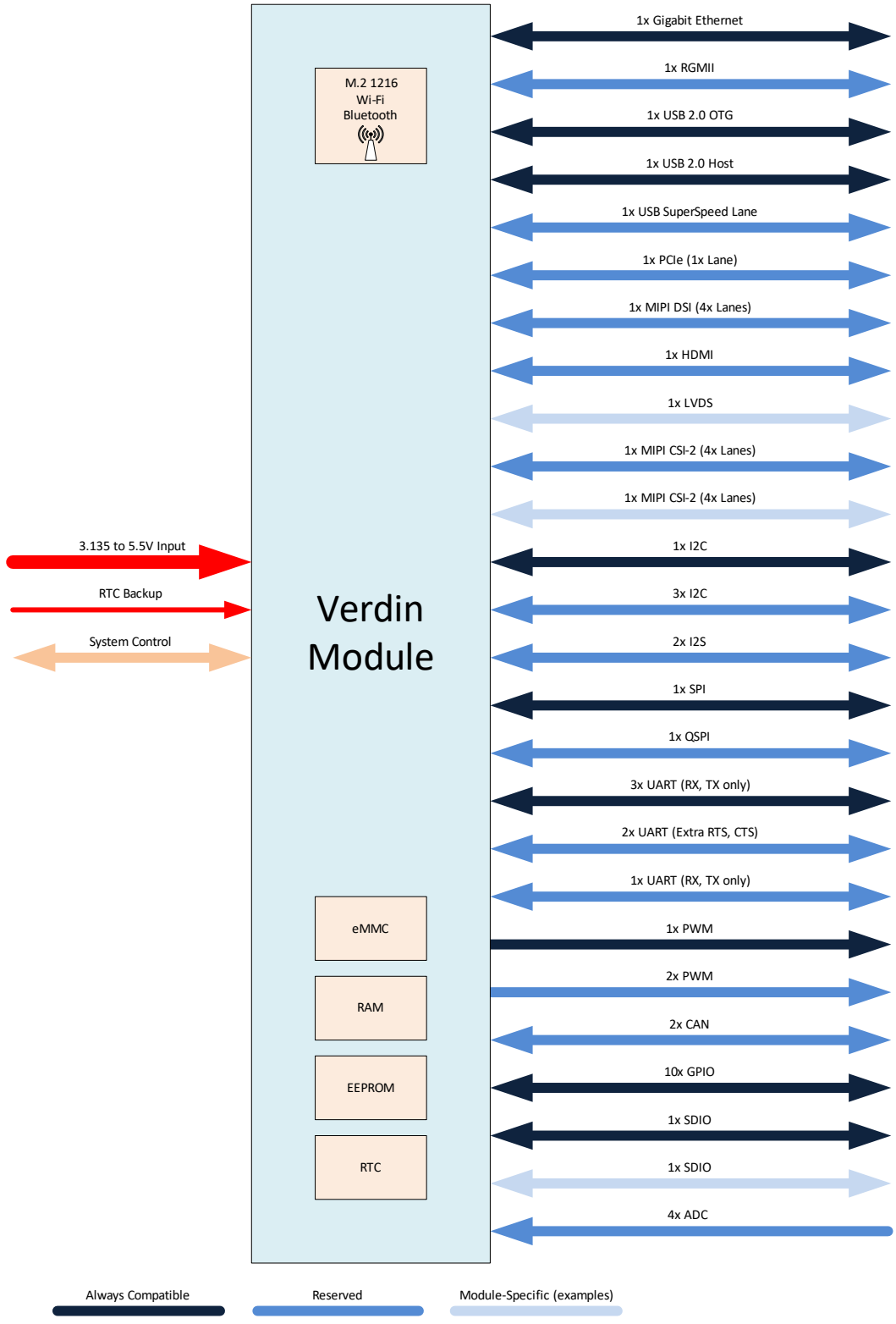
Abbreviation	Explanation
RMII	Reduced Media-Independent Interface, an interface between Ethernet MAC and PHY for up to 100Mb/s
RS232	Single-ended serial port interface
RS422	Differential signaling serial port interface, full-duplex
RS485	Differential signaling serial port interface, half-duplex, multi-drop configuration possible
R-UIM	Removable User Identity Module, identifications card for CDMA phones and networks, an extension of the GSM SIM card
S/PDIF	Sony/Philips Digital Interconnect Format, an optical or coaxial interface for audio signals
SATA	Serial ATA, high-speed differential signaling interface for hard drives and SSD
SD	Secure Digital, flash memory card
SDIO	Secure Digital Input Output, an external bus for peripherals that uses the SD interface
SIM	Subscriber Identification Module, an identification card for GSM phones
SMBus	System Management Bus (SMB), a two-wire bus based on the I^2C specifications, is used primarily in x86 design for system management.
SoC	System on a Chip, IC which integrates the main component of a computer on a single chip
SPI	Serial Peripheral Interface Bus, a synchronous four-wire full-duplex bus for peripherals
TIM	Thermal Interface Material, a thermally conductive material between CPU and heat spreader or heat sink
TMDS	Transition-Minimized Differential Signaling, serial high-speed transmitting technology that is used by DVI and HDMI
TVS Diode	Transient-Voltage-Suppression Diode, a diode that is used to protect interfaces against voltage spikes
UFP	Upstream Facing Port, USB Type-C port that acts as a client
UART	Universal Asynchronous Receiver/Transmitter, serial interface, in combination with a transceiver an RS232, RS422, RS485, IrDA or similar interface can be achieved
USB	Universal Serial Bus, serial interface for internal and external peripherals
VCC	Positive supply voltage
VGA	Video Graphics Array, analog video interface for monitors

Table 1: Abbreviations

2 Interfaces

2.1 Architecture

The block diagram in Figure 1 shows the basic architecture of the Verdin module, depicting the "Always Compatible" interfaces, "Reserved" interfaces, and some examples of "Module-specific" interfaces.



Features of Verdin modules are split into three distinct groups: "Always Compatible", "Reserved", and "Module-specific".

"Always Compatible" interfaces are features that shall be present on each SoM in the Verdin Family. Customers can expect upgradeability and maximum scalability.

"Reserved" interfaces are features that are defined and reserved but possibly missing on some Verdin SoMs. The reason for that could be that a certain SoC does not feature an interface, or there is an assembly option that omits certain interfaces for cost optimization purposes. Replacement pins must be electrically compatible with the functionality specified. This means that any Verdin SoM can be inserted into any Verdin carrier board without risking damage to the module or the carrier board (caused by electrically not-compatible pins).

A "Module-specific" feature is a feature that is not guaranteed to be functionally or electrically compatible across Verdin modules. Suppose a carrier board design uses such features. In that case, it is possible that other modules in the Verdin module family do not provide these features and instead provide other features on the associated pins. In this case, Verdin modules that are suitable for being used together with the carrier board design may need to be restricted. An incompatible SoM/carrier board combination may disable any/all functionalities or even damage the SoM or the carrier board. Using or relying on functionalities provided on "Module-specific" pins or interfaces in the context of a carrier board could make upgrades to other Verdin modules impossible.

2.1.1 "Always Compatible" Interfaces

The table below shows the "Always Compatible" interfaces provided by every Verdin module. The "GPIO Capable" column indicates whether, for a specific interface, the assigned pins can be used as GPIOs.

The "Instances" column indicates the number of interfaces that the Verdin specification defines for the "Always Compatible" interfaces. Even though the "Always Compatible" interfaces shall be available on all Verdin modules, customers should consult the datasheet for specific Verdin module variants to check for special features or restrictions of the interface.

Description	Instances	Note	GPIO Capable
Gigabit Ethernet	1	Media-dependent interface (PHY on module), backward compatible with Fast Ethernet.	No
USB 2.0 Host	1	High-Speed USB, backward compatible with Full and Low-Speed USB.	No
USB 2.0 OTG	1	Can be configured for host or client usage. SoC usually uses this port in recovery mode.	No
I^2C	1	General Purpose	Yes*
SPI	1	Single chip-select pin	Yes*
UART (RX, TX)	2	General Purpose	Yes*
UART (RX, TX)	1	Primary operating system debug port (console)	Yes*
PWM	1	General Purpose	Yes*
SDIO	1	4-bit interface, I/O voltage might be switchable between 1.8V and 3.3V for UHS-I support	Yes*
GPIO	4	General Purpose	Yes
JTAG	1		No*

Table 2: "Always Compatible" Interfaces

*May differ on some modules. Please check the datasheet of the respective module or the Pinout Designer tool.

2.1.2 "Reserved" Interfaces

Some of the "Reserved" interfaces are adding extra functionality to an "Always Compatible" interface. For example, the additional USB 3.x SuperSpeed signals in the "Reserved" class are required to be used in conjunction with the USB 2.0 Host interface signals in the "Always Compatible" class. There are additional RTS/CTS hardware flow control signals which need to be used in conjunction with the respective general-purpose UARTs found in the "Always Compatible" class.

Since "Reserved" interfaces are possibly not provided by some modules, it is mandatory to consult module datasheets for further information. A helpful tool is the Toradex Pinout Designer, which supports comparing the available features of different Verdin modules.

Suppose a module does not feature all possible instances of "Reserved" interfaces (defined by the Verdin standard). In that case, interfaces are filled in an ascending order (starting from the lowest instance index). For example, in the Verdin standard, there are two CAN interfaces (CAN_1 and CAN_2). Both are in the "Reserved" class. If only one CAN is required by a custom carrier board design, it is advisable to use CAN_1. This guarantees better compatibility with other Verdin modules. For example, when featuring a single CAN interface (CAN_1) only.

Some interfaces (I^2C and PWM) have instances that are reserved for other interfaces (e.g., HDMI). When filling interfaces during the design of Verdin SoMs, these instances are prioritized according to the availability of the interface they belong to. For example, there are up to four I^2C instances in the Verdin specification (I2C_1, I2C_2_DSI, I2C_3_HDMI, I2C_4_CSI). If an SoC features only three I^2C instances and offers no HDMI interface but has a CSI interface, the following interface interfaces are provided by the module: I2C_1, I2C_2_DSI, and I2C_4_CSI. As the example shows, in these cases, the indices of interfaces provided can be non-continuous.

Description	Standard	Note	GPIO Capable
MIPI DSI	1	Primary display interface, up to 4 data lanes.	No
HDMI	1	Secondary display interface	No
RGMII	1	Backward compatibility with RMII is not mandatory	Optional
USB 3.x Host	1	Additional SuperSpeed signals that need to be used in conjunction with the USB 2.0 Host interface	No
PCIe	1	1 lane with a reference clock. Supported generation depends on the module	No
I^2C	3	1x reserved for DSI (might be usable as general-purpose) 1x reserved for HDMI (might be usable for general purpose) 1x reserved for CSI (might be usable as general-purpose)	Yes*
QSPI	1	Backward compatible with SPI interface, independent from general-purpose SPI interface.	Yes*
UART (RX, TX)	1	Secondary operating system (real-time OS) debug port. It might be usable as general purpose UART.	Yes*
UART (RTS, CTS)	2	Complementary hardware flow control signals for the fully compatible general purpose UART interfaces	Yes*
CAN	2	CAN or CAN FD compatible	Yes*
MIPI CSI-2	1	Up to 4 data lanes	No
PWM	2	1x general purpose 1x reserved for display backlight control	Yes*
I^2S	2	1x with master clock output 1x without master clock output	Yes*
GPIO	6	2x reserved for MIPI DSI 4x reserved for MIPI CSI-2	Yes
ADC	4		No*

Table 3: "Reserved" Interfaces

*May differ on some modules. Please check the datasheet of the respective module or the Pinout Designer tool.

2.1.3 "Module-specific" Interfaces

"Module-specific" interfaces allow for the possibility of including and providing module interfaces to customers which may not be widely adopted (yet) or may be specific to a device or groups of devices. They also offer a mechanism for extending features present on "Always Compatible" or "Reserved" interfaces, such as providing additional PCI-Express lanes.

It should be noted that "Module-specific" interfaces are kept standard across modules that share such interfaces (whenever possible). For example, if both module A and module B have an LVDS interface in the "Module-specific" category, they shall be provided on the same "Module-specific" pins. Hence, both module A and module B shall share compatibility between these parts of the "Module-specific" interface. Please note that exceptions are possible to this rule. Please always consult the datasheet(s) of the respective module(s).

2.1.4 Pin Numbering

The Verdin module follows the same pin numbering scheme as the SODIMM DDR4 standard. Pins on the top side of the module have an odd number, while the pins on the bottom side have an even number.

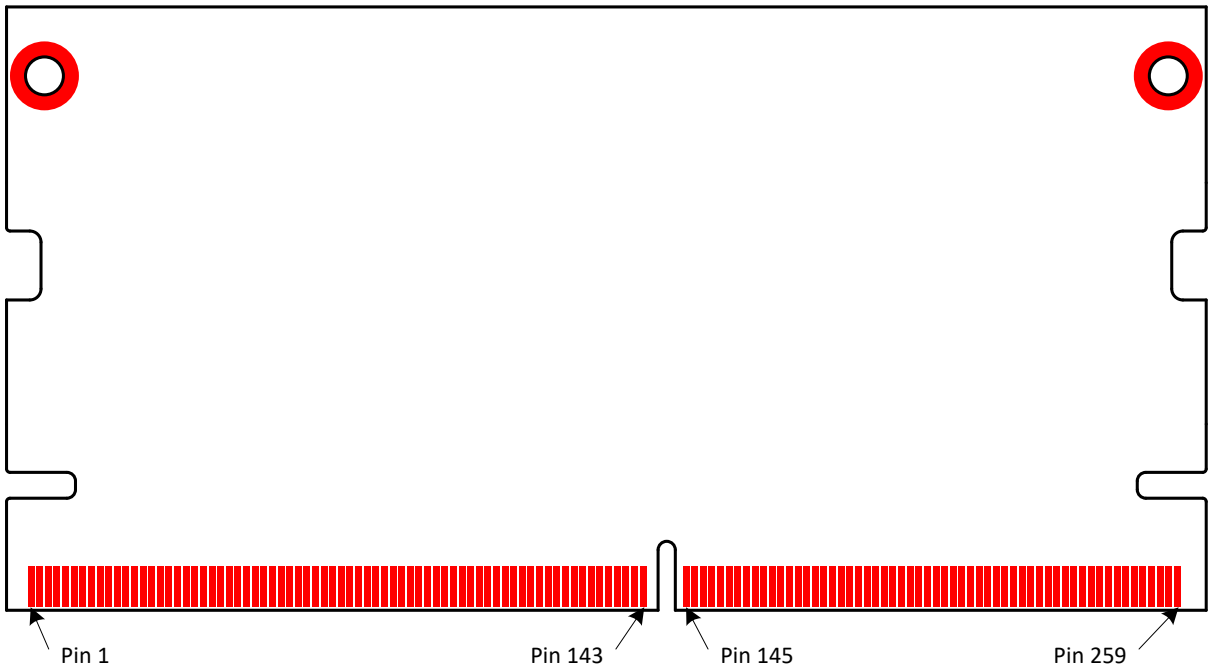


Figure 1: Pin numbering schema on the top side of the module (top view)

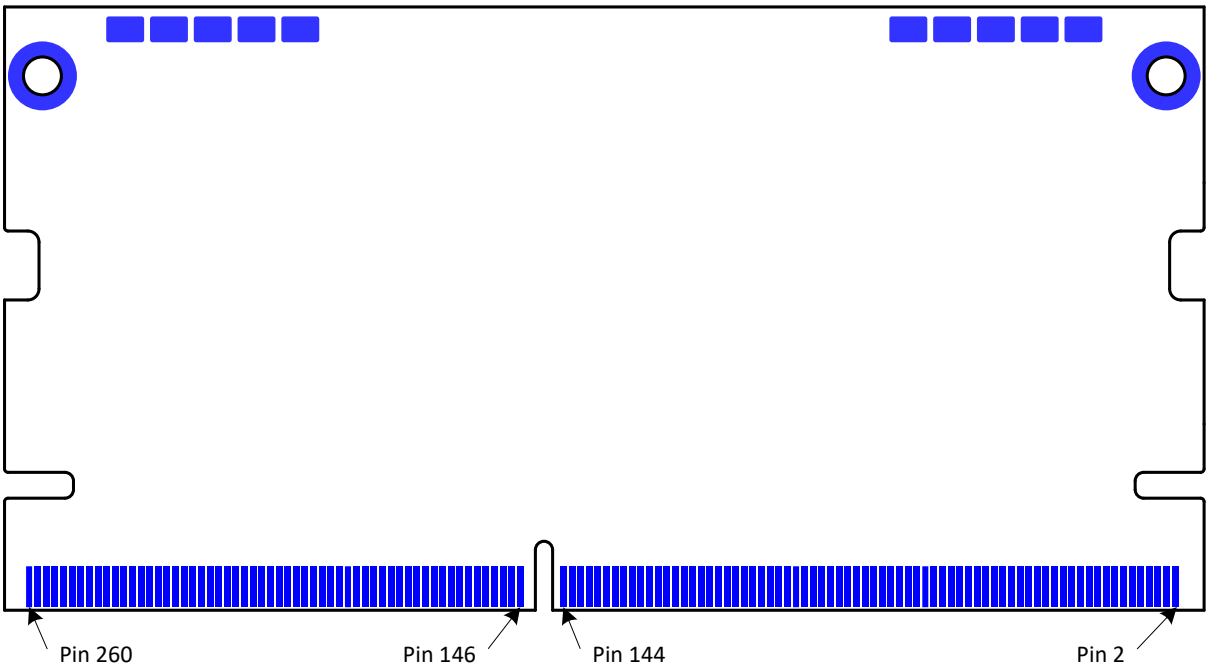


Figure 2: Pin numbering schema on the bottom side of the module (bottom view)

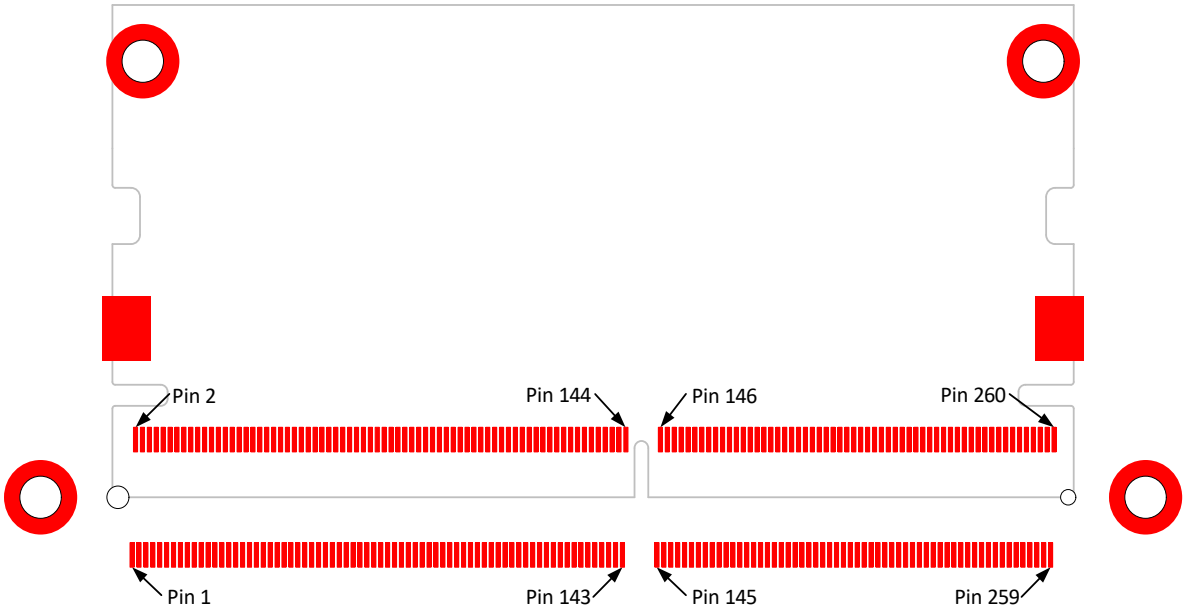


Figure 3: Pin numbering schema on the module connector land pattern (top view)

2.2 PCI Express

The Verdin module form factor features one PCIe lane as a "Reserved" interface. Depending on the module, there may be additional lanes available in the "Module-specific" area.

2.2.1 PCIe Signals

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
228	PCIE_1_CLK_P	O	PCIe		PCIe 100MHz reference clock output positive
226	PCIE_1_CLK_N	O	PCIe		PCIe 100MHz reference clock output negative
234	PCIE_1_L0_RX_P	I	PCIe		PCIe receive data positive
232	PCIE_1_L0_RX_N	I	PCIe		PCIe receive data negative
240	PCIE_1_L0_TX_P	O	PCIe		PCIe transmit data positive
238	PCIE_1_L0_TX_N	O	PCIe		PCIe transmit data negative
252	CTRL_WAKE1_MICO#	I	CMOS	1.8V	General-purpose wake signal
244	PCIE_1_RESET#	O	CMOS	1.8V	Dedicated PCIe reset output
12	I2C_1_SDA	I/O	OD	1.8V	General-purpose I2C interface data, optional
14	I2C_1_SCL	O	OD	1.8V	General-purpose I2C interface clock, optional

Table 4: PCIe signals

The PCIe interface supports polarity inversion. This means that the positive and negative signal pins can be inverted to simplify the layout by avoiding crossing the signals. Some PCIe devices support additional lane reversal for multi-lane interfaces. As the "Reserved" interfaces on Verdin provide a single lane PCIe interface, the lane reversal feature is not relevant to the Verdin specification. Some Verdin modules provide additional multi-lane PCIe interfaces as "Module-specific" interfaces. Please consult the datasheets of such modules to determine if lane reversal is applicable and supported.

2.2.2 Reference Schematics

The PCIe schematic differs depending on whether the PCIe device is soldered directly to the carrier board (device-down) or is located on a PCIe card. Special care needs to be taken to determine whether AC coupling capacitors are required. The maximum trace length of the lanes depends on whether the design is for an external card or a device-down.

Every PCIe lane consists of a pair of transmitting (TX) and receiving (RX) traces. Unfortunately, the names RX and TX can be confusing as the host transmitter needs to be connected to the receiver of the device and vice versa. Usually, the signals are named from the host's perspective until they reach the pins of the PCIe device. Therefore, the Verdin modules' transmitting pins should be called TX at the carrier board, while the module's receiving pins should be called RX. Please carefully read the datasheet of the PCIe device to make sure that RX and TX are not inadvertently swapped.

PCIe devices need a 100MHz reference clock. It is not permitted to connect a reference clock to two device loads. The Verdin module provides one reference clock output as a "Reserved" interface. There may be additional PCIe reference clock outputs in the "Module-specific" area. If there are not enough PCIe reference clocks available (e.g., if a PCIe switch is used or the PCIe interfaces in the "Module-specific" area do not provide additional clock outputs), a zero-delay PCIe clock buffer is required on the carrier board. Some PCIe switches feature an internal PCIe clock buffer, eliminating the need for a dedicated clock buffer.

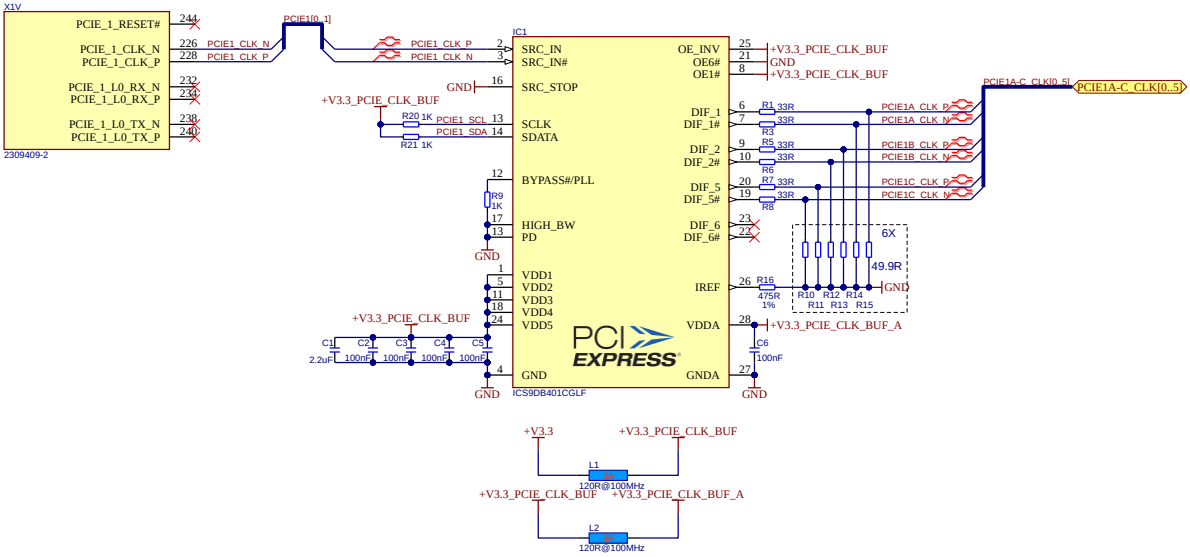


Figure 4: PCIe reference clock buffer example

2.2.2.1 PCIe x1 Slot Connector Schematic Example

For a regular PCIe slot connector, no additional decoupling capacitors are permitted to be placed on the carrier board in the RX, TX, and reference clock lines. The decoupling capacitors are located on the module and the PCIe card.

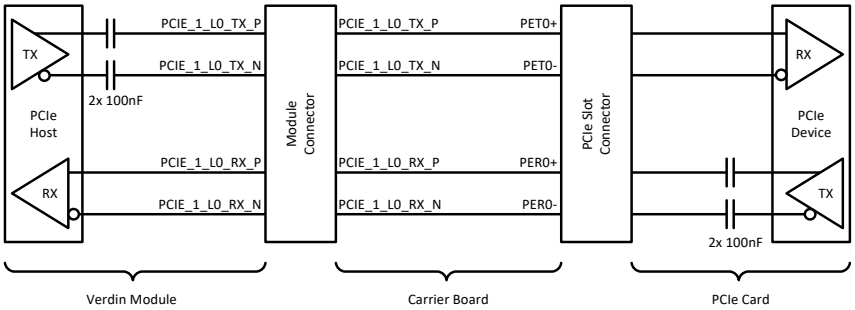


Figure 5: PCIe x1 Slot Connector Block Diagram

The Verdin module standard features a dedicated PCIe reset. This reset (PCIE_1_RESET#) should be used to guarantee the power ramp-up timing requirements of PCI Express. Since the PCIe slot connector has a 3.3V logic level and the PCIE_1_RESET# output of the module is only 1.8V, a level shifter is required. Please note that the Verdin module standard does not support PCIe hot-plug functionality.

The PCIe x1 slot connector has two card present signals (PRSNT1# pin A1 and PRSNT2# pin B18) that are shorted to ground by the card (if it is inserted). Since the Verdin standard does not feature the PCIe hot-plug feature, these pins can be left unconnected or connected to any free module GPIOs if the presence detection of the card needs to be emulated.

The wake output of the PCIe slot (WAKE#, pin B11) can be connected to the general wake input of the Verdin module (CTRL_WAKE1_MICO#). Wake-up-capable PCIe cards such as Ethernet cards can use this signal to wake up the module from the suspend state. The WAKE# signal of the PCIe card slot is an open drain type. Therefore, no level shifter is required if the signal is pulled up to 1.8V on the carrier board and not to 3.3V.

The JTAG interface on the PCIe slot can be left unconnected. This interface is only used for debugging purposes. No termination on the carrier board is needed.

The PCIe slot pin-out features an SMB interface for additional power management control. As the SMB and I2C buses are compatible from a hardware perspective, it is recommended that the general-purpose I2C_1 interface of the Verdin module is used if the SMB interface is needed. Most PCIe cards do not make use of the SMB interface. Therefore, these pins can be left unconnected for most applications. Please note that the SMB interface has a logic level of 3.3V while the I2C_1 has 1.8V. Therefore, a bidirectional level shifter is required.

According to the PCIe specifications, the regular +3.3V supply rail (pin A9, A10, and B8) and the +12V (pin A2, A3, B1, and B2) are required to be provided. The +3.3Vaux is optional. However, the +3.3Vaux must be supplied to the PCIe add-in card slot if the platform supports the wake features (WAKE#).

Not all PCIe cards need a +12V supply. It might be challenging for a battery-powered system or a carrier board with a wide voltage input range to generate a regulated 12V rail. In this case, we recommend checking with the PCIe card(s) manufacturer to determine if the +12V supply is required. Please note that omitting the +12V violates the PCI Express specifications and makes the design incompatible with some add-in cards.

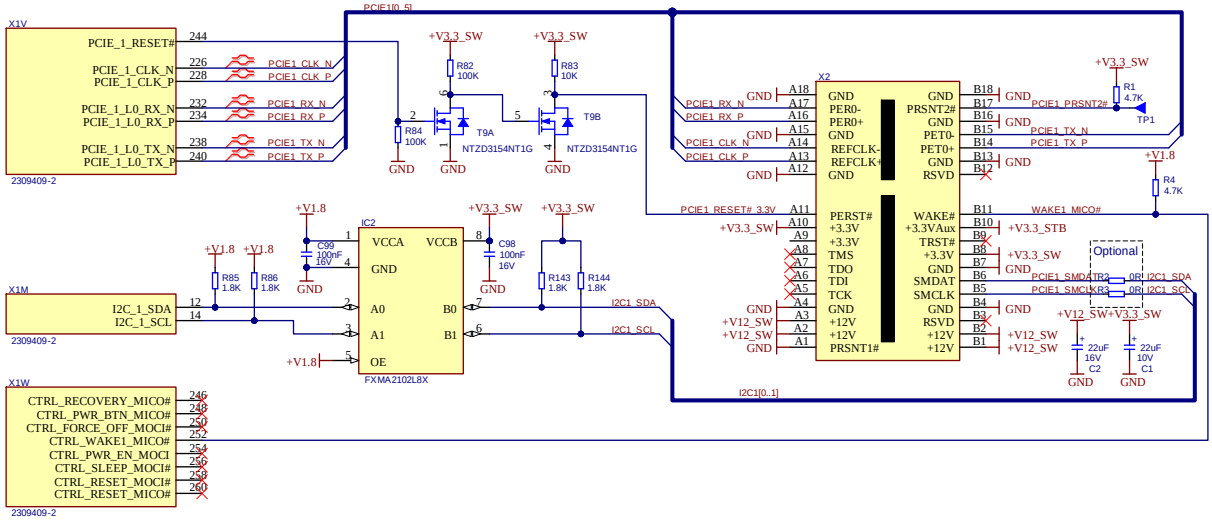


Figure 6: PCIe x1 slot reference schematic

2.2.2.2 Mini PCIe Card Schematic Example

The Mini PCIe Card (also called PCI Express Mini Card, Mini PCI Express, or Mini PCIe) features besides the PCIe link a USB 2.0 high-speed interface. To be compliant, the carrier board needs to provide both interfaces, the PCIe and USB. As most of the Mini PCIe Cards use only one of its interfaces for an embedded carrier board developed for a restricted set of compatible cards, it might be enough to implement only the required interface. Check with the Mini PCIe Card vendor whether the card uses the USB, PCIe, or both interfaces.

The Mini PCIe Card features the decoupling capacitors for the RX lines on the card. Therefore, no additional decoupling capacitors should be placed on the carrier board in either the RX, TX, or reference clock lines.

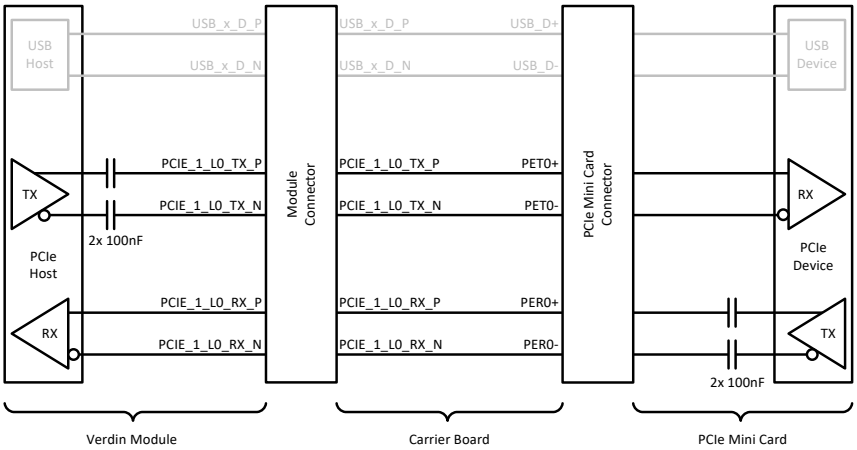


Figure 7: Mini PCIe Card Block Diagram

The Verdin module standard features a dedicated PCIe reset. This reset (PCIE_1_RESET#) should be used to guarantee the power ramp-up timing requirements of PCI Express. Since the Mini PCIe card has a 3.3V logic level for the reset input (PERST#, pin 22) and the PCIE_1_RESET# output of the module is only 1.8V, a level shifter is required. Please note that the Verdin module standard does not support PCIe hot-plug functionality.

The clock request output of the card (CLKREQ#, Pin 7) can be left unconnected. It might also be connected to a free GPIO on the Verdin module. In this case, the clock request functionality needs to be implemented in software.

The wake output of the Mini PCIe Card (WAKE#, pin 1) can be connected to the generic wake input of the Verdin module (CTRL_WAKE1_MICO#). Wake-up-capable Mini PCIe Cards such as Ethernet cards can use this signal to wake up the module from the suspend state. The WAKE# signal of the Mini PCIe Cards slot is an open drain type. Therefore, no level shifter is required if the signal is pulled up to 1.8V on the carrier board and not to 3.3V.

The R-UIM interface of the Mini PCIe Card (UIM, pin 8, 10, 12, 14, and 16) is only needed for mobile broadband modem cards such as 3G and 4G cards. If the card interface needs to support such modems, an additional SIM-card holder must be attached to this interface.

The Mini PCIe Card pin-out features an SMB interface for additional power management control. As the SMB and I2C buses are compatible from a hardware perspective, it is recommended that the general-purpose I2C_1 interface on the Verdin module is used if the SMB interface is needed. Most Mini PCIe Card does not make use of the SMB interface. Therefore, these pins can be left unconnected for most applications. Please note that the SMB interface has a logic level of 3.3V while the I2C_1 has 1.8V. Therefore, a bidirectional level shifter is required.

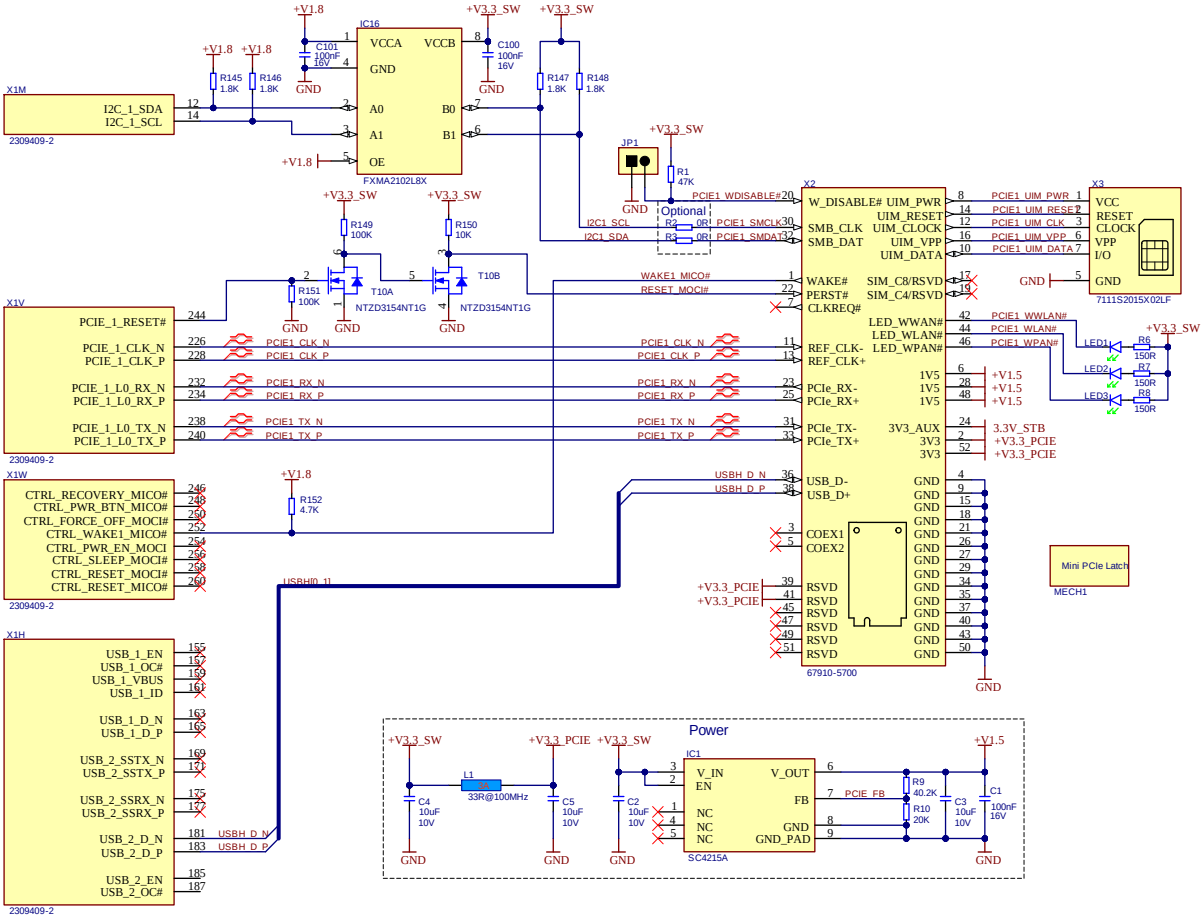


Figure 8: Mini PCIe card reference schematic

2.2.2.3 PCIe x1 Device-Down Schematic Example

Device-Down means that the PCIe device is soldered directly to the carrier board. The decoupling capacitors for the RX lanes (TX from the device) need to be placed on the carrier board. As the TX lanes' capacitors are located on the Verdin module, no additional capacitors should be placed on the TX lines. The reference clock lines do not need decoupling capacitors.

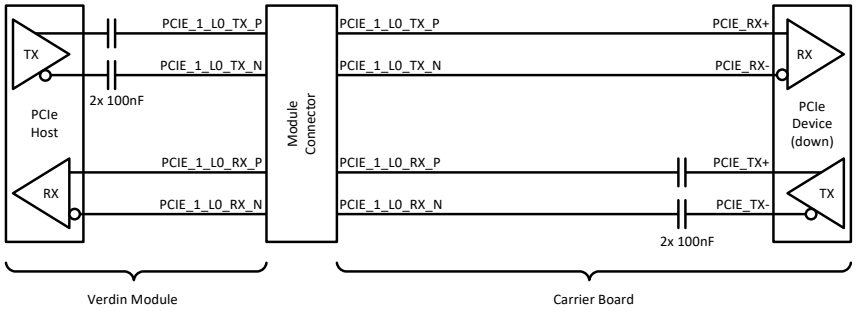


Figure 9: PCIe Device-Down block diagram

The schematic diagram shown below is an example of a device-down design of a gigabit Ethernet controller. Please be aware that the TX lane from the module needs to be connected to the RX input of the controller. The RX lane from the module needs to be connected to the TX output of the controller. Check your device carefully to determine whether it needs this crossing or not.

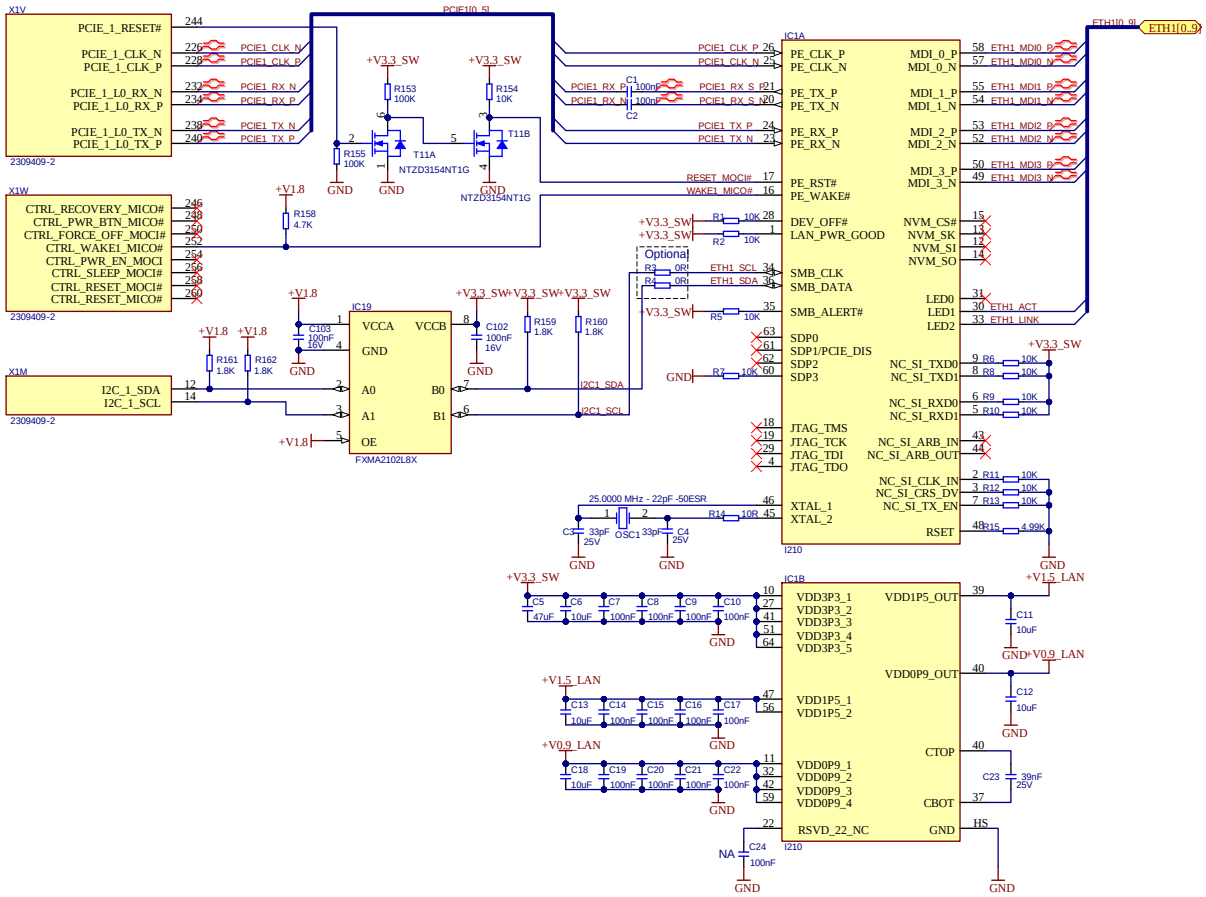


Figure 10: PCIe Device-Down example schematic

2.2.3 Unused PCIe Signals Termination

Verdin Pin	Verdin Signal Name	Recommended Termination
228	PCIE_1_CLK_P	Leave NC if not used
226	PCIE_1_CLK_N	Leave NC if not used
234	PCIE_1_L0_RX_P	Preferable connect to GND if not used or leave NC
232	PCIE_1_L0_RX_N	Preferable connect to GND if not used or leave NC
240	PCIE_1_L0_TX_P	Leave NC if not used
238	PCIE_1_L0_TX_N	Leave NC if not used
252	CTRL_WAKE1_MICO#	Add pull-up resistor or disable the wake function in the software
244	PCIE_1_RESET#	Leave NC if not used
12	I2C_1_SDA	Add pull-up resistor or disable the I²C function in the software
14	I2C_1_SCL	Add pull-up resistor or disable the I²C function in the software

Table 5: Unused PCIe Signals Termination

2.3 Ethernet

The Verdin module standard features up to two Ethernet interfaces. There is a media-dependent Gigabit Ethernet port on the "Always Compatible" interfaces with the Ethernet PHY on the module. A second Ethernet interface is available as Reduced Gigabit Media-Independent Interface (RGMII) as a "Reserved" interface. The RGMII requires a PHY to be placed on the carrier board and uses multiple media types for the physical link layer.

2.3.1 Media Dependent Ethernet Port

The Verdin features one media-dependent Gigabit Ethernet (1000Base-T) interface port (MDI). The interface is backward compatible with the 10/100Mbit Ethernet (10BASE-T and 100BASE-TX) standard. The Ethernet PHY is located on the module. Therefore, only the magnetics are required on the carrier board. The interface operates in the "voltage" mode. This means there is no center tap voltage required.

2.3.1.1 Media Dependent Ethernet Signals

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
225	ETH_1_MDI0_P	I/O	Analog		1000Base-T: DA+ 10/100Base-TX: Transmit +
227	ETH_1_MDI0_N	I/O	Analog		1000Base-T: DA- 10/100Base -TX: Transmit -
233	ETH_1_MDI1_P	I/O	Analog		1000Base-T: DB+ 10/100Base -TX: Receive +
231	ETH_1_MDI1_N	I/O	Analog		1000Base-T: DB- 10/100Base -TX: Receive -
239	ETH_1_MDI2_P	I/O	Analog		1000Base-T: DC+ 10/100Base -TX: Unused
241	ETH_1_MDI2_N	I/O	Analog		1000Base-T: DC- 10/100Base -TX: Unused
247	ETH_1_MDI3_P	I/O	Analog		1000Base-T: DD+ 10/100Base -TX: Unused
245	ETH_1_MDI3_N	I/O	Analog		1000Base-T: DD- 10/100Base -TX: Unused
237	ETH_1_LED_2	O	OD	3.3V tolerant	LED indication output for established Ethernet link
235	ETH_1_LED_1	O	OD	3.3V tolerant	LED indication output for activity on the Ethernet port

Table 6: Ethernet signals

2.3.1.2 Media Dependent Ethernet Reference Schematics

Ethernet connectors with integrated magnetics are preferable. If a design with external magnetics is chosen, additional care must be taken to route the signals between the magnetics and Ethernet connector. If only a fast Ethernet (100Mbit/s) is required, some design costs may be saved using only 10/100Base-TX magnetics.

The magnetics provide a certain ESD protection which is enough for many designs. However, especially in Power over Ethernet (PoE) systems, additional transient voltage suppressor diodes (TVS) are highly recommended to be placed between the module and the magnetics. More information can be found in the following application note from Microchip:
http://ww1.microchip.com/downloads/en/AppNotes/00002157B.pdf

The LED output signals ETH_1_LED_1 and ETH_1_LED_2 are 3.3V tolerant open-drain signals with no pull-up resistor on the module. The pins can be connected directly to the LED of the Ethernet jack with suitable series resistors. There is no need for additional buffering if the current drawn does not exceeds 10mA. The ETH_1_LED_2 signal is used as a reference for the ETH_1_MDI2_P signal on the SODIMM connector, and the ETH_1_LED_1 is a reference for the ETH_1_MDI1_P signal. Therefore, it is recommended to add a strapping capacitor of 1nF to GND as close as possible to the SODIMM connector.

2.3.1.2.1 Gigabit Ethernet Schematic Example (Integrated Magnetics)

The Verdin module does not require a center tap voltage. Therefore, add individual 100nF capacitors to the center taps of the magnetics. Do not connect the center taps together.

The Ethernet connector with integrated magnetics provides a certain amount of protection against ESD. If a higher level is required, optional ESD protection diodes are recommended.

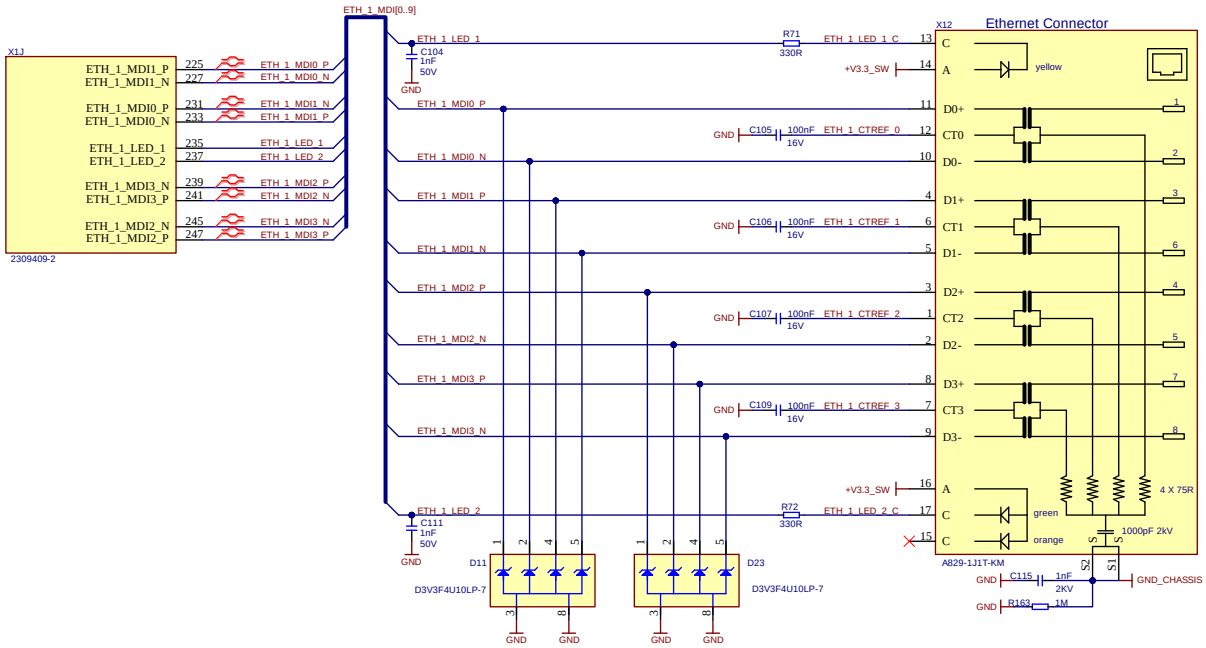


Figure 11: Gigabit Ethernet with integrated magnetics reference schematic

2.3.1.2.2 Gigabit Ethernet Schematic Example (Discrete Magnetics)

If discrete magnetics are used instead of an RJ-45 Ethernet jack with integrated magnetics, special care must be taken to route the signals between the magnetics and the jack. These signals are required to be high voltage isolated from the other signals. Therefore, it is necessary to place a dedicated ground plane under these signals, which has a minimum separation of 2mm from every other signal and plane. Try to place the magnetics as close as possible to the Ethernet jack. This reduces the length of the signal traces between the magnetics and jack.

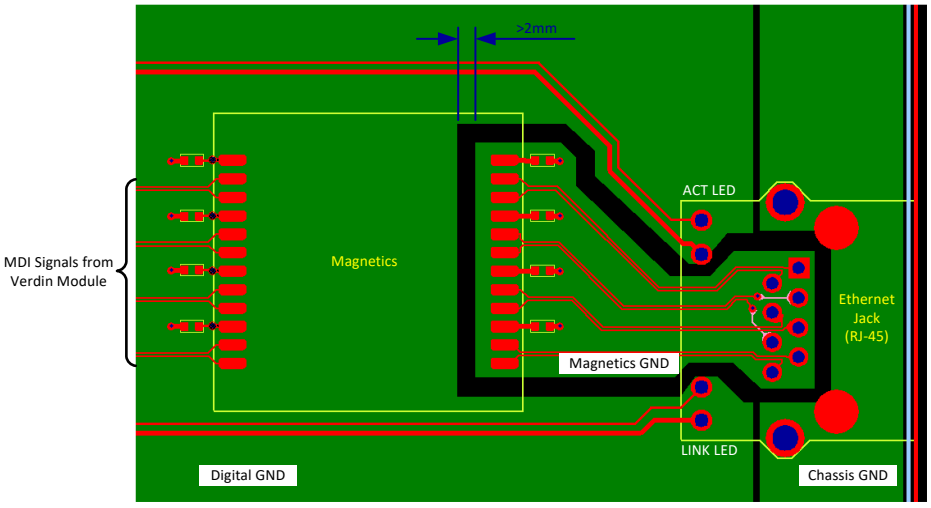


Figure 12: Separation of magnetics ground

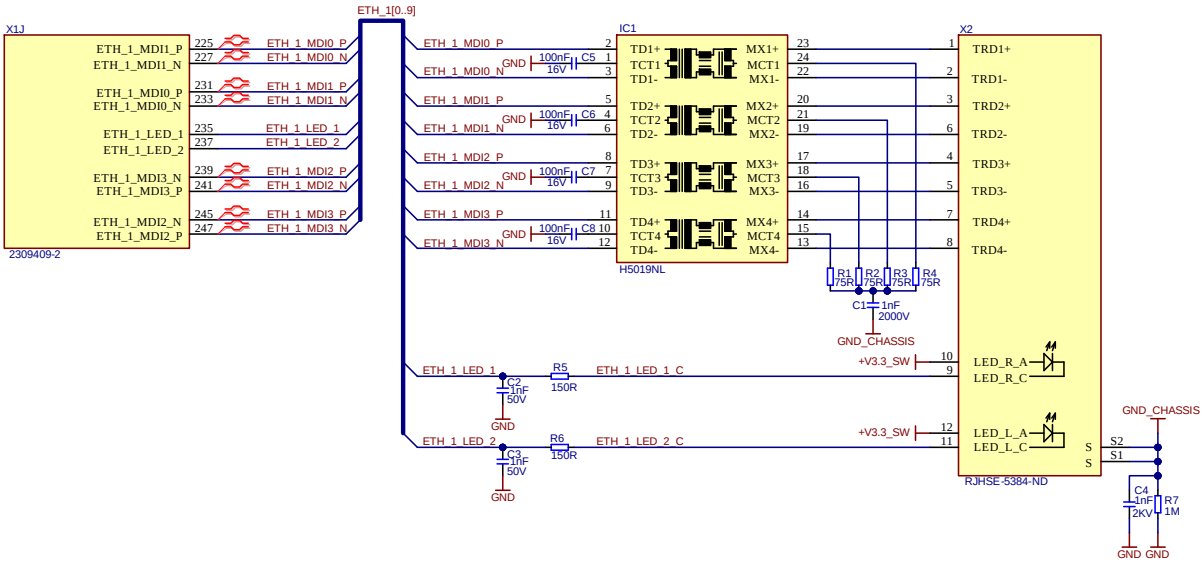


Figure 13: Gigabit Ethernet with discrete magnetics reference schematic

2.3.1.2.3 10/100Mbit Ethernet Schematic Example (Integrated Magnetics)

The Fast Ethernet interface uses the MDI0 as transmitting lanes and the MDI1 as receiving lane. As most Ethernet PHYs feature Auto-MDIX, the signal direction RX and TX could be swapped. However, it is recommending not to swap the RX and TX lanes to ensure compatibility between all Verdin modules.

The MDI2 and MDI3 lanes are not used for the 10/100Base-TX interface. These signals can be left unconnected.

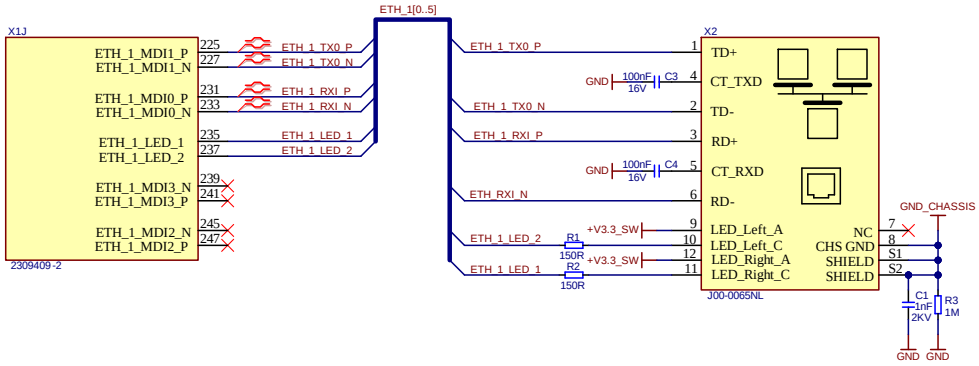


Figure 14: Fast Ethernet with integrated magnetics reference schematic

2.3.1.3 Unused Ethernet Signals Termination

All unused Media Independent Ethernet signals can be left unconnected.

2.3.2 Reduced Gigabit Media-Independent Interface Ethernet Port

In addition to the Media Dependent Ethernet port, the Verdin family provides a second Ethernet port in the "Reserved" category. However, this secondary port is provided as a Reduced Gigabit Media-Independent Interface (RGMII). This means only the Ethernet MAC (Medium Access Control) is on the module. The PHY (physical layer) needs to be on the carrier board. This allows for additional flexibility in choosing the suitable transport medium (e.g., fiber-optical cable).

Some of the Verdin modules also allow using the interface as RMII (Reduced Media-Independent Interface) for Fast Ethernet. For compatibility reasons, the RGMII is the preferred interface for an Ethernet PHY on the carrier board.

The RGMII standard supports different I/O voltages. However, for the Verdin module family, the preferred I/O voltage is 1.8V. This increases the compatibility between different Verdin modules.

Besides the RGMII, there is a Management Data Input/Output interface (MDIO) for managing the PHY on the carrier board. Some Verdin modules maybe share the interface with the on-module Ethernet PHY. In these cases, special care must be taken to address the carrier board PHY does not conflict with the on-module PHY address.

2.3.2.1 RGMII Signals

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
199	ETH_2_RGMII_RX_CTL	I	CMOS	1.8V	Multiplexing of data received is valid and receiver error
197	ETH_2_RGMII_RXC	I	CMOS	1.8V	Received clock signal
201	ETH_2_RGMII_RXD_0	I	CMOS	1.8V	Received data (PHY to MAC)
203	ETH_2_RGMII_RXD_1	I	CMOS	1.8V	
205	ETH_2_RGMII_RXD_2	I	CMOS	1.8V	
207	ETH_2_RGMII_RXD_3	I	CMOS	1.8V	
211	ETH_2_RGMII_TX_CTL	O	CMOS	1.8V	Multiplexing of transmitter enable and transmitter error
213	ETH_2_RGMII_TXC	O	CMOS	1.8V	Transmit clock signal
221	ETH_2_RGMII_TXD_0	O	CMOS	1.8V	Data to be transmitted (MAC to PHY)
219	ETH_2_RGMII_TXD_1	O	CMOS	1.8V	
217	ETH_2_RGMII_TXD_2	O	CMOS	1.8V	
215	ETH_2_RGMII_TXD_3	O	CMOS	1.8V	
193	ETH_2_RGMII_MDC	O	CMOS	1.8V	Management interface clock (output from MAC)
191	ETH_2_RGMII_MDIO	I/O	OD	1.8V	Management interface data (bidirectional, needs pull-up on carrier board)
189	ETH_2_RGMII_INT#	I	OD	1.8V	Optional interrupt, requires a pull-up on the carrier board

2.3.2.2 RGMII Reference Schematics

For best software compatibility, the Gigabit Ethernet Transceiver KSZ9131RNX from Microchip is a preferred solution. This Ethernet PHY supports the 1.8V I/O voltage level of the RGMII interface. For other Ethernet PHY solutions, check the availability of software drivers.

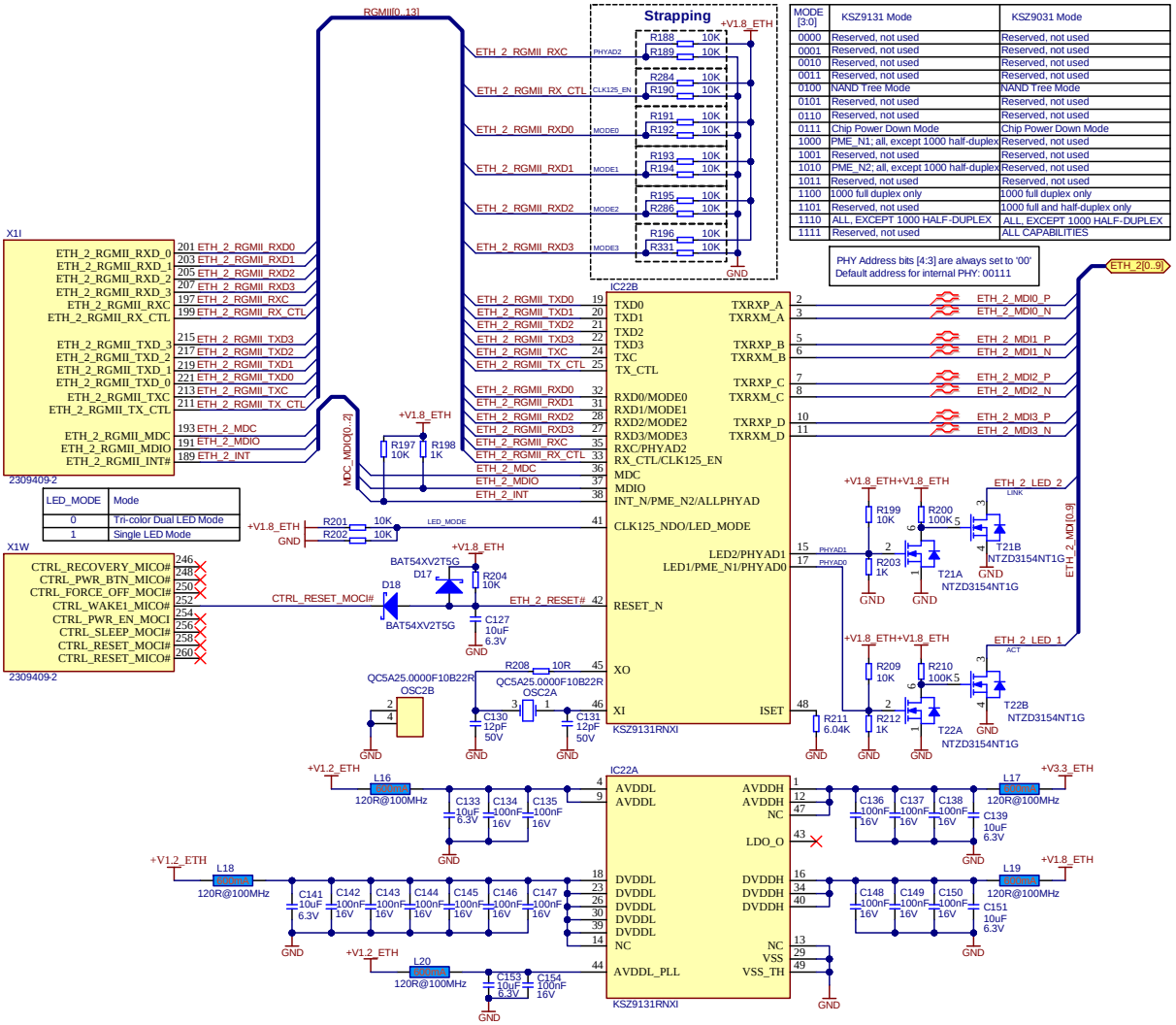


Figure 15: RGMI reference schematic

2.4 USB

The Verdin specifications contain two USB ports. One port is an OTG port that can be configured as a host or client. This port is usually used in the recovery mode for loading new software onto the module. The second port supports host mode only. Both ports can support the low, full, and high-speed modes of the USB 2.0 specifications.

Verdin Port	1.5Mbit/s Low Speed (1.1)	12 Mbit/s Full Speed (1.1)	480Mbit/s High Speed (2.0)	5Gbit/s SuperSpeed (3.x)	10Gbit/s SuperSpeed (3.x)	OTG
USB_1	✓	✓	✓			✓
USB_2	✓	✓	✓	✓	✓	

Table 7: Maximum possible supported features for the USB ports

In the "Reserved" pin category of the Verdin specifications, there are additional SuperSpeed signals which are intended to be used in conjunction with the USB_2 port (host only) in the "Always Compatible" class. This upgrades the port to a USB 3.x capable interface. The naming schemes of USB 3.x can be a bit confusing. There are different names for the same speed grade, depending on the revision of the specifications that are taken. Table 8 shows a comparison of the different transfer modes and their naming schemes. Not all the USB 3.x transfer modes are possible with the Verdin module since only one lane of SuperSpeed signals is reserved in the Verdin standard.

The actual possible USB 3.x mode also varies by the module itself. Therefore, it is essential to check the module datasheet whether the SuperSpeed signals are available and which maximum speed they support.

Marketing Name	USB 3.2 Name	USB 3.1 Name	USB 3.0 Name	Nominal Speed	SuperSpeed Lanes	Supported by Verdin
SuperSpeed USB	USB 3.2 Gen 1x1	USB 3.1 Gen 1	USB 3.0	5 Gbit/s 0.5 GByte/s	1	Possible
SuperSpeed USB 10 Gbit/s	USB 3.2 Gen 1x2			10 Gbit/s 1 GByte/s	2	No
SuperSpeed USB 10 Gbit/s	USB 3.2 Gen 2x1	USB 3.1 Gen 2		10 Gbit/s 1.2 GByte/s	1	Possible
SuperSpeed USB 20 Gbit/s	USB 3.2 Gen 2x2			20 Gbit/s 2.4 GByte/s	2	No

Table 8: USB 3.x Transfer Mode Naming Schemes

The first generation (Gen 1) uses 8b/10b encoding, while the second generation (Gen 2) uses the more efficient 128b/132b encoding. This is the reason why the second generation can reach a higher byte-rate than the first generation with the same bitrate.

2.4.1 USB Signals

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
165	USB_1_D_P	I/O	USB		Positive differential USB signal, OTG capable
163	USB_1_D_N	I/O	USB		Negative differential USB signal, OTG capable
161	USB_1_ID	I	CMOS	1.8V	Cable identification pin for the OTG
159	USB_1_VBUS	I	CMOS	5V tolerant	Bus voltage detection in the OTG client mode
155	USB_1_EN	O	CMOS	1.8V	Enable signal for the bus voltage output in host mode
157	USB_1_OC#	I	OD	1.8V	Overcurrent input signal

Table 9: USB_1 Signals

While all the signals of the USB_2 port that are required for running the interface with High-Speed USB 2.0 are in the "Always Compatible" category, the additional SuperSpeed signals for running the interface in USB 3.x mode are in the "Reserved" category. These signals are not available on all the Verdin modules.

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
183	USB_2_D_P	I/O	USB		Positive differential USB 2.0 signal
181	USB_2_D_N	I/O	USB		Negative differential USB 2.0 signal
177	USB_2_SSRX_P	I	PCIe		Positive differential receiving signal (reserved for USB 3.x)
175	USB_2_SSRX_N	I	PCIe		Negative differential receiving signal (reserved for USB 3.x)
171	USB_2_SSTX_P	O	PCIe		Positive differential transmission signal (reserved for USB 3.x)
169	USB_2_SSTX_N	O	PCIe		Negative differential transmission signal (reserved for USB 3.x)
185	USB_2_EN	O	CMOS	1.8V	Enable signal for the bus voltage output
187	USB_2_OC#	I	OD	1.8V	Overcurrent input signal

Table 10: USB_2 Signals

SuperSpeed signals are basically PCIe signals and therefore support polarity inversion. This means the positive and negative signal pins can be inverted to simplify the layout by avoiding crossing the signals. It is not permitted to swap the receiving signals with the transmitting ones. Noteworthy, the USB 2.0 data signals do not support polarity inversion; USB_x_D_P and USB_x_D_N cannot be swapped.

2.4.2 Reference Schematics

As the additional SuperSpeed USB 3.x data signals are PCIe signals at the physical layer. Therefore, the schematic requirements are like those for PCIe. This means AC coupling capacitors are required. The placement of the capacitors depends on whether the USB 3.x device is populated on the carrier board (device-down) or is connected over a cable. The USB 2.0 data signals do not need any coupling capacitors.

The SuperSpeed interface consists of a pair of transmitting (TX) and receiving (RX) traces. Unfortunately, the names RX and TX can be confusing as the host transmitter needs to be connected to the receiver of the device and vice versa. Usually, the signals are named after the host until they reach the pins of the USB device. Therefore, the Verdin module's transmitting pins should be called TX on the carrier board, while the receiving pins should be called RX. Please read the datasheet of the USB device (device-down) carefully to ensure RX and TX are not confused.

2.4.2.1 USB 2.0 OTG Schematic Example

If the USB signals are externally available, ESD protection diodes need to be placed on all USB signals. Make sure that the protection diodes are USB 2.0 compliant. The USB signals additionally require a common mode choke for passing EMI testing. Use common mode chokes that are specified for High-speed USB 2.0.

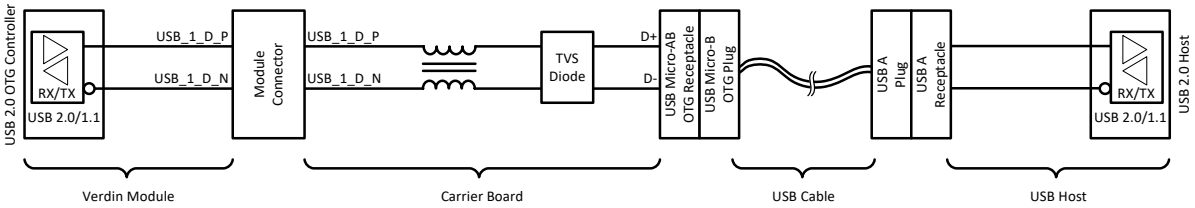


Figure 16: USB 2.0 OTG Block Diagram

The USB_1_ID signal is used to detect which type of USB connector is plugged into the OTG jack (Micro-AB jack). When a Micro-A connector is inserted, the ID pin is connected to signal ground, causing the OTG port to be configured as a host. If a Micro-B USB connector is inserted, the ID pin is left unbiased, and the OTG port is configured as a slave device. For the USB_1_ID signal, a pull-up resistor to 1.8V is needed.

The USB_1_VBUS input signal is only used if the OTG port is in client mode (Micro-B USB connector plugged in). The signal is used to detect whether a host is connected to the other end of the USB cable. This signal is 5V tolerant and can be connected directly to the power supply pin of the USB jack. ESD protection diodes should be used for this signal.

The USB_1_EN signal enables the USB bus power supply if a Micro-A USB connector is plugged in. The USB_1_EN signal has an I/O level of 1.8V. Depending on the power switch IC, a simple level shifter may be required.

A USB compliant design needs to detect over-current on the provided bus power output. The output rail needs to be turned off in case an over-current condition occurs. The USB_1_OC# signal is used to notify the module that an over-current condition has occurred. This signal is active-low and requires a pull-up resistor to 1.8V on the baseboard.

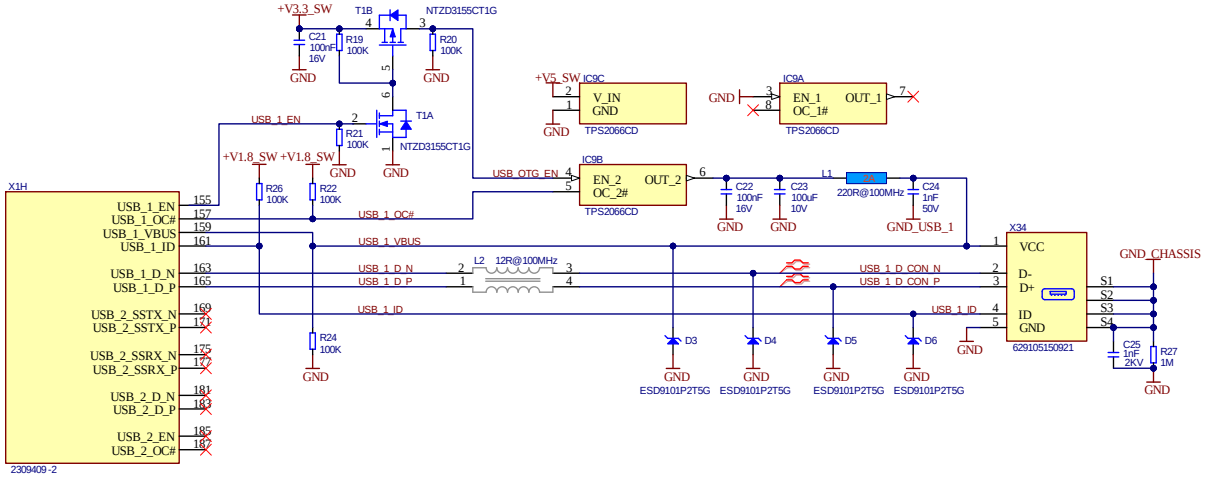


Figure 17: USB OTG reference schematic

2.4.2.2 USB-C Dual Role Schematic Example

The term USB OTG is only used in conjunction with the USB Micro-AB or the obsolete USB Mini-AB receptacle. The term OTG is replaced with the name Dual Role Device (DRD) when it comes to USB Type-C receptacles and connectors. Like the old USB OTG, a USB-C DRD can change its role from being a device to be a host and vice versa. The USB OTG receptacle was using the ID pin for detecting whether a Type-A or Type-B plug is connected to know in which role the communication must start and whether the bus power needs to be provided or not. The USB Type-C does not feature an ID pin anymore. The detection of the role is done by the two Configuration Channel (CC) pins.

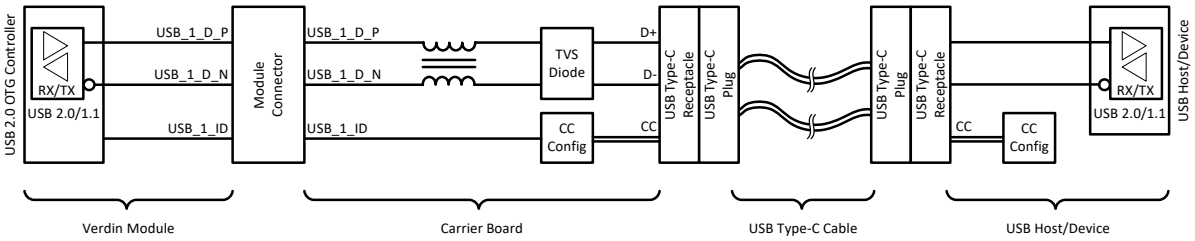


Figure 18: USB Type-C Block Diagram

The CC pins serve multiple purposes on a Type-C connector. It is used to detect the connector's orientation in the receptacle, negotiating the power delivery (voltage and current), and negotiating the role of the device. For the CC detection of a DRD port, a port control IC is used. The TUSB321 can translate the CC detection to a USB OTG ID signal which can be used with the Verdin module. If the port has been negotiated as the source for the power (Downstream Facing Port DFP), the VBUS needs to be provided. The TUSB321 can be strapped to announce different current levels to the device. The over-current protection IC on the carrier board needs to be set to a level that complies with the announced current.

The USB 2.0 signals are in the center of the USB Type-C connector. Therefore, the signals of the top and bottom side of the connector can be connected together without significant stubs. This means no multiplexer is required if the SuperSpeed signals are not provided to the connector.

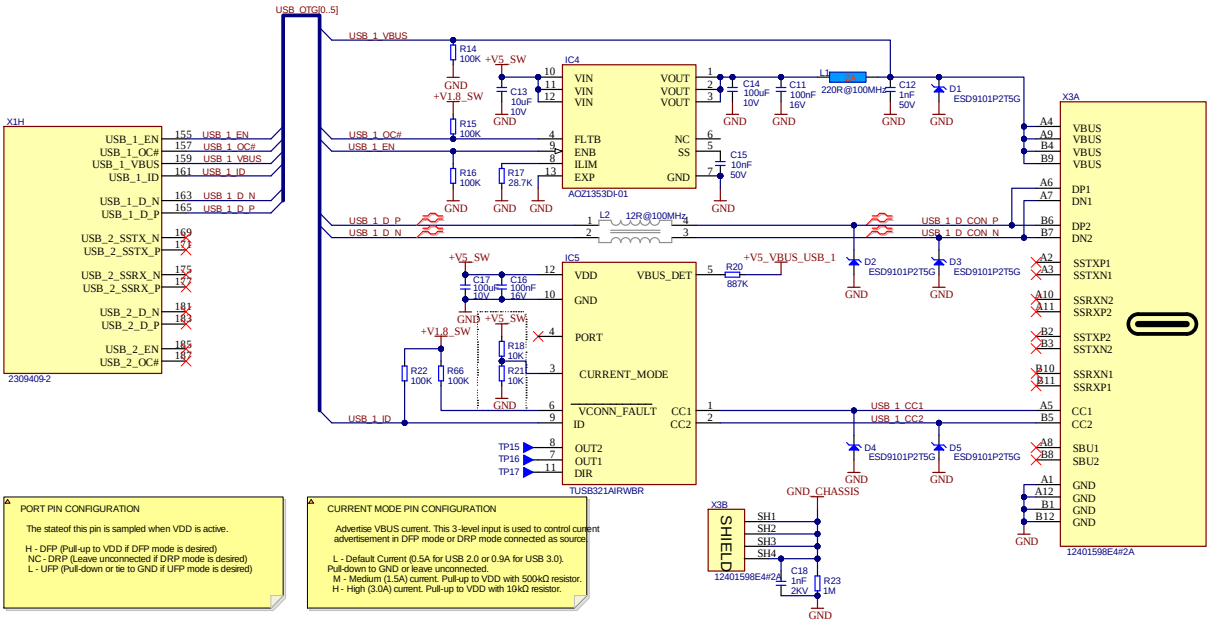


Figure 19: USB Type-C reference schematic

2.4.2.3 USB Client Only Schematic Example

If the USB_1 port is used only as a client interface (e.g., if only used for the recovery mode), the schematic diagram can be simplified.

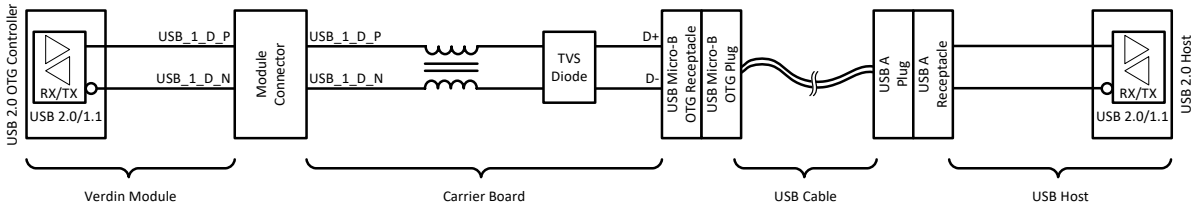


Figure 20: USB 2.0 client block diagram

USB_1_EN, USB_1_OC# and USB_1_ID pins are not used in this configuration. The USB_1_EN pin can be left unconnected. The USB_1_OC# should be pulled up to 1.8V or disabled in the software. The USB_1_ID pin needs to be pulled up to 1.8V, or the OTG port needs to be configured to a client-only mode in the software.

The USB_1_VBUS pin can be connected directly to the USB bus power supply of the USB Micro-B connector. This signal is needed to indicate to the system that a host is connected at the other end of the USB cable.

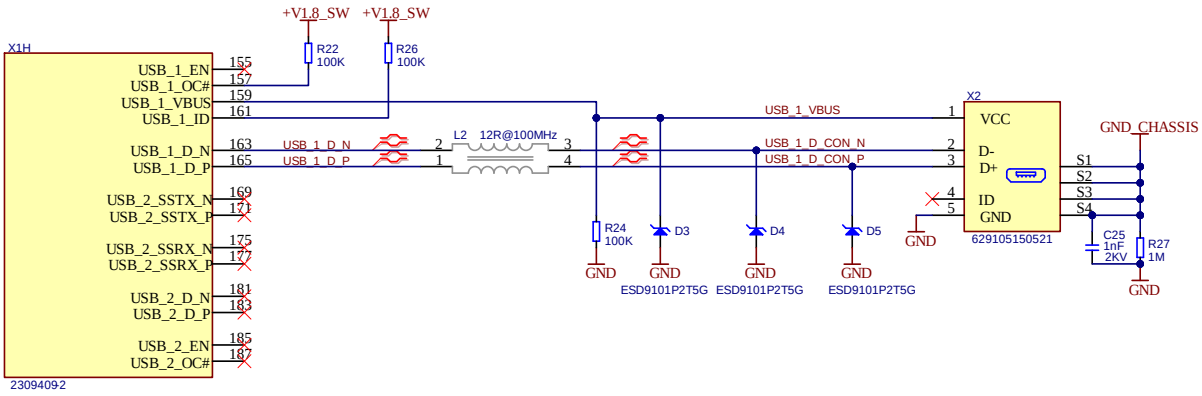


Figure 21: USB 2.0 client reference schematic

2.4.2.4 USB 3.x Host Connector Schematic Example

The USB_2 port of the Verdin module specifications reserves additional SuperSpeed signals, which makes it possible to provide a USB 3.x host interface. The SuperSpeed signals are physically related to the PCIe interface. Therefore, special attention is required with the series capacitors. The AC coupling capacitors of the TX SuperSpeed signals are located on the Verdin module, while the capacitors for the RX signals are located on the USB device. Therefore, no additional capacitors are required nor permitted on the carrier board. The USB 2.0 data signals do not need any series capacitors at all.

If the USB signals are externally available, ESD protection diodes need to be placed on all the USB signals. Make sure that the protection diodes are compliant with the very high frequency of USB 3.x.

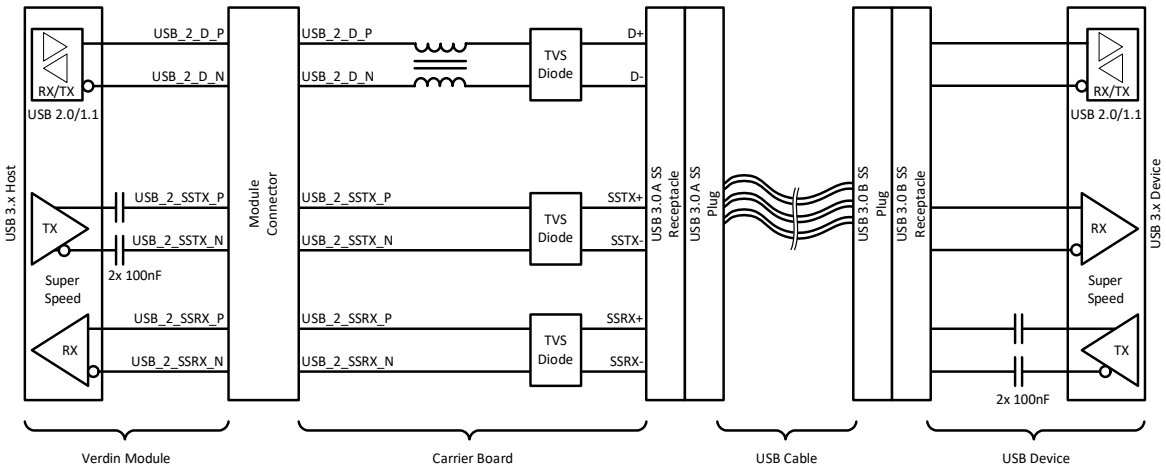


Figure 22: USB 3.x host block diagram

Please note that a Type A USB 3.x compliant host port needs to provide up to 900mA bus supply while the USB 2.0 ports were only rated up to 500mA for a regular, non-charging port. Make sure the bus voltage power distributor switch IC can deliver this higher current. According to the USB specifications, an output capacitor of at least 100µF needs to be added to the USB bus voltage.

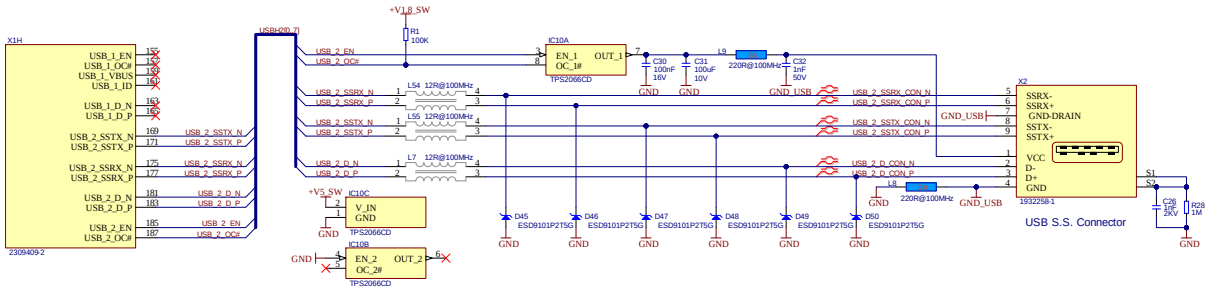


Figure 23: USB 3.0 host reference schematic

2.4.2.5 USB 3.x Device Down Schematic Example

Device-Down means that the USB device is soldered to the carrier board. The AC coupling capacitors for the SuperSpeed RX lane (TX from the device) need to be placed on the carrier board. As the TX lane's capacitors are located on the Verdin module, no additional capacitors are required or permitted on the TX lines.

ESD protection diodes and common-mode chokes are usually not needed for device-down implementations.

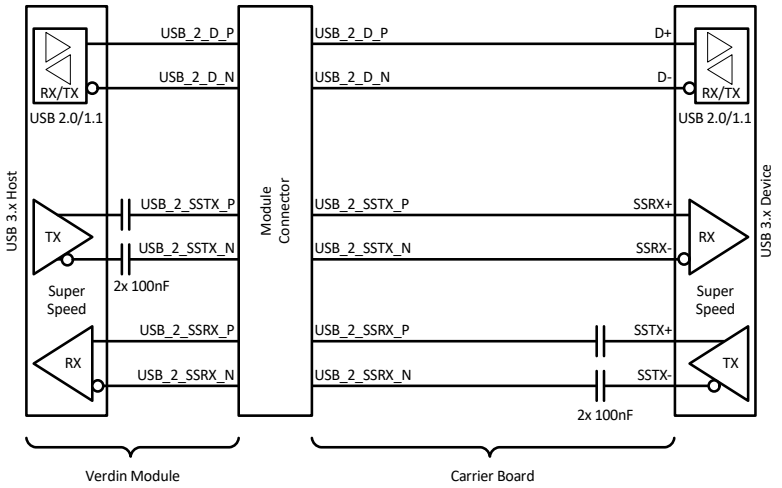


Figure 24: USB 3.0 device down block diagram

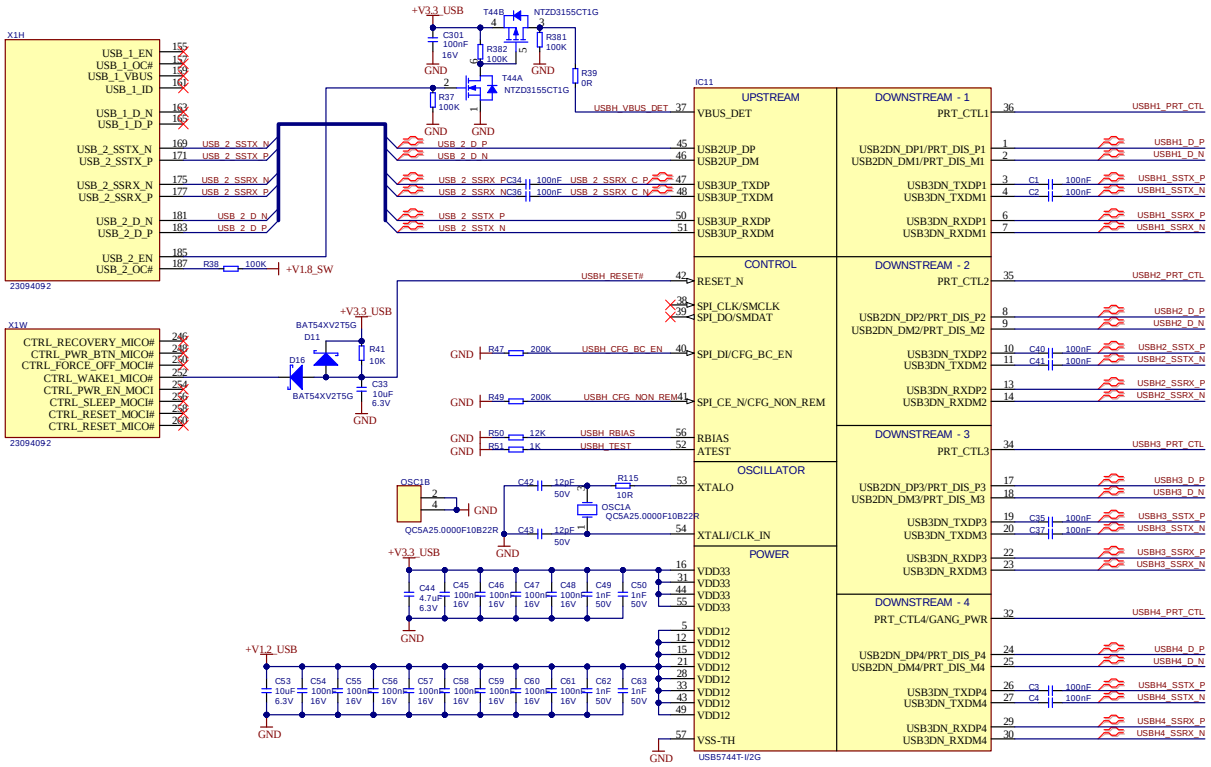


Figure 25: USB 3.0 device down reference schematic (USB3.1 Gen1 Hub)

2.4.2.6 USB 2.0 Host Connector Schematic Example

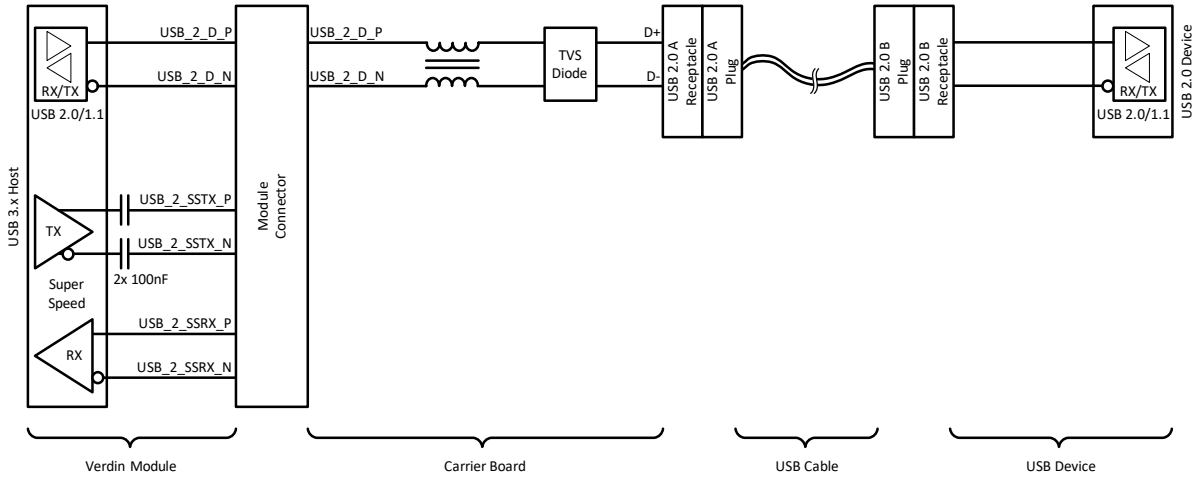


Figure 26: USB 2.0 host block diagram

Limiting the USB host port to USB 2.0 can cut costs on the carrier board. Additionally, not all Verdin modules support the SuperSpeed signals for the USB_2 port. Implementing a USB 2.0 host port means that the SuperSpeed signals of the module edge connector can be left unconnected. Since in the USB 2.0 specifications, the output current is limited to 500mA, the power budget on the 5V rail may be reduced, which can be another cost saver.

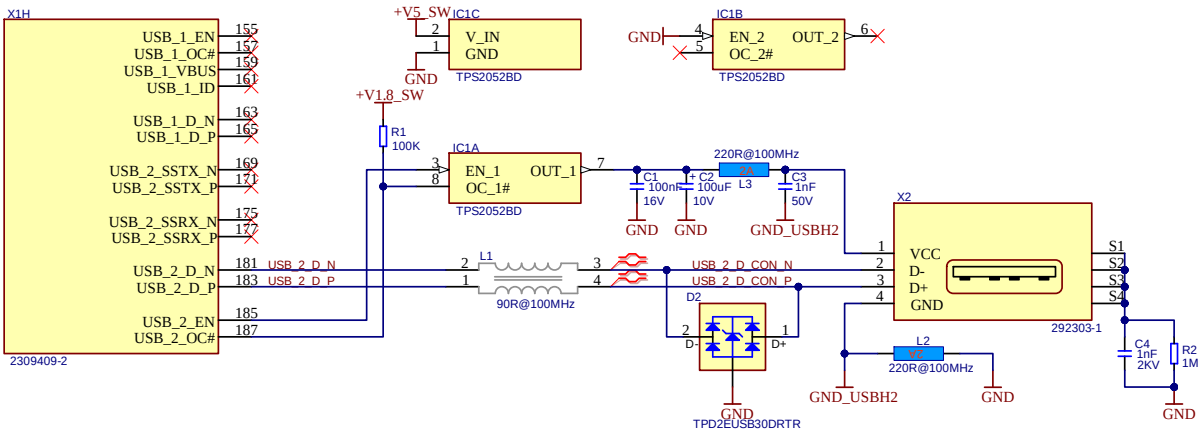


Figure 27: USB 2.0 host reference schematic

2.4.3 Unused USB Signal Termination

Verdin Pin	Verdin Signal Name	Recommended Termination
165	USB_1_D_P	Leave NC if not used
163	USB_1_D_N	Leave NC if not used
161	USB_1_ID	Leave NC and set the USB port direction in software to host or client OR ground the pin if it is used permanently as a host OR add pull-up resistor if the port is used as a slave.
159	USB_1_VBUS	Leave NC if not used
155	USB_1_EN	Leave NC if not used
157	USB_1_OC#	Add pull-up resistor or disable the over-current function in the software
183	USB_2_D_P	Leave NC if not used
181	USB_2_D_N	Leave NC if not used
177	USB_2_SSRX_P	Leave NC if not used
175	USB_2_SSRX_N	Leave NC if not used
171	USB_2_SSTX_P	Leave NC if not used

Verdin Pin	Verdin Signal Name	Recommended Termination
169	USB_2_SSTX_N	Leave NC if not used
185	USB_2_EN	Leave NC if not used
187	USB_2_OC#	Add pull-up resistor or disable the over-current function in the software

Table 11: Unused USB signal termination

2.5 HDMI/DVI

The HDMI and DVI interfaces use a TMDS compatible physical link to transfer video and optional audio data. Electrically, HDMI and DVI are equal, but there can be some differences in the protocol. HDMI is the DVI successor and specifies the additional transport for audio data and content protection (HDCP). HDMI devices (monitor, television set, among others.) can be driven with the DVI interface as HDMI is backward compatible. Compatibility is not guaranteed when attempting to drive a DVI device with an HDMI interface. Not all DVI displays accept the HDMI protocol or are HDCP compatible. Please read the datasheet of the Verdin module for more information about the supported HDMI and DVI protocols.

The HDMI and DVI interfaces define different connectors. There are passive adapters available in both directions. Please be aware that HDMI and HDCP have licensing restrictions in place. If you plan to implement HDMI in a final product, you need to check for the HDMI adopter license.

2.5.1 HDMI/DVI Signals

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
69	HDMI_1_TXC_P	O	TDMS		HDMI/DVI differential clock positive
67	HDMI_1_TXC_N	O	TDMS		HDMI/DVI differential clock negative
75	HDMI_1_TXD0_P	O	TDMS		HDMI/DVI differential data lane 0, positive
73	HDMI_1_TXD0_N	O	TDMS		HDMI/DVI differential data lane 0, negative
81	HDMI_1_TXD1_P	O	TDMS		HDMI/DVI differential data lane 1, positive
79	HDMI_1_TXD1_N	O	TDMS		HDMI/DVI differential data lane 1, negative
87	HDMI_1_TXD2_P	O	TDMS		HDMI/DVI differential data lane 2, positive
85	HDMI_1_TXD2_N	O	TDMS		HDMI/DVI differential data lane 2, negative
63	HDMI_1_CEC	I/O	OD	1.8V	HDMI consumer electronic control
61	HDMI_1_HPD	I	CMOS	1.8V	Hot Plug Detect
57	I2C_3_HDMI_SDA	I/O	OD	1.8V	I2C interface for reading the extended display identification data (EDID) over DDC. This interface is shared with other display interfaces
59	I2C_3_HDMI_SCL	O	OD	1.8V	

Table 12: HDMI/DVI signals

2.5.2 Reference Schematics

2.5.2.1 DVI Schematic Example

There are different DVI connector configurations available. The DVI-D (digital) supports only the native DVI signals. The DVI-A (analog) provides only analog VGA signals. The DVI-I (integrated) combines the digital DVI signals and the analog VGA signals. For the DVI-A and DVI-I, there are passive adapters to the D-SUB VGA connector available. There is only one DDC channel available on the DVI-I interface. Therefore, the connector is not designed to use both links (DVI and VGA) simultaneously.

Nevertheless, there are Y-cables available that provide a DVI and VGA output. Such cables are not standardized. They provide the DDC on either the DVI or VGA output. Please be aware of this when using a similar Y-cable.

The following schematic example shows a DVI-D implementation since the Verdin module does not provide a VGA output. The DDC signals require a level shifter since the signal level on the Verdin module is 1.8V while the DVI uses 5V. The same is necessary for the hotplug detect signal. The TDMS signals need to be ESD protected using diodes. The schematic example shows a discrete solution for the level shifting and protection. There are integrated solutions also available.

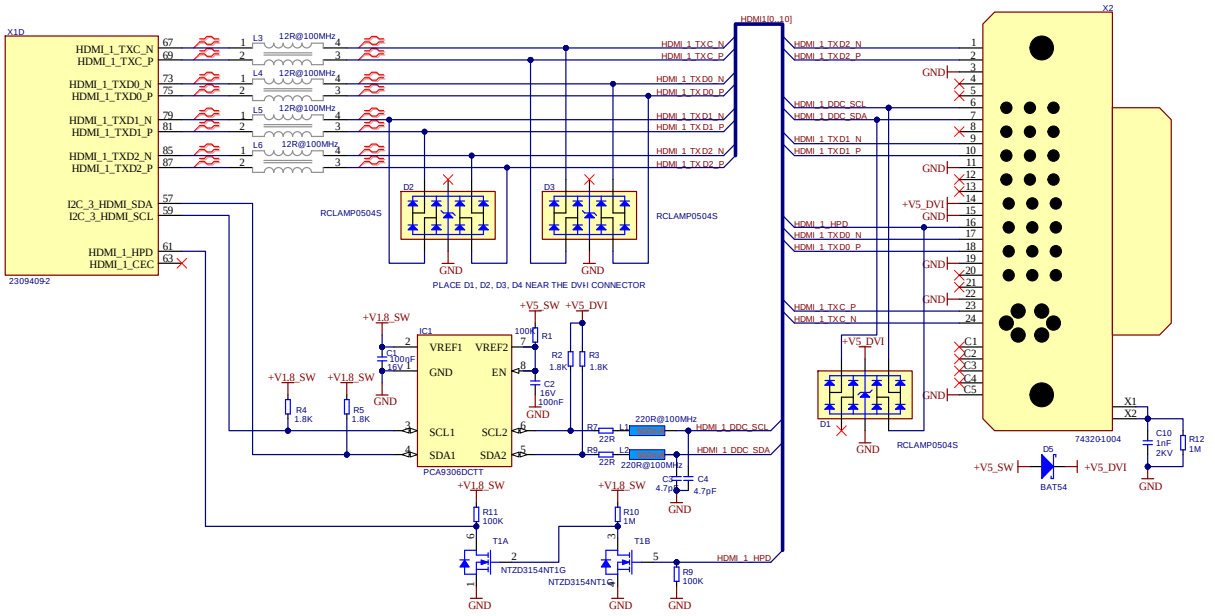


Figure 28: DVI-D reference schematic

2.5.2.2 HDMI Schematic Example

The HDMI connector does not feature an Analog VGA interface, but an optional Consumer Electronics Control (CEC) interface is available. This one-wire interface is used to control consumer audio and video devices such as televisions or AV receivers. There are many different CEC trade names (VIERA Link, Anynet+, EasyLink, Aquos Link, BRAVIA Link, and others.) The CEC is a 3.3V interface on the HDMI connector. Therefore, a level shifter is required.

The I²C signals for the DDC and the hot-plug detection (HPD) need to be shifted to/from the 5V logic level of the HDMI interface to the Verdin module signal level of 1.8V. The DDC requires external pull-up resistors on the carrier board.

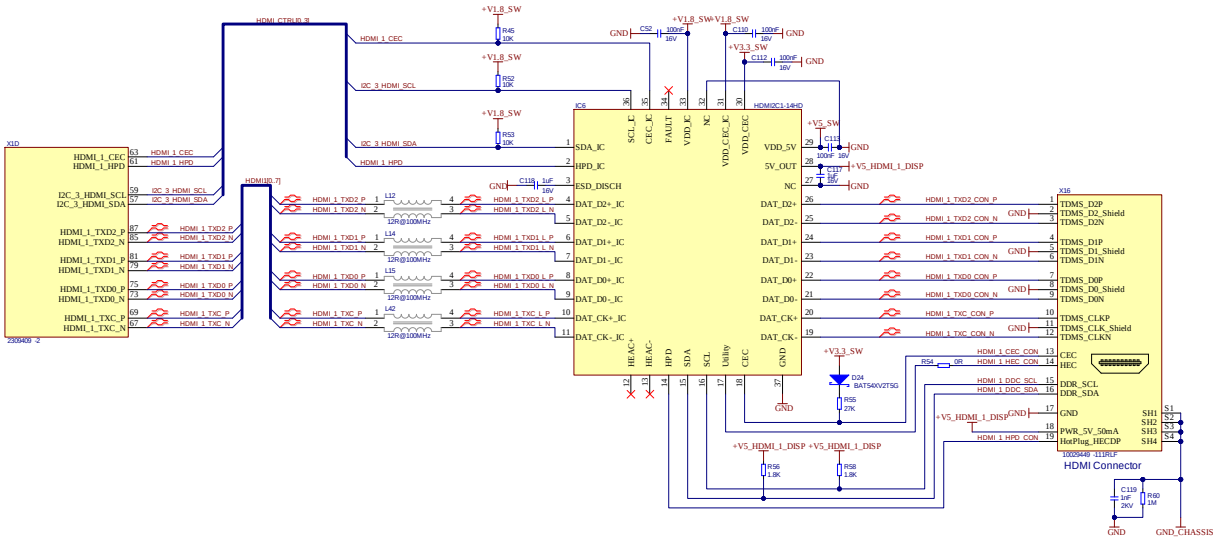


Figure 29: HDMI reference schematic

2.5.3 Unused HDMI/DVI Signal Termination

All unused HDMI/DVI signals can be left unconnected.

Verdin Pin	Verdin Signal Name	Recommended Termination
69	HDMI_1_TXC_P	Leave NC if not used
67	HDMI_1_TXC_N	Leave NC if not used
75	HDMI_1_TXD0_P	Leave NC if not used
73	HDMI_1_TXD0_N	Leave NC if not used
81	HDMI_1_TXD1_P	Leave NC if not used
79	HDMI_1_TXD1_N	Leave NC if not used
87	HDMI_1_TXD2_P	Leave NC if not used
85	HDMI_1_TXD2_N	Leave NC if not used
63	HDMI_1_CEC	Add pull-up resistor or disable the CEC function in the software
61	HDMI_1_HPD	Add pull-up resistor or disable the HDMI function in the software
57	I2C_3_HDMI_SDA	Add pull-up resistor or disable the I2C function in the software
59	I2C_3_HDMI_SCL	Add pull-up resistor or disable the I2C function in the software

Table 13: Unused HDMI/DVI signal termination

2.6 Display Serial Interface (MIPI DSI)

The Digital Serial Interface (DSI) is specified by the Mobile Industry Processor Interface Alliance (MIPI) and is available as a "Reserved" interface on the Verdin module specifications. The interface targets to connect high-resolution displays with low energy consumption. The interface is intended to be used for internal displays with shorter cable lengths.

The interface consists of a differential pair bit clock and between one and four differential data signal lanes. While the data lanes 1 to 3 are traveling from the module to the display, the lane 0 is bidirectional. This lane is capable of a bus turnaround (BTA) for commands. In the low power mode, the separate clock signal is disabled. The clock is then embedded into the data lanes. However, image data can only be sent in the high-speed mode, which also uses the external clock signal.

2.6.1 MIPI DSI Signals

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
37	DSI_1_CLK_P	O	D-PHY		MIPI DSI differential clock positive
35	DSI_1_CLK_N	O	D-PHY		MIPI DSI differential clock negative
49	DSI_1_D0_P	I/O	D-PHY		MIPI DSI differential data lane 0, positive
47	DSI_1_D0_N	I/O	D-PHY		MIPI DSI differential data lane 0, negative
43	DSI_1_D1_P	O	D-PHY		MIPI DSI differential data lane 1, positive
41	DSI_1_D1_N	O	D-PHY		MIPI DSI differential data lane 1, negative
31	DSI_1_D2_P	O	D-PHY		MIPI DSI differential data lane 2, positive
29	DSI_1_D2_N	O	D-PHY		MIPI DSI differential data lane 2, negative
25	DSI_1_D3_P	O	D-PHY		MIPI DSI differential data lane 3, positive
23	DSI_1_D3_N	O	D-PHY		MIPI DSI differential data lane 3, negative
55	I2C_2_DSI_SCL	O	OD	1.8V	I^2C interface, intended to be used as DDC
53	I2C_2_DSI_SDA	I/O	OD	1.8V	
19	PWM_3_DSI	I/O	CMOS	1.8V	Dedicated PWM output for the display backlight brightness control, could also be used as general-purpose IO
17	GPIO_9_DSI	I/O	CMOS	1.8V	Dedicated general-purpose IO for DSI bridges
21	GPIO_10_DSI	I/O	CMOS	1.8V	Dedicated general-purpose IO for DSI bridges

Table 14: MIPI DSI signals

Additional to the high-speed MIPI DSI signals, the Verdin reserves also pins for a dedicated I^2C, a PWM, and two GPIOs for the DSI interface. These signals are intended to be used for controlling an attached display as well as DSI bridges. Some DSI bridges can embed also sound in the interface (e.g., HDMI). The I2S_2 interface is recommended to be used in combination with the DSI interface. The following table shows how the additional signals are recommended to be used for the different use cases. Whenever possible, follow these recommendations to be software compatible with the reference designs.

Verdin Pin	Verdin Signal Name	MIPI DSI Display	DSI to HDMI Bridge	DSI to LVDS Bridge	DSI to RGB Bridge
55	I2C_2_DSI_SCL	Reserved	HDMI DDC	Reserved	Reserved
53	I2C_2_DSI_SDA	Reserved	HDMI DDC	Reserved	Reserved
19	PWM_3_DSI	Display Brightness	HDMI HPD	Display Brightness	Display Brightness
17	GPIO_9_DSI	Reserved	Bridge Interrupt	Bridge Interrupt Touch Interrupt	Bridge Interrupt Touch Interrupt
21	GPIO_10_DSI	Reserved	Bridge Reset	Bridge Reset	Bridge Reset
48	I2S_2_D_IN	Reserved	Reserved	Reserved	Reserved
46	I2S_2_D_OUT	Display Backlight Enable	HDMI Audio	Display Backlight Enable	Display Backlight Enable
44	I2S_2_SYNC	Reserved	HDMI Audio	Reserved	Reserved
42	I2S_2_BCLK	Touch Reset	HDMI Audio	Touch Reset	Touch Reset

Table 15: Recommended Usage of DSI Control Signals

2.6.2 Reference Schematics

Besides attaching a display directly to the MIPI DSI interface, there are many display adapters available. The following display adapters are also available as add-on boards for the Verdin reference designs. Therefore, bridges used on these adapters are supported by the regular BSP for the Verdin modules.

2.6.2.1 DSI to HDMI Schematic Example

This reference schematic uses Lontium Semiconductor LT8912B MIP DSI to HDMI bridge. The bridge requires all four DSI lanes. The bridge supports up to 1080p60 and has an I²S interface for embedding a stereo audio output channel into the HDMI stream.

We recommend using the I2C_1 port for communicating with the bridge, not the I2C_2_DSI. The LT8912B uses the same I²C addresses as the regular HDMI monitors for the DDC. Therefore, the I²C interface of the LT8912B cannot be on the same I²C bus as the HDMI DDC.

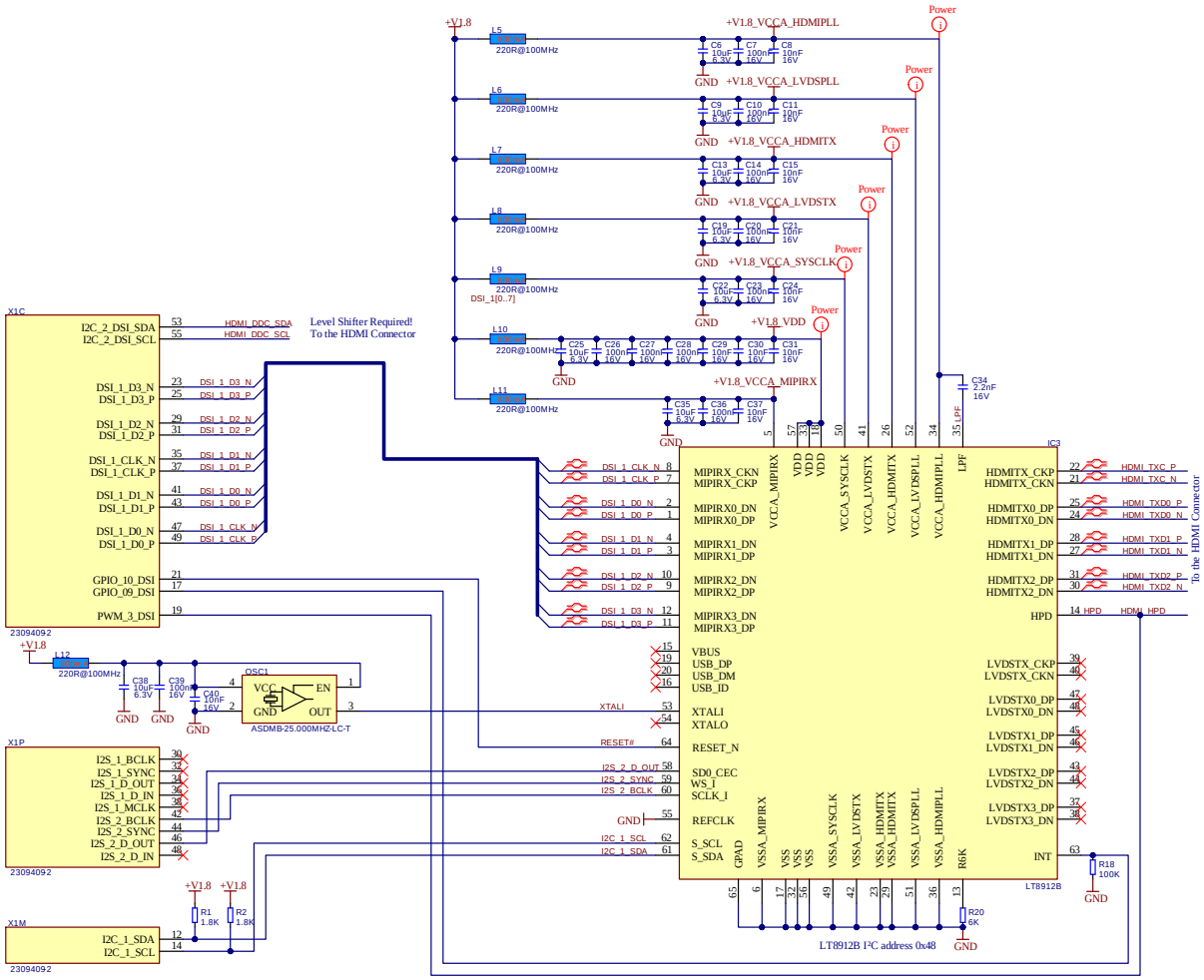


Figure 30: DSI to HDMI reference schematic

2.6.2.2 DSI to LVDS Schematic Example

The official name for the LVDS interface is FPD-Link or FlatLink. However, in this document, we use the more common term LVDS. The Texas Instruments SN65DSI84-Q1 is a DSI to LVDS bridge that can be configured for single-channel and dual-channel LVDS output. In the dual-channel mode, it supports up to 1080p60 with 24bit color. Depending on the resolution, the bridge requires one, two, or all four DSI lanes for operation.

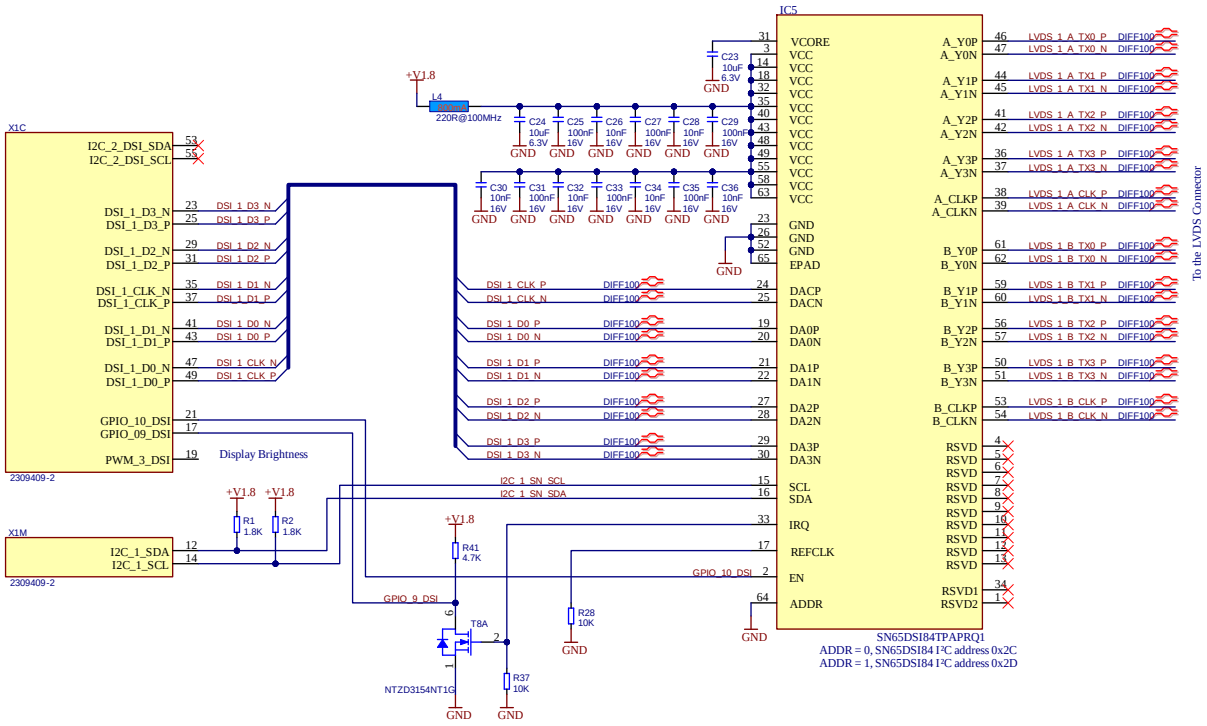


Figure 31: DSI to LVDS reference schematic

2.6.2.3 DSI to Parallel RGB Schematic Example

The DSI to parallel RGB bridge TC358867XBG from Toshiba in the schematic below only supports 1.8V logic level at the RGB output signals. Depending on the display, a level shifter is required.

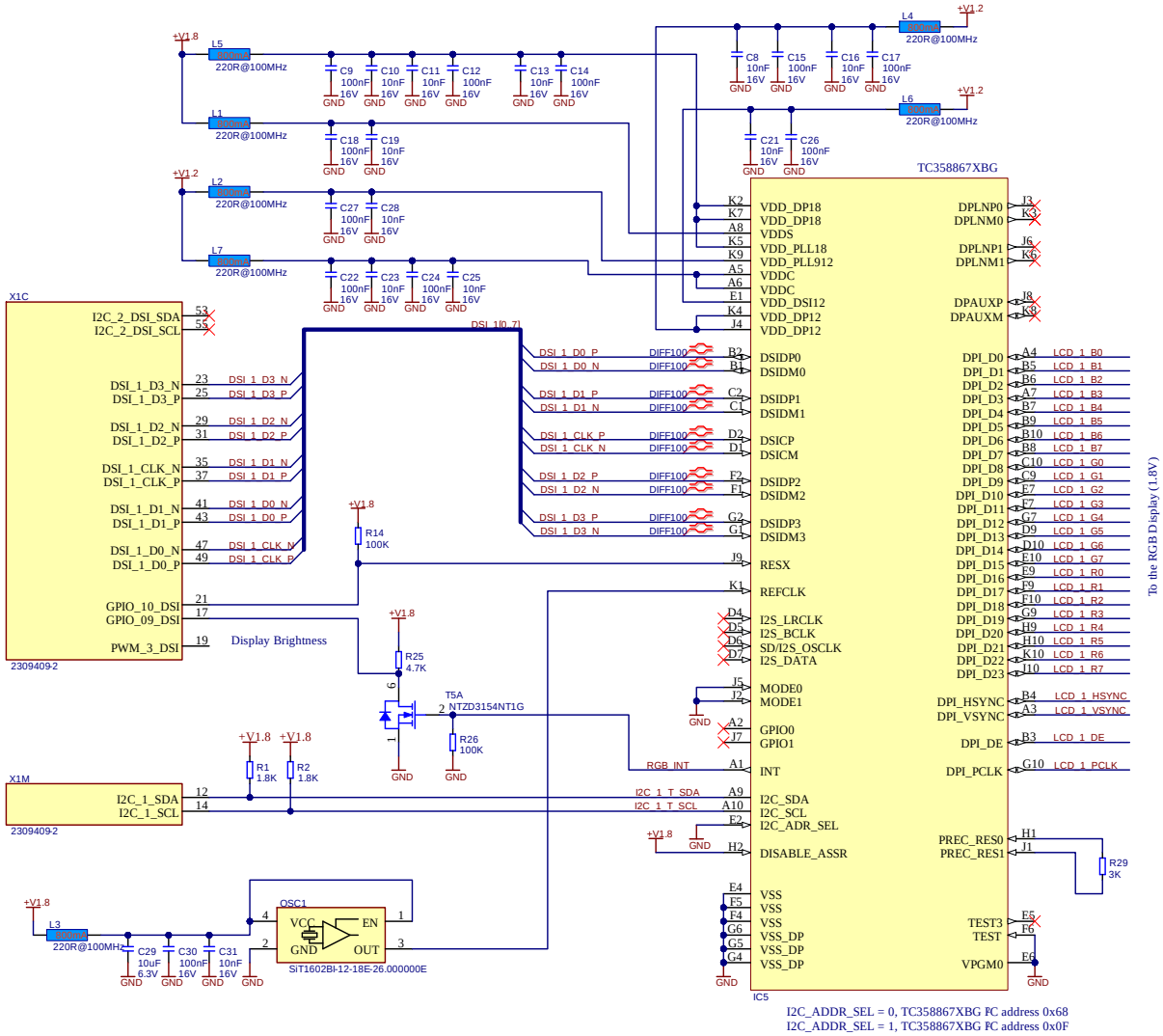


Figure 32: DSI to Parallel RGB reference schematic

2.6.3 MIPI DSI Display Adapters

Toradex offers several MIPI DSI display adapters for bridging to HDMI, LVDS, parallel RGB, and other standard display interfaces. These simple and flexible products are meant to be used primarily for evaluation purposes. The adapters are based on the Samtec LSS-130-03-L-DV-A-K-TR high-speed connector (https://www.samtec.com/products/lss-130-03-l-dv-a-k-tr). This connector is hermaphroditic, which means that the same connector is used on the carrier board and the display adapter. However, the location of pin 1 needs to be different for mating these two boards together.

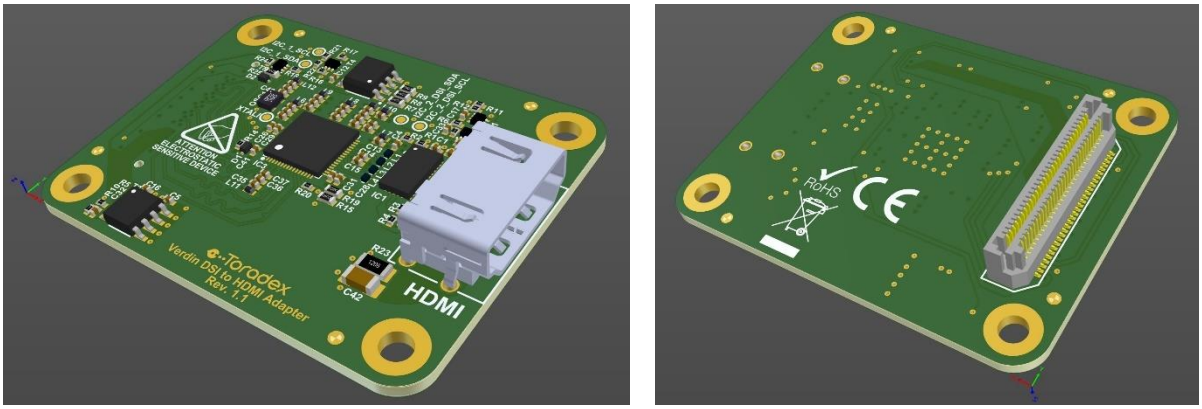


Figure 33: Front and backside of Verdin DSI to HDMI Adapter

The following table contains the pinout of the MIPI DSI display adapter connector and its recommended connection on the carrier board. The direction is indicated from the adapter point of view.

Adapter Pin	Adapter Signal Name	I/O	Type	Power Rail	Description
24	DSI_1_CLK_P	I	D-PHY		MIPI DSI differential clock
26	DSI_1_CLK_N				
12	DSI_1_D0_P	I/O	D-PHY		MIPI DSI differential data lane 0
14	DSI_1_D0_N				
18	DSI_1_D1_P	I	D-PHY		MIPI DSI differential data lane 1
20	DSI_1_D1_N				
30	DSI_1_D2_P	I	D-PHY		MIPI DSI differential data lane 2
32	DSI_1_D2_N				
36	DSI_1_D3_P	I	D-PHY		MIPI DSI differential data lane 3
38	DSI_1_D3_N				
52	I2C_2_DSI_SCL	I	OD	1.8V	I^2C interface, intended to be used as DDC
54	I2C_2_DSI_SDA	I/O			
58	PWM_3_DSI	I/O	CMOS	1.8V	Dedicated PWM for the display backlight brightness control, could also be used as general-purpose IO
8	GPIO_9_DSI	I/O	CMOS	1.8V	Dedicated general-purpose IO for DSI bridges
56	GPIO_10_DSI	I/O	CMOS	1.8V	Dedicated general-purpose IO for DSI bridges
48	I2S_2_D_IN	O	CMOS	1.8V	Serial audio input data stream to the Verdin Module
46	I2S_2_D_OUT	I	CMOS	1.8V	Serial audio output data stream from the Verdin Module
44	I2S_2_SYNC	I/O	CMOS	1.8V	Synchronization/ field select/ left-right channel select
42	I2S_2_BCLK	I/O	CMOS	1.8V	Serial bit clock
6	I2C_1_SCL	I	OD	1.8V	General-purpose I^2C interface, intended to be used for controlling the bridge IC and the touch interface
4	I2C_1_SDA	I/O			
57	CTRL_RESET_MOCI#	I	OD	3.3V Tolerant	General reset signal
59	DSI_1_PWR_EN	I	CMOS	1.8V	Power enable signal for the bridge
43, 45, 47, 49, 51	+V1.8_SW	I	PWR	1.8V	
31, 33, 35, 37, 39	+V3.3_SW	I	PWR	3.3V	
19, 21, 23, 25, 27	+V5_SW	I	PWR	5V	
7, 9, 11, 13, 15	+V_SUPPLY_FILT_SW	I	PWR	7-24V	
3, 10, 16, 22, 28, 34, 40, 50, 55, 60	GND				
1, 2, 5, 17, 29, 41, 53	NC				

Table 16: MIP DSI display adapter

Since the MIPI DSI display adapter connector is hermaphroditic, special attention must be taken to the pin numbering. Even though the adapter and the carrier board connector are identical, the pin numbering must be different.

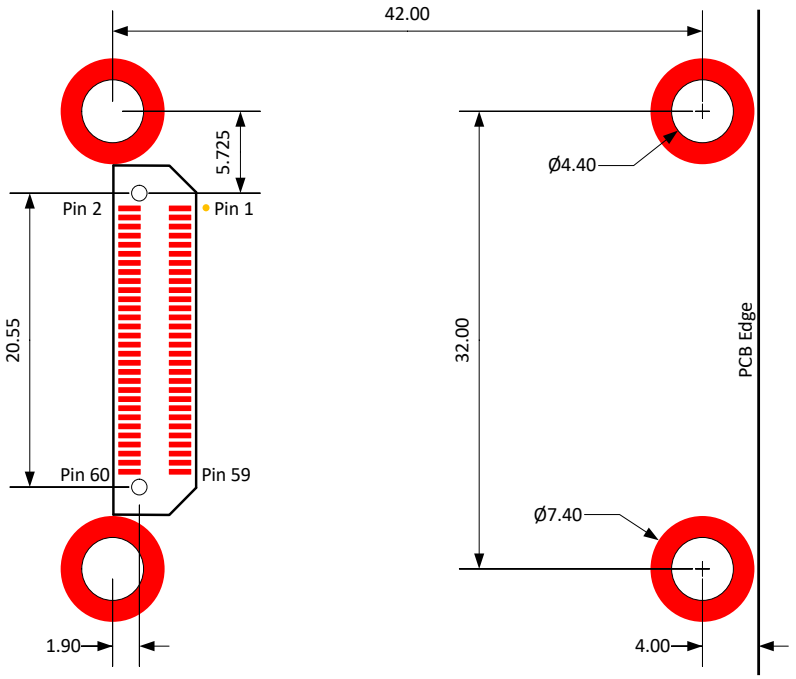


Figure 34: Carrier board dimensions for MIPI DSI display adapter (top view)

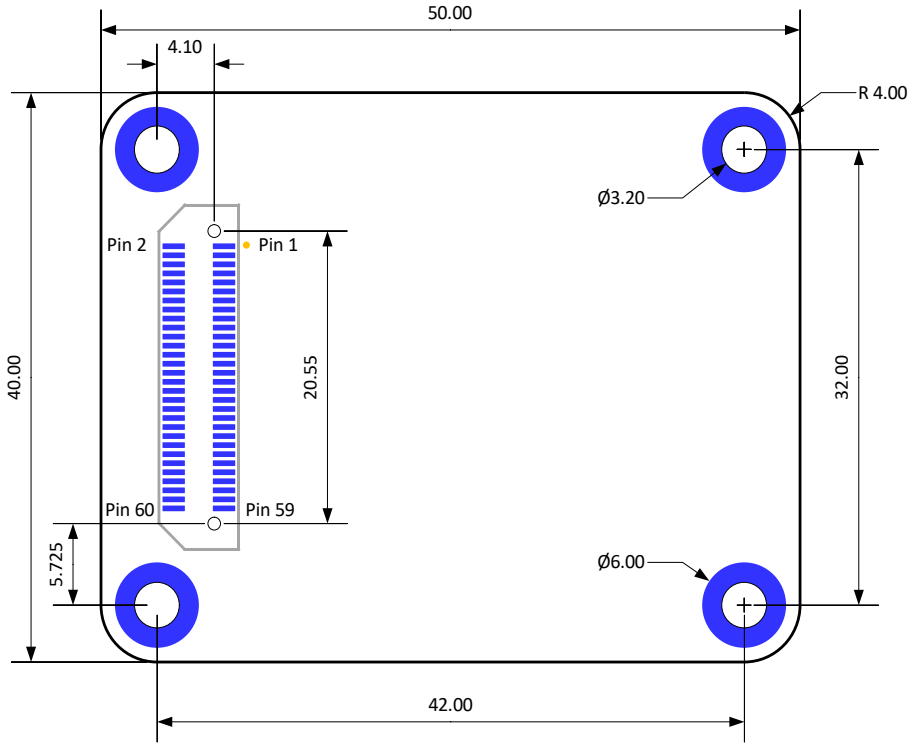


Figure 35: MIPI DSI display adapter dimensions (top view through the PCB)

2.6.4 Unused MIPI DSI Signal Termination

All unused MIPI DSI signals can be left unconnected.

Verdin Pin	Verdin Signal Name	Recommended Termination
37	DSI_1_CLK_P	Leave NC if not used
35	DSI_1_CLK_N	Leave NC if not used
49	DSI_1_D0_P	Leave NC if not used
47	DSI_1_D0_N	Leave NC if not used
43	DSI_1_D1_P	Leave NC if not used
41	DSI_1_D1_N	Leave NC if not used
31	DSI_1_D2_P	Leave NC if not used
29	DSI_1_D2_N	Leave NC if not used
25	DSI_1_D3_P	Leave NC if not used
23	DSI_1_D3_N	Leave NC if not used
55	I2C_2_DSI_SCL	Add pull-up resistor or disable the I2C function in the software
53	I2C_2_DSI_SDA	Add pull-up resistor or disable the I2C function in the software
19	PWM_3_DSI	Leave NC if not used
17	GPIO_9_DSI	Leave NC if not used
21	GPIO_10_DSI	Leave NC if not used

Table 17: Unused MIPI DSI signal termination

2.7 Camera Serial Interface (MIPI CSI-2)

The Camera Serial Interface (CSI) from the Mobile Industry Processor Interface Alliance (MIPI) is related to the MIPI DSI, intended to be used for displays. The Verdin standard reserves up to four lanes for the version CSI-2. This interface version uses the MIPI D-PHY as a physical layer which is also used for the MIPI DSI interface on the Verdin module. As with the MIPI DSI, the first data lane is bidirectional.

The MIPI CSI-2 supports different camera formats (e.g., RGB, YUV, YCbCr, RAW Bayer, and others.). Please carefully check the datasheet of the Verdin module whether it supports the format of the camera. Also, the maximum interface speed and supported camera resolution depend on the module.

2.7.1 MIPI CSI-2 Signals

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
111	CSI_1_CLK_P	I	D-PHY		MIPI CSI-2 differential clock positive
113	CSI_1_CLK_N	I	D-PHY		MIPI CSI-2 differential clock negative
123	CSI_1_D0_P	I/O	D-PHY		MIPI CSI-2 differential data lane 0, positive
125	CSI_1_D0_N	I/O	D-PHY		MIPI CSI-2 differential data lane 0, negative
117	CSI_1_D1_P	I	D-PHY		MIPI CSI-2 differential data lane 1, positive
119	CSI_1_D1_N	I	D-PHY		MIPI CSI-2 differential data lane 1, negative
105	CSI_1_D2_P	I	D-PHY		MIPI CSI-2 differential data lane 2, positive
107	CSI_1_D2_N	I	D-PHY		MIPI CSI-2 differential data lane 2, negative
99	CSI_1_D3_P	I	D-PHY		MIPI CSI-2 differential data lane 3, positive
101	CSI_1_D3_N	I	D-PHY		MIPI CSI-2 differential data lane 3, negative
95	I2C_4_CSI_SCL	O	OD	1.8V	I2C interface, intended to be used for controlling the camera
93	I2C_4_CSI_SDA	I/O	OD	1.8V	
91	CSI_1_MCLK	O	CMOS	1.8V	Master clock output for the camera.
216	GPIO_5_CSI	I/O	CMOS	1.8V	Reserved GPIO for MIPI CSI interface
218	GPIO_6_CSI	I/O	CMOS	1.8V	Reserved GPIO for MIPI CSI interface
220	GPIO_7_CSI	I/O	CMOS	1.8V	Reserved GPIO for MIPI CSI interface
222	GPIO_8_CSI	I/O	CMOS	1.8V	Reserved GPIO for MIPI CSI interface

Table 18: MIPI CSI-2 signals

2.7.2 Reference Schematics

The master clock output on the module edge connector pin 91 can reduce the BOM cost. However, for longer camera cables or trace length on the carrier board, the master clock signal can become a source for EMI issues. Check also whether the selected Verdin module can provide the correct frequency for the camera. Alternatively, an external oscillator or crystal can be used. It is recommended to put this oscillator as close as possible to the camera.

The ESD protection diodes and the common-mode chokes are optional. The protection diodes are only required if the cables are accessible, or the display does not have enough protection. The chokes can reduce EMI if the camera cable is longer.

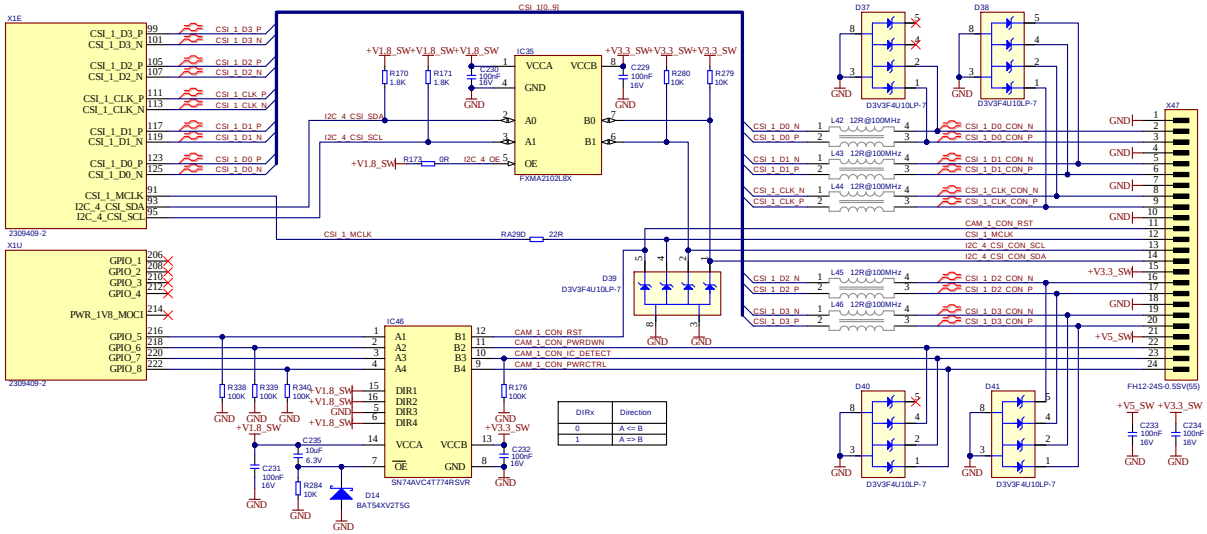


Figure 36: MIPI CSI-2 reference schematic

2.8 SD/MMC/SDIO

The Verdin module form factor features one SDIO interface as "Always Compatible". The interface provides 4 data bit which can be used for interfacing SD, SDIO, MMC and eMMC devices.

The SD cards support different bus speed modes. The required signal voltage depends on the bus speed mode. In UHS-I (Ultra High Speed), the signaling voltage must be changed from 3.3V to 1.8V. In the Verdin module definition, all GPIO capable interfaces are defined for 1.8V only. The SDIO interface pins are an exception here. To be compliant with older SD cards, IO pins need to start the communication at a 3.3V voltage level. Therefore, the IO voltage rail of the SD card signals is switchable between 1.8V and 3.3V voltage levels.

Some Verdin modules may feature additional SD interfaces as alternate functions of other interfaces or on the "Module-specific" pins. Some of these additional SD interfaces may support only 1.8V IO voltage levels. Since a detachable SD card needs to start the negotiation at a 3.3V voltage level, these ports can only be used for permanently attached devices like an eMMC memory or an SDIO peripheral device.

Bus Speed Mode	Max. Clock Frequency	Max. Bus Speed	Signal Voltage	Remarks
Default Speed	25 MHz	12.5 MB/s	3.3V	Default Speed
High Speed	50 MHz	25 MB/s	3.3V	High Speed
SDR12	25 MHz	12.5 MB/s	1.8V	UHS-I
SDR25	50 MHz	25 MB/s	1.8V	
DDR50	50 MHz	50 MB/s	1.8V	
SDR50	100 MHz	50 MB/s	1.8V	
SDR104	208 MHz	104 MB/s	1.8V	

Table 19: SD Card Bus Speed Modes

2.8.1 SD/MMC/SDIO Signals

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
80	SD_1_D0	I/O	CMOS	1.8V/3.3V	Data signals [3:0] - used for SD, MMC, and SDIO interfaces; pull-up resistors on the module
82	SD_1_D1	I/O	CMOS	1.8V/3.3V	
70	SD_1_D2	I/O	CMOS	1.8V/3.3V	
72	SD_1_D3	I/O	CMOS	1.8V/3.3V	
74	SD_1_CMD	I/O	CMOS	1.8V/3.3V	Command signal; pull-up resistors on the module
78	SD_1_CLK	O	CMOS	1.8V/3.3V	Clock output
84	SD_1_CD#	I	OD	1.8V/3.3V	Card detect; pull-up resistors on the module
76	SD_1_PWR_EN	O	CMOS	1.8V/3.3V	Power Enable output

Table 20: 4bit SD/MMC/SDIO signals

The SD card bus signals (SD_1_D[0..3], SD_1_CMD, and SD_1_CLK) switch their input voltage range altogether. The card-detect (SD_1_CD#) and the power-enable (SD_1_PWR_EN) signals may change their IO voltage together with the bus or remain at 1.8V. The behavior depends on the Verdin module. The circuit on the carrier board needs to have different IO voltages on these pins, depending on the module and the inserted card.

2.8.2 Reference Schematics

Even though the SD card signals change their voltage between 1.8V and 3.3V, the card is always powered with 3.3V. The signal pull-up resistors of the interface are located on the module or inside the SoC. There are no pull-up resistors required on the carrier board. Therefore, there is no need for a voltage rail on the carrier board that switches between 1.8V and 3.3V.

Depending on the Verdin module, the IO voltage of the card-detect (SD_1_CD#) and the power-enable (SD_1_PWR_EN) signals may also change together with the SD bus signals from 3.3V to 1.8V. The circuit on the carrier board needs to be able to work with both IO voltage levels. The card detect signal is an open-drain input with the pull-up resistor on the module. This means the carrier board has only to short this pin simply to ground when the card is inserted.

The SD card interface does not have a dedicated reset input. The only way to reset a card is to power cycle it. When changing the bus voltage from 1.8V to 3.3V, officially, the card needs to be reset. A reset could also be required if the card is not responding anymore. However, most cards work without the need for a reset. Nevertheless, we recommend implementing a card-reset by adding a switch to the SD card's supply voltage. The Microchip MIC94073 power switch in the reference schematic features a built-in logic shifter that can handle 1.8V or 3.3V as logic high for the SD_1_PWR_EN signal.

There is no dedicated write-protection signal available on the standard Verdin pin-out. Any free GPIO capable signal can be used if the write-protection function is required. The ESD protection diodes are optional. Whether the protection is required or not depends on how accessible the card slot is to the user.

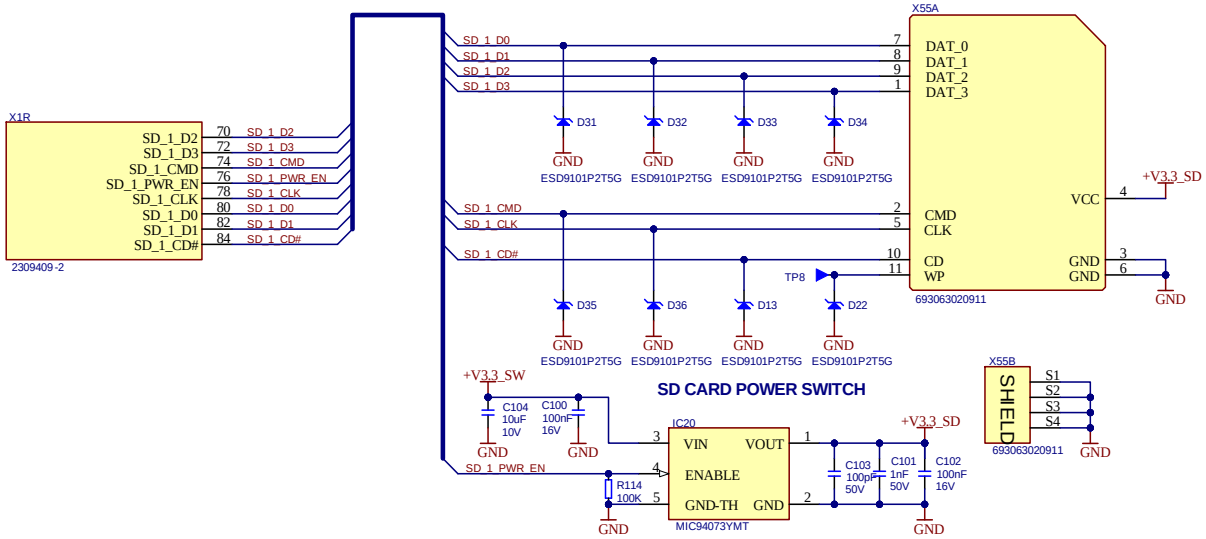


Figure 37: 4bit SD Card Reference Schematic

2.8.3 Unused SD/MMC/SDIO Interface Signal Termination

All unused SD interface signals can be left unconnected. If the SD/MMC/SDIO port is unused, the signal could be used as GPIO. Check the datasheet of the Verdin module whether there are any restrictions for using the signals as GPIOs.

2.9 I²C

The Verdin module standard features four I²C interfaces. The interface I2C_1 is a general-purpose I²C and is in the "Always Compatible" interface group. The additional three I²C ports are in the "Reserved" group and are dedicated to other interfaces. I2C_2_DSI is dedicated to the MIPI DSI port, I2C_3_HDMI is dedicated to the HDMI port, and I2C_4_CSI is dedicated to the MIPI CSI port. Check the Verdin datasheet whether these I²C ports can be used as general-purpose interfaces. Some modules do not provide all four I²C ports. Whether a port is available or not depends on whether the interface they are dedicated to is existing.

The I²C interfaces do not feature any pull-up resistors on the module. It is required to add pull-up resistors for the data and clock lines on the carrier board. The pull-up resistor value is typically

between 1Ω and 10kΩ. A small pull-up resistor increases power consumption, while a large resistor could lead to signal quality problems. The optimum size of the resistor depends on the capacitive load on the I²C lines and the required bus speed.

2.9.1 I²C Signals

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
14	I2C_1_SCL	I/O	OD	1.8V	General-purpose I²C interface
12	I2C_1_SDA	O	OD	1.8V	
55	I2C_2_DSI_SCL	I/O	OD	1.8V	Dedicated I²C port for the MIPI DSI
53	I2C_2_DSI_SDA	O	OD	1.8V	
59	I2C_3_HDMI_SCL	I/O	OD	1.8V	Dedicated I²C port for the HDMI port (DDC)
57	I2C_3_HDMI_SDA	O	OD	1.8V	
95	I2C_4_CSI_SCL	I/O	OD	1.8V	Dedicated I²C port for the MIPI CSI
93	I2C_4_CSI_SDA	O	OD	1.8V	

Table 21: I²C signals

2.9.2 Reference Schematics

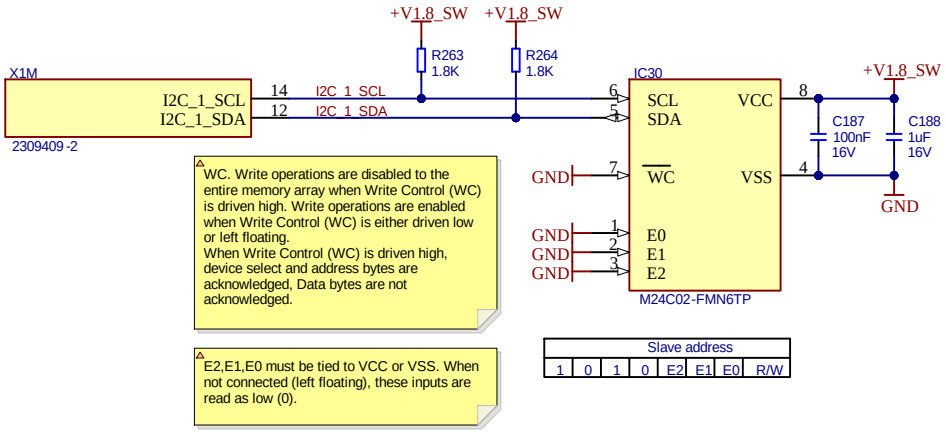


Figure 38: EEPROM Reference Schematic

2.9.3 Unused I²C Signal Termination

All unused I²C can be left unconnected if the I²C port is switched off in software. Otherwise, it is recommended to keep the pull-up resistors available. Unused I²C signals can be configured as GPIO.

2.10 UART

There are four UART ports available in the Verdin module standard. UART_1 and UART_2 are general-purpose interfaces. The RX and TX signals of these interfaces are in the "Always Compatible" section, while the additional RTS/CTS signals for hardware flow control are in the "Reserved" group.

UART_3 is in the "Always Compatible" section and is intended to be used for main OS debug log output. It could be used for general purposes, but we recommend making this interface available for debugging purposes. UART_4 is in the "Reserved" class. On modules with a real-time core, this instance is intended to be used as the debug log output of the real-time operating system. The interface may be used as a general-purpose UART.

Please note that changing the default UART interface instances being used for debug log output or serial console purposes is not supported in software. It is highly recommended to use the default UART interface instances specified for these purposes.

2.10.1 UART Signals

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
129	UART_1_RXD	I	CMOS	1.8V	Received Data of general-purpose UART_1
131	UART_1_TXD	O	CMOS	1.8V	Transmitted Data of general-purpose UART_1
137	UART_2_RXD	I	CMOS	1.8V	Received Data of general-purpose UART_2
139	UART_2_TXD	O	CMOS	1.8V	Transmitted Data of general-purpose UART_2
147	UART_3_RXD	I	CMOS	1.8V	Received Data for main OS debug UART_3
149	UART_3_TXD	O	CMOS	1.8V	Transmitted Data for main OS debug UART_3

Table 22: "Always Compatible" UART Signals

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
133	UART_1_RTS	O	CMOS	1.8V	Request to Send of general-purpose UART_1
135	UART_1_CTS	I	CMOS	1.8V	Clear to Send of general-purpose UART_1
141	UART_2_RTS	O	CMOS	1.8V	Request to Send of general-purpose UART_2
143	UART_2_CTS	I	CMOS	1.8V	Clear to Send of general-purpose UART_2
151	UART_4_RXD	I	CMOS	1.8V	Received Data for real-time core debug UART_4
153	UART_4_TXD	O	CMOS	1.8V	Transmitted Data for real-time core debug UART_4

Table 23: "Reserved" UART Signals

2.10.2 Reference Schematics

2.10.2.1 RS232 Reference Schematics

The RS232 interface can be classified as Data Terminal Equipment (DTE) or Data Communication Equipment (DCE). This classification is inherited from the usage of the interface for modems. The signal direction of these modes is different. Some Verdin modules might allow changing the mode and, therefore, also the data direction, but this is not a mandatory requirement. According to the Verdin specifications, the interface is intended to be used in the DTE configuration.

Signal	Name	Usage	DTE Direction (Verdin standard)	DCE Direction
UART_1_RXD	Received Data	Data from DCE to DTE	Input	Output
UART_1_TXD	Transmitted Data	Data from DTE to DCE	Output	Input
UART_1_RTS	Request to Send	DTE request to DCE be prepared to receive data	Output	Input
UART_1_CTS	Clear to Send	DCE indicates ready to accept data	Input	Output

Table 24: RS232 Signal Modes

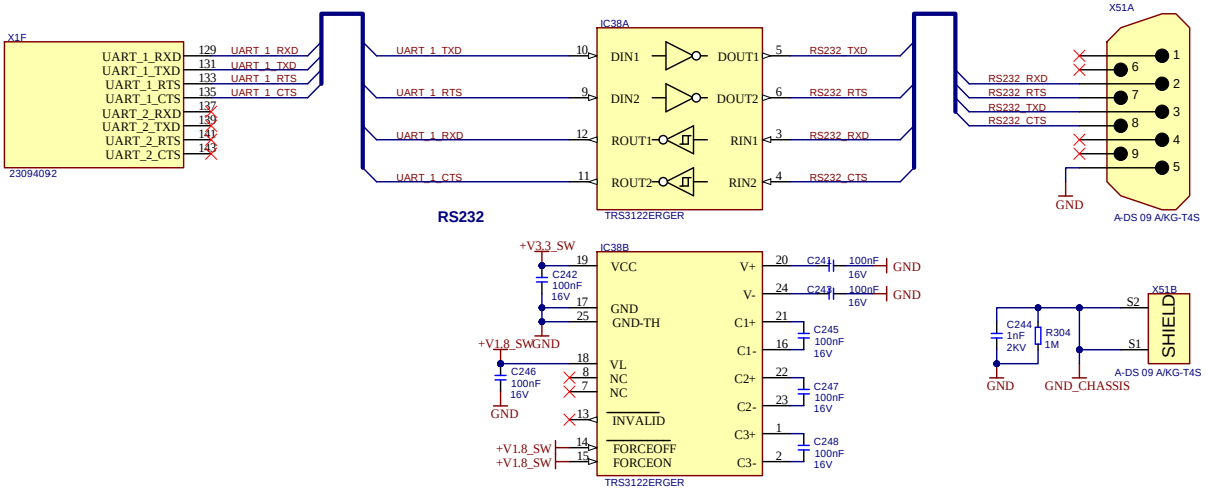


Figure 39: RS232 Reference Schematic

2.10.2.2 RS422 Reference Schematics

The RS422 is a full-duplex serial interface with differential pair signals. This allows higher data rates over longer distances as with the RS232. Since the RS422 has separate RX and TX signal pairs, no additional control signals are required for changing the signal direction. This means the RS422 requires only the RX and TX signals of the UART interface. Therefore, it is possible to use any of the four standard UART interfaces of the Verdin standard.

The RS422 specification does not contain a connector. Therefore, there is no standard connector for this interface available. The reference schematic below uses the 9-pin D-sub connector (DE-9). Peripherals might have a different pin-out even if they use a DE-9 connector as well.

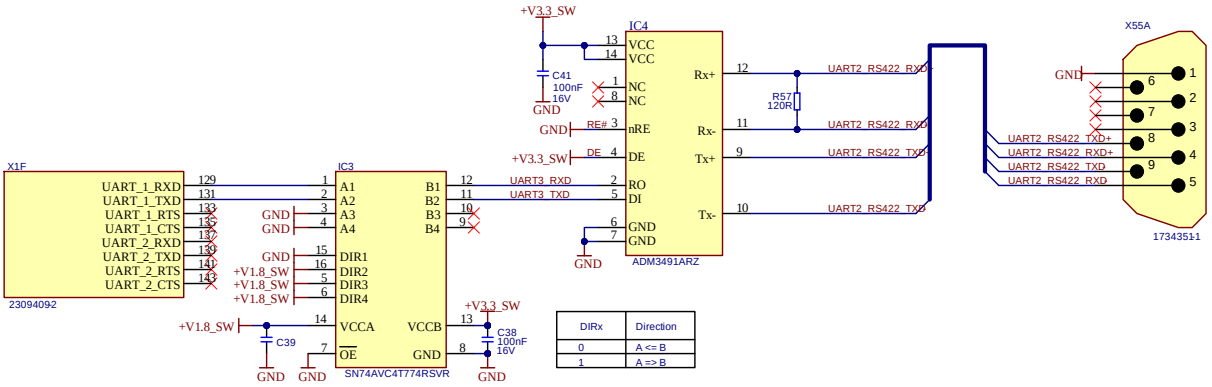


Figure 40: RS422 Reference Schematic

2.10.2.3 RS485 Reference Schematics

The RS485 interface is a half-duplex serial interface with differential pair signals. Instead of two differential pair wires (RS422), only one pair is used for transmitting and receiving the data. The bus allows Multi-Point connections. An additional control signal is required since the transceiver needs to be set either in the transmitting or receiving mode. It is recommended to use the RTS signal of the corresponding UART interface. The RTS signal is only available on the UART_1 and UART_2 as a Verdin standard interface. The schematic shown below inverts the RTS signal for the data enable input of the transceiver. Some modules allow inverting the signal in the software. However, it is recommended to keep the inverter circuit in the RTS signal to maintain compatibility with different modules and drivers provided by Toradex. For some applications, the UART controller should not see the TX message on its RX pins (the echo of the sent message). In this case, the receive enable pin (RE#) can be driven with the RTS signal. This turns off the RX output buffer while sending a message.

Like the RS422, the RS485 specification does not describe a standard connector. The reference schematic shown below uses a DE-9 connector that may have a different pin-out than some peripheral devices.

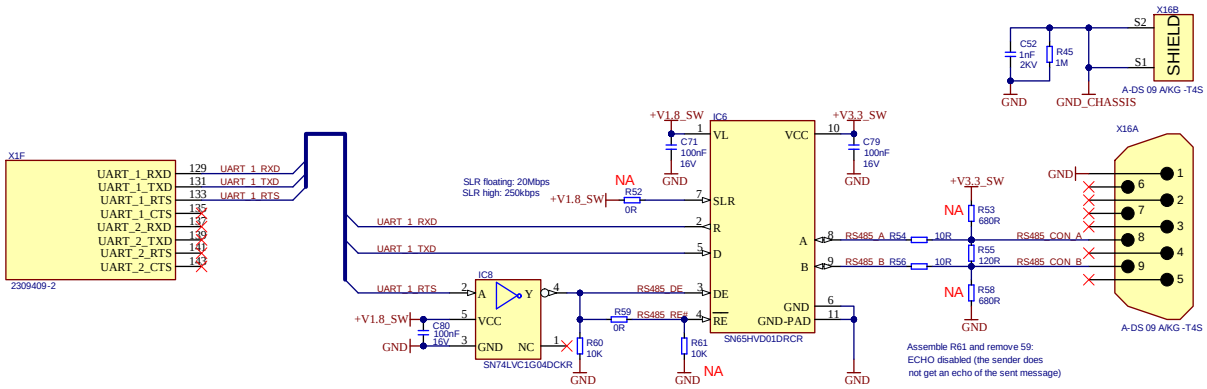


Figure 41: RS485 Reference Schematic

2.10.3 Unused UART Signal Termination

Unused UART interface signals can be left unconnected. For debugging purposes, it is recommended to have at least the UART_3_RXD and UART_3_TXD signals accessible.

2.11 SPI

The serial peripheral interface (SPI) bus is a synchronous, full-duplex interface. The Verdin module form factor features one SPI interface in the "Always Compatible" class. The interface has one chip select signal. Some modules may feature an additional chip select signal or additional SPI interfaces as a secondary function of other pins.

The clock polarity and phase of the SPI bus are not standardized. Some peripherals latch the data at the positive edge of the clock, while others latch it at the negative edge. The SPI modes describe these different behaviors. Make sure that the relevant Verdin module and the peripheral devices are set to the same SPI mode.

SPI Mode	Clock Polarity	Clock Phase	Description
0	0	0	The clock has a positive polarity, and the data is latched at the positive edge of the SCK
1	0	1	The clock has a positive polarity, and the data is latched at the negative edge of the SCK
2	1	0	The clock has a negative polarity, and the data is latched at the positive edge of the SCK
4	1	1	The clock has a negative polarity, and the data is latched at the negative edge of the SCK

Table 25: SPI Modes

2.11.1 SPI Signals

An SPI bus consists of one master and one or many slaves. In the Verdin standard, the module is the SPI master. Some modules may also allow themselves to be used as SPI slaves. Some modules may provide this function on different, non-standard pins.

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
200	SPI_1_MOSI	O	CMOS	1.8V	Master Output, Slave Input
198	SPI_1_MISO	I	CMOS	1.8V	Master Input, Slave Output
202	SPI_1_CS	O	CMOS	1.8V	Slave Select
196	SPI_1_CLK	O	CMOS	1.8V	Serial Clock

Table 26: SPI Signals

2.11.2 Unused SPI Signal Termination

Unused SPI signals can be left unconnected.

2.12 Quad Serial Peripheral Interface (Quad SPI)

The Quad Serial Peripheral Interface (Quad SPI) is mainly used for interfacing NAND and NOR flash memory. The Quad SPI offers four bidirectional data lines for half-duplex communication for much higher speed than regular SPI. Regular SPI uses individual single data lines for transferring and receiving data (full-duplex).

Even though QSPI is often used as a short form for Quad SPI, it should not be confused with the Queued Serial Peripheral Interface, which also uses the abbreviation QSPI and which is basically a regular SPI interface with an additional data queue. With this wrapper, the peripherals can appear as memory-mapped parallel devices.

2.12.1 Quad SPI Signals

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
54	QSPI_1_CS#	O	CMOS	1.8V	Chip Select 0
64	QSPI_1_CS2#	O	CMOS	1.8V	Chip Select 1, dual die flash requires both chip-select signals CS0 and CS1
52	QSPI_1_CLK	O	CMOS	1.8V	Serial Clock
56	QSPI_1_IO0	I/O	CMOS	1.8V	Serial I/O for command, address, and data
58	QSPI_1_IO1	I/O	CMOS	1.8V	Serial I/O for command, address, and data
60	QSPI_1_IO2	I/O	CMOS	1.8V	Serial I/O for command, address, and data
62	QSPI_1_IO3	I/O	CMOS	1.8V	Serial I/O for command, address, and data
66	QSPI_1_DQS	I	CMOS	1.8V	Data Strobe signal, required on some high- speed DDR devices

Table 27: Quad SPI signals

2.12.2 Unused Quad SPI Signal Termination

Unused Quad SPI signals can be left unconnected.

2.13 CAN

The controller area network (CAN) bus is a multi-master serial bus standard. It was first introduced for the automotive sector and soon became widely adopted in the industrial sector. Different versions of CAN specifications are available. Make sure that the corresponding Verdin module complies with the required version. Some Verdin modules support CAN FD for up to 5 times higher data rates and larger message sizes (compared to "regular" CAN).

2.13.1 CAN Signals

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
20	CAN_1_TX	O	CMOS	1.8V	CAN port 1 transmit pin
22	CAN_1_RX	I	CMOS	1.8V	CAN port 1 receive pin
24	CAN_2_TX	O	CMOS	1.8V	CAN port 2 transmit pin
26	CAN_2_RX	I	CMOS	1.8V	CAN port 2 receive pin

Table 28: CAN Signals

2.13.2 Reference Schematics

The CAN interface requires a transceiver on the carrier board. Often, the CAN interface needs to be galvanically isolated from the Verdin computer module. There are transceivers with integrated signal isolation available (for example, the TI ISO1042BDWR). An example of a CAN FD transceiver without integrated isolation is the Microchip MCP2558FDT. There are different types of connectors used for the CAN interface. The reference schematic below uses a single-row pin header as a connector. Since this is not an official standard, some devices might have a different connector or pin-out.

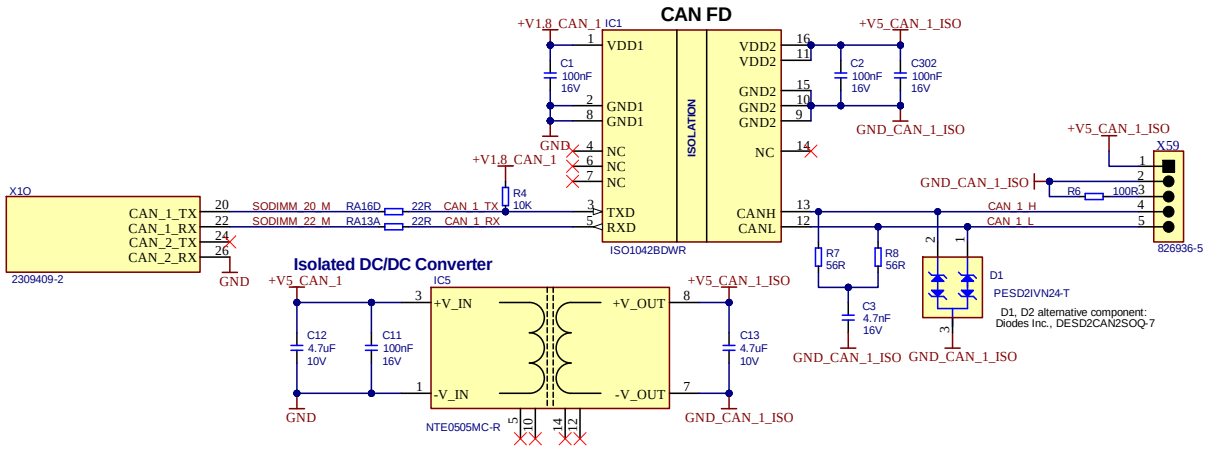


Figure 42: CAN Reference Schematic

2.13.3 Unused CAN Interface Signal Termination

According to the Verdin standard, the CAN interface signals do not need to be GPIO capable. It depends on the module whether the CAN interface signal pins can be used for other purposes if the CAN interface is not in use. Some Verdin modules provide the CAN interface by using a dedicated controller. It is recommended to tie the CAN RX signals to ground or 1.8V if the interface is not used. This can help in reducing the power consumption of modules with a stand-alone CAN controller.

2.14 PWM

The Verdin module form factor defines three pulse width modulator (PWM) outputs. PWM_1 is a general-purpose PWM and is in the "Always Compatible" class. The PWM_2 is also intended to be used for general purpose applications, but it is in the "Reserved" class. The third signal, the PWM_3_DSI, is dedicated to the display backlight control of the MIPI DSI port. This signal is also labeled as "Reserved". Some Verdin modules feature more than three PWM outputs. These signals are available as alternate functions of other interfaces or in the "Module-specific" section of the module edge connector. The additional PWM outputs are not guaranteed to be pin-compatible with other Verdin modules.

The maximum output frequency and the possible duty cycle steps vary between the different Verdin modules. Please carefully read the datasheets of Verdin modules for more information on the performance of the PWM interface pins.

2.14.1 PWM Signals

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
15	PWM_1	O	CMOS	1.8V	General-purpose PWM "Always Compatible"
16	PWM_2	O	CMOS	1.8V	General-purpose PWM "Reserved"
19	PWM_3_DSI	O	CMOS	1.8V	Dedicated PWM for display backlight "Reserved"

Table 29: PWM Signals

2.14.2 Reference Schematics

The PWM output signals can be used to drive motors, LEDs, robotic servos, fans, and others. It is possible to get an analog signal with a simple low pass filter.

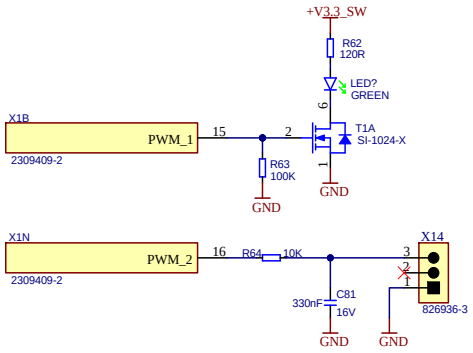


Figure 43: PWM Example Schematic

2.14.3 Unused PWM Signal Termination

Unused PWM signals can be left unconnected.

2.15 Inter-IC Sound (I²S)

The Verdin module features up to two digital audio interfaces in the "Reserved" category. The interfaces are intended to support the Inter-IC Sound (I²S) standard for connecting to an audio codec on the carrier board or other compatible audio equipment (e.g., HDMI audio, Bluetooth adapter, DSP, and others.). Depending on the Verdin module, the digital audio interfaces may support additional standards, such as AC'97 or HAD. However, the I²S is the preferred standard for additional compatibility between different Verdin modules.

2.15.1 Digital Audio Signals

The Verdin I²S consists of data input, data output, synchronization, and the bit clock signal. Each of the two data signals holds two stereo streams. The synchronization signal is used for identifying whether the data belongs to the right or left channel and marks the start of each word. In the I²S standard, the sync and clock signal can be generated either by the SoC or the codec. Check in the module datasheet and in the codec datasheet which direction is supported. Often it is preferred to have the codec send the bit clock and the sync signal to the SoC.

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
36	I2S_1_D_IN	I	CMOS	1.8V	Serial input data stream to the Verdin Module
34	I2S_1_D_OUT	O	CMOS	1.8V	Serial output data stream from the Verdin Module
32	I2S_1_SYNC	I/O	CMOS	1.8V	Synchronization/ field select/ left-right channel select
30	I2S_1_BCLK	I/O	CMOS	1.8V	Serial bit clock
38	I2S_1_MCLK	O	CMOS	1.8V	External Peripheral Clock
48	I2S_2_D_IN	I	CMOS	1.8V	Serial input data stream to the Verdin Module
46	I2S_2_D_OUT	O	CMOS	1.8V	Serial output data stream from the Verdin Module
44	I2S_2_SYNC	I/O	CMOS	1.8V	Synchronization/ field select/ left-right channel select
42	I2S_2_BCLK	I/O	CMOS	1.8V	Serial bit clock

Table 30: Digital Audio Signals

2.15.2 Reference Schematics

It is recommended to place 22R series resistors on the signal lines. Place these resistors close to the signal outputs

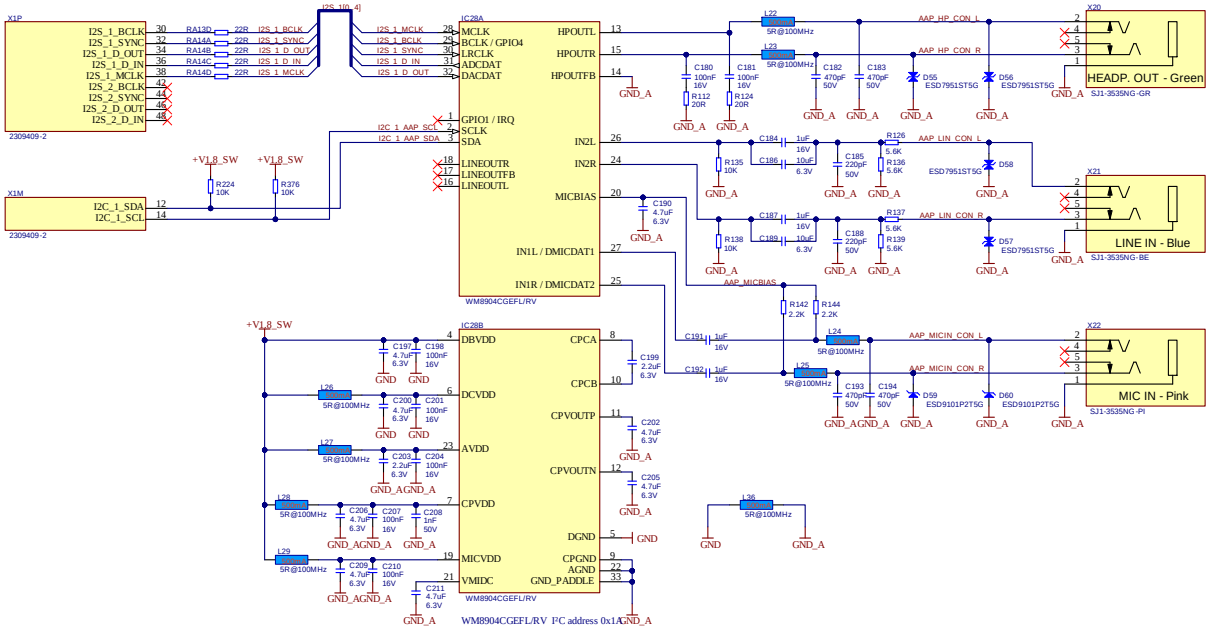


Figure 44: I²S Codec Reference Schematic

2.15.3 Unused Digital Audio Interface Signal Termination

Unused digital audio interface signals can be left unconnected.

2.16 Analog Inputs

The Verdin modules feature up to four analog input channels. The supported sampling rates and resolutions depend on the module. According to the Verdin specifications, the input voltage span is from 0V to 1.8V. Some modules support a wider input voltage range. However, it is recommended for compatibility reasons to limit the input to positive voltages up to 1.8V.

The analog input channels are not designed to be used for high-precision measurement tasks. The interface is intended to be used for battery voltage monitoring (additional circuit required), ambient light sensors, simple analog joystick input devices, and others.

2.16.1 Analog Input Signals

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
2	ADC_1	I	Analog	1.8V	ADC input (recommended 0V to 1.8V max)
4	ADC_2	I	Analog	1.8V	ADC input (recommended 0V to 1.8V max)
6	ADC_3	I	Analog	1.8V	ADC input (recommended 0V to 1.8V max)
8	ADC_4	I	Analog	1.8V	ADC input (recommended 0V to 1.8V max)

Table 31: Analog Input Signals

2.16.2 Unused Analog Inputs Signal Termination

The unused analog input signals can be left unconnected or tied to the ground. It is recommended to disable the corresponding inputs in the driver or disable the whole ADC block if unused.

2.17 General Purpose Clock Outputs

The Verdin module standard reserves two module edge connector pins as general-purpose clock outputs. One output is intended to be used for the digital audio interface, while the other one is reserved for the camera interface. The clock outputs could also be used for other purposes if not required by the dedicated function. Please note that on some modules, the possible output frequencies are limited. There might also be limitations due to the other clock sources used in the module, or the interface they are dedicated to needs to be enabled to enable the clock output. Read the relevant datasheets carefully.

2.17.1 Clock Output Signals

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
38	I2S_1_MCLK	O	CMOS	1.8V	Clock output for the digital audio interface
91	CSI_1_MCLK	O	CMOS	1.8V	Clock output for the MIPI CSI-2 camera interface

Table 32: Clock Output Signals

2.17.2 Schematic and Layout Considerations

The clock output signals can have a pretty high frequency, especially for single-ended clock signals. This could lead to significant problems due to electromagnetic interferences (EMI). The clock signals should be kept as short as possible. High slew rates of the signal can increase the EMI problems. Therefore, it is desirable to reduce the slew rate as much as the signal quality allows it. Therefore, series resistors should be placed close to the clock output of the module. Start with a value of 22Ω. Try to increase this value until the corresponding interface fails due to the signal quality of the clock signal. Decrease the serial resistor again to have a reasonable margin.

Instead of using the clock output signals, some of the interfaces also allow using a different asynchronous clock reference. For example, suppose the audio codec or the camera needs to be located far away from the Verdin computer module. In that case, it might be a better solution to use an oscillator instead of the reference clock output of the module. This oscillator can be placed close to the audio codec or camera.

2.17.3 Unused Clock Output Signal Termination

Unused clock output signals can be left unconnected. The output should be disabled for reducing power consumption and EMI problems.

2.18 GPIO

The Verdin form factor features four dedicated general-purpose input-output pins (GPIO) plus additional two GPIOs reserved for the MIPI DSI interface. Additional four GPIOs are reserved for the MIPI CSI interface. Besides these 10x GPIOs, several pins can be used as GPIO if their primary function is not used. Table 2 and Table 3 show an overview of the interfaces.
For carrier boards intended to provide the highest compatibility with all different Verdin modules, it is recommended to use the 10x GPIO signals first. If additional GPIO signals are required, unused signal pins of the interfaces stated as “GPIO Capable” could be used.

2.18.1 GPIO Signals

The following table contains the 10x GPIO pins available on Verdin modules. Consult the relevant datasheet of the modules for information on the other module edge connector pins that can be used as GPIO interface.

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
206	GPIO_1	I/O	CMOS	1.8V	General-purpose GPIO
208	GPIO_2	I/O	CMOS	1.8V	General-purpose GPIO
210	GPIO_3	I/O	CMOS	1.8V	General-purpose GPIO
212	GPIO_4	I/O	CMOS	1.8V	General-purpose GPIO
216	GPIO_5_CSI	I/O	CMOS	1.8V	Reserved general-purpose IO for MIPI CSI interface
218	GPIO_6_CSI	I/O	CMOS	1.8V	Reserved general-purpose IO for MIPI CSI interface
220	GPIO_7_CSI	I/O	CMOS	1.8V	Reserved general-purpose IO for MIPI CSI interface
222	GPIO_8_CSI	I/O	CMOS	1.8V	Reserved general-purpose IO for MIPI CSI interface
17	GPIO_9_DSI	I/O	CMOS	1.8V	Reserved general-purpose IO for MIPI DSI interface
21	GPIO_10_DSI	I/O	CMOS	1.8V	Reserved general-purpose IO for MIPI DSI interface

Table 33: Dedicated GPIO Signals

2.18.2 Unused GPIO Termination

The GPIO signals do not need to be terminated if they are not in use.

2.19 JTAG interface

The Verdin module specification features JTAG test interface signals on the module edge connector. The JTAG interface can be helpful for advanced debugging of the main and real-time (if available) operating system.

2.19.1 JTAG Signals

The JTAG signals usually have an IO voltage level of 1.8V. However, there could be modules with a different JTAG voltage level. Therefore, the JTAG interface has a voltage reference output that represents the IO voltage of the module. This rail should be used for the JTAG adapter as a reference voltage.

The JTAG_1_TRST# signal is an optional signal that allows the test adapter to reset the devices on the JTAG interface. It depends on the module, whether the TRST signal is available and whether it also resets further peripherals on the module.

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
1	JTAG_1_TDI	I	CMOS	JTAG_1_VREF	Test Data In
5	JTAG_1_TDO	O	CMOS	JTAG_1_VREF	Test Data Out
9	JTAG_1_TCK	I	CMOS	JTAG_1_VREF	Test Clock
13	JTAG_1_TMS	I	CMOS	JTAG_1_VREF	Test Mode Select
3	JTAG_1_TRST#	I	CMOS	JTAG_1_VREF	Test Reset (optional)
7	JTAG_1_VREF	O	CMOS	1.8V*	Reference output voltage for JTAG adapter

Table 34: JTAG Signals

2.19.2 Reference Schematics

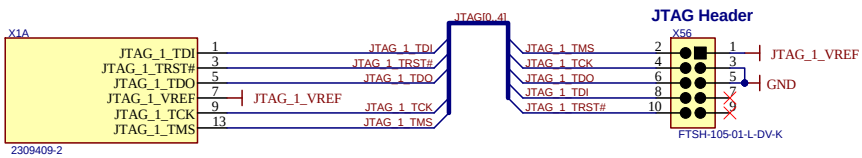


Figure 45: JTAG Example Schematic

2.19.3 Unused JTAG Signal Termination

Unused JTAG signals can be left unconnected.

2.20 Module Recovery

Recovery mode is the only officially supported method for flashing the bootloader onto Verdin modules. It is highly recommended to evaluate the need for the in-field recovery and software update functionalities in the context of the end-product at the time of designing the system.

If in-field recovery needs to be supported, it is recommended to define and implement a hardware-based solution for entering into recovery mode. In case the bootloader fails, the hardware-based solution is the only method available for entering into recovery mode.

To enter recovery mode, the dedicated recovery pin (CTRL_RECOVERY_MICO#, SODIMM pin 246) needs to be pulled down with ≤1kΩ during the initial power on (cold boot) of the module. The software could be downloaded to the module via the USB_1 interface in USB client mode (USB OTG) in recovery mode.

If the in-field recovery and software update use cases need to be supported by the end-device, it is highly recommended to make the USB_1 (USB OTG or USB client) interface available externally on the end-product.

2.20.1 Recovery Signals

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
246	CTRL_RECOVERY_MICO#	I	OD	1.8V	Recovery mode strapping input. Pull-up resistor on the module. Additional pull-up on carrier board is not allowed.
165	USB_1_D_P	I/O	USB		USB interface used for recovery mode
163	USB_1_D_N	I/O	USB		
161	USB_1_ID	I	CMOS	1.8V	If only recovery is used (only client mode), this pin can be permanently pulled up to 1.8V
159	USB_1_VBUS	I	CMOS	5V tolerant	Bus voltage detection in client mode

Table 35: Recovery Signals

2.20.2 Reference Schematics

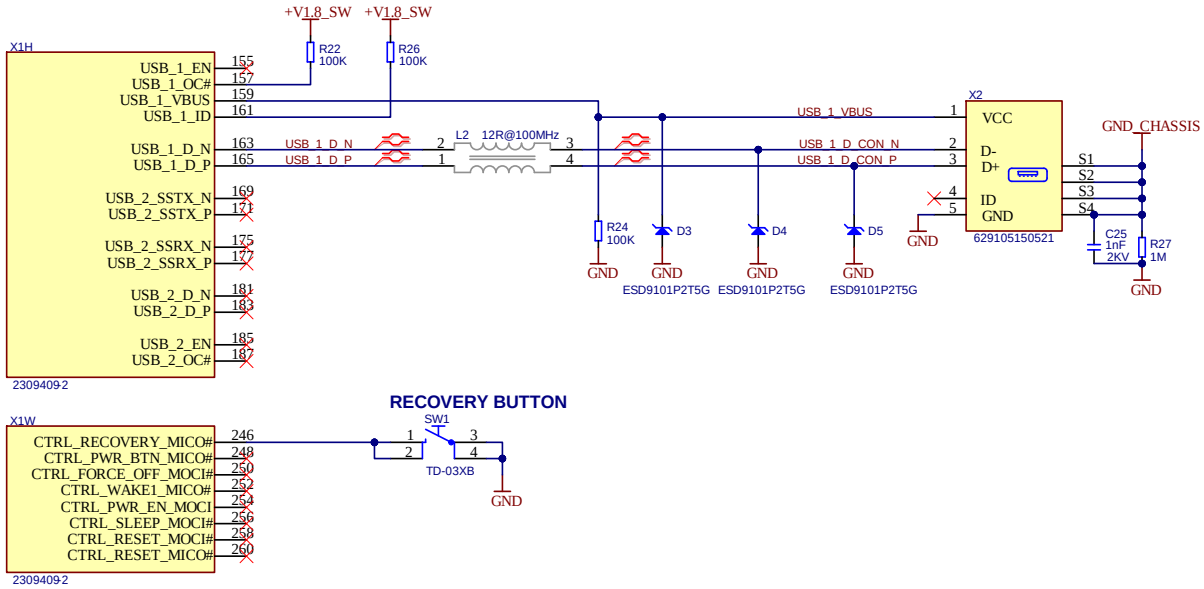


Figure 46: Recovery Reference Schematic

2.20.3 Unused Recovery Signal Termination

The CTRL_RECOVERY_MICO# can be left unconnected if the recovery feature is not needed. There is a pull-up resistor on the module. No external pull-up resistor is allowed on the carrier board.

3 Power Management

3.1 Power Supply Design

All Verdin modules can be powered with a single main power supply powering VCC, and if required, a low current backup power supply for purposes such as Real Time Clock (RTC) support. The main power supply input can accept a wide voltage range between 3.135V and 5.5V (absolute). This allows supplying the module from a 3.3V +/-5% or a 5V +/-10% power supply, or even a single Lithium battery cell. For simple applications, the module can run directly from a USB power port.

The Verdin form factor is specified for a maximum sustained power consumption of up to 8.25W and a maximum peak power consumption of up to 12.5W for the SoMs.

The peak/maximum power consumption of individual SoMs depends on the use case, the silicon revision of the SoC, the versions of software components being used and the ambient temperature, among other factors.

For this reason, as a generic rule of thumb, we recommend scaling the carrier board power supplies for being able to reliably deliver the maximum peak power consumption specified for Verdin modules in order to ensure compatibility with the broadest range of existing and future Verdin modules.

Do not forget to take the additional power consumption of the carrier board peripheral devices on the module power rail (3.3V or 5V) into the power budget.

Most of the GPIO-capable I/O pins operate at a 1.8V logic level.

Verdin modules provide a 1.8V reference output with a current of up to 250mA. Carrier boards may use this power source directly as the only 1.8V supply for their peripherals. This saves complexity and cost on custom carrier boards.

3.1.1 Power Supply Signals

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
251, 253, 255, 257, 259	VCC	I	PWR	3.135V to 5.5V	Main power supply input for the module
10, 11, 18, 27, 28, 33, 39, 40, 45, 50, 51, 65, 68, 71, 77, 83, 86, 89, 97, 98, 103, 109, 110, 115, 121, 122, 127, 134, 145, 146, 158, 167, 170, 173, 179, 182, 194, 195, 204, 209, 223, 224, 229, 230, 236, 242, 243	GND	I	PWR		Common signal and power ground
249	VCC_BACKUP	I	PWR	3.0V	RTC supply, can be left unconnected if internal RTC is not used
214	PWR_1V8_MOCI	O	PWR	1.8V	250mA output for carrier board peripherals

Table 36: Power supply signals

3.1.2 Power Management Signals

Besides the power supply signals, the Verdin form factor supports several power-management signals. Most of these signals are optional for the carrier board. However, they allow different power management schemes for the carrier board from a straightforward approach to an advanced one with extra power-saving features and systems with single-cell Lithium batteries.

Verdin Pin	Verdin Signal Name	I/O	Type	Power Rail	Description
258	CTRL_RESET_MOCI#	O	OD	3.3V Tolerant	Reset output for carrier board peripherals. This reset is derived from the SoC reset on the module. Note that during and after a sleep state, the CTRL_RESET_MOCI# does not get asserted. The output is an open-drain type without a pull-up resistor on the module. The signal is 3.3V tolerant. The carrier board can pull the signal up to 1.8V or 3.3V. The signal can be left floating on the carrier board.
254	CTRL_PWR_EN_MOCI	O	CMOS	1.8V	Enable signal for the power rails of the carrier board peripherals. This output remains high during sleep modes.
256	CTRL_SLEEP_MOCI#	O	CMOS	1.8V	Enable signal for the power rails on the carrier board peripherals, which need to be turned off during sleep mode. It is only high during the running mode. The signal is standard GPIO with an on-module 10k pull-down resistors. The signal is defined during the power-up sequence. The signal can be left floating on the carrier board.
260	CTRL_RESET_MICO#	I	OD	1.8V	Open-drain input, which resets the module if shorted to ground on carrier board. One 100k on-module pull-up to the 1.8V RTC rail is present on the module. This means that the signal can be left floating on the carrier board.
248	CTRL_PWR_BTN_MICO#	I	OD	1.8V	Pulling down for a longer period of time is shutting down the module. Short pulling down is turning on module from off state. Open-drain input with 100k pull-up resistor to the 1.8V RTC rail is on the module. The signal can be left floating on carrier boards.
246	CTRL_RECOVERY_MICO#	I	OD	1.8V	Shorting to the ground during power-up is setting the module into recovery mode. There is a 10k pull-up on the module. The signal can be left floating on carrier boards.
252	CTRL_WAKE1_MICO#	I	CMOS	1.8V	Wake capable pin, which allows resuming from sleep mode. There are no pull resistors on the carrier board. The signal can be left floating on carrier boards if the wake feature is disabled in the software.
250	CTRL_FORCE_OFF_MOCI#	O	OD	5V Tolerant	Output for forcing the turning-off of the carrier board power rails. This signal needs to be ignored for the first 400ms during the power-up sequence. The output is an open-drain type without a pull-up resistor on the module. The signal is 5V tolerant. The carrier board can pull the signal up to 1.8V, 3.3V, or 5V. The signal can be left floating on carrier boards.

Table 37: Power management signals

To make the direction of the power management signals clear, the ending MICO or MOCI are appended to the signal names. MICO is the abbreviation for “Module Input, Carrier board Output”, while MOCI stands for “Module Output, Carrier board Input”.

3.2 Module Power States

Verdin modules have different power states. The following table describes what the different states mean. Depending on the carrier board power supply use case, some of the states may not be available.

Name	Description
No VCC	The main VCC power rail is not applied to the module. The VCC_BACKUP may be available for keeping the RTC running. The CTRL_PWR_EN_MOCI and CTRL_SLEEP_MOCI# are low to ensure no peripheral rails on the carrier board are enabled. CTRL_RESET_MOCI# and CTRL_FORCE_OFF_MOCI# are undefined. They can be high-z or driven low in this state.
Running	The module is running. Some unused module or carrier board peripherals may be switched off.
Reset	The module and the peripheral devices are in a reset state. The preferred reset mode is a “cold reset”. This means that the PMIC shuts down all the rails on the module and drives the CTRL_PWR_EN_MOCI and CTRL_SLEEP_MOCI# low to turn off also the carrier board rails. Some modules may implement a “warm reset” instead. The rails on the module, including CTRL_PWR_EN_MOCI, are kept up while only the reset signals are asserted in this reset state. The Verdin module datasheet contains information on which type of reset is implemented by the module. If the CTRL_RESET_MICO# is low, the module is kept in reset mode. This allows the carrier board to prolong the reset cycle.
Sleep	The CPU is in a suspended state. The peripherals on the module are either turned off or are put into a sleep state. The CTRL_SLEEP_MOCI# is driven low, allowing to turn off the power rails of peripherals that do not need to be powered in the sleep mode. The module can be woken up by an RTC event, a wake-capable on-module peripheral, the CTRL_PWR_BTN_MICO# (power button), the CTRL_WAKE1_MICO#, or a wake-enabled GPIO (for wake capabilities of GPIO pins, please refer to module datasheets).
Module OFF	The PMIC on the module has shut down all the power rails, but the VCC is still applied to the module. CTRL_PWR_EN_MOCI, CTRL_SLEEP_MOCI#, and CTRL_RESET_MOCI# are all set low to turn off peripheral power rails on the carrier board. The CTRL_FORCE_OFF_MOCI# output is also low. It depends on the carrier board power supply scheme whether this causes the module to stay in the “Module OFF” state or the VCC is removed, which means the module goes into “No VCC” mode (see section 3.4). The power consumption of the module is very low in this state. The VCC rail is only used for keeping the power management circuits and the RTC on. The actual consumption can be found in the datasheets of Verdin modules.

Table 38: Available Verdin power states

The module automatically transitions to the running mode when the VCC main power rail is applied to the module. In other words, all Verdin modules are ramping up the power rails and boot the system when the VCC is applied.

The CTRL_PWR_BTN_MICO# allows implementing a power button behavior like the ones used on regular personal computers and smartphones. Short pressing the power button is powering up the system from the “Module OFF” state or wakes the system from the sleep state. If the module is running, short pressing the power button generates a software interrupt. Depending on the operating system settings, this starts a software shut down or opens a menu that lets the customer decide what to do. Pressing the power button longer than 5 seconds shuts the system down immediately (without any software interaction).

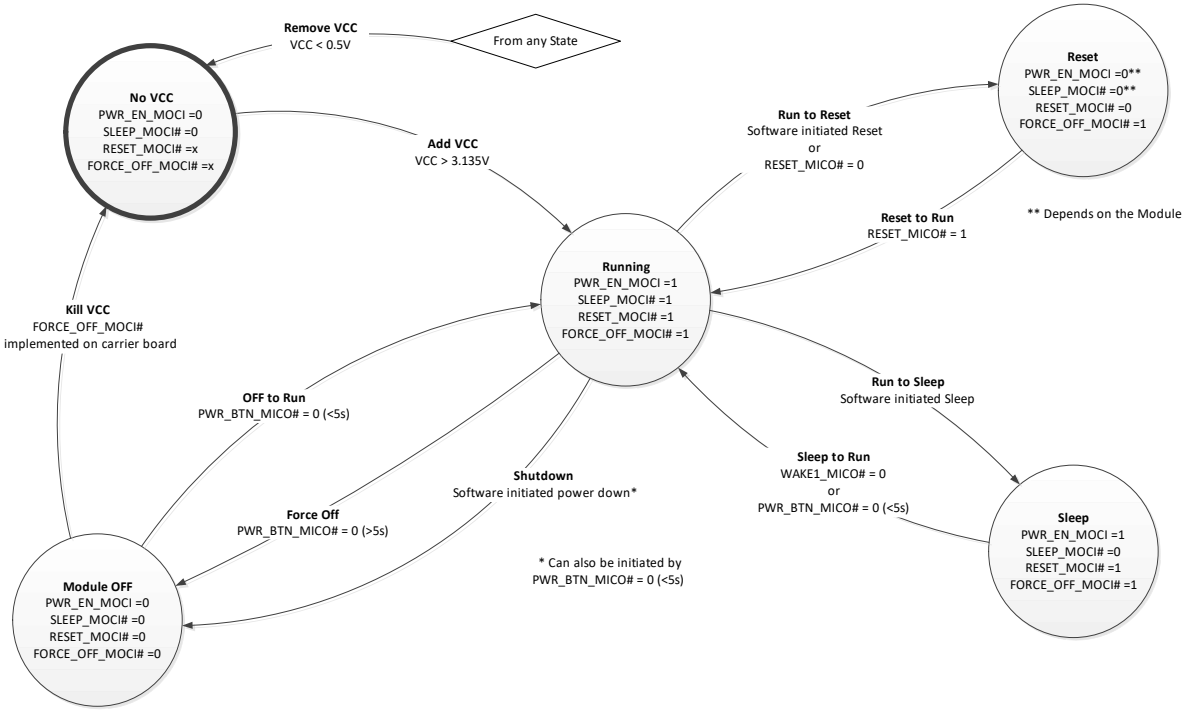


Figure 47: Module Power States and Transitions

3.3 General Power Sequences

3.3.1 "No VCC" to "Running" (startup)

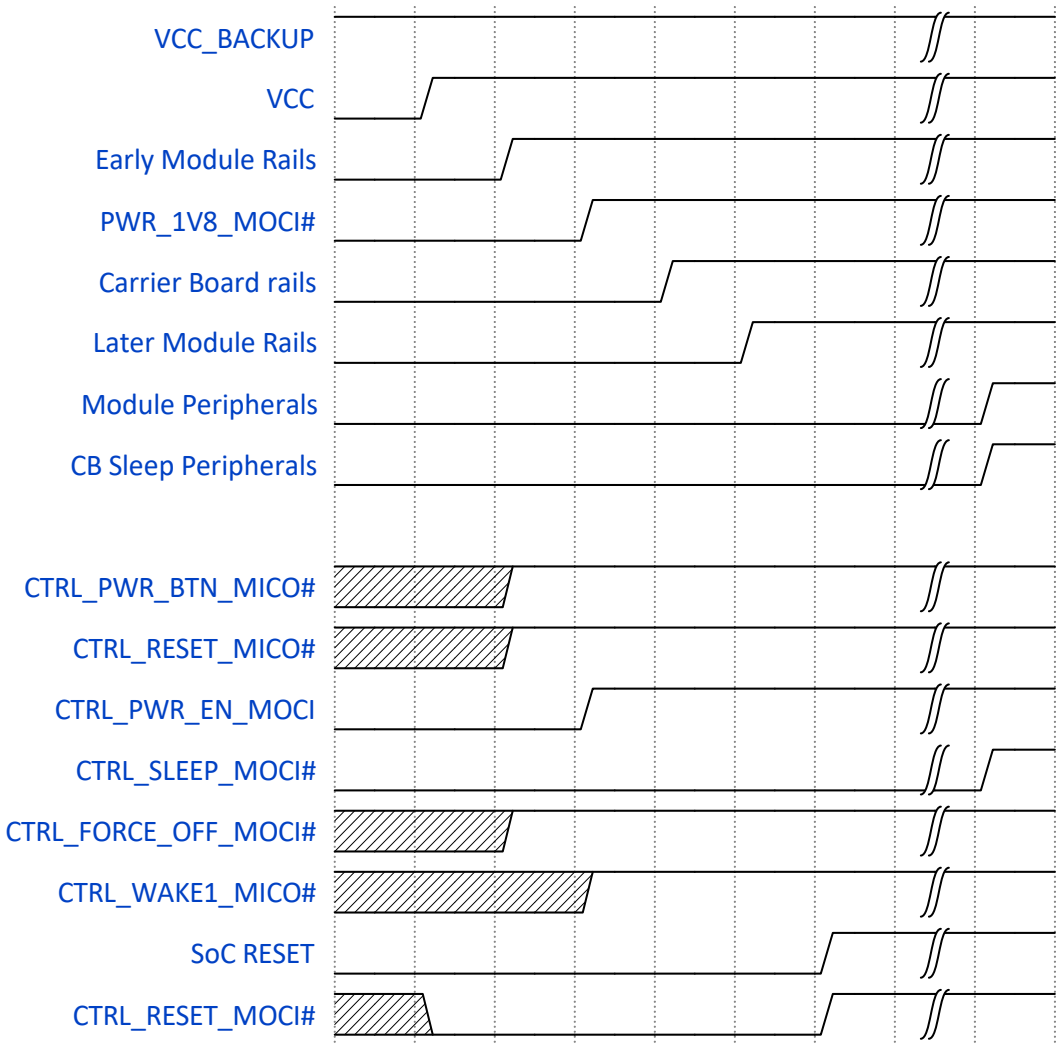


Figure 48: "No VCC" to "Running" (startup) Power Sequence

The Verdin module starts the power-up sequence when the VCC main input voltage is applied. There is no need to press the power button signal (CTRL_PWR_BTN_MICO#) for starting the module. The module ramps up early rails on the module. At this point, the pull-up resistors for the CTRL_PWR_BTN_MICO# and CTRL_RESET_MICO# get enabled. The CTRL_FORCE_OFF_MOCI# signal goes high. Before enabling these early rails on the module, the signal can be undefined. Therefore, the carrier board needs to blank (ignore) the CTRL_FORCE_OFF_MOCI# for the first 400ms after VCC has been applied.

After the early module rails are ramped up, the Verdin module outputs the PWR_1V8_MOCI# output rail and releases the CTRL_PWR_EN_MOCI. The CTRL_PWR_EN_MOCI is used for ramping up the carrier board rails. The module is enabling all the rest of the rails that are required for the module to be able to boot up.

After all rails are ramped up and settled, the SoC reset is released together with the CTRL_RESET_MOCI# for the carrier board. The module determines the length of the delay between enabling CTRL_PWR_EN_MOCI and releasing the carrier board reset. The carrier board must be ramping up the voltage rails within 10ms after the CTRL_PWR_EN_MOCI is released.

The module then starts booting the operating system. The CTRL_SLEEP_MOCI# signal is released while booting the operating system. This signal is used for enabling the power rails of peripherals on the carrier board that are disabled during a sleep state. Also, some on-module peripherals are enabled during the boot. This means that the CTRL_SLEEP_MOCI# signal and these on-module peripherals are under complete software control (whether they are enabled during the boot process).

3.3.2 "Running" to "Reset" (reset)

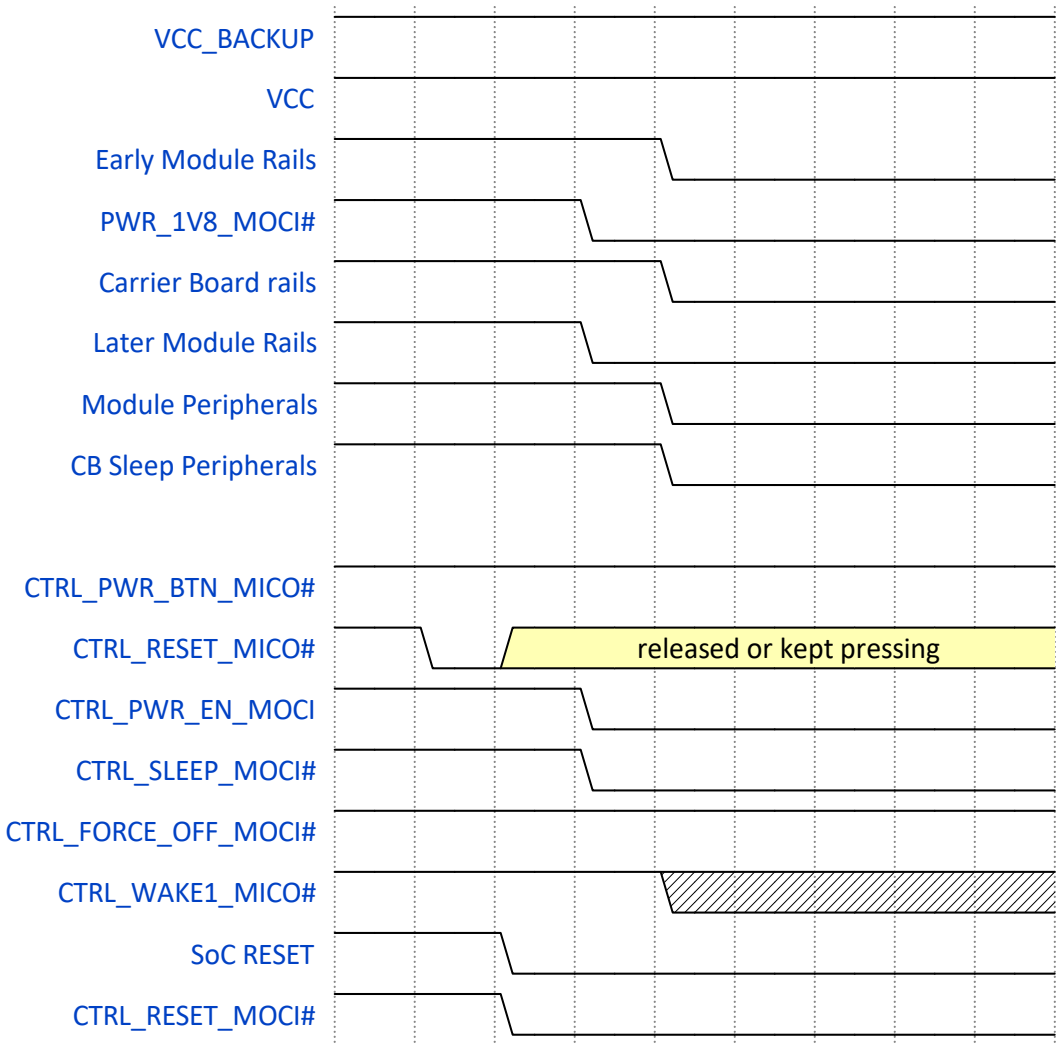


Figure 49: "Running" to "Reset" (reset) Power Sequence

The reset cycle can be initiated by a falling edge on the CTRL_RESET_MICO# (some modules add some debouncing time) or by software. In the preferred reset mode "cold reset", first the SoC reset and the CTRL_RESET_MOCI# are going low. Then all the rails on the module are removed (except for a few PMIC control rails). Basically, the module shuts down the rails in a controlled sequence. This also includes the CTRL_PWR_EN_MOCI and the CTRL_SLEEP_MOCI# to turn off the carrier board's power rails.

After all the rails are removed, the module remains in this state for a minimum reset time. The reset time can be extended by keeping the CTRL_RESET_MICO# low.

3.3.3 “Reset” to “Running” (startup after reset)

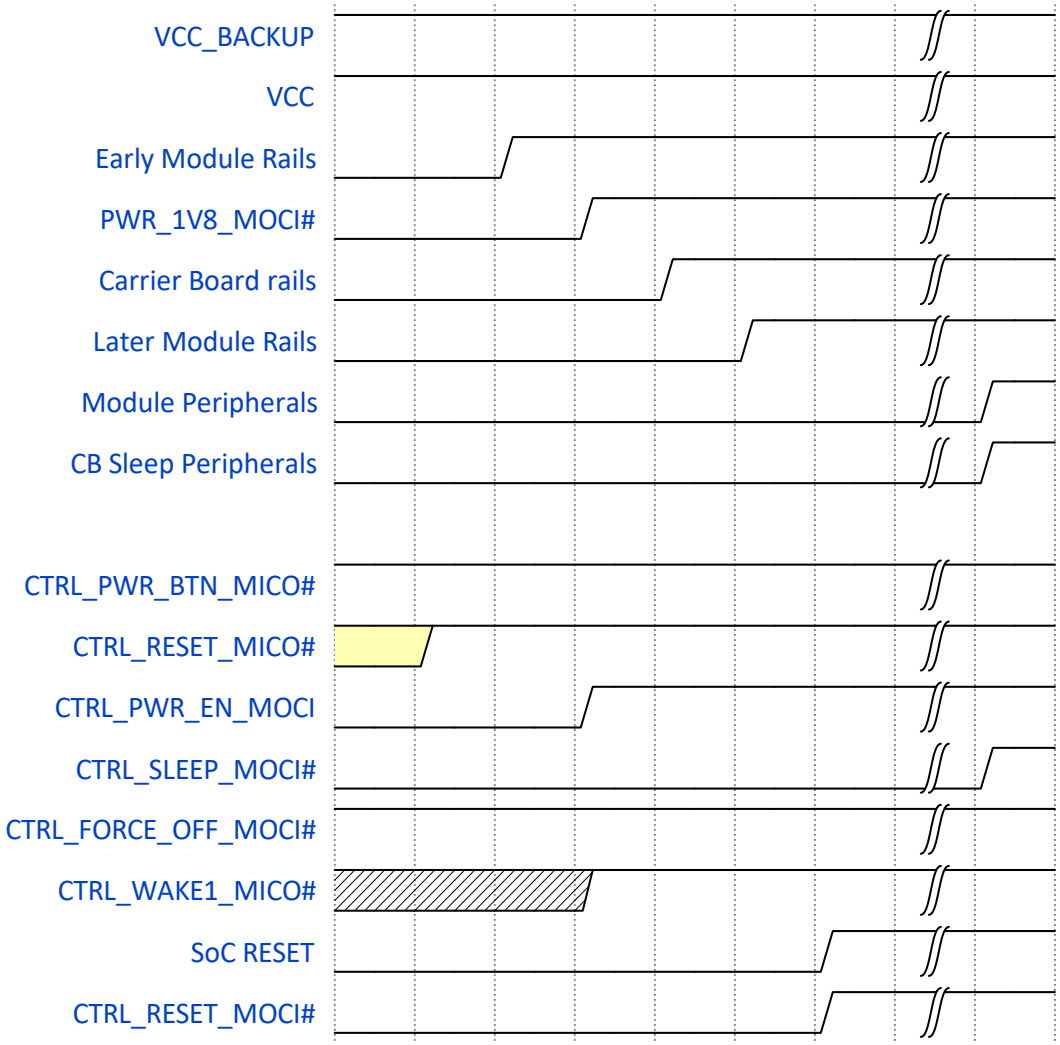


Figure 50: “Reset” to “Running” (startup after reset) Power Sequence

The transition back from the reset state starts when the CTRL_RESET_MICO# is released and the minimum reset time has elapsed. The actual reset time depends on the module. The rails are turned back on in the same order as during a regular module boot. See sequence description in the section “No VCC” to “Running” (startup).

3.3.4 "Running" to "Sleep" (sleep)

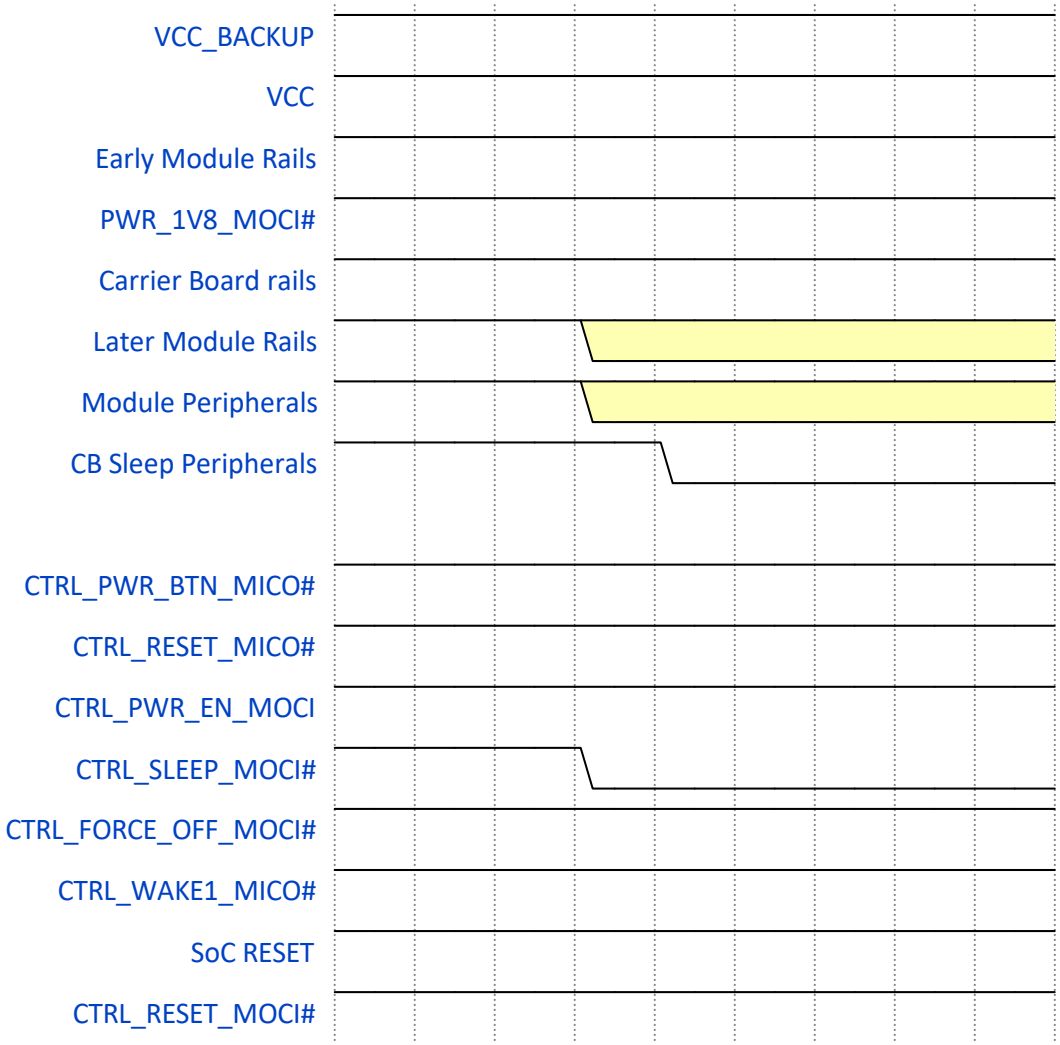


Figure 51: "Running" to "Sleep" (sleep) Power Sequence

In the sleep state, the CPU is suspended, and the RAM is put into self-refresh mode. Only a few peripherals are still running to keep the energy consumption low. The transition to the sleep state is initiated by software. The operating system makes sure that all the peripherals are put into a state that allows going to a low power mode or shutting them off.

Some non-essential and peripheral voltage rails are turned off on the module. The module outputs a low level at the CTRL_SLEEP_MOCI# signal. The carrier board uses this signal for turning off any rails that are not required in the sleep mode. It depends on the carrier board design, which rails can be turned off in the sleep mode.

It is crucial to make sure back-feeding is avoided. This means if a peripheral rail on the carrier board is turned off, all interface pins to and from the module need to be set either to high-z or a low voltage. The same goes for the peripherals on the module. If an on-module peripheral is turned off in the sleep mode, try to ensure that the carrier board is not driving interface pins high during the sleep mode.

3.3.5 "Sleep" to "Running" (wake)

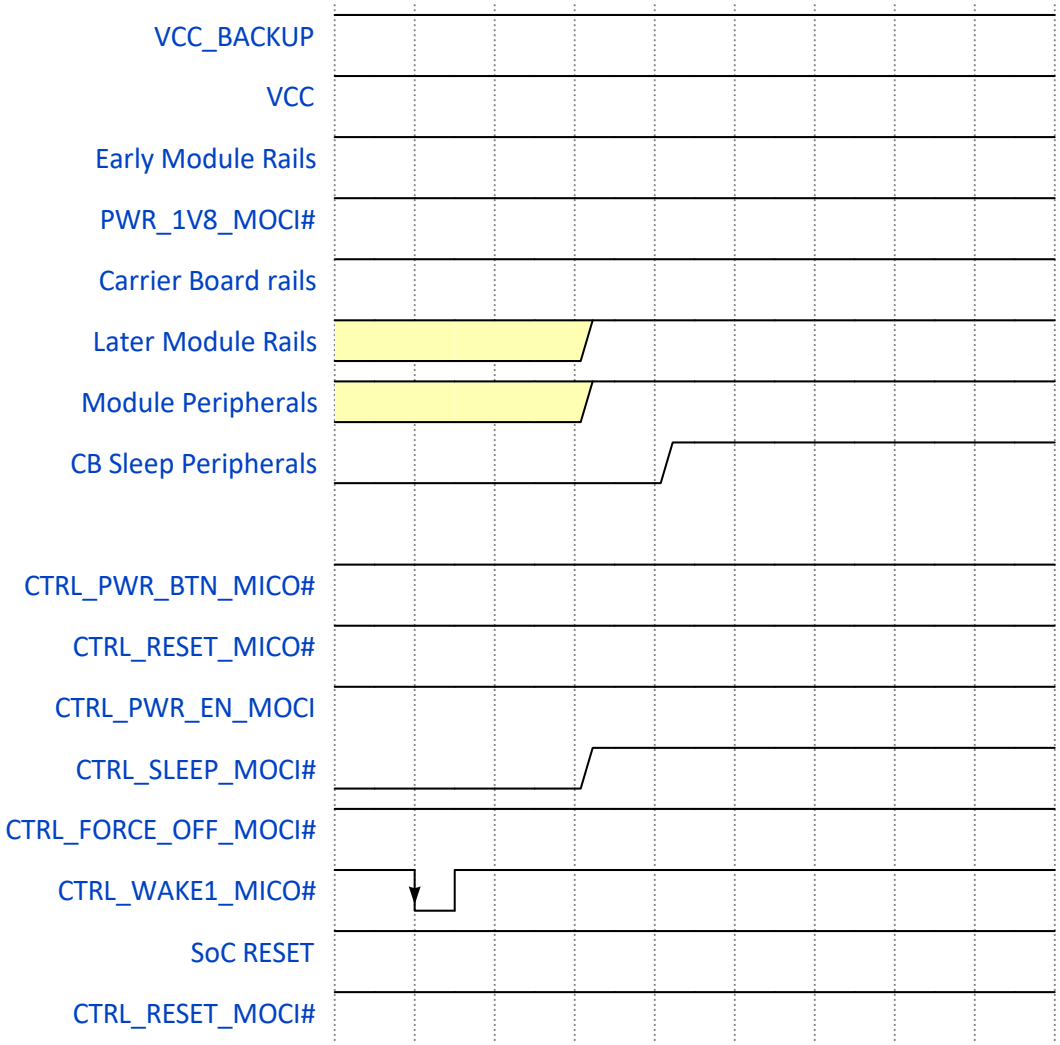


Figure 52: "Sleep" to "Running" (wake) Power Sequence

The module can be woken up from the sleep mode by an RTC event, a wake-capable on-module peripheral device, the CTRL_PWR_BTN_MICO# (power button), the CTRL_WAKE1_MICO#, or any wake-enabled GPIO (please refer to module datasheets). A falling edge on the CTRL_WAKE1_MICO# is the preferred wake source for keeping a design compatible between different Verdin modules.

The module re-enables the voltage rails and sets the CTRL_SLEEP_MOCI# signal high. This enables the peripheral rails on the carrier board. Since the CTRL_RESET_MOCI# is not cycled during the sequence from the sleep mode back to running, the peripherals that are turned off in sleep mode need their own power-on reset or a separate GPIO as a reset signal.

3.3.6 "Running" to "Module OFF" (shutdown)

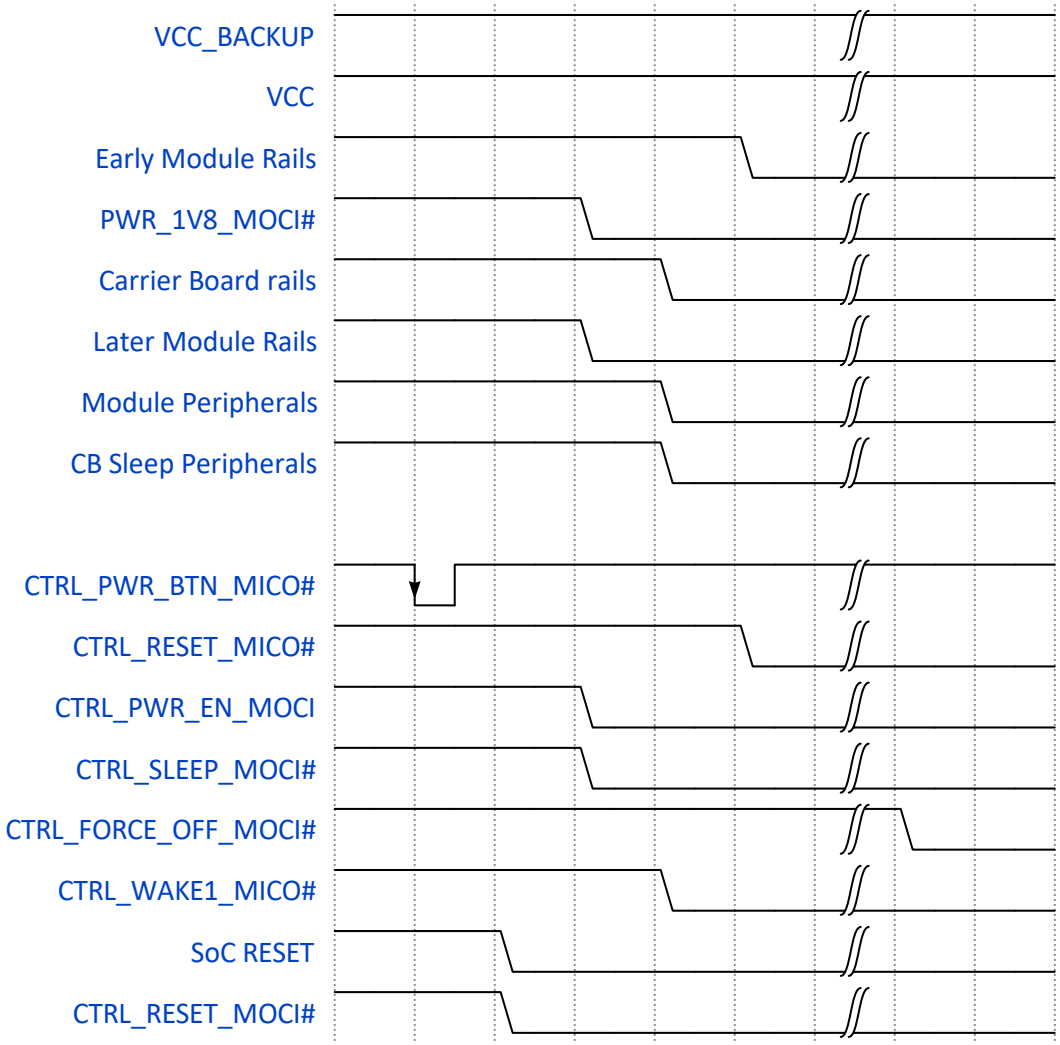


Figure 53: "Running" to "Module OFF" (shutdown) Power Sequence

The operating system initiates the regular shutdown sequence. A short pressing on the power button (CTRL_PWR_BTN_MICO#) generates an interrupt. However, the operating system is responsible for reacting to this interrupt and initiating a shutdown. Depending on system requirements, the OS may directly initiate the shutdown process, display power options, or not react to the power button interrupts.

The operating system makes sure that everything is put to a state in which a shutdown sequence can be performed without corrupting the system. For example, this could be saving temporary data, flushing buffers, closing files, or disconnecting services. After all processes are stopped, the operating system's last task is to request a shutdown from the PMIC.

The PMIC is first asserting the SoC reset as well as the CTRL_RESET_MOCI#. It then removes the different voltage rails in the required order. This also includes disabling the CTRL_PWR_EN_MOCI signal. The carrier board needs to turn off the power rails after the CTRL_PWR_EN_MOCI signal is disabled.

After all the rails have been removed, the main module input rail VCC remains. The CTRL_FORCE_OFF_MOCI# remains high for a certain amount of time. On some modules, it takes several seconds until the CTRL_FORCE_OFF_MOCI# goes low. If the carrier board ignores the CTRL_FORCE_OFF_MOCI# signals and does not implement the kill feature, VCC remains applied to the module, and the system remains in the "Module OFF" state.

3.3.7 “Running” to “No VCC” (force-off)

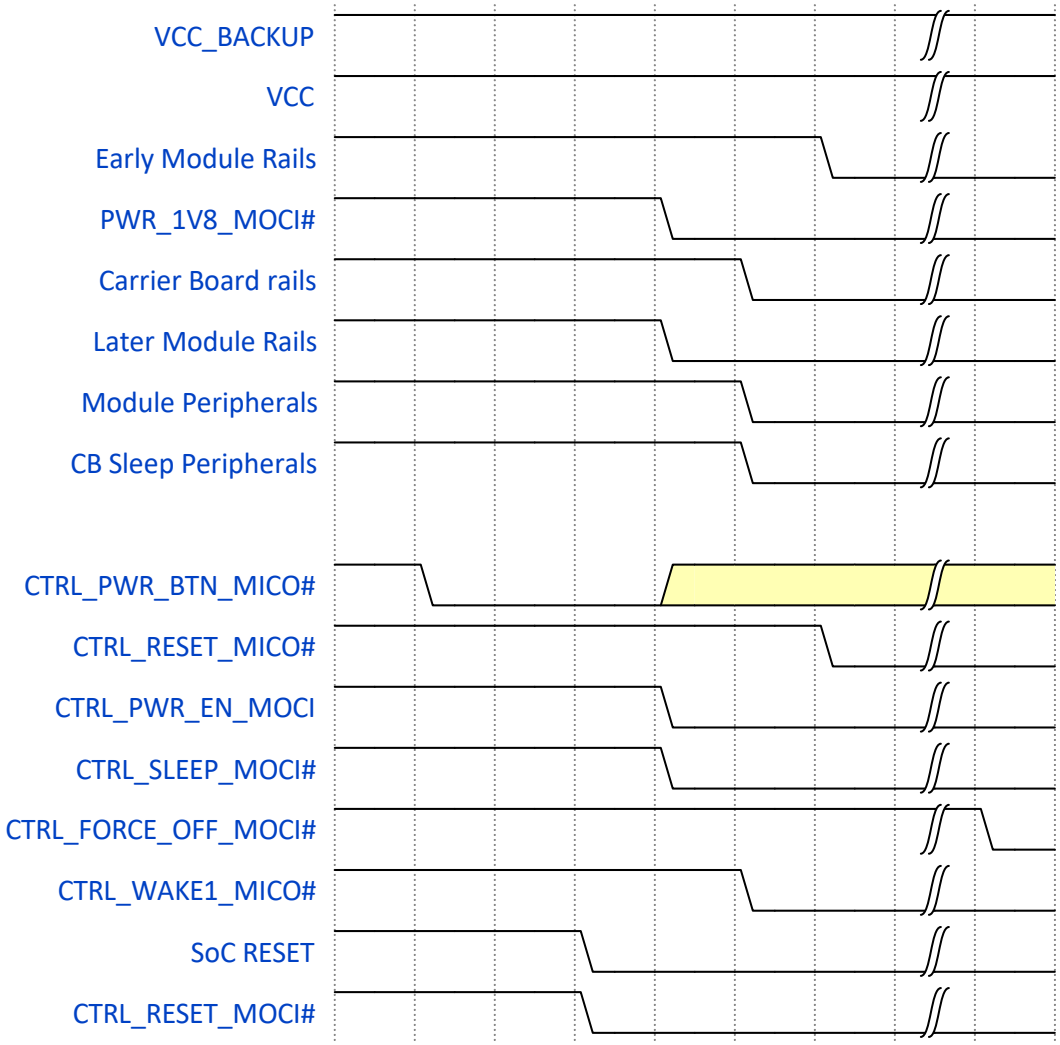


Figure 54: “Running” to “No VCC” (force off) Power Sequence

The force-off sequence is initiated by pressing the power button for more than 5 seconds. The difference between the force-off and a regular shutdown sequence is that the force-off starts without interaction with the operating system. This means the operating system cannot prevent corruption by saving temporary data, flushing buffers, closing files, or disconnecting services. On the other hand, with force-off, the system can be shut down independently of the operating system's state or other software running on the module.

The force-off sequence is identical to the shutdown sequence. This means that the PMIC first sets the reset signals low and then removes the power rails in the required order. After all rails have been removed, there is a delay, after which the CTRL_FORCE_OFF_MOCI# goes low.

3.3.8 "Module OFF" to "Running" (startup after shutdown)

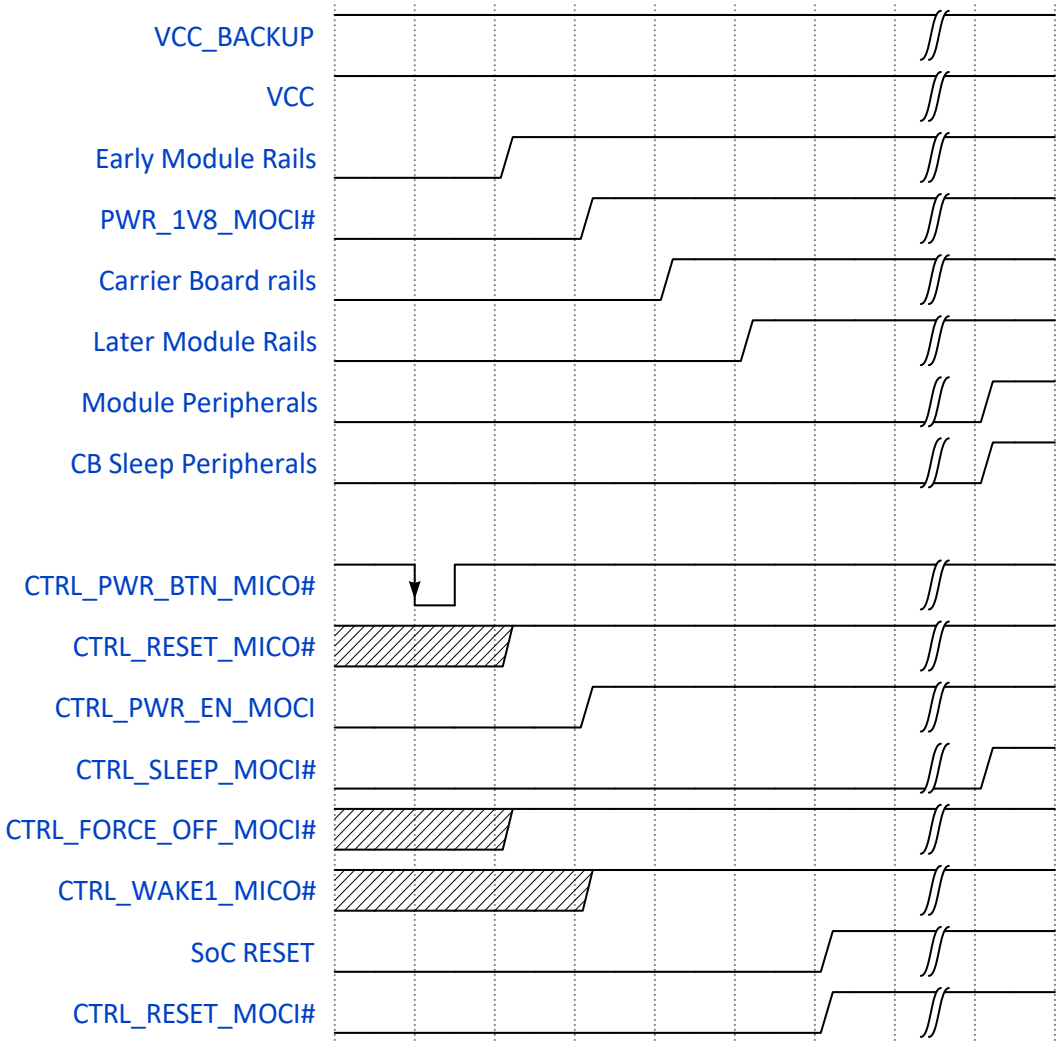


Figure 55: "Module OFF" to "Running" (startup after shutdown) Power Sequence

In the "Module OFF" state, the module can be turned on by a falling edge of the CTRL_PWR_BTN_MICO# signal. The power button must be pressed for less than 5 seconds. If the button is pressed longer than 5 seconds, some modules directly initiate a force OFF sequence. Some modules would ignore a long press to the power button if the CTRL_PWR_BTN_MICO# was not going high after detecting the power-on event. The actual behavior depends on the module (please refer to module datasheets).

After detecting the power button event, the module begins to ramp up all the voltage rails in the same sequence as described in the section "No VCC" to "Running" (startup).

3.3.9 "Module OFF" to "No VCC" (power off after shutdown)

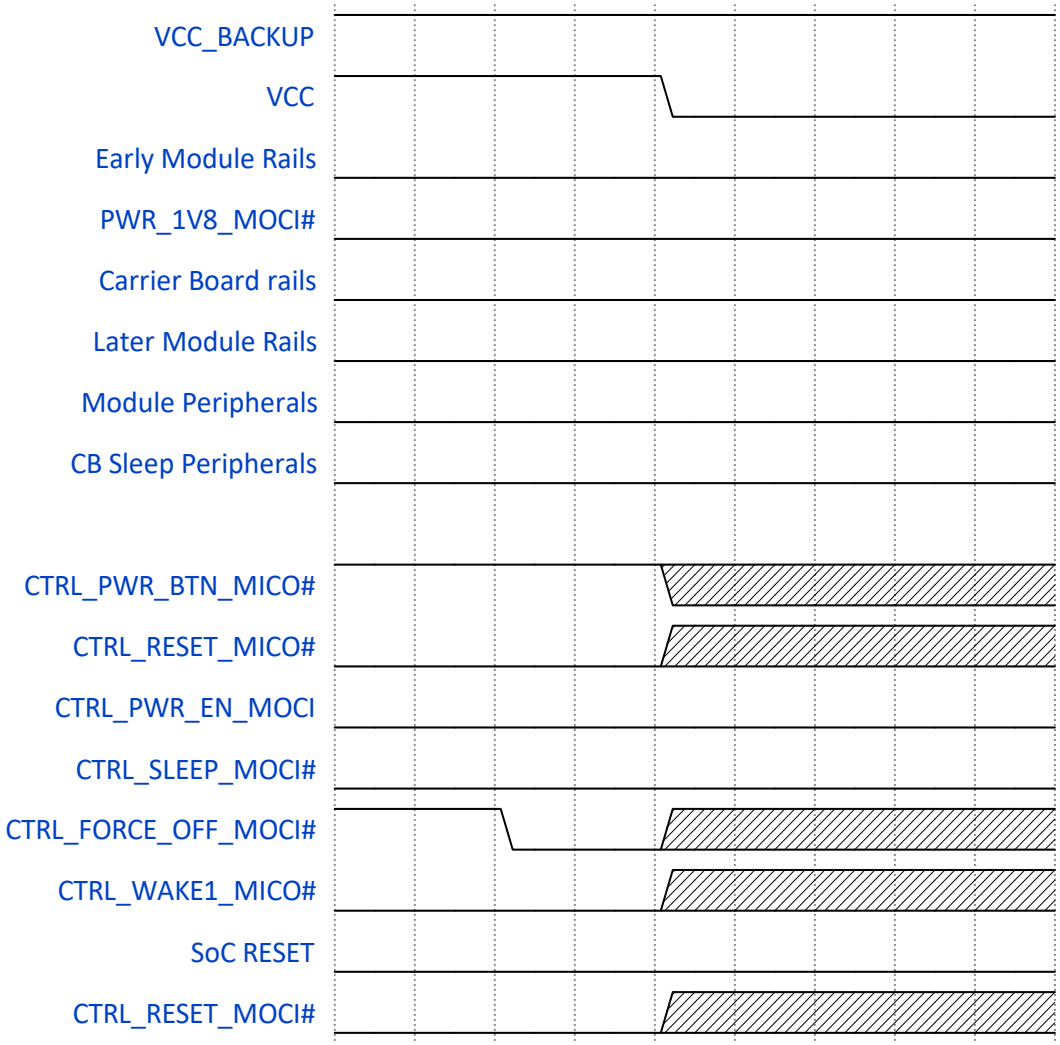


Figure 56: "Module OFF" to "No VCC" (power off after shutdown) Power Sequence

As described in section 3.3.6, "Running" to "Module OFF" (shutdown), the CTRL_PWR_BTN_MICO# goes low after a certain time after the last rail was removed. Depending on the module, this delay can be several seconds. If a carrier board uses the CTRL_PWR_BTN_MICO# signal for killing the main module voltage rail VCC, the system transitions to the "No VCC" state. This means the VCC is removed from the module.

The only rail that is still optionally supplied to the module is the VCC_BACKUP rail for the on-module real-time clock. The carrier board should avoid having any signal driving high connected to the module to prevent back feeding.

3.3.10 Remove VCC in any power state

If the main module power rail is removed in any power state, the different power rails are shut down in a non-graceful order. This should not physically damage the module. However, the flash memory may get corrupted. Therefore, removing the VCC should be avoided if the system was not shut down properly in advance.

3.4 Power Supply Use Cases

The power control pins of the Verdin module are very flexible and allow different use cases for the power supply on the carrier board. The following approaches are just examples of the most common use cases. There are other options possible.

3.4.1 Switched VCC Approach (Verdin Development Board)

The switched VCC approach is basically the one that is implemented on the Verdin Development Board. There is a power button control IC that handles the switching of the main VCC for the module. This approach makes use of the CTRL_FORCE_OFF_MOCI# signal, which switches off VCC after the module has been successfully shut down.

3.4.1.1 Power Block Diagram

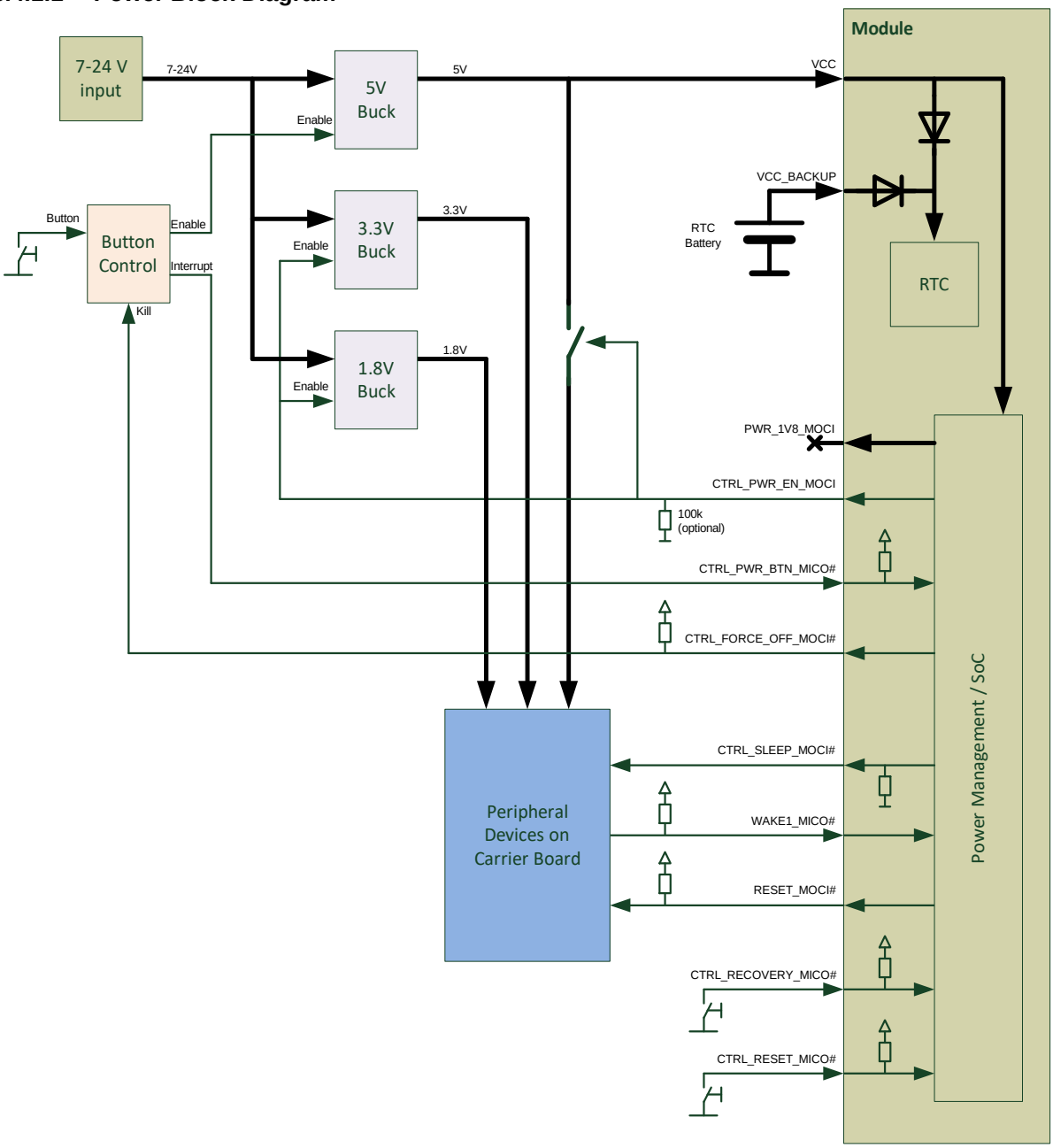


Figure 57: Switched VCC Approach Block Diagram

The module gets powered from a 5V buck regulator. This regulator is enabled by a button control IC. Short pressing the power button enables the 5V buck regulator, which powers up the Verdin

module. The Verdin module then enables the carrier board's peripheral power rails by asserting the CTRL_PWR_EN_MOCI signal. There is an optional pull-down resistor on the CTRL_PWR_EN_MOCI signal. This resistor makes sure the power supplies are not turning on if there is no module inserted. However, this is not required for a carrier board that is never to be operated without a Verdin module.

In this example, the carrier board creates 1.8V, 3.3V, and 5V for the peripherals. For the 1.8V and the 3.3V, there are buck converters on the carrier board, which are enabled by the CTRL_PWR_EN_MOCI signal. Since there is already a buck converter for the main 5V VCC rail, only a switch is required for the peripheral 5V rail. The PWR_1V8_MOCI is not used in this approach since there is a dedicated 1.8V buck on the carrier board.

If the module is running, a short pressing of the power button generates an interrupt output at the power button control IC. This interrupt is connected to the CTRL_PWR_BTN_MICO# input of the module. A falling edge on this input causes a software interrupt. Depending on the configuration, the OS then starts shutting down the software and ramping down power rails on the module. The module asserts the CTRL_FORCE_OFF_MOCI# signal, which kills the enable output of the power button control IC. This disables the main 5V VCC rail.

If the module is running, a long pressing of the power button (>5s) generates an emergency power shutdown of the system. The power button control IC is forwarding the long press event to the CTRL_PWR_BTN_MICO# input of the module PMIC. The PMIC is shutting down all power rails without software interaction. In the end, the CTRL_FORCE_OFF# is asserted, which turns off the main 5V regulator.

3.4.1.2 System Power States

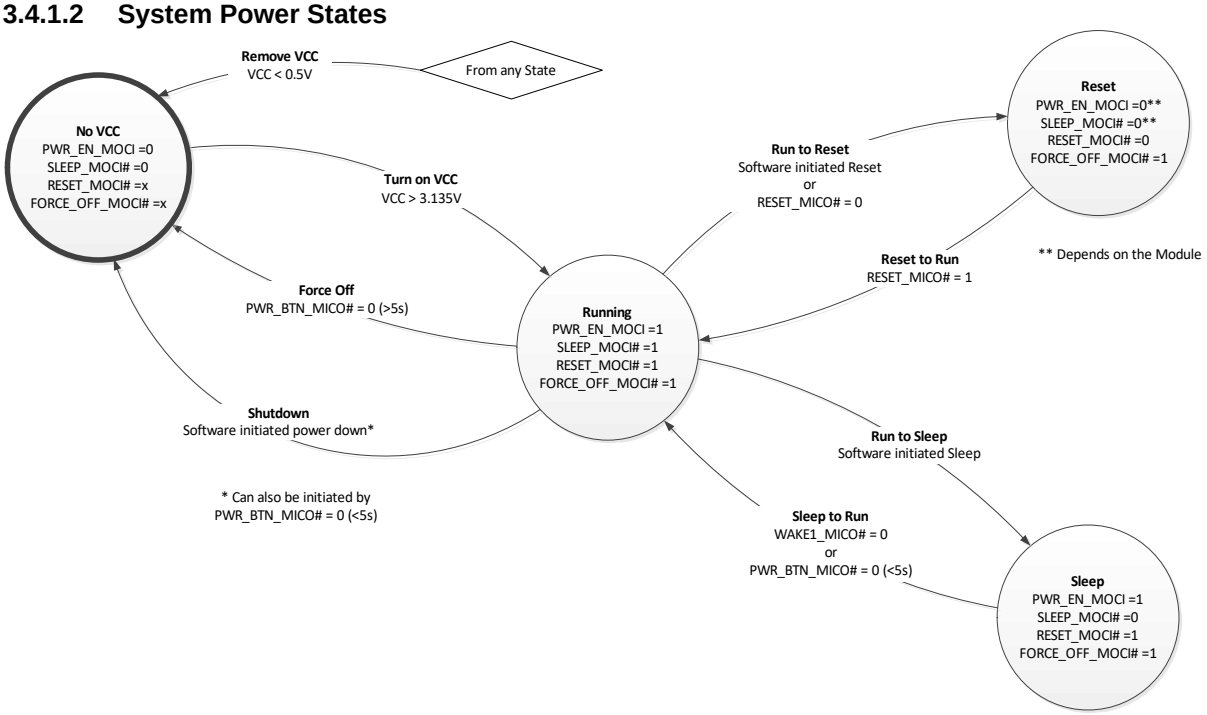


Figure 58: System Power States and Transitions

Compared to the module power states found in section 0, the system does not have a “Module OFF” state. This module state is only temporary since the carrier board kills the VCC when the module asserts the CTRL_FORCE_OFF_MOCI# as a final act in the shutdown and force OFF cycle.

The system is booted by turning on the main VCC rail of the module by the power button IC on the carrier board. This power button IC has an interrupt output which is used to get the power button press information to the Verdin module by connecting it to the CTRL_PWR_BTN_MICO# input. The power button IC on the carrier board also features a shut down by long-pressing the button. This long-press limit must be set to a longer period (e.g., 7 seconds) than the 5-second limit the Verdin

module has. This makes sure that the module performs the force OFF cycle before the power button IC is removing VCC by the long press event.

3.4.1.3 Reference Schematics

Place enough power supply bypass capacitors on the peripheral devices' voltage inputs (see Toradex Layout Design Guide). Place a bypass capacitor on the power input pins of the Verdin module. Be aware of the total capacity on a voltage rail when switching the voltage. If the rails are switched on too fast, the inrush current for charging all the bypass capacitors can be very high. This can produce unacceptable disturbances or can trigger an over-current protection circuit. In such cases, tweak the soft-start functions of the switches and regulators (if available).

For designing the power supply on the carrier board, a current consumption budget needs to be considered. In this approach, the Verdin module is powered from the 5V rail. This means the consumption of the module needs to be in the budget of the 5V buck converter. The module's current consumption that should be put into the budget depends on whether the carrier board should be designed for one specific module or should be compatible with multiple Verdin modules. The Verdin modules are thermally designed for a maximum sustained power consumption of up to 8.25 continuously. However, this means that the peak power consumption and the peak current consumption can be higher. To be compatible with all existing and future Verdin modules, it is recommended to design for at least 12.5W peak module power.

The reference schematic below contains the power button IC circuit and the primary buck converters. Additional schematics and design files of the different Verdin carrier boards are freely available on the Toradex developer website.

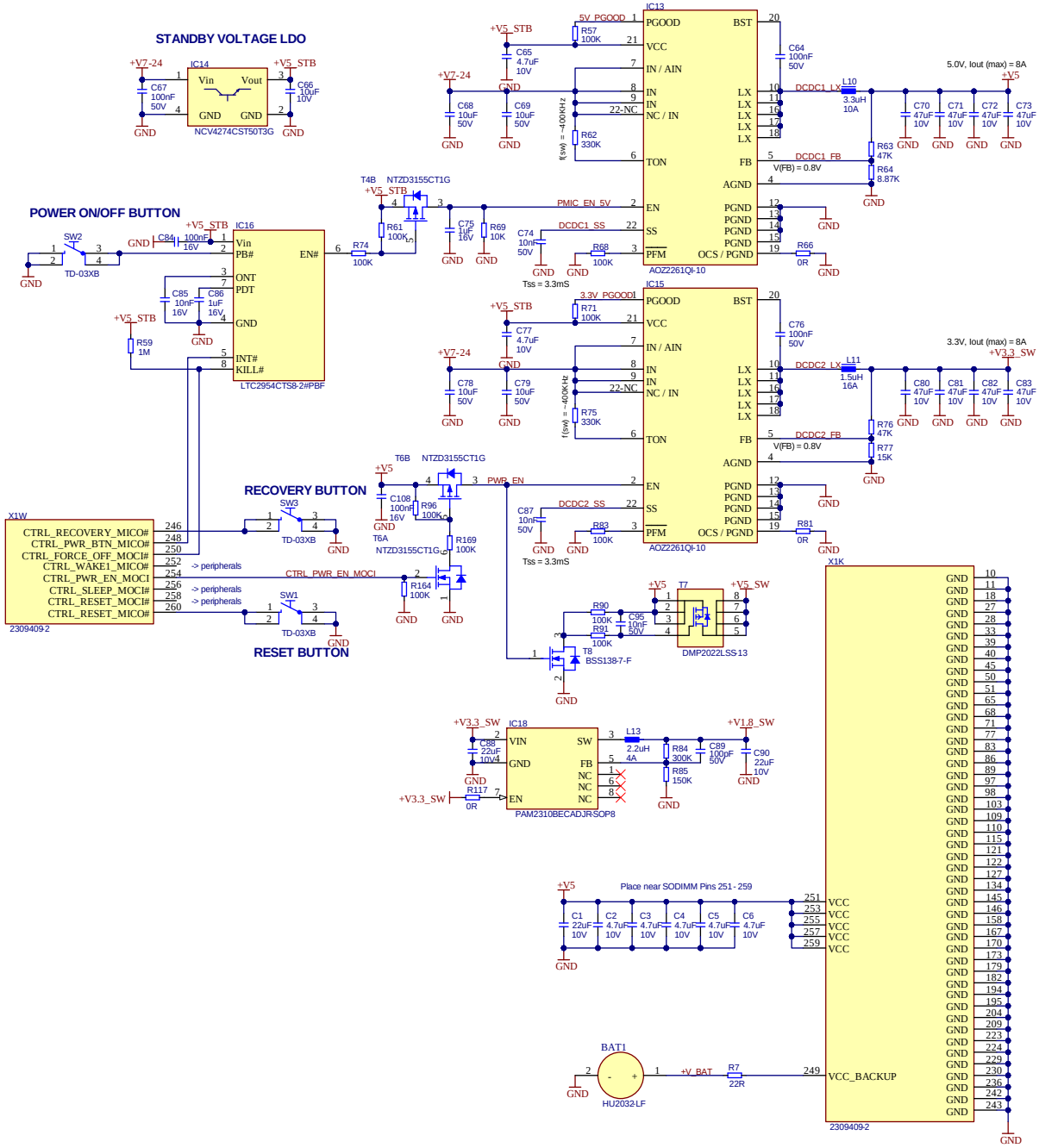


Figure 59: Switched VCC Approach Power Supply Reference Schematics

3.4.2 Minimalist Carrier Board Power Approach

The minimalist carrier board power approach shows the absolute minimum amount of external components required for running the Verdin module with a carrier board. The Verdin module can run directly from any power source between 3.135V and 5.5V. This means that the module can run directly from a 5V USB power port. The PWR_1V8_MOCI provides up to 250mA output current from the module to peripherals on the carrier board. This means that for simple applications - which only feature a few sensors and peripherals on the carrier board - no extra 1.8V buck converter is needed.

3.4.2.1 Power Block Diagram

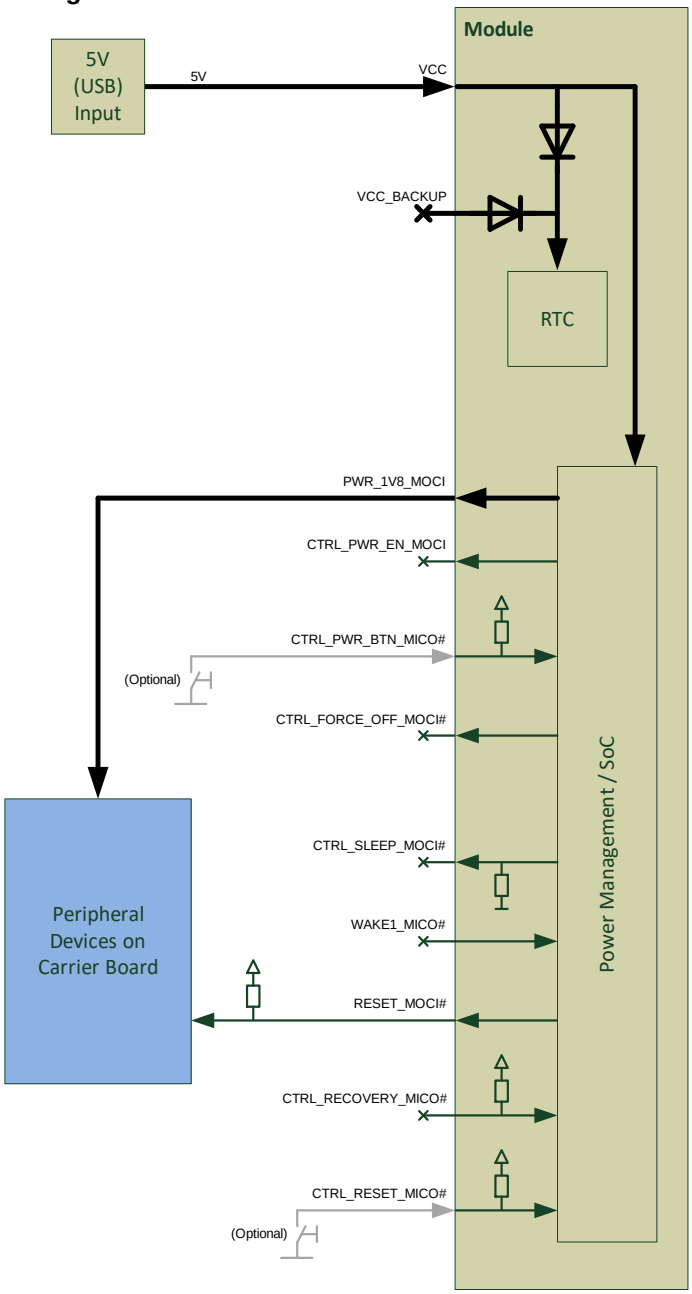


Figure 60: Minimalist Power Approach Block Diagram

In this approach, the module is directly powered from a 5V USB power input. It must be noted here that for being USB compliant, it is required to add a circuit that detects whether the USB power source is actually able to deliver enough current (USB BC 1.2 or USB PD detection) and the actual current consumption of the system does not exceed the limits. However, these circuits are not in this minimalist approach for the sake of simplification. This approach can also be used for any other power source from 3.135V to 5.5V (e.g., simple barrel connector power supply).

The 5V from the USB is directly connected to the VCC input voltage of the module. No further buck regulator is needed. The module starts automatically when the VCC is applied. The VCC_BACKUP is not required for running the module. However, without a coin cell battery on VCC_BACKUP, the real-time clock is only running if the VCC rail is available.

Optionally, a simple push-button can be added to the CTRL_PWR_BTN_MICO# and the CTRL_RESET_MICO# input. Short pressing the power button when the system is booted generates a software interrupt. Depending on the configuration, the OS starts shutting down the software

and ramping down power rails on the module (including the PWR_1V8_MOCI). In this off-state, the system can be turned on by pressing the power button again. A long pressing on the power button (>5s) initiates an emergency power shutdown. All power rails are turned off. The module can be turned back on by using the power button. Without the power button, the module can only be turned on after shutting it down in software and power cycling the main VCC rail after.

All the rest of the power management signals can be left unconnected.

3.4.2.2 System Power States

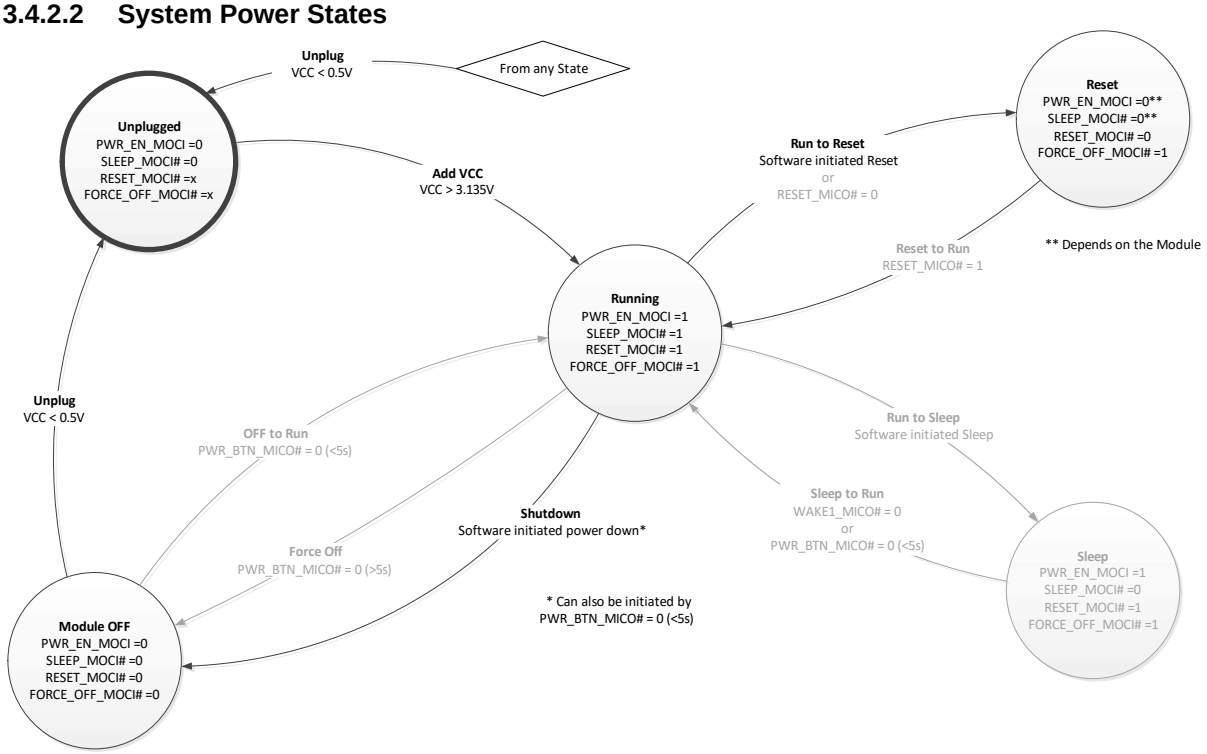


Figure 61: System Power States and Transitions

The sleep state is optional. Therefore, this state and its transitions are grayed out in the state diagram. If the reset button (CTRL_RESET_MICO#) is not implemented in such a power scheme, it is still possible to do software-initiated reset cycles. Without implementing a power button (CTRL_PWR_BTN_MICO#), the only option for exiting the module OFF state is to "unplug" the system.

3.4.2.3 Reference Schematics

The reference schematics below show the minimum amount of external components required for running the Verdin module.

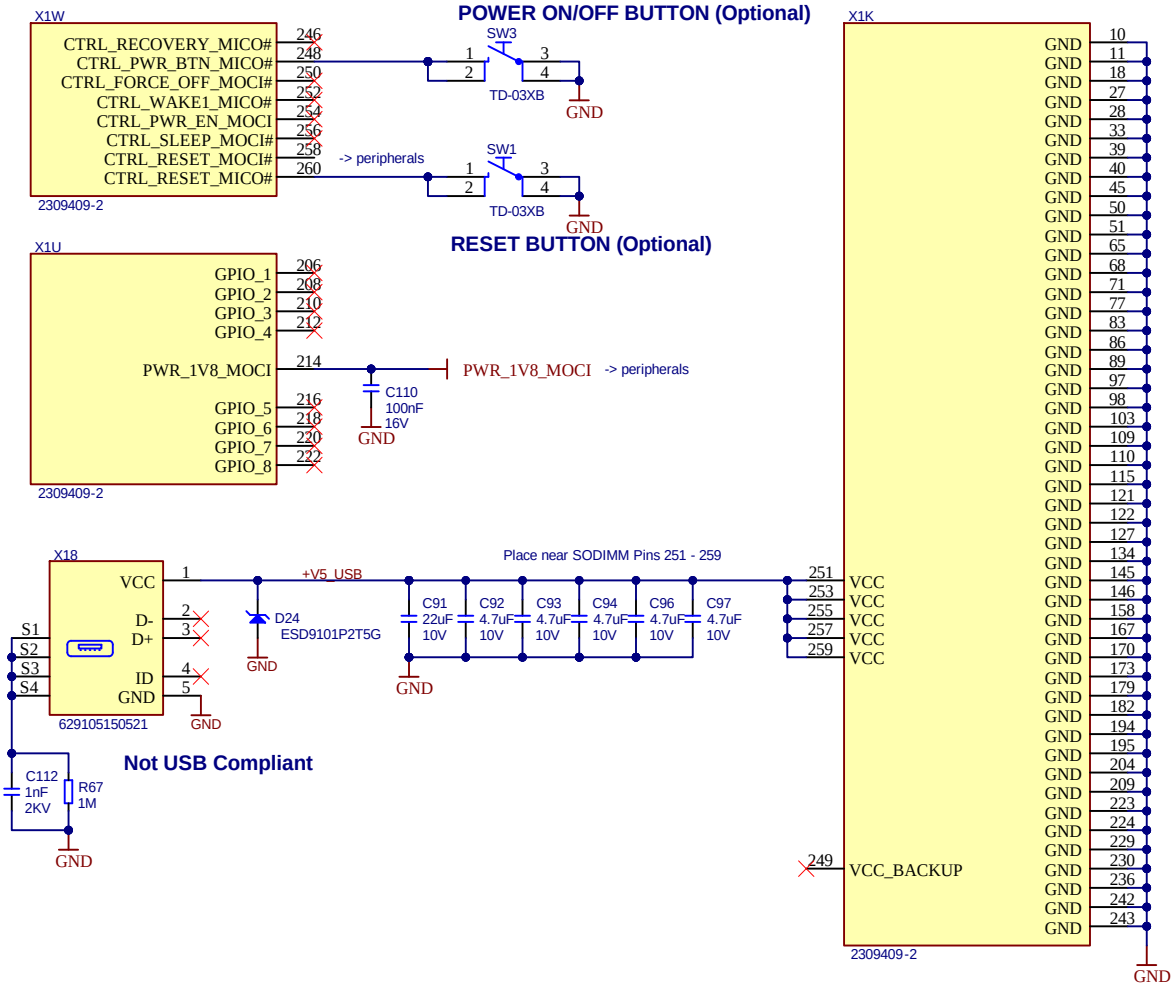


Figure 62: Minimalistic Power Supply Reference Schematics

Please note that this circuit is not compliant with the USB specifications. An additional circuit is required that detects whether the USB power source can deliver enough current and the system does not exceed these limits. This can be achieved by a USB BC 1.2 detection IC or - in the case of a USB-C power source - a USB PD detection IC.

3.4.3 Single Cell Battery Power Approach

The wide input voltage range of the Verdin module allows it to run directly from a single cell Li-ion battery. This makes it much easier to implement a rechargeable battery solution for the Verdin module. When charging a regular Li-ion battery, the voltage rises to a maximum of 4.4V. The cell gets damaged when it gets discharged below 2.5V. The Verdin module runs guaranteed down to a minimum input voltage of 3.135V. Battery voltages falling between 3.135V and 2.5V represent a capacity reserve that cannot be used with Verdin modules. While this represents only a tiny portion of total battery capacity, it also helps prevent battery deep discharge events from happening.

3.4.3.1 Power Block Diagram

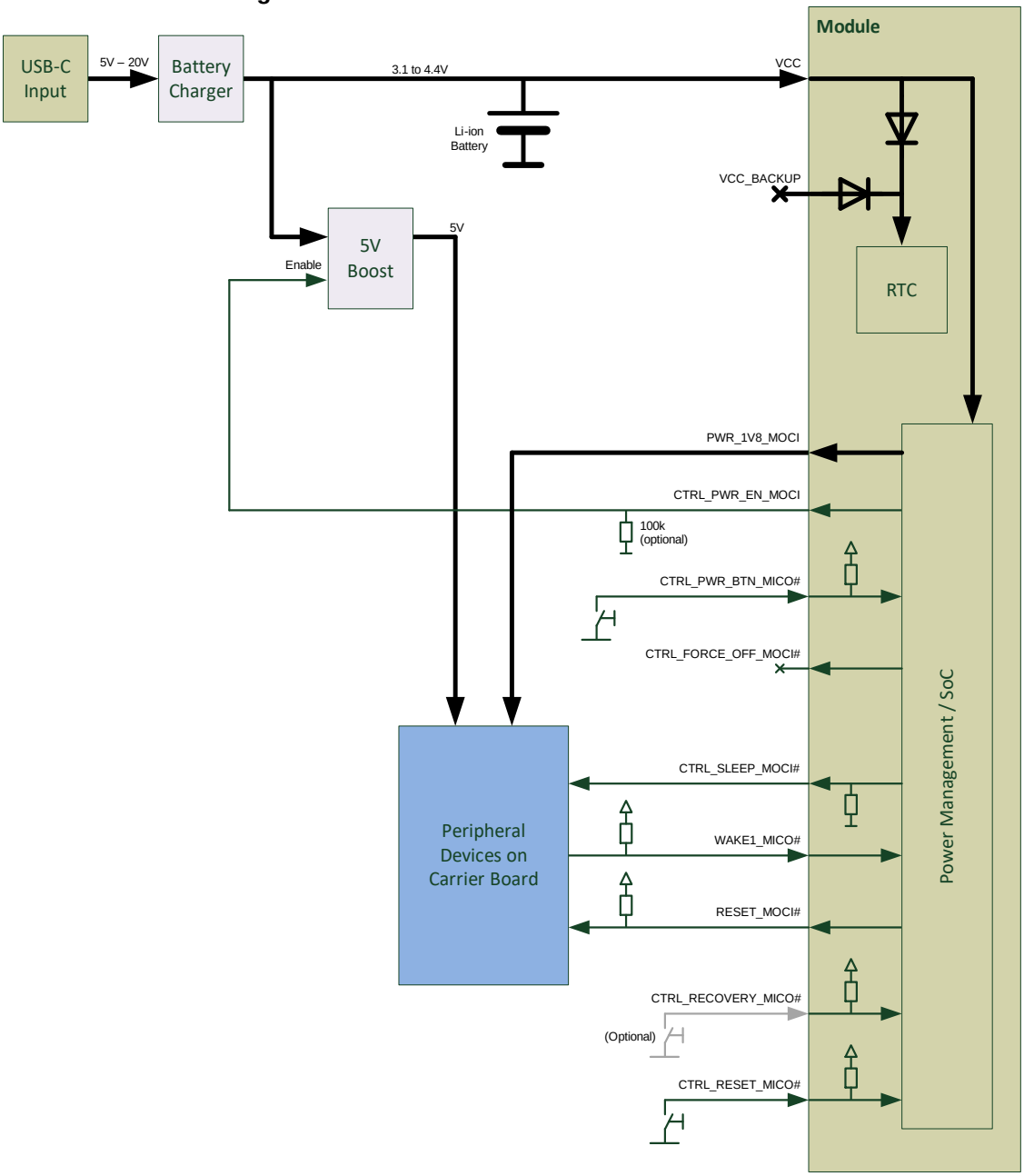


Figure 63: Switched VCC Approach Block Diagram

The module VCC can be connected directly to the system voltage, which is coming from the battery charger IC and is also used for charging the Li-ion battery. Having the module VCC connected directly to the system battery means that VCC is available to the module all the time, and the VCC_BACKUP rail is not required to be provided to the module.

The system voltage can range from 3.135V to 4.4V, making the creation of a 3.3V +/-5% rail challenging. A better approach is to run peripherals from 1.8V and reducing the components on the 3.3V supply. Some interfaces like the SD card require a 3.3V rail. Since the SD card can officially run down to 2.7V, a suitable option could be using an LDO regulator with a very low dropout or a buck converter with a constant-on option.

3.4.3.2 System Power States

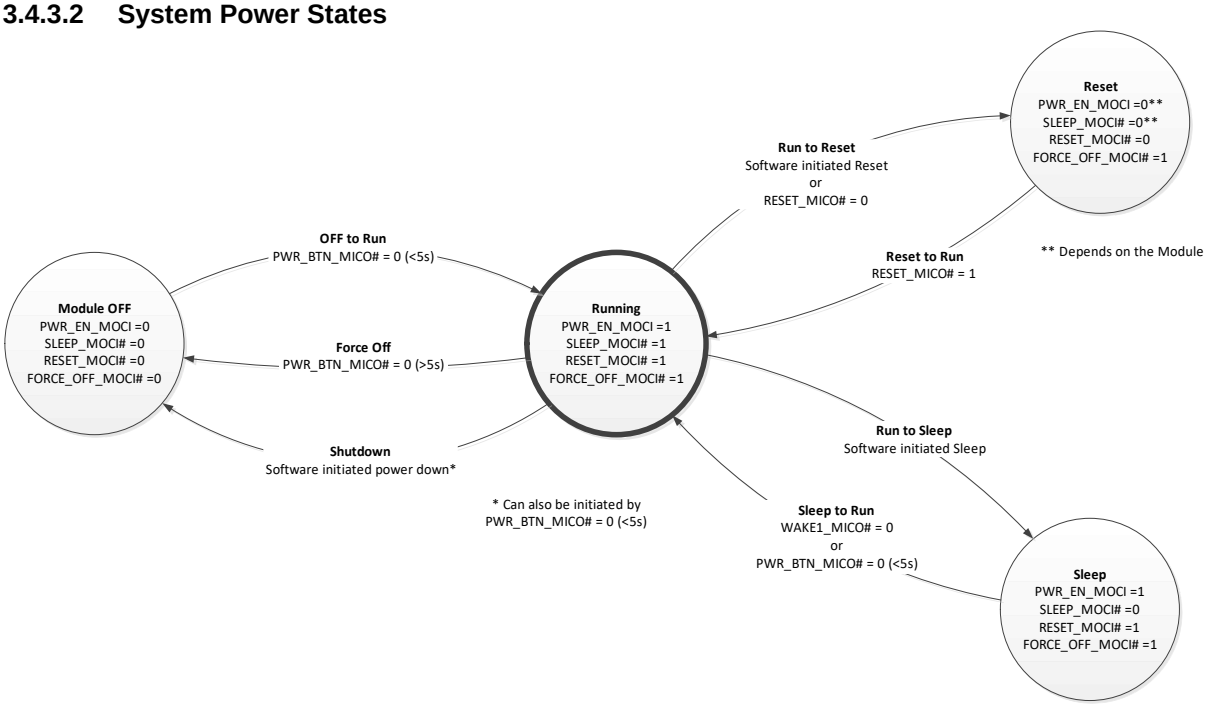


Figure 64: System Power States and Transitions

Since the main voltage VCC is always available on the module, the state "No VCC" does not exist in this approach. The carrier board ignores the CTRL_FORCE_OFF_MOCI# signals, which means the module remains in the "Module OFF" state. The power consumption in this state is small enough for keeping the VCC rail permanently on for several months with a regular Li-ion battery.

It should be noted that the module is directly turning on when the Li-ion battery is attached for the first time during production. While the ramping up of the module voltages cannot be prevented, the booting of the module can be prevented by keeping the CTRL_RESET_MICO# low. This allows to shut down the module by long-pressing CTRL_PWR_BTN_MICO# without actually booting the module.

3.4.3.3 Reference Schematics

TBA

3.5 Backfeeding

3.5.1 Introduction

Backfeeding is sometimes also called backflow. Backfeeding is an unintentional and irregular flow of current mainly over the signal path. It can happen if interfaces are crossing different power domains. Backfeeding can happen between circuit blocks powered by or switched by different power rails (power domains) and thus transitioning through different power states over time. A domain that is still powered can feed another power domain. This can lead to residual voltages on a power rail that is supposed to be turned off.

The most obvious consequences of backfeeding are increased power consumption, unexpected behaviors, failing power-on resets, and in the worst-case, damages of interfaces. This section discusses why backfeeding occurs, how it can be identified, and potential preventions of backfeeding in a Verdin carrier board design.

Interfaces that are prone to backfeed are UART, RS232, HDMI, and I2C. Therefore, special attention is required to these interfaces when designing a carrier board for the Verdin module.

3.5.2 What is Backfeeding

Backfeeding is sometimes also called backflow. To understand what backfeeding is, we need to look at the internal circuit of an input pin. Most Verdin module pins (and also peripheral device input pins) feature ESD protection diodes. These protection diodes provide basic protection for electrostatic discharge. Depending on the SoC and peripheral devices, the pins are typically only protected up to 1kV (Human Body Model) or 250V (Charged-Device Model). This means additional ESD protection is still needed for signals that are exposed to the real world. The basic ESD protection is usually accomplished with two (Schottky) diodes. One diode is between the pin and the ground, and a second between the pin and the power rail of the I/O block (IO rail). These diodes are the reason why for a lot of IO pins, the absolute maximum voltage is specified as VDD+0.3V.

Figure 65 shows a typical low-speed SoC input pin with ESD protection diodes. If the IO rail and the peripheral rail are turned on, these ESD diodes are not conducting. The diodes can basically be ignored. There is a small current flowing from the peripheral output to the input buffer of the SoC. This is not backfeeding. This is a regular signal current.

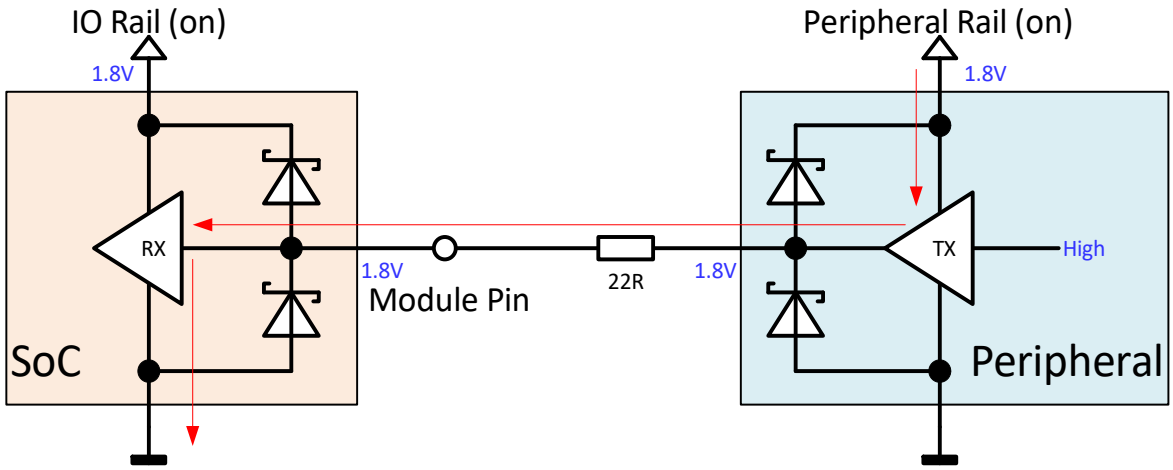


Figure 65: SoC input pin with ESD protection, both power rails on

But what happens if the on-module IO rail is turned off while the peripheral rail is still on and the peripheral signal is set to high? In this situation, there is a non-marginal current from the output buffer of the peripheral interface into the SoC input pin. Since the IO rail is turned off, the upper ESD protection diode of the input pin becomes forward-biased. The current flows through the diode to the IO rail pin. In other words, the IO rail gets fed through the IO pin. This is called backfeeding. Figure 66 shows a backfeeding path and possible voltage values. Depending on the situation, the backfeeding can reach several milliamperes. Therefore, the output buffer of the peripheral signal already has some voltage drop. In the example, the drop in the buffer is 0.2V. This means the output voltage is only 1.6V. Some voltage is lost in the series resistor. Therefore, only 1.3V arrives at the SoC input pin. There is a further voltage drop in the ESD protection diode. 0.3V is a typical value for a Schottky type diode. In this example, the backfeeding path lifts the IO rail to 1V, even though the power supply is turned off. Of course, the actual resulting IO voltage is heavily dependent on the load on the IO rail and the backfeeding path and the number of pins that are backfeeding.

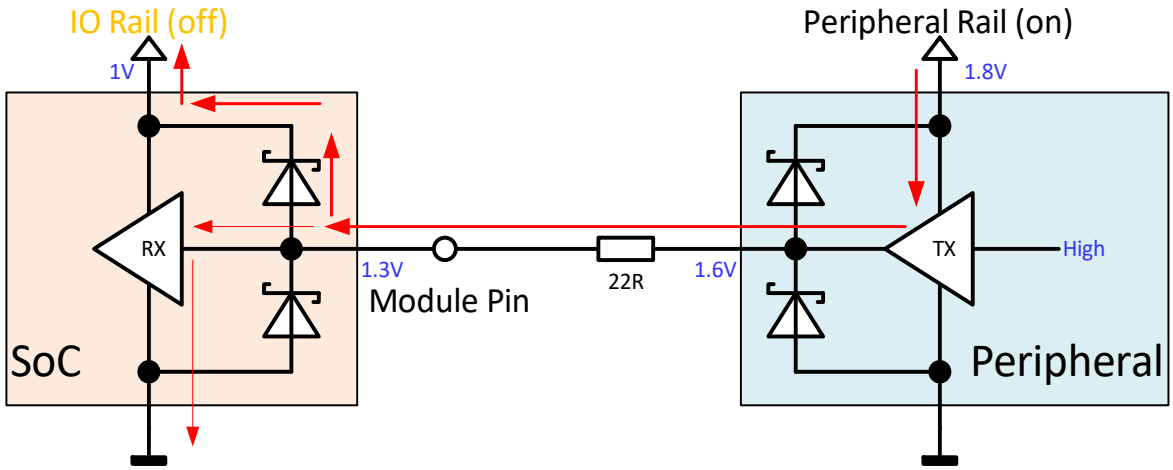


Figure 66: Backfeeding if IO rail is off and the peripheral signal is high

Open drain signals can also cause backfeeding if the pull-up resistor is still powered while the IO rail on the module is off. However, the backfeeding currents are more likely much smaller than with a regular push-pull peripheral output pin. The pull-up resistor value limits the current.

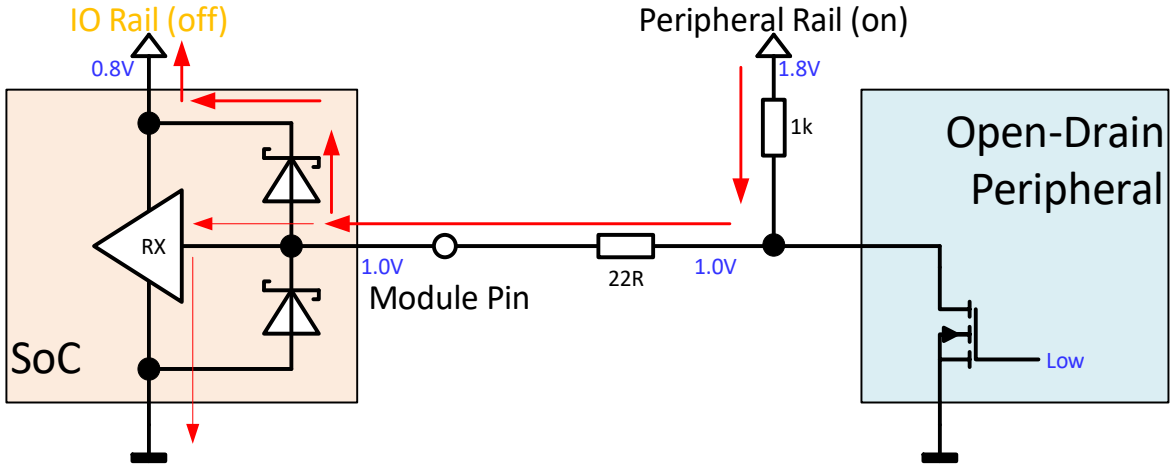


Figure 67: Backfeeding with open-drain signals

Interfaces that are prone to backfeeding are, for example, UART and HDMI. The problem is that the UART signals are high in idle. If the transceiver is not switched off when the module is shut down, there is potential backfeeding. The transition-minimized differential signals (TMDS) of the HDMI interface are terminated to 3.3V at the receiver side (e.g., a display). Therefore, the signals have a DC offset. Even if the module and carrier board are turned-off, the TMDS signals can be lifted to 3.3V by the monitor. If an improper HDMI circuit is used, this can cause backfeeding. The DDC and the hotplug detection signal can cause further backfeeding in combination with an HDMI monitor.

Besides the HDMI DDC, I^2C interfaces, in general, can be sources for backfeeding if the pull-up resistor is using a different voltage domain than the module IO rail. Due to the pull-up resistor value, the current usually is smaller than with regular CMOS signals. However, with backfeeding, the amount of interface pins that are backfeeding signals is essential. If a system has many open-drain signals backfeeding, this can still lead to problematic high IO rail voltage.

Backfeeding can also happen in the other direction. For saving energy, unused peripherals are often turned off by switching off their power rails. If the module output signals are still driven high, the module can feed back the peripheral rail.

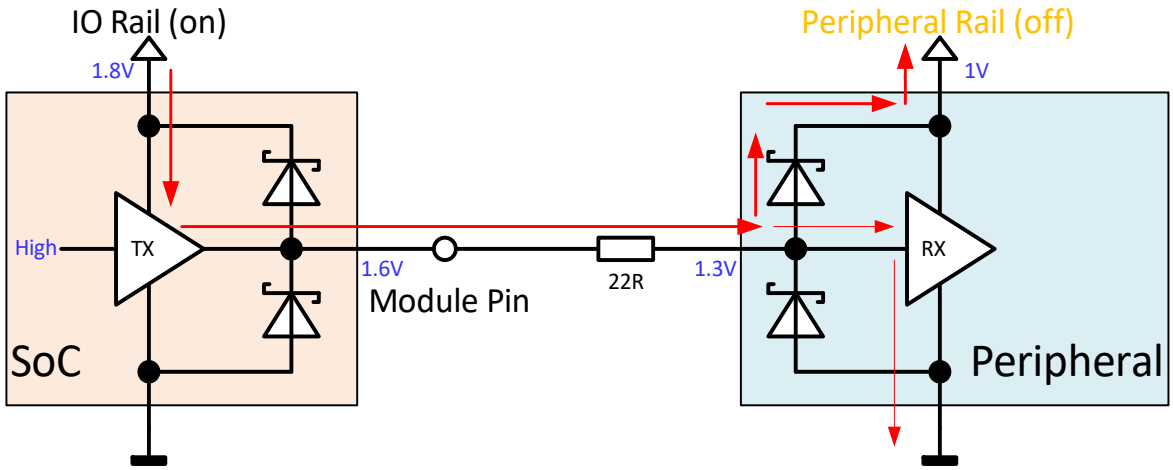


Figure 68: Backfeeding to peripherals

3.5.3 Potential Issues Caused by Backfeeding

In many systems, it is difficult and expensive to avoid backfeeding altogether. Various issues could be caused by backfeeding. For example, the resulting backfeeding current could overload the output driver of the signal causing the backfeeding. If the backfeeding path has series resistors, the current might get limited to a non-damaging value. Series resistors also allow for checking the backfeeding current by measuring the voltage drop over the resistor. A high continuous backfeeding current can also damage the ESD protection diode. Standard on-chip ESD protection diodes are characterized to withstand tens of amps for nanoseconds, but not continuously. Continuous current through the protection diode causes power dissipation, which can be above the diode's limits. However, a few milliamperes are usually neither damaging the ESD protection diode nor the output driver. Please check whether there any information available in the SoC and peripheral datasheets.

Even if the resulting input current of a pin is small enough not to damage the ESD protection diode, the absolute maximum input voltage specifications are violated in many cases. An input pin's absolute maximum input voltage is often specified by a similar formula:

$$V_{in\,max} = V_{DD} + 0.3V$$

The ESD protection diode dictates the 0.3V in this formula. According to the device specifications, the input voltage always needs to be small enough for not having the protection diode conducting. This means backfeeding is often per se violating the maximum input voltage specifications. Therefore, the manufacturer does not guarantee that backfeeding is not damaging the device.

Damaged input or output signal paths due to backfeeding current are usually a minor problem. Issues caused by a residual voltage on a turned-off IO rail are often more pronounced. If the IO rail reaches a certain voltage level, other devices on the same rail might show unexpected behavior. Especially if the voltage level reaches the power-on-reset threshold, devices (or blocks of devices) might start to run. This could lead to a higher current draw on the backfeeding path, which could lower the voltage again. This could cause cyclical behavior in which devices are oscillating between starting and crashing. Such behavior could result in higher overall power consumption or even audible noise of power converters. Some LEDs may slightly light up or start blinking.

Backfeeding can cause latch-up situations. IO blocks can go into unintended states, which might even cause short-circuits that could lead to further chip damages if countermeasures are not taken.

If the IO rail reaches a certain voltage level, it could mean that some power-on-reset circuits are not triggering when fully turning on the power rails since the reset was already released. This can

cause devices and peripherals to stay in unintended/unpredictable states and might fail to boot the system. The system could be locked up by backfeeding.

Whether backfeeding is actually causing issues or not depends on the backfeeding current and its residual voltage on the IO rail. It also depends on the specific chip design. The lower the current per backfeeding pin is, the smaller the chance of damage is. The lower the remaining voltage on the IO rail is, the smaller the chance of unexpected behavior is. As a rule of thumb, a few milliamperes are unlikely to cause damages to an IO pin. If the resulting IO rail voltage is below 0.5V, issues are often not to be expected. However, these are just rough numbers. The actual limits are heavily depending on the system and the actual devices in use.

3.5.4 Identify Backfeeding Issues

3.5.4.1 System Design

Ideally, potential backfeeding issues should be identified in the design phase of a carrier board, not in the prototype phase. A power delivery block diagram can help to identify different power domains. A power domain is a group of devices or peripherals which are always in the same power state. Figure 69 shows a simple example of a system block diagram. The Verdin module and the RS232 transceiver are in the same power domain. The transceiver uses the PWR_1V8_MOCI, which switches on together with the IO rails of the module.

On the other hand, the camera is in a different power domain since its power gets enabled by the CTRL_SLEEP_MOCI# signal. Therefore, the power rails of the camera are switched off during sleep states. In this example, the SD card is also in its own power domain since the SD_1_PWR_EN signal individually controls the card power. Also, external devices like the HDMI display or the host PC must be considered as separate power domains. These peripheral devices are powered independently from the Verdin carrier board.

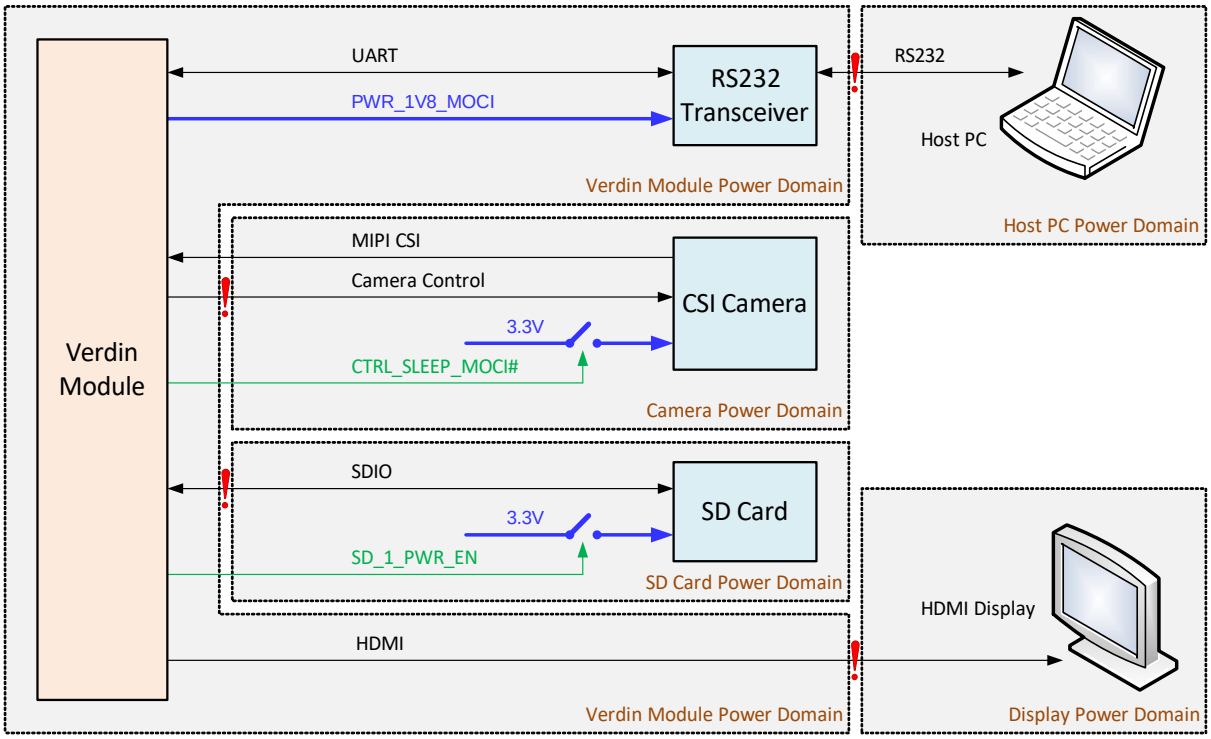


Figure 69: Power Domain Example

Each time a signal crosses the boundaries of power domains, you need to check whether backfeeding could be an issue. For each signal, check whether the output is driven high while the other side's power domain is turned off. In the example above, we need to check whether the software drives a camera control signal high while the system is in sleep mode (CTRL_SLEEP_MOCI# low). In the Verdin platform, the pull-up resistors of the SD card interface are

on the module. Therefore, the pull-up resistors need to be disabled (or its power rail be turned off) while the SD_1_PWR_EN turns off the card rail. Otherwise, the module can back feed to the card. The signal states of the external devices like the RS232 signals of the host PC or the display's HDMI signals are hard to control by the Verdin module and the carrier board. Therefore, it might be required to take other countermeasures for preventing the backfeeding of these interfaces.

3.5.4.2 Prototype Testing

For identifying backfeeding on a system with a Verdin module, it is recommended to measure the IO rails of the different power domains in different scenarios. Different scenarios mean testing different power states of the systems with different types of peripheral devices plugged in and turned on. If you can measure any significant residual voltage on an IO rail, further investigations are required for identifying the source of the backfeeding.

The first option is to unplug external peripherals and observe the residual voltage. If the voltage drops, the peripheral signals are likely a source of backfeeding. If you measure residual voltage in one power domain, all the input signals crossing this domain should be checked. Measure the voltage levels on these inputs. A pin that is the source for backfeeding has a higher voltage than the residual voltage on its IO rail. Typically, due to the protection diode in the backfeeding path, the voltage at the input pin is around 200mV to 300mV higher than the residual voltage (see Figure 70)

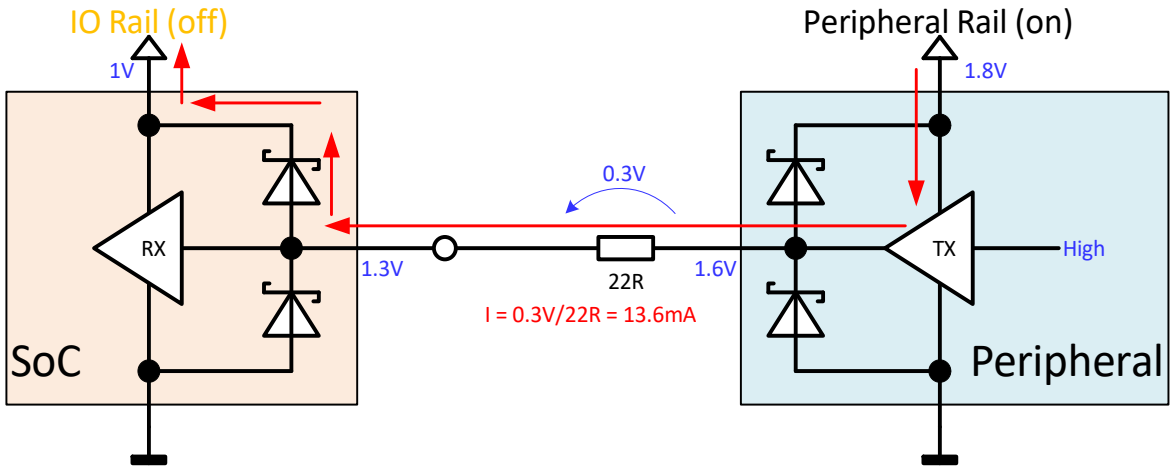


Figure 70: Measuring backfeeding current

If a signal features a series resistor, the voltage drop can be used to measure the backfeeding current. Some signals might not have a series resistor for measuring the current. By adding a load resistor to the backfeeding signal (for example, a 100Ω resistor), the voltage with and without extra load can be measured. This allows to estimate the internal resistance of the driver by using the following formula:

$$R_i \approx \frac{(V_{no\ load} - V_{load}) \cdot R_{load}}{V_{no\ load}}$$

With the help of the estimated internal driver resistance, the backfeeding current on the pin can be estimated by using the following formula ($V_{peripheral\ IO\ rail}$ is the peripheral rail voltage, $V_{backfeeding}$ is the voltage on the signal without the extra load resistor):

$$I_{backfeeding} \approx \frac{(V_{peripheral\ IO\ rail} - V_{backfeeding})}{R_i}$$

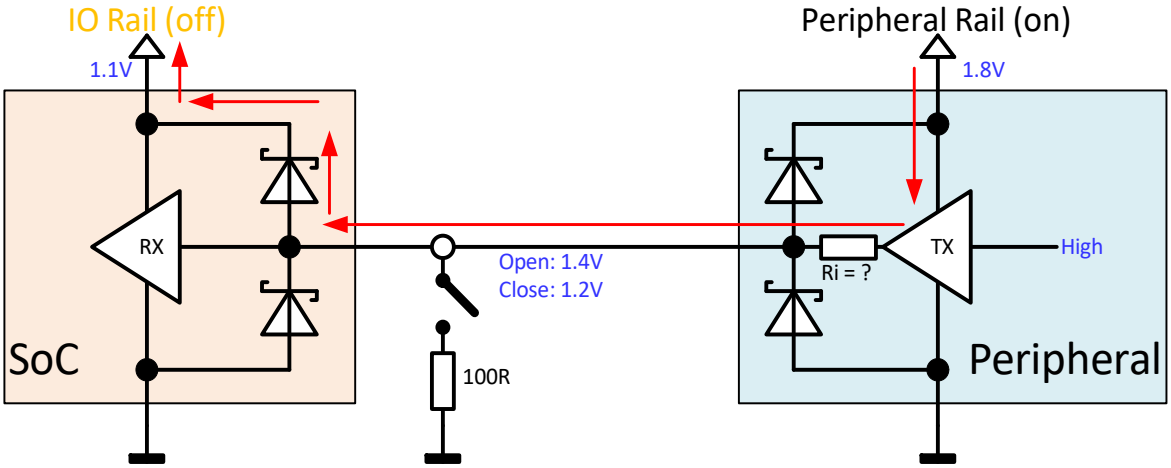


Figure 71: Evaluating the internal resistance of the driver

With the help of these formulas, the measured values in Figure 71 would lead to the following internal resistance and backfeeding current:

$$R_i \approx \frac{(1.4V - 1.2V) \cdot 100\Omega}{1.4V} = 14.3\Omega$$

$$I_{backfeeding} \approx \frac{(1.8V - 1.4V)}{14.3\Omega} = 28mA$$

Often it is crucial to know whether all the backfeeding pins are identified, or the search for backfeeding sources must continue. Ideally, you might be able to disconnect individual pins by removing series resistors or a jumper (for example, possible on the Verdin Development Board). Unfortunately, this is not always the case. However, there is another method for estimating the number of backfeeding pins.

By adding a load resistor to the IO rail and observing the residual voltage changes, the total internal resistance of the backfeeding can be estimated. A good value for the load resistor is 100Ω. You might need to select a different value if the voltage is dropping too little or too much. The best values can often be achieved by a voltage drop between 50mV and 100mV. The formula for estimating the internal resistance is the same as used for the individual pin. Assuming the voltage drop over the ESD diode is constant, the diode voltage drop is eliminated from the formula. Please keep in mind that this formula only provides a rough estimated value. There might be devices on the IO rail which behave non-linear to voltage changes. Therefore, the forced voltage change should be kept small for better results.

$$R_{i\,total} \approx \frac{(U_{no\,load} - U_{load}) \cdot R_{load}}{U_{no\,load}}$$

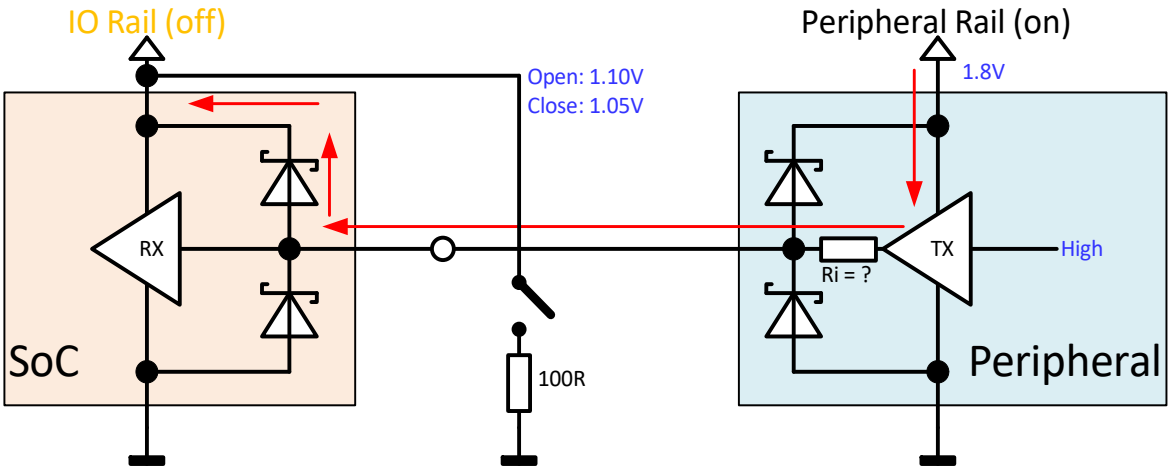


Figure 72: Evaluating the total internal resistance of the backfeeding

Using the numbers in Figure 72 as an example, we get the following total internal resistance:

$$R_{i\,total} \approx \frac{(1.10V - 1.05V) \cdot 100\Omega}{1.10V} = 4.5\Omega$$

The total internal resistance measured on the IO rail can then be compared to the estimated internal resistance of the backfeeding IO pins. If the total resistance is smaller than the combined resistance of the IO pins, there are still other backfeeding sources to be uncovered.

Comparing the results from Figure 71 and Figure 72, we see that the total internal resistance is around three times smaller than a single signal pin. This means there are probably a total of three (similar) signal pins that are backfeeding to this IO rail.

3.5.5 Backfeeding Prevention

There are multiple approaches for preventing backfeeding from happening. Some of them are very cost-effective but do not apply to all types of signals or situations. Other solutions are expensive or require extra precious PCB real estate. Therefore, defining the right backfeeding prevention approach is challenging. The following list of potential solutions starts from the cheap and straightforward approaches and stretches to the complicated and expensive ones. This is not a complete list. There are other solutions that are not discussed here. Some backfeeding countermeasures are specific to an interface. Therefore, following the reference schematics is advised.

3.5.5.1 Avoid Multiple Power Domains

The best solution for preventing backfeeding is trying to avoid having different power domains. If the peripheral rails are turned off together with the Verdin module's IO rails, backfeeding cannot happen. This can be accomplished by using the output rail PWR_1V8_MOCI for powering the peripherals. The PWR_1V8_MOCI is designed to be turned on together with the IO rails on the Verdin modules. The same is achievable by using the CTRL_PWR_EN_MOCI signal for switching peripheral rails on the carrier board.

Both Verdin module outputs, the PWR_1V8_MOCI, and CTRL_PWR_EN_MOCI have been introduced with backfeeding prevention in mind. It is recommended to use these signals on a custom carrier board.

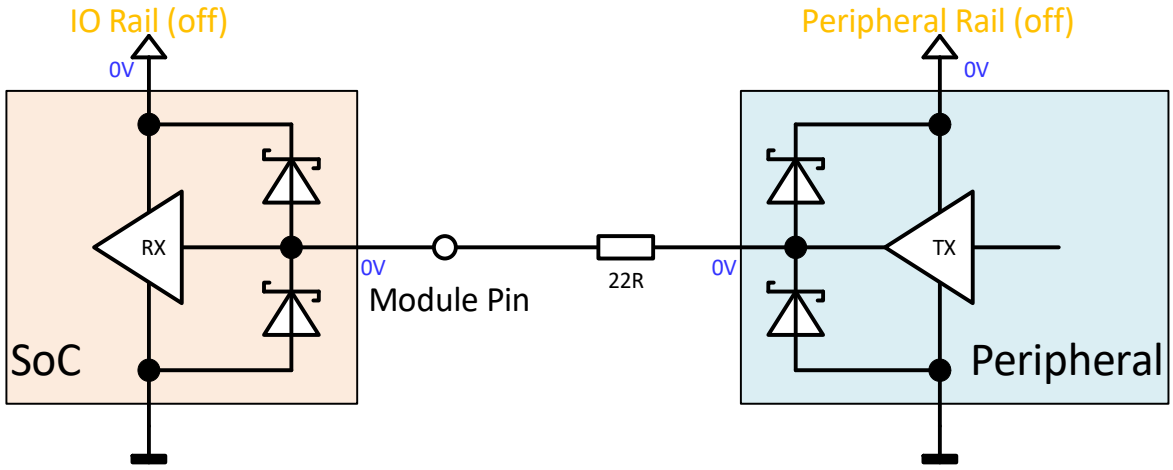


Figure 73: Keep the peripherals on the same Domain

3.5.5.2 Avoid Driving Outputs High

Backfeeding can be prevented by ensuring the output pin is not driven high while the IO rail of the input side is powered off. This is a standard solution for preventing backfeeding from the module to peripheral devices. Before disabling the peripherals' power rails (for example, when going into sleep mode), the software makes sure that the output signals are either driven low or set into a high-Z mode. Some SoC pins have internal pull-up resistors. It is also important to switch off the pull-up resistors and optionally enable the pull-down resistor.

An example of this backfeeding prevention solution is the SD card interface of the Verdin module. The SD card signals feature pull-up resistors, either located inside the SoC or on the Verdin module. The SD card driver needs to disable the pull-up resistors (or its power rail) when disabling SD_1_PWR_EN.

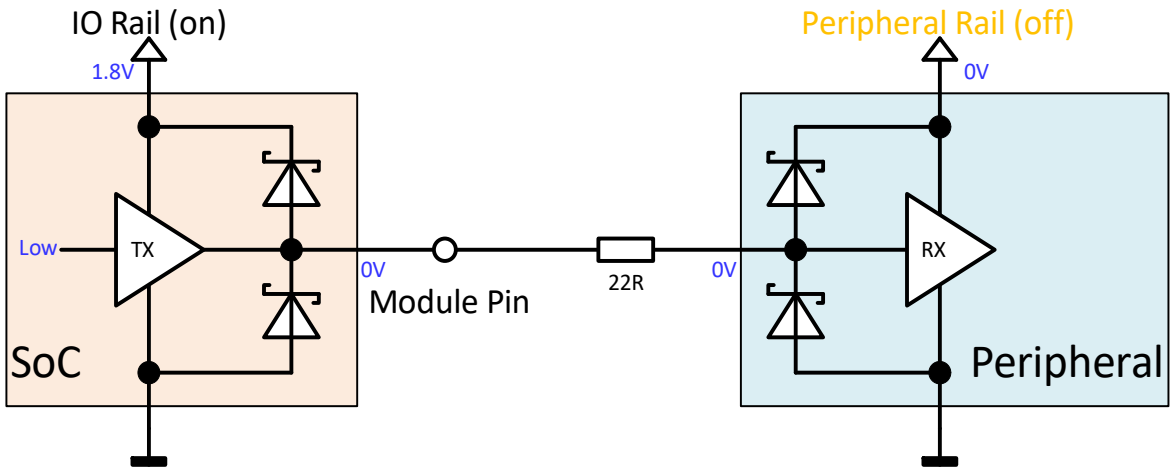


Figure 74: Make sure outputs are not driven high

3.5.5.3 Inputs without Backfeeding Path

Certain interfaces have different input circuits that are not prone to backfeeding or are having backfeeding prevention built-in. Some interfaces use a different ESD protection approach and therefore do not offer a backfeeding path. An example of an interface with built-in backfeeding prevention is the USB interface of the Verdin module. The USB cable can be connected to a powered peripheral or host device, even if the Verdin module is powered off. In this situation, the USB_1_VBUS can carry 5V, or the USB 2.0 data signals could be pulled up to 3.3V. The Verdin module already prevents backfeeding over the USB_1_VBUS and the USB data signals. Therefore, no further backfeeding prevention is required for these signals on the carrier board.

Whenever you are selecting peripheral devices, it is advised to check whether the input pins of the device have any built-in protection again backfeeding. Using such a device can eliminate complicated external circuits required for backfeeding prevention.

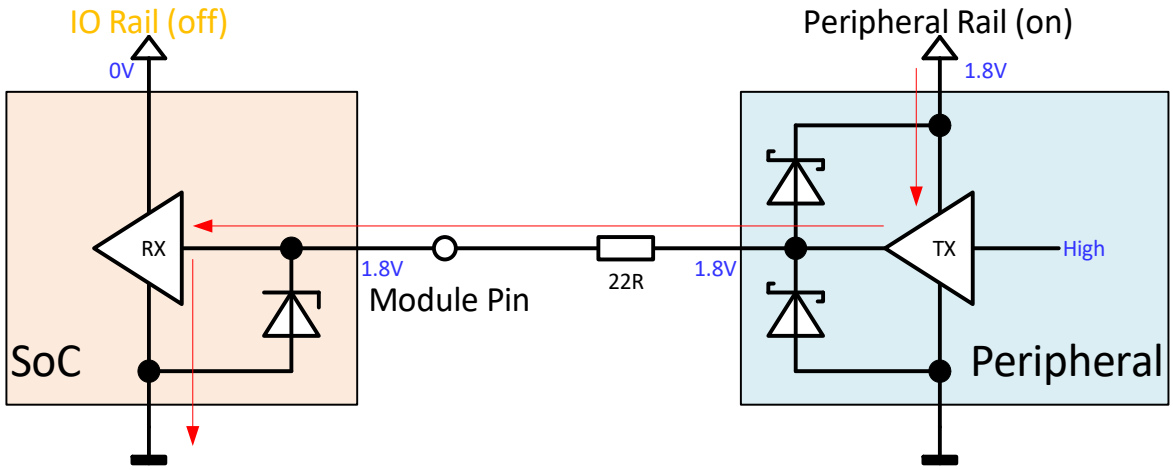


Figure 75: Input without backfeeding path

3.5.5.4 Series Resistor

For low-speed signals, a simple and cost-effective method can be using a higher value series resistor. Of course, this only works if the input impedance is big enough and the parasitic capacity is small enough (in order not to degrade the signal quality). The series resistor does not eliminate backfeeding entirely, but it limits the current and, therefore, also the residual voltage.

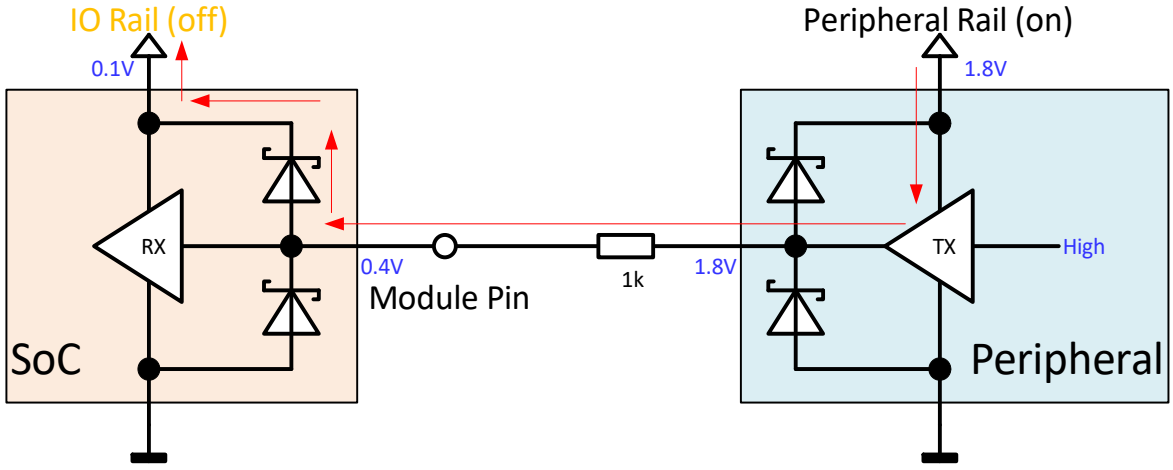


Figure 76: Series resistor for limiting backfeeding

3.5.5.5 Open Drain Signals

When using open-drain signals, it is crucial to use the correct voltage domain for the pull-up resistor. In Figure 67, the peripheral rail is used, and therefore backfeeding occurs. By using the same voltage domain for the pull-up resistor as the input side, backfeeding is eliminated. When using a computer module, using the IO rail might not be feasible. However, the Verdin module features the PWR_1V8_MOCI voltage output, which is in the same power domain as the IO rail. Therefore, it is recommended to use this PWR_1V8_MOCI for open-drain pull-up resistors.

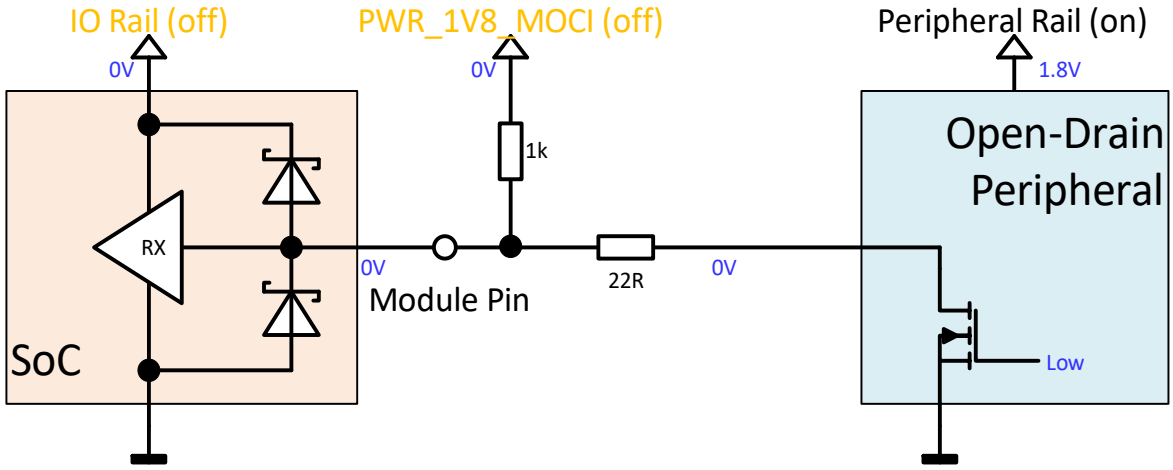


Figure 77: Correct pull-up rail for open-drain signals

3.5.5.6 Simple FET Circuit for Open-Drain Signals

Sometimes, it is impossible to move the pull-up resistor to the IO rail domain since there is already a pull-up resistor on the peripheral rail. Maybe this pull-up resistor is inside the peripheral device and cannot be switched off. The simple FET circuit in Figure 78 can offer a solution for blocking backfeeding. This circuit also works for bidirectional open-drain signals such as I^2C and can be used as a low-cost level shifter.

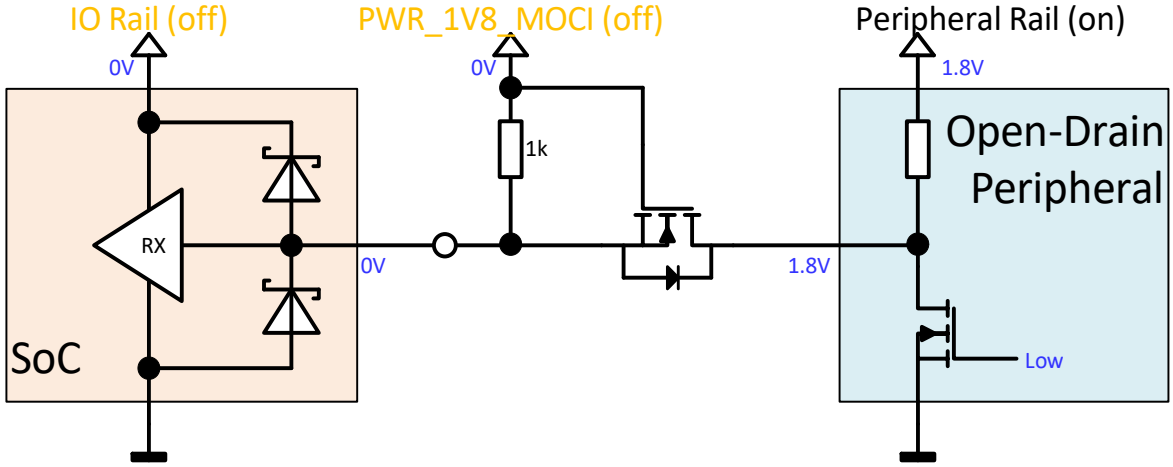


Figure 78: Simple FET circuit for open-drain signals

3.5.5.7 Blocking Diode

Another solution for low-speed signals is to use a diode and a pull-up resistor for blocking backfeeding. The pull-up resistor must be on the same voltage domain as the IO rail of the input side. Most SoC GPIO pins have configurable internal pull-up resistors. This can eliminate the need for an external resistor. The advantage of the internal resistor is that it is using the correct IO rail. The biggest drawback of this solution is that the low level of the signal is increased. Therefore, using a Schottky diode is recommended due to the smaller forward voltage drop. Make sure the specified maximum low level of the input pin is not violated.

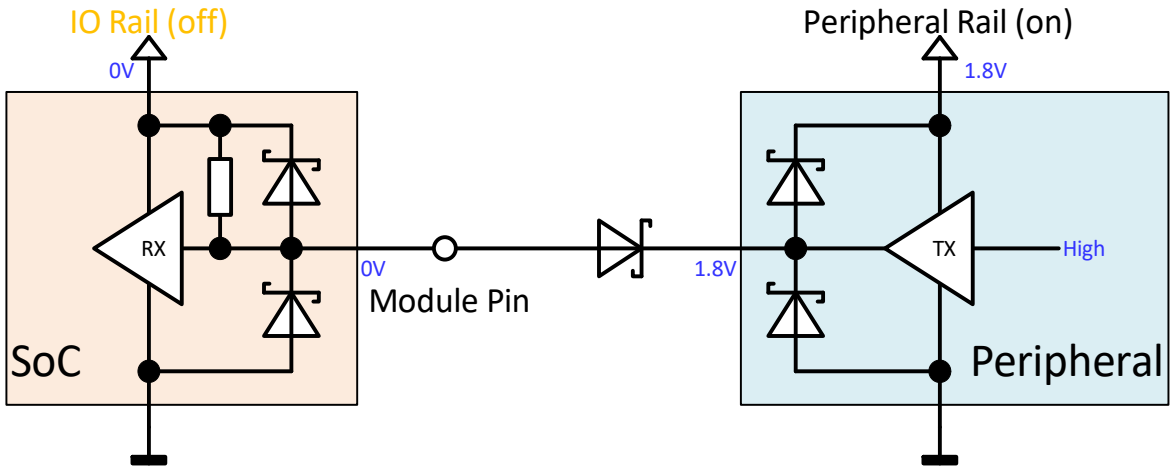


Figure 79: Diode circuit for backfeeding prevention with an on-chip pull-up resistor

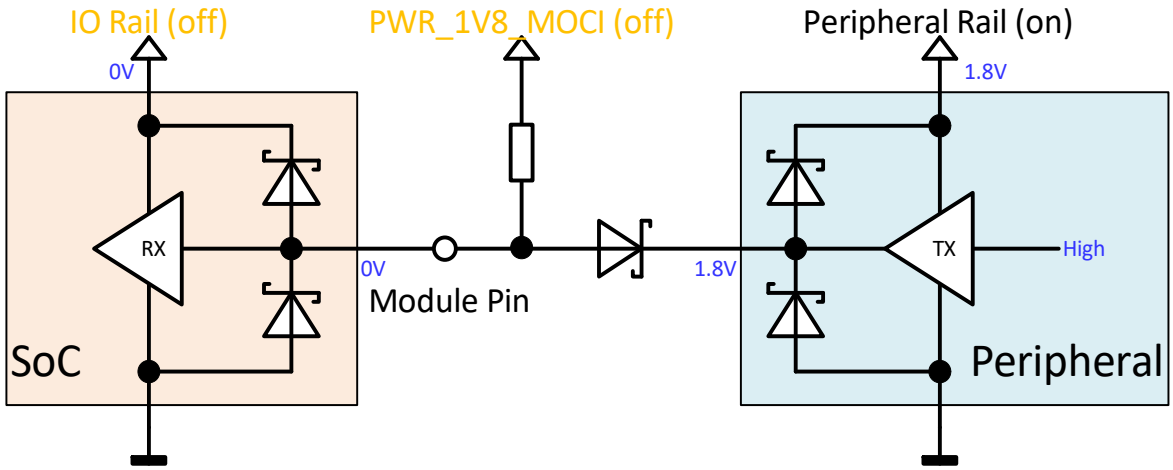


Figure 80: Diode circuit for backfeeding prevention with an external pull-up resistor

3.5.5.8 Capacitive Coupling

Some high-speed signals allow (or require) capacitive coupling. Capacitive coupling blocks all DC current and eliminates backfeeding caused by a DC offset of high-speed signals. Most high-speed interfaces and differential clocks (e.g., LVPECL, CML) use capacitive coupling nowadays. Typical signals using capacitive coupling are PCIe, SATA, DisplayPort, and the SuperSpeed signals of USB. Some of these signals are featuring the coupling capacitors already on the Verdin module. Please read the interface guidelines in section 2 of this document carefully for understanding whether coupling capacitors are required on the carrier board or not.

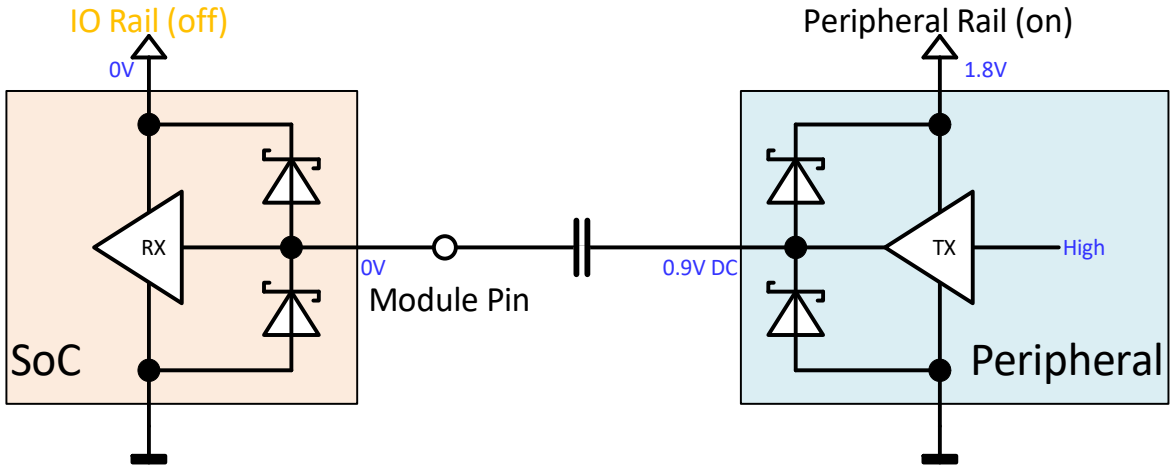


Figure 81: Capacitive coupled signals

3.5.5.9 Non-Backfeeding Buffer

Placing an additional buffer in the signal path can prevent backfeeding. The buffer needs to be powered from the same domain as the rail of the input. If the Verdin module is the signal input, using the PWR_1V8_MOCI as the buffer's power supply is the right approach (if the PWR_1V8_MOCI can provide enough current). Noteworthy, the buffer should not have an ESD protection circuit at its input that allows for backfeeding. Otherwise, the signal would back feed to the PWR_1V8_MOCI, and the whole circuit would lose its purpose.

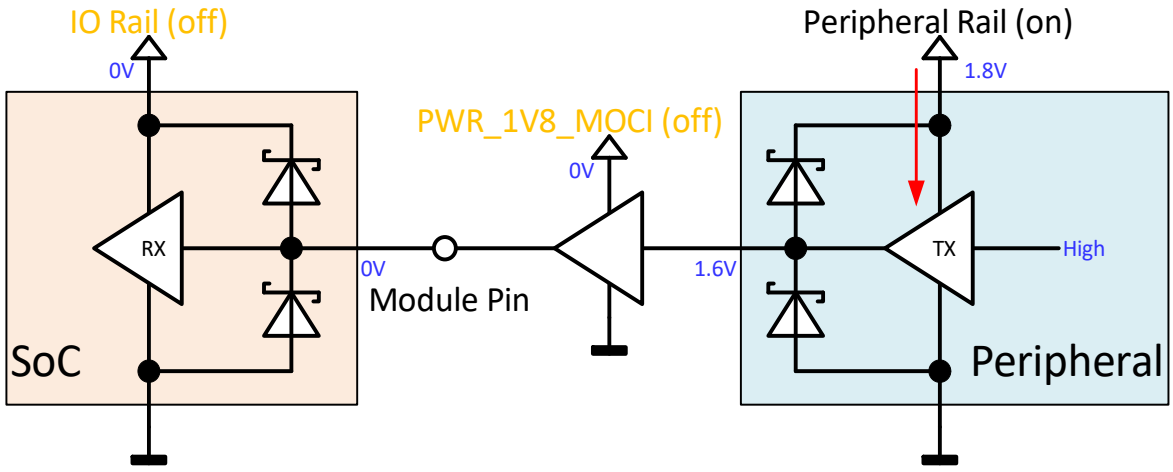


Figure 82: Non-backfeeding buffer

3.5.5.10 Dual-FET circuit

For low-speed signals, two transistors and two resistors can be used for blocking backfeeding. The first transistor is inverting the signal, while the second one makes it an open-drain type. Make sure the pull-up resistors are on the input IO rail. Instead of using two transistors, it might be possible to invert the signal in software and use only a single FET.

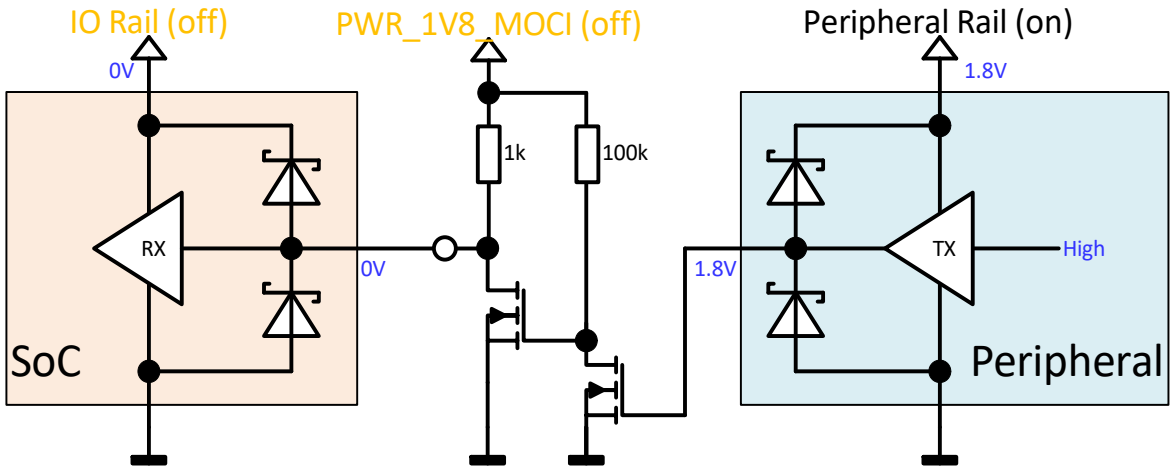


Figure 83: Dual-FET circuit

3.5.5.11 Tristate Buffer

Tristate buffers that feature an output enable control signal can be a solution. For example, RS232 transceivers often feature an output enable signal. The biggest challenge with this solution is to control the output enable signal. Often you cannot directly use the IO rail or the PWR_1V8_MOCI as an output enable signal. If there is backfeeding to the power rail used as the output enable signal, the buffers might never turn off, and therefore the backfeeding remains. Likely another circuit is required for generating a proper output enable signal.

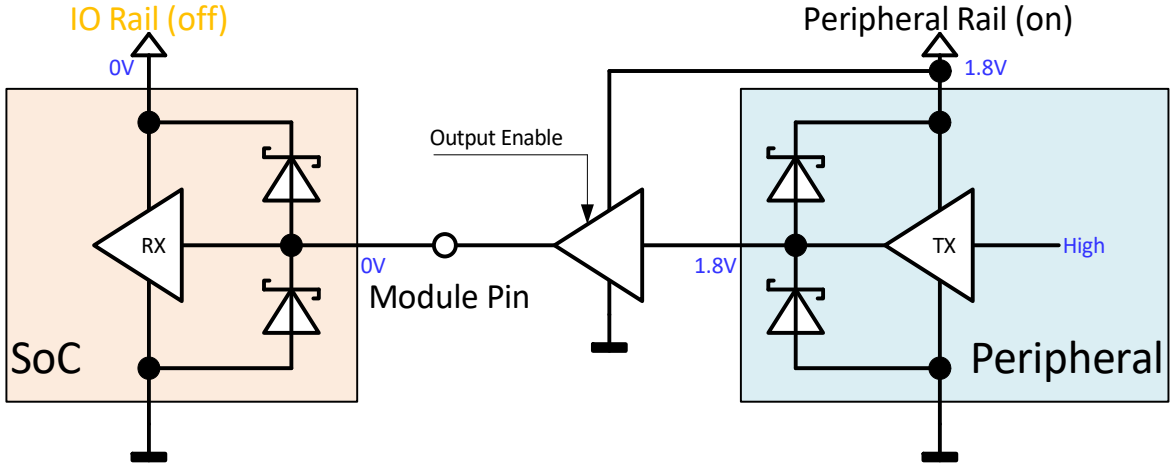


Figure 84: Tristate buffer

3.5.5.12 Level Shifter

Level shifters can be an effective method for preventing backfeeding. Especially if you anyway need a level shifter in the signal path. Even if both sides have the same IO voltage level, a level shifter can still be a good option. It is crucial to select a level shifter that allows both power rails to be switched off individually. Not all level shifters allow that without causing backfeeding. A good candidate for preventing backfeeding is the SN74AVC4T774 from TI. For open-drain signals such as the I²C bus, the FXMA2102L8X from ON Semiconductor prevents backfeeding.

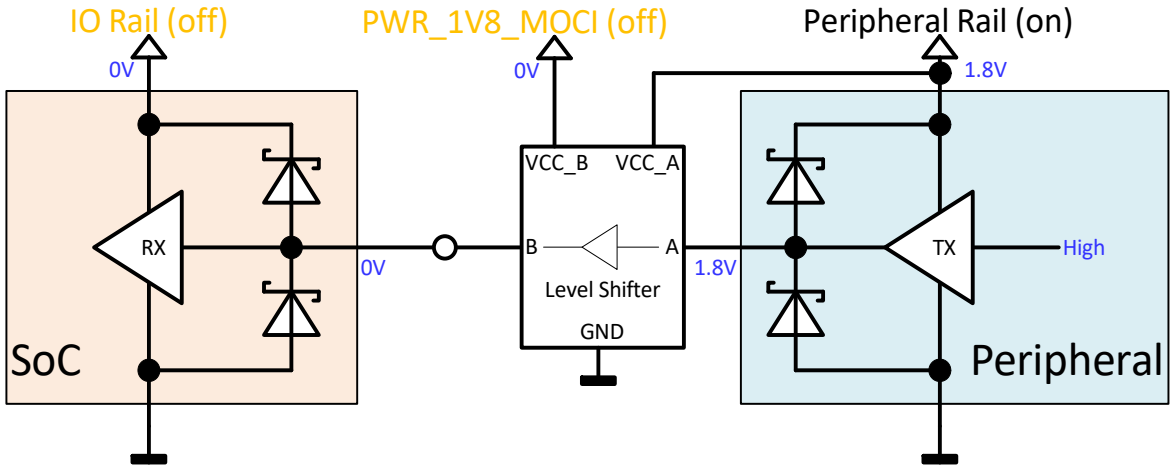


Figure 85: Level shifter for preventing backfeeding

3.5.5.13 Galvanic Isolation

Galvanic isolations in the signal path can be achieved by transformers, optocouplers, or specialized ICs. Especially in harsh environments, galvanic isolation is a preferred method for isolating power domains of different devices. The so-called magnetics inside the Ethernet connector is also a galvanic isolator and prevents backfeeding over the Ethernet cable. Galvanic isolators are also preferred way for protecting different power domains of CAN interfaces.

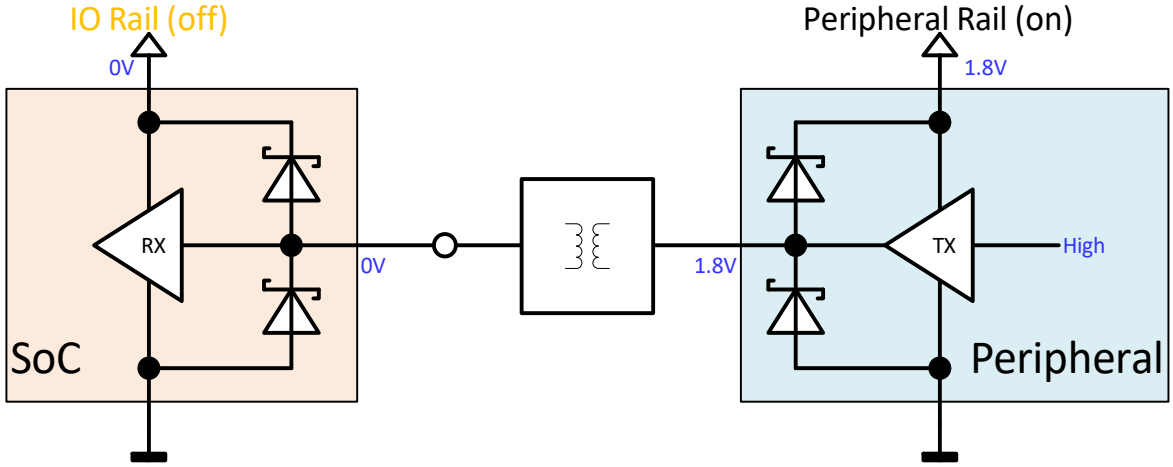


Figure 86: Galvanic isolation between input and output

3.5.5.14 Reverse Current Protection in IO Rail

By placing a diode in the IO rail's power supply, reverse current to other IO rail devices can be prevented. For example, this is a preferred solution for protecting the HDMI CEC signal from backfeeding to the 3.3V rail. However, it is not always a feasible solution due to the forward voltage drop on the IO voltage rail.

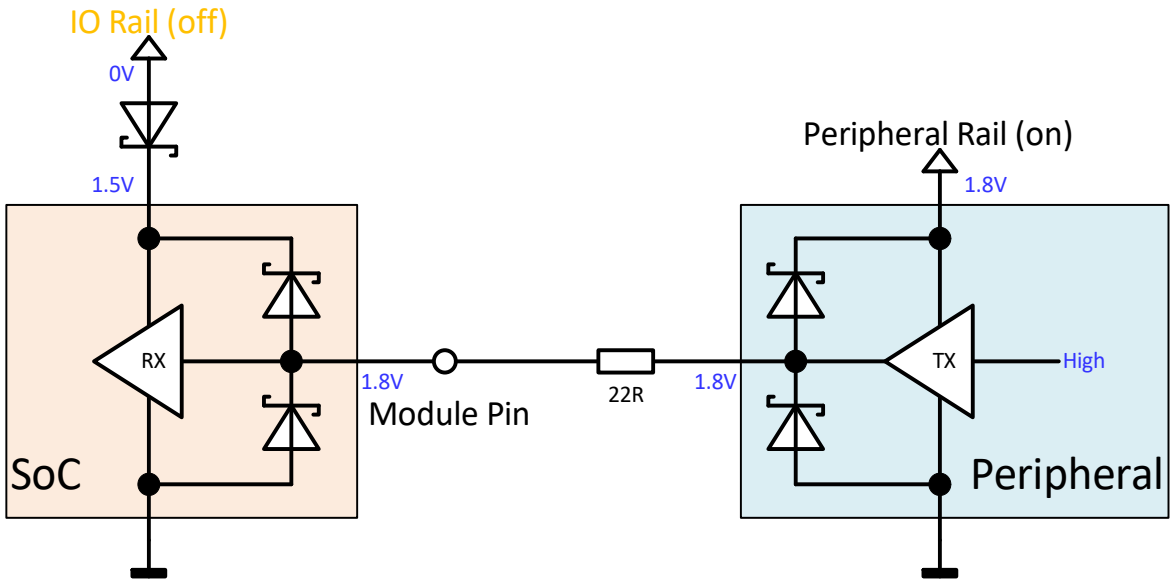


Figure 87: Reverse current protection diode

3.5.5.15 Extra Load on Rail

Suppose the primary issue caused by the residual voltage is an above-threshold voltage compromising the power-on reset or an incorrect device configuration strapped. In that case, a solution might be adding an extra load to the affected rail. Turning this load on only during the power-up sequence is advisable for reducing the extra power consumption. Before implementing this approach, make sure the extra load is not overloading the output driver or the ESD protection diode. Often this method is used in conjunction with other methods described before as an additional fallback solution. For example, the driver should drive output signals low to prevent backfeeding. If the driver fails to set the output signals correctly, the extra load can make sure that the peripheral's power-on reset is still triggering.

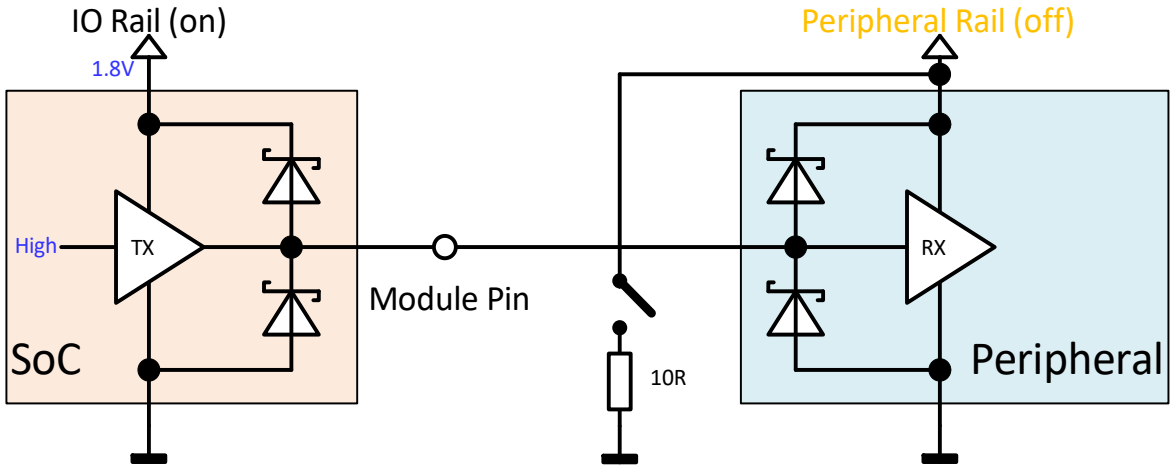


Figure 88: Additional load on the peripheral rail

4 Mechanical and Thermal Consideration

4.1 Module Dimensions

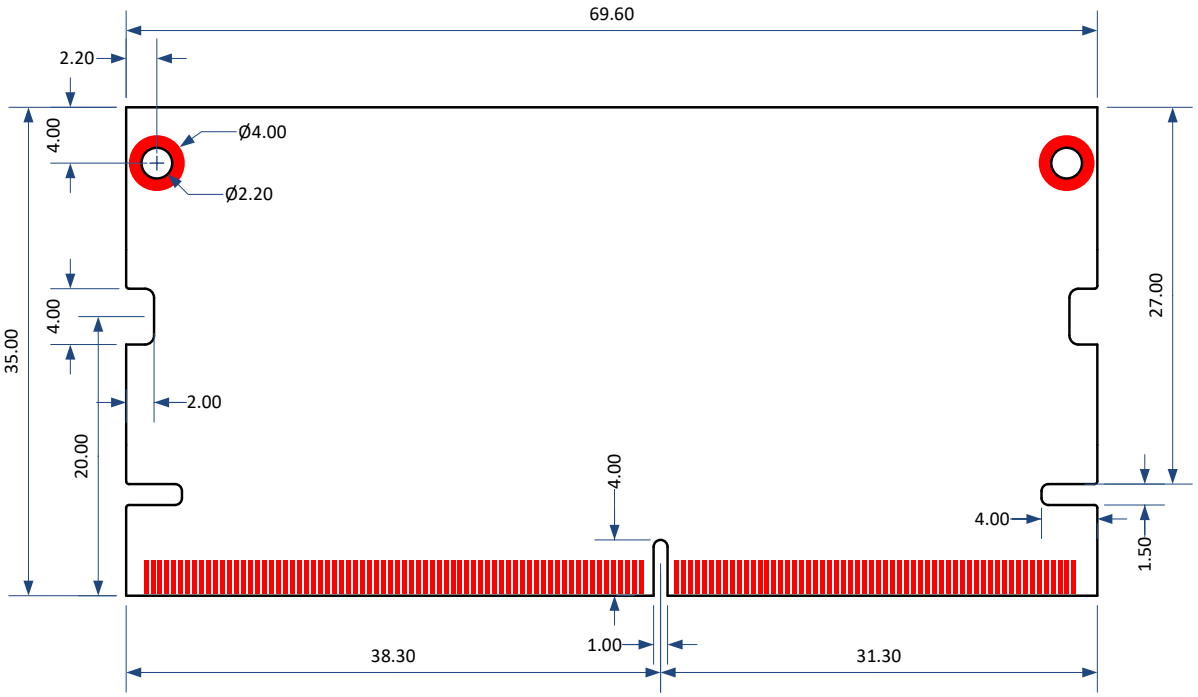


Figure 89: Module dimensions top side (mm)

On the bottom side of the Verdin module, there are 10 test pads (5 on each side). These pads are used by the module manufacturer for test purposes. On a custom carrier board, these test pads do not need to be connected.

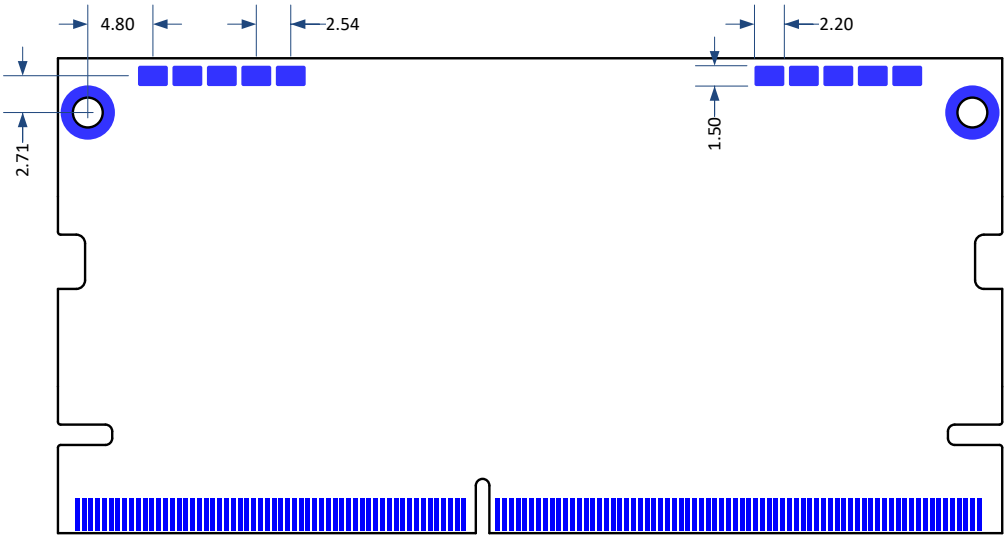


Figure 90: Module dimension bottom side (mm)

4.2 Module Connector and Stacking Height

The Verdin module uses the SODIMM DDR4 memory module edge connector. This connector has 260 pins with a 0.5mm pitch. Suitable connectors are available from different manufacturers in various board-to-board stacking heights. Manufacturers such as Amphenol or TE Connectivity use the term stacking height for the connector's overall height. This is not the actual distance between the module and the carrier board, as the board-to-board connectors. Amphenol and TE Connectivity provide four different connector heights from 4mm to 9.2mm.

The following table compares the different options. The connector height is the total height of the connector that can also be found in the name of the connector. The board-to-board distance is the nominal space between the carrier board and the module. Please note that in worst-case situations, this distance can be smaller. The column "Component Height Carrier Board" indicates the recommended maximum height of components underneath the module. Close to the SODIMM connector, there is an area that allows for higher components such as decoupling capacitors or series resistors to be placed. The maximum height in this area is listed in the column "Component Height Carrier Board (next to connector)".

Connector Height	Board-to-board distance	Component Height Carrier Board	Component Height Carrier Board (next to connector)	Remarks
4 mm	1.52 mm			Connector not suitable for Verdin modules due to the too-small board-to-board distance
5.2 mm	2.62 mm	0 mm	0.8 mm	Recommended stacking height for Verdin modules
8 mm	5.42 mm	2.8 mm	3.6 mm	
9.2 mm	6.62 mm	4 mm	4.8 mm	

Table 39: SODIMM Connector Stacking Height

There are also reverse angle connectors available. These connectors are not recommended for modules that require a cooling solution. Toradex recommends using the TE Connectivity 2309409-2 which has a connector height of 5.2mm that provides a board-to-board distance of 2.62mm.

The Verdin module does not follow the JEDEC specifications, which allow only a maximum of 1.2 mm for components on the top and bottom side of the module. The components on the top side of the Verdin module are limited to 3.0 mm in height. In contrast, the absolute maximum height for components placed on the bottom side is limited to 2.0 mm, except for an area next to the edge connector in which the module components are limited to 1.2 mm height. This allows for an extra 0.8 mm for decoupling capacitors and series resistors on the carrier board.

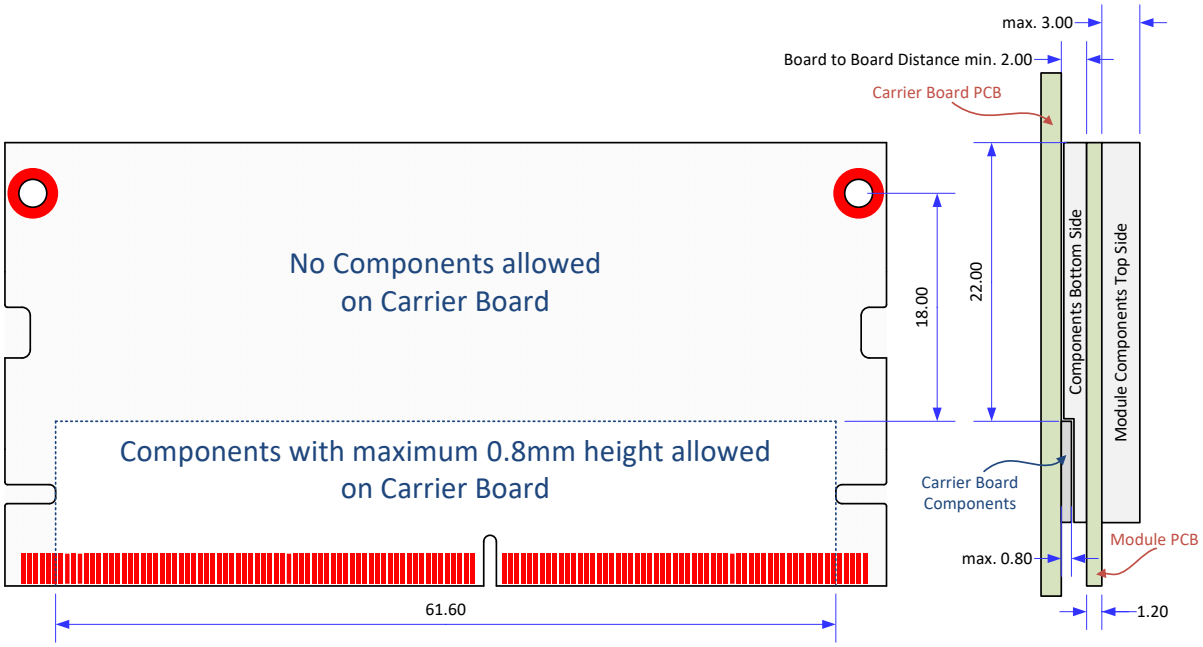


Figure 91: Maximum Component Height with a 5.2 mm SODIMM Connector

Even though a SODIMM with 5.2 mm height provides a nominal board-to-board distance of 2.62 mm, it is not recommended to place any components underneath the module (except for those next to the edge connector). The clip mechanism of the SODIMM connector is not rigid. This means that upon inserting the module, the module can be pushed a bit further down in the carrier board's direction. With the additional tolerances of the connector and the module PCB thickness, there is no space left for components on the carrier board.

Even if a module does not use up all the component height allowance, it is advisable not to squeeze in additional components between the module and the carrier board. Reserving the complete component height to the module guarantees mechanical compatibility with existing and future Verdin modules and module versions. If components need to be placed underneath the module, a connector with a larger stacking height is recommended.

4.3 Fixation of the Module

The SODIMM DDR4 connector comes with an integrated clip mechanism for a fast, secure, and convenient module fixation. For many applications, this fixation is enough. However, if the module is used in a harsh environment where higher vibration and shock tolerance/resistance is required, the module can be screwed down to the carrier board. Screwing down the module is also advisable if heavier heatsinks are mounted directly to the module. There are two mounting holes at the edge of the module designed to be used with M2 screws.

On Toradex carrier boards, there are two standoffs below the longer edge (further from the SODIMM DDR4 connector) of the SoM (S1 and S2 in Figure 92). These are used for providing a more robust fixation of Verdin modules to carrier boards and are only 2 mm tall. This allows for easier insertion of modules and an improved mounting experience. However, for a final product, it is recommended to use 2.5 mm standoffs for S1 and S2, especially if a heatsink will also be mounted to those spacers. This provides a less convenient mounting experience but ensures the parallel alignment of the module and the carrier board PCBs.

4.4 Thermal Solution

4.4.1 Verdin Industrial Heatsink

There are four standoffs required for mounting the Verdin Industrial Heatsink (S1, S2, S3, and S4 in Figure 92). The two standoffs underneath the module (S1 and S2) need to have a height of 2.5 mm. The two additional standoffs next to the SODIMM DDR4 connector (S3 and S4) need to be 7.0 mm tall.

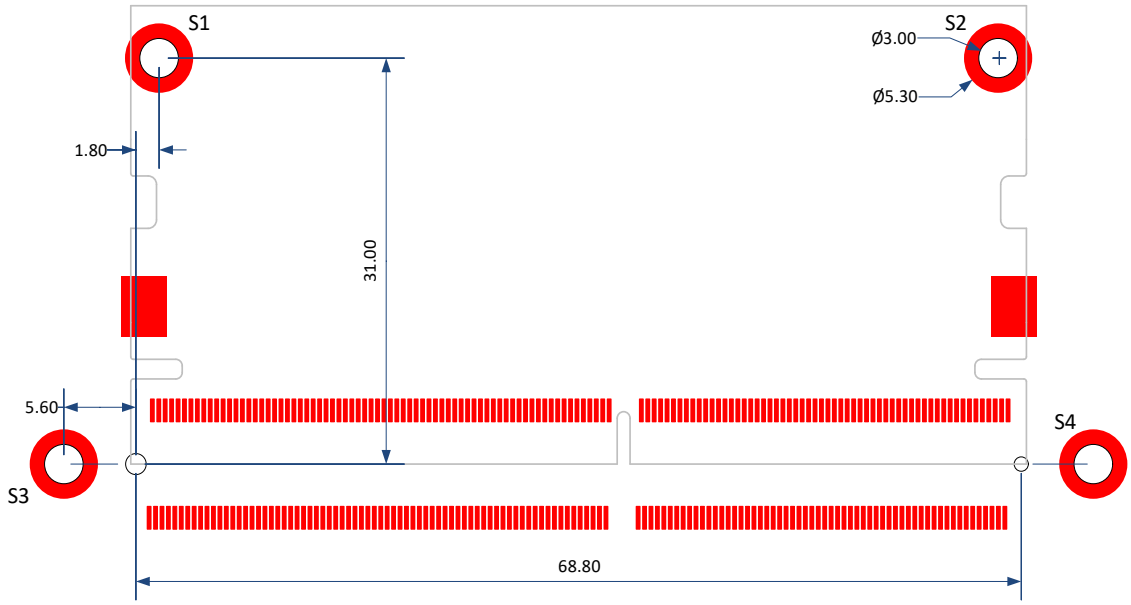


Figure 92: Standoff Locations (mm)

4.4.2 Verdin Clip-on Heatsink

TBA

4.5 Connector and Standoff Land Pattern Requirements

The required land pattern depends on the need for additional standoffs. All of the standoffs are optional. Either no standoffs, only the two at the long edge of the module further from the SODIMM DDR4 connector (S1 and S2), or all four (S1, S2, S3, and S4) are acceptable. The standoffs S1 and S2 are used for additional fixation of the module (see section 4.3). For these, it is recommended to use M2x0.4 standoffs with a height of 2.5 mm. For mounting the optional Verdin Industrial Heatsink, two additional M2x0.4 standoffs (S3 and S4) are required. The height of these standoffs needs to be 7.0 mm.

The land pattern below is optimized for the TE Connectivity 2309409-2 SODIMM DDR4 connector. If a different connector is used, please check the land pattern recommendations of the connector manufacturer. Please adjust the heights of the standoffs accordingly.

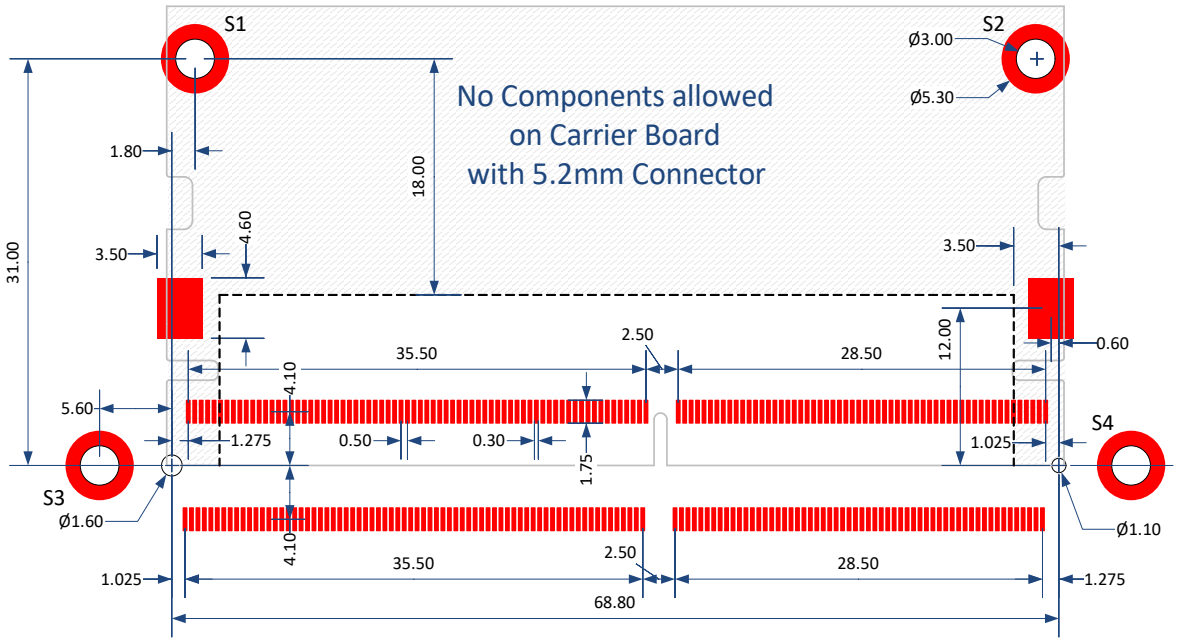


Figure 93: Carrier Board Land Pattern (mm)

4.6 Carrier Board Space Requirements

The required PCB area for the module depends on the module fixing method and the cooling solution.

5 Appendix A – Module Top Side Signal Definition

Pin Number	Signal Group	Signal Name	Signal Type	Feature Group
1	JTAG	JTAG_1_TDI	Input (VREF level)	"Reserved"
3		JTAG_1_TRST#	Input (VREF level)	"Reserved"
5		JTAG_1_TDO	Output (VREF level)	"Reserved"
7		JTAG_1_VREF	Reference Output	"Reserved"
9		JTAG_1_TCK	Input (VREF level)	"Reserved"
11		GND		
13		JTAG_1_TMS	Input (VREF level)	"Reserved"
15	PWM	PWM_1	Output 1.8V	"Always Compatible"
17	DSI	GPIO_9_DSI	Bidirectional 1.8V	"Reserved"
19		PWM_3_DSI	Output 1.8V	"Reserved"
21		GPIO_10_DSI	Bidirectional 1.8V	"Reserved"
23		DSI_1_D3_N	Differential Pair Output	"Reserved"
25		DSI_1_D3_P	Differential Pair Output	"Reserved"
27		GND		
29		DSI_1_D2_N	Differential Pair Output	"Reserved"
31		DSI_1_D2_P	Differential Pair Output	"Reserved"
33		GND		
35		DSI_1_CLK_N	Differential Pair Output	"Reserved"
37		DSI_1_CLK_P	Differential Pair Output	"Reserved"
39		GND		
41		DSI_1_D1_N	Differential Pair Output	"Reserved"
43		DSI_1_D1_P	Differential Pair Output	"Reserved"
45		GND		
47		DSI_1_D0_N	Differential Pair Bidirectional	"Reserved"
49		DSI_1_D0_P	Differential Pair Bidirectional	"Reserved"
51		GND		
53		I2C_2_DSI_SDA	Open Drain 1.8V	"Reserved"
55		I2C_2_DSI_SCL	Open Drain 1.8V	"Reserved"
57	HDMI	I2C_3_HDMI_SDA	Open Drain 1.8V	"Reserved"
59		I2C_3_HDMI_SCL	Open Drain 1.8V	"Reserved"
61		HDMI_1_HPD	Input 1.8V	"Reserved"
63		HDMI_1_CEC	Bidirectional 1.8V	"Reserved"
65		GND		
67		HDMI_1_TXC_N	Differential Pair Output	"Reserved"
69		HDMI_1_TXC_P	Differential Pair Output	"Reserved"
71		GND		
73		HDMI_1_TXD0_N	Differential Pair Output	"Reserved"
75		HDMI_1_TXD0_P	Differential Pair Output	"Reserved"
77		GND		
79		HDMI_1_TXD1_N	Differential Pair Output	"Reserved"
81		HDMI_1_TXD1_P	Differential Pair Output	"Reserved"

83		GND		
85		HDMI_1_TXD2_N	Differential Pair Output	"Reserved"
87		HDMI_1_TXD2_P	Differential Pair Output	"Reserved"
89	CSI	GND		
91		CSI_1_MCLK	Output 1.8V	"Reserved"
93		I2C_4_CSI_SDA	Open Drain 1.8V	"Reserved"
95		I2C_4_CSI_SCL	Open Drain 1.8V	"Reserved"
97		GND		
99		CSI_1_D3_P	Differential Pair Input	"Reserved"
101		CSI_1_D3_N	Differential Pair Input	"Reserved"
103		GND		
105		CSI_1_D2_P	Differential Pair Input	"Reserved"
107		CSI_1_D2_N	Differential Pair Input	"Reserved"
109		GND		
111		CSI_1_CLK_P	Differential Pair Input	"Reserved"
113		CSI_1_CLK_N	Differential Pair Input	"Reserved"
115		GND		
117		CSI_1_D1_P	Differential Pair Input	"Reserved"
119		CSI_1_D1_N	Differential Pair Input	"Reserved"
121		GND		
123		CSI_1_D0_P	Differential Pair Bidirectional	"Reserved"
125		CSI_1_D0_N	Differential Pair Bidirectional	"Reserved"
127		GND		
129	UART	UART_1_RXD	Input 1.8V	"Always Compatible"
131		UART_1_TXD	Output 1.8V	"Always Compatible"
133		UART_1_RTS	Output 1.8V	"Reserved"
135		UART_1_CTS	Input 1.8V	"Reserved"
137		UART_2_RXD	Input 1.8V	"Always Compatible"
139		UART_2_TXD	Output 1.8V	"Always Compatible"
141		UART_2_RTS	Output 1.8V	"Reserved"
143		UART_2_CTS	Input 1.8V	"Reserved"
Notch				
145	DEBUG UART	GND		
147		UART_3_RXD	Input 1.8V	"Always Compatible"
149		UART_3_TXD	Output 1.8V	"Always Compatible"
151		UART_4_RXD	Input 1.8V	"Reserved"
153		UART_4_TXD	Output 1.8V	"Reserved"
155	USB	USB_1_EN	Output 1.8V	"Always Compatible"
157		USB_1_OC#	Input 1.8V	"Always Compatible"
159		USB_1_VBUS	Input 5V Tolerant	"Always Compatible"
161		USB_1_ID	Input 1.8V	"Always Compatible"
163		USB_1_D_N	Differential Pair Bidirectional	"Always Compatible"
165		USB_1_D_P	Differential Pair Bidirectional	"Always Compatible"
167		GND		

169		USB_2_SSTX_N	Differential Pair Output	"Reserved"
171		USB_2_SSTX_P	Differential Pair Output	"Reserved"
173		GND		
175		USB_2_SSRX_N	Differential Pair Input	"Reserved"
177		USB_2_SSRX_P	Differential Pair Input	"Reserved"
179		GND		
181		USB_2_D_N	Differential Pair Bidirectional	"Always Compatible"
183		USB_2_D_P	Differential Pair Bidirectional	"Always Compatible"
185		USB_2_EN	Output 1.8V	"Always Compatible"
187		USB_2_OC#	Input 1.8V	"Always Compatible"
189	RGMII	ETH_2_RGMII_INT#	Input 1.8V	"Reserved"
191		ETH_2_RGMII_MDIO	Bidirectional 1.8V	"Reserved"
193		ETH_2_RGMII_MDC	Output 1.8V	"Reserved"
195		GND		
197		ETH_2_RGMII_RXC	Input 1.8V	"Reserved"
199		ETH_2_RGMII_RX_CTL	Input 1.8V	"Reserved"
201		ETH_2_RGMII_RXD_0	Input 1.8V	"Reserved"
203		ETH_2_RGMII_RXD_1	Input 1.8V	"Reserved"
205		ETH_2_RGMII_RXD_2	Input 1.8V	"Reserved"
207		ETH_2_RGMII_RXD_3	Input 1.8V	"Reserved"
209		GND		
211		ETH_2_RGMII_TX_CTL	Output 1.8V	"Reserved"
213		ETH_2_RGMII_TXC	Output 1.8V	"Reserved"
215		ETH_2_RGMII_TXD_3	Output 1.8V	"Reserved"
217		ETH_2_RGMII_TXD_2	Output 1.8V	"Reserved"
219		ETH_2_RGMII_TXD_1	Output 1.8V	"Reserved"
221		ETH_2_RGMII_TXD_0	Output 1.8V	"Reserved"
223	Gigabit Ethernet	GND		
225		ETH_1_MDI0_P	Differential Pair Bidirectional	"Always Compatible"
227		ETH_1_MDI0_N	Differential Pair Bidirectional	"Always Compatible"
229		GND		
231		ETH_1_MDI1_N	Differential Pair Bidirectional	"Always Compatible"
233		ETH_1_MDI1_P	Differential Pair Bidirectional	"Always Compatible"
235		ETH_1_LED_1	Open-Drain Output, 3.3V Tolerant	"Always Compatible"
237		ETH_1_LED_2	Open-Drain Output, 3.3V Tolerant	"Always Compatible"
239		ETH_1_MDI2_P	Differential Pair Bidirectional	"Always Compatible"
241		ETH_1_MDI2_N	Differential Pair Bidirectional	"Always Compatible"
243		GND		
245		ETH_1_MDI3_N	Differential Pair Bidirectional	"Always Compatible"
247		ETH_1_MDI3_P	Differential Pair Bidirectional	"Always Compatible"
249	Power	VCC_BACKUP	Power Input 3.6V Max	"Always Compatible"
251		VCC	Power Input 3.135 – 5.5V	"Always Compatible"
253		VCC	Power Input 3.135 – 5.5V	"Always Compatible"
255		VCC	Power Input 3.135 – 5.5V	"Always Compatible"

257		VCC	Power Input 3.135 – 5.5V	"Always Compatible"
259		VCC	Power Input 3.135 – 5.5V	"Always Compatible"

6 Appendix B – Module Bottom Side Signal Definition

Pin Number	Signal Group	Signal Name	Signal Type	Feature Group
2	ADC	ADC_1	Analog Input 1.8V	"Reserved"
4		ADC_2	Analog Input 1.8V	"Reserved"
6		ADC_3	Analog Input 1.8V	"Reserved"
8		ADC_4	Analog Input 1.8V	"Reserved"
10		GND		
12	I2C	I2C_1_SDA	Open Drain 1.8V	"Always Compatible"
14		I2C_1_SCL	Open Drain 1.8V	"Always Compatible"
16	PWM	PWM_2	Output 1.8V	"Reserved"
18	CAN	GND		
20		CAN_1_TX	Output 1.8V	"Reserved"
22		CAN_1_RX	Input 1.8V	"Reserved"
24		CAN_2_TX	Output 1.8V	"Reserved"
26		CAN_2_RX	Input 1.8V	"Reserved"
28	I2S	GND		
30		I2S_1_BCLK	Bidirectional 1.8V	"Reserved"
32		I2S_1_SYNC	Bidirectional 1.8V	"Reserved"
34		I2S_1_D_OUT	Output 1.8V	"Reserved"
36		I2S_1_D_IN	Input 1.8V	"Reserved"
38		I2S_1_MCLK	Output 1.8V	"Reserved"
40		GND		
42		I2S_2_BCLK	Bidirectional 1.8V	"Reserved"
44		I2S_2_SYNC	Bidirectional 1.8V	"Reserved"
46		I2S_2_D_OUT	Output 1.8V	"Reserved"
48		I2S_2_D_IN	Input 1.8V	"Reserved"
50	QSPI	GND		
52		QSPI_1_CLK	Output 1.8V	"Reserved"
54		QSPI_1_CS#	Output 1.8V	"Reserved"
56		QSPI_1_IO0	Bidirectional 1.8V	"Reserved"
58		QSPI_1_IO1	Bidirectional 1.8V	"Reserved"
60		QSPI_1_IO2	Bidirectional 1.8V	"Reserved"
62		QSPI_1_IO3	Bidirectional 1.8V	"Reserved"
64		QSPI_1_CS2#	Output 1.8V	"Reserved"
66		QSPI_1_DQS	Output 1.8V	"Reserved"
68	SDIO	GND		
70		SD_1_D2	Bidirectional 3.3V/1.8V	"Always Compatible"
72		SD_1_D3	Bidirectional 3.3V/1.8V	"Always Compatible"
74		SD_1_CMD	Bidirectional 3.3V/1.8V	"Always Compatible"
76		SD_1_PWR_EN	Output 3.3V/1.8V	"Always Compatible"
78		SD_1_CLK	Output 3.3V/1.8V	"Always Compatible"
80		SD_1_D0	Bidirectional 3.3V/1.8V	"Always Compatible"
82		SD_1_D1	Bidirectional 3.3V/1.8V	"Always Compatible"

84		SD_1_CD#	Input 3.3V/1.8V	"Always Compatible"
86	"Module-specific"	GND		
88		MSP_1	Differential Pair/ Single Ended	"Module-specific"
90		MSP_2	Differential Pair/ Single Ended	"Module-specific"
92		MSP_3	GND/ Low Speed/ Single Ended	"Module-specific"
94		MSP_4	Differential Pair/ Single Ended	"Module-specific"
96		MSP_5	Differential Pair/ Single Ended	"Module-specific"
98		GND		
100		MSP_6	Differential Pair/ Single Ended	"Module-specific"
102		MSP_7	Differential Pair/ Single Ended	"Module-specific"
104		MSP_8	GND/ Low Speed/ Single Ended	"Module-specific"
106		MSP_9	Differential Pair/ Single Ended	"Module-specific"
108		MSP_10	Differential Pair/ Single Ended	"Module-specific"
110		GND		
112		MSP_11	Differential Pair/ Single Ended	"Module-specific"
114		MSP_12	Differential Pair/ Single Ended	"Module-specific"
116		MSP_13	GND/ Low Speed/ Single Ended	"Module-specific"
118		MSP_14	Differential Pair/ Single Ended	"Module-specific"
120		MSP_15	Differential Pair/ Single Ended	"Module-specific"
122		GND		
124		MSP_16	Differential Pair/ Single Ended	"Module-specific"
126		MSP_17	Differential Pair/ Single Ended	"Module-specific"
128		MSP_18	GND/ Low Speed/ Single Ended	"Module-specific"
130		MSP_19	Differential Pair/ Single Ended	"Module-specific"
132		MSP_20	Differential Pair/ Single Ended	"Module-specific"
134		GND		
136		MSP_21	Differential Pair/ Single Ended	"Module-specific"
138		MSP_22	Differential Pair/ Single Ended	"Module-specific"
140		MSP_23	GND/ Low Speed/ Single Ended	"Module-specific"
142		MSP_24	Differential Pair/ Single Ended	"Module-specific"
144		MSP_25	Differential Pair/ Single Ended	"Module-specific"
Notch				
146	"Module-specific"	GND		
148		MSP_26	Differential Pair/ Single Ended	"Module-specific"
150		MSP_27	Differential Pair/ Single Ended	"Module-specific"
152		MSP_28	GND/ Low Speed/ Single Ended	"Module-specific"
154		MSP_29	Differential Pair/ Single Ended	"Module-specific"
156		MSP_30	Differential Pair/ Single Ended	"Module-specific"
158		GND		
160		MSP_31	Differential Pair/ Single Ended	"Module-specific"
162		MSP_32	Differential Pair/ Single Ended	"Module-specific"
164		MSP_33	GND/ Low Speed/ Single Ended	"Module-specific"
166		MSP_34	Differential Pair/ Single Ended	"Module-specific"
168		MSP_35	Differential Pair/ Single Ended	"Module-specific"

170		GND		
172		MSP_36	Differential Pair/ Single Ended	"Module-specific"
174		MSP_37	Differential Pair/ Single Ended	"Module-specific"
176		MSP_38	GND/ Low Speed/ Single Ended	"Module-specific"
178		MSP_39	Differential Pair/ Single Ended	"Module-specific"
180		MSP_40	Differential Pair/ Single Ended	"Module-specific"
182		GND		
184		MSP_41	Differential Pair/ Single Ended	"Module-specific"
186		MSP_42	Differential Pair/ Single Ended	"Module-specific"
188		MSP_43	GND/ Low Speed/ Single Ended	"Module-specific"
190		MSP_44	Differential Pair/ Single Ended	"Module-specific"
192		MSP_45	Differential Pair/ Single Ended	"Module-specific"
194	SPI	GND		
196		SPI_1_CLK	Output 1.8V	"Always Compatible"
198		SPI_1_MISO	Input 1.8V	"Always Compatible"
200		SPI_1_MOSI	Output 1.8V	"Always Compatible"
202		SPI_1_CS	Output 1.8V	"Always Compatible"
204	GPIO	GND		
206		GPIO_1	Bidirectional 1.8V	"Always Compatible"
208		GPIO_2	Bidirectional 1.8V	"Always Compatible"
210		GPIO_3	Bidirectional 1.8V	"Always Compatible"
212		GPIO_4	Bidirectional 1.8V	"Always Compatible"
214		PWR_1V8_MOCI	1.8V Output 250mA max.	"Always Compatible"
216		GPIO_5_CSI	Bidirectional 1.8V	"Always Compatible"
218		GPIO_6_CSI	Bidirectional 1.8V	"Always Compatible"
220		GPIO_7_CSI	Bidirectional 1.8V	"Always Compatible"
222		GPIO_8_CSI	Bidirectional 1.8V	"Always Compatible"
224	PCIe	GND		
226		PCIE_1_CLK_N	Differential Pair Output	"Reserved"
228		PCIE_1_CLK_P	Differential Pair Output	"Reserved"
230		GND		
232		PCIE_1_L0_RX_N	Differential Pair Input	"Reserved"
234		PCIE_1_L0_RX_P	Differential Pair Input	"Reserved"
236		GND		
238		PCIE_1_L0_TX_N	Differential Pair Output	"Reserved"
240		PCIE_1_L0_TX_P	Differential Pair Output	"Reserved"
242		GND		
244		PCIE_1_RESET#	Output 1.8V	"Reserved"
246	System Control	CTRL_RECOVERY_MICO#	Open-Drain Input 1.8V	"Always Compatible"
248		CTRL_PWR_BTN_MICO#	Open-Drain Input 1.8V	"Always Compatible"
250		CTRL_FORCE_OFF_MOCI#	Open-Drain Output, 5V Tolerant	"Always Compatible"
252		CTRL_WAKE1_MICO#	Input 1.8V	"Always Compatible"
254		CTRL_PWR_EN_MOCI	Output 1.8V	"Always Compatible"
256		CTRL_SLEEP_MOCI#	Output 1.8V	"Always Compatible"

258		CTRL_RESET_MOCI#	Open-Drain Output, 3.3V Tolerant	"Always Compatible"
260		CTRL_RESET_MICO#	Open-Drain Input 1.8V	"Always Compatible"

7 Appendix C - Physical Pin Definition and Location

Signal Group	Module Top Side	MXM3 Pins		Module Bottom Side	Signal Group
JTAG	JTAG_1_TDI	1	2	ADC_1	ADC
	JTAG_1_TRST#	3	4	ADC_2	
	JTAG_1_TDO	5	6	ADC_3	
	JTAG_1_VREF	7	8	ADC_4	
	JTAG_1_TCK	9	10	GND	
	GND	11	12	I2C_1_SDA	I2C
	JTAG_1_TMS	13	14	I2C_1_SCL	
PWM	PWM_1	15	16	PWM_2	PWM
DSI	GPIO_9_DSI	17	18	GND	CAN
	PWM_3_DSI	19	20	CAN_1_TX	
	GPIO_10_DSI	21	22	CAN_1_RX	
	DSI_1_D3_N	23	24	CAN_2_TX	
	DSI_1_D3_P	25	26	CAN_2_RX	
	GND	27	28	GND	I2S
	DSI_1_D2_N	29	30	I2S_1_BCLK	
	DSI_1_D2_P	31	32	I2S_1_SYNC	
	GND	33	34	I2S_1_D_OUT	
	DSI_1_CLK_N	35	36	I2S_1_D_IN	
	DSI_1_CLK_P	37	38	I2S_1_MCLK	
	GND	39	40	GND	
	DSI_1_D1_N	41	42	I2S_2_BCLK	
	DSI_1_D1_P	43	44	I2S_2_SYNC	
	GND	45	46	I2S_2_D_OUT	
	DSI_1_D0_N	47	48	I2S_2_D_IN	
	DSI_1_D0_P	49	50	GND	QSPI
	GND	51	52	QSPI_1_CLK	
	I2C_2_DSI_SDA	53	54	QSPI_1_CS#	
	I2C_2_DSI_SCL	55	56	QSPI_1_IO0	
HDMI	I2C_3_HDMI_SDA	57	58	QSPI_1_IO1	
	I2C_3_HDMI_SCL	59	60	QSPI_1_IO2	
	HDMI_1_HPD	61	62	QSPI_1_IO3	
	HDMI_1_CEC	63	64	QSPI_1_CS2#	
	GND	65	66	QSPI_1_DQS	
	HDMI_1_TXC_N	67	68	GND	SDIO
	HDMI_1_TXC_P	69	70	SD_1_D2	
	GND	71	72	SD_1_D3	
	HDMI_1_TXD0_N	73	74	SD_1_CMD	
	HDMI_1_TXD0_P	75	76	SD_1_PWR_EN	
	GND	77	78	SD_1_CLK	
	HDMI_1_TXD1_N	79	80	SD_1_D0	
	HDMI_1_TXD1_P	81	82	SD_1_D1	

	GND	83	84	SD_1_CD#	
	HDMI_1_TXD2_N	85	86	GND	"Module-specific"
	HDMI_1_TXD2_P	87	88	MSP_1	
CSI	GND	89	90	MSP_2	
	CSI_1_MCLK	91	92	MSP_3	
	I2C_4_CSI_SDA	93	94	MSP_4	
	I2C_4_CSI_SCL	95	96	MSP_5	
	GND	97	98	GND	
	CSI_1_D3_P	99	100	MSP_6	
	CSI_1_D3_N	101	102	MSP_7	
	GND	103	104	MSP_8	
	CSI_1_D2_P	105	106	MSP_9	
	CSI_1_D2_N	107	108	MSP_10	
	GND	109	110	GND	
	CSI_1_CLK_P	111	112	MSP_11	
	CSI_1_CLK_N	113	114	MSP_12	
	GND	115	116	MSP_13	
	CSI_1_D1_P	117	118	MSP_14	
	CSI_1_D1_N	119	120	MSP_15	
	GND	121	122	GND	
	CSI_1_D0_P	123	124	MSP_16	
	CSI_1_D0_N	125	126	MSP_17	
	GND	127	128	MSP_18	
UART	UART_1_RXD	129	130	MSP_19	
	UART_1_TXD	131	132	MSP_20	
	UART_1_RTS	133	134	GND	
	UART_1_CTS	135	136	MSP_21	
	UART_2_RXD	137	138	MSP_22	
	UART_2_TXD	139	140	MSP_23	
	UART_2_RTS	141	142	MSP_24	
	UART_2_CTS	143	144	MSP_25	
Notch					
DEBUG UART	GND	145	146	GND	"Module-specific"
	UART_3_RXD	147	148	MSP_26	
	UART_3_TXD	149	150	MSP_27	
	UART_4_RXD	151	152	MSP_28	
	UART_4_TXD	153	154	MSP_29	
USB	USB_1_EN	155	156	MSP_30	
	USB_1_OC#	157	158	GND	
	USB_1_VBUS	159	160	MSP_31	
	USB_1_ID	161	162	MSP_32	
	USB_1_D_N	163	164	MSP_33	
	USB_1_D_P	165	166	MSP_34	
	GND	167	168	MSP_35	

	USB_2_SSTX_N	169	170	GND	
	USB_2_SSTX_P	171	172	MSP_36	
	GND	173	174	MSP_37	
	USB_2_SSRX_N	175	176	MSP_38	
	USB_2_SSRX_P	177	178	MSP_39	
	GND	179	180	MSP_40	
	USB_2_D_N	181	182	GND	
	USB_2_D_P	183	184	MSP_41	
	USB_2_EN	185	186	MSP_42	
	USB_2_OC#	187	188	MSP_43	
RGMII	ETH_2_RGMII_INT#	189	190	MSP_44	
	ETH_2_RGMII_MDIO	191	192	MSP_45	
	ETH_2_RGMII_MDC	193	194	GND	SPI
	GND	195	196	SPI_1_CLK	
	ETH_2_RGMII_RXC	197	198	SPI_1_MISO	
	ETH_2_RGMII_RX_CTL	199	200	SPI_1_MOSI	
	ETH_2_RGMII_RXD_0	201	202	SPI_1_CS	
	ETH_2_RGMII_RXD_1	203	204	GND	GPIO
	ETH_2_RGMII_RXD_2	205	206	GPIO_1	
	ETH_2_RGMII_RXD_3	207	208	GPIO_2	
	GND	209	210	GPIO_3	
	ETH_2_RGMII_TX_CTL	211	212	GPIO_4	
	ETH_2_RGMII_TXC	213	214	PWR_1V8_MOCI	
	ETH_2_RGMII_TXD_3	215	216	GPIO_5_CSI	
	ETH_2_RGMII_TXD_2	217	218	GPIO_6_CSI	
	ETH_2_RGMII_TXD_1	219	220	GPIO_7_CSI	
	ETH_2_RGMII_TXD_0	221	222	GPIO_8_CSI	
Gigabit Ethernet	GND	223	224	GND	PCIe
	ETH_1_MDI0_P	225	226	PCIE_1_CLK_N	
	ETH_1_MDI0_N	227	228	PCIE_1_CLK_P	
	GND	229	230	GND	
	ETH_1_MDI1_N	231	232	PCIE_1_L0_RX_N	
	ETH_1_MDI1_P	233	234	PCIE_1_L0_RX_P	
	ETH_1_LED_1	235	236	GND	
	ETH_1_LED_2	237	238	PCIE_1_L0_TX_N	
	ETH_1_MDI2_P	239	240	PCIE_1_L0_TX_P	
	ETH_1_MDI2_N	241	242	GND	
	GND	243	244	PCIE_1_RESET#	
	ETH_1_MDI3_N	245	246	CTRL_RECOVERY_MICO#	System Control
	ETH_1_MDI3_P	247	248	CTRL_PWR_BTN_MICO#	
Power	VCC_BACKUP	249	250	CTRL_FORCE_OFF_MOCI#	
	VCC	251	252	CTRL_WAKE1_MICO#	
	VCC	253	254	CTRL_PWR_EN_MOCI	
	VCC	255	256	CTRL_SLEEP_MOCI#	

	VCC	257	258	CTRL_RESET_MOCI#	
	VCC	259	260	CTRL_RESET_MICO#	

DISCLAIMER: