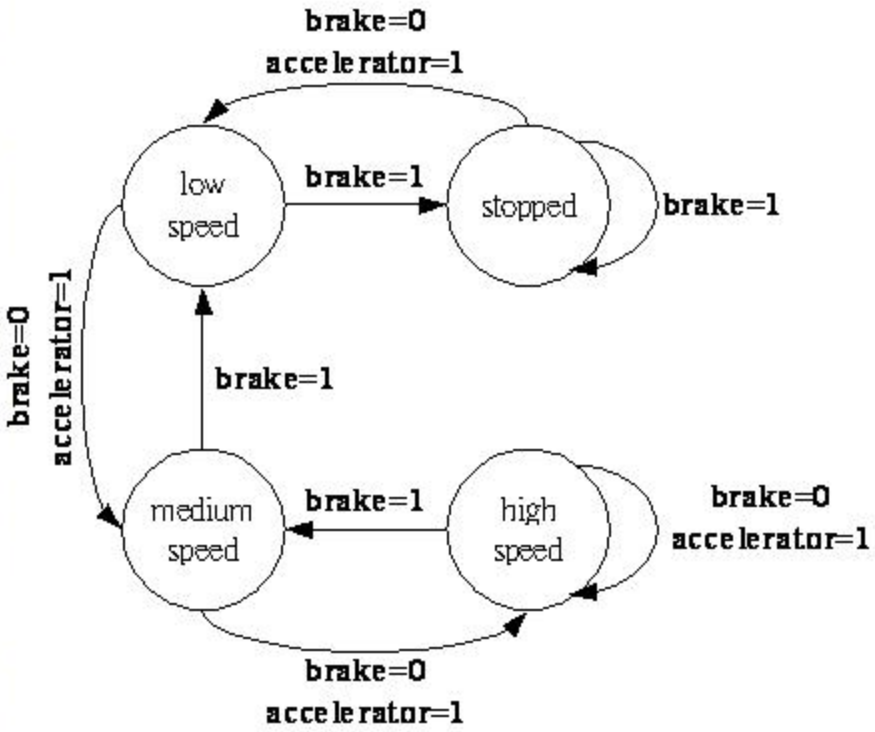
FSM Example


brake=0
accelerator=1
low speed
brake=1
stopped
brake=1
brake=0
accelerator=1
brake=1
medium speed
brake=1
high speed
brake=0
accelerator=1
brake=0
accelerator=1


brake
accelerator
speed
clock

FSM Example1

```
`timescale 1ns/10ps
module fsm(clk,acc,brake,speed);

  input clk,acc,brake;
  output [1:0] speed;
  reg [1:0] state,next_state;

  parameter stopped =2'b00;
  parameter s_low   =2'b01;
  parameter s_medium=2'b10;
  parameter s_high  =2'b11;

  assign speed=state;

always @(posedge clk)
  state <= next_state;
```

```
always @(state or acc or brake)
  if (brake)
     case (state)
       stopped: next_state<=stopped;
       s_low:   next_state<=stopped;
       s_high:  next_state<=s_medium;
       s_medium:next_state<=s_low;
       default: next_state<=stopped;
     endcase
  else if(acc)
     case(state)
       stopped: next_state<=s_low;
       s_low:   next_state<=s_medium;
       s_medium:next_state<=s_high;
       s_high:  next_state<=s_high;
       default: next_state<=stopped;
     endcase
  else
    next_state<=state;
endmodule
```