S5KJN5SP03

1/2.8" 50MP CMOS Image Sensor

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Application Note

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Chip Handling Guide

Precaution against Electrostatic Discharge

When using semiconductor devices, ensure that the environment is protected against static electricity:

1. Wear antistatic clothes and use earth band.
2. All objects that are in direct contact with devices must be made up of materials that do not produce static electricity.
3. Ensure that the equipment and work table are earthed.
4. Use ionizer to remove electron charge.

Contamination

Do not use semiconductor products in an environment exposed to dust or dirt adhesion.

Temperature/Humidity

Semiconductor devices are sensitive to:

- Environment
- Temperature
- Humidity

High temperature or humidity deteriorates the characteristics of semiconductor devices. Therefore, do not store or use semiconductor devices in such conditions.

Mechanical Shock

Do not to apply excessive mechanical shock or force on semiconductor devices.

Chemical

Do not expose semiconductor devices to chemicals because exposure to chemicals leads to reactions that deteriorate the characteristics of the devices.

Light Protection

In non- Epoxy Molding Compound (EMC) package, do not expose semiconductor IC to bright light. Exposure to bright light causes malfunctioning of the devices. However, a few special products that utilize light or with security functions are exempted from this guide.

Radioactive, Cosmic and X-ray

Radioactive substances, cosmic ray, or X-ray may influence semiconductor devices. These substances or rays may cause a soft error during a device operation. Therefore, ensure to shield the semiconductor devices under environment that may be exposed to radioactive substances, cosmic ray, or X-ray.

EMS (Electromagnetic Susceptibility)

Strong electromagnetic wave or magnetic field may affect the characteristic of semiconductor devices during the operation under insufficient PCB circuit design for Electromagnetic Susceptibility (EMS).

Revision History

Revision No.	Date	Description	Author(s)
0.00	Oct.31, 2023	• Initial Draft	DU Yang
0.01	Nov.13, 2023	• Added to AEB	DU Yang
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List of Conventions

Register RW Access Type Conventions

Type	Definition	Description
R	Read Only	The application has permission to read the Register field. Writes to read-only fields have no effect.
RW	Read/Write	The application has permission to read and writes in the Register field. Written value effects on the next frame.
RW/R	Read/Write	The application has permission to read and writes in the Register field. Written value effects only on exit from stand-by.
RW/C	Read/Write	The application has permission to read and writes in the Register field. Changing value typically causes configuration change (either in abort timing or preserve timing modes).
RW/SR	Read/Write	The application has permission to read and writes in the Register field. Changing value may cause entering stand-by / software reset.

Register Value Conventions

Expression	Description
x	Undefined bit
X	Undefined multiple bits
?	Undefined, but depends on the device or pin status
Device dependent	The value depends on the device
Pin value	The value depends on the pin status

Reset Value Conventions

Expression	Description
0	Clears the register field
1	Sets the register field
x	Don't care condition

Warning: Some bits of control registers are driven by hardware or write operation only. As a result the indicated reset value and the read value after reset might be different.

1 Product Overview

1.1 Overview

S5KJN5SP03 is a highly integrated 50.3MP camera chip that includes a CMOS Image Sensor (CIS) with image correction functionality and serial transmission using multi-lane MIPI (4-lane for D-PHY and 3-trio for C-PHY). It is designed for fast and low-power operation to deliver full resolution 50.3MP capture at 15 frames per second (fps), 12.5MP (4:3) video stream at 60fps.

S5KJN5SP03 supports High Dynamic Range (HDR) image capture at both video & still modes, allowing high quality image capture in cases of mixed lighting scenes. It also supports Q-Cell structure which allows efficient Auto Focus in the system.

S5KJN5SP03 is fabricated by the Samsung ISOCELL process developed for imaging applications to realize a high-efficiency and low-power photo sensor. The sensor consists of 8192x6144 effective pixels that matches with the 1/2.8” optical format.

CIS has on-chip Analog to Digital Converter (ADC) arrays to digitize the pixel output and on-chip Correlated Double Sampling (CDS) to drastically reduce the Random Noise (RN) and Fixed Pattern Noise (FPN). It incorporates on-chip camera functions such as defect correction, exposure gain control and image crop.

S5KJN5SP03 CIS is programmable through Camera Control Interface (CCI) and includes on-chip One-Time Programmable (OTP) Non-Volatile Memory (NVM).

S5KJN5SP03 is suitable for a low-power camera module with a 2.2 V/1.8 V/1.0 V power supply.

1.2 Features

S5KJN5SP03 supports the following features:

- 50.3 MP sensor with 1/2.8" optics, Unit pixel size of 0.64 ㎛ x 0.64 ㎛
- Effective resolution of 8192 (H) x 6144 (V) pixels
- 2X2 (at same channel) color filter array
- Q-Cell structure for advanced auto focus
- Electronic rolling shutter
- Maximum normal frame rate of 15 fps @ full 50.3MP, 60 fps @ 12.5 MP
- Maximum video frame rate of 60 fps @ 4K, 240 fps @ FHD(w/o AF)
- Maximum Stg.HDR frame rate of 15 fps @ 12.5 MP/4K
- Maximum DSG frame rate of 30 fps @ 12.5 MP/4K
- ADC accuracy 10 bits
- Embedded H/W remosaic for 50MP RGB bayer output
- 12-bit image capturing with merger interfaces
- Interfaces
  - Fine interface frequency control using additional dedicated PLL for EMI avoidance and integration flexibility
  - MIPI CSI-2: Four lanes (4.5 Gbps per lane) D-PHY / three lanes (4.0 Gsps per lane) C-PHY
- Control interface
  - CCI high-speed I2C-compatible interface: 2-wire serial communication circuit up to 1 MHz
  - I3C compatible interface: 2-wire serial communication circuit up to 12.5 MHz
- Maximum analog gain of 160X with High conversion gain (TBD)
- Dual sensor synchronization
- Vertical flip and horizontal mirror mode
- Bad pixel correction for HW remosaic
- Built-in test pattern generation
- 6Kbits of OTP ROM for users
- Built-in temperature sensor
- Supply voltage of 2.2 V for analog, 1.8 V for I/O, and 1.0 V for digital core supply
- Operating temperature ranges from -20ºC to +85ºC

1.3 Functional Block Diagram

S5KJN5SP03 is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. It uses an on-chip Phase-Locked Loop (PLL) to generate all internal clocks from a single master input clock running between 12 MHz and 64 MHz. Dedicated PLL can generate output interface clocks for maximum flexibility in interface frequency and for EMI avoidance.

Figure 1 illustrates the functional block diagram of sensor.

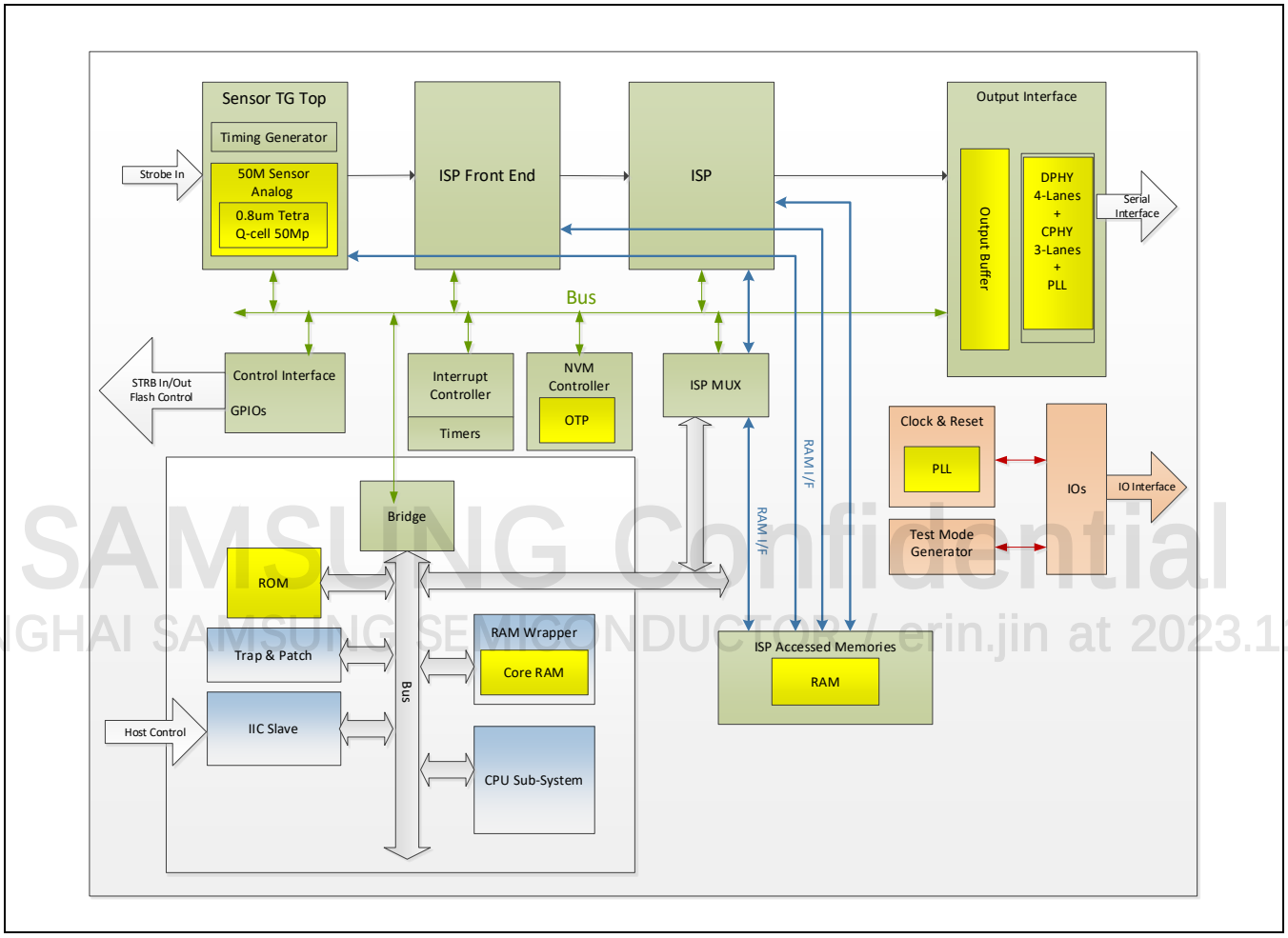


Figure 1 Functional Block Diagram

The image sensor has an on-chip ADC. A column parallel ADC scheme is used for low-power analog processing.

The analog output signal of each pixel includes some temporary random noise caused by the pixel reset action and some fixed pattern noise caused by the in-pixel amplifier offset deviation. To eliminate these noise components, two CDS circuits are used before converting the analog signal to digital signal.

The output from the ADC is a 10-bit value for each pixel in the array. The ADC output passes through a digital processing signal chain, which provides further data path corrections and applies digital gain.

The digital processing chain performs frame black level recovery, compensation for various analog circuit

variations, and non-uniform pixel levels. This compensation is very flexible to allow different compensation for each pixels type and exposure level.

Low-power bad pixel correction block fixes the pre-defined defects that are not handled perfectly by the host ISP bad pixel correction block, such as bad pixel clusters and small level outliers. Isolated bad pixels and pixel pairs can be dynamically detected and replaced based on neighboring pixel pattern.

Remosaic block is used to rearrange 2x2 pattern into Bayer pattern to provide the full resolution output.

S5KJN5SP03 performs and activates deterministic pattern generator and a MIPI CSI-2 frame formatter with embedded line support.

The sensor is interfaced using a set of control and status registers that control many aspects of the sensor behavior, such as frame size, exposure, and gain setting. These registers can be accessed through a CCI interface.

2 Pixel Array Information

2.1 Pixel Array Information

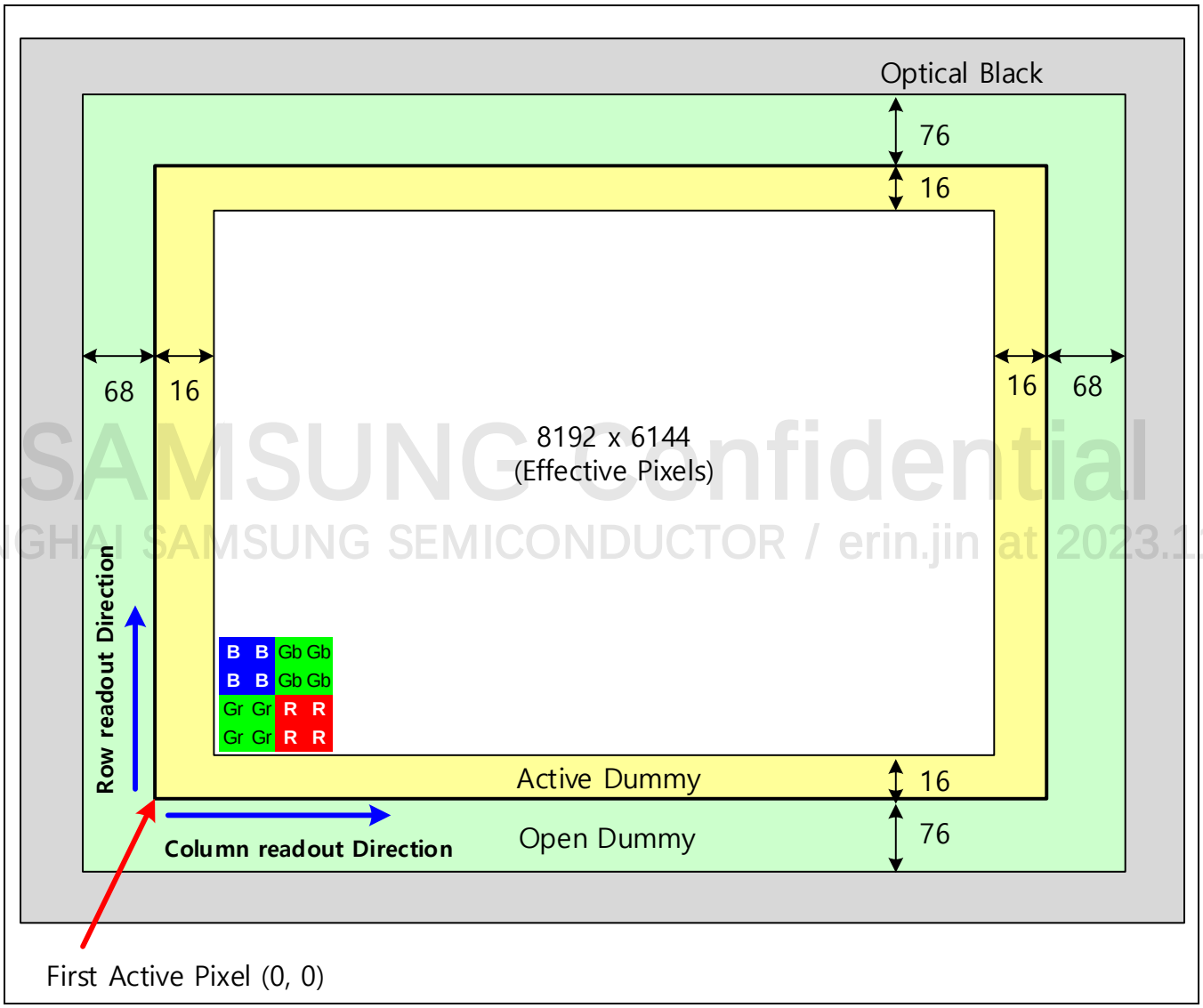


Figure 2 Top View of Pixel Array Information

NOTE: The displayed image is flipped.

Guide: The physical address of the first active pixel is (X = 216, Y = 160).

2.2 Pad Configuration

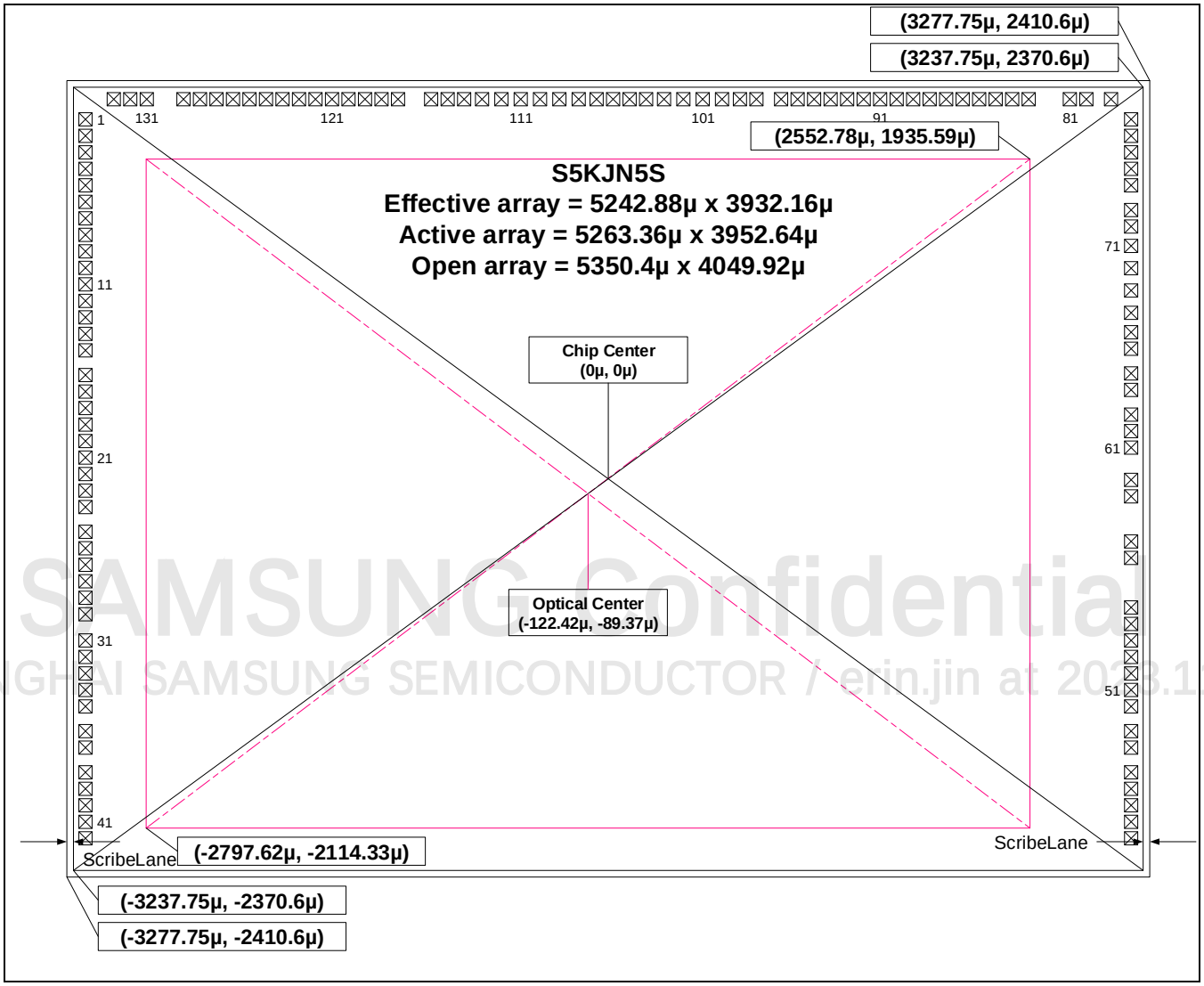


Figure 3 Top View of Chip Dimension

Table 1 describes the pad information of a chip.

- Origin = Center of chip
- NC = Not connected

Table 1 Pad Description

Pad No.	Pad Name	Type	A/D	X-Axis	Y-Axis	Description
1	VSSA18_OTP	GND	A	-3165.095	2176.2	1.8-V ground of OTP
2	VDDA18_OTP	PWR	A	-3165.095	2076.3	1.8-V power of OTP
3	VDDD_L0	O	A	-3165.095	1976.4	1.0V Digital Power
4	NC	BI	A	-3165.095	1876.5	Not Connected
5	VSSD_L1	GND	D	-3165.095	1776.6	1.0V Digital Ground
6	VDDD_L1	PWR	D	-3165.095	1676.7	1.0V Digital Power
7	VDDD_L3	PWR	D	-3165.095	1576.8	1.0V Digital Power
8	VDDD_L4	PWR	D	-3165.095	1476.9	1.0V Digital Power
9	VDDD_L2	PWR	D	-3165.095	1377	1.0V Digital Power
10	VSSD_L2	GND	D	-3165.095	1277.1	1.0V Digital Ground
11	NC	O	A	-3165.095	1177.2	Not Connected
12	NC	O	A	-3165.095	1077.3	Not Connected
13	VSSD_L3	GND	D	-3165.095	977.4	1.0V Digital Ground
14	VSSA18_ABBG	GND	A	-3165.095	877.5	1.8-V ground of ABBG
15	VDDA18_ABBG	PWR	A	-3165.095	777.6	1.8-V power of ABBG
16	VDDD_L5	PWR	D	-3165.095	628.2	1.0V Digital Power
17	VSSD_L4	GND	D	-3165.095	528.3	1.0V Digital Power
18	VDDD_L6	PWR	D	-3165.095	428.4	1.0V Digital Power
19	RETLDO_PD	I	A	-3165.095	328.5	Power Down control input for Retention LDO • Use Retention LDO: "PD" PAD is not connected and a 2.2uF external capacitor is attached to the "RETLDO_VOUT " PAD. • Not use Retention LDO: Connect 1.8V power supply to " RETLDO_PD " PAD and

						VDDD to " RETLDO_VOUT " PAD.
20	RETLDO_VOUT	O	D	-3165.095	228.6	Output Voltage from Retention LDO
21	VDDA_IO_RETLDO	PWR	A	-3165.095	128.7	Shared Power Supply of Retention/IO LDO
22	IOLDO_PD	I	A	-3165.095	28.8	Power Down control input for I/O LDO
23	VSSA_IO_RETLDO	GND	A	-3165.095	-71.1	Shared Ground of Retention/IO LDO
24	IOLDO_VOUT	O	A	-3165.095	-171	LDO output(1.2V)
25	VSS_PLL	GND	A	-3165.095	-320.4	Shared Ground of SYS PLL & DBR PLL
26	VDDD_PLL	PWR	A	-3165.095	-420.3	Shared Power Supply of SYS PLL & DBR PLL
27	VDDA_PLL	PWR	A	-3165.095	-520.2	Shared Power Supply of SYS PLL & DBR PLL
28	AVDD18_PLL	PWR	A	-3165.095	-620.1	Shared Power Supply of SYS PLL & DBR PLL
29	VDDD_L9	PWR	D	-3165.095	-720	1.0V Digital Power
30	VSSD_L5	GND	D	-3165.095	-819.9	1.0V Digital Ground
31	VSUB_L	GND	D	-3165.095	-978.3	GND for substrate connection
32	VDDD_L7	PWR	A	-3165.095	-1078.2	1.0V Analog Power
33	VDDD_L8	PWR	A	-3165.095	-1178.1	1.0V Analog Power
34	VSSD_L6	GND	A	-3165.095	-1278	1.0V Analog Ground
35	VSSD_L7	GND	A	-3165.095	-1377.9	1.0V Analog Ground
36	VSSA_OTA2_L1	GND	A	-3165.095	-1527.3	Ground of CDS
37	VDDA_CDS_L1	PWR	A	-3165.095	-1627.2	Power supply of CDS
38	VDDA_APS_L1	PWR	A	-3165.095	-1776.6	Power Supply for APS
39	VDDA_APS_L2	PWR	A	-3165.095	-1876.5	Power Supply for APS
40	VSSA_APS_L1	GND	A	-3165.095	-1976.4	Ground for APS

41	VSSA_APS_L2	GND	A	-3165.095	-2076.3	Ground for APS
42	NC	GND	A	-3165.095	-2176.2	Not Connected
43	NC	GND	A	3165.095	-2176.2	Not Connected
44	VSSA_APS_R1	GND	A	3165.095	-2076.3	Ground for APS
45	VSSA_APS_R2	GND	A	3165.095	-1976.4	Ground for APS
46	VDDA_APS_R1	PWR	A	3165.095	-1876.5	Power Supply for APS
47	VDDA_APS_R2	PWR	A	3165.095	-1776.6	Power Supply for APS
48	VDDA_CDS_R1	PWR	A	3165.095	-1627.2	Power supply of CDS
49	VSSA_OTA2_R1	GND	A	3165.095	-1527.3	Ground of CDS
50	VSSD_R1	GND	A	3165.095	-1377.9	1.0V Analog Ground
51	VSSD_R2	GND	A	3165.095	-1278	1.0V Analog Ground
52	VDDD_R1	PWR	A	3165.095	-1178.1	1.0V Analog Power
53	VDDD_R2	PWR	A	3165.095	-1078.2	1.0V Analog Power
54	VSUB_R	GND	A	3165.095	-978.3	GND for substrate connection
55	VSSD_R3	GND	D	3165.095	-878.4	1.0V Digital Ground
56	VDDD_R3	PWR	D	3165.095	-778.5	1.0V Digital Power
57	VDDA_RMP1	PWR	A	3165.095	-478.8	Power supply for RMP
58	VDDA_RMP2	PWR	A	3165.095	-378.9	Power supply for RMP
59	VSSA_RMP1	GND	A	3165.095	-106.2	Ground for RMP
60	VSSA_RMP2	GND	A	3165.095	-6.3	Ground for RMP
61	NC	BI	A	3165.095	189	Not Connected
62	VDDA_REF	PWR	A	3165.095	288.9	Power supply for REF
63	VSSA_REF	GND	A	3165.095	388.8	Ground for REF
64	VSSA_BGR	GND	A	3165.095	538.2	Ground for BGR inside REF
65	VDDA_BGR	PWR	A	3165.095	638.1	Power supply for BGR inside REF
66	VSSD_R4	GND	D	3165.095	787.5	1.0V Digital Ground

67	VDDD_R4	PWR	D	3165.095	887.4	1.0V Digital Power
68	VRG	BI	A	3165.095	1004.85	APS RG drive voltage
69	VDCG	BI	A	3165.095	1139.85	APS DCG drive voltage
70	VSEL	BI	A	3165.095	1274.85	APS SEL drive ON voltage
71	VTG	BI	A	3165.095	1409.85	APS TG drive ON voltage
72	VSSA_DBR	GND	A	3165.095	1527.3	Ground for DBR
73	VDDA_DBR	PWR	A	3165.095	1627.2	Power Supply for DBR
74	VNTG	BI	A	3165.095	1776.6	RDV negative power supply for TG switch
75	VSSA18_ATOP_R	GND	A	3165.095	1876.5	1.8V Power supply
76	VDDA18_ATOP_R	PWR	A	3165.095	1976.4	1.8V Power supply
77	NC	GND/X2_VNCP	A	3165.095	2076.3	Not Connected
78	NC	GND/X1_VNCP	A	3165.095	2176.2	Not Connected
79	VSSPN_TR	GND	A	3043.35	2297.945	Power Supply for APS
80	VDDA_APS_TR	PWR	A	2893.95	2297.945	Power Supply for APS
81	VSSA_APS_TR	GND	A	2794.05	2297.945	Power Supply for APS
82	NC	BI	D	2544.75	2297.945	Not Connected
83	NC	BI	D	2444.85	2297.945	Not Connected
84	GPIO_3	BI	D	2344.95	2297.945	General purpose I/O 1
85	GPIO_2	BI	D	2245.05	2297.945	General purpose I/O 2
86	GPIO_1	BI	D	2145.15	2297.945	General purpose I/O 3
87	NC	BI	D	2045.25	2297.945	Not Connected
88	VDDIO_T1	PWR	A	1945.35	2297.945	I/O Power Supply
89	VSSIO_T1	GND	A	1845.45	2297.945	I/O Power Supply
90	NC	BI	D	1745.55	2297.945	Not Connected
91	NC	BI	D	1645.65	2297.945	Not Connected
92	NC	BI	D	1545.75	2297.945	Not Connected
93	NC	BI	D	1445.85	2297.945	Not Connected

94	VDDD_T1	PWR	D	1345.77	2297.945	1.0V Digital Power
95	VSSD_T1	GND	D	1245.87	2297.945	1.0V Digital Ground
96	VDDD_T2	PWR	D	1145.97	2297.945	1.0V Digital Power
97	VSSD_T2	GND	D	1046.07	2297.945	1.0V Digital Ground
98	M_VDD1_T1	PWR	A	896.67	2297.945	1.0 V Power for Internal Logic
99	M_VSS_T1	GND	A	796.77	2297.945	1.0 V Ground for Internal Logic
100	M_DPDATA3	O	A	688.32	2297.945	Master DATA3 Lane DP for D-PHY
101	M_DNDATA3_C2	O	A	571.32	2297.945	Master DATA3 Lane DP for D-PHY
102	M_DPDATA2_B2	O	A	454.32	2297.945	Master DATA2 Lane DP for D-PHY and Master B2 Lane for C-PHY
103	M_DNDATA2_A2	O	A	337.32	2297.945	Master DATA2 Lane DN for D-PHY and Master A2 Lane for C-PHY
104	VSSD_T3	GND	A	228.87	2297.945	1.0V Digital Ground
105	VDDD_T3	PWR	A	128.97	2297.945	1.0V Digital Power
106	M_VDD1_T2	PWR	A	29.07	2297.945	1.0 V Power for Internal Logic
107	M_VSS_MIPI	GND	A	-70.83	2297.945	Ground for MIPI
108	M_DPCLK_C1	O	A	-179.28	2297.945	Master CLK Lane DP for D-PHY and Master C1 Lane for C-PHY
109	M_DNCLK_B1	O	A	-296.28	2297.945	Master CLK Lane DN for D-PHY and Master B1 Lane for C-PHY
110	M_DPDATA1_A1	O	A	-413.28	2297.945	Master DATA1 Lane DP for D-PHY and Master A1 Lane for C-PHY
111	M_DNDATA1_C0	O	A	-530.28	2297.945	Master DATA1 Lane DN for D-PHY and Master C0 Lane for C-PHY

112	M_DPDATA0_B0	O	A	-647.28	2297.945	Master DATA0 Lane DP for D-PHY and Master B0 Lane for C-PHY
113	M_DNDATA0_A0	O	A	-764.28	2297.945	Master DATA0 Lane DN for D-PHY and Master A0 Lane for C-PHY
114	M_VSS_T2	GND	A	-872.73	2297.945	1.0 V Power for Internal Logic (MIPI)
115	M_VDD1_T3	PWR	A	-972.63	2297.945	1.0 V Power for Internal Logic (MIPI)
116	M_VDD18	PWR	A	-1072.53	2297.945	1.8 V Power for Analog (MIPI)
117	MCLK	I	D	-1273.05	2297.945	External Input Clock
118	RSTN	I	D	-1372.95	2297.945	Master Reset, active low
119	TST	I	D	-1472.85	2297.945	Test: EDS test configuration pin. Tie low in normal operation
120	VSYNC	BI	D	-1572.75	2297.945	VSYNC Signal
121	I2C_SPI_N_SEL	I	D	-1672.65	2297.945	SPI/CCI Select (1: CCI, 0: SPI)
122	VDDD_T10	PWR	D	-1772.55	2297.945	1.0V Digital Power
123	VSSD_T10	GND	D	-1872.45	2297.945	1.0V Digital Power
124	VSSIO_T2	GND	A	-1972.35	2297.945	I/O Power Supply
125	VDDIO_T2	PWR	A	-2072.25	2297.945	I/O Power Supply
126	SCK	BI	D	-2172.15	2297.945	SPI mode: Serial Data Clock / CCI Data, connect external 2.2KOhm resistor
127	SDI	BI	D	-2272.05	2297.945	SPI mode: Serial Data Input / CCI Clock, connect external 2.2KOhm resistor
128	SDO	BI	D	-2371.95	2297.945	SPI mode: Serial Data output / CCI mode: I2C/I3C Select (0:I2C, 1:I3C)
129	I2C_A0_XCE	BI	D	-2471.85	2297.945	SPI mode: Serial Data Chip Select / CCI mode : i2c id select - LSB

130	I2C_A1	BI	D	-2571.75	2297.945	CCI mode : i2c id select - MSB
131	NC	GND	A	-2794.05	2297.945	Not Connected
132	VSSA_APS_LT	GND	A	-2893.95	2297.945	Power Supply for APS
133	VDDA_APS_LT	PWR	A	-2993.85	2297.945	Power Supply for APS

2.3 Application Circuit

Figure 4 illustrates the top view of a module application circuit.

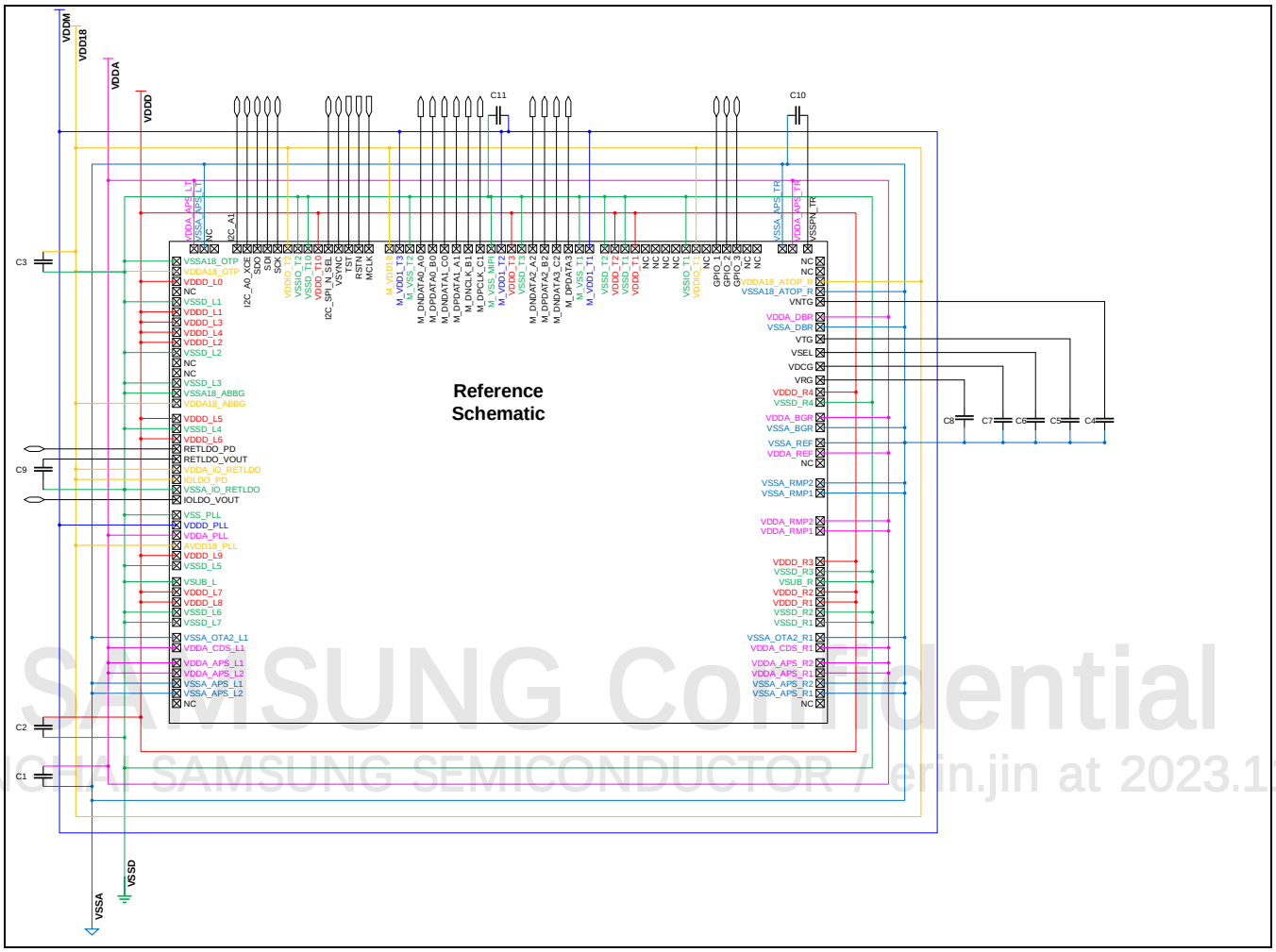


Figure 4 Top View of Module Application Circuit (1.8V IOs)

3 Embedded Controller

4 Control Interface (I2C/I3C)

5 Clock Settings

6 Functional Operation Modes

S5KJN5SP03 can support a wide range of operation modes. These operation modes consist of following mode parameters:

- Interface bandwidth
- Image requested quality
- H/W limitations (For example, minimum H/V-blank and blocks delay)
- Requested sensor output size and sensor operation mode
- CIS output size and number of bits per pixel (For example, RAW12, RAW10)
- Required V-blank time
- Power consumption limitations
  (For example, using single PLL, limited MIPI lanes, and system low-power modes)

오류! 참조 원본을 찾을 수 없습니다. describes the typical operation modes and its related typical settings.

Modes	Methodology	Frame Rate(2)	CIS Output		PDAF Tail mode	Max. user Again(2)
			H	V		
50 MP	Full output	15 fps	8192	6144	Support	X32
12.5 MP	SUM mode	60 fps	4096	3072	Support	X160
12.5 MP(10bit)	SUM, Stg.HDR (Global Fixed Again)	30fps(1)	4096	3072	Support	X160
12.5 MP(10bit)	SUM, Stg.HDR (Separate Again)	15fps(1)	4096	3072	Support	X160
12.5 MP(12bit)	SUM, DSG	30fps	4096	3072	Support	X40
4K	SUM & Crop	60 fps	4096	2304	Support	X160
4K(10bit)	Sum & Crop, Stg.HDR (Global Fixed Again)	30fps(1)	4096	2304	Support	X160
4K(10bit)	Sum & Crop, Stg.HDR (Separate Again)	15fps(1)	4096	2304	Support	X160

1. Stg.HDR fps will be changed according to Analog gain control
2. Framerate is based on half of max user Again. If applying max. user gain, framerate will be decreased 1/2

7 Power Sequence

8 Frame Settings

9 Exposure Control

10 AE Update Timing

11 Gain Control

11.1 Analog Gain Control

Analog gain can be calculated by the following equation:

$$gain = \frac{x}{0x20}$$

Where "x" is the user's input for analog gain parameter.

Table 2 Analog Gain Control Registers

Name	Address	Assigned Byte	Default Value	Description
Analog gain	0x40000204	2	0x0020	Set the analog gain, the value is divided by 0x20

NOTE: In S5KJN5SP03, analog gain is global; there is no per-channel gain. $gain = \frac{x}{32}$

Table 3 Analog gain example Table

Gain Value	Analog_gain_code_XXX Register Value
X1	0x0020
X2	0x0040
X3	0x0060
X8	0x0100
X10	0x0140
X12	0x0180
X16	0x0200
X32	0x0400
X64	0x0800 (only in 12.5MP mode)
X80	0x0A00 (only in 12.5MP mode)
X160	0x1400 (only in 12.5MP mode)

NOTE: 12.5MP Summation mode support up to x160

11.2 Digital Gain Control

Digital gain can be calculated by the following equation:

$$gain = \frac{x}{0x100}$$

Where "x" is the user's input for analog gain parameter.

Table 4 Digital Gain example Table

Gain Value[times]	Analog gain Register Value (Hex)
X1	0x0100
X2	0x0200
X3	0x0300
X8	0x0800
x16	0x1000

Table 5 Digital Gain Control Registers

Name	Address	Assigned Byte	Default Value	Description
digital_gain_digital_gain_mode	0x4000020D	1	0x00	0 = control all channels by using green red register 1 = Per channel digital gain 2 = control all channels and all exposures by using green red register
digital_gain_gains_green_red	0x4000020E	2	0x0100	Digital gain control for the green pixels on rows that also contain red pixels – short only or single exposure
digital_gain_gains_red	0x40000210	2	0x0100	Red channel digital gain control – short only or single exposure
digital_gain_gains_blue	0x40000212	2	0x0100	Blue channel digital gain control – short only or single exposure
digital_gain_gains_green_blue	0x40000214	2	0x0100	Digital gain control for the green pixels on rows that also contain blue pixels – short only or single exposure

Guide: Apply Analog Gain to the maximum and then apply Digital gain

11.3 White Balance Digital Color Gain for Re-mosaic mode

The **S5KJN5SP03** supports H/W remosaic in Full (50Mp) mode, which requires color gain (R,G,B) information in real time for the H/W remosaic block. To ensure picture quality, the user needs to apply the white balance gain, which is done in real time by the AP, to the following registers. Failure to apply the color gain of the white balance may result in unexpected false colors and sharpness degradation, affecting picture quality.

Table 6 White Balance Gain Control Registers

Name	Address	Assigned Byte	Default Value	Description
absolute_gain_red	0x40000D82	2	0x0400	Calculated gain for red channel, in 10 fraction bits (max = x16) 0x0400h (x1), 0x0800h (x2)
absolute_gain_green	0x40000D84	2	0x0400	Calculated gain for green channel, in 10 fraction bits (max = x16) 0x0400h (x1), 0x0800h (x2)
absolute_gain_blue	0x40000D86	2	0x0400	Calculated gain for blue channel, in 10 fraction bits (max = x16) 0x0400h (x1), 0x0800h (x2)

12 Auto Exposure Bracketing (AEB)

12.1 Overview

AEB is a function that allows you to obtain multiple images with different settings such as exposure, gain and so on. Outputs frames by applying pre-defined shutter, gain, and Frame Length Lines (FLL) settings into Look-Up Table (LUT) without adjusting exposure level at each frame.

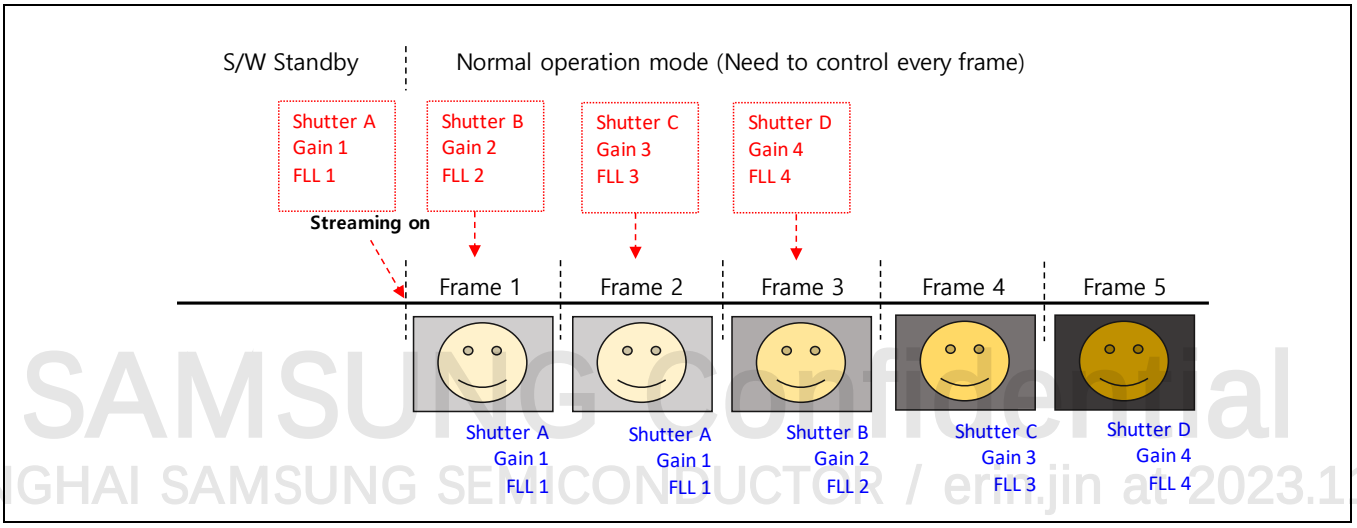


Figure 5 Normal Operation Mode output

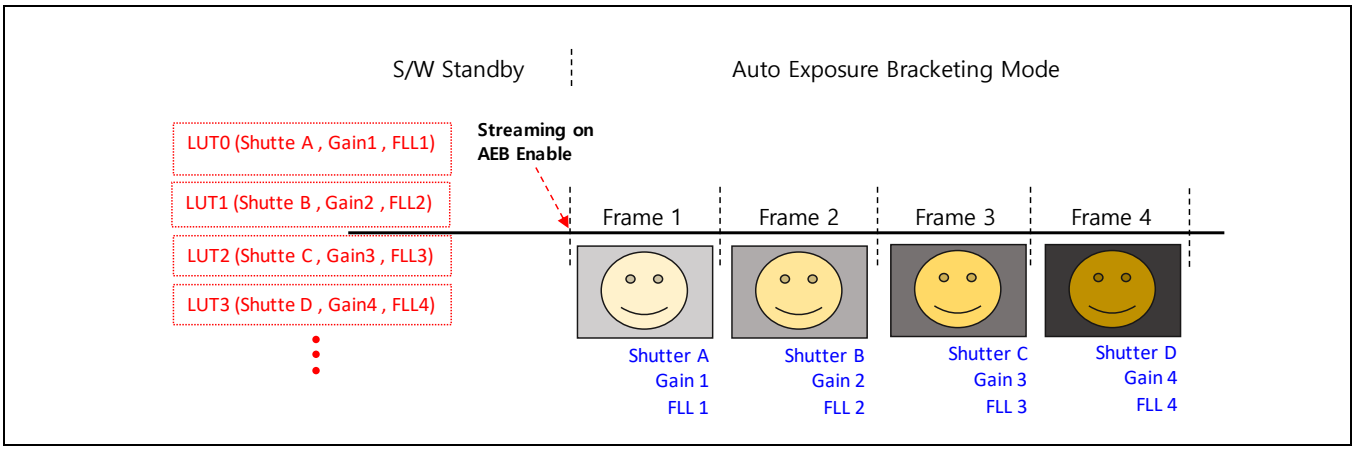


Figure 6 AEB Operation Mode output

12.2 AEB Control Register

Table 7 Bracketing Control Registers

Name	Address	Assigned Byte	Description
api_rw_bracketing_lut_control	0x40000E00	1	AEB enable and the number of bracketing frames 0 : disable 1 ~ N : bracketing over N frames. The maximum value of N depends on the number of selected fileds. Max N = Total # of LUT(120) / # of selected field ** If you use AEB with bracketing frame control (VC, Frame ID, Data type, Max N is 4 frames.
api_rw_bracketing_lut_mode	0x40000E01	1	[0]: 0 = return to SW Standby after bracketing, 1 = continue in streaming after bracketing [1]: 0 = single bracketing, 1 = loop mode [3]: 0 = load new LUT as soon as possible 1 = run the current LUT again before loading new fast configuration chang [4]: 0 = load new LUT as soon as possible 1 = run the current LUT again before loading new LUT [5]: 0 = load new LUT as soon as possible 1 = in case of last frame in the loop, run an additional loop, else, finish current loop before fast configuration chang [6]: 0 = load LUT only after loop has finished 1 = load LUT each frame
api_rw_bracketing_selected_fields	0x40000E04	2	[0]: 1 = coarse integration time [1]: 1 = global analog gain [2]: 1 = long coarse integration time [3]: 1 = long analog gain [4]. 1 = flash strobe [5]: 1 = global digital gain [6]: 1 = long digital gain [10]: 1 = frame length lines (FLL) [11]: 2 = VC DT (byte 0/1 – VC short/long, byte 2/3 - DT) [12]: 2 = PDAF VC DT (byte 0/1 - VC, byte 2/3 - DT) [13]: 1 = Frame ID [14]: 1 = Force DCG mode
api_rw_bracketing_loop_mode_num_of_repetitions	0x40000E03	1	when using loop mode (lut_mode[1] = 1), this field specifies the number of times to repeat the loop 0 - repeat the loop indefinitely. 1-0xFF - number of times to repeat the loop when using loop mode (lut_mode[1] = 1), this field specifies the number of times to repeat the loop

Name	Address	Assigned Byte	Description
			0 - repeat the loop indefinitely. 1-0xFF - number of times to repeat the loop

12.3 AEB setting example

Case1. CINTR, Single AEB Mode

```
s60284000 //Page
s01000000 // Streaming off
s03340001 // api_rw_frame_timing_dynamic_frame_rate_enable
s0E000201 // api_rw_bracketing_lut_control (40000E00 02), api_rw_bracketing_lut_mode    (40000E01 01)
s0E048001 // api_rw_bracketing_selected_fields
s0E100400 //1st frame shutter
s0E121c00 //2nd frame shutter

s01000100 //Stream On
```

Example 1 Single Bracketing

Case2. CINTR & Again & SHIFTER & Dgain N-times loop AEB Mode

```
s60284000  //Page
s01000000 // Streaming off
s03340001 // api_rw_frame_timing_dynamic_frame_rate_enable
s020C0002 // dgain mode
s0E000203 // api_rw_bracketing_lut_control (40000E00 02), api_rw_bracketing_lut_mode (40000E01 03)
s0E020003 //api_rw_bracketing_loop_mode_num_of_repetitions
s0E040023 // api_rw_bracketing_selected_fields
s07020400 // api_rw_long_frame_timing_frame_length_lines_sh
s07040400 // api_rw_long_frame_timing_coarse_integration_time_sh
s0E100500 //1st frame color shutter
s0E120020 //1st frame Analog Gain
s0E140200 //1st frame Color Digital
s0E160500 //2nd frame color shutter
s0E180020 //2nd frame Analog Gain
s0E1A0600 //2nd frame color digital gain
s01000100 //Stream On
```

Example 2 N loop mode Bracketing

Case3. CINTR & Again & SHIFTER & Dgain infinite loop AEB Mode

```
s60284000  //Page
s01000000 // Streaming off
s03340001 // api_rw_frame_timing_dynamic_frame_rate_enable
s020C0002 // dgain mode
s0E000203 // api_rw_bracketing_lut_control (40000E00 02), api_rw_bracketing_lut_mode (40000E01 03)
s0E020000 // repeat the loop indefinitely
s0E040023 // api_rw_bracketing_selected_fields
s07020400 // api_rw_long_frame_timing_frame_length_lines_sh
s07040400 // api_rw_long_frame_timing_coarse_integration_time_sh
s0E100500 //1st frame color shutter
s0E120020 //1st frame Analog Gain
s0E140200 //1st frame Color Digital
s0E160500 //2nd frame color shutter
s0E180020 //2nd frame Analog Gain
s0E1A0600 //2nd frame color digital gain
s01000100 //Stream On
```

Example 3 infinite loop mode Bracketing

13 Stream Preserving and Interrupting Register Updates

14 Output Interface

15 Image Signal Processing Front End

16 Dual Sensor Synchronization

17 HW Guide for Dual Module

17.1 Module Design

All ground and power must be separated between master and slave sensor.
The same domain of power sources should be placed close or overlap together.(ex. AVDD_S and AGND_S)
Each power pin should be placed more than S(=3*W).

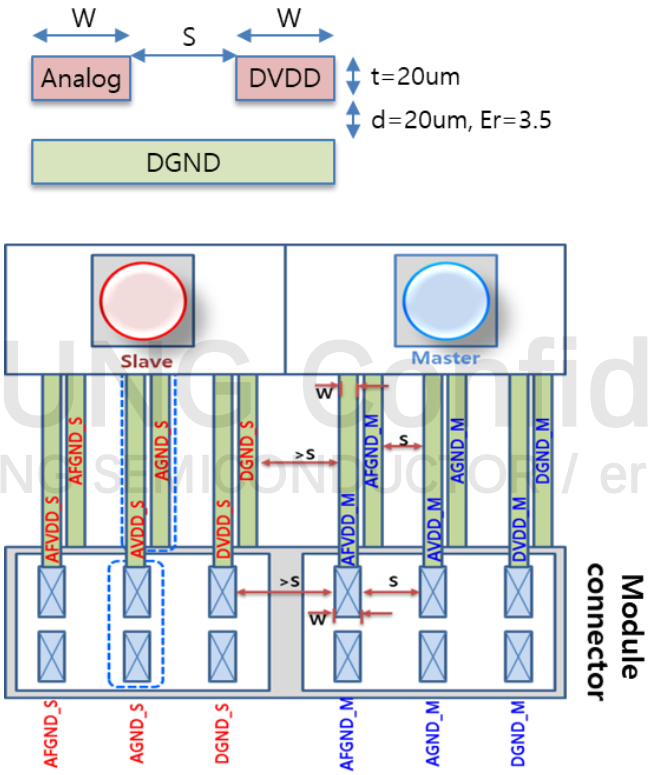


Figure 7 Module Design Guide

17.2 Simulation result

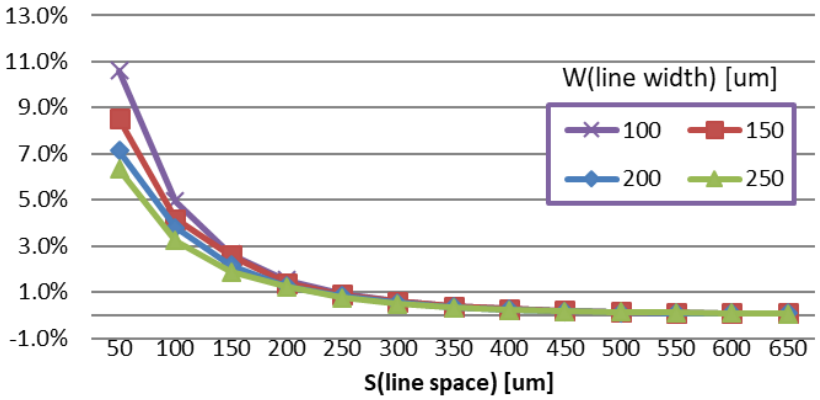


Figure 8 Coupling ratio vs. W, S on FPCB

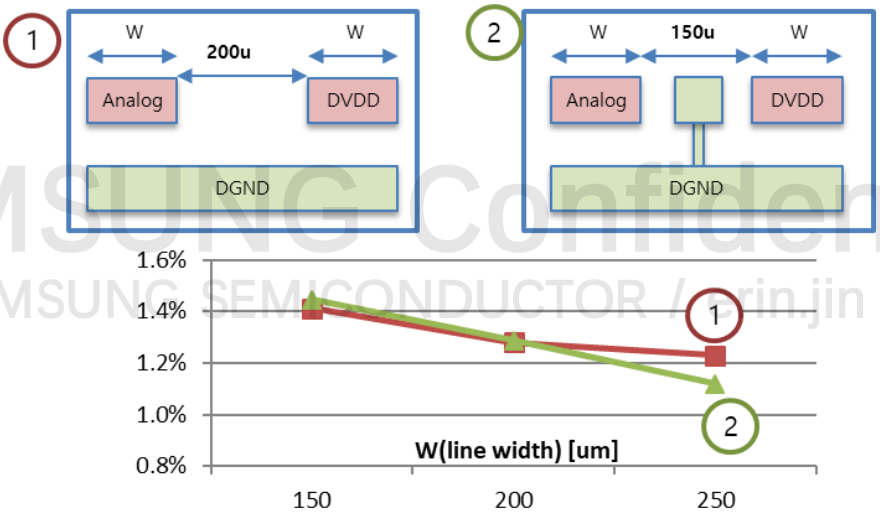


Figure 9 Coupling ratio vs. GND shield

17.3 LDO Selection Guide for Dual module

- Must-Do's
- Use an LDO (low-dropout regulator) rather than a PMIC
  (Recommended suppliers: TI, Ricoh and ON Semi, to name a few)
- Ripple rejection (RR): > 40 dB around 10 kHz – 1 MHz
  (If RR is not satisfied, increase output capacitance or use a better LDO)

Table 8 Minimum output capacitor per LDO

Supplier	Product name	Min. output capacitor

TI	LP5907	1.0 μF
Ricoh	RP112	1.0 μF
Ricoh	RP114	4.7 μF
ON Semi	NCP160	4.7 μF
SGMICRO	SGM2031	10 μF

- Better-to-Do's
  - RVDD < 30 mΩ, RGND < 10 mΩ
  - Put extra capacitor near the sensor module side, if needed.

17.4 Exclusive Usage of LDO

- VDDD(Digital Power)
  - Generally use each LDO due to the power consumption

- VDDA(Analog Power)
  - Must use each VDDA-LDO for minimizing the power coupling. Because a frequency band around 100Khz could be sensitive to external power noise.
  - So required the exclusive use of each LDO.

- VDDIO(I/O Power)
  - Recommend to use each VDDIO-LDO.

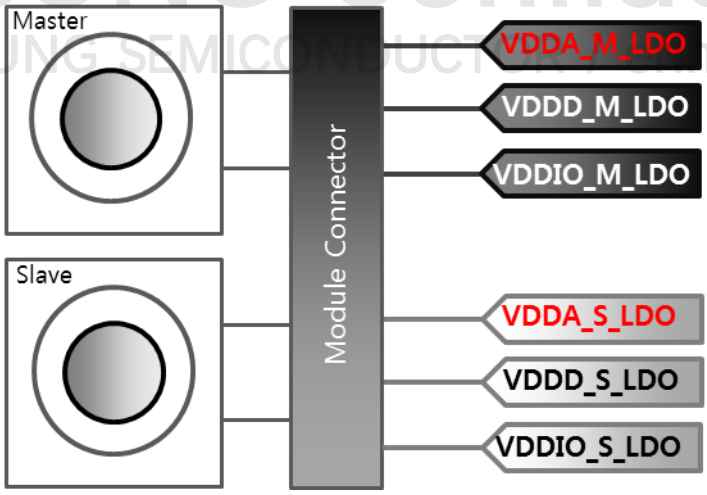


Figure 10 Exclusive LDO

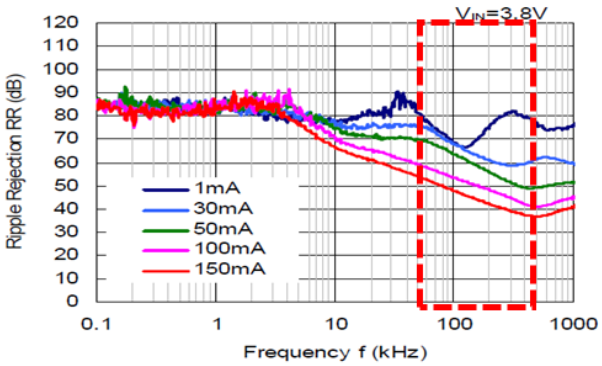
17.5 Recommended LDO Selection

- Recommended LDO suppliers: TI, Ricoh and ON Semi
  - Detailed data in the attached spreadsheet

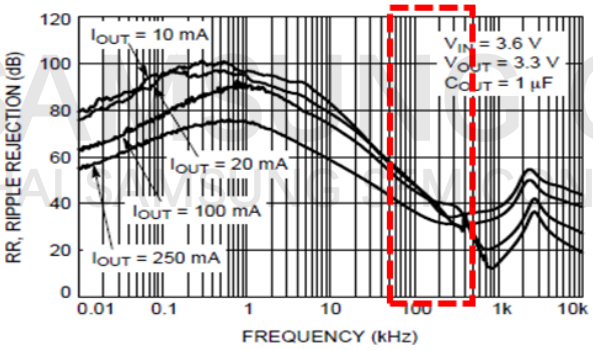
- Most important specification on a datasheet: **Ripple Rejection** around **100 kHz*** (in log scale): > **40 dB**
  - to compensate for sensor's PSRR

Recommended

< Ricoh – RP112 >

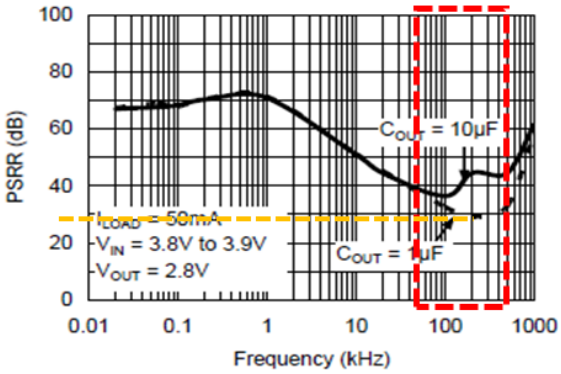


< ON Semi – NCP160 >

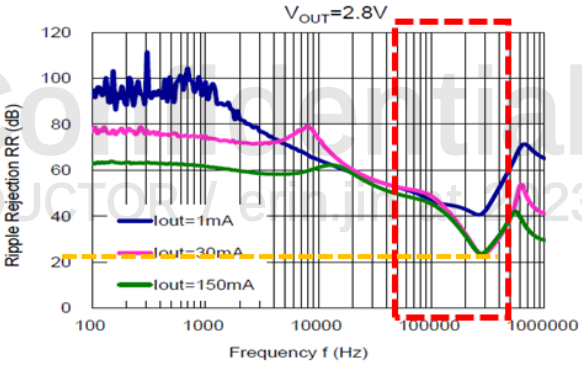


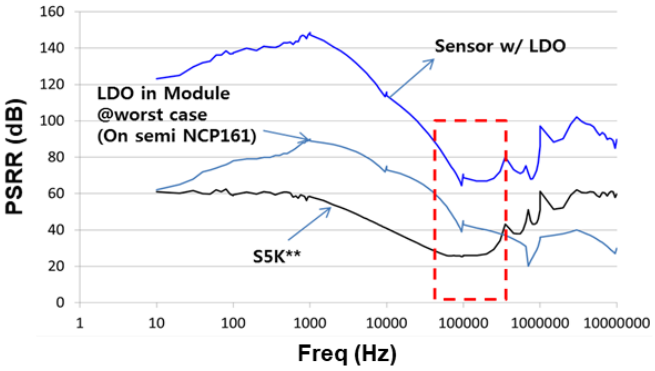
Not recommended

< SGMICRO – SGM2031 >



< DIODE5 – AP7343 >





[General LDO performance by supplier]

	100Hz	1KHz	10KHz	100KHz	1MHz
SGMICRO	80	70	55	30	10
Will Semiconductor	70	70	62.5		
DIODES	70	73	50	30	55
OnSemi	80	75	68	50	43
Richo	70	60	55	45	55
TI	85	85	75	68	60

Figure 11 Recommended LDO Characteristics

18 NVM Memory (non-volatile OTP memory)

18.1 NVM Memory Overview

S5KJN5SP03 supports NVM Memory. The NVM memory module is a non-volatile (One-Time Programmable-OTP) memory module. Some areas of the NVM memory store data unique to the chip in the factory, and some areas store values for calibration. Of the total memory capacity, 6Kbits are allocates for use by user.

18.2 NVM(OTP) Memory Map

1Page = 64bytes

NVM Memory Size: 64bytes x 768Page = 49,152 bytes

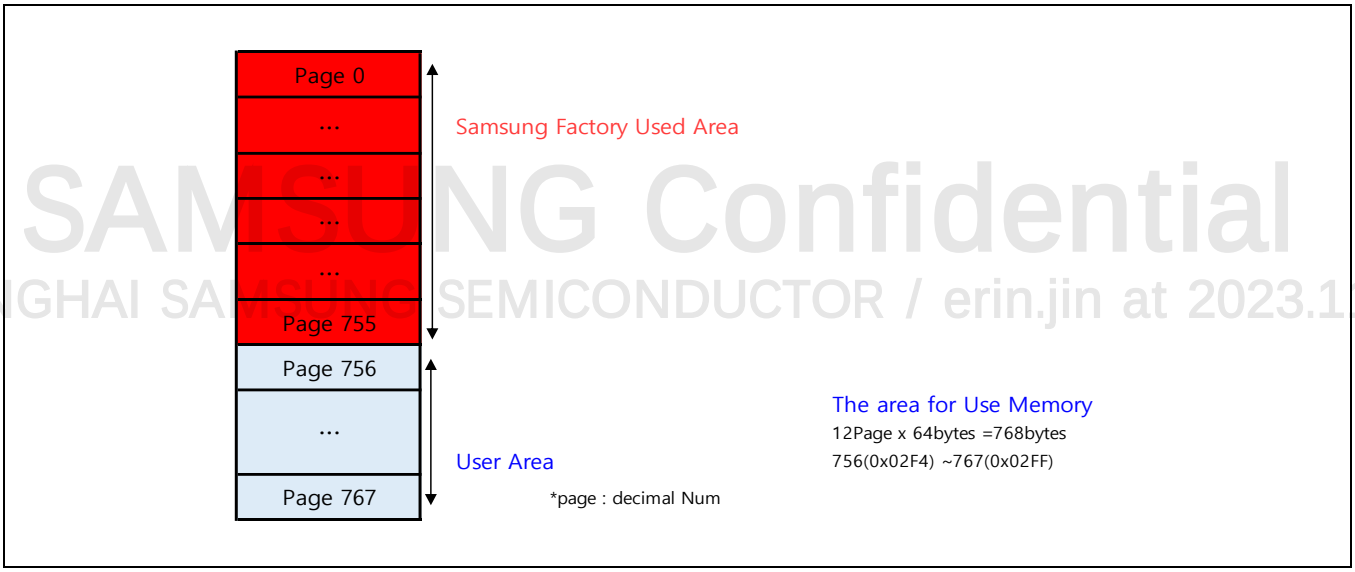


Figure 12 NVM map for S5KJN5SP03

18.3 NVM(OTP) Control registers

Table 9 OTP Control Registers

Name	Address	Assigned Byte	Default Value	Description
api_rw_data_transfer	0x40000A00	1	0x00	Bit[0] : 1- Enable 0-Disable Bit[1] : 1- Write enable 0- Read enable At the end of the sequence 0x00 Read completed with no errors

				0x04 Read completed with errors 0x02 Write completed with no errors (Buffer is not cleared) 0x06 Write completed with errors 0x82 Write completed with no errors (Buffer cleared) 0x86 Write completed with errors

18.4 NVM Memory Read

It is used to read for verifying that the value written in the NVM is normal. Sensor name, Chip-ID, and version are created in the factory can also be read in the following sequence.

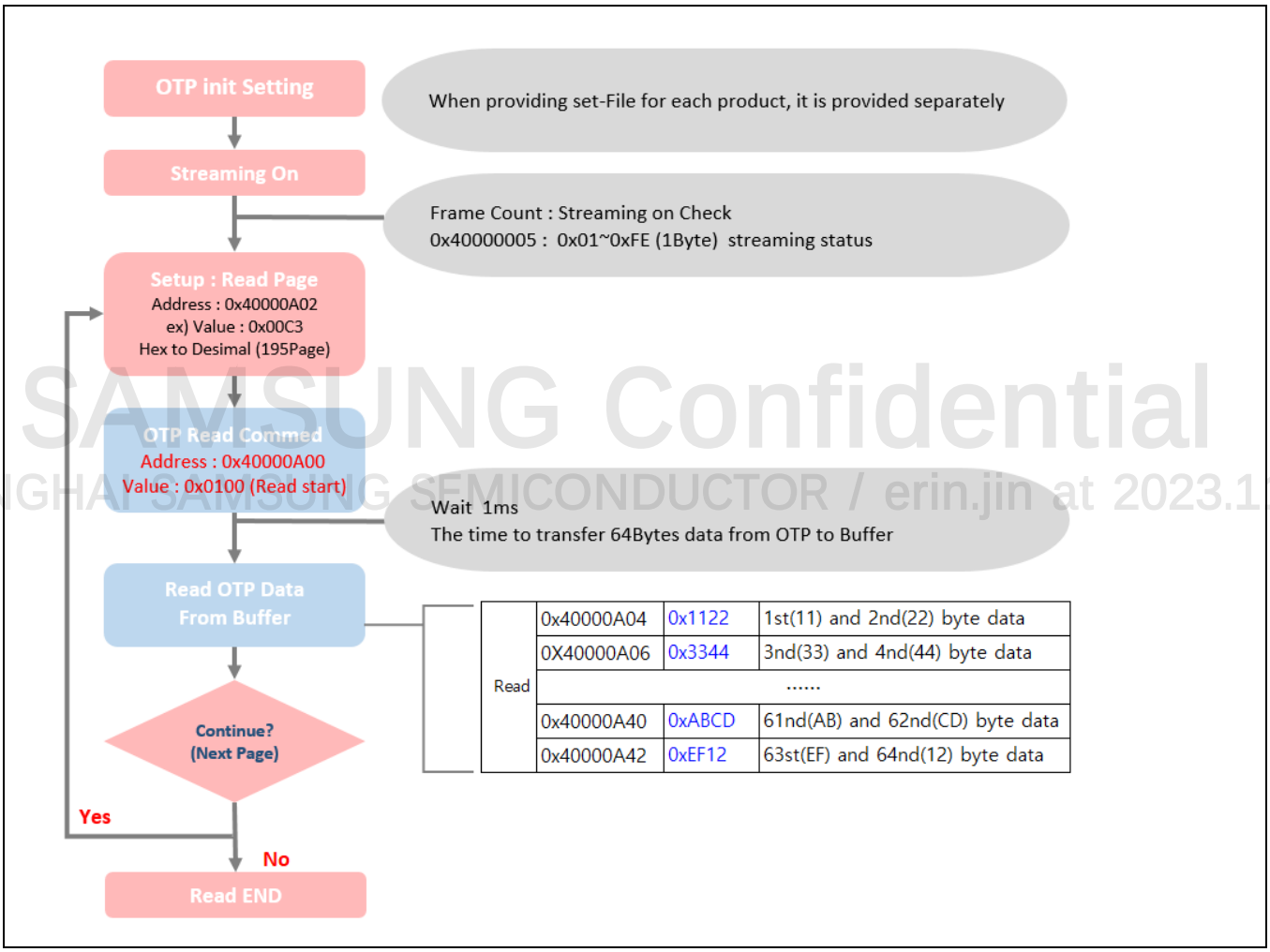


Figure 13 NVM Read Sequence

18.5 NVM Memory Write

Each calibration data like x-talk compensation and user data for module house may be written on NVM(OTP) memory. .

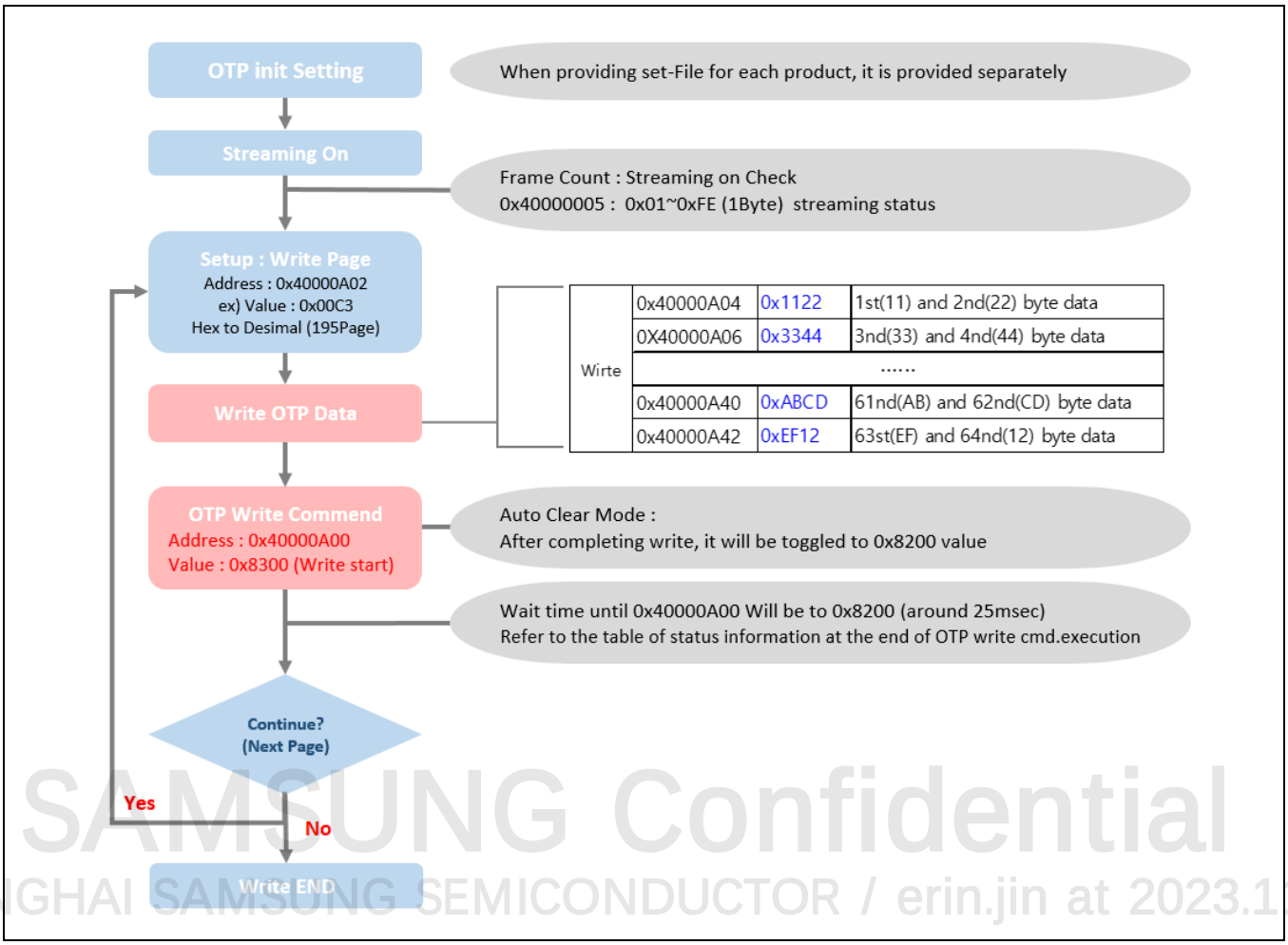
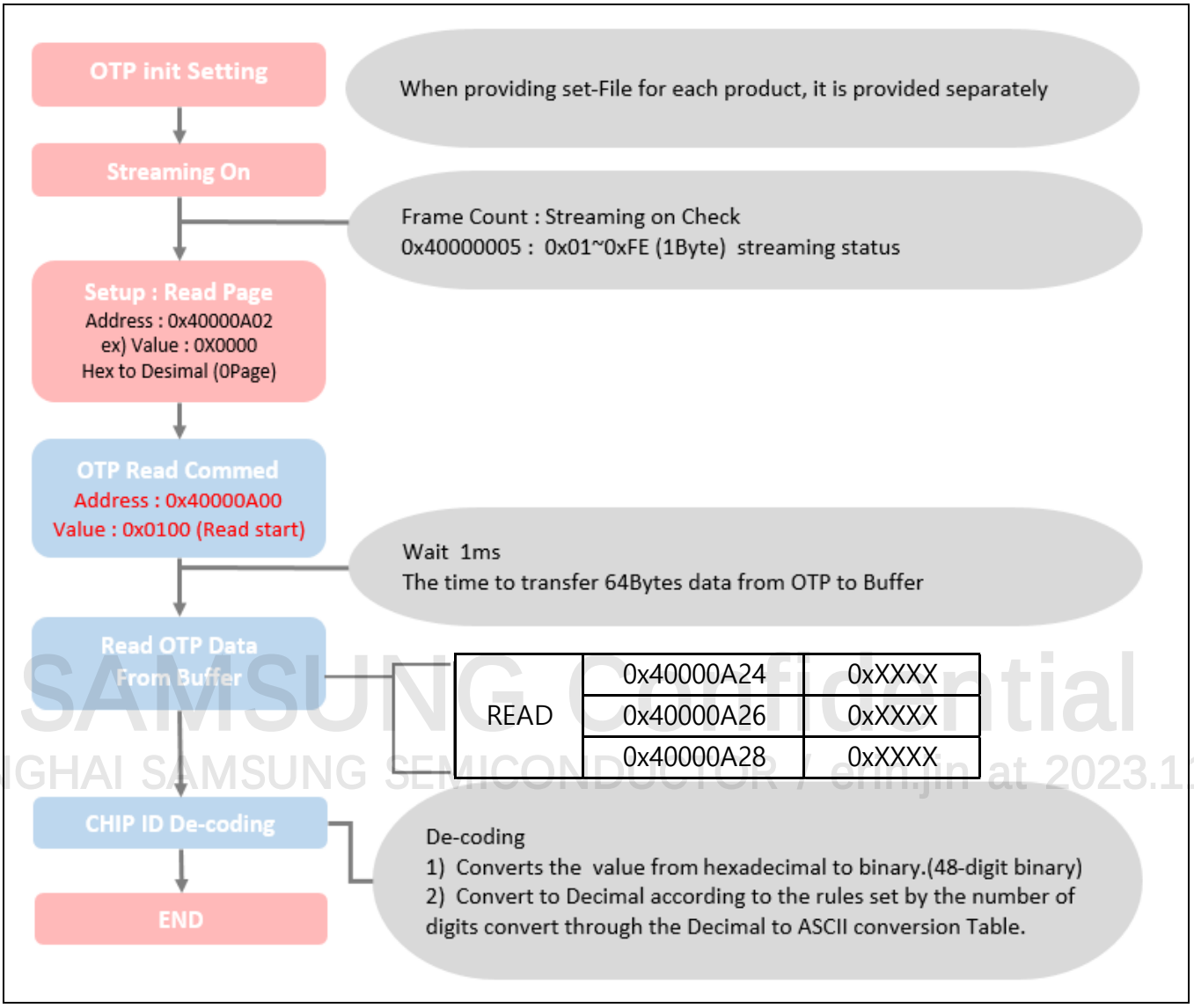


Figure 14 NVM Write Sequence

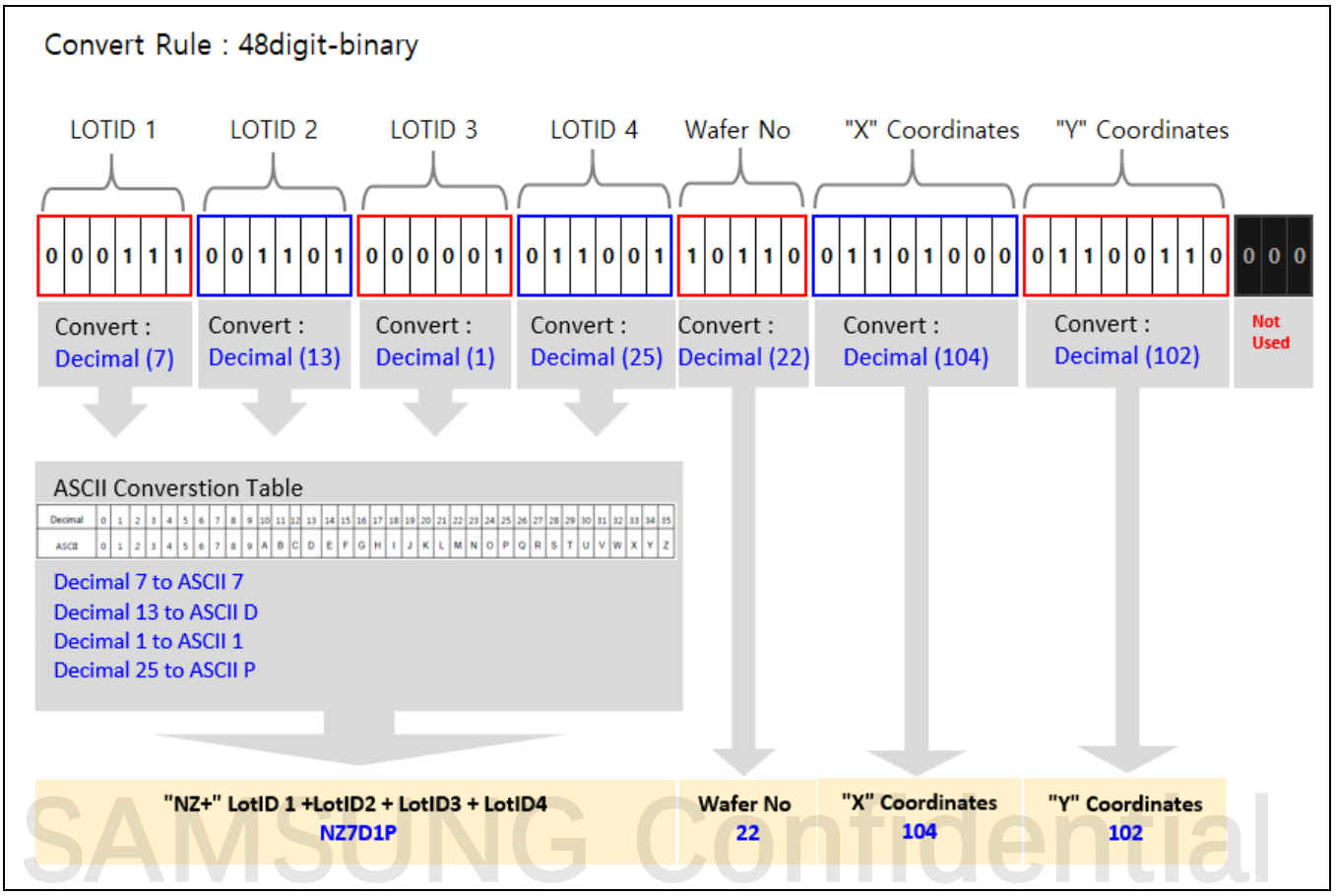
18.6 Example Read Chip ID (written at the factory)



Example 4 Chip ID Read

18.6.1 Chip ID De-coding example

1. Converts the value from hexadecimal to binary. (48-digit binary)
2. The digit conversion rule is as follows.
3. Converts through the Decimal to ASCII conversion.



Example 5 Converts Chip ID

19 Embedded Data Lines

20 Deterministic Test Patterns

21 Fast Change Mode

22 Dual Slope Gain

23 Temperature Monitoring Circuit

24 PSRR

25 MIPI Interface

25.1 Overview

S5KJN5SP03 MIPI CSI-2 interface is selectable between 2 high speed serial transmission options - 4-lane differential interface with maximum bitrate of 2.5Gbps per lane (DPHY) or 3-lanes of 3-wire serial data with maximum rate of 3.5Gsps (CPHY). Either option connects the camera sensor to host process allowing high-speed image output.
S5KJN5SP03 supports all mandatory requirements in MIPI CSI-2 version 2.10, CPHY version 1.2 and DPHY version 2.1 specifications. Please see MIPI Alliance CSI-2 1.3 specification for details.

Following are the main features of MIPI CSI-2:

- RAW8 and RAW10 and RAW12 data types
- Data output types
  - Video stream
  - PDAF stream
  - Embedded lines (Ydata, Statistics)
- Integrated MIPI DPHY
- MIPI transmit only
- Up to four data lanes and one clock lane
- Swap in MIPI data lanes
- Ultra Low Power Status Mode MIPI I/F General Control Registers (default: ULPS On)

25.1.1 DPHY Control

S5KJN5SP03 MIPI CSI-2 DPHY interface is a four-lane high-speed serial interface that connects a mobile display

driver or a camera sensor to a host processor. MIPI core IP is compatible with the MIPI Alliance Standards for DPHY, CSI2, and DSI. A bi-directional low-power mode data transmission capability has been implemented.

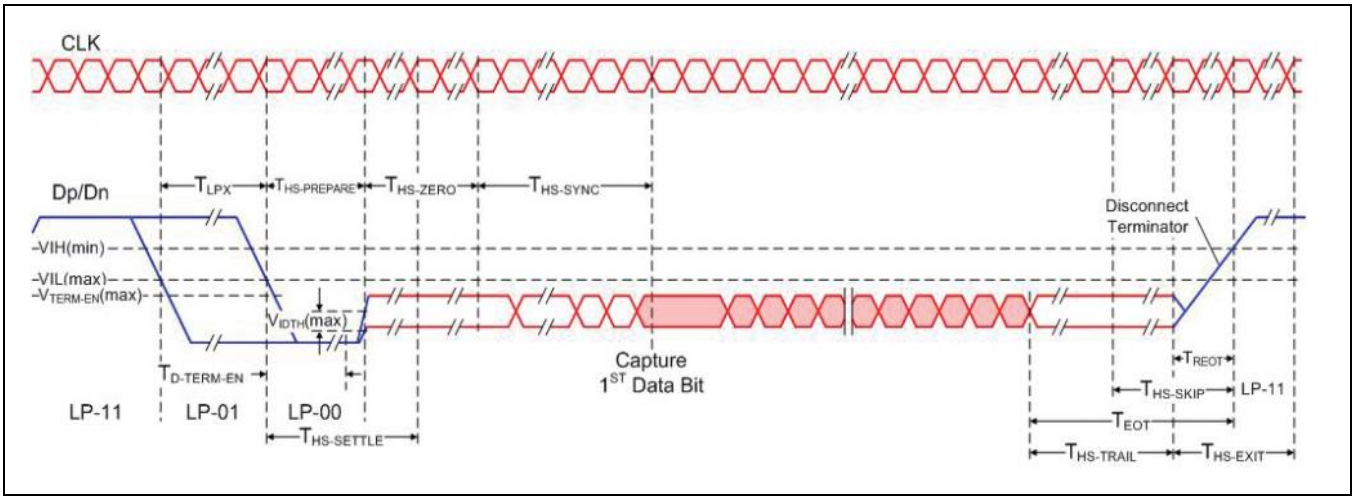


Figure 15 Modes and States in a D-PHY Data lane.

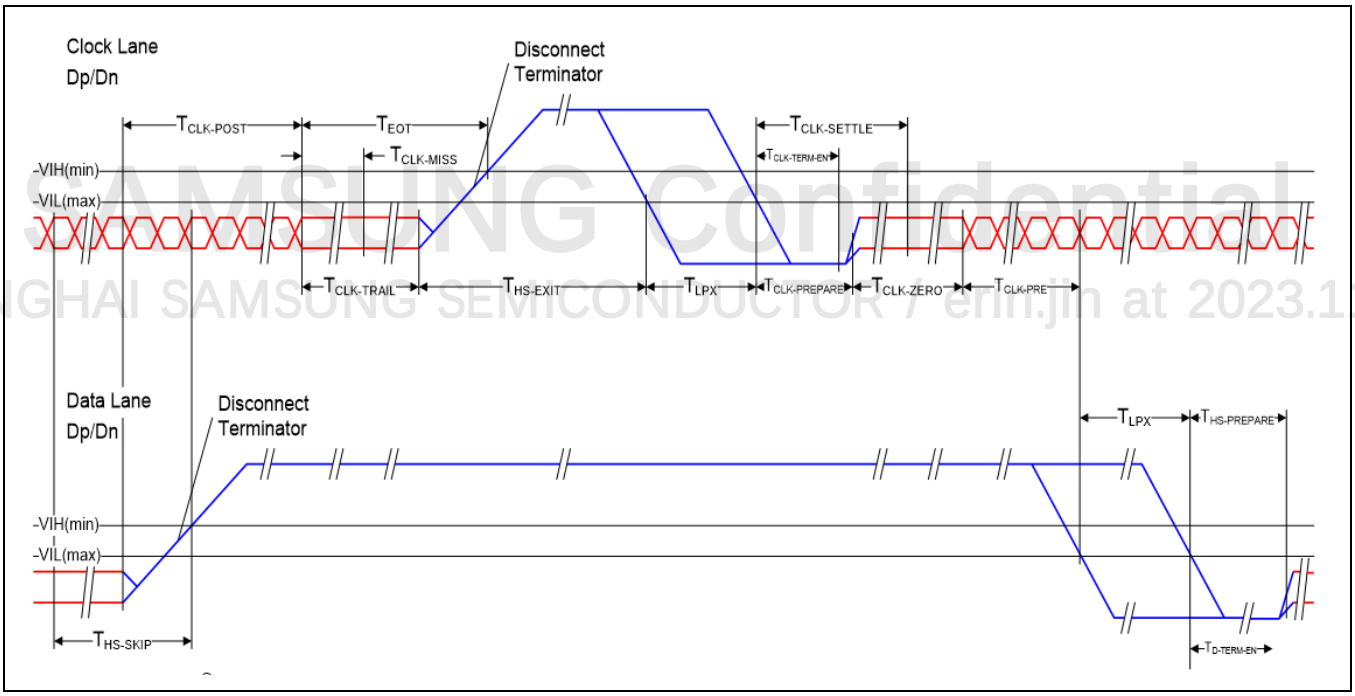


Figure 16 Modes and States in a D-PHY Clock lane.

25.1.1.1 DPHY Timing Control

Name	Address	Assigned	Default	Description

		Byte	Value	
Dphy timing tclk post	0x4000080E	1	0x00	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode.
Dphy timing tclk prepare	0x40000813	1	0x00	Time to drive LP-00 to prepare for HS clock transmission.
Dphy timing hs preamble	0x4000081A	1	0x00	HS preamble

25.1.1.2 VOD Level Control

Guide: 'Regulator output level value' recommend using the default values. Using other values after testing requires discussion with the MIPI IP designer.

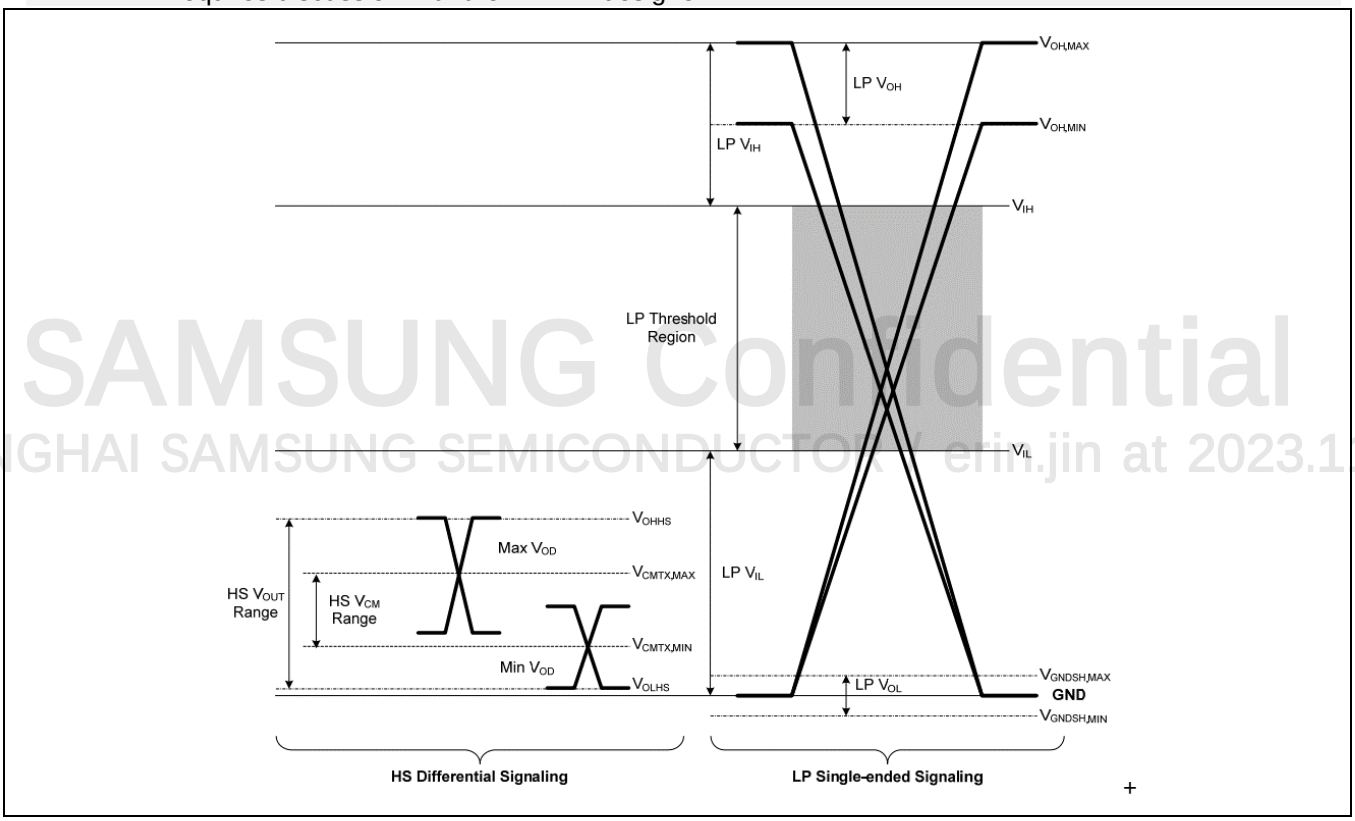


Figure 17 DPHY Signaling Level

Mode	Address	Assigned Bit [3:0]	Effect	Description
HS Mode	0x40008E48	4'b 0000	400mV : default	HS-TX Regulator Output Level
		4'b 0011	420mV	
		4'b 0100	440mV	

		4’b 1101	460mV	
		4’b 1111	500mV	
		4’b 0001	380mV	
LP Mode	0x40008E4A	3’b 000	1.10V : default	LP-TX Regulator Output Level
		3’b 001	1.13V	
		3’b 010	1.16V	
		3’b 011	1.18V	
		3’b 100	1.21V	
		3’b 101	1.02V	
		3’b 110	1.05V	
		3’b 111	1.07V	

25.1.1.3 HS-TX Impedance Control

Mode	Address	Assigned Bit [3:0]	Effect	Description
HS Mode	0x40008E3C Data0[11:8] 0x40008E3E Data1[11:8] 0x40008E42 Data2[11:8] 0x40008E44 Data3[11:8] 0x40008E40 CLK[11:8]	4’b 0000	49.0 Ω	HS-TX Driver Termination Impedance Control (up-side, For each channel) Data Impedance : D/C PHY Control Same value Don't care "Clock Lane" at CPHY
		4’b 0001	50.8 Ω	
		4’b 0010	52.6 Ω	
		4’b 0011	54.7 Ω	
		4’b 0100	57.0 Ω	
		4’b 0101	59.5 Ω	
		4’b 0110	62.4 Ω	
		4’b 0111	65.6 Ω	
		4’b 1000	39.7 Ω	
		4’b 1001	40.2 Ω	
		4’b 1010	41.2 Ω	
		4’b 1011	42.3 Ω	
		4’b 1100	43.4 Ω	
		4’b 1101	46.0 Ω	
		4’b 1110	47.5 Ω	
		4’b 1111	49.0 Ω	
	0x40008E3C Data0[15:12] 0x40008E3E Data1[15:12] 0x40008E42 Data2[15:12] 0x40008E44 Data3[15:12] 0x40008E40 CLK[15:12]	4’b 0000	49.3 Ω	HS-TX Driver Termination Impedance Control (Down-side, For each channel) Data Impedance : D/C PHY Control Same value Don't care "Clock Lane" at CPHY
		4’b 0001	51.1 Ω	
		4’b 0010	53.0 Ω	
		4’b 0011	55.0 Ω	
		4’b 0100	57.3 Ω	
		4’b 0101	59.9 Ω	
		4’b 0110	62.7 Ω	

		4'b 0111	65.9 Ω	
		4'b 1000	39.6 Ω	
		4'b 1001	40.6 Ω	
		4'b 1010	41.6 Ω	
		4'b 1011	43.8 Ω	
		4'b 1100	45.1 Ω	
		4'b 1101	46.4 Ω	
		4'b 1110	47.9 Ω	
		4'b 1111	49.3 Ω	

25.1.1.4 Tr/Tf Control

Mode	Address	Assigned Bit [3:0]	Effect	Description
HS Mode	0x40008E38 CLK [4] 0x40008E38 Data0[0] 0x40008E38 Data1[1] 0x40008E38 Data2[2] 0x40008E38 Data3[3]	5'b 00000	Off	Enable for **CLK**LANE Enable for **DATA**LANE 0/1/2/3
		5'b 11111	On	
	0x40008E40 CLK[3:0] 0x40008E3C Data0[3:0] 0x40008E3E Data1[3:0] 0x40008E42 Data2[3:0] 0x40008E44 Data3[3:0]	4'b 0000	0 tab : default	Control : Cap Peaking Control for **CLK**LANE Cap Peaking Control for **DATA**LANE 0/1/2/3
		4'b 0011	+3 tab	
		4'b 0101	+5 tab	
		4'b 0111	+7 tab	
		4'b 1101	+10 tab	
		4'b 1110	+12 tab	

25.1.1.5 LP-TX Slew Rate Control

Mode	Address	Assigned Bit	Effect	Description
LP Mode	0x40008E4C[4:0]	5'b 00000	-	LP-TX Slew Rate Up Control • 5'b00000 = All No Change (Default) • 5'b11111 = All Slew Rata UP
	0x40008E4E[4:0]	5'b 00000	-	LP-TX Slew Rate Down Control • 5'b00000 = All No Change (Default) • 5'b11111 = All Slew Rata UP

25.1.1.6 De-emphasis Control

Mode	Address	Assigned Bit	Effect	Description
HS Mode	0x40008E40 CLK[5:4] 0x40008E3C Data0 [5:4] 0x40008E3E Data1 [5:4] 0x40008E42 Data2 [5:4] 0x40008E44 Data3 [5:4]	2'b 00	0dB : default	De-emphasis(TXEQ) Enable
		2'b 01	-1.6dB	
		2'b 10	-3.5dB	
		2'b 11	-6dB	

25.1.2 CPHY Control

S5KJN5SP03 MIPI CSI-2 CPHY is an embedded clock link that provides extreme flexibility to reallocate the lanes within a link.

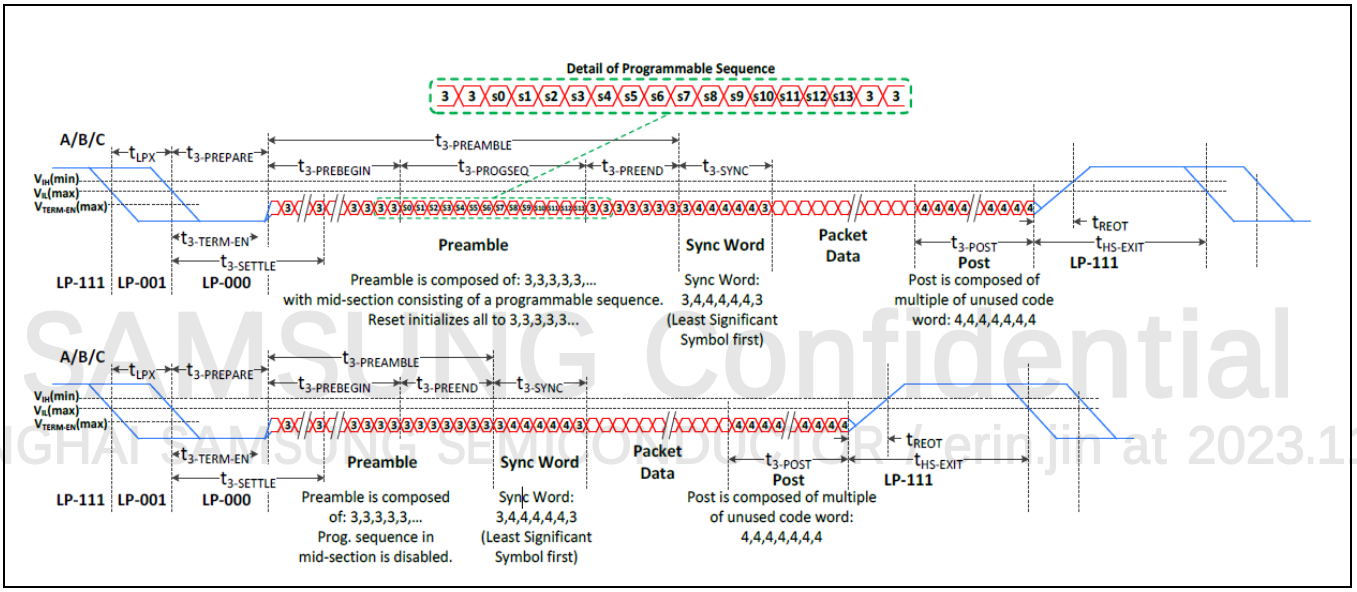


Figure 18 High-Speed Data Transmission in Burst

25.1.2.1 CPHY Timing Control

Name	Address	Assigned Byte	Default Value	Description
Cphy_timing_ths_prepare	0x4000081C	1	0x00	THS-PREPARE, is the time to drive LP-000 before starting the HS transmission on a Data Lane.
Cphy_timing_ths_preamble_ctl	0x4000081D	1	0x00	
Cphy_timing_hs_post_ctl	0x4000081E	1	0x00	Time to drive HS differential state after last payload clock bit of a HS transmission burst.
Cphy_timing_tlpx	0x4000081F	1	0x00	Length of any Low-Power state period.
Cphy_timing_ths_exit	0x40000820	1	0x00	

25.1.2.2 VOD Level Control

Guide: 'Regulator output level value' recommend using the default values. Using other values after testing requires discussion with the MIPI IP designer.

Mode	Address	Assigned Bit [3:0]	Effect	Description
HS Mode	0x40008E48	4'b 0000	450mV : default	HS-TX Regulator Output Level
		4'b 0010	400mV	
		4'b 0001	420mV	
		4'b 0110	440mV	
		4'b 1111	460mV	
		4'b 1100	480mV	
		4'b 1101	500mV	
		4'b 1010	520mV	
		4'b 1011	540mV	
LP Mode	0x40008E4A	4'b 0000	1.10V: default	LP-TX Regulator Output Level
		4'b 0001	1.13V	
		4'b 0010	1.16V	
		4'b 0011	1.18V	
		4'b 0100	1.21V	
		4'b 0101	1.02V	
		4'b 0111	1.07V	

25.1.2.3 Tr/Tf Control

Mode	Address	Assigned Bit [3:0]	Effect	Description
HS Mode	0x40008E38 CLK [4] 0x40008E38 Data0[0] 0x40008E38 Data1[1] 0x40008E38 Data2[2] 0x40008E38 Data3[3]	5'b 00000	Off	Enable for **CLK**LANE Enable for **DATA**LANE 0/1/2/3
		5'b 11111	On	
	0x40008E40 CLK[3:0] 0x40008E3C Data0[3:0] 0x40008E3E Data1[3:0] 0x40008E42 Data2[3:0] 0x40008E44 Data3[3:0]	4'b 0000	0 tab : default	Control : Cap Peaking Control for **CLK**LANE Cap Peaking Control for **DATA**LANE 0/1/2/3
		4'b 0011	+3 tab	
		4'b 0101	+5 tab	
		4'b 0111	+7 tab	

25.1.2.4 LP-TX Slew Rate Control

Mode	Address	Assigned Bit	Effect	Description
LP Mode	0x40008E4C[4:0]	5'b 00000	-	LP-TX Slew Rate Up Control • 5'b00000 = All No Change (Default) • 5'b11111 = All Slew Rata UP

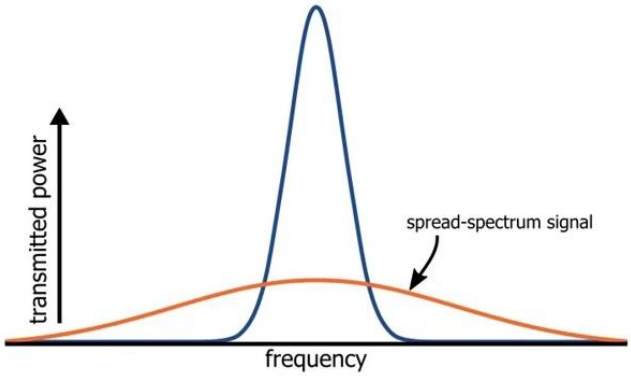
	0x40008E4E[4:0]	5'b 00000	-	LP-TX Slew Rate Down Control • 5'b00000 = All No Change (Default) • 5'b11111 = All Slew Rata UP
	0x40008E4C Data0[6:5] 0x40008E4C Data1[8:7] 0x40008E4C Data2[12:11] 0x40008E4C Data3[14:13]	10'b 0000000000	All Min :default	Don't care "Clock Lane" at CPHY
		10'b 1111111111	All Max	
	0x40008E4E Data0[6:5] 0x40008E4E Data1[8:7] 0x40008E4E Data2[12:11] 0x40008E4E Data3[14:13]	10'b 0000000000	All Min :default	Don't care "Clock Lane" at CPHY • 2'b00 = No Change (Default) • 2'b01 = Decrease about 15% • 2'b10 = Decrease about 15% • 2'b11 = Decrease about 30%
		10'b 1111111111	All Max	

25.1.2.5 De-emphasis Control

Mode	Address	Assigned Bit	Effect	Description
HS Mode	0x40008E40 CLK[5:4] 0x40008E3C Data0 [5:4] 0x40008E3E Data1 [5:4] 0x40008E42 Data2 [5:4] 0x40008E44 Data3 [5:4]	2'b 00	0dB : default	De-emphasis(TXEQ) Enable
		2'b 11	-3.5dB	

25.2 SSCG (Spread spectrum Clock Generation)

The spread spectrum clock generator (SSCG) reduces radiated emissions by spreading the emissions over a wider frequency band. SSCG has been demonstrated to reduce peak radiation. The SSCG radiated emissions by spreading the emissions over a wider frequency band.



Spread Spectrum clock generation

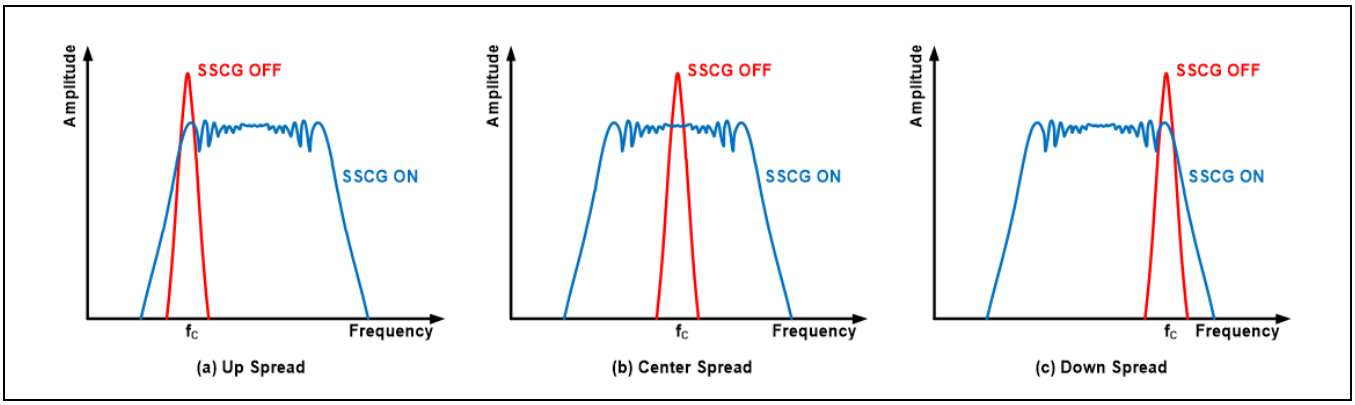


Figure 19 Spread spectrum clock generation

Name	Address	Assigned Byte	Default Value	Description
SSCG enable	0x2000231E	1	0x00	0x00 : Off 0x01 : On
SSCG sel pf	0x2000231F	1	0x00	0x00 : down spread, 0x01 : up spread, 0x10 : center spread

25.3 Frequency Hopping

Electromagnetic interference (EMI) issues are caused by overlap with other bands and sensor operating frequencies and cause communication failures. If the sensor's operating frequency cannot be changed, EMI can be avoided by frequency hopping. Frequency hopping is a method of transmitting wireless signals by rapidly switching the carrier between multiple frequencies by changing the clock settings without resetting the sensor. Hopping shifts the sensor's clock at the moment of overlap. It can be changed in a range of ±2.5% of the operating clock.

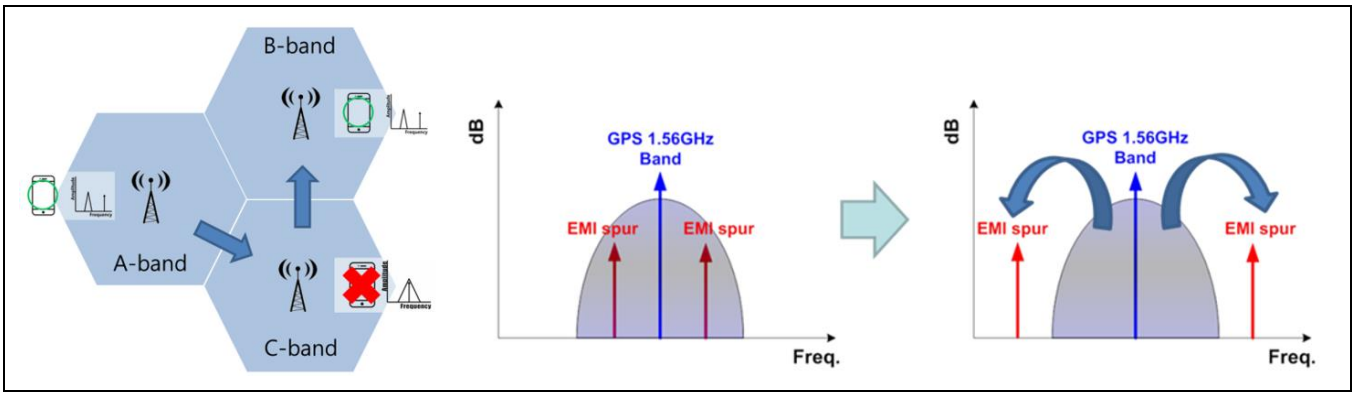


Figure 20 Introduction to Frequency Hopping

Frequency hopping is a method of transmitting radio signals in IP by rapidly switching carriers between multiple frequencies using PLL divider sequence changes without a reset signal. Frequency hopping can change the frequency by controlling the value of M (the PLL multiplier), which must change within ±2.5% without a reset to prevent instability of the PLL. The frequency hopping sequence is terminated after sufficient time (at least 75 us) has elapsed for the frequency to stabilize. The frequency hopping function must operate during the V-Blank period.

Name	Address	Assigned Byte	Default Value	Description
Freq hopping enable	0x40000328	1	0x00	0x00: disable 0x01: enable This register must be enabled before the streaming on.
Hopping pll m shift on	0x40000329	1	0x00	Request for MIPI PLL frequency hopping 0x00 = Use 'default' MIPI PLL M 0x01 = Use shifted MIPI PLL M If set only before EOF(end of frame), it will be applied to that frame.
Hopping pll m shift val	0x20002520	1	0x01	positive integer or negative integer(2's complement) ※ Need to consider min/max limitation depending on the PLL

26 PDAF Guide

26.1 Y data information

26.1.1 AF Output

	Full	4sum
LR Kernel	4x8	2x4

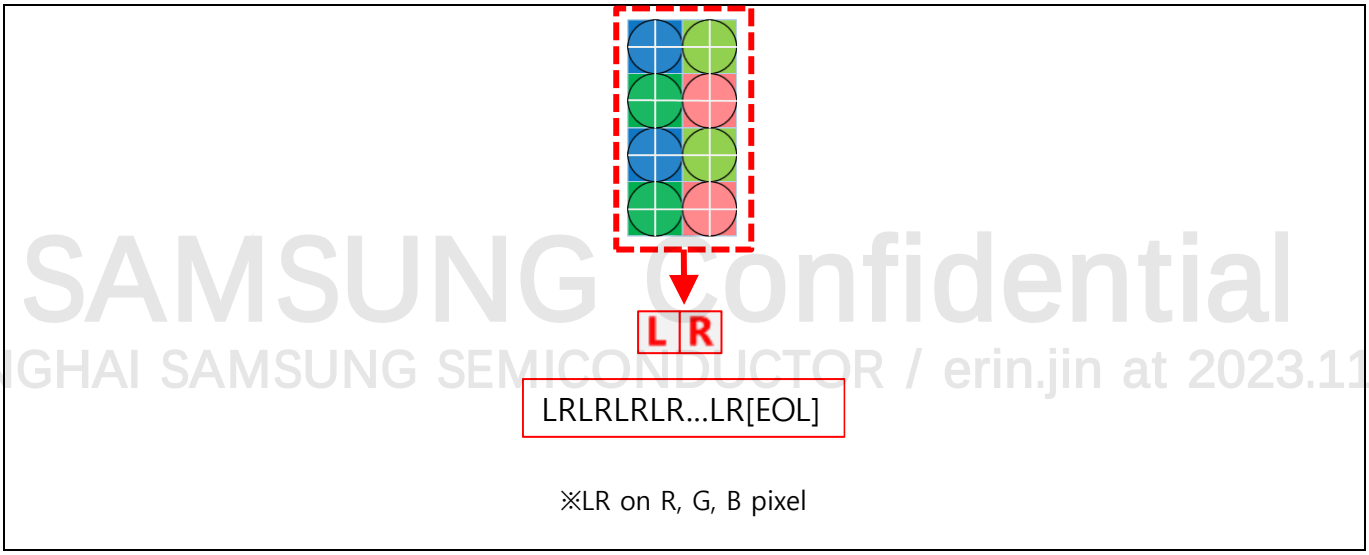


Figure 21 Full Mode

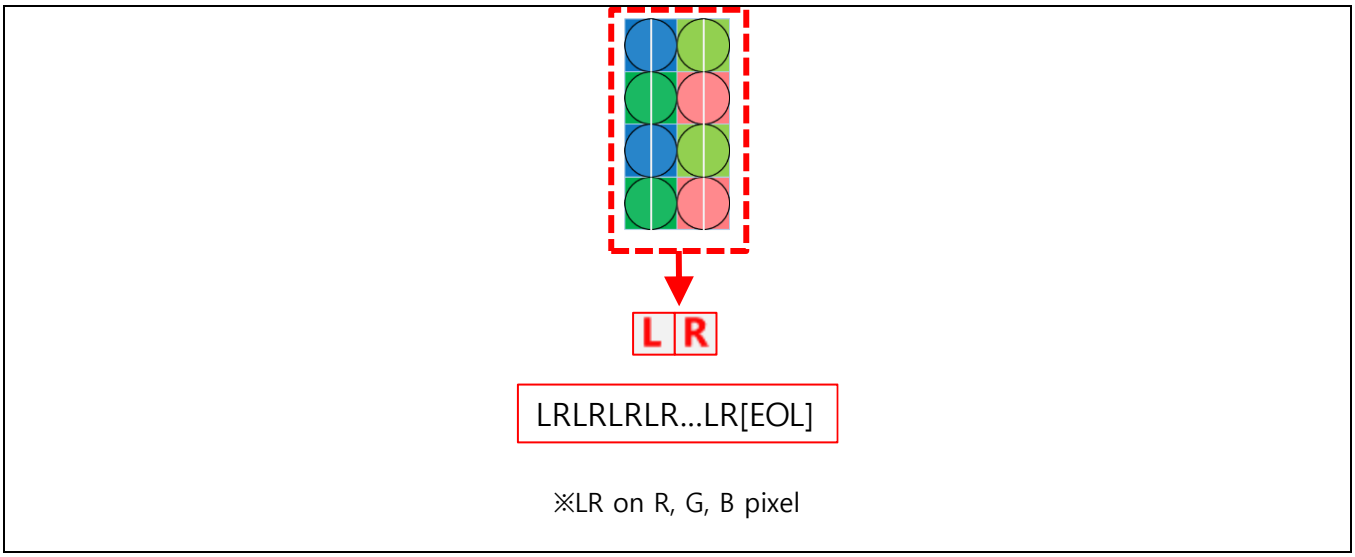


Figure 22 4sum Mode

26.2 Output Size

	Output Size		Tail Size	
	X	Y	X	Y
Full	8192	6144	4096	768
4Sum	4096	3072	4096	768

26.2.1 MIPI frame structure

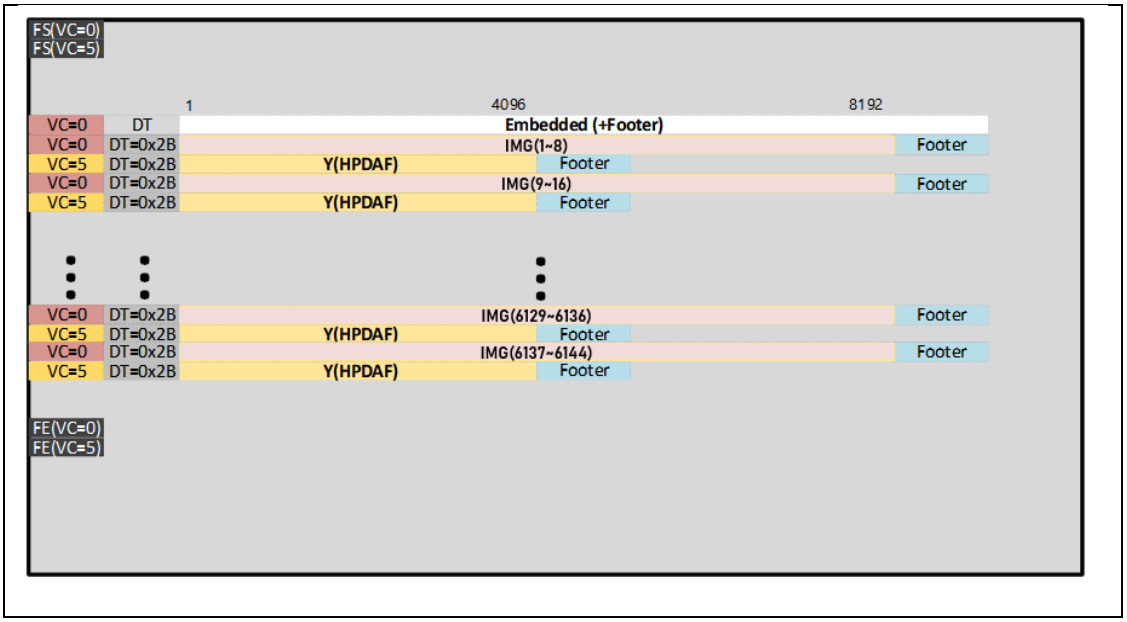


Figure 23 Full Mode with Normal mode Y data transmission

Caution: Even if crop the image, PDAF size can remain using dummy

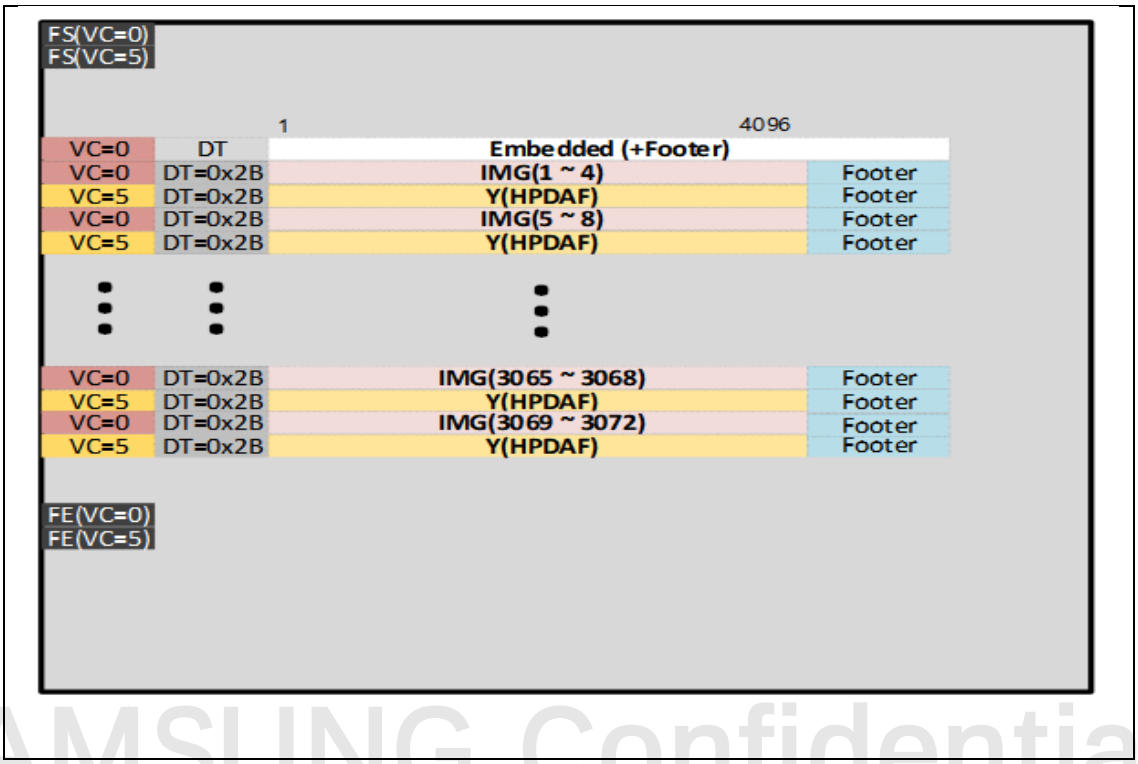


Figure 24 4sum Mode with Normal mode Y data transmission

FS(VC=0)
FS(VC=5)

		1	512		8192
VC	DT			Embedded (+ Footer)	
VC=0	DT=0x2B			IMG1	Footer
VC=5	DT=0x2B	Y1_1(HPDAF)	Footer		
VC=0	DT=0x2B			IMG2	Footer
VC=5	DT=0x2B	Y1_2(HPDAF)	Footer		
VC=0	DT=0x2B			IMG3	Footer
VC=5	DT=0x2B	Y1_3(HPDAF)	Footer		
VC=0	DT=0x2B			IMG4	Footer
VC=5	DT=0x2B	Y1_4(HPDAF)	Footer		
VC=0	DT=0x2B			IMG5	Footer
VC=5	DT=0x2B	Y1_5(HPDAF)	Footer		
VC=0	DT=0x2B			IMG6	Footer
VC=5	DT=0x2B	Y1_6(HPDAF)	Footer		
VC=0	DT=0x2B			IMG7	Footer
VC=5	DT=0x2B	Y1_7(HPDAF)	Footer		
VC=0	DT=0x2B			IMG8	Footer
VC=5	DT=0x2B	Y1_8(HPDAF)	Footer		
⋮	⋮			⋮	⋮
VC=0	DT=0x2B			IMG6137	Footer
VC=5	DT=0x2B	Y768_1(HPDAF)	Footer		
VC=0	DT=0x2B			IMG6138	Footer
VC=5	DT=0x2B	Y768_2(HPDAF)	Footer		
VC=0	DT=0x2B			IMG36139	Footer
VC=5	DT=0x2B	Y768_3(HPDAF)	Footer		
VC=0	DT=0x2B			IMG6140	Footer
VC=5	DT=0x2B	Y768_4(HPDAF)	Footer		
VC=0	DT=0x2B			IMG6141	Footer
VC=5	DT=0x2B	Y768_5(HPDAF)	Footer		
VC=0	DT=0x2B			IMG6142	Footer
VC=5	DT=0x2B	Y768_6(HPDAF)	Footer		
VC=0	DT=0x2B			IMG6143	Footer
VC=5	DT=0x2B	Y768_7(HPDAF)	Footer		
VC=0	DT=0x2B			IMG6144	Footer
VC=5	DT=0x2B	Y768_8(HPDAF)	Footer		

FE(VC=0)
FE(VC=5)

Figure 25 Full Mode with Split mode Y data transmission (n=8)

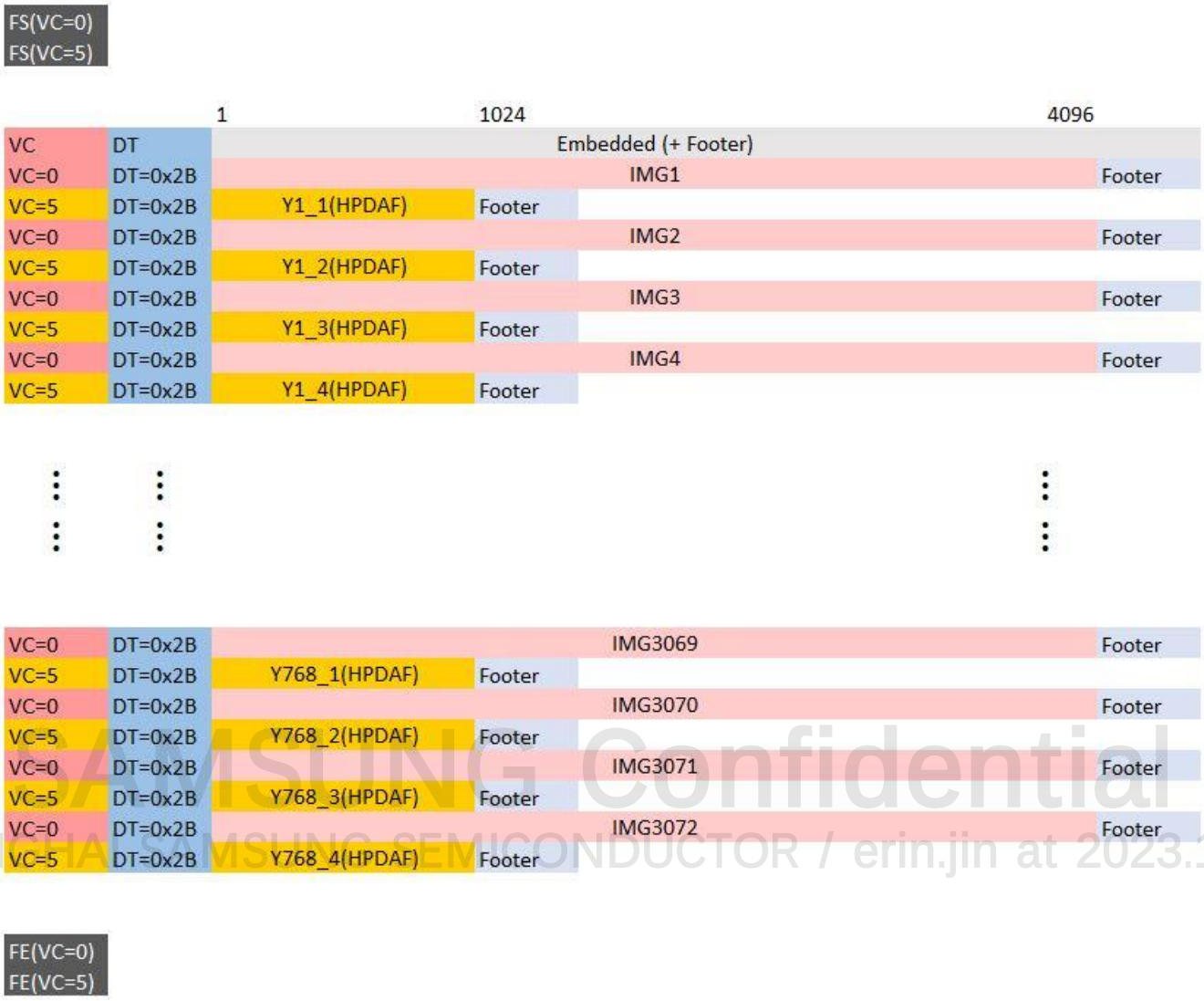


Figure 26 4sum Mode with Split mode Y data transmission (n=4)

26.3 Limitation

Table 10 Limitation

PDAF(H)	Full	4sum
Y size	8N	8N

26.4 Y Data Format

Y streaming data can be distinguished using VC or DT

Table 11 Y Data Format

Name	Address	Assigned Byte	Default Value	Description
Y_stream_enable	0x40000720	2	0x0000	0x0000 : disable 0x0001 : enable
Y_stream_output_mode	0x40000724	2	0x0000	0x0000 : LR
Output_virtual_channel_ydata_0	0x40000264	1	0x05	Virtual channel control
Output_virtual_channel_ydata_1	0x40000265	1	0x06	Not used in JN5
Output_data_type_ydata_0	0x40000274	1	0x2B	Data type control
Output_data_type_ydata_1	0x40000275	1	0x2B	Not used in JN5

26.5 Y Data Equation

$$Y_L(y,x) = \frac{1}{N_{LR}}\left(C_{g0}\sum_{\substack{j=even,\\ 4x\le j<4(x+1),\\ 8y\le i<8(y+1)}} Gr(i,j) + C_{g1}\sum_{\substack{j=even,\\ 4x\le j<4(x+1),\\ 8y\le i<8(y+1)}} Gb(i,j) + C_r\sum_{\substack{j=even,\\ 4\le j<4x+1),\\ 8y\le i<8(y+1)}} R(i,j) + C_b\sum_{\substack{j=even,\\ 4x\le j<4x+1),\\ 8y\le i<8(y+1)}} B(i,j)\right) \quad where\ N_{LR} = \frac{(4\times 8)}{2}$$

$$Y_R(y,x) = \frac{1}{N_{LR}}\left(C_{g0}\sum_{\substack{j=odd,\\ 4x\le j<4(x+1),\\ 8y\le i<8(y+1)}} Gr(i,j) + C_{g1}\sum_{\substack{j=odd,\\ 4x\le j<4(x+1),\\ 8y\le i<8(y+1)}} Gb(i,j) + C_r\sum_{\substack{j=odd,\\ 4\le j<4x+1),\\ 8y\le i<8(y+1)}} R(i,j) + C_b\sum_{\substack{j=odd\\ 4x\le j<4x+1),\\ 8y\le i<8(y+1)}} B(i,j)\right)$$

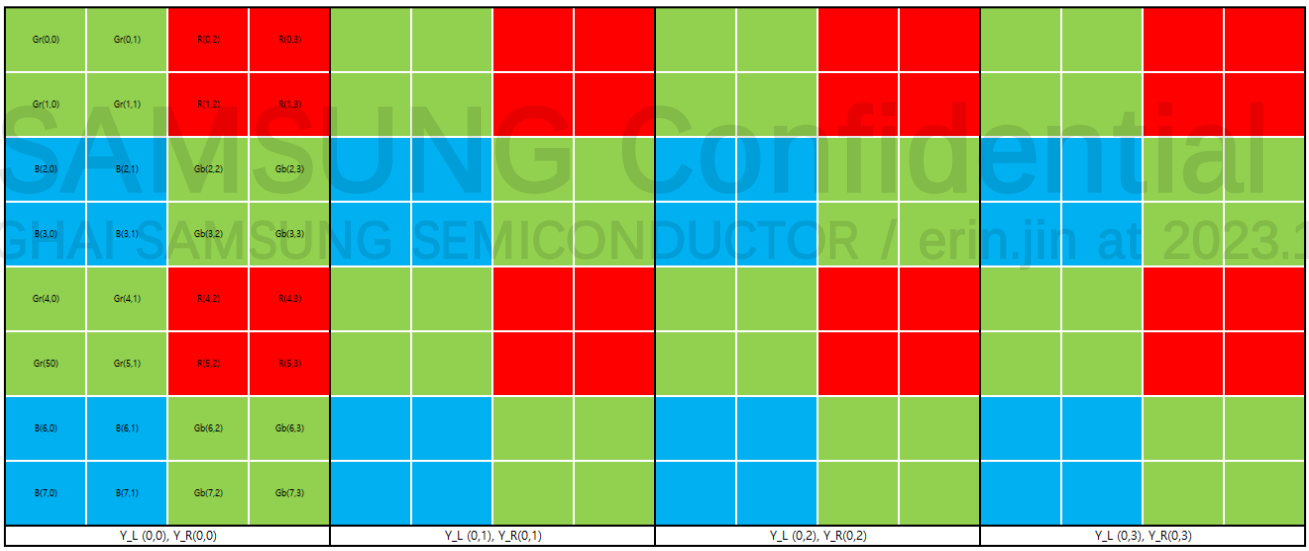


Figure 95 Full Mode Y Data Equation

$$Y_L(y,x) = \frac{1}{N_{LR}}\left(C_{g0}\sum_{\substack{j=even,\\ 4x\le j<4(x+1),\\ 4y\le i<4(y+1)}} Gr(i,j) + C_{g1}\sum_{\substack{j=even,\\ 4x\le j<4(x+1),\\ 4y\le i<4(y+1)}} Gb(i,j) + C_r\sum_{\substack{j=even,\\ 4\le j<4x+1),\\ 4y\le i<4(y+1)}} R(i,j) + C_b\sum_{\substack{j=even,\\ 4x\le j<4x+1),\\ 4y\le i<4(y+1)}} B(i,j)\right) \qquad where\ N_{LR} = \frac{(4\times 4)}{2}$$

$$Y_R(y,x) = \frac{1}{N_{LR}}\left(C_{g0}\sum_{\substack{j=odd,\\ 4x\le j<4(x+1),\\ 4y\le i<4(y+1)}} Gr(i,j) + C_{g1}\sum_{\substack{j=odd,\\ 4x\le j<4(x+1),\\ 4y\le i<4(y+1)}} Gb(i,j) + C_r\sum_{\substack{j=odd,\\ 4\le j<4x+1),\\ 4y\le i<4(y+1)}} R(i,j) + C_b\sum_{\substack{j=odd\\ 4x\le j<4x+1),\\ 4y\le i<4(y+1)}} B(i,j)\right)$$

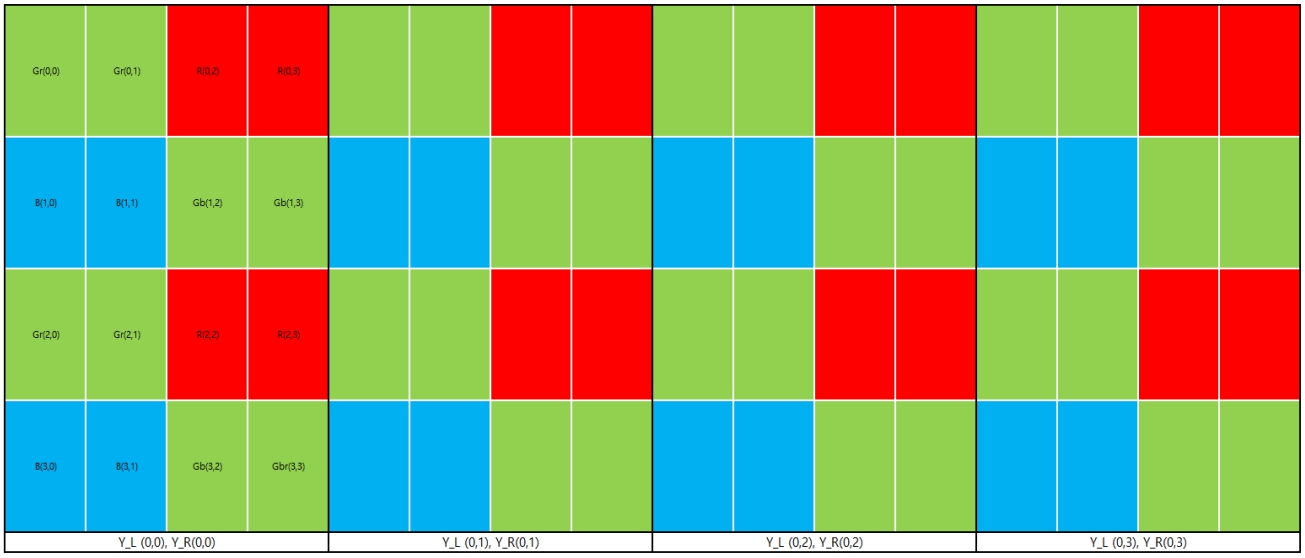


Figure 96 4Sum Mode Y Data Equation

27 Lens Position Guide For XTC

28 OIS sync

29 IBIS

29.1 Overview

We can support IBIS model for better module design.

We will provide it as simulation files.