

IMX355

MIPI D-PHY Global Timing parameters

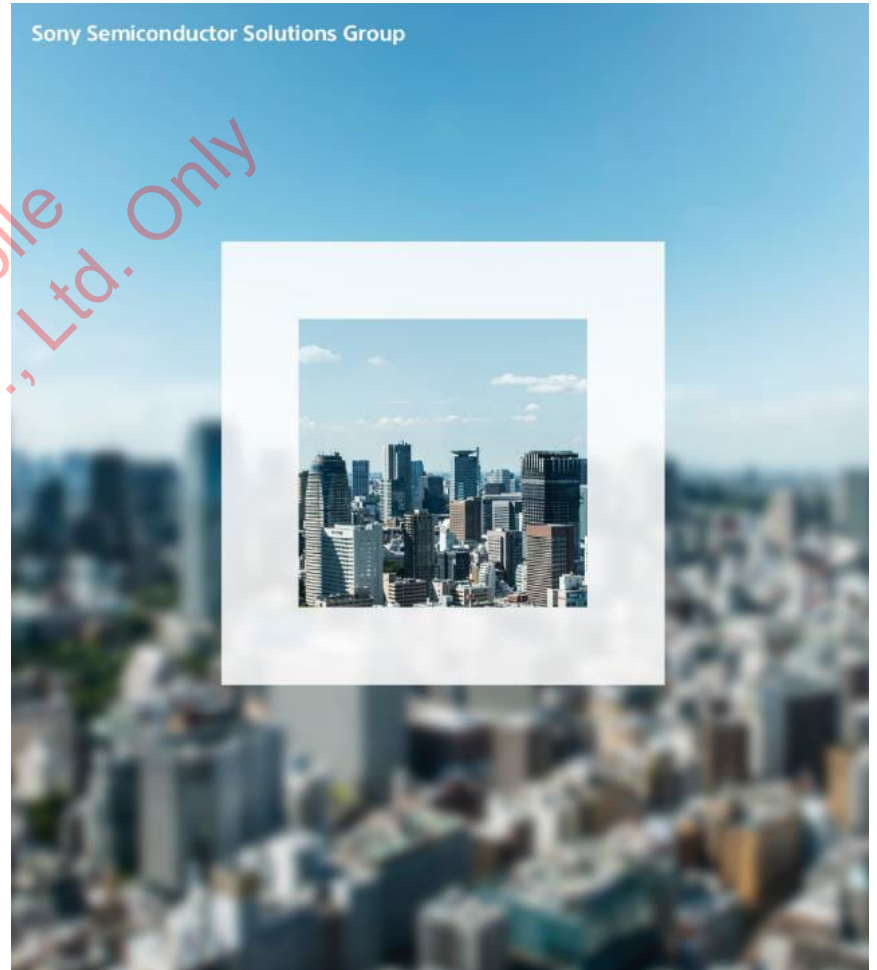
Information on additional register settings
to support MediaTek DX-1, DX-2, and DX-P

Both ($T_{HS-TRAIL} + T_{CLK-POST} \Rightarrow 224 \text{ UI}$) &
($T_{HS-TRAIL} + T_{HS-EXIT} \Rightarrow 224 \text{ UI} + 70 \text{ ns}$)

2024/02/27

Mobile System Business Division
Sony Semiconductor Solutions Corporation

Copyright 2022, 2023, 2024 Sony Semiconductor Solutions Corporation



Revision History

Version	Date	Description
1.0	Mar. 29, 2022	1 st release
1.1	July 29, 2022	Reg_D was removed, Reg_A1, Reg_B1, and Reg_I1 were added
1.2	June 13, 2023	Reg_J and Reg_K were added
1.3	Jan. 19, 2024	Reg_F1 was added
1.4	Feb. 21, 2024	Reg_F2 was added
1.5	Feb. 27, 2024	Reg_F3 and Reg_F4 were added

Additional settings for MIPI D-PHY Global Operation Timing Parameters

Dedicated information for register settings in IMX355-PQH_OPPO-DPHY-24M_RegisterSetting_ver8.0-3.01_240227.xlsx.

Additional register settings in the table below support both $T_{HS-TRAIL} + T_{CLK-POST} \Rightarrow 224 \text{ UI}$ & $T_{HS-TRAIL} + T_{HS-EXIT} \Rightarrow 224 \text{ UI} + 70 \text{ ns}$.

I ² C Write address	Register Name	reg_A 702 Mbps	reg_B 528 Mbps	reg_C 720 Mbps	reg_E 360 Mbps	reg_F 648 Mbps	reg_G 720 Mbps	reg_H 720 Mbps	reg_I 504 Mbps	reg_D1 720 Mbps	reg_A1 720 Mbps
0x0808	PHY_CTRL	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02
0x080A	TCLK_POST_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x080B	TCLK_POST_EX[7:0]	0xAF	0xB7	0xAF	0xBF	0xAF	0xAF	0xAF	0xB7	0xAF	0xAF
0x080C	THS_PREPARE_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x080D	THS_PREPARE_EX[7:0]	0x2F	0x27	0x2F	0x1F	0x2F	0x2F	0x2F	0x27	0x2F	0x2F
0x080E	THS_ZERO_MIN_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x080F	THS_ZERO_MIN_EX[7:0]	0x57	0x3F	0x57	0x2F	0x4F	0x57	0x57	0x3F	0x57	0x57
0x0810	THS_TRAIL_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0811	THS_TRAIL_EX[7:0]	0x2F	0x27	0x2F	0x1F	0x2F	0x2F	0x2F	0x27	0x2F	0x2F
0x0812	TCLK_TRAIL_MIN_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0813	TCLK_TRAIL_MIN_EX[7:0]	0x2F	0x1F	0x2F	0x17	0x27	0x2F	0x2F	0x1F	0x2F	0x2F
0x0814	TCLK_PREPARE_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0815	TCLK_PREPARE_EX[7:0]	0x2F	0x1F	0x2F	0x17	0x27	0x2F	0x2F	0x1F	0x2F	0x2F
0x0816	TCLK_ZERO_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0817	TCLK_ZERO_EX[7:0]	0xBF	0x8F	0xBF	0x6F	0xB7	0xBF	0xBF	0x8F	0xBF	0xBF
0x0818	TLPX_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0819	TLPX_EX[7:0]	0x27	0x1F	0x27	0x17	0x27	0x27	0x27	0x1F	0x27	0x27
0x30A2	THS_EXIT[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x30A3	THS_EXIT[7:0]	0xE3	0xDD	0xE3	0xDD	0xDF	0xE3	0xE3	0xDD	0xE3	0xE3
0x30A0	TCLK_PRE[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x30A1	TCLK_PRE[7:0]	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F

Note: Any of register writes need to be done during SW-standby.

Additional settings for MIPI D-PHY Global Operation Timing Parameters (Cont'd)

Dedicated information for register settings in IMX355-PQH_OPPO-DPHY-24M_RegisterSetting_ver8.0-3.01_240227.xlsx.

Additional register settings in the table below support both $T_{HS-TRAIL} + T_{CLK-POST} \Rightarrow 224 \text{ UI}$ & $T_{HS-TRAIL} + T_{HS-EXIT} \Rightarrow 224 \text{ UI} + 70 \text{ ns}$.

I ² C Write address	Register Name	reg_B1 720 Mbps	reg_I1 720 Mbps	reg_J 552 Mbps	reg_K 720 Mbps	reg_F1 720 Mbps	reg_F2 600 Mbps	reg_F3 684 Mbps	reg_F4 498 Mbps
0x0808	PHY_CTRL	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02
0x080A	TCLK_POST_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x080B	TCLK_POST_EX[7:0]	0xAF	0xAF	0xB7	0xAF	0xAF	0xAF	0xAF	0xB7
0x080C	THS_PREPARE_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x080D	THS_PREPARE_EX[7:0]	0x2F	0x2F	0x27	0x2F	0x2F	0x2F	0x2F	0x27
0x080E	THS_ZERO_MIN_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x080F	THS_ZERO_MIN_EX[7:0]	0x57	0x57	0x47	0x57	0x57	0x4F	0x57	0x3F
0x0810	THS_TRAIL_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0811	THS_TRAIL_EX[7:0]	0x2F	0x2F	0x27	0x2F	0x2F	0x2F	0x2F	0x27
0x0812	TCLK_TRAIL_MIN_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0813	TCLK_TRAIL_MIN_EX[7:0]	0x2F	0x2F	0x27	0x2F	0x2F	0x27	0x2F	0x1F
0x0814	TCLK_PREPARE_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0815	TCLK_PREPARE_EX[7:0]	0x2F	0x2F	0x27	0x2F	0x2F	0x27	0x2F	0x1F
0x0816	TCLK_ZERO_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0817	TCLK_ZERO_EX[7:0]	0xBF	0xBF	0x9F	0xBF	0xBF	0xB7	0xBF	0x8F
0x0818	TLPX_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0819	TLPX_EX[7:0]	0x27	0x27	0x1F	0x27	0x27	0x27	0x27	0x1F
0x30A2	THS_EXIT[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x30A3	THS_EXIT[7:0]	0xE3	0xE3	0xE1	0xE3	0xE3	0xDF	0xE3	0xDD
0x30A0	TCLK_PRE[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x30A1	TCLK_PRE[7:0]	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F

Note: Any of register writes need to be done during SW-standby.

SONY

CONFIDENTIAL
Guangdong OPPO Mobile
Telecommunications Corp., Ltd. Only

SONYはソニー株式会社の登録商標または商標です。

各ソニー製品の商品名・サービス名はソニー株式会社またはグループ各社の登録商標または商標です。その他の製品および会社名は、各社の商号、登録商標または商標です。