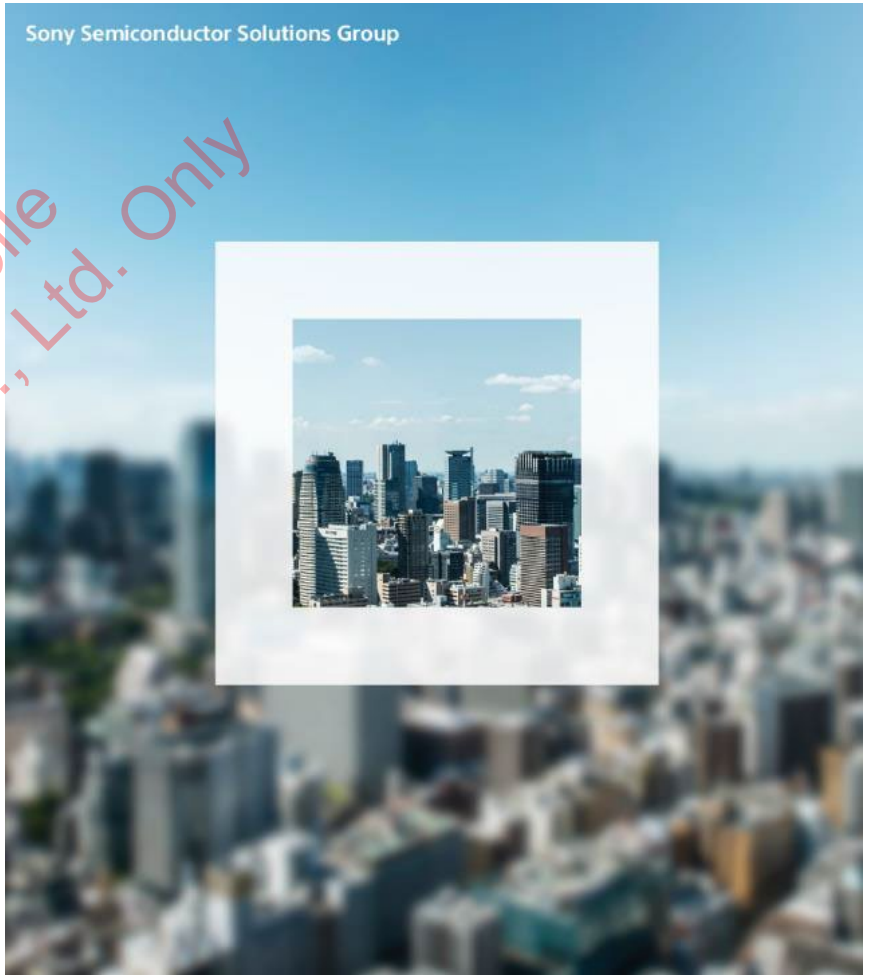
SONY

IMX355
MIPI D-PHY Global Timing parameters

Information on additional register settings to support MediaTek DX-1, DX-2, and DX-P

Both ($T_{HS\text{-}TRAIL}$ + $T_{CLK\text{-}POST}$ => 224 UI) &
($T_{HS\text{-}TRAIL}$ + $T_{HS\text{-}EXIT}$ => 224 UI + 70 ns)



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Mobile System Business Division
Sony Semiconductor Solutions Corporation

Revision History

Version	Date	Description
1.0	Mar. 29, 2022	1st release
1.1	July 29, 2022	Reg_D was removed, Reg_A1, Reg_B1, and Reg_I1 were added
1.2	June 13, 2023	Reg_J and Reg_K were added

Additional settings for MIPI D-PHY Global Operation Timing Parameters

Dedicated information for register settings in IMX355-PQH_OPPO-DPHY-24M_RegisterSetting_ver5.0-3.01_230613.xlsx.
Additional register settings in the table below support both $T_{HS-TRAIL} + T_{CLK-POST}$ => 224 UI & $T_{HS-TRAIL} + T_{HS-EXIT}$ => 224 UI + 70 ns.

I^2C Write address	Register Name	reg_A 702 Mbps	reg_B 528 Mbps	reg_C 720 Mbps	reg_E 360 Mbps	reg_F 648 Mbps	reg_G 720 Mbps	reg_H 720 Mbps	reg_I 504 Mbps	reg_D1 720 Mbps	reg_A1 720 Mbps
0x0808	PHY_CTRL	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02
0x080A	TCLK_POST_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x080B	TCLK_POST_EX[7:0]	0xAF	0xB7	0xAF	0xBF	0xAF	0xAF	0xAF	0xB7	0xAF	0xAF
0x080C	THS_PREPARE_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x080D	THS_PREPARE_EX[7:0]	0x2F	0x27	0x2F	0x1F	0x2F	0x2F	0x2F	0x27	0x2F	0x2F
0x080E	THS_ZERO_MIN_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x080F	THS_ZERO_MIN_EX[7:0]	0x57	0x3F	0x57	0x2F	0x4F	0x57	0x57	0x3F	0x57	0x57
0x0810	THS_TRAIL_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0811	THS_TRAIL_EX[7:0]	0x2F	0x27	0x2F	0x1F	0x2F	0x2F	0x2F	0x27	0x2F	0x2F
0x0812	TCLK_TRAIL_MIN_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0813	TCLK_TRAIL_MIN_EX[7:0]	0x2F	0x1F	0x2F	0x17	0x27	0x2F	0x2F	0x1F	0x2F	0x2F
0x0814	TCLK_PREPARE_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0815	TCLK_PREPARE_EX[7:0]	0x2F	0x1F	0x2F	0x17	0x27	0x2F	0x2F	0x1F	0x2F	0x2F
0x0816	TCLK_ZERO_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0817	TCLK_ZERO_EX[7:0]	0xBF	0x8F	0xBF	0x6F	0xB7	0xBF	0xBF	0x8F	0xBF	0xBF
0x0818	TLPX_EX[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x0819	TLPX_EX[7:0]	0x27	0x1F	0x27	0x17	0x27	0x27	0x27	0x1F	0x27	0x27
0x30A2	THS_EXIT[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x30A3	THS_EXIT[7:0]	0xE3	0xDD	0xE3	0xDD	0xDF	0xE3	0xE3	0xDD	0xE3	0xE3
0x30A0	TCLK_PRE[9:8]	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x30A1	TCLK_PRE[7:0]	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F

Note: Any of register writes need to be done during SW-standby.

Additional settings for MIPI D-PHY Global Operation Timing Parameters (Cont'd)

Dedicated information for register settings in IMX355-PQH_OPPO-DPHY-24M_RegisterSetting_ver5.0-3.01_230613.xlsx.
Additional register settings in the table below support both $T_{HS\text{-}TRAIL}$ + $T_{CLK\text{-}POST}$ => 224 UI & $T_{HS\text{-}TRAIL}$ + $T_{HS\text{-}EXIT}$ => 224 UI + 70 ns.

I^2C Write address	Register Name	reg_B1 720 Mbps	reg_I1 720 Mbps	reg_J 552 Mbps	reg_K 720 Mbps
0x0808	PHY_CTRL	0x02	0x02	0x02	0x02
0x080A	TCLK_POST_EX[9:8]	0x00	0x00	0x00	0x00
0x080B	TCLK_POST_EX[7:0]	0xAF	0xAF	0xB7	0xAF
0x080C	THS_PREPARE_EX[9:8]	0x00	0x00	0x00	0x00
0x080D	THS_PREPARE_EX[7:0]	0x2F	0x2F	0x27	0x2F
0x080E	THS_ZERO_MIN_EX[9:8]	0x00	0x00	0x00	0x00
0x080F	THS_ZERO_MIN_EX[7:0]	0x57	0x57	0x47	0x57
0x0810	THS_TRAIL_EX[9:8]	0x00	0x00	0x00	0x00
0x0811	THS_TRAIL_EX[7:0]	0x2F	0x2F	0x27	0x2F
0x0812	TCLK_TRAIL_MIN_EX[9:8]	0x00	0x00	0x00	0x00
0x0813	TCLK_TRAIL_MIN_EX[7:0]	0x2F	0x2F	0x27	0x2F
0x0814	TCLK_PREPARE_EX[9:8]	0x00	0x00	0x00	0x00
0x0815	TCLK_PREPARE_EX[7:0]	0x2F	0x2F	0x27	0x2F
0x0816	TCLK_ZERO_EX[9:8]	0x00	0x00	0x00	0x00
0x0817	TCLK_ZERO_EX[7:0]	0xBF	0xBF	0x9F	0xBF
0x0818	TLPX_EX[9:8]	0x00	0x00	0x00	0x00
0x0819	TLPX_EX[7:0]	0x27	0x27	0x1F	0x27
0x30A2	THS_EXIT[9:8]	0x00	0x00	0x00	0x00
0x30A3	THS_EXIT[7:0]	0xE3	0xE3	0xE1	0xE3
0x30A0	TCLK_PRE[9:8]	0x00	0x00	0x00	0x00
0x30A1	TCLK_PRE[7:0]	0x0F	0x0F	0x0F	0x0F

Note: Any of register writes need to be done during SW-standby.