AVR AT nega 32 mich controler A Advanced RISC Archibecture

132 * 8

130 General purpose Registers La peripheral Fealures * Two 8-bil finer * One 16-bil lines A Four PWM * 8 - Chernel 10- bil ADC # Two will serial infleture, USART, SPI & Walchday timer & for stacked loops on Anelog Comparolor L> pin configrations 32 programmable 1/0 lines L> Block dagram 1 LO AVR CPU core * Harvard architecture finemony X SRAM memory

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* Strigt Level pipeline feter & diesde

* Strigt Level ALV * Fool *

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* Slubio register "SREG" Stil each bil means a flery

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* 02 pointed to point to the address

Byolall untle + PORTA = (volable untle £*) (0x3B)

type 8-bils (6 convert (0x3B) to an address

> OR &

W 01 * (voluble unil 8 - 2*) (0x3B)) = 0x10 or #define #

/ / : DIO Programmyling الموضوع : ESAVR ATmegre 32 hers 32 pogrammable 1/0 pms # 32 pins -> 4 ports
Ls each port conluns 8 pins. [] A to couch port can be configured as general DI JC
perpos 1/0 perpos 1/0

*Cerel ph hus a specific function

*Cerel ph com be configered using 8 1/0 registers

" DORTER" "PINAN" "DOR xn", "PORTxn", "PINXn" 65 Dele direction register "DDRx" # weld lo configer each pin
** 8-bil regisler, each bil controls its muped pin SonFiguring Pin 2 in Parl A as an impul pin => DDRA &=~ (1<<2); & clear bil Lon Pigurhay pin6 in Parl A as as original pin DDRA 1= (1<<6); & sel bil 45 Port register "Port x" to used to pull each pin high"1" or low"0" Spullpin3 in ParlA Low => PORTA &=~ (1<<3) i L> N N 5 N N High => PORFA != (1<<5);

التاريخ: ١/ ١٠ الموضوع: Us Parl INpul register "PINX" * slove each pin slele high or low-level 6 Read shale of PINT in Porl A (PIN & (1 << 7)) << 7 6 10 N N N 2 N NN (PIN & (12<2)) <<2 Us Configuring the pin \$ 1/0 pms to Current * pm scales 6