



74LVC574A

Octal D-type flip-flop with 5 V tolerant inputs/outputs;
positive edge-trigger; 3-state

Rev. 7.1 — 2 November 2023

Product data sheet

1. General description

The 74LVC574A is an 8-bit positive-edge triggered D-type flip-flop with 3-state outputs. The device features a clock (CP) and output enable (\overline{OE}) inputs. The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH clock (CP) transition. A HIGH on \overline{OE} causes the outputs to assume a high-impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the flip-flops. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

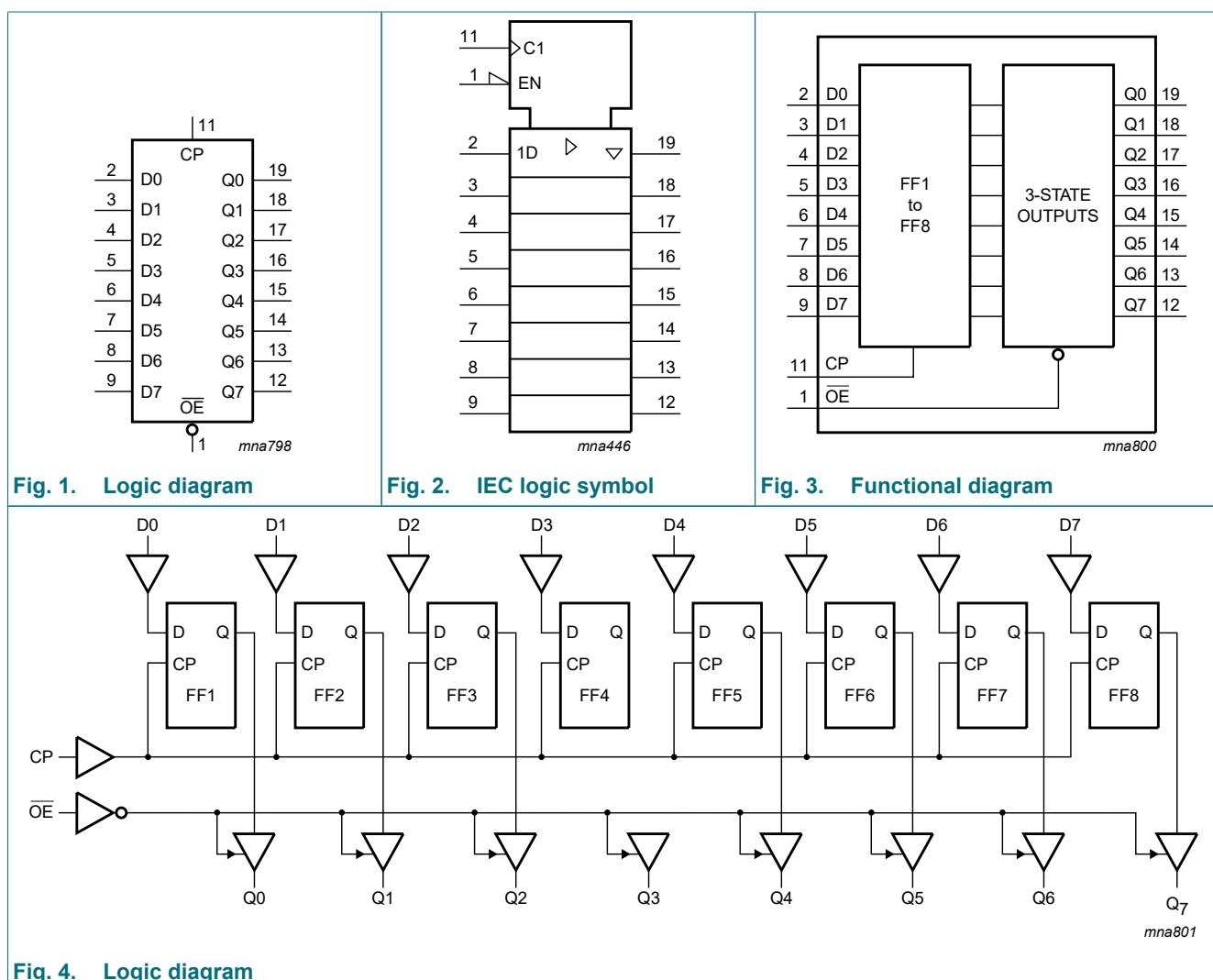
- Wide supply voltage range from 1.2 to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Overvoltage tolerant inputs to 5.5 V
- High-impedance when $V_{CC} = 0$ V
- 8-bit positive edge-triggered register
- Independent register and 3-state buffer operation
- Flow-through pin-out architecture
- I_{OFF} circuitry provides partial Power-down mode operation
- Complies with JEDEC standard:
 - JESD8-7A (1.65 V to 1.95 V)
 - JESD8-5A (2.3 V to 2.7 V)
 - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

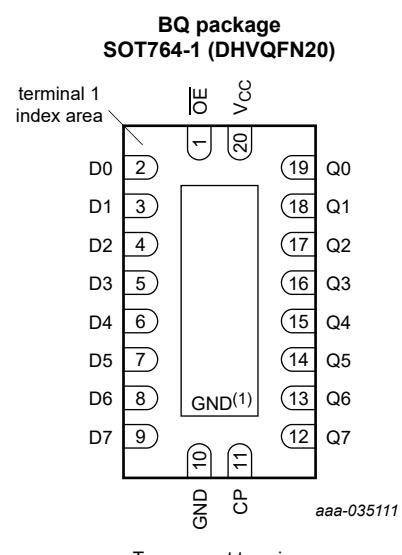
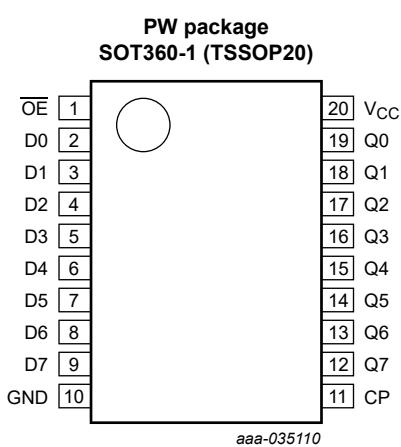
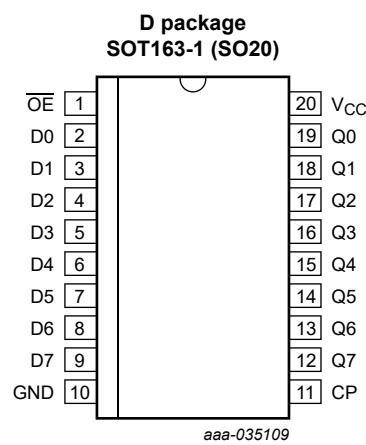
Type number	Package	Temperature range	Name	Description	Version
74LVC574AD	SO20	-40 °C to +125 °C		plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVC574APW	TSSOP20	-40 °C to +125 °C		plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74LVC574ABQ	DHVQFN20	-40 °C to +125 °C		plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm	SOT764-1

4. Functional diagram



5. Pinning information

5.1. Pinning



(1) This is not a ground pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to GND.

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
OE	1	output enable input (active LOW)
CP	11	clock input (LOW to HIGH; edge triggered)
D0, D1, D2, D3, D4, D5, D6, D7	2, 3, 4, 5, 6, 7, 8, 9	data input
Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7	19, 18, 17, 16, 15, 14, 13, 12	data output
GND	10	ground (0 V)
V _{CC}	20	supply voltage

6. Functional description

Table 3. Functional table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW to HIGH CP transition;

L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW to HIGH CP transition;

↑ = LOW to HIGH clock transition;

Z = high-impedance OFF-state

Operating modes	Input			Internal flip-flop	Output
	OE	CP	Dn		
Load and read register	L	↑	l	L	L
	L	↑	h	H	H
Load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0	-50	-	mA
V _I	input voltage		[1]	-0.5	+6.5
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0	-	±50	mA
V _O	output voltage	output HIGH or LOW state	[2]	-0.5	V _{CC} + 0.5
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[3]	-	500 mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C.

For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.

For SOT764-1 (DHVQFN20) package: P_{tot} derates linearly with 12.9 mW/K above 111 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output HIGH or LOW state	0	-	V_{CC}	V
		output 3-state	0	-	5.5	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65 \text{ V to } 2.7 \text{ V}$	0	-	20	ns/V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C	Unit	
			Min	Typ[1]	Max			
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.2 \text{ V}$	1.08	-	-	1.08	-	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	$0.65 \times V_{CC}$	-	-	$0.65 \times V_{CC}$	-	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	-	-	1.7	-	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.2 \text{ V}$	-	-	0.12	-	0.12	V
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	-	$0.35 \times V_{CC}$	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	-	0.7	-	0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		$I_O = -100 \mu\text{A}; V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	$V_{CC} - 0.2$	-	-	$V_{CC} - 0.3$	-	V
		$I_O = -4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	1.2	-	-	1.05	-	V
		$I_O = -8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	1.8	-	-	1.65	-	V
		$I_O = -12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	2.2	-	-	2.05	-	V
		$I_O = -18 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.4	-	-	2.25	-	V
		$I_O = -24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	2.2	-	-	2.0	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		$I_O = 100 \mu\text{A}; V_{CC} = 1.65 \text{ V to } 3.6 \text{ V}$	-	-	0.2	-	0.3	V
		$I_O = 4 \text{ mA}; V_{CC} = 1.65 \text{ V}$	-	-	0.45	-	0.65	V
		$I_O = 8 \text{ mA}; V_{CC} = 2.3 \text{ V}$	-	-	0.6	-	0.8	V
		$I_O = 12 \text{ mA}; V_{CC} = 2.7 \text{ V}$	-	-	0.4	-	0.6	V
		$I_O = 24 \text{ mA}; V_{CC} = 3.0 \text{ V}$	-	-	0.55	-	0.8	V
I_I	input leakage current	$V_{CC} = 3.6 \text{ V}; V_I = 5.5 \text{ V or GND}$	-	± 0.1	± 5	-	± 20	μA

Octal D-type flip-flop with 5 V tolerant inputs/outputs; positive edge-trigger; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
I _{OZ}	OFF-state output current	V _I = V _{IH} or V _{IL} ; V _{CC} = 3.6 V; V _O = 5.5 V or GND	-	0.1	±10	-	±20	µA
I _{OFF}	power-off leakage supply	V _{CC} = 0 V; V _I or V _O = 5.5 V	-	0.1	±10	-	±20	µA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	10	-	40	µA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	-	5000	µA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND to V _{CC}	-	5.0	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see [Fig. 8](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t _{pd}	propagation delay	CP to Qn; see Fig. 5 [2]						
		V _{CC} = 1.2 V	-	17.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	4.6	6.4	13.1	4.6	15.1	ns
		V _{CC} = 2.3 V to 2.7 V	2.6	3.9	7.9	2.6	9.1	ns
		V _{CC} = 2.7 V	1.5	3.7	8.0	1.5	10.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	3.5	7.0	1.5	9.0	ns
t _{en}	enable time	OE to Qn; see Fig. 7 [2]						
		V _{CC} = 1.2 V	-	19.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	1.5	7.0	17.1	1.5	19.8	ns
		V _{CC} = 2.3 V to 2.7 V	1.5	4.0	9.4	1.5	10.9	ns
		V _{CC} = 2.7 V	1.5	4.1	8.5	1.5	11.0	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	3.2	7.5	1.5	9.5	ns
t _{dis}	disable time	OE to Qn; see Fig. 7 [2]						
		V _{CC} = 1.2 V	-	9.0	-	-	-	ns
		V _{CC} = 1.65 V to 1.95 V	2.5	4.1	10.1	2.5	11.6	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.3	5.7	1.0	6.6	ns
		V _{CC} = 2.7 V	1.5	3.1	6.5	1.5	8.5	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	2.9	6.0	1.5	7.5	ns
t _w	pulse width	clock HIGH or LOW; see Fig. 5						
		V _{CC} = 1.65 V to 1.95 V	5.0	-	-	5.0	-	ns
		V _{CC} = 2.3 V to 2.7 V	4.0	-	-	4.0	-	ns
		V _{CC} = 2.7 V	3.3	-	-	3.3	-	ns
		V _{CC} = 3.0 V to 3.6 V	3.3	1.7	-	3.3	-	ns

Octal D-type flip-flop with 5 V tolerant inputs/outputs; positive edge-trigger; 3-state

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{su}	set-up time	Dn to CP; see Fig. 6						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	4.0	-	-	4.0	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	2.5	-	-	2.5	-	ns
		$V_{CC} = 2.7 \text{ V}$	2.0	-	-	2.0	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	2.0	0.3	-	2.0	-	ns
t_h	hold time	Dn to CP; see Fig. 6						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	3.0	-	-	3.0	-	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	2.0	-	-	2.0	-	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	-	-	1.5	-	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	+1.5	-0.2	-	+1.5	-	ns
f_{max}	maximum frequency	see Fig. 5						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	100	-	-	80	-	MHz
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	125	-	-	100	-	MHz
		$V_{CC} = 2.7 \text{ V}$	150	-	-	120	-	MHz
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	150	200	-	120	-	MHz
$t_{sk(0)}$	output skew time	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	[3]	-	-	1.0	-	1.5 ns
C_{PD}	power dissipation capacitance	per flip-flop; $V_I = \text{GND to } V_{CC}$	[4]					
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	11.2	-	-	-	pF
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	13.2	-	-	-	pF
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	14.9	-	-	-	pF

[1] Typical values are measured at $T_{amb} = 25 \text{ }^{\circ}\text{C}$ and $V_{CC} = 1.2 \text{ V}, 1.8 \text{ V}, 2.5 \text{ V}, 2.7 \text{ V}$ and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

t_{en} is the same as t_{PZL} and t_{PZH} .

t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz;

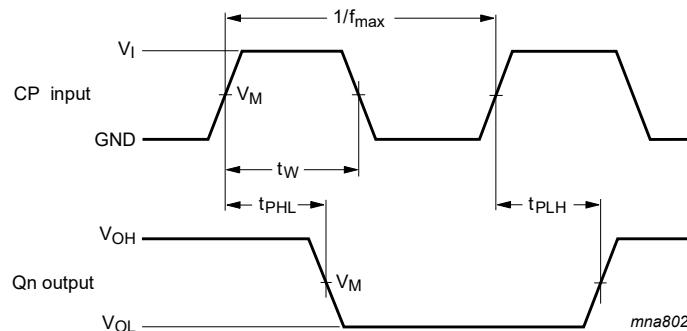
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

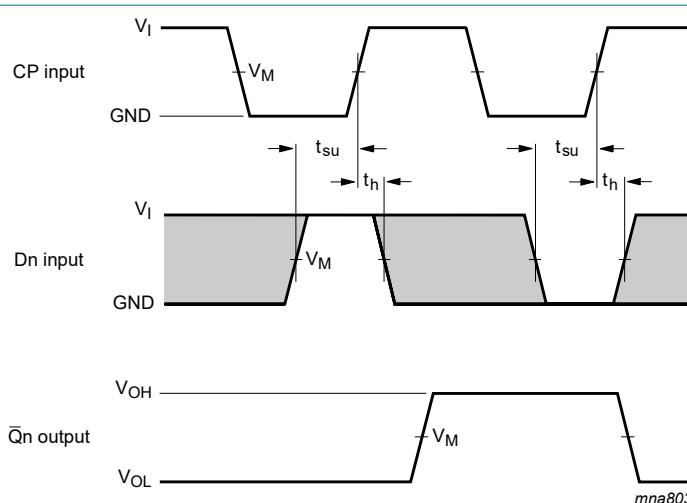
10.1. Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. Clock (CP) to output (Qn) propagation delays, the clock pulse width, output transition times, and the maximum frequency



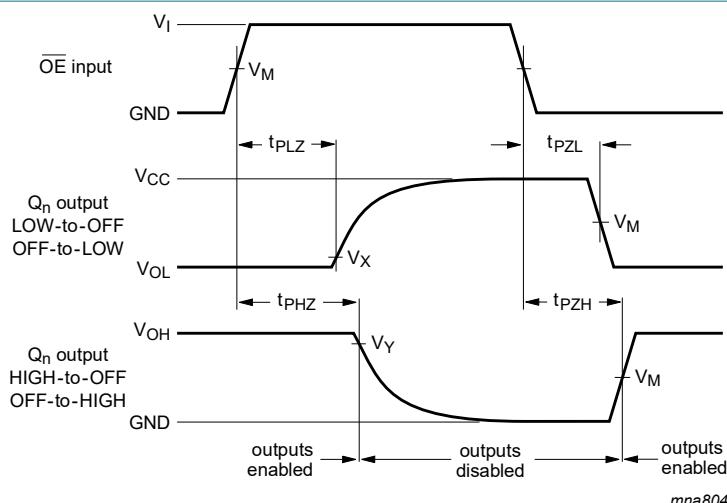
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 6. Data set-up and hold times for the Dn input to the CP input

Octal D-type flip-flop with 5 V tolerant inputs/outputs; positive edge-trigger; 3-state



Measurement points are given in [Table 8](#).

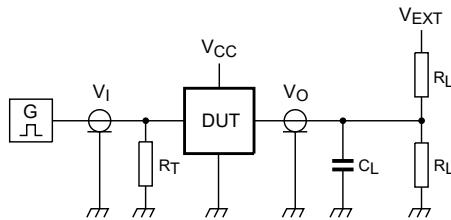
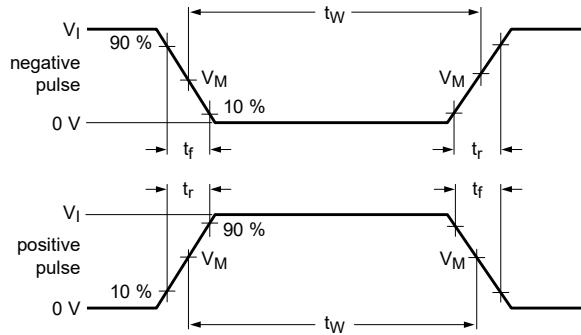
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 7. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input	Output			
V_{CC}	V_I	V_M	V_M	V_X	V_Y
1.2 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
1.65 V to 1.95 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V

Octal D-type flip-flop with 5 V tolerant inputs/outputs; positive edge-trigger; 3-state



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Test data is given in [Table 9](#).

Definitions for test circuit:

 R_L = Load resistance; C_L = Load capacitance including jig and probe capacitance; R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator; V_{EXT} = External voltage for measuring switching times.

Fig. 8. Test circuit for measuring switching times

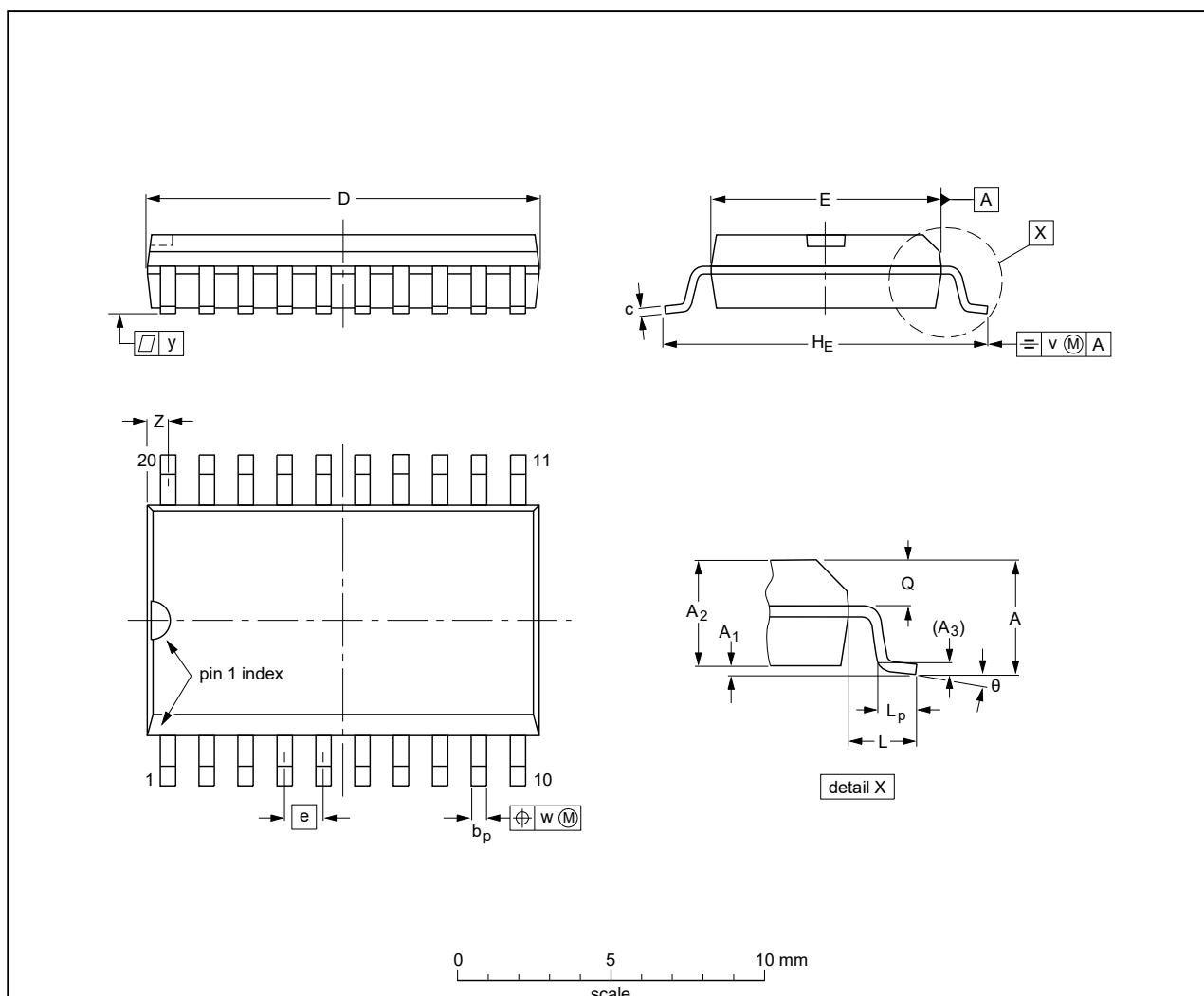
Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

11. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				99-12-27 03-02-19

Fig. 9. Package outline SOT163-1 (SO20)

Octal D-type flip-flop with 5 V tolerant inputs/outputs; positive edge-trigger; 3-state

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

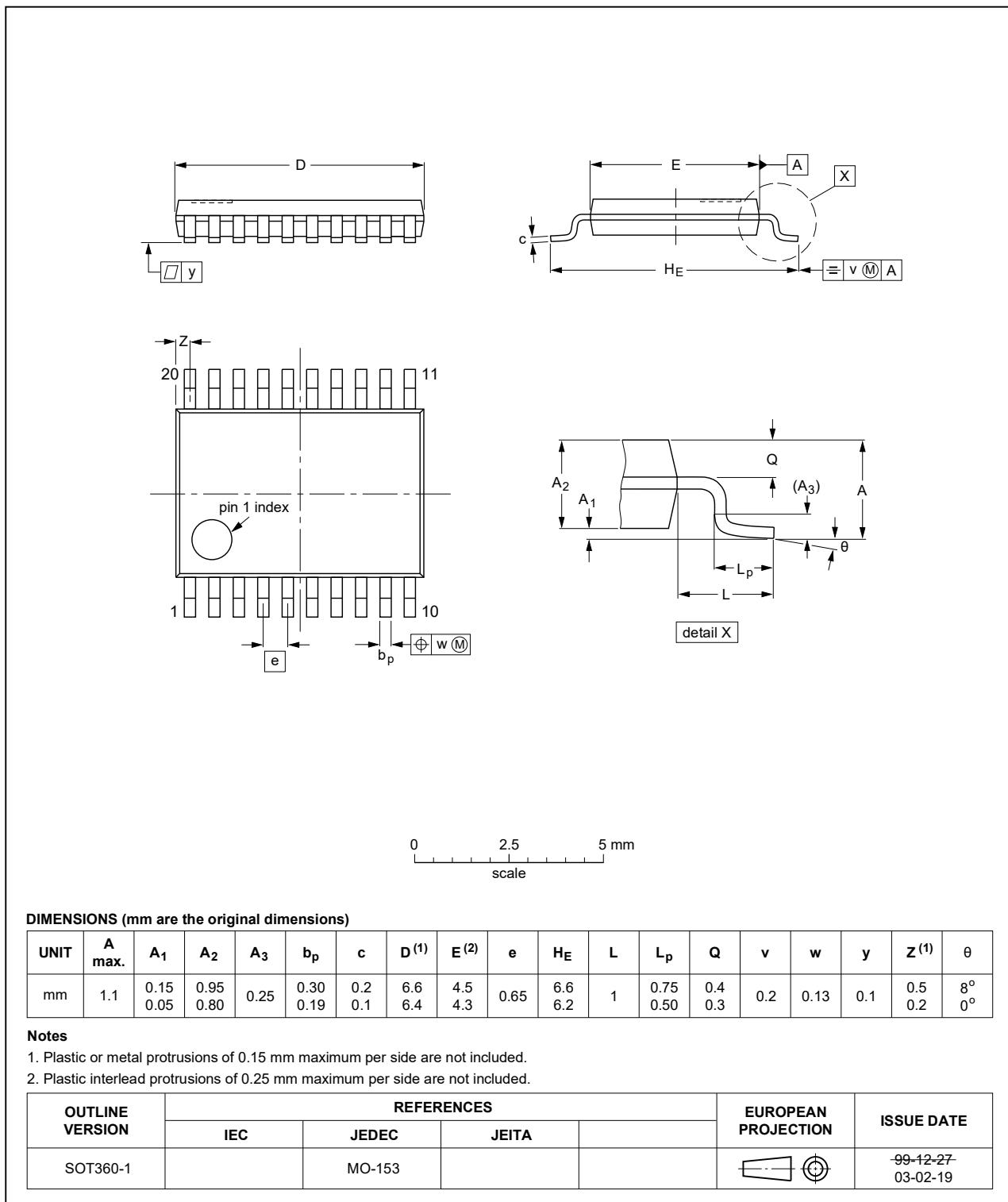


Fig. 10. Package outline SOT360-1 (TSSOP20)

Octal D-type flip-flop with 5 V tolerant inputs/outputs; positive edge-trigger; 3-state

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

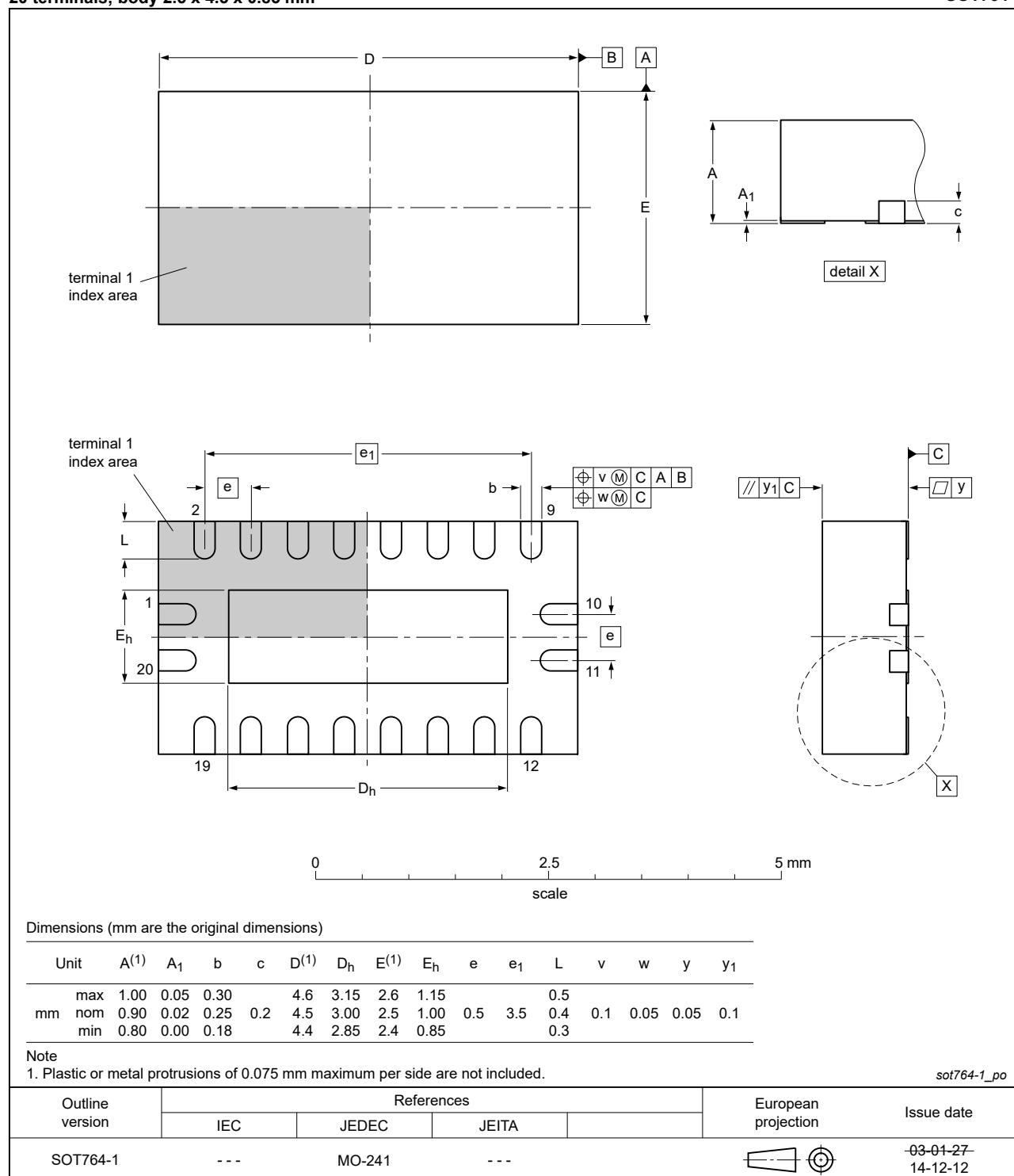


Fig. 11. Package outline SOT764-1 (DHVQFN20)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC574A v.7.1	20231102	Product data sheet	-	74LVC574A v.6
Modifications:	<ul style="list-style-type: none"> Section 2: ESD specification updated according to the latest JEDEC standard. 			
74LVC574A v.6	20210830	Product data sheet	-	74LVC574A v.5
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 1 and Section 2 updated. Type number 74LVC574ADB (SOT339-1/SSOP20) removed. Section 7: Derating values for P_{tot} total power dissipation updated. Fig. 11: Package outline drawing SOT764-1 (DHVQFN20) updated. 			
74LVC574A v.5	20121218	Product data sheet	-	74LVC574A v.4
Modifications:	<ul style="list-style-type: none"> Changed interlacing into interfacing (errata) in features list. 			
74LVC574A v.4	20121203	Product data sheet	-	74LVC574A v.3
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Table 4, Table 5, Table 6, Table 7, Table 8 and Table 9: values added for lower voltage ranges. 			
74LVC574A v.3	20040322	Product specification	-	74LVC574A v.2
74LVC574A v.2	20030620	Product specification	-	74LVC574A v.1
74LVC574A v.1	19980729	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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