

# N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY			
$V_{DS}$ (V)	$R_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>a</sup>	$Q_g$ (Typ.)
40	0.0088 at $V_{GS} = 10$ V	50	16 nC
	0.0105 at $V_{GS} = 4.5$ V	50	

## FEATURES

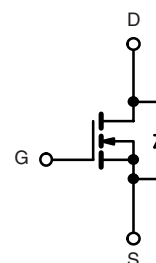
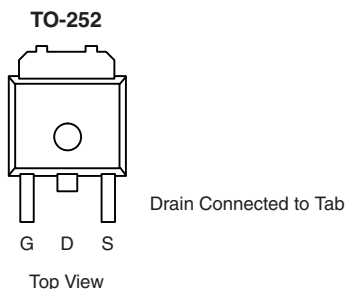
- Halogen-free According to IEC 61249-2-21 Definition
- TrenchFET® Power MOSFET
- 100 % UIS Tested
- 100 %  $R_g$  Tested
- PWM Optimized
- Compliant to RoHS Directive 2002/95/EC



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**

## APPLICATIONS

- LCD Display Backlight Inverters
- DC/DC Converters



Ordering Information: SUD50N04-8m8P-4GE3 (Lead (Pb)-free and Halogen-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_A = 25$ °C, unless otherwise noted				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		$V_{DS}$	40	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 150$ °C)	$T_C = 25$ °C	$I_D$	50 <sup>a</sup>	A
	$T_C = 70$ °C		44	
	$T_A = 25$ °C		14 <sup>b</sup>	
	$T_A = 70$ °C		11.2 <sup>b</sup>	
Pulsed Drain Current		$I_{DM}$	100	
Continuous Source-Drain Diode Current	$T_C = 25$ °C	$I_S$	40	A
	$T_A = 25$ °C		2.6 <sup>b</sup>	
Single Pulse Avalanche Current	L = 0.1 mH	$I_{AS}$	30	mJ
Avalanche Energy		$E_{AS}$	45	
Maximum Power Dissipation	$T_C = 25$ °C	$P_D$	48.1	W
	$T_C = 70$ °C		30.8	
	$T_A = 25$ °C		3.1 <sup>b</sup>	
	$T_A = 70$ °C		2.0 <sup>b</sup>	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to 150	°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>b</sup>	Steady State	$R_{thJA}$	32	40	°C/W
Maximum Junction-to-Case	Steady State	$R_{thJC}$	2.1	2.6	

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

**SPECIFICATIONS**  $T_J = 25\text{ }^{\circ}\text{C}$ , unless otherwise noted

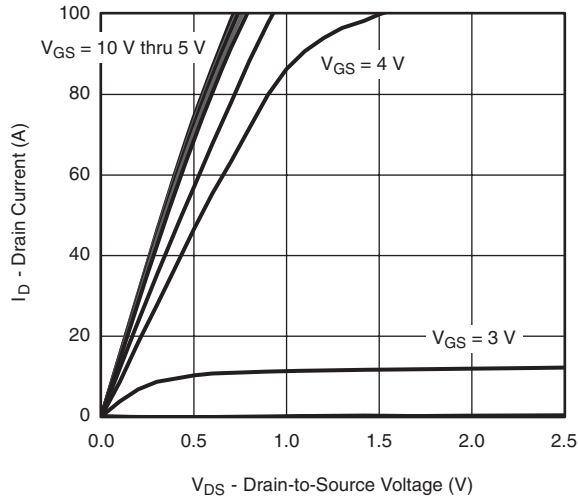
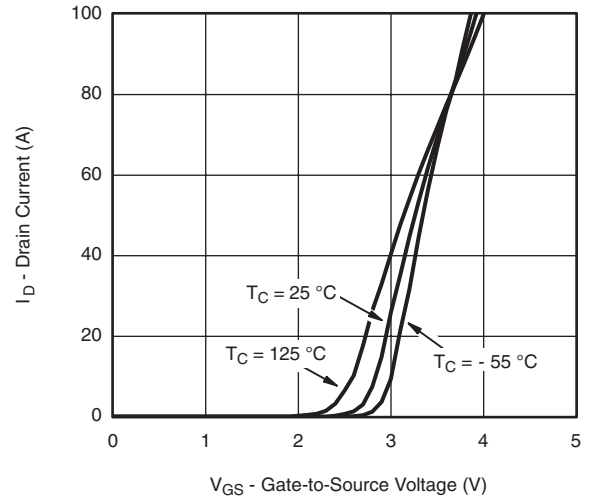
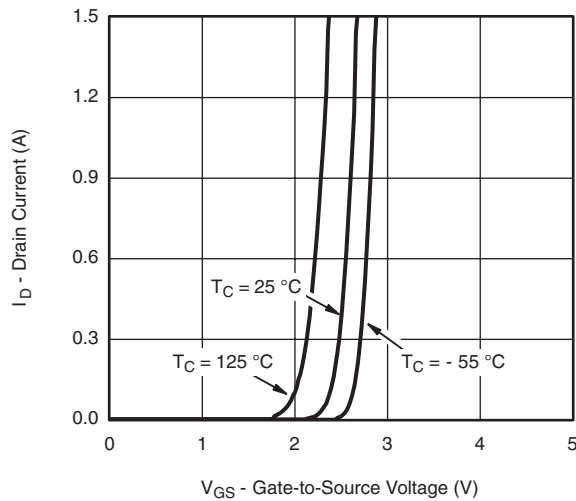
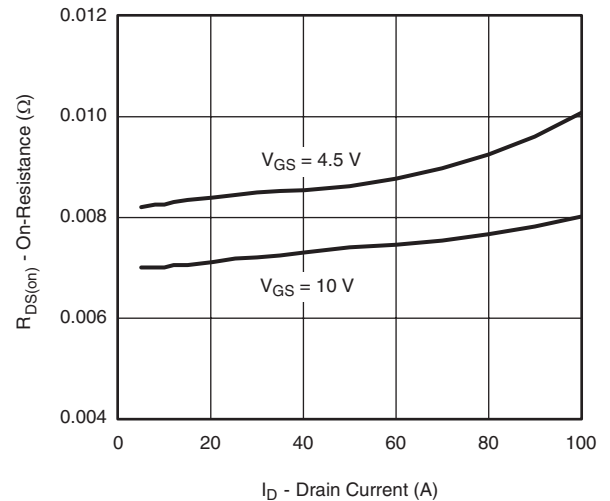
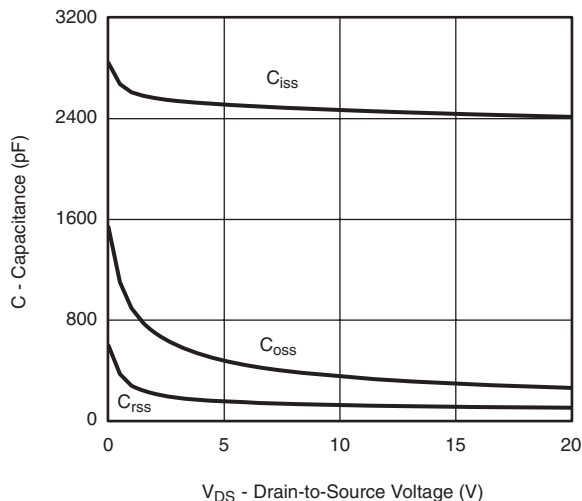
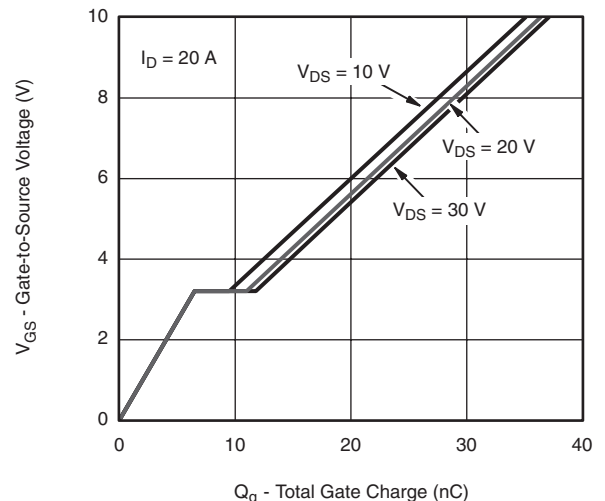
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	40			V
V <sub>DS</sub> Temperature Coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = 1.0 mA		44		mV/°C
V <sub>GS(th)</sub> Temperature Coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>			- 5.9		
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.5		3.0	V
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C			20	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	50			A
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		0.0069	0.0088	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 15 A		0.0084	0.0105	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A		75		S
Dynamic <sup>b</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, f = 1 MHz		2400		pF
Output Capacitance	C <sub>oss</sub>			260		
Reverse Transfer Capacitance	C <sub>rss</sub>			100		
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		37	56	nC
		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A		16	24	
Gate-Source Charge	Q <sub>gs</sub>			6.5		
Gate-Drain Charge	Q <sub>gd</sub>			4.5		
Gate Resistance	R <sub>g</sub>	f = 1 MHz	2.5	5.5	8.5	Ω
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 20 V, R <sub>L</sub> = 1 Ω I <sub>D</sub> ≅ 20 A, V <sub>GEN</sub> = 4.5 V, R <sub>g</sub> = 1 Ω		30	45	ns
Rise Time	t <sub>r</sub>			15	25	
Turn-Off Delay Time	t <sub>d(off)</sub>			45	70	
Fall Time	t <sub>f</sub>			15	25	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 20 V, R <sub>L</sub> = 1 Ω I <sub>D</sub> ≅ 20 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω		9	15	
Rise Time	t <sub>r</sub>			5	10	
Turn-Off Delay Time	t <sub>d(off)</sub>			40	60	
Fall Time	t <sub>f</sub>			5	10	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			40	A
Pulse Diode Forward Current <sup>a</sup>	I <sub>SM</sub>				100	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 10 A		0.81	1.2	V
Body Diode Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 20 A, dI/dt = 100 A/μs, T <sub>J</sub> = 25 °C		22	35	ns
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>			14	25	nC
Reverse Recovery Fall Time	t <sub>a</sub>			11		ns
Reverse Recovery Rise Time	t <sub>b</sub>			11		

Notes:

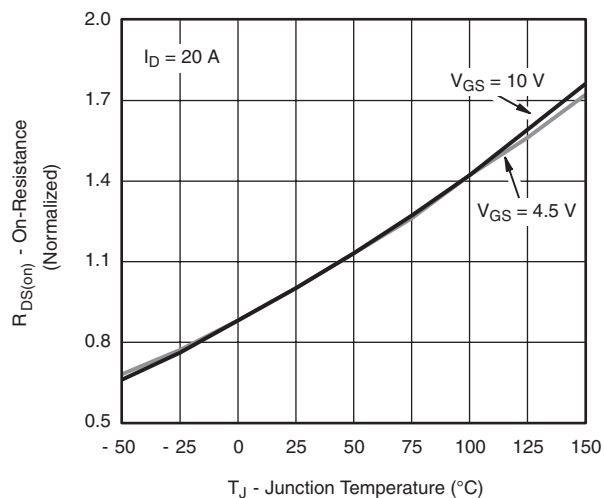
a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .

b. Guaranteed by design, not subject to production testing.

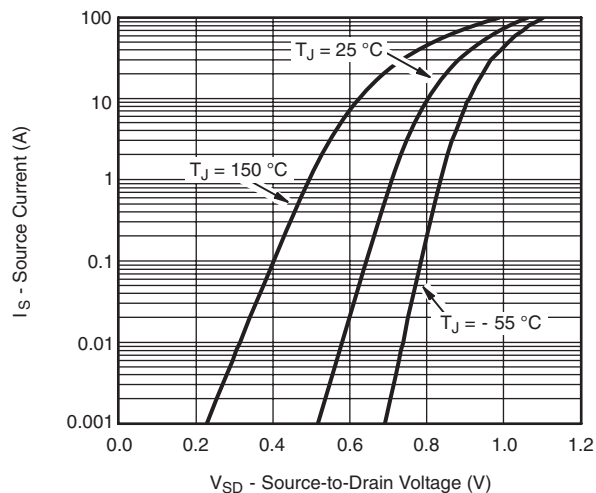
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Output Characteristics**

**Transfer Characteristics**

**Transfer Characteristics**

**On-Resistance vs. Drain Current**

**Capacitance**

**Gate Charge**

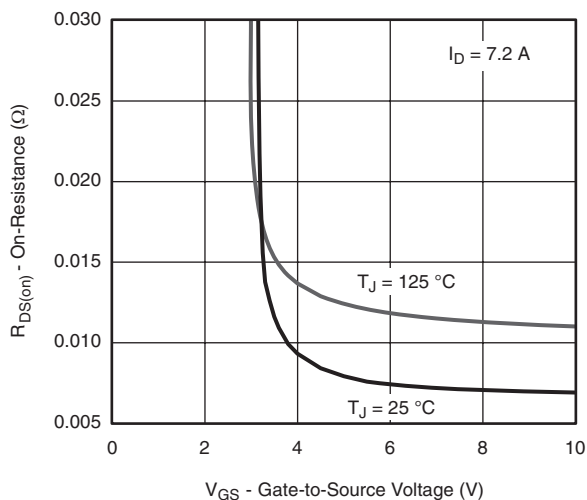
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



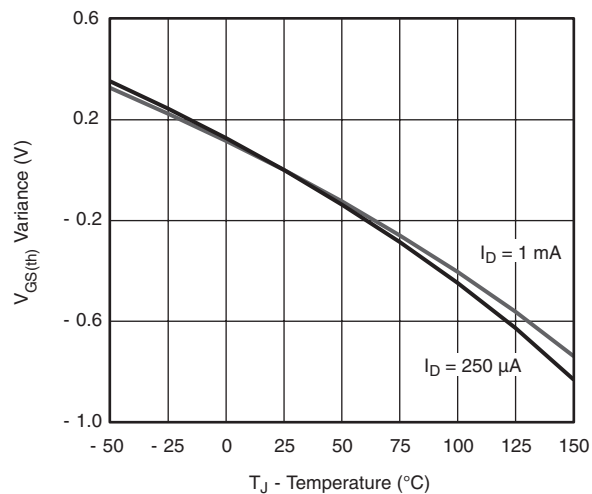
On-Resistance vs. Junction Temperature



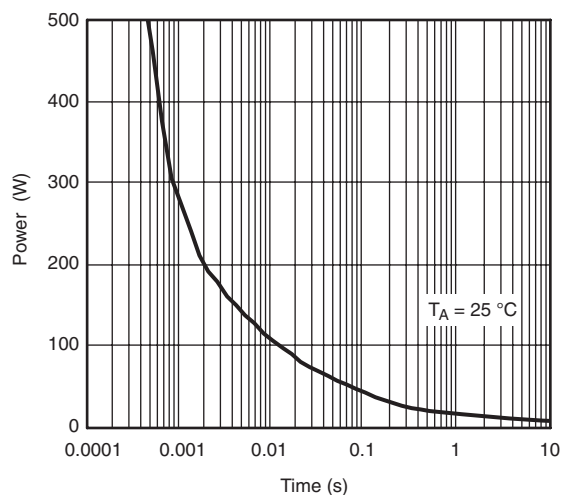
Source-Drain Diode Forward Voltage



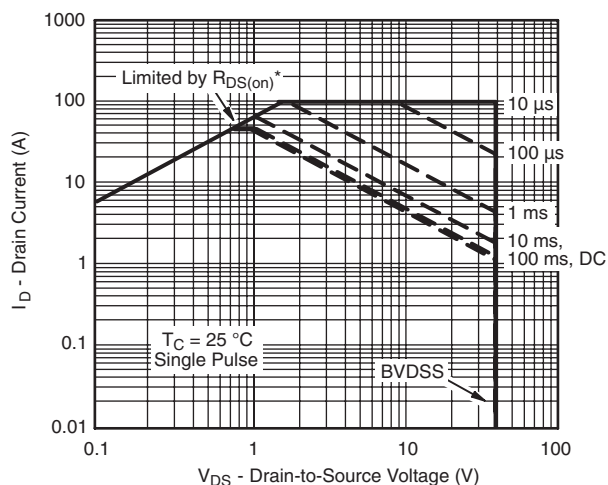
On-Resistance vs. Gate-to-Source Voltage



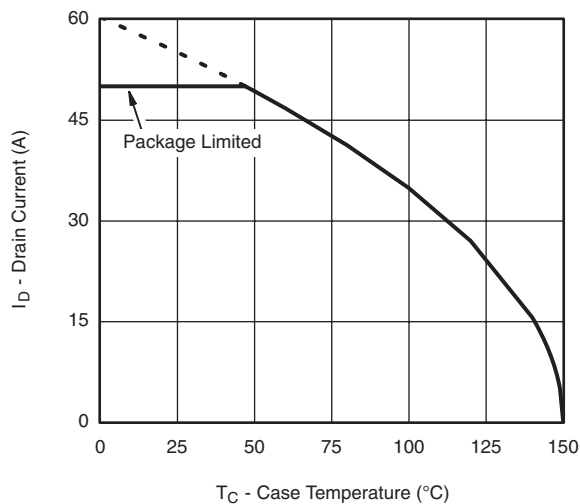
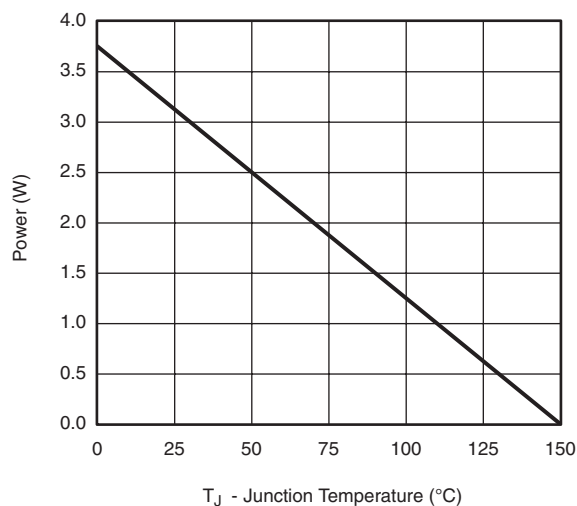
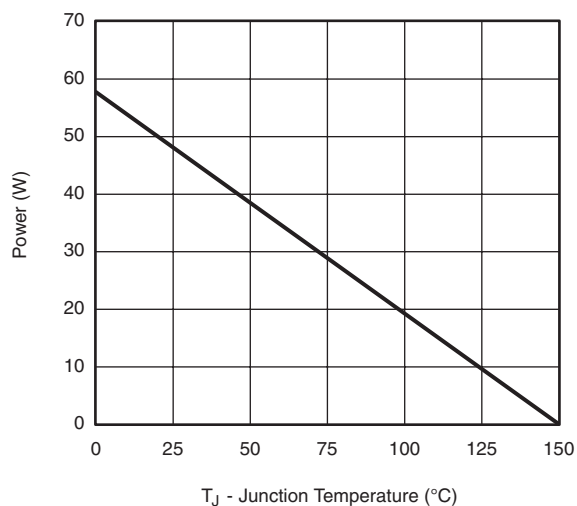
Threshold Voltage



Single Pulse, Junction-to-Ambient

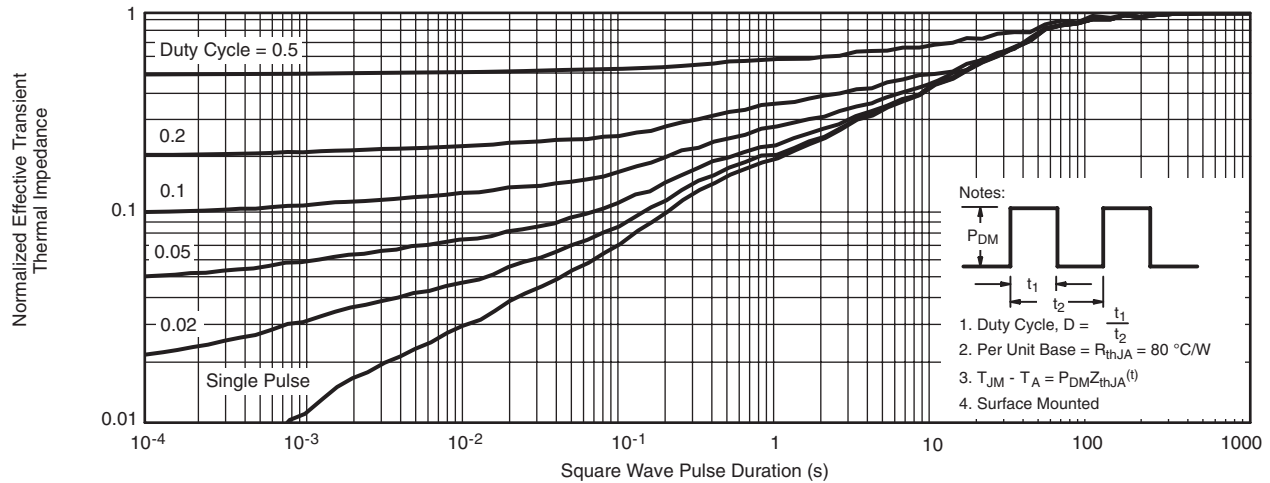


\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified  
Safe Operating Area, Junction-to-Case

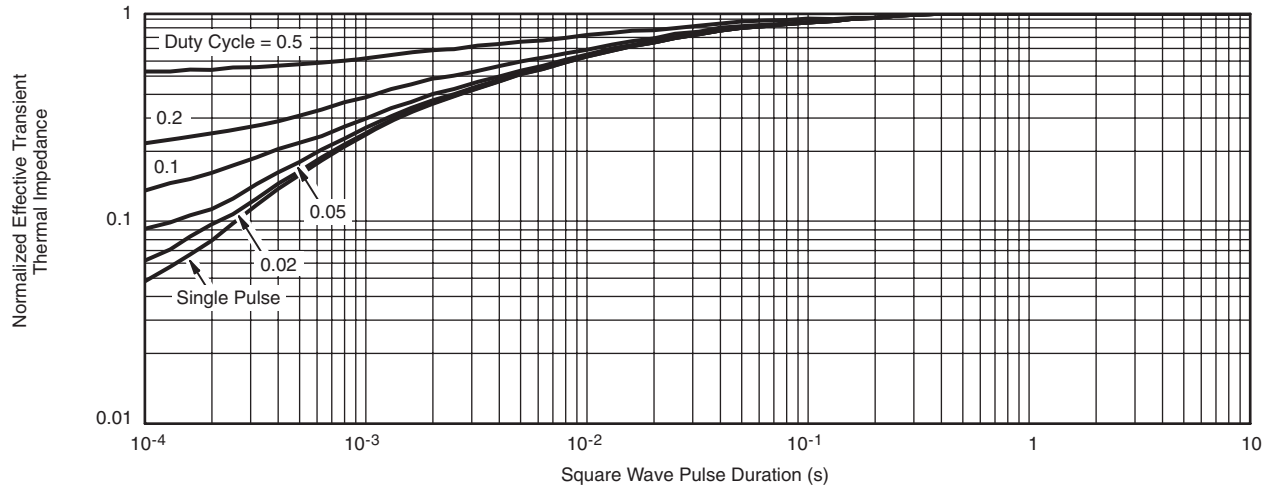
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted

**Current Derating\*, Junction-to-Case**

**Power Derating, Junction-to-Ambient**

**Power Derating, Junction-to-Case**

\* The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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## TO-252AA Case Outline

### VERSION 1: FACILITY CODE = Y



MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

#### Note

- Dimension L3 is for reference only



## VERSION 2: FACILITY CODE = N



DIM.	MILLIMETERS	
	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

DIM.	MILLIMETERS	
	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
theta	0°	10°
theta1	0°	15°
theta2	25°	35°

### Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E22-0399-Rev. R, 03-Oct-2022  
DWG: 5347



## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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