MOSFET – Single N-Channel

60 V, 3.9 mΩ, 103 A

NTTFS3D7N06HL

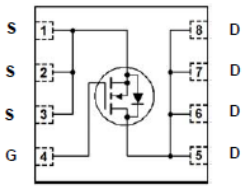
$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
60 V	3.9 mΩ @ 10 V	103 A
	5.2 mΩ @ 4.5 V	

Features

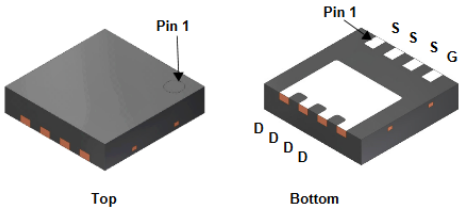
- Max $R_{DS(on)}$ = 3.9 mΩ at V_{GS} = 10 V, I_D = 23 A
- Max $R_{DS(on)}$ = 5.2 mΩ at V_{GS} = 4.5 V, I_D = 18 A
- High Performance Technology for Extremely Low $R_{DS(on)}$
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- DC-DC Buck Converters
- Point of Load
- High Efficiency Load Switch and Low Side Switching
- Oring FET



N-CHANNEL MOSFET



WDFN8
3.3X3.3, 0.65P
CASE 483AW

MARKING DIAGRAM

S3D7 = Specific Device Code
A = Assembly Plant Code
Y = Numeric Year Code
WW = Work Week Code
ZZ = Assembly Lot Code

MAXIMUM RATINGS (T_J = 25 °C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	60	V
Gate-to-Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	T_C = 25 °C	I_D	103	A
Power Dissipation $R_{\theta JC}$ (Note 1)			P_D	83	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	T_A = 25 °C	I_D	16	A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)			P_D	2.2	W
Pulsed Drain Current	T_A = 25 °C, t_p = 10 μs		I_{DM}	658	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +150	°C
Source Current (Body Diode)			I_S	69	A
Single Pulse Drain-to-Source Avalanche Energy (I_{AV} = 40 A, L = 0.1 mH) (Note 3)			E_{AS}	80	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case − Steady State (Note 1)	$R_{\theta JC}$	1.5	°C/W
Junction-to-Ambient − Steady State (Note 1)	$R_{\theta JA}$	54.8	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using 1 in^2 pad size, 1 oz. Cu pad.
3. E_{AS} of 80 mJ is based on started T_J = 25 °C, I_{AS} = 40 A, V_{DD} = 60 V, V_{GS} = 10 V. 100% test at I_{AS} = 40 A.

ORDERING INFORMATION

Device	Package	Shipping†
NTTFS3D7N06HLTWG	WDFN8 (Pb-Free)	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, ref to 25 °C			38.84		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 60 V	T_J = 25 °C			10	μA
			T_J = 125 °C			100	
Gate-to-Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				±100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 120 μA		1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 120 μA, ref to 25 °C			−4.83		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 23 A			3.2	3.9	mΩ
		V_{GS} = 4.5 V, I_D = 18 A			4.1	5.2	
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 23 A			170		S
Gate-Resistance	R_G	T_A = 25 °C			1		Ω
CHARGES & CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 30 V			2383		pF
Output Capacitance	C_{OSS}				400		
Reverse Transfer Capacitance	C_{RSS}				11.7		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 48 V, I_D = 11.5 A			32.7		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 48 V, I_D = 11.5 A			15.1		nC
Gate-to-Source Charge	Q_{GS}				5.5		
Gate-to-Drain Charge	Q_{GD}				3.3		
Plateau Voltage	V_{GP}				2.5		V
SWITCHING CHARACTERISTICS (Note 4)							
Turn-On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 48 V, I_D = 11.5 A, R_G = 2.5 Ω			15.6		ns
Rise Time	t_r				8.4		
Turn-Off Delay Time	$t_{d(OFF)}$				24.3		
Fall Time	t_f				6.2		
DRAIN-SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 23 A	T_J = 25 °C		0.8	1.2	V
			T_J = 125 °C		0.7		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 11.5 A			39		ns
Reverse Recovery Charge	Q_{RR}				28		nC
Charge Time	t_a	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 11.5 A			21		ns
Discharge Time	t_b				16		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Switching characteristics are independent of operating junction temperatures
5. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS

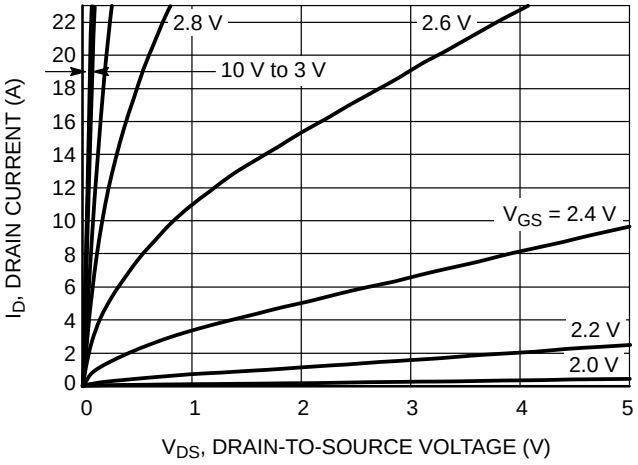


Figure 1. On-Region Characteristics

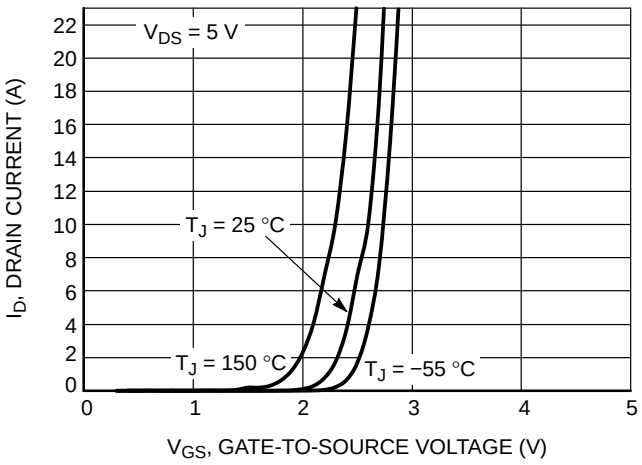


Figure 2. Transfer Characteristics

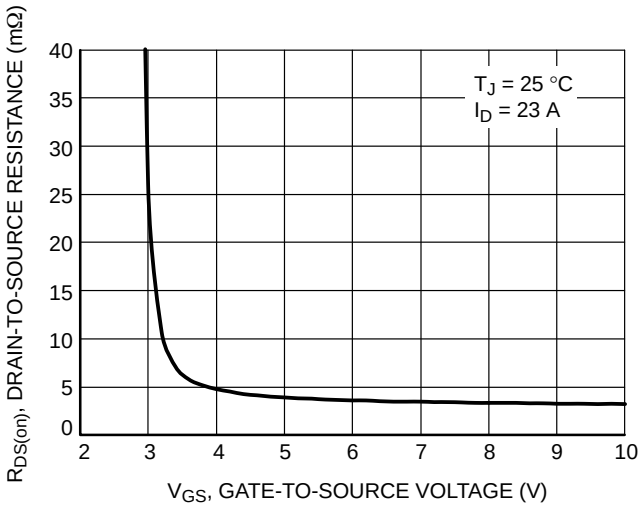


Figure 3. On-Resistance vs. Gate-to-Source Voltage

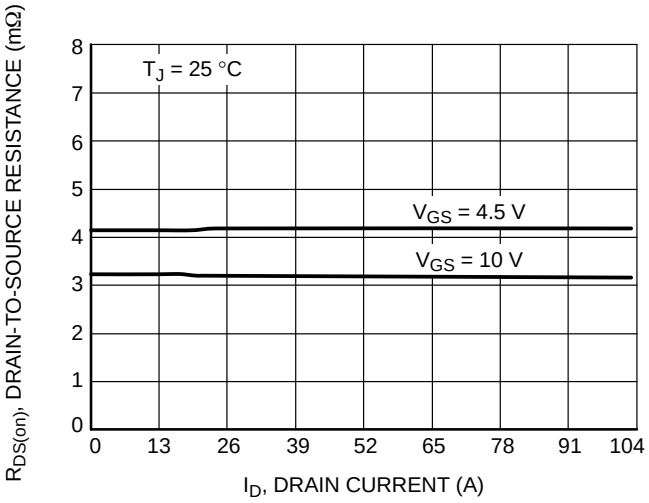


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

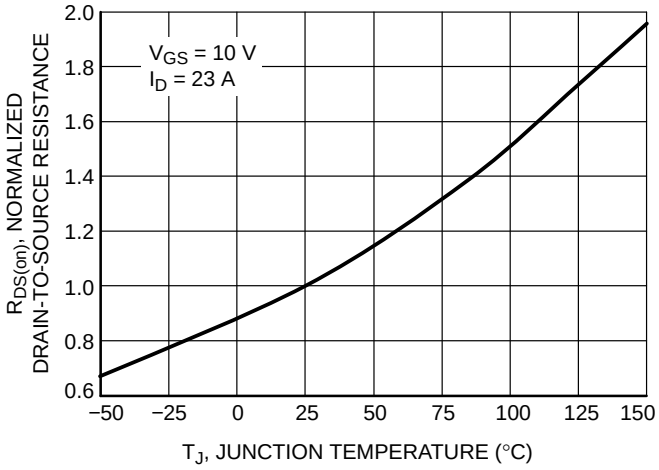


Figure 5. On-Resistance Variation with Temperature

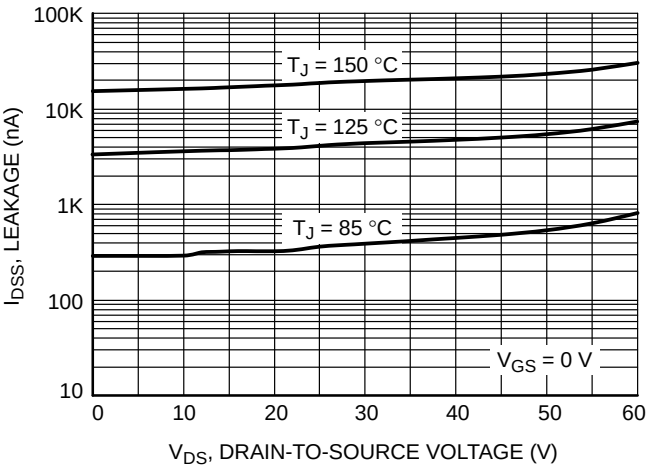


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

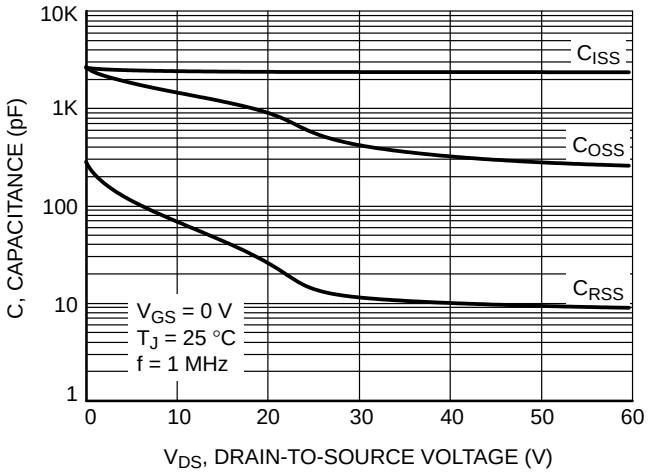


Figure 7. Capacitance Variation

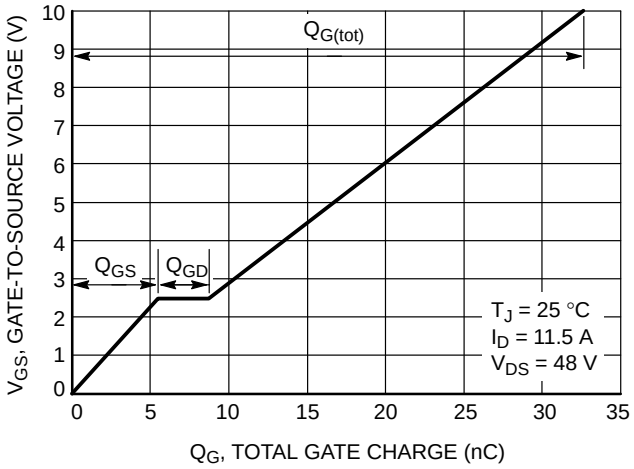


Figure 8. Gate-to-Source Voltage vs. Total Charge

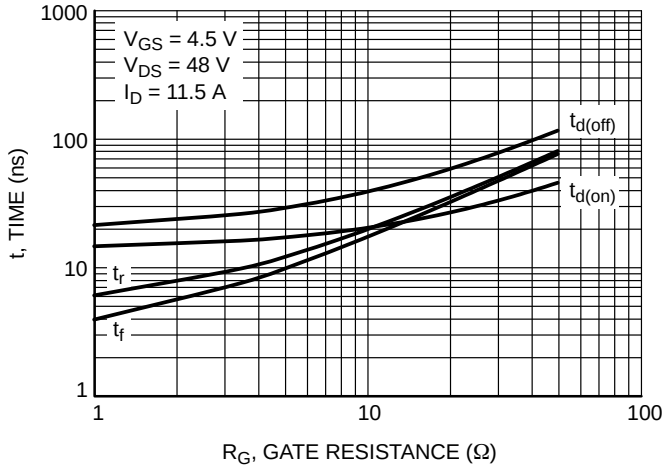


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

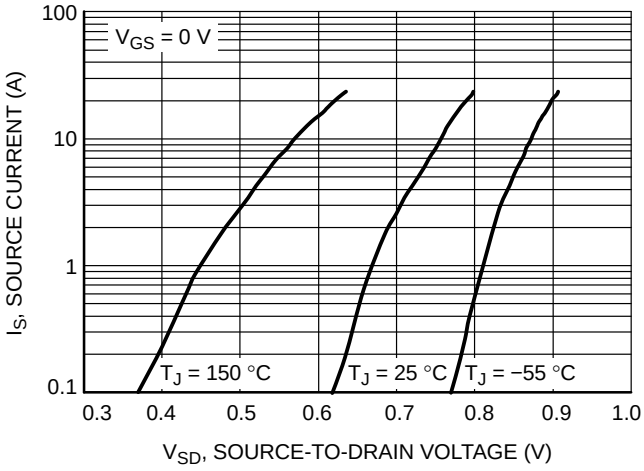


Figure 10. Diode Forward Voltage vs. Current

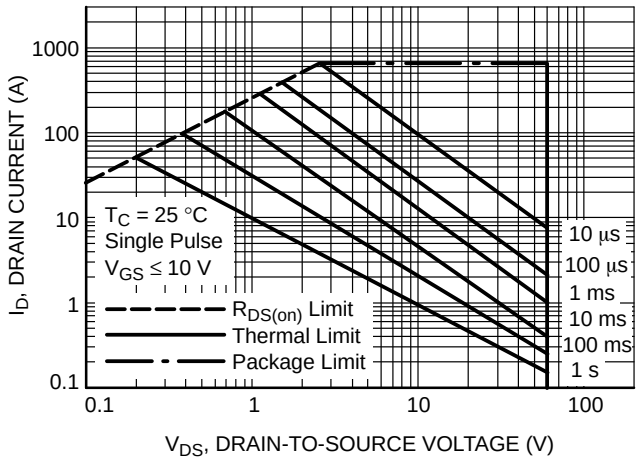


Figure 11. Maximum Rated Forward Biased Safe Operating Area

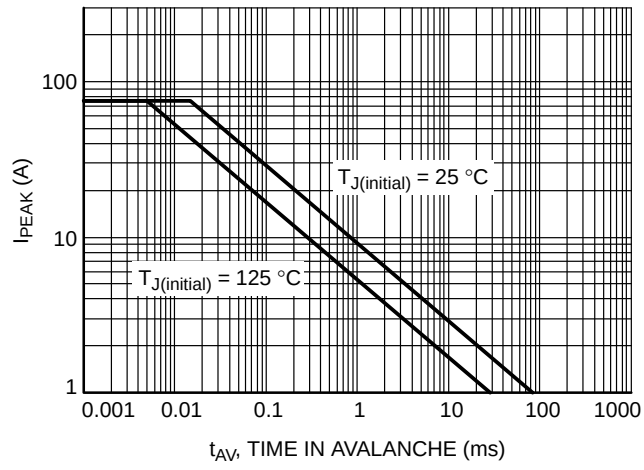


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

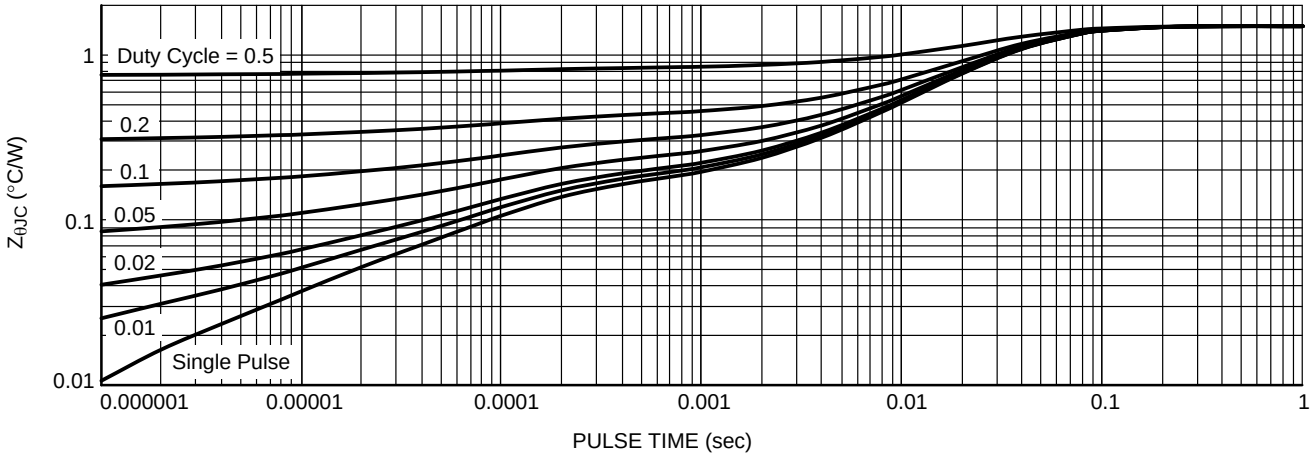
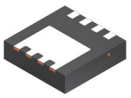


Figure 13. Transient Thermal Impedance

REVISION HISTORY

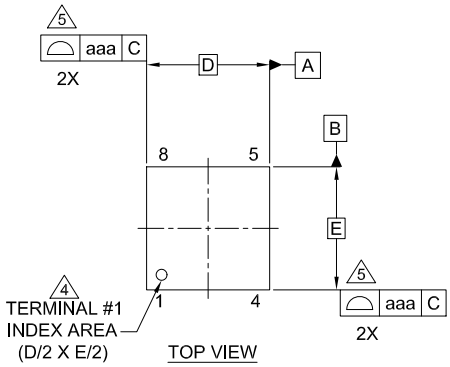
Revision	Description of Changes	Date
3	Rebranded the Data Sheet to **onsemi** format.	10/17/2025

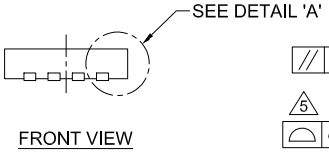
This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

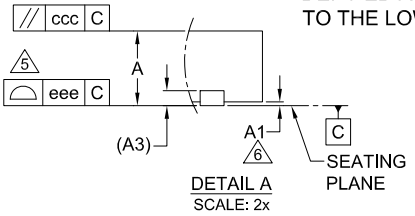


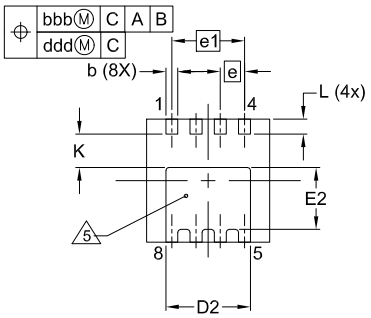
WDFN8 3.30x3.30x0.75, 0.65P
CASE 483AW
ISSUE B

DATE 22 MAR 2024







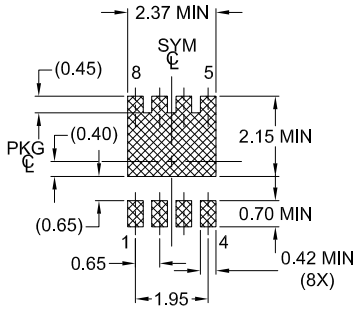


NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEP95 SEC. 3 SPP-12. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD, EMBEDDED METAL OR MARKED FEATURE.
5. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. 'A1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	--	--	0.05
A3		0.20 REF	
b	0.27	0.32	0.37
D		3.30 BSC	
D2	2.17	2.27	2.37
E		3.30 BSC	
E2	1.56	1.66	1.76
e		0.65 BSC	
e1		1.95 BSC	
K	0.90	--	--
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.05	

LAND PATTERN RECOMMENDATION



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WDFN8 3.30x3.30x0.75, 0.65P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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