Verilog Assignment 6
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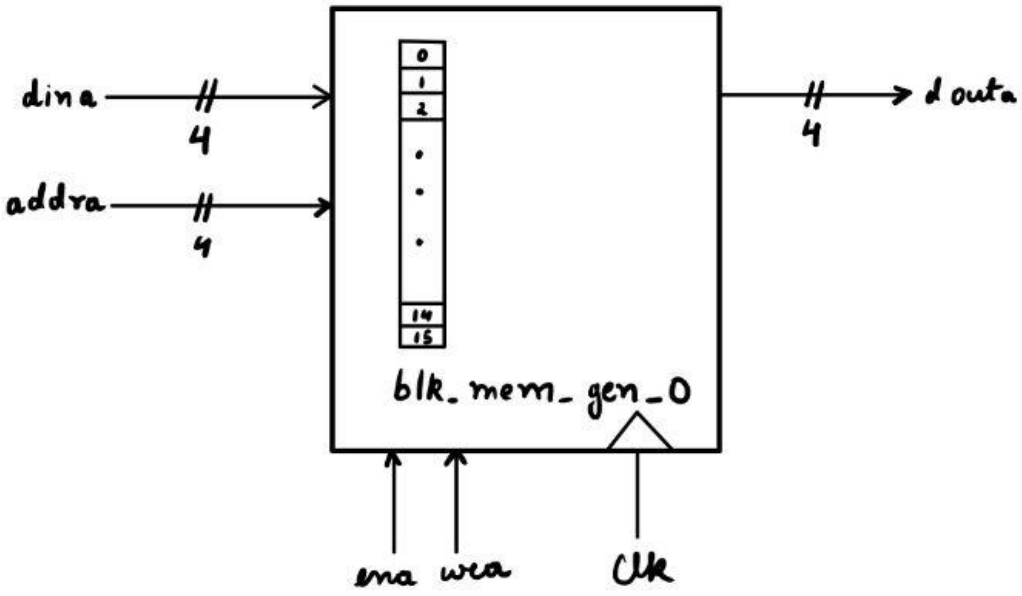
Question 1:

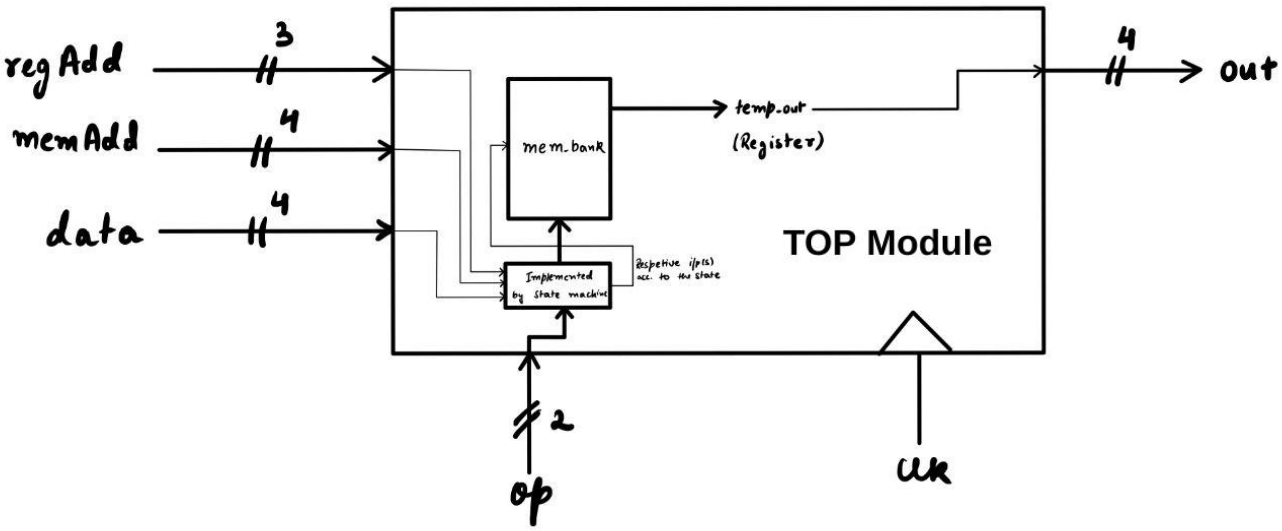
We are tasked with making an interface for an 8x4 register bank to a 16x4 memory system, with suitable control signals for read and write operations. We have implemented a Single Port RAM. We set the width and depth as 4 to store 4-bit data and to address 16 memory places. The module blk_mem_gen_0 is instantiated as mem_bank whose I/O is as follows:-

- Clock passed as clk for clka
- Enable bit passed as e for ena
- Write-enable bit passed as w for wea
- Address of port A passed as ma to addra
- Data input passed as dt for dina
- Data output received as temp_out for douta

We implemented the different operations as states specified by the opcode for carrying out that particular operation. The states are given as follows:-

- 0: corresponds to dina⇒memory[memAdd].
- 1: corresponds to regs[regAdd]⇒memory[memAdd].
- 2: corresponds to memory[memAdd]⇒regs[regAdd].
- 3: corresponds to displaying contents memory[memAdd].




regAdd
3
memAdd
4
data
4
mem_bank
temp_out
(Register)
4
out
Implemented
by state machine
respective i/p(s)
acc. to the state
TOP Module
2
op
clk