Verilog Assignment 7 Part 3
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We implemented a 32 register bank (of 32 bit each) and integrated the same with our ALU Module. This allows us to do operations of the form **Rx = Ry op Rz**.

Our regbank module has signals writeSP and readSP for reading to SP and writing ‘write_dataSP’ to SP respectively. SP is r[31] by default in our register bank. We have r[0] as the zero register. The signal writeReg is on when we want to write ‘write_data’ to ‘dr’ register. We can read 2 registers ‘sr1’ and ‘sr2’ simultaneously, with their contents being available on ‘read_data1’ and ‘read_data2’ respectively.

As we don’t have any memory to interface yet, we have hardcoded some values in the regbank to show it’s working.

In our FPGA demo, we set shamt as Ry[0], and used that shamt if required for any shifting operation.