Verilog Assignment 4
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Question 1:

We are given the task of performing Booth Multiplication for 8-bit operands. We are using the algorithm specified in the slides to calculate such a result. Note that we are printing the 2's complement of the answer in the decimal form so any negative number is displayed in the decimal form of its 2's complement. We are using a state machine to achieve this whose working is as follows.

- Default state: We enter this for the initialization part, for the further iterations.
- s1: When both q0 and q-1 are equal we make the desired changes and undergo the transition.
- s2: When q0 = 1 and q-1 = 0, a=a-m, this is taken care of in this state.
- s3: When q0 = 0 and q-1 = 1, a=a+m, this is taken care of in this state.
- s4: The final state, when output is assigned to out (by concatenation of a and q).