LOW POWER AND HIGH-PERFORMANCE ASSOCIATIVE MEMORY DESIGN

SOHAN DAS (20BEE0330)

Abstract

Content Addressable Memory (CAM) is a special memory used in search engines for numerous applications, especially in network routers for packet forwarding. The CAM operation begins with pre-charging followed by evaluating the match-lines (MLs) for searching the data in the stored memory. CAM stores unique words in their array of cells such that only one word is matched for a given search word. ML associated with matched word retains its state and the remaining MLs drain their charge. Ternary content addressable memory (TCAM) is a fast lookup hardware device used for high-speed packet forwarding. However, significant power consumption and high cost limits its versatility and popularity. In this paper, a design has been made for TCAM architecture with pre-charge controller. The pre-charge controller helps in predicting the mismatched MLs during pre-charge phase. This prediction happens at an early stage and helps in terminating the pre-charging of the line. This assures the design of TCAM which consumes low power and also improves the performance. The proposed early predict 8 × 8 TCAM architecture simulations were performed in 45nm technology node using Cadence Virtuoso. The proposed TCAM design exhibits 16.6% reduction in power, 24.7% decrement in delay and 37.1% minimization in energy metric than basic TCAM NOR.

Introduction

Fast and accurate reconstruction of particle tracks is a common challenge in high energy physics experiments. The Fast Tracker (FTK) is a dedicated electronics system being integrated in the ATLAS experiment for real-time reconstruction of all particle tracks with transverse momentum above a sufficiently threshold produced in the proton-proton collisions at the Large Hadron Collider (LHC) at CERN. The FTK drastically improves the capability of the online event selection system of the ATLAS experiment enabling the full exploitation of the physics capability of the LHC. The core of the FTK is a dedicated VLSI processor, the AM06 chip, which provides highly parallelized and fast pattern recognition. The AM06 chip is manufactured in TSMC 65 nm CMOS technology. In the next years, the energy and intensity of the proton beams of the LHC will significantly be upgraded. This strongly requires next generation of AMs with faster processing, lower power consumption and higher memory cell area density. The proposed solution is to move to the 28 nm CMOS technology. The aim of the next test version of AM chip, AM07, is to guarantee the working functionality of two newly designed memory cell technologies at the clock frequency of 200 MHz to pioneer the design of the future AMs for the ATLAS and CMS experiments at the LHC. In addition, AM07 will be exploited in the development of an integrated system of pattern recognition in the context of the image analysis.

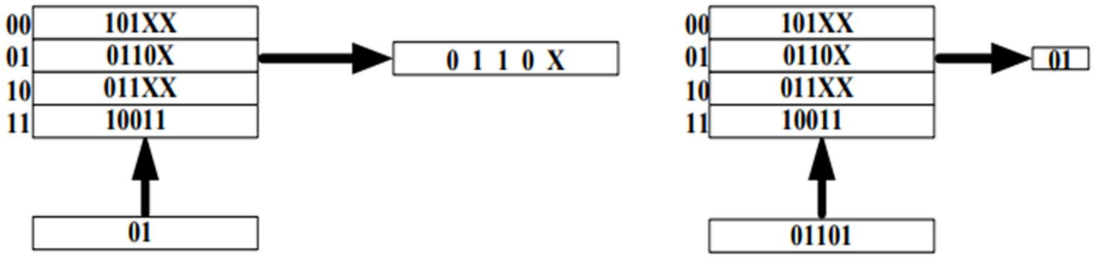

Figure 1. *RAM Versus CAM*

Architecture

The AM07 chip is organized in banks of Content Addressable Memories (CAMs) designed with two new custom layouts: DOXORAM and KOXORAM based on the previous XORAM. The area densities of these layouts are increased by a factor of 4 with respect to the AM06 chip. The power consumption of DOXORAM and KOXORAM are 30% and 75% less than AM06, respectively. As depicted, 16k patterns are organized in four 4k blocks (two DOXORAM blocks and two KOXORAM blocks). A 4k block consists of eight 512 blocks, each of which is made up of eight 64 blocks, which is the minimum unit of the AM07 chip. The figure shows the functional diagram of the 64 blocks. The memory matrix of the 64 block consists of eight columns, each of which is organized in 64 rows of 18-bit CAM segment word (CAMs). The Bit-Lines (BLs) and the Search-Lines (SLs) are 18-bit double polarized buses which connect a column of the memory matrix and they are respectively used to write CAMs and test for matches of the bus data to words written in CAMs. When a match is found in a CAMs the associated Set-Reset flip-flop (SR) is registered, and the match pattern in a row is stored in a segment of eight flip-flops (8FF). The majority logic counts the number of matches in a row and, if it exceeds a programmable threshold, the address of the row and the match pattern are read out. Each row of the memory matrix is connected by a WriteLine (WL). The on and off of WLs is controlled by external signals via a demultiplexer and all CAMs in a row are written in parallel when the WL signal for the row is turned on.

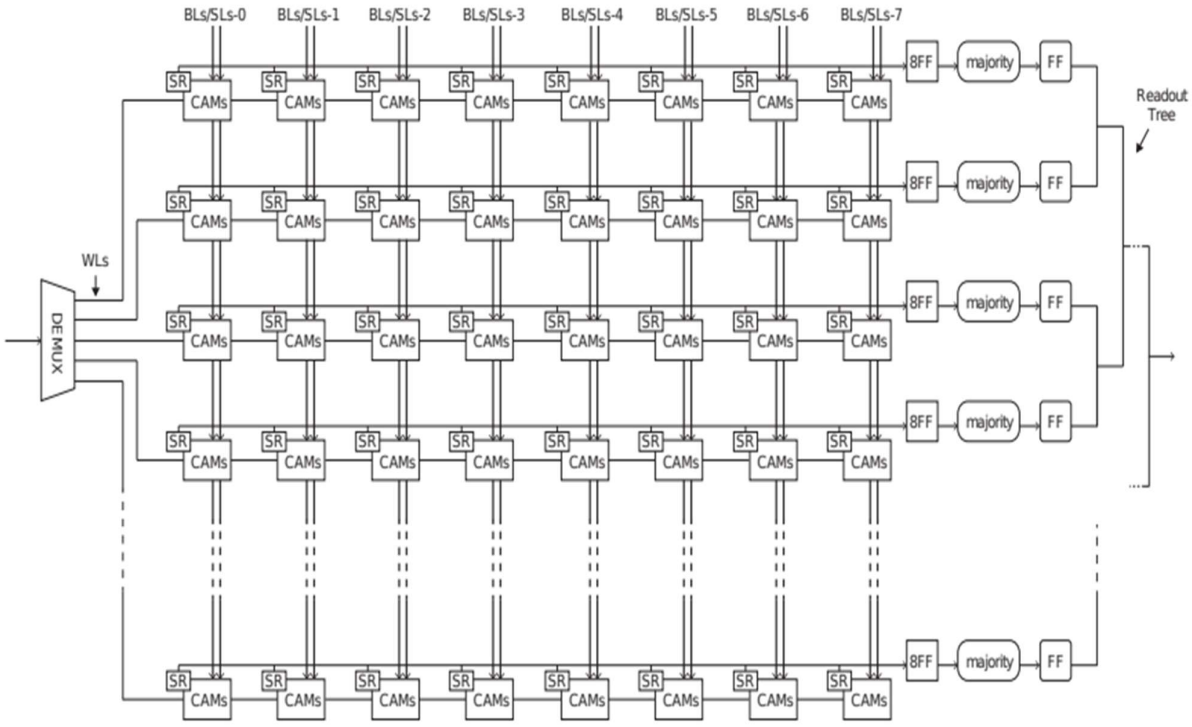

Fig. 2. Functional diagram of the 64 block of the AM07 chip.

A set of eight single polarization 18-bit input buses are connected to each 4k block through the 'DDR module' as shown in figure. Information in the buses is propagated to the BLs and the SLs in the 64 blocks. The bus mode is controlled by an external signal (STATE) as shown in Table I. The propagation of information to each 4k block could respectively be disabled in the DDR module.

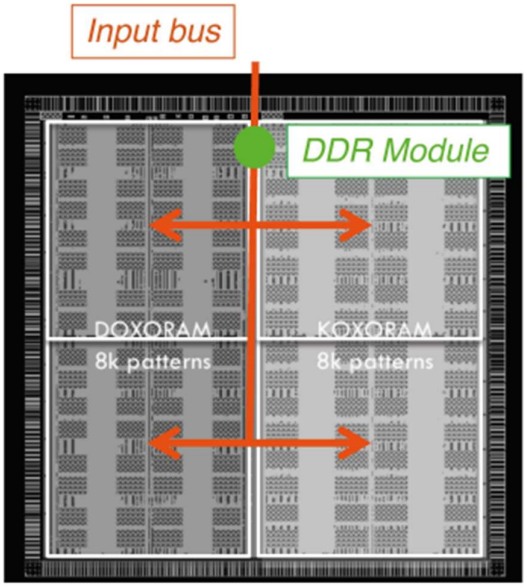

Fig. 3. Schematic drawing of the the input bus distribution to each 4k block.

At the same point the information on the input buses is sampled at the rising edge of the input clock and propagated to the double polarized internal buses. The original sampled information is passed to positive buses and negated information is passed to negative buses. The AM07 chip could operate in the Double Data Rate (DDR) data transfer mode. When the DDR mode is turned on, the input buses are sampled at both edges of the input clock. Information is sampled at both clock edges, stored in a set of flip-flops and passed to the double polarized internal buses at the next positive edge.

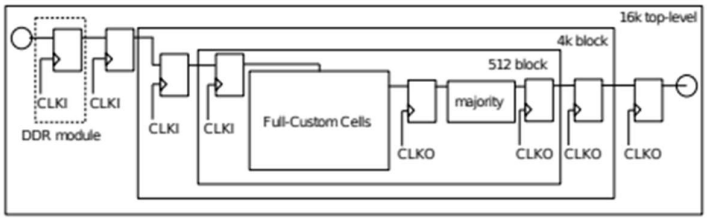

Fig. 4. Schematic diagram of the AM07 clock domains.

The information sampled at the rising (falling) edge is passed to the positive (negative) buses. The bus for BLs/SLs-0 (bus0) has a special structure to test the tolerance against high input clock frequency of the LVDS I/O cells. Due to this special feature, the bus0 is not equipped with the DDR mode i.e., this bus operates in the normal mode even when the DDR mode is turned on.

Simulation Results

To assess the TCAM design for high performance and low power, TCAM architectures are implemented and simulated in Cadence Virtuoso at a supply voltage Vdd=1V and frequency 200 MHz using 45nm technology node. Stability, search delay, and power are the three important parameters which determine the performance of memory design. Static noise margin (SNM) determines the stability of the system. Graphically, stability of the memory design is calculated from the butterfly curve. SNM value is obtained by inserting a largest possible square inside the lobe of the graph, thereby subtracting the diagonal value. The butterfly curve of the proposed TCAM cell design is

shown in the Figure 8. The SNM values of the proposed design and conventional design are 407.66mV and 398.43mV respectively. SNM values show that the proposed design has better stability than the conventional TCAM cell design. The Search delay is calculated from the transient response graph. The time difference between the miss/match line output and rising edge of the precharge signal will give the value of search delay. The power consumption of proposed design is calculated from the parameter storage format (PSF) file generated by the Virtuoso tool. Energy metric (EM) is one of the important performance metrics which is calculated by equation:

$$EM = \frac{power \times \text{delay}}{Total\ number\ of\ bits}(j/bit/search)$$

Typical comparison results of conventional and proposed TCAM architecture of 8(words) × 8(bits) for power, search delay and energy metric are shown in Table 2. Typical simulation results of proposed design show 35.15% lower energy metric, 24.61 % lower search delay and 16.63% lower power consumption. To determine the functionality of TCAM design, Monte Carlo (MC) simulations were also performed for 500 runs with a Gaussian 3σ variation on different parameters of the device. CAM stores unique data in their words. Search input word is selected randomly for performing the MC to a ascertain performance metric. Search delay and power consumption for proposed TCAM design are averaged in MC simulations for 500 runs as shown in Figure 9, Figure 10. In MC simulation the average search delay obtained is 262pS and average power consumption per bit is 586.102nW. Different process corner simulations like FF, SS, SF, & FS for proposed TCAM design are also performed. Table 3 shows process corner simulation results of power, search delay and energy metric for proposed 8×8 early predict TCAM architecture. It is observed that the worst case of energy metric is 0.222 fJ/bit/search and best case of energy metric is 0.0291fJ/bit/search. For functionality check, the timing simulation waveforms of conventional and proposed TCAM designs are shown in Figures.

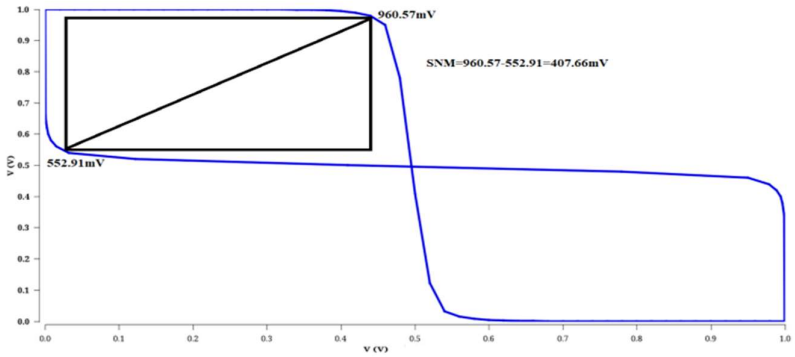

Figure 8. *Static noise margin of proposed early predict TCAM design*

Table 2. *Performance comparison of TCAM*

8×8 TCAM	Power consumption (μW)	Search delay (pS)	Energy Metric (fJ/bit/search)
NOR	28.322	349.36	0.15459
Proposed TCAM	23.610	263.36	0.09715

Table 3. *Process corner simulations for proposed TCAM*

Parameters	TT	FF	SS	SF	FS
Power (μW)	23.16	10.46	35.10	39.27	50.24
Delay (pS)	263.36	178.32	405.36	316.16	238.08
Energy Metric (fJ/bit/search)	0.09715	0.0291	0.222	0.1940	0.186

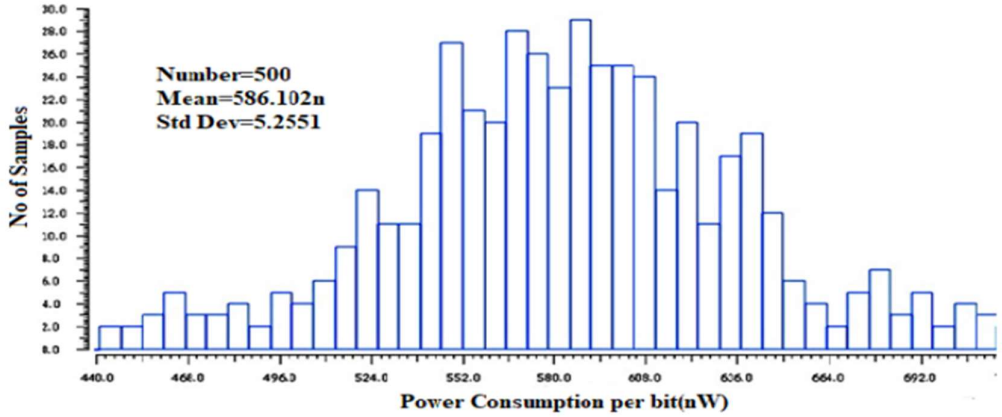

Figure 9. *Performance metric of early predict TCAM on MC simulations for 500 runs- histogram of power consumption*

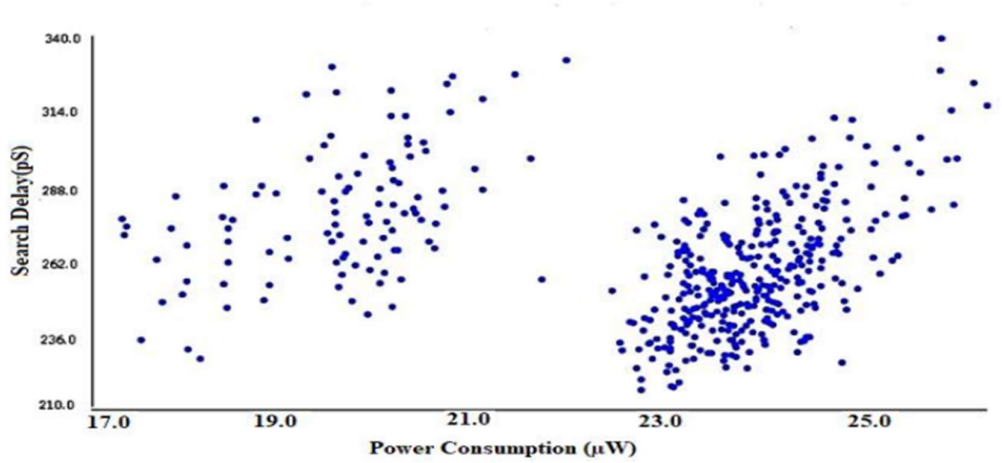

Figure 10. *Performance metric of early predict TCAM on MC simulations for 500 runs- power consumption and search delay scattered plot*

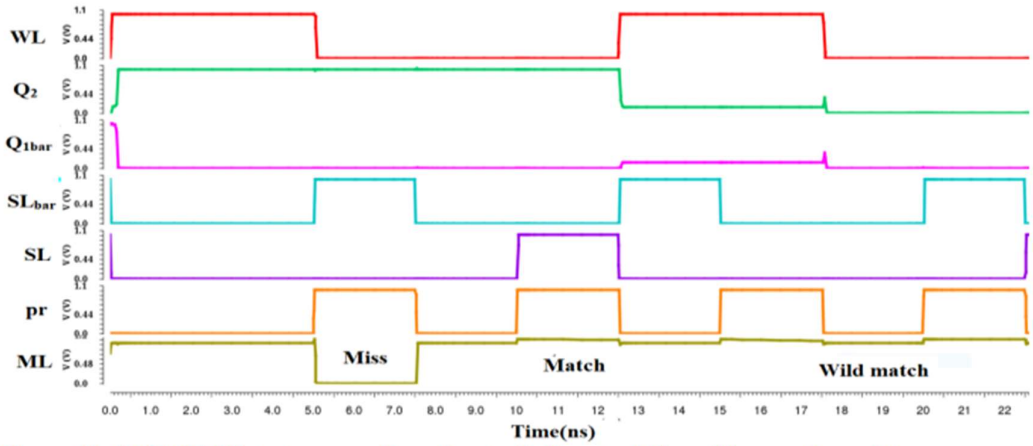

Figure 11*. NOR TCAM timing wave form for single bit miss followed by match condition*

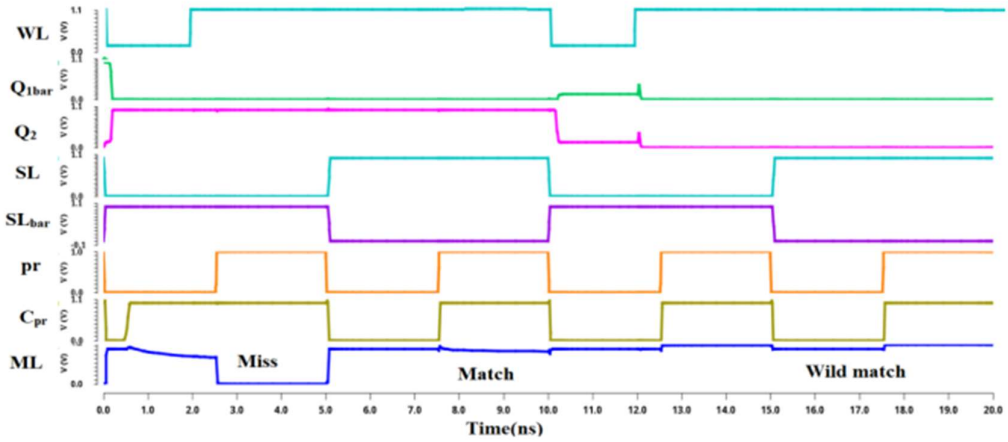

Figure 12. *Early Predict TCAM timing wave form for single bit miss followed by match condition*

Conclusion

In TCAM search operation, during miss-match, voltage swing in ML contributes to large search delay and power consumption. To overcome these problems and to reduce the miss-matched voltage swing, early predict TCAM architecture is designed. Early predict pre-charge circuitry helps to reduce the voltage swing on miss-matched ML dynamically, to improve the performance metric. In addition, proposed TCAM has greater stability than conventional TCAM due to use of PMOS access transistors for controlling the static random-access memories. Proposed TCAM architecture was simulated in CMOS process at 45nm technology node using Cadence Virtuoso and results are compared with TCAM NOR architecture. When compared with NOR TCAM architecture the proposed design offers 16.6% reduction in power, 24.7% minimization in search delay and it reduces the energy metric by 37.1%. Monte Carlo simulations and Process Corner simulations are also performed to validate the proposed TCAM for low power and low search delay. Simulation results show that the proposed design is useful for high speed, low power network packet forwarding applications with longer word lengths memory designs.

References

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