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ABSTRACT

This review aims to provide a technical roadmap and progress update for backplane thin film transistors (TFTs) used in organic light emitting diodes flat panel displays and next-generation flexible displays. In the introduction, we provide a general overview as well as trends in research on backplane TFTs. The main section describes current technical level and future prospects for amorphous metal oxide, semiconducting carbon nanotube, 2D transition metal dichalcogenide, and organic TFTs. The summary and prospects are provided in the conclusion.

1. Introduction

In the past 40 years, flat panel displays have greatly improved as a result of development of new display modes, improved electrical characteristics of backplane thin film transistors (TFTs), and optimization of materials and manufacturing processes [1,2]. Currently, the display market is divided into a high-end market with organic light emitting diodes (OLEDs) and a general and low-end market based on liquid crystal display (LCD). Recently, interest in form-free displays is increasing with the introduction of foldable and rollable OLED displays.

Semiconducting materials that are currently being used as the active layer of backplane TFTs or are being developed for flat-panel displays include polycrystalline silicon, amorphous metal oxides, semiconducting carbon nanotubes (CNTs) and two-dimensional semiconductors for OLEDs, and amorphous silicon and organic semiconductors for LCDs or e-paper displays. To achieve dynamic current-driving mode and low off-state current for low power consumption, the driving TFTs for OLEDs require high carrier mobility $(\mu) > 10$ cm$^2 \cdot$V$^{-1} \cdot$s^{-1}. To minimize brightness differences under the same gate bias, the driving TFTs of OLEDs require a very stringent operation reliability, including threshold voltage shift < 0.5 V. Semiconducting materials for the backplane TFTs in the

flat panel displays have a range of achieved and possible μ (Figure 1).

Indium gallium zinc oxide (IGZO), the prototypical amorphous metal oxide TFT, has $\mu \sim 10$ cm$^2 \cdot$V$^{-1} \cdot$s^{-1}. IGZO has been commercialized for OLED TVs. To increase the resolution and speed of OLED display applications, however, the carrier mobility of metal oxide must be increased further. Various metal oxide materials have been evaluated to obtain higher μ than IGZO TFTs can, but the materials have not achieved the stability, reliability, and large-area uniformity that IGZO provides, so further development is required before they can be commercialized.

Low-temperature polycrystalline silicon (LTPS) has been commercialized as a backplane for high-resolution mobile OLED displays due to its high μ. However, LTPS is fabricated using laser annealing, but this process cannot easily achieve a high yield of uniform backplane TFT for a large OLED TV. Therefore, applications to large, high-resolution OLED TVs require development of methods to overcome this limitation. For this purpose, research is being conducted on new semiconductor materials such as 2D transition metal dichalcogenides (TMDCs) and semiconducting carbon nanotubes (CNTs). However, many challenges such as optimization of materials,
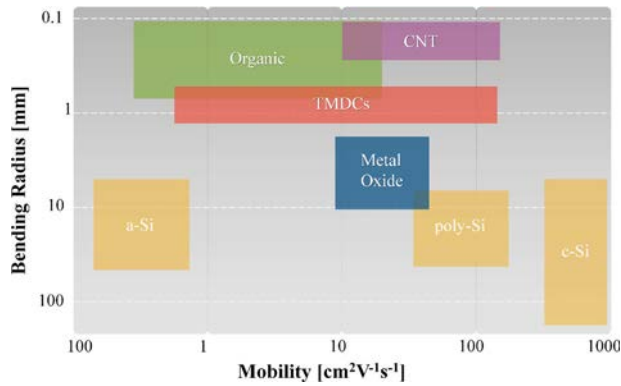

Figure 1. Charge-carrier mobility vs mechanical flexibility of various semiconducting materials for thin film transistors (TFTs) for flat panel display application. This figure is inspired and redrawn from a seminar presentation by Dr. Gerwin Gelinck (Holst Center)[1].

process, and device must be met before such materials can be used in backplane TFTs of commercial OLEDs and next generation displays.

Flexible displays have high form freedom and are therefore considered to constitute the next generation of displays. The backplane TFTs of a display that has true form freedom should include flexible semiconducting materials. Therefore, organic semiconductors, TMDCs, and CNT are promising candidate materials due to their high mechanical flexibility (Figure 1).

This review article provides a technical roadmap and recent progress update in the development of backplane TFTs for OLED flat panel displays and next-generation flexible displays. It mainly discusses the current technical level and prospects for amorphous metal oxide, semiconducting CNT, TMDCs, and organic TFTs (Figure 2).

2. Metal oxide TFTs

The first transistors equipped with oxide semiconductors used binary oxides such as ZnO, SnO, and their results

were not noteworthy [3,4]. However, in 2003, the use of indium-gallium-zinc-oxide (IGZO) was reported [5] and its applications have rapidly expanded. Amorphous oxide semiconductors began to gain attention because of their higher μ and reliability compared to a-Si TFT, and they were commercialized in active matrix organic light-emitting diode (AMOLED) backplanes.

Over the past decade, the direction of progress in this technology has been clearly divided into subjects of study. The two biggest trends in research on oxide TFTs research are vacuum-based and solution-based processes.

Vacuum-processes. Research trends (Table 1) for vacuum-processed oxide TFTs are as follows: (1) variation in oxide semiconductor materials and use of high-k dielectrics to achieve high μ [6–13]; (2) low-cost and non-toxic implementation using indium-free compositions [14–16]; (3) high-reliability components based on flexible substrates [17]; and (4) vacuum-deposition technology that uses non-sputtering methods (e.g. atomic-layer deposition (ALD) or metalorganic chemical-vapor deposition (MOCVD)) [14,16,18].

Research on ALD-based oxide TFTs has increased rapidly over the past decade (Figure 3), and multi-component studies have multiplied since 2014. The characteristics of TFTs have also improved significantly to become comparable to sputtering-based TFTs. ALD has several advantages over sputtering, including excellent controllability of film thickness and high process consistency. The method has achieved $10 \leq \mu \leq 50$ $cm^2 \cdot V^{-1} \cdot s^{-1}$. However, ALD has a low deposition rate, which impedes its use in commercial processes.

Early oxide TFTs had poor reliability. This problem has been reduced by the increase in understanding of the effect of hydrogen in TFTs, and by optimization of passivation and structures. However, oxide TFTs show a trade-off between reliability and high μ. Research to optimize or circumvent this trade-off is ongoing.

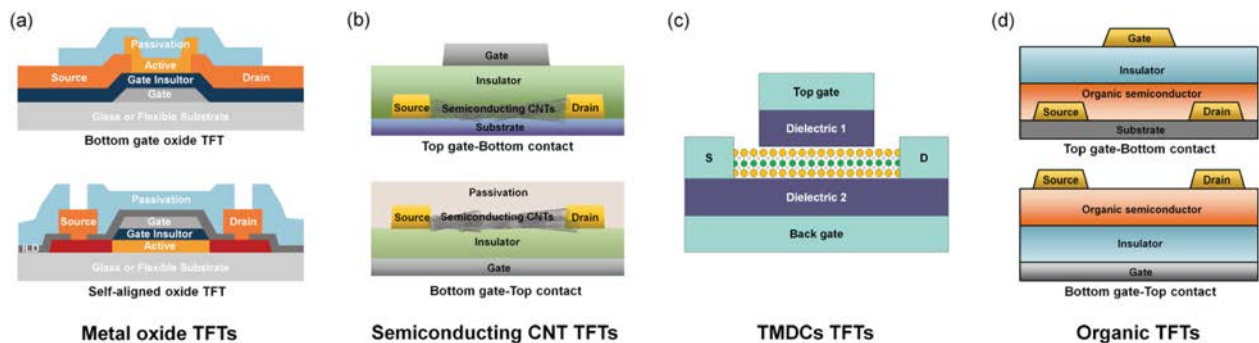Low-temperature polycrystalline oxide (LTPO) technology [19] has been used to commercialize hybrid

Figure 2. Typical device structures of metal oxide, semiconducting CNT, TMDCs, and organic TFTs.

Table 1. Recent progress on vacuum-based oxide TFTs.

Year	Materials	Type	Process	μ [cm$^2\cdot$V$^{-1}\cdot$s^{-1}]	S.S. [V·dec^{-1}]	I_{on}/I_{off}	Comments	Ref.
2010	IGZO	n	RF Sputtering	28	0.56	$\sim 10^6$	ZrO$_2$ dielectric	[9]
	ZnO	n	ALD	0.72	0.45	$\sim 10^6$	O$_2$ plasma treatment for the surface defect reduction	[16]
2011	IGZO	n	RF Sputtering	8.6	0.25	$\sim 10^6$	HfO$_2$/Al$_2$O$_3$ passivation for the WVTR improvement	[11]
2012	IGO	n	DC Sputtering	39.1	0.12	~ 10[10]	Polycrystalline IGO	[6]
	ZnO	n	Reactive RF Sputtering	7.4	0.58	$\sim 10^7$	Zn reactive (150 °C)	[39]
2013	SnO	P	RF Sputtering	1.8	-	$\sim 10^3$	SnO ceramic target	[40]
2014	IZO/IGZO	n	ALD	14.4	0.13	$\sim 10^7$	Dual channel	[13]
	ITZO	n	RF Sputtering	39.6	0.25	$\sim 10^7$	High μ (In:Sn:Zn:O = 4:4:1:15 at.%)	[41]
2015	SnO	p	DC Sputtering	2.39	7.5	$\sim 10^3$	CMOS fabrication (n-type SnO/Cu$_2$O, p-type SnO)	[42]
	IGZO	n	Co-sputtering	16.1	0.21	$\sim 10^7$	ZnO-IGZO co-sputtering	[43]
2016	ZTO	n	Remote Plasma Reactive Sputtering	15	0.55	$\sim 10^8$	Indium free	[15]
	ITZO	n	DC Sputtering	30	0.38	$\sim 10^7$	High μ	[12]
2017	IGO	n	ALD	9.45	0.26	$\sim 10^8$	Multicomponent ALD growth	[44]
	LIZO	n	ALD	40	0.13	$\sim 10^9$	Al$_2$O$_3$/MgO encapsulation / 2.2" flexible AMOLED demo	[17]
2018	IGZO	n	ALD	22.1	0.3	$\sim 10^8$	High speed ALD-IGZO	[45]
	IGZO	n	RF Sputtering	10.3	0.28	$\sim 10^7$	Low temp (200°C) flexible TFT	[8]
2019	IGZO	n	ALD	20.1	0.49	$\sim 10^7$	High-μ IGZO by ALD	[18]
	ZnO	n	ALD	36.8	0.069	$\sim 10^7$	High-k dielectric for low voltage driving	[14]
	IGZO	n	PEALD	74	0.26	$\sim 10^8$	Stacked InO$_x$, ZnO$_x$, and GaO$_x$ vertical channel	[46]
2020	IZTO	n	RF Sputtering	29.1	0.12	$\sim 10^8$	Oxygen control for the high reliability	[10]
	ZnON	n	RF Sputtering	147	0.21	$\sim 10^4$	Dual gate, PEN substrate	[128]
	IGZTO	n	RF Sputtering	46.7	0.15	$\sim 10^8$	High μ / Annealing effect	[47]

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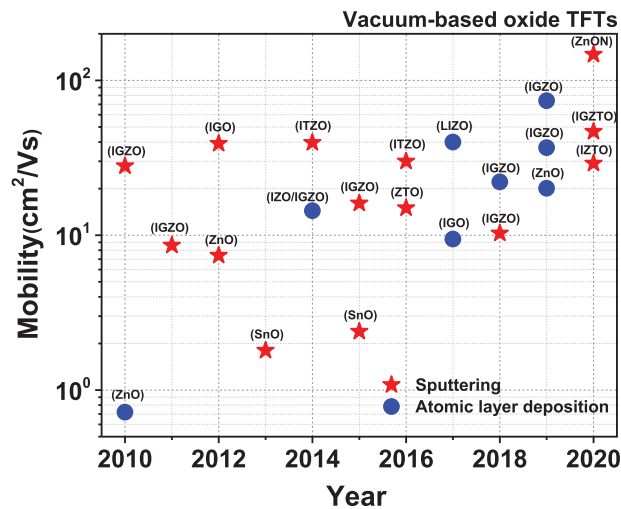
Figure 3. Carrier-mobility trends of vacuum-processed oxide TFTs for different deposition methods.

circuits that use both vacuum-based oxide TFT and LTPS to achieve low power consumption by AMOLEDs. LTPO combines LTPS switching circuits and oxide TFT driving circuits. Such hybrid circuits reduce power consumption compared to the only-LTPS backplane. However, the process requires precise control of a large number of masks and of the different material properties of LTPS and oxide TFTs.

Solution processes. Research on solution-based oxide TFTs has used diverse approaches and the results

have improved very quickly (Table 2). Achievements in solution-based oxide TFTs over the past decade can be summarized as follows: (1) low-temperature process technology by the synthesis of new precursors and the control of thermodynamic reaction [20–27]; (2) low-temperature or high μ using various post-processing methods [28–33]; (3) high-performance implementation according to changes in material composition by using spin coating, spray pyrolysis, inkjet, slot-die coating, and e-jet [7,22,34–38].

Chemical approaches have lowered processing temperatures from 600 to 150°C, and have been critically important in the development of solution-based oxide semiconductors. Combustion reaction, aqueous synthesis, and effective elimination of ligand residual have been suggested as ways to lower processing temperatures.

Post-treatment approaches have also been proposed. Examples include high-pressure annealing, wet annealing, ozone annealing, microwave, infrared annealing, and deep ultraviolet annealing. These methods improved reliability and reduced process temperatures while increasing film density. In the case of deep ultraviolet treatment, oxide TFTs operated via even room temperature processing facilitated the integration of circuits on the flexible substrate [30]. Solution materials are compatible with various deposition techniques, so researchers are trying to find a suitable direction for applications in the industry. Other methods such as spin-coating, spray pyrolysis, slot die coating, bar coating, ink-jet printing,

Table 2. Recent progress of solution-based oxide TFTs.

Year	Materials	Type	Process (Temp. °C)	μ (cm^2·V^{-1}·s^{-1})	S.S. (V·dec^{-1})	I_{on}/I_{off}	Comments	Ref.
2011	In$_2$O$_3$, ZTO, IZO	*n*	S.C.(200-400)	0.81-9.78	-	$\sim 10^6$	Combustion method	[27]
	In$_2$O$_3$	*n*	S.C.(280)	22.14	-	$\sim 10^6$	Ozone annealing	[28]
2012	IGZO	*n*	S.C.(R.T.)	14	-	$\sim 10^8$	Photo annealing at room temperature	[30]
	ZTO	*n*	S.C.(300)	1.05	0.11	$\sim 10^7$	Solution-processed HfO$_2$ dielectric and ZTO channel	[48]
	ZnO	*n*	S.C.(400)	45.5	0.18	$\sim 10^6$	All solution process (S/D, G.I, Gate, Channel)	[49]
	SnO	*p*	S.C.(450)	0.13	-	$\sim 10^2$	First *p*-type solution process	[50]
2013	In$_2$O$_3$	*n*	S.C.(250)	82	0.27	$\sim 10^3$	Solution-processed AlO$_x$ dielectric and In$_2$O$_3$ channel	[7]
	IGZO	*n*	S.C.(240)	2.04	0.84	$\sim 10^6$	IR irradiation	[32]
2014	IGZO	*n*	S.C.(200-350)	84.4	-	$\sim 10^5$	Direct light patterning of all oxide TFTs	[20]
	ITZO/IGZO	*n*	S.C.(450)	21.27	0.51	$\sim 10^7$	Heterostructure	[34]
2015	ZnO	*n*	S.P.(400)	40	-	$\sim 10^7$	Spray pyrolysis	[51]
	In$_2$O$_3$	*n*	S.C.(300)	8.84	0.92	$\sim 10^7$	Chlorine residual control	[23]
	CuO	*p*	S.C.(600)	0.29	0.8	$\sim 10^4$	Solution-processable *p*-type Channel	[33]
2016	IGO	*n*	S.C.(400)	52.6	0.16	$\sim 10^8$	Optimization of Ga contents	[52]
	IZO	*n*	S.P.(275)	6.2	-	$\sim 10^4$	Spray combustion, flexible substrate	[21]
2017	In$_2$O$_3$/ZnO	*n*	S.P.(210)	210	30	$\sim 10^6$	Ultrasonic spray pyrolysis, heterostructure	[53]
	IGO	*n*	Inkjet	350–450	11.7	$\sim 10^7$	All inkjet-printed devices	[35]
2018	IGZO	*n*	S.C.(230)	61.3	0.12	$\sim 10^6$	IR irradiation	[54]
	In$_2$O$_3$	*n*	S.P.(200)	3.67	0.18	$\sim 10^7$	Purification of HfO$_2$ precursor	[26]
2019	GTO	*n*	S.C.(350)	69	0.08	$\sim 10^7$	Al$_2$O$_3$ dielectric	[55]
	IGZO	*n*	S.C.(300)	2.5	2.0	$\sim 10^6$	DI water solvent	[22]
2020	IZO	*n*	S.C.(370)	1.4	-	~ 10[10]	Na$_2$CO$_3$ as a mild resist developer for the suppressing of chemical damage to IZO	[56]
	InSmO	*n*	S.C.(350)	21.51	0.66	$\sim 10^8$	Oxygen vacancies are suppressed by Sm / Aqueous synthesis	[36]

and electrohydrodynamic-jet printing, have also been studied. Research on device optimization and role of composition variation has also been approached in various ways.

Over the past 10 years, the carrier mobility of solution-based oxide TFTs has significantly increased. Its reliability is still inferior to those vacuum-fabricated devices, but it has consistently improved (Figure 4). The characteristics of vacuum-based p-type SnO and Cu$_2$O have steadily improved. Solution-based p-type oxide TFTs have been reported since 2014, and their characteristics are also expected to be improved.

The recent research strategies for Oxide TFTs have been facing a new turning point described as follows: (1) implementing small and medium display backplane technology to replace LTPO or LTPS by using oxide TFTs that have $\mu \sim 100$ cm^2·V^{-1}·s^{-1} to implement various logics that use CMOS; (2) high-μ p-type oxide TFTs; and (3) commercialization of solution-based oxide TFTs for low-cost display backplanes. Research on oxide semiconductors shows no sign of slowing and significant progress is expected.

3. Semiconducting CNT TFTs

CNTs have unique optical and electrical properties, which are consequences of the energy-band structure of quasi-one-dimensional nanowire. A single CNT itself has excellent mechanical properties, and a CNT network can be applied to flexible, stretchable, and even wearable displays [57–59].

To utilize semiconducting CNTs as the active layer in a TFT, they must be synthesized at high purity. However, existing synthesis methods do not permit easy control of the electrical properties of CNTs. These properties result from its cylindrical structure, or 'chirality', and semiconducting CNTs that have specific chiralities can be sorted from CNT bundles by a subsequent process, such as density gradient ultracentrifugation (DGU), [60] DNA wrapping, [61] gel chromatography, [62] aqueous two phase (ATP) extraction [63] or conjugated polymer wrapping (CPW) [64]. DGU and CPW processes have been developed for commercial mass production. Flexible, large-area display with CNT TFTs would be manufactured using high-purified semiconducting CNT ink that is produced by these sorting processes at low temperature and low cost.

The performances of CNT TFTs are affected by many factors, including CNT network morphology, contact resistance, and interface between dielectric and semiconductor layer (Table 3). To achieve high μ of CNT TFTs, intertube junctions should be reduced in the CNT network by using alignment methods, including dielectrophoresis, [65] Langmuir–Blodgett (LB), [66,67] and

Table 3. Representative structures and carrier mobilities μ of CNT TFTs.

| | | | | μ (cm^{2}V^{-1}s^{-1}) | | | |
CNT type	Deposition technique	Dielectric	Contact	μ_h	μ_e	I_{on}/I_{off}	Ref.
FC-CVD	Transfer	SiO$_2$	Au	35		$\sim 10^6$	[57]
Arc discharge	Immersion	Al$_2$O$_3$	Ti/Pd	32		$\sim 10^5$	[58]
Arc discharge	Langmuir–Blodgett	SiO$_2$	Pd	~ 100		$\sim 10^6$	[67]
Arc discharge	Blade coating	SiO$_2$	Au	50		$\sim 10^5$	[69]
HiPCO	Blade coating	SiO$_2$	Au	16			[72]
HiPCO	Blade coating	SiO$_2$	Au		5		[72]
CoMoCAT	Spin coating	PMMA/HfO$_2$	Au		10	$\sim 10^8$	[82]
Arc discharge	Aerosol jet	Ion gel	Au	50	50	$\sim 10^4$	[83]
Plasma torch	Spin coating	PMMA/HfO$_2$	Au	50	50	$\sim 10^6$	[84]
TUBALL	dip coating	SiO$_2$	Pd	13		$\sim 10^2$	[85]
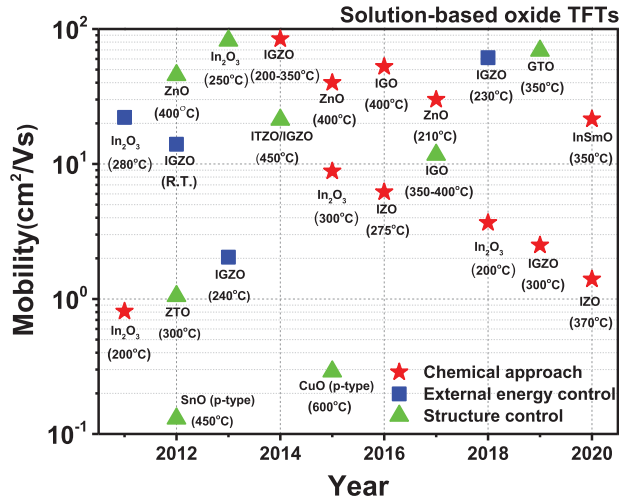
Figure 4. Carrier-mobility trends of solution-processed oxide TFTs for different deposition methods.

blade coating [68,69]. Furthermore, the Schottky barrier of TFTs decreases as the diameter of the CNTs increases [70].

Additives to a CNT solution, or a doping layer atop the CNT layer, can increase the charge-carrier density of the active layer. For example, the hole current can be slightly increased by the strong electron affinity of tetrafluorotetracyano-p-quinodimethane (F4TCNQ), p-dopant [71,72]. In contrast, electron density can be increased by application of n-dopants such as Polyethylenimine (PEI) [73,74] and dimethyl-dihydro-benzoimidazoles (DMBI) [72,75].

Doping can modify the interface between the semi-conductor layer where various types of traps occur and the channel is accumulated [76]. Fabricated CNT TFTs on SiO$_2$ show strong p-type behavior and large hysteresis due to the hydroxyl group of SiO$_2$, although CNTs are intrinsically ambipolar [77]. In nano-sized CNT TFTs, contact resistance greatly contributes to nonideal charge injection [78]. To reduce the injection barrier, a charge-transfer layer is lain over the contact metal and the

electrodes are replaced with metals that have low work function [79,80].

Knowledge gained by these studies has guided applications of CNT TFTs to drive displays, and much effort has been devoted to applying CNT TFTs in the backplane of large-area displays. For that use, the density of CNTs must be finely adjusted on nano-sized transistors, and uniform brightness requires development of a technology to remove CNT aggregates [81].

4. TFTs based on 2D van der Waals semiconductor

2D transition metal dichalcogenides (TMDCs) have high μ, high optical transmittance, and high mechanical flexibility, which are superior to bulk counterparts. Such exceptional properties can be exploited as backplane transistors for displays. However, the combination of TMDC with metals has high contact resistance R_C, which degrades μ, on/off-current ratio I_{on}/I_{off}, and subthreshold swing SS of devices that use them. This disadvantage has hindered integration of TDMC-based TFTs into display backplanes.

Methods proposed to reduce R_C include several approaches to improve the contact properties of TMDCs, including molecular doping [86], phase engineering [87], graphene contact [88,89] and van der Waals clean interface contacts [90,91]. Molecular doping has been extensively used because it is simple and scalable. Doping with polyethylenimine (PEI) molecules significantly increased μ and I_{on} of MoS$_2$ FETs as a result of the reduced R_C (2.28 kΩ·μm) [86].

Use of graphene as a metallic electrode reduce R_C in MoS$_2$ devices [88]. The tunability of the graphene Fermi level was exploited to reduce R_C of a MoS$_2$ FET to 3.7 kΩ μm, with high I_{on}/I_{off} $\sim 10^7$ and a high field-effect $\mu = 32.3$ cm^2·V^{-1}·s^{-1}.

Recent studies have demonstrated ultraclean van der Waals interface contacts formed by transferred metal electrodes [90] and indium/gold electrodes [91]. These
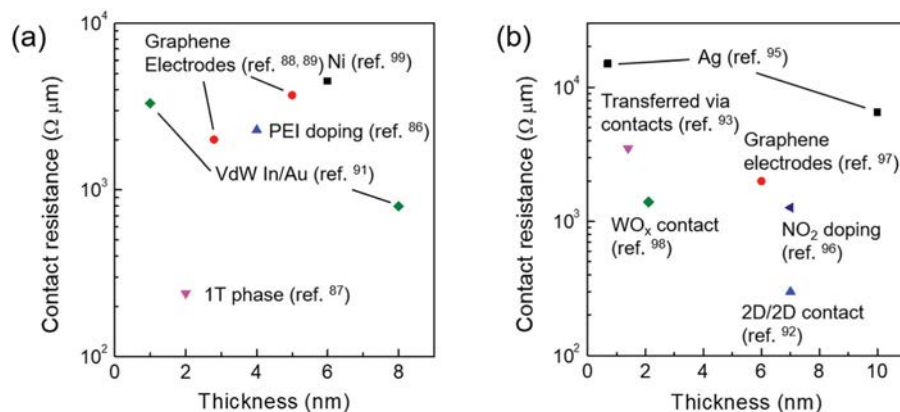
Figure 5. Comparison of contact resistance as a function of thickness for (a) MoS_2 and (b) WSe_2.

Table 4. Recent representative results of 2D TMDC-based TFTs.

Channel material (thickness)	Contact strategy	Contact resistance [$k\Omega\ \mu m$]	I_{on}/I_{off}	μ [$cm^2\ V^{-1}\ s^{-1}$]	Year	Ref
Exfoliated MoS_2 (6 nm)	Ni	4.5	-	48 (electrons)	2012	[99]
Exfoliated MoS_2 (4-5 nm)	PEI doping	2.28	10^5	33 (electrons)	2013	[86]
Exfoliated MoS_2 (2-3L)	Metallic 1 T phase	0.24	10^8	46 (electrons)	2014	[87]
Exfoliated MoS_2 (5-6 nm)	Graphene	3.7	10^7	32.3 (electrons)	2014	[88]
Exfoliated MoS_2 (4L)	Graphene	2	-	40 (electrons)	2015	[89]
MoS_2 (4-20 nm)	Transferred metal	-	10^6	260 (electrons)	2018	[90]
CVD-MoS_2 (1L)	Van der Waals In/Au contact	3.3	10^6	170 (electrons)	2019	[91]
Exfoliated MoS_2 (8.1 nm)		0.8	10^5	-		
WSe_2 (1L)	Ag	15	10^7	44 (holes)	2013	[95]
WSe_2 (10 nm)		6.5	-	-		
WSe_2 (7 nm)	NO_2 doping	1.27	10	-	2014	[96]
WSe_2 (9L)	Graphene	2	10^7 (170 K)	204 (holes; 160 K,)	2014	[97]
WSe_2 (3 L)	WO_x contact	1.4	10^7	31 (holes)	2016	[98]
WSe_2 (10L)	2D/2D contact	0.3	10^9	200 (holes)	2016	[92]
WSe_2 (2L)	Transferred via contacts (TVCs)	3.5	10^6	160 (holes)	2019	[93]

electrodes can form clean and defect-free interface with TMDCs to yield low R_C and high electron mobility μ_e.

WSe$_2$ is a TMDC material that exhibits p-type or ambipolar characteristic and has been extensively investigated for use in 2D electronic devices that are complementary to n-type TMDCs. However, the Schottky barrier between metal and WSe$_2$ is high, so R_C is large and the electrical characteristics of WSe$_2$ FETs was inferior to whose of MoS$_2$ FETs. Thus, several strategies have been undertaken to improve the contacts to WSe$_2$. A WSe$_2$ FET with 2D/2D contact was demonstrated, in which degenerately p-doped WSe$_2$ contacts interfaced directly with an undoped WSe$_2$ channel [92]. Recently, a high-quality WSe$_2$-based FET was achieved using transferred *via* contacts (TVCs) [93].

Although rapid progress has been made over the decade (Table 4, Figure 5) [86–99], emphasis should be placed on scaling and large-scale fabrication. Research should focus on contact engineering to reduce R_C and improve the electrical characteristics of scaled FETs. Moreover, growth methods that can create large-area 2D materials must be developed. Most of the research

reported to date has used mechanically exfoliated flakes (micrometer-scale), which are not adaptable to practical applications. Although wafer-scale MoS$_2$ growth has been demonstrated [94], growth of other 2D materials, such as WSe$_2$, and MoTe$_2$, is still in the early stages of development.

5. Organic TFTs

Organic semiconductors (OSCs) are flexible, so they can be applied to flexible, large-area display applications. OSCs can be synthesized in a nearly infinite number of molecular structures with unique properties by applying design rules.

Small-molecule OSCs with highly ordered crystalline domains can be deposited by thermal evaporation or by a solution process. An organic TFT (OTFT) with pentacene was initially fabricated using thermal evaporation [100]. An ultra-flexible OTFT composed of a soluble small molecule, bis-(triisopropylsilylethynyl) pentacene (TIPS-pentacene), has been fabricated using a solution process [101]. An inkjet-printed OTFT composed of

Table 5. Representative structures and carrier mobilities of OTFTs.

Semiconductor	Deposition technique	Structure	Dielectric	μ_h	μ_e	Ref.
				μ ($cm^2 \cdot V^{-1} \cdot s^{-1}$)		
Pentacene	Evaporation	BG/TC	PVP	3		[100]
TIPS-pentacene	Blade coating	BG/TC	SiO_2	11		[127]
C_8-BTBT	Inkjet	TG/BC	Parylene C	30		[102]
P(NDI2OD-T2)	Bar coating	TG/BC	PMMA		6.4	[104]
IDT-BT	Spin coating	TG/BC	CYTOP	2.5		[113]
DPPT-TT	Off-center spin coating	TG/BC	PMMA	2		[115]
DPPT-TT	Bar coating	TG/BC	PMMA	2.8		[116]
DPPT-TT	Slot-die coating	BG/TC	AlO_x	10.2		[117]

2,7-dioctyl[1]benzothieno[3,2-b][1] benzothiophene (C_8-BTBT) achieved a hole mobility $\mu_h \sim 30$ $cm^2 \cdot V^{-1} \cdot s^{-1}$ [102].

π-Conjugated polymer semiconductors are generally deposited using a solution process and their solubilities are controlled by adjusting the length of the alkyl chain. Close $\pi-\pi$ stacking distance increases charge-transport efficiency in polymer thin-film, so various polymers that include planar moieties such as naphthalene diimide (NDI) [103,104], diketopyrrolopurrole (DPP) [105–109] have been developed to achieve high μ.

To adjust the lowest unoccupied molecular orbital and highest occupied molecular orbital levels, Donor–Acceptor (D-A) alternating copolymers have been synthesized with electron-rich moieties as donor units and electron-poor moieties as acceptor units [110,111]. Recently, one D-A copolymer, Indacenodithiophene-co-benzothiadiazole (IDT-BT) has been reported to show disorder-free charge transport due to the flattened energy orientation along a torsion-free backbone [112,113]. The orientation of the OSC film has been modified physically by uniaxial alignment processes such as off-center spin coating [114,115], bar coating [116], slot-die coating [117], which apply shearing force to the polymer solution in one direction.

Interface engineering can be used to reduce the trap density in polymer film and thereby guarantee reliable and stable electrical characteristics of TFTs. Blending additives with OSCs can increase their chemical stability in the air. In a representative study, the added small molecules into IDT-BT prevented nanometer-scale voids from adsorbing water molecules, and thereby inhibited charge trapping and device degradation [118]. Use of inorganic SiO_2 has the disadvantage that its hydroxyl group is an electron trap that degrades the n-type electrical characteristics of OTFTs, but when a polymer insulator is used, the OTFT shows ambipolar characteristics [119].

Conventional OTFTs have a strong Schottky barrier at the metal–semiconductor interface; and this barrier is a critical obstacle to efficient charge injection [120–123]. To obtain Ohmic contact, several strategies for energy level alignment have been demonstrated. Contact doping has been studied widely as one facile method to realize Ohmic contact. High μ_e can be obtained by covering the electrode with an interlayer such as CsF [124], DMBI [125] or pyronin B [126].

In the last decade, tremendous progress has been made in the field of organic electronics (Table 5). Advances include design rules for synthesis, a simplified deposition process, interface engineering, doping techniques, and analysis of charge-carrier density and charge transport. Many reported OSCs have higher μ than that of a-Si. Integrated circuits that use OTFTs have been developed. Further research should focus on translating single-OTFT devices to large-area arrays deposited by in-air Roll-to-Roll processing for mass production.

6. Conclusion and perspective

This paper has reviewed the current state of research on backplane TFTs for rigid and flexible OLED displays, including amorphous metal oxides, CNTs, TMDCs, and organic semiconductors. Existing LTPS TFTs suffer from high manufacturing cost, high I_{off} and low uniformity of electrical characteristics over large areas. These demerits provide the main motivation for the development of new TFT materials. Mechanical flexibility of semiconducting materials is required for flexible OLED backplane but this requirement is not strict because the effective TFT area in OLED display is small. Replacement of conventional vacuum-deposition methods by solution-based techniques has recently been pursued, particularly towards cost-effective manufacturing. Many pioneering display-panel companies have recently run pilot lines that use inkjet printing to manufacture front panels for OLED displays. After front-panel production using inkjet printing is commercialized, the next goal would be back plane production. With this goal in mind, printable channel materials have been studied for a decade and should be optimized in the future.

Disclosure statement

No potential conflict of interest was reported by the author(s).

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