The TFT—A New Thin-Film Transistor*

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Summary—**A thin-film transistor, TFT, fabricated by evaporation of all components on to an insulating substrate has been developed. Operation is based upon the control of injected majority carriers in a wide-band-gap semiconductor by means of an insulated control gate. Experimental units using microcrystalline layers of cadmium sulfide have yielded voltage amplification factors greater than 100, transconductances greater than 10,000 μmho, input impedances greater than 10^6 Ω shunted by 50 pf and gain-bandwidth products greater than 10 Mc. Switching speeds of less than 0.1 μsec have been observed.**

Simple evaporated thin-film circuits incorporating the TFT have been built. Direct coupling between stages is permitted since the insulated gate electrode can be biased positively as well as negatively without drawing appreciable gate current. Modified forms of the TFT have been built for use as a flip-flop, an AND gate and a NOR gate in computer applications.

I. Introduction

THE POTENTIAL advantages of thin-film circuits have been largely unrealized to date because of the lack of a thin-film transistor which could be deposited by the same techniques upon an insulating substrate. The present paper will describe a new high-gain transistor[1] for which all components including the semiconductor and metal electrodes are deposited by evaporation upon a glass plate.

Owing to the extremely short lifetime of minority carriers in microcrystalline films it was assumed at the start of this development that a majority carrier type of thin-film triode had a greater probability of success than a bipolar type of transistor. Majority carrier transistors were proposed [1] as long ago as 1935 and have been investigated in various laboratories [2]–[4]. The best known of these is the Shockley unipolar [2] field-effect transistor based upon the pinch-off of a conduction channel by the expansion of the depletion layer in a back-biased *p-n* junction.

More recently, papers on a field-effect photo-transistor [5] and an analog transistor [6] using majority-carrier conduction in cadmium sulfide crystals have appeared. While the relatively low mobility of electrons in cadmium sulfide would not appear to recommend the material for a conventional transistor, cadmium sulfide offered some attractive features for exploratory studies of a thin-film triode. Single crystals of cadmium sulfide had been studied extensively [7], and considerable technological experience with thin films of cadmium sulfide had been acquired in the fabrication of photoconductive devices [8]. In addition, the wide-band-gap of cadmium sulfide made it well suited for the study of space-charge-limited currents in insulators [9], [10], a phenomenon which offered considerable potential for the development of new devices [6], [11]–[13].

The present investigation has yielded a new thin-film transistor [13] called the TFT whose performance utilizing microcrystalline layers of cadmium sulfide approaches that of commercial transistors made of single-crystal germanium or silicon. The surprisingly good performance of the TFT is due partly to the use of evaporation techniques which permit very small electrode spacings and gate widths. More important, however, has been the development of an insulating gate contact which permits operation in either the enrichment or depletion mode without drawing appreciable gate current. The enrichment mode is of particular interest from the standpoint of thin-film circuits since it permits direct coupling between stages. This mode of operation has not been used to date in commercially available transistors, although the effect was noted in some early experiments on "conductivity modulation" by Shockley and Pearson [14]. Recently, several single-crystal devices having an insulated control gate have been reported [15], [16]. The enrichment mode of operation has been discussed in connection with the "Electrolyte Field Effect" [17], "the Surface Field Effect Transistor" [15], the "Surface-Potential Controlled Transistor" [16], and the "Chargistor" [18].

The fabrication techniques employed in making the TFT are equally suitable for depositing interconnections and associated resistors, capacitors and diodes. Complete functional circuits containing many active and passive components can thus be fabricated in a single operation. As a simple illustration of the potential applications of the TFT a multistage thin-film amplifier was built. Other modifications of the TFT designed for particular circuit functions in computers will be described. These include an AND gate, a NOR gate and a simple flip-flop element.

II. Description of the Insulated-Gate TFT Structure

Fig. 1 illustrates one form of TFT which has yielded excellent results. The semiconductor film in most cases has been a microcrystalline layer of cadmium sulfide. The "source" and "drain" electrodes are ordinarily formed of metals which make a low resistance contact to the semiconductor. Evaporated gold is suitable for cadmium sulfide. The "gate" electrode may also be of gold but the contact must be formed in such a manner that a thin film of insulator is interposed between the metal electrode and the semiconductor. The thickness of the semiconductor is usually less than one micron and the source-drain spacing has been in the

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[1] The word transistor is used in its broadest sense here. The mode of operation of the device to be described is different from either the conventional unipolar or bipolar transistor.

range of 5 to 50 microns. The gate electrode is separated from the semiconductor by means of a thin evaporated layer of insulating material such as silicon monoxide. Fig. 2 shows a 1-in square glass plate (mounted on a lucite block) upon which three such transistors have been evaporated.

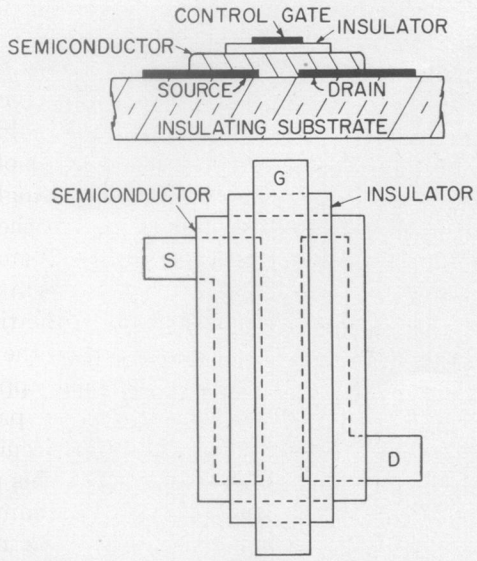

Fig. 1—Cross-sectional and plan view of an evaporated thin film transistor. The thickness of the evaporated layers is shown greatly exaggerated as compared to the lateral dimensions and to the thickness of the substrate.

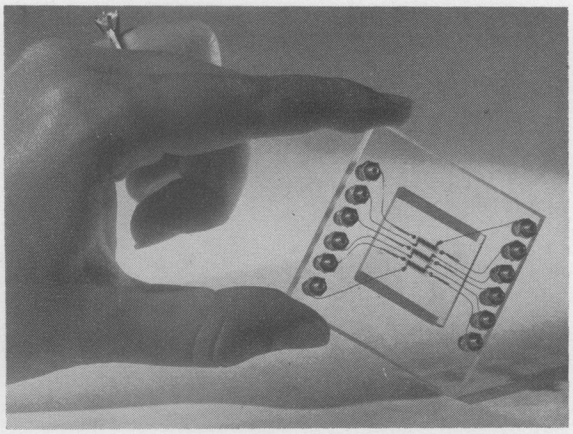

Fig. 2—A 1-in square glass plate (mounted on a lucite block) upon which 3 TFT's have been deposited.

A plot of drain current versus drain voltage for various values of positive gate bias is shown in Fig. 3 for one experimental unit. Since the drain current increases by a factor of 10 to 1000 as the gate bias is raised from zero to several volts positive, this type of operation is called the "enrichment" or "enhancement mode." This mode is to be contrasted with the "depletion mode" used in the conventional form of unipolar transistor having a *p-n* junction at the gate. In the depletion mode maximum useful drain current is obtained at zero gate bias while a negative gate bias "pinches off" the source-drain current by expanding the depletion layer. Although the TFT's can be designed for operation in either or both the enrichment and depletion mode, somewhat higher values of transconductance are usually obtained with the enrichment mode. The insulated gate permits operation in either mode without drawing appreciable gate current. Fig. 4 shows the characteristic curves of a TFT which operates with a gate bias near zero in either the enrichment or depletion mode.

The performance of the TFT can be predicted from the characteristic curves and a knowledge of the input capacitance. The unit shown in Fig. 3 has a transconductance of 5000 μa/v at a drain current of 6.5 ma and a gate bias approximately the same as the drain voltage. The voltage amplification factor derived from the curve is 50. The measured input capacitance of this unit was 300 pf, although this value was considerably larger than necessary. The gain-bandwidth product can be calculated from the approximate relation,

$$\text{G.B.} = \frac{g_m}{2\pi C_g} \tag{1}$$

where g_m and C_g are the transconductance and input capacitance, respectively. A value of 3 Mc was obtained, which is in good agreement with the measured frequency response curves on this unit.

More recently, TFT's similar to the above unit have been made with values of g_m as high as 25,000 μa/v for an input capacitance of less than 50 pf. Such units have yielded experimental gain-bandwidth products of about 12 Mc although the g_m/C ratio would indicate considerably higher capabilities. Oscillations have been obtained at frequencies up to 17 Mc, but no particular care has been taken to design the units for high frequency operation. All of the results quoted here were obtained with microcrystalline films of cadmium sulfide. There is excellent reason to believe that the performance can be extended considerably beyond the present values either by improved processing of the cadmium sulfide or by the use of a different semiconductor.

Although cadmium sulfide is an excellent photoconductor, no attempt was made in the above units to process the TFT's for maximum photosensitivity. The results quoted were obtained with the units in the dark. The effect of light, however, is to increase the transconductance for operation in either the enhancement or depletion mode. Fig. 5 shows characteristic curves for a unit operating in the enhancement mode in the dark and in the presence of light.

III. Physical Processes in the TFT

An approximate description of the operation of the insulated-gate TFT can be derived from consideration of a typical field-effect experiment [19], [20] such as used in the study of semiconductor surfaces. In this type of experiment a transverse field is applied to the surface of the semiconductor by means of a close-spaced metal plate. That part of the charge induced in the semiconductor surface which is not bound in surface states

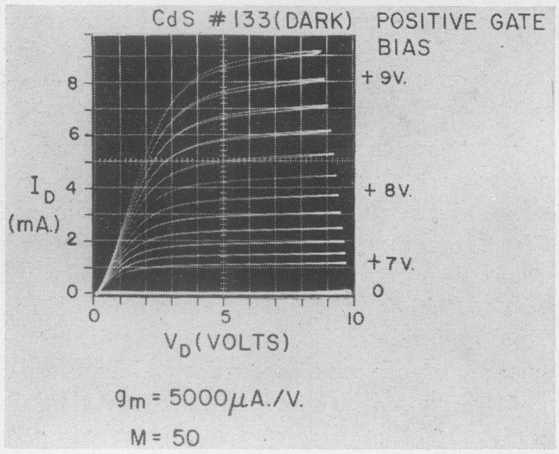

Fig. 3—Characteristic curves for an experimental cadmium sulfide TFT designed for operation in the "enrichment" mode. Drain current is plotted against drain voltage for different values of positive gate bias. (Source is grounded.) These curves were taken with the TFT in the dark.

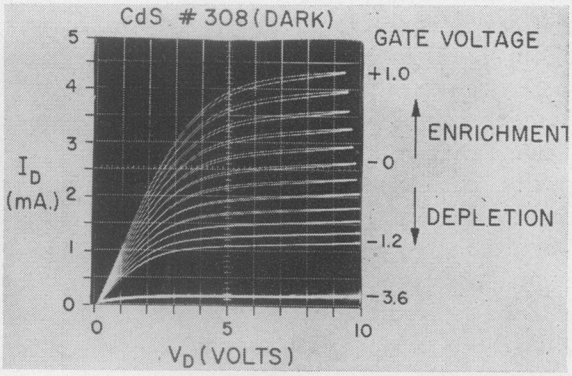

Fig. 4—Characteristic curves for an experimental TFT designed for operation in either the "enrichment" or the "depletion" mode. The hysteresis effect yielding the small loops noted in some units is now undergoing study.

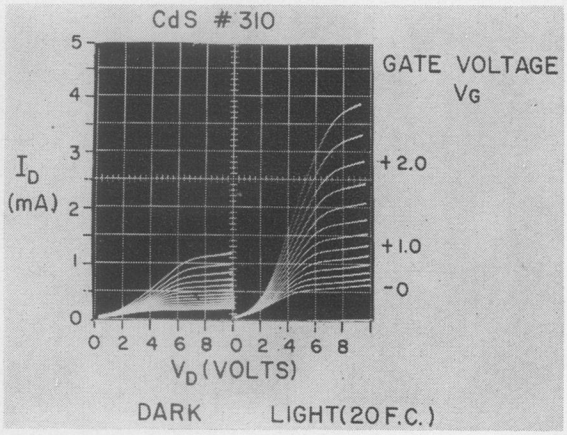

Fig. 5—Characteristic curves for an experimental TFT showing the effect of light. (Cadmium sulfide semiconductor.)

or other immobile sites will appear as a change in density of the mobile carriers. The surface conductivity can thus be either enhanced or diminished by the field plate by an amount depending upon the potential applied and the nature of semiconductor-insulator contact.

The TFT differs from most of the above field-effect experiments in the use of smaller dimensions and in the choice of a wide-band-gap semiconductor such as cadmium sulfide. In such a material the thermally-generated carrier density is small compared to the density of majority carriers which can be injected from the source electrode. With a suitable low resistance contact at the source, current densities of the order of hundreds or thousands of amperes per square centimeter can be drawn through the cadmium sulfide film in spite of its normally high resistance.

Fig. 6 shows an energy band picture of the contacts used at the source and gate electrodes in a TFT. At zero bias in a unit designed particularly for operation in the enhancement mode, the bands should bend up at the semiconductor-insulator interfaces as shown. When the gate is biased positively, electrons are drawn toward the interface, causing the bottom of the conduction band at the interface to be lowered relative to the Fermi level giving a highly conducting channel close to the insulator surface. (The small voltage drop in the semiconductor across the thickness of the layer is ignored in this drawing.) Conversely, a contact designed for the depletion mode of operation would aim to have a conducting surface channel present initially at zero gate bias which

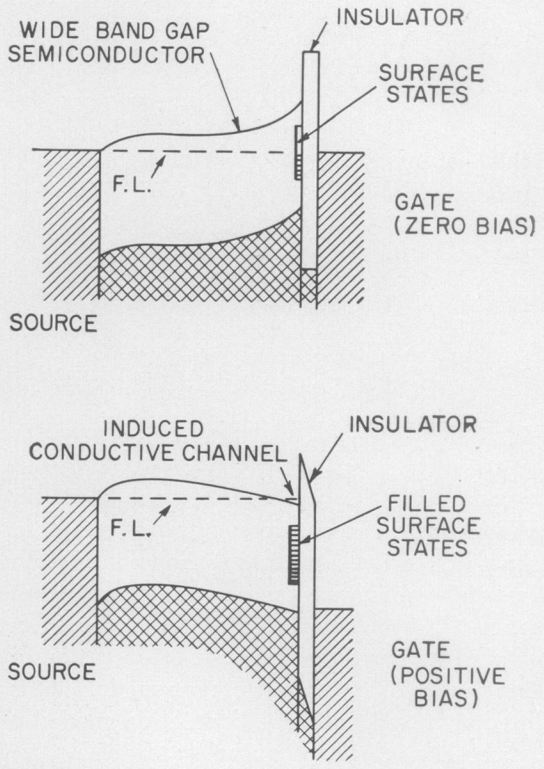

Fig. 6—An energy band picture of the "ohmic" source contact and the insulated-gate contact in a TFT designed for operation in the enrichment mode.

would then be depleted by operation with a negative gate bias.

An approximate expression for the transconductance of the TFT, based upon the above field-effect considerations, may be derived as follows: Consider a thin sheet of semiconductor of area $L \cdot W$ and a thickness h, separated from a close-spaced field plate by a thin dielectric spacer of thickness t. (See Fig. 7.) The dimensions L and W are assumed to be large compared to the film thicknesses, t and h. The positive potential V_g applied to the field plate (or gate) is assumed to be large compared to the potential difference between source and drain. A small increase in gate potential ΔV_g will draw Δn electrons/cm^3 into the semiconductor given by

$$\Delta n = \frac{\text{total charge drawn in}}{e \cdot \text{total volume}} = \frac{C_g \cdot \Delta V_g}{e \cdot L \cdot W \cdot h}. \qquad (2)$$

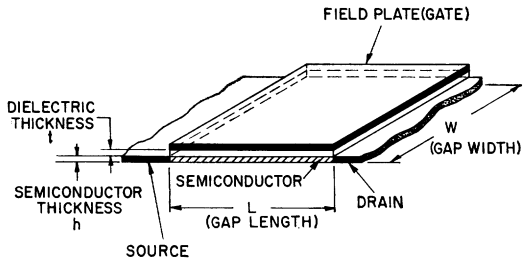

Fig. 7—Field-effect structure equivalent to the insulated-gate TFT.

The resulting increase in source-drain current is approximately

$$\Delta I_D = V_D \cdot \frac{Wh}{L} \Delta\sigma = V_D \cdot \frac{Wh}{L} \Delta n e \mu_d \qquad (3)$$

where

$\Delta\sigma$ = the change in conductivity of the semiconductor produced by the change in gate potential ΔV_g,
V_D = the source-drain potential difference and
μ_d = the effective drift mobility of the Δn electrons.

Combining (2) and (3) we obtain

$$\frac{\Delta I_D}{\Delta V_g} \cdot \frac{1}{C_g} = \frac{\mu_d V_D}{L^2} \quad \text{or} \quad \frac{g_m}{C_g} = \frac{\mu_d V_D}{L^2}. \qquad (4)$$

The significance of small source-drain spacings is apparent since the gap length L is squared. The thickness of the dielectric spacer t and the width of the gate W appear implicitly in (4) in the gate capacitance. If we solved directly for g_m we would have

$$g_m = \frac{kW}{t} \frac{\mu_d V_D}{L} \qquad (5)$$

where k is the dielectric constant of the dielectric spacer. In general, (4) is more useful than (5) since g_m/C_g may be substituted in (1) to give the gain-bandwidth product of the device. It may be noted that the right-hand side of (4) is simply the inverse of the transit time of the electrons between the source and drain if the field were uniform.

In deriving (4) it was assumed that the drift mobility μ_d was a constant independent of variations in V_g. This is true in wide band-gap materials only under certain conditions. When the semiconductor contains many traps or surface states, the large fraction of trapped electrons may cause the effective drift mobility to be much smaller than the microscopic or Hall mobility by the factor θ:

$$\mu_d = \mu_D \cdot \theta = \mu_D \frac{n_F}{n_F + n_T} \qquad (6)$$

where

μ_d = effective drift mobility in the presence of traps,
μ_D = true drift mobility, which is assumed here to be equal to the Hall mobility,
n_F = is the free carrier density and
n_T = is the density of trapped carriers.

As the gate is made positive nearly all of the initial carriers drawn into the semiconductor may fall into the traps giving only a small increase in conductivity. For these electrons the effective drift mobility and the value of θ are very small. However, as the gate bias is further increased, most of the available traps should become filled (or otherwise inactivated) giving much larger increases in conductivity of the semiconductor. Under these conditions the drift mobility μ_d should approach a constant value equal to the Hall mobility ($\theta = 1$) and the g_m should become a constant independent of gate bias as predicted by (4).

The experimental results are in only partial agreement with the above analysis. The initial slow rise of drain current with gate voltage followed by a rapid rise at a large positive bias observed in Fig. 3 is consistent with the need for filling the surface states and traps to obtain adequate drift mobility. The surface state density for this unit calculated from the gate bias and gate capacitance is of the order of 10^{12} to 10^{13} per square centimeter, a not unreasonable value. However, as shown in Fig. 4, CdS units can be made which do not require a large positive gate bias for satisfactory operation. In such units the trapping state density is either much smaller or the traps have been filled by other processes.

The incorporation of shallow donors into the surface layer or the generation of free electrons by absorption of light represent two alternative ways of filling the traps.[2] Fig. 8 shows the variation in drain current with gate voltage for units having the two types of characteristics shown in Figs. 3 and 4.

[2] An entirely different process for neutralizing the effect of traps in the TFT is by emptying traps rather than by *filling* them. (See Bube [21].) Although sufficiently high fields may exist under some conditions in the gap region to empty shallow traps by impact ionization, it is not yet clear whether or not this process is a significant one in the TFT.

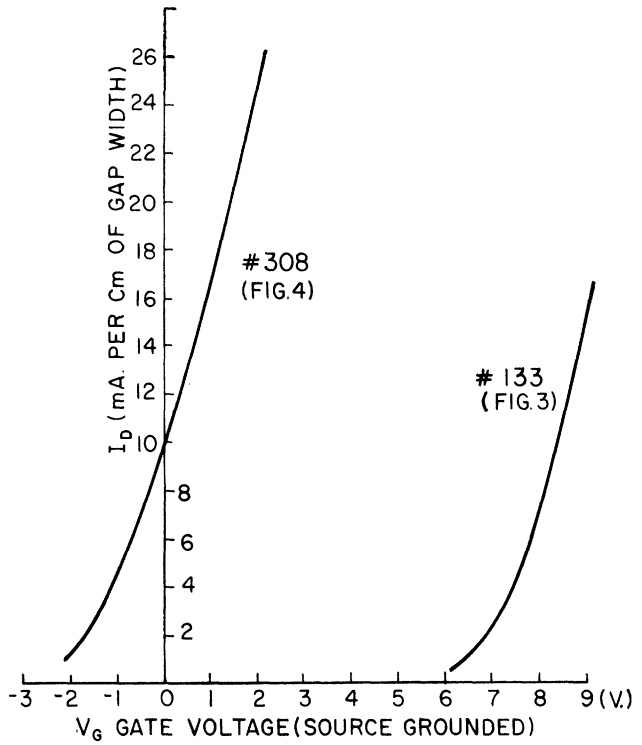

Fig. 8—Drain current versus gate voltage characteristics for TFT's of the types shown in Fig. 3 and 4.

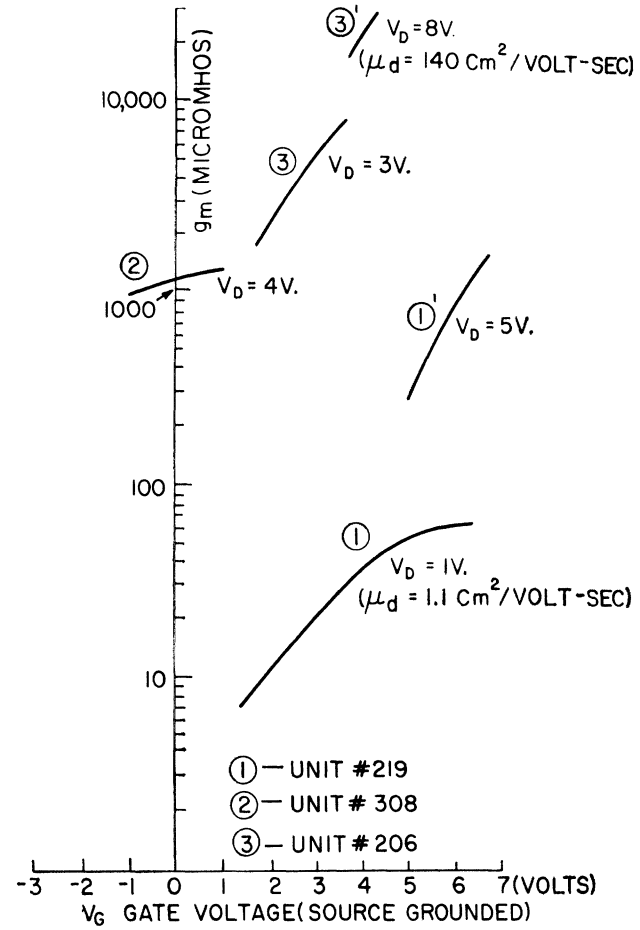

Fig. 9—Transconductance-versus-gate voltage for selected TFT's.

In Fig. 9 the experimental values of transconductance for widely differing units have been plotted as a function of gate bias. A log scale was chosen for g_m simply to accommodate the large range of data selected. From the above discussion one would expect g_m to reach a constant value at high positive gate biases as the effective drift mobility approaches the Hall mobility. Such a leveling off does indeed occur in curve 1 for drain voltage equal to 1 volt. The drift mobility could then be calculated from the g_m and the gate capacitance by the use of (4). For this calculation C_g was measured with an LC meter at a frequency of 150 kc and a normal positive gate bias. (The change in C_g with bias is usually less than 25 per cent.) The drift mobility computed in this manner was 1.1 cm²/v-sec, in fair agreement with independent measurements [11] of Hall mobility on polycrystalline cadmium sulfide layers. In curve 2 the g_m approaches a constant value of 1200 for $V_D = 4$ v, yielding a drift mobility of 6 cm²/v-sec. Curve 3 shows little tendency for g_m to reach a constant value even at low drain voltages.

It is clear that (4), which was derived assuming low drain voltages and a constant mobility, is inadequate for units operating with higher drain voltages as illustrated in curves 3 and 3′. Although the control mechanism in this case is probably more complex than can be explained solely by field effect considerations, it is interesting to use (4) as before to calculate the effective drift mobility. For curve 3′, μ_d was found to be 140 cm²/v-sec, a value considerably higher than would be expected from Hall mobility measurements on polycrystalline cadmium sulfide films. The reasons for this discrepancy are now being investigated. However, regardless of the explanation this result is exceedingly encouraging from the standpoint of device performance. Such performance makes a striking contrast with the early experiments on conductivity modulation [14] with evaporated germanium where the surface state density was so large as to severely limit the control action of the gate.

At drain voltages exceeding the gate bias the drain current in the usual TFT will saturate with drain voltage as shown in Fig. 3. This saturation effect is very important from the operational standpoint, since it is required for high voltage amplification factors. A rigorous analysis of the effect for the enrichment mode of operation is not presently available. From simple field-effect considerations, however, the saturation of drain current can be "explained" in terms of the following model: When the drain voltage becomes more positive than the gate, the induced channel adjacent to the insulator would be completely pinched off at the drain end were it not for the high field extending in from the drain. Owing to the thinness of the layers, however, the lateral component of the electrostatic field from the drain can penetrate only a short distance beneath the gate. The particular equipotential surface in the channel whose potential is equal to gate voltage thus remains relatively close to the drain electrode regardless of an increasing

drain voltage. The total current is limited by the electron flow *entering* this high field region, which, for drain voltages exceeding the gate voltage is consequently controlled by the gate voltage alone.[3] The failure of the drain current to completely saturate in practice would result from the gradual widening of the high field region due to incomplete shielding of the gate electrode. At much higher drain voltages (*e.g.*, 20 v in some cases) the drain current may again start rising rapidly with drain voltages. In terms of the above picture this effect could be caused by avalanche breakdown in the high field region near the drain, hole injection from the drain, or, in poor units, by leakage across the gate insulator.

The question of saturation of drain current in the TFT is considerably more complex than the preceding discussion would indicate. Experimental units have been made which gave large enhancement currents without saturation at drain voltages considerably exceeding gate voltage (see Fig. 10). Failure to saturate can arise from the existence of non-modulated current paths existing in series or in parallel with the conduction channel. Such characteristics would also be expected if the high resistivity region near the drain were prevented from forming. This might occur due to a premature setting in of any of the conditions enumerated above normally giving the second rise in current at high drain voltages.

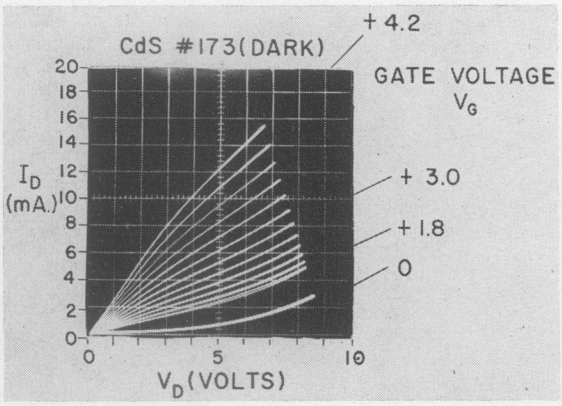

Fig. 10—Characteristic curves for a TFT showing failure of I_D to saturate.

It is not surprising that all aspects of the various TFT characteristics do not appear to be accounted for by field effect considerations. The spacings involved in the insulated-gate structure are finer and the stand-off insulator considerably thinner than normally found in field-effect experiments.[4] Although such dimensions permit the relatively high values of g_m and g_m/C which have been observed, close spacings may also introduce other phenomena, such as hot electron effects, diffusion of minority carriers and tunnelling phenomena. In spite of the added complexity introduced by such effects, they enhance the interest in the TFT from both the physics and the device application standpoint.

[3] In units which saturate at drain voltages less than gate voltage, the equipotential surface separating the low field region from the high field region will be correspondingly less than gate potential.

[4] DeWald in [17] achieved the equivalent of a very thin insulating spacer by the use of an electrolyte as a gate electrode.

IV. Alternate Forms of TFT's

Fig. 11 illustrates structural variations of the insulated-gate TFT which can be fabricated by the same evaporation techniques used for the standard structure of Fig. 1. Although experimental units have been made it is too early to attempt to evaluate their performance. The ability to fabricate the TFT in many different forms should be an advantage in designing TFT's for particular applications and in incorporating them into thin film circuits.

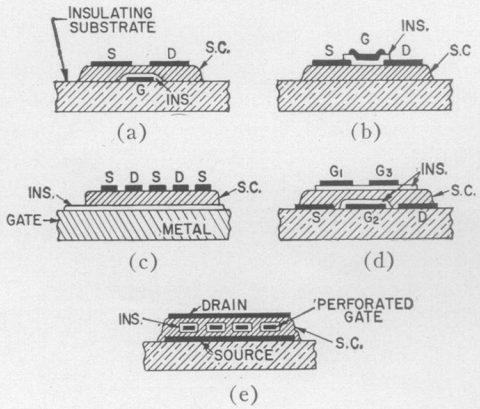

Fig. 11—Structural variations of the insulated-gate TFT.

The structure in Fig. 11(a) differs from the standard structure only in the sequence of evaporating the layers. In Fig. 11(b) all of the electrodes are applied on the same side of the semiconductor. Fig. 11(c) shows an interdigitated source and drain deposited upon an insulated metal gate for higher power output. Fig. 11(d) illustrates a pentode multiple gate structure designed to provide shielding between input and output.

Fig. 11(e) shows a layer-type TFT in which the control gate is a perforated metal film or an array of evaporated strips encased in insulator and embedded in the semiconductor. When biased positively or negatively with respect to the semiconductor the conductivity in the neighborhood of the apertures can be modulated, thus controlling the source-drain current. Although somewhat more lengthy to fabricate than the planar type TFT a possible advantage of the layer-type of unit may arise from a reduced source-drain transit time.

Many additional variations of the TFT will arise as the units are modified to serve particular functions in thin-film circuits. Several illustrations are given in Section VI.

V. Fabrication of the TFT

Although numerous thin-film techniques are available for fabricating the TFT, evaporation of all constit-

uents using movable masks for defining the electrode and semiconductor patterns has proved to be satisfactory for experimental purposes. A precision masking jig of a type originally developed for making a multiple electrode television camera tube target [22] provided a simple method of achieving very fine patterns, without requiring very fine masks. As indicated by (4), close spacing of the source and drain is desirable in the TFT in order to obtain the highest possible g_m and g_m/C ratios for a given semiconductor material. This type of jig is capable of reasonable accuracy with 5 micron spacings, and the technique can be extended to electrode dimensions of less than one micron.

Fig. 12 depicts the masking arrangement employed. A fine wire grill of variable wire spacing is mounted close to the glass substrate blank, whose lateral position relative to the wires can be adjusted from outside the vacuum enclosure. By moving the glass blank between successive evaporations gap spacings considerably smaller than the wire diameter can be deposited. An additional set of movable masks positioned between the wire grill and the evaporation source serves to define the length of the evaporated strips and provides lateral connections for evaporated circuits. This procedure avoids the problems associated with the use of extremely fine wires and greatly extends the versatility of a given set of masks.

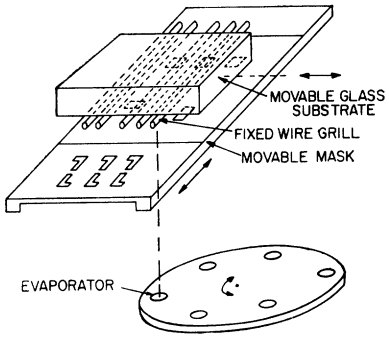

Fig. 12—Evaporation mask arrangement used in fabricating the TFT.

VI. Application of the TFT in Thin Film Circuits

The ability to fabricate circuits and components in the same operation points directly toward the "integrated circuit" concept [23] now being investigated in various forms in several laboratories. Although in an early stage of development, the TFT thin-film circuit is believed to offer some significant advantages when compared with existing techniques for forming transistors and circuits upon a single crystal block of silicon. An insulating substrate of nearly unlimited size permits a large array of circuits to be deposited on a single continuous support. In addition, the electrically inert base offers greater freedom in the design of the active elements and in the geometrical layout of intricate circuit patterns, since active and passive elements can be deposited in layers in any order. Both of these factors should lead not only to greater circuit density in complex devices but also to new applications where the available space for the electronics is at an absolute minimum. A TFT circuit could, in principle, be deposited upon any part of an existing device offering a few square millimeters of free surface. If the surface is a metal, a preliminary coating of insulator would be applied as substrate for the TFT.

The fabrication of thin film circuits incorporating transistors, resistors, capacitors and diodes can be carried out by the same evaporation techniques as described in the preceding section for the TFT. To illustrate the method a three-stage direct-coupled thin-film amplifier was built (see Fig. 13). Since many components are deposited simultaneously the number of operations required for a complete circuit increases very slowly or not at all with increasing complexity of the circuit. Complete circuits containing hundreds or thousands of active elements deposited in one evaporation sequence appear to be entirely feasible.

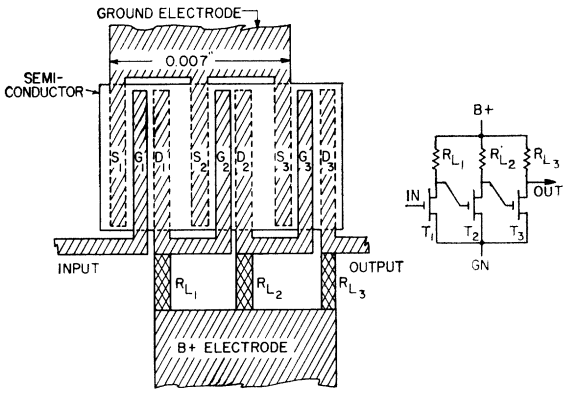

Fig. 13—A 3-stage direct-coupled thin film amplifier. Direct coupling is feasible because the insulated-gate TFT does not draw appreciable gate current.

Some preliminary consideration has been given to the application of the TFT in miniaturized computer circuits. Although the basic elements of a computer could be constructed using TFT triodes in combination with other thin-film components it may be advantageous to evaporate multi-electrode active elements designed particularly for the required function. Fig. 14 shows a direct-coupled flip-flop based upon the TFT. By inverting one of the triodes in the flip-flop the cross connections are simplified. Fig. 15 illustrates AND and NOR gates derived from the TFT. The semiconductor itself is used as the load resistor for the NOR gate.

The thin film circuits of Figs. 13–15 illustrate only crudely the potentialities of the TFT in integrated circuit design. It is apparent, however, that the distinction between components and circuits will become more and more diffuse when devices of extreme complexity can be fabricated in one coherent piece. To adequately design, build and use such integrated devices a new type of engineering skill will have to be developed.

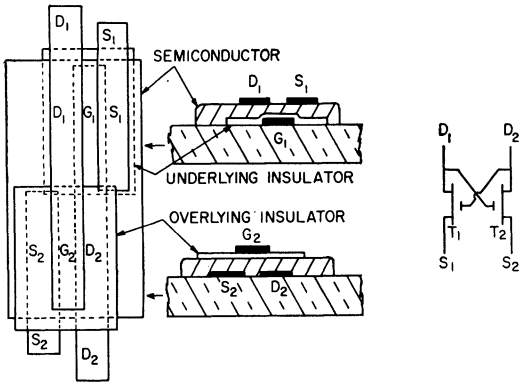

Fig. 14—A thin film flip-flop element equivalent to 2 TFT's with direct-coupled cross connections.

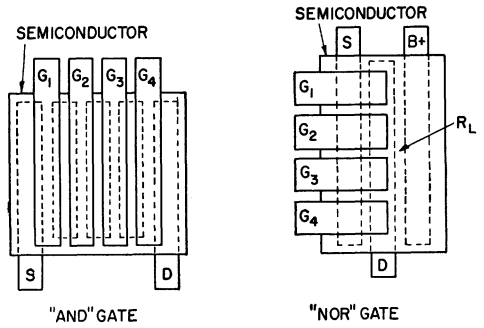

Fig. 15—Thin film AND and NOR gates derived from the TFT.

VII. Discussion and Conclusions

A striking aspect of the TFT development is the demonstration that a high-gain transistor can be built using a semiconductor as imperfect as a polycrystalline evaporated layer. Equally significant is that these transistors operate by the control of injected majority carriers with an insulated-gate structure. While the close spacing of electrodes has contributed to the surprisingly good performance the results are a convincing demonstration of the potentialities of devices utilizing injected majority carriers in wide-band-gap materials. Considering that TFT's have oscillated at frequencies up to 17 Mc using layers of the type yielding Hall mobilities of the order of 5 cm^2/v-sec, the prospect for improving the frequency response by one or two orders of magnitude appears good. This may require materials having higher mobility and structures with closer spacings.

On the basis of the results to date the TFT appears ready for evaluation in thin circuit applications. However, it is clear that much development work remains to be done. Questions such as stability, need for encapsulation, and ability to meet design tolerances, etc., have yet to be answered to fully assess the impact the TFT will have on circuit design. If these results are favorable (as preliminary tests appear to indicate) this impact could be very great indeed.

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References

[1] O. Heil, Brit. Patent No. 439,457; 1935.
[2] W. Shockley, "A unipolar field-effect transistor," Proc. IRE, vol. 40, pp. 1365–1376; November 1952.
[3] G. C. Dacey and I. M. Ross, "The field effect transistor," *Bell. Sys. Tech. J.*, vol. 34, pp. 1149–1189; November, 1955.
[4] S. Teszner, "Le Technetron," in "Solid State Physics in Electronics and Telecommunications," M. Desirant and J. L. Michiels, Eds., Academic Press London Ltd., Eng., pp. 1086–1099; 1960.
[5] R. Bockemuehl, "Cadmium sulfide field-effect phototransistor," Proc. IRE, vol. 48, pp. 875–882; May, 1960.
[6] W. Ruppel and R. W. Smith, "A CdS analog diode and triode," *RCA Rev.*, vol. 20, pp. 702–714; December, 1959.
[7] R. W. Smith and A. Rose, "Space-charge-limited currents in single crystals of cadmium sulfide," *Phys. Rev.*, vol. 97, pp. 1531–1537; March 15, 1955.
[8] P. K. Weimer, S. V. Forgue, and R. R. Goodrich, "The Vidicon —photoconductive camera tube," *RCA Rev.*, vol. 12, pp. 306–313; September, 1951.
[9] A. Rose, "Space-charge-limited currents in solids," *Phys. Rev.*, vol. 97, pp. 1538–1544; March, 1955.
[10] A. Rose and M. Lampert, "Photoconductor performance, space-charge-limited currents and the steady state Fermi level," *Phys. Rev.*, vol. 113, pp. 1227–1235; March 1, 1959.
[11] G. T. Wright, "A proposed space-charge-limited dielectric triode," *J. Brit. IRE*, vol. 20, p. 337; May, 1960.
[12] J. Dresner and F. V. Shallcross, "Rectification and space-charge-limited currents in CdS films," *Solid State Electronics*, to be published.
[13] P. K. Weimer, "An Evaporated Thin Film Triode," presented at IRE-AIEE Device Res. Conf., Stanford University, Calif., June, 1961; "Evaporated Circuits Incorporating Thin Film Transistors," presented at Internatl. Solid-State Circuits Conf., Philadelphia, Pa.; February, 1962.
[14] W. Shockley and G. L. Pearson, "Modulation of conductance of thin films of semiconductors by surface charges," *Phys. Rev.*, vol. 74, pp. 232–233; July 15, 1948.
[15] M. M. Atalla, Solid-State Device Res. Conf. at the Mellon Inst. and Carnegie Inst. of Technology, Pittsburgh, Pa.; June, 1960.
[16] C. T. Sah, "A new semiconductor tetrode—the surface-potential controlled transistor," Proc. IRE, vol. 49, pp. 1623–1634; November, 1961.
[17] J. F. DeWald, "A new type of semiconductor amplifier—the electrolyte field effect," *Bull. Am. Phys. Soc.*, vol. 3, p. 129; March, 1958.
[18] H. N. Yu, "The chargistor, a new class of semiconductor devices," *IBM J.*, vol. 5, pp. 328–330; October, 1961.
[19] W. H. Brattain and C. G. B. Garrett, "Surface states" in "Methods of Experimental Physics—Solid State," K. Lark-Horovitz and V. A. Johnson, Eds., Academic Press, London Ltd., Eng., vol. 6B, ch. 7–8, pp. 136–143; 1959.
[20] G. Heiland, "Feld Effekt und Photoleitung an ZnO-Einkristallen," *J. Phys. Chem. Solids*, vol. 6, pp. 155–168; August, 1958.
[21] R. Bube, "Trap density determination by space-charge-limited currents," *J. Appl. Phys.*, to be published.
[22] P. K. Weimer, S. Gray, C. Beadle, H. Borkan, S. Ochs and H. Thompson, "A developmental tricolor vidicon having a multiple electrode target," IRE Trans. on Electron Devices, vol. ED-7, pp. 147–153; July, 1960.
[23] T. O. Stanley, "Integrated electronics," *Am. Scientist*, vol. 49, pp. 169–181; June, 1961.