SiEPIC – Silicon Photonics – Fabrication via Electron Beam Lithography at UW – Process Design Kit (PDK)

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Introduction

- The fabrication is performed by Richard Bojko at the Washington Nanofabrication Facility at the University of Washington, Seattle.
- The EBeam tool was purchased by a grant applied for by Prof. Michael Hochberg.
- The process development was performed by R. Bojko and M. Hochberg's group.
- Numerous fabrication runs (20+) were performed by L. Chrostowski's group at UBC, Prof. D. Ratner's group, and others, since 2011, to stabilize the fabrication process and develop devices.
- Fabrication coordination and PDK are provided by the SiEPIC program – www.siepic.ubc.ca. The fabrication flow has been used by many research groups, some examples which are provided in this document below, and online at the UW web page.
- Details on the Ebeam and UW – https://ebeam.mff.uw.edu/ebeamweb
- Typical cost for a single chip is $1,000-4,000.

Fabrication

- Soitec UNIBOND. 6". Prime grade. 220 nm silicon with a 6 sigma of 22.3 nm. Buried Oxide thickness of 3.017 µm with a 6 sigma of 6 nm.
- Negative resist, HSQ – https://ebeam.mff.uw.edu/ebeamweb/process/processmain.html
- Pattered using a JEOL JBX-6300FS e-beam, with mask data prep performed by software "Beamer". Using the 4th Lens Mode and Normal writing.
- Single full-etch using ICP
- 82º sidewall angle
- Minimum isolated feature size of 60 nm.
- Shot Pitch – Default is 6 nm. This is a "snapping" of all layout features to a 6 nm grid. Periodic structures, e.g., Bragg gratings, should use integer multiples of the Shot Pitch to

avoid quantization errors. Smaller shot pitches (more expensive) and Shot pitch fracturing are available.
- Write conditions – 4th Lens, 2-pass field shift writing, with default 6 nm shot pitch, 8 nA beam current.
- Oxide cladding deposition, 2-3 µm, PECVD.

GDS Layers

GDS #	Name	Description
1	Si	Silicon 220 nm remaining. Where drawn is 220 nm; elsewhere is 0 nm. Shot pitch = 6 nm. Recommended for most silicon devices.
~~**2**~~	~~SiEtch1~~	~~Partial etch of 70 nm. Where 1 & 2 are drawn, you will get ~150 nm silicon~~
10	Text	Text labels for automated measurements.
~~**11**~~	~~M1~~	~~Metal heater layer. Where drawn there will be metal. Molybdenum ~250 nm thick. ~21 ohm/sq. Min feature 0.5 µm, min spacing 2 µm. M1 is aligned to "Si" to within 0.25 µm.~~
~~**12**~~	~~M2~~	~~Metal contact layer. Where drawn there will be metal. Ti 10-20nm / Au 250 nm. Min feature 5 µm, min spacing 5 µm. M2 is aligned to M1 to within 3 µm.~~
26	SEM_ROI	SEM imaging requests; see below.
31	Si_p6nm	Fabricated at the same time as Layer "Si", except with Shot Pitch Fracturing of 1 nm. Cost is similar to Layer "Si". See description below. Recommended for Bragg gratings. Layer is perfectly aligned to Layer "Si".
33	Si_p2nm	Fabricated at the same time as Layer "Si", **but not aligned** to Layer "Si". Shot Pitch = 2 nm. Cost is 8X higher than Layer "Si".
99	Floorplan	Indicate the assigned area for your layout with a rectangle.

Layout Tools

There are numerous tools that can produce the GDS files required for fabrication. The following is a description of several tools used by SiEPIC researchers:

KLayout

- Free software.
- Tutorial for EBeam https://ebeam.mff.uw.edu/ebeamweb/training/cad_tut_main/cad_tutorial_main.html
- Download from http://www.klayout.de/
- Offers scripting capabilities, including PCells http://www.klayout.de/doc/about/about_pcells.html
- Provided file "Example/PCells.gds" includes a ring resonator and a path that is converted to a smooth waveguide with 90º bends.
- Design Rule Checking file provided "KLayout_EBeam_DRC.rtf". Load the DRC file http://www.klayout.de/doc/manual/drc_basic.html#h2-172

Mentor Graphics

- Commercial EDA (Electronic Design Automation) tools.
- Mentor Graphics Pyxis – for mask layout
- Mentor Graphics Calibre – for verification
- PDKs available for EBeam, IME and imec fabrication.

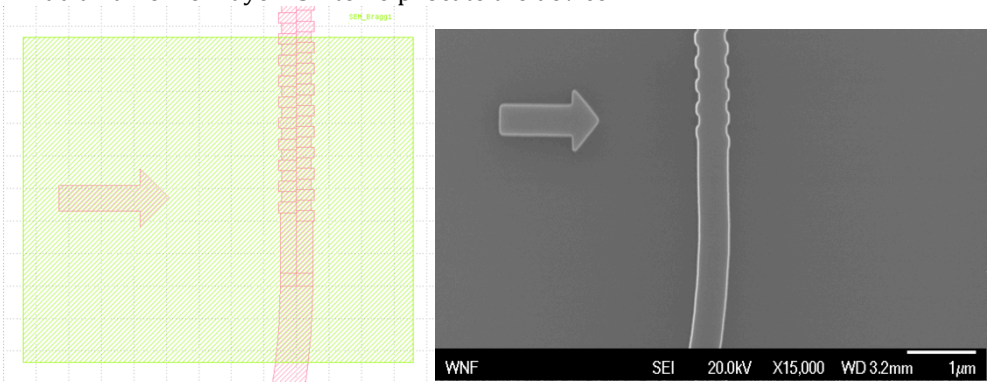
MatlabGDSPhotonicsToolbox

- Free toolbox using commercial Matlab software

- http://www.mathworks.in/matlabcentral/fileexchange/46827-nicolasayotte-matlabgdsphotonicstoolbox
- Specifically designed for silicon photonics. Includes automated waveguide routing. Scripted components. PDKs for various processes including EBeam.

SEM images

- SEM images available upon request, at an additional cost (typically $25 incremental cost per image + setup time)
- Instrument: SEM JEOL JSM-7400; cold-field emission; operated at conditions near where the current of electrons emitted from the chip is not too different from the incident beam current which is typically 20-22 kV for the low beam currents used;
- SEM image requests are done by:
    1. https://ebeam.mff.uw.edu/ebeamweb/remote/remote/sem_inspection_sites.html
    2. Drawing a rectangle around the area of interest, on layer "SEM_ROI". Choose the size based on available ones.
    3. Add a text label with a name, on layer "SEM_ROI"
    4. Add an arrow on layer "Si" to help locate the device.



- See example file "SEM/SEM.GDS"

Automated Measurements

- To take advantage of the automated testing, please make sure your grating couplers are facing right (waveguide on the right side), and on a 127 μm pitch vertically. Counting from top down, the 1st, 3rd and 4th fibre in the array will be used for the outputs, and the 2nd fibre will be input. Please label the 2nd fibre (input) as:
    - opt_in_<polarization={TE, TM}>_<wvl>_device_<deviceID>_<comment>
- example:
    - opt_in_TE_1550_device_McGillRing10_r5um
- The label format is case sensitive, and cannot have extra "_" characters. The labels MUST BE UNIQUE.
- Examples layouts that conform to these test rules are provided in folder "Examples".

Example devices and circuits

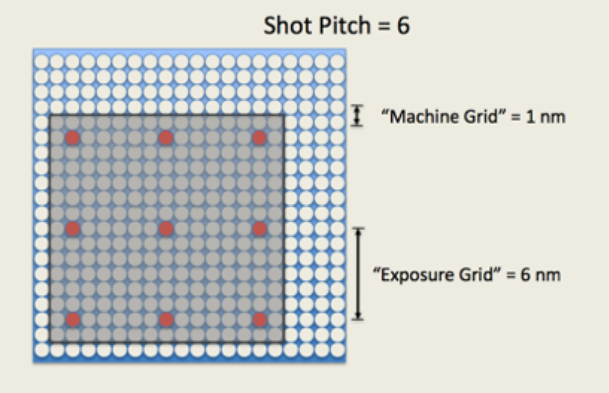
A list of publications via the University of Washington EBeam lithography is available at the following link: https://ebeam.mff.uw.edu/ebeamweb/news/news/pubs.html
The mask layout (GDS) is available for several examples provided in the file "**SiEPIC_EBeam_UW_Examples**". This includes grating couplers, a YBranch, ring resonator, Bragg grating, etc.

Advanced Topics

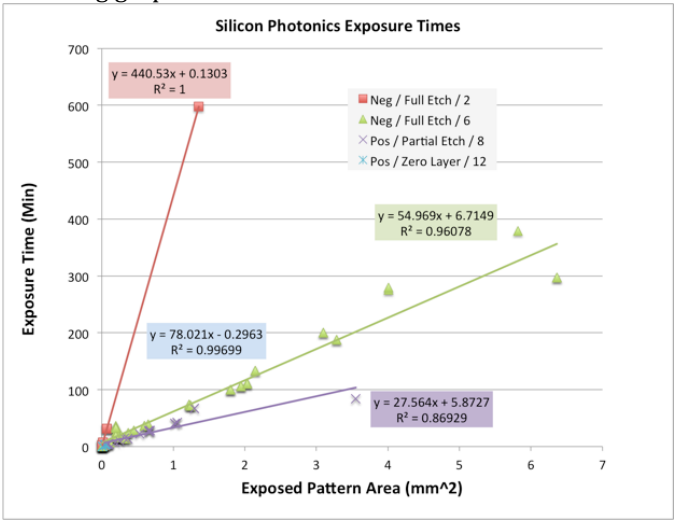
Shot Pitch

Shot pitch in EBeam lithography describes the grid on which the beam can be positioned. These are analogous to pixels in displays. Smaller pixels give you higher resolution capabilities.

- Feature size accuracy and size increment can directly influence device performance. For example, a waveguide bend (or ring resonator) will have a lower loss when written with a finer pitch since there will be less waveguide roughness. The same is true even for straight waveguides.
- Smaller fracturing/writing grid is desirable, but results in longer write times, since we have to use a lower beam current for smaller writing grid size. This is a familiar trade-off to everyone using direct-write EBL
- Example of Shot Pitch = 6 nm:



The write time for different shot pitches, based on previous fabrication runs, is provided in the following graph.

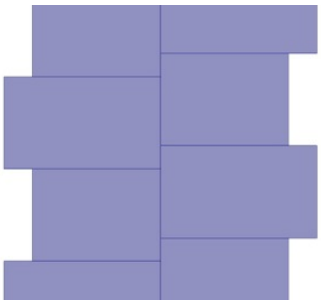


- Alternative: Coarse/Fine Split – One option is to split the exposure into two parts, written with two beam currents
    - Requires change of beam current, lens stabilization wait, and recalibration at second beam current for each chip

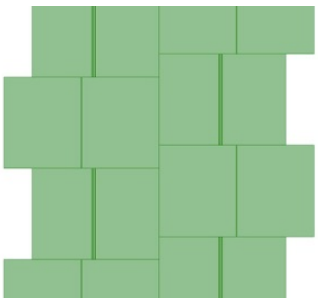
- Possibility of placement mismatch from system or environmental drift (careful design to include intentional overlaps may compensate)

Shot Pitch Fracturing

- Alternative: Shot Pitch Fracturing – Beamer option of Beam Step Size Fracturing gives you a clever method to still get the edge placement of fine-grid shape fracturing while writing with larger beam currents



Original layout

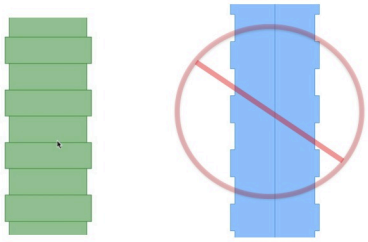


After "Shot Pitch Fracturing"

- Sub-fractures designs with overlapping regions buried in the middle
- The size of each shape is still a multiple of the Beam Step Size, in this case 6 nm
- The outer edges are now placed to the 1 nm machine grid
- Small overlapping shapes buried in the middle of the shape
- What was 2 shapes in conventional fracturing is now 5 shapes

SPF Usage:

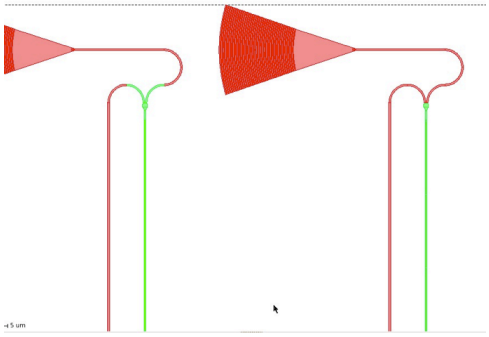
- Design structures as follows:



Design as separate rectangles

Do not design as a polygon

- Hybrid approach – Grating couplers and routing waveguides done on regular layer (Si), and critical features on Shot Pitch Fracturing layer (Si_p6nm):



- More details provided in Richard Bojko, Xu Wang, Yun Wang, Jonas Flueckiger, Nicolas Jaeger, Lukas Chrostowski, "Beam Step Size Fracturing for Bragg Grating Waveguides", GenISys BEAMeeting at EIPBN 2014, 27th May 2014,
File: ShotPitch/Bojko_BeamStepFracturing_BeamMeeting_EIPBN2014.pdf,
and Bragg_Shot_Pitch_Fracturing.gds