

# Introduction to Analog Layout Design

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# Analog VLSI Design

- Implementation of analog circuits and systems using integrated circuit technology.
- Unique Features of Analog IC Design
  - Customized design
  - Designed at the circuit level.
  - Geometry is an important part of the design.
  - Usually implemented as a mixed analog- digital circuit
    - Typically Analog is 20% and digital 80% of the chip area.
  - Analog requires 80% of the design time
    - Requires more iterations
      - Passes for success: 2-3 for analog, 1 for digital.
- In general, analog circuits are more complex than digital.
  - Need to have good knowledge of both circuit analysis, modeling and technology

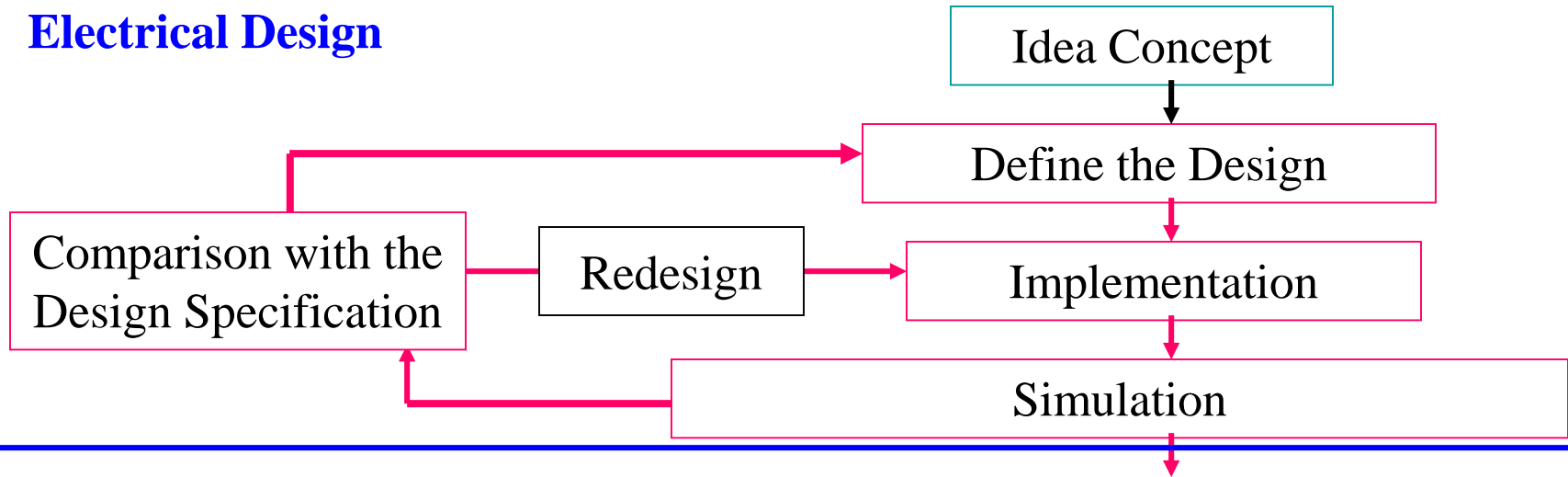
# Analog Design Flow

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- Electrical Design
- Physical Design
- Fabrication and Testing
- Final Product

# Analog Design Flow

## Electrical Design



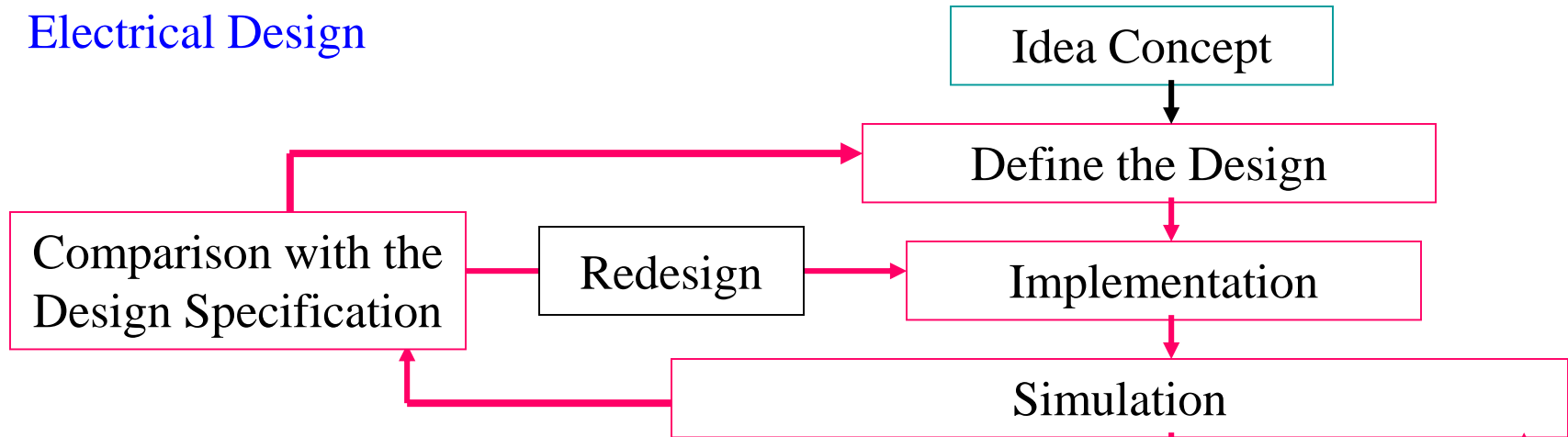
## Physical Design

## Fabrication

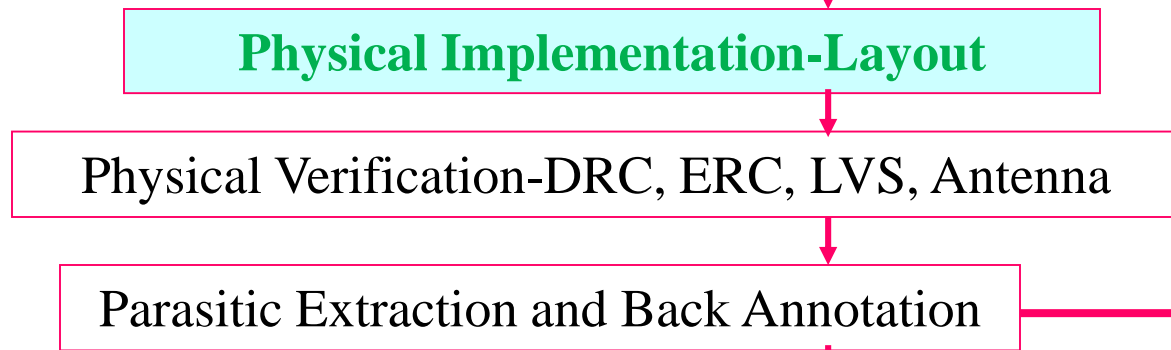
## Testing and Product Development

# Analog Design Flow

## Electrical Design



## Physical Design

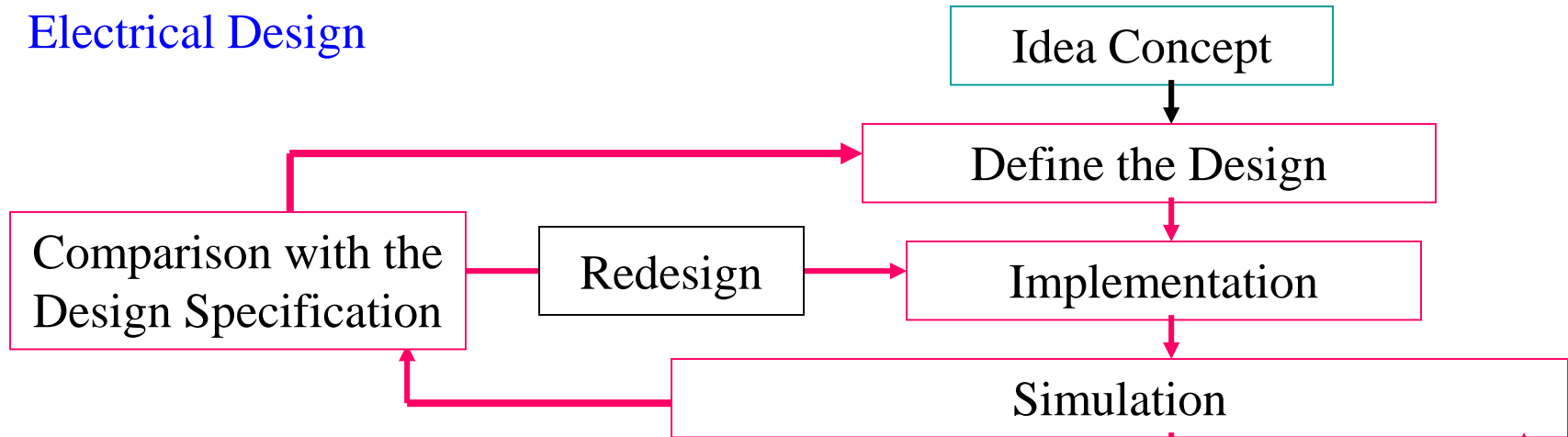


## Fabrication

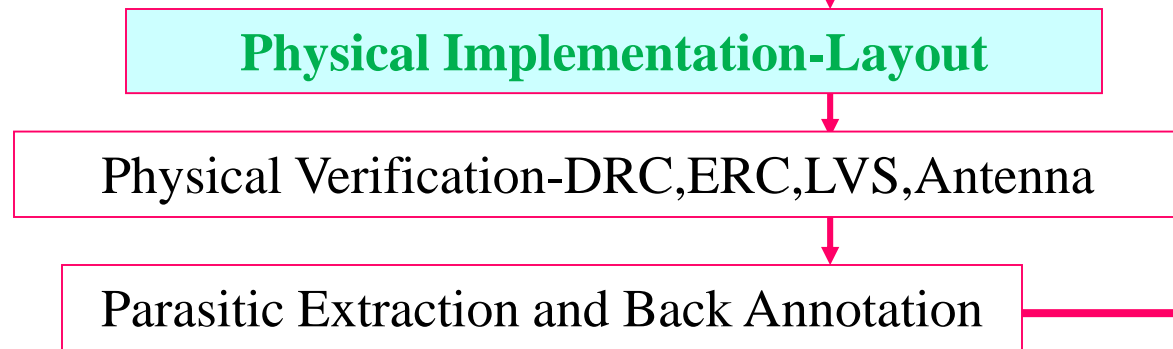
## Testing and Product Development

# Analog Design Flow

## Electrical Design



## Physical Design

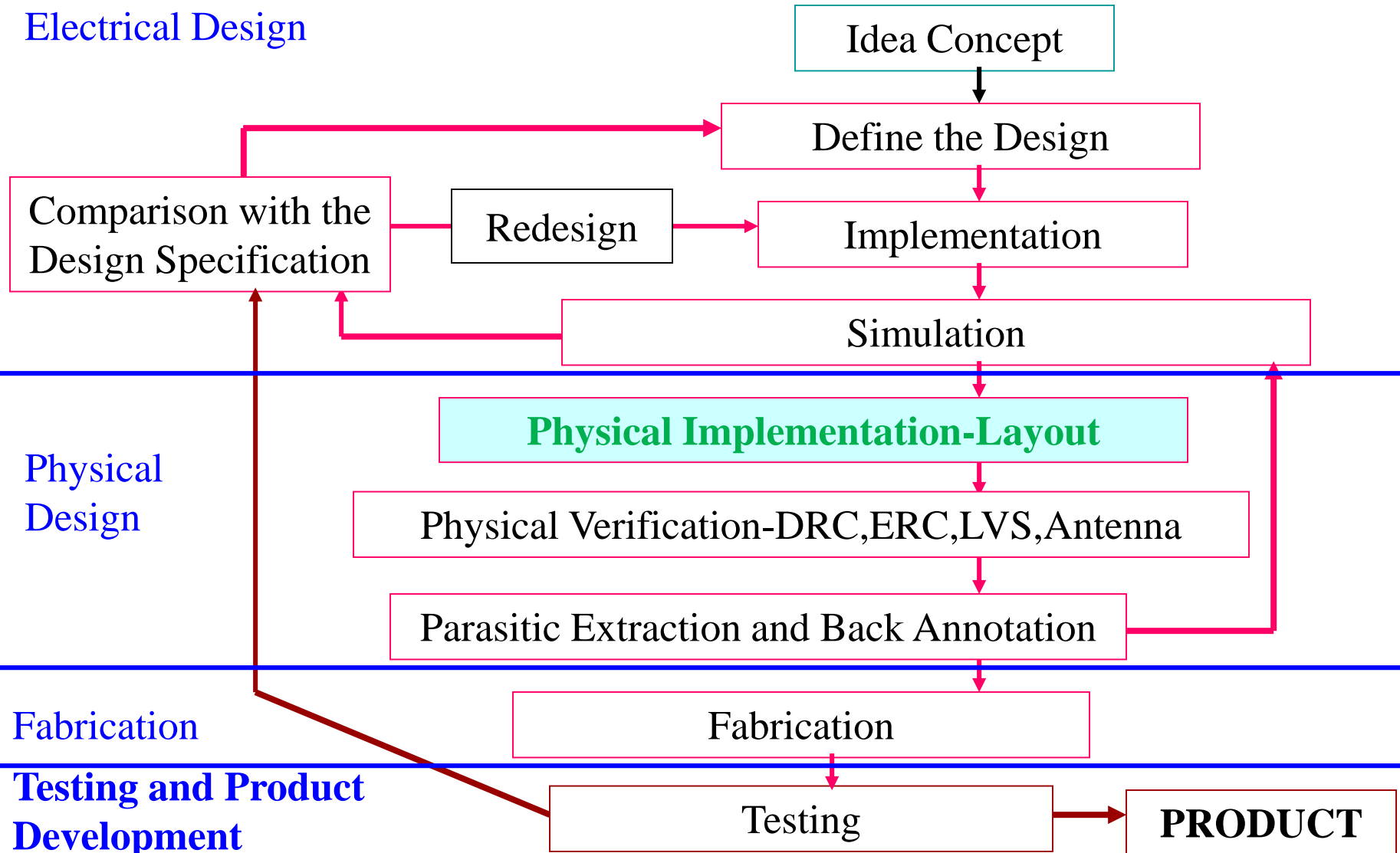


## Fabrication



## Testing and Product Development

# Analog Design Flow



# The Layers

- Layers in a Typical process

		Align to	Purpose	Mask CIF	
1	Active	notch	Defines Active area	CAA	43
2	Pwell	1	Pwell and also sidewall implants(STI)	CWP	41
3	Nwell	1	Nwell and also sidewall implants	CWN	42
4	Poly	1	Poly gate	CPG	46
5	N Select	1	Source drain implants / nLDD implants	CSN	45
6	P Select	1	Source drain implants/ pLDD implants	CSP	44
7	Contact	4	Defines contacts to poly and active	CCP or CCA	47,48
8	Metal 1	7	First level metal interconnect	CMF	49
9	Via1	8	Via between m1 and m2	CVA	50
10	Metal 2	9	Defines second level metal interconnect	CMS	51
11	Pad OVGL	10	Defines bond pad openings	COG	52



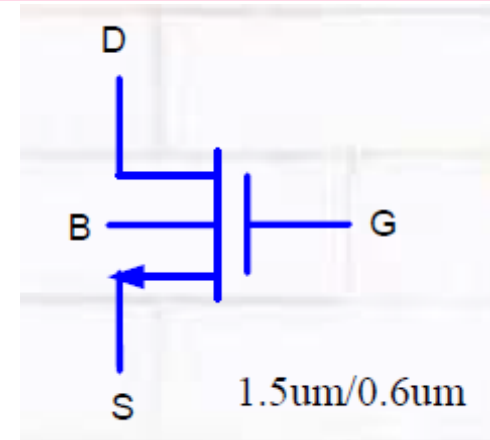
# Analog Design components

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- Active devices
  - Transistors
    - N-mos and P-mos
- Passives
  - Resistors
  - Capacitors
  - Inductors
    - Implemented using existing layers and masks
      - Possibly adding a few extra layers

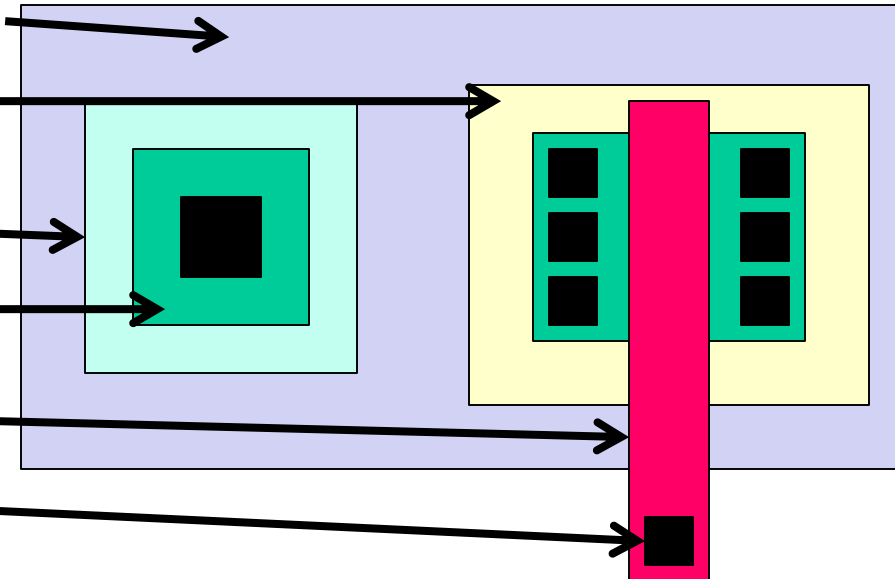
# The transistor-NMOS

- Four terminal Device
  - NMOS Bulk terminal is tied to p substrate which is tied to  $V_{ss}$ : Ground terminal



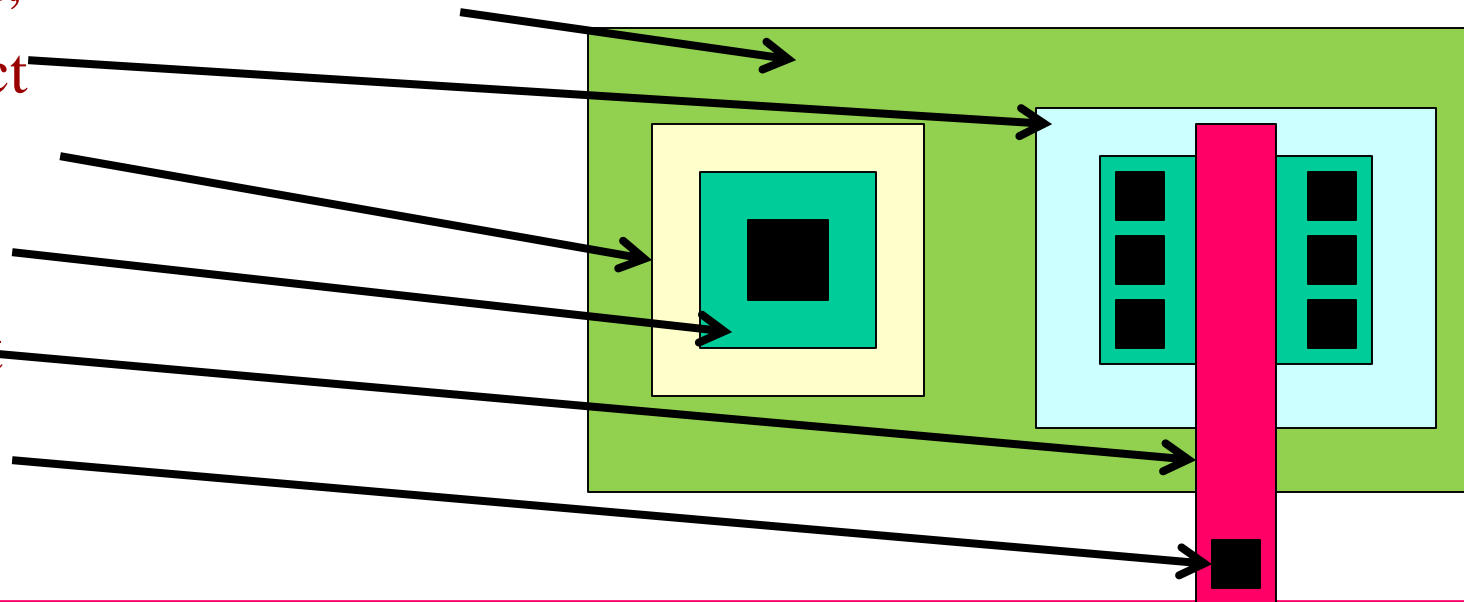
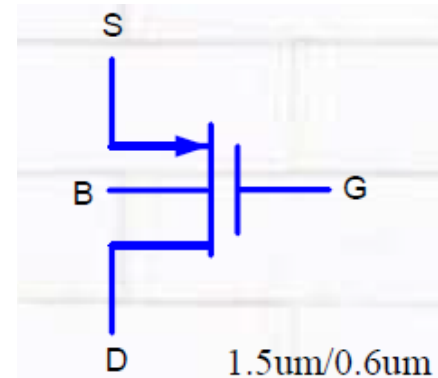
- Layers required :

- P-Well (in twin well process)
- N-select
- P-Select
- Active
- Poly
- Contact



# The transistor-PMOS

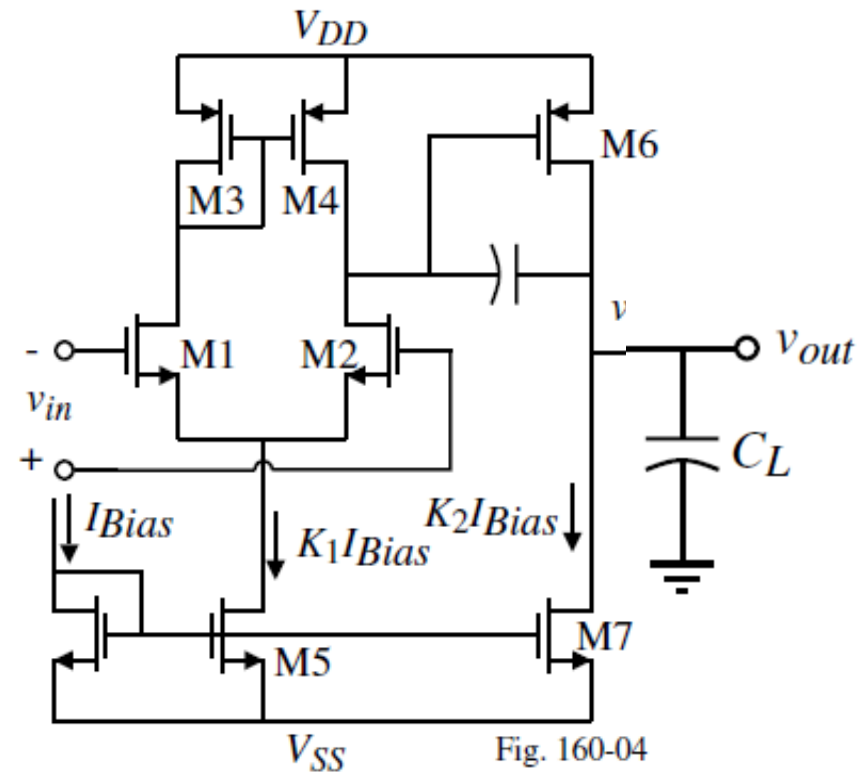
- PMOS
  - Bulk terminal is tied to N-Well which is tied to Vdd:
- Layers required :
  - N-Well (in twin well process)
  - P-select,
  - N-Select
  - Active
  - Poly
  - Contact



# Design of an OpAMP

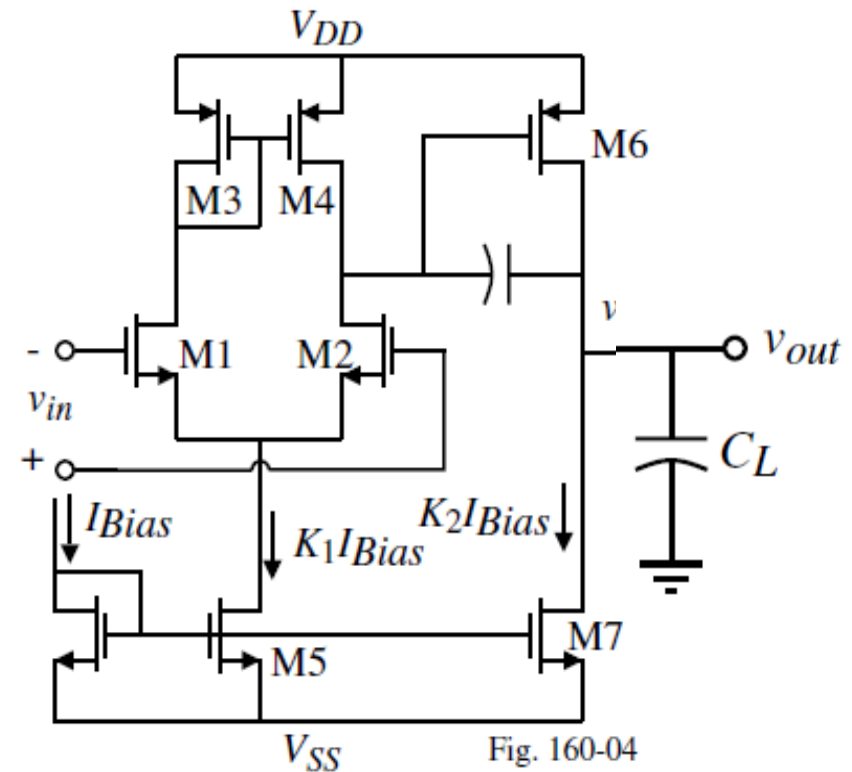
- Specification

- $V_{DD} = 1.8 \text{ V}$
- $V_{SS} = 0 \text{ V}$
- Power Dissipation  $< 0.3 \text{ mW}$
- Load =  $2 \text{ pF}$
- Slew rate =  $20 \text{ V}/\mu\text{sec}$
- $\text{ICMR}_+ = 1.6 \text{ V}$
- $\text{ICMR}_- = 0.8 \text{ V}$
- DC gain =  $60 \text{ dB} = 1000$
- Phase Margin =  $60^\circ$
- Unity Gain BW =  $30 \text{ MHz}$



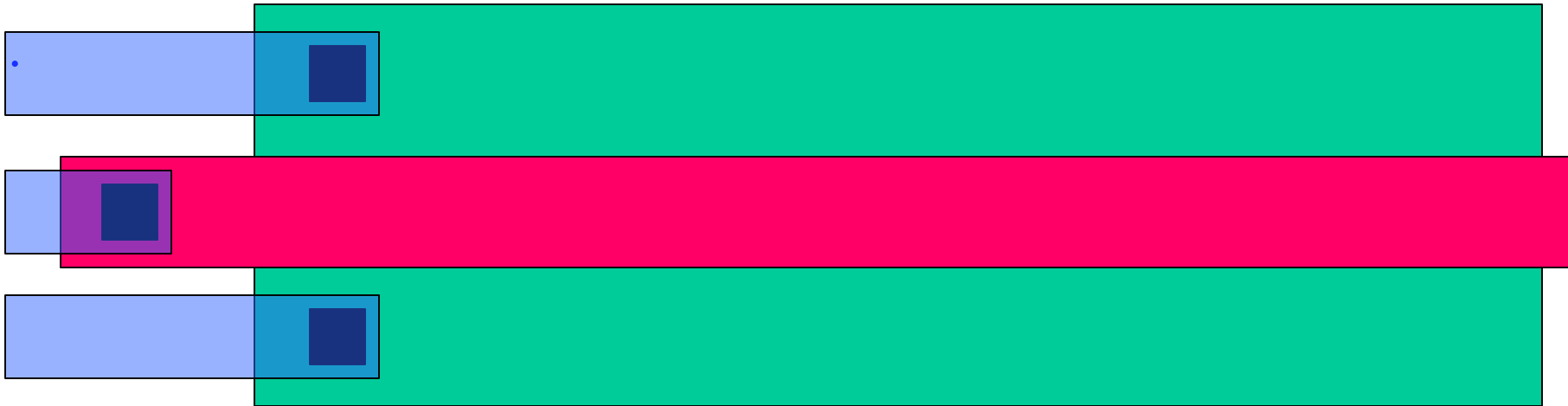
# Design

Using Slew rate and load estimate current	20 $\mu\text{A}$
Using Phase margin and load determine miller capacitance $C_c$	800 fF
Using GBW estimate (W/L) of M1 and M2	6
Using ICMR+ estimate size (W/L) of M3 and M4	14
Using ICMR- estimate size (W/L) of M5	12
Using Phase Margin size M6;	174
Using Current requirement size M7( $I_7 = 125 \mu\text{A}$ )	75
Using Current requirement size M8( $I_7 = 20 \mu\text{A}$ )	12



# Drawing Wide Transistor

- M6  $W/L = 174$

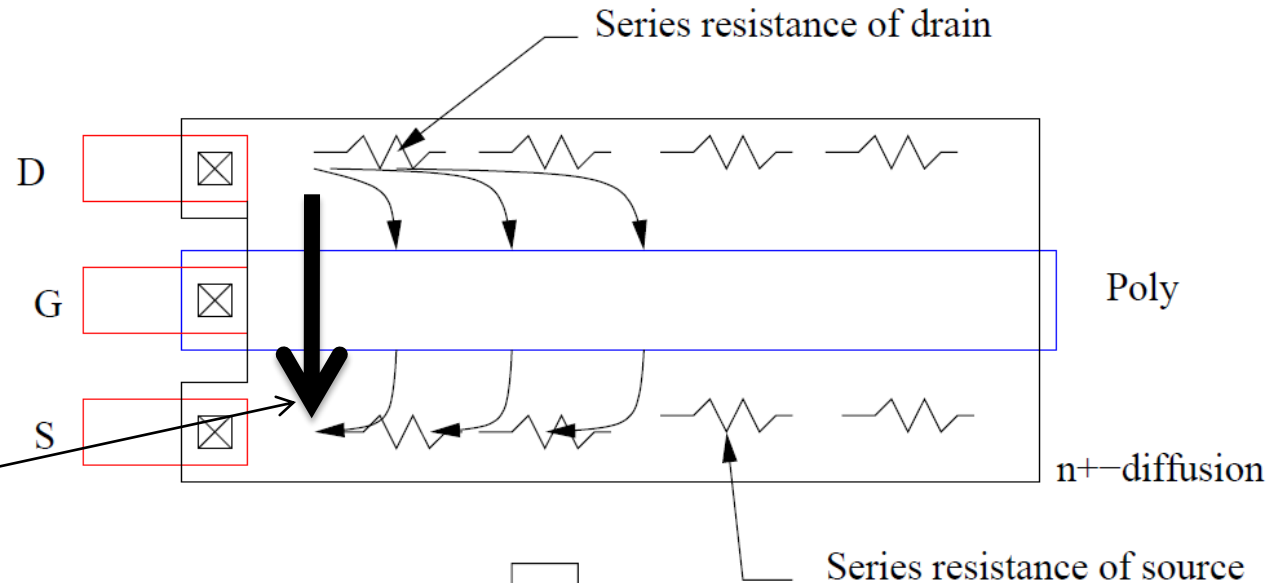


Active, Poly, Contact and M1

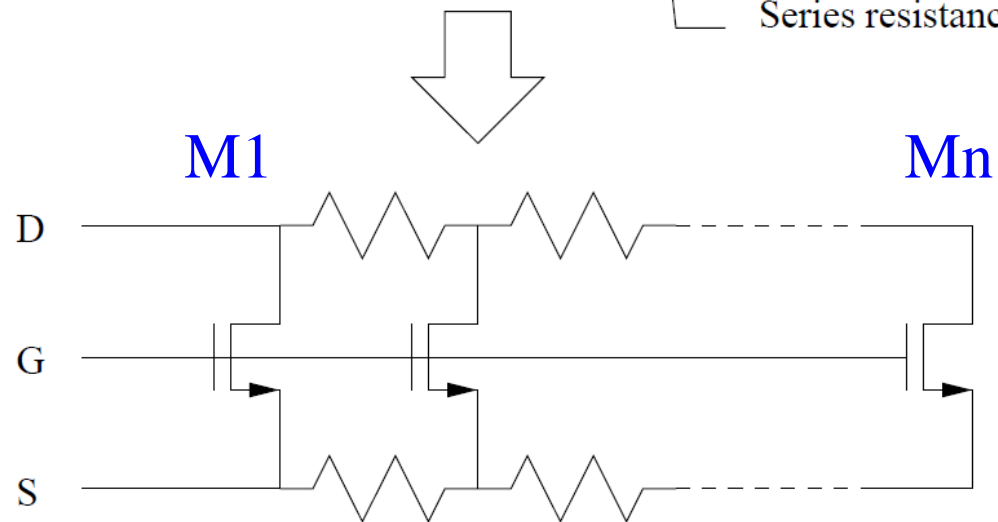
# MOS transistor Layout

- Non-uniform current flow

**Most of the current  
will be shrunk to  
this side**

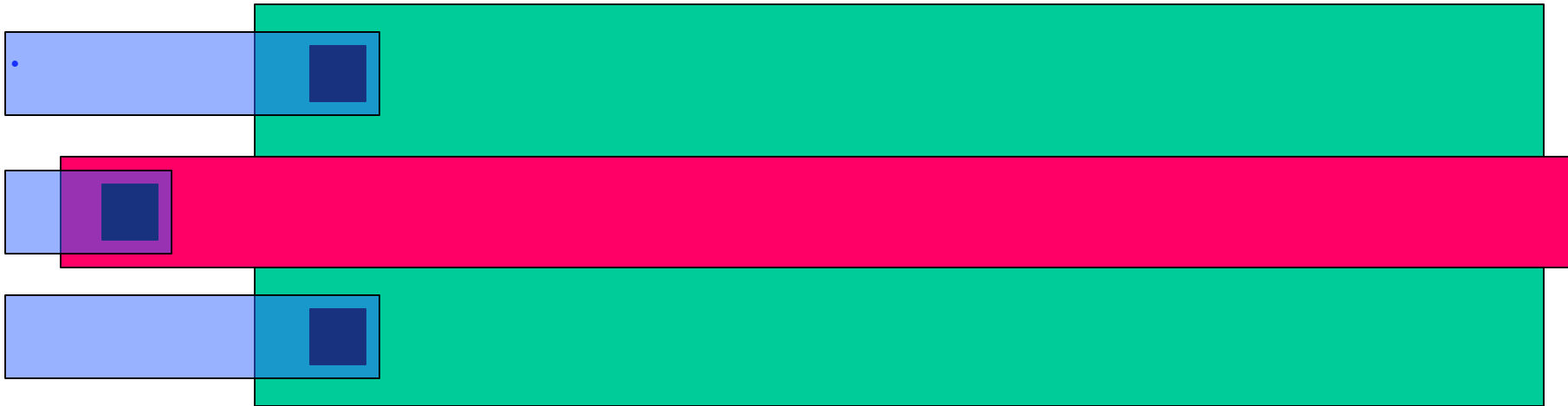


M1 carries the most current and Mn carries the least current).



# Drawing Wide Transistor

- M6  $W/L = 174$



for typical 0.18 $\mu$  CMOS processes

Large gate series resistance:	7.8 $\pm$ 2.5 Ohm/sq
Large distributed resistance of source/drain:	6.8 $\pm$ 2.5Ohm/sq for n+ and 7.2 $\pm$ 2.5Ohm/sq for p+.
Large source/substrate and drain/substrate parasitic capacitances	N-900 fF/um2, 100fF/um P-800 fF/um2, 100fF/um



# MOS transistor Layout

- Parasitic resistance at source and drain must be kept as low as possible
- Gate series resistance must be minimized
  - Series resistance slows down switching speed
  - Also introduces unwanted noise.
- Parasitic source/substrate & drain/substrate capacitances must be minimized
  - Parasitic capacitance slows down switching speed
  - Increases power dissipation(Capacitance switching)
  - Additional load capacitance
    - Need to increase bias current to maintain bandwidth and/or slew rate.
    - Can lead to instability in high gain feedback systems.

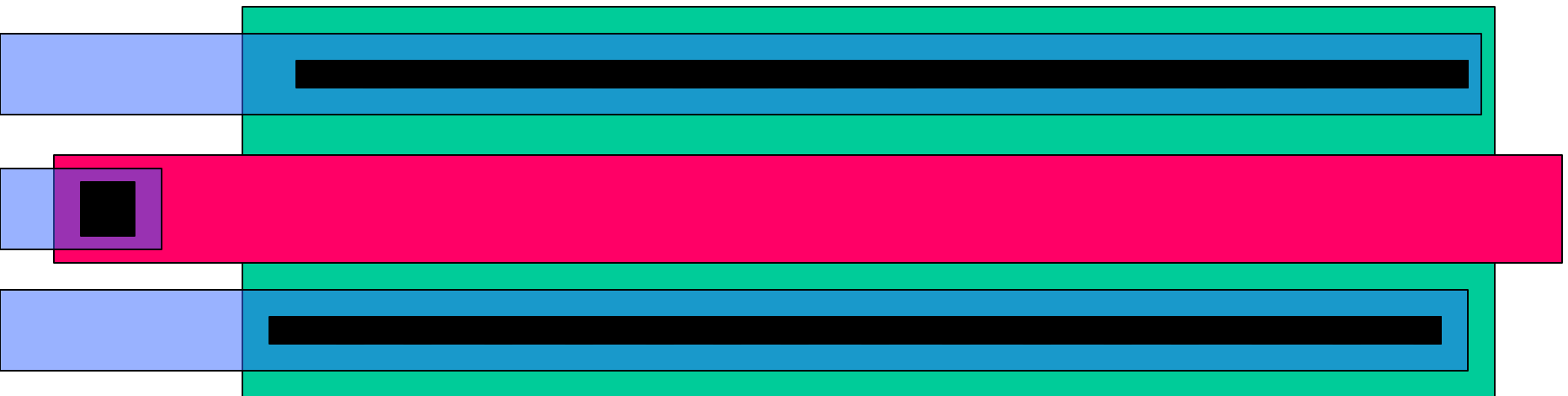
# Layout of MOS Transistors

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- Criteria for MOS Transistor Layout
  - Minimize source/drain resistances.
  - Minimize source/substrate & drain/substrate parasitic capacitances.
  - Minimize gate series resistance.
- Parasitic aware layout

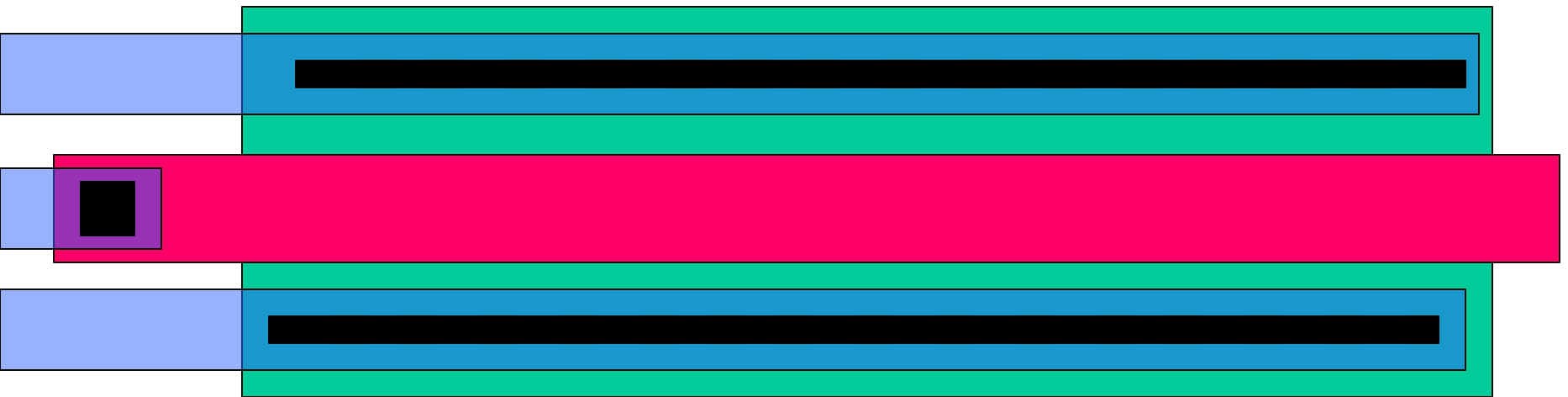
# Layout of MOS Transistors

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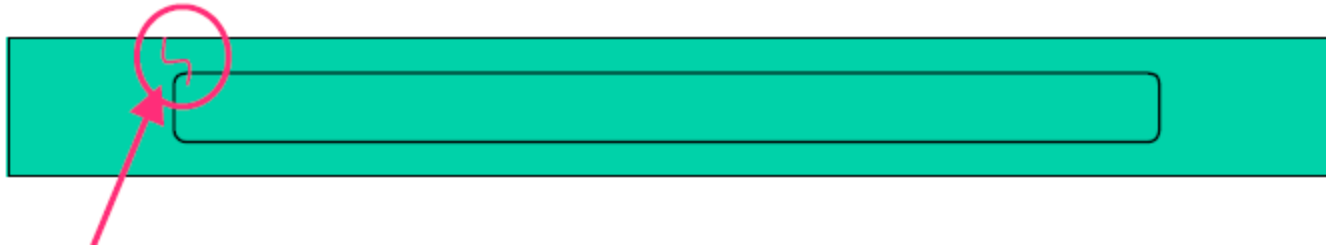
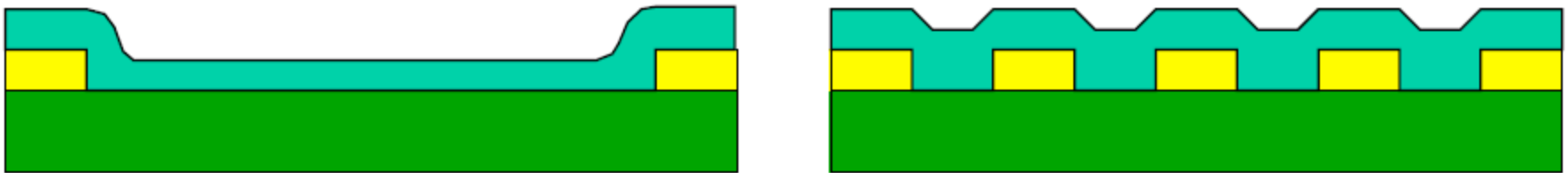
# Parasitic aware layout

- Multiple Contacts or one big contact



# MOS transistor Layout

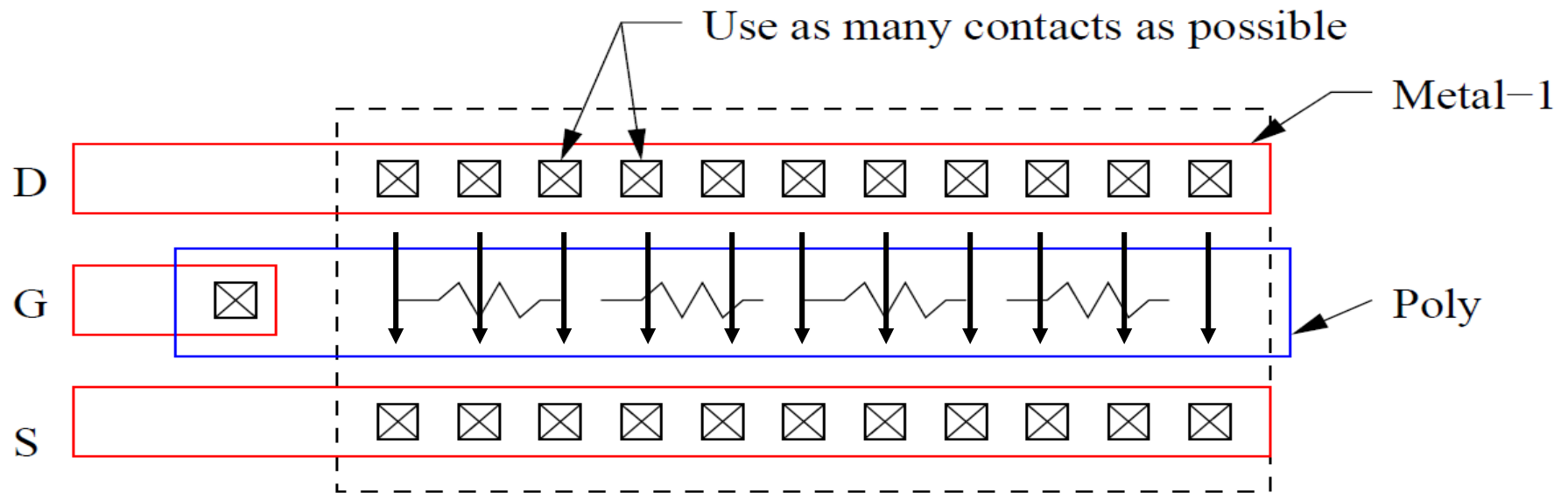
- Reliability issues : Curvature in metal Layer- Can lead to microfracture



Can lead to Electromigration

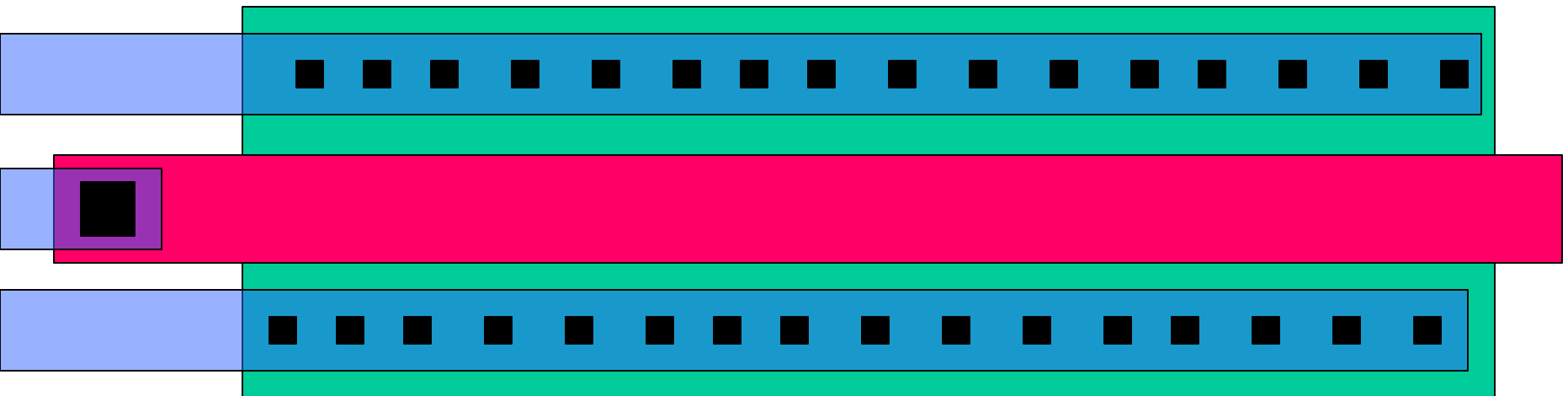
# Layout of MOS Transistors

- Multiple contacts at source/drain
  - **Current is spread**
  - **Smaller source/drain resistances**



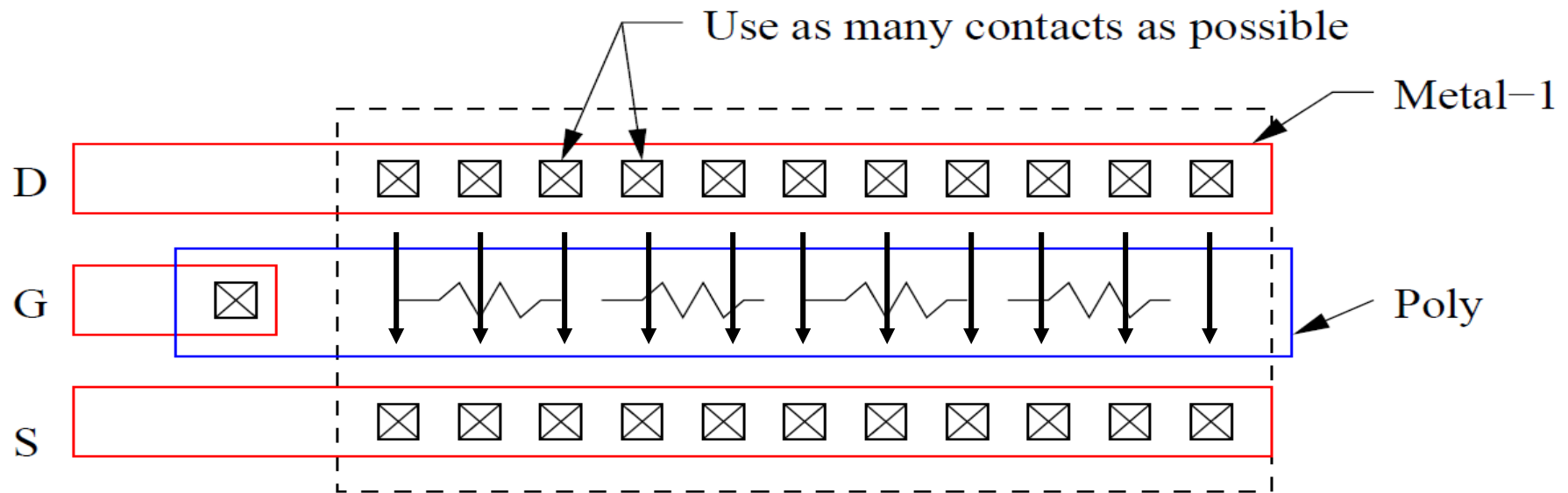
# Parasitic aware layout

- Multiple Contacts or one big contact
- Multiple contacts at source/drain
  - High reliability
    - Better contact at source/drain
      - Smaller contact resistance
        - »  $R = R_c/N$ , where  $N$ =number of contacts



# Layout of MOS Transistors

- Multiple contacts at source/drain
  - **Current is spread**
  - **Smaller source/drain resistances**
    - Series resistance is negligible but lateral resistance still exists.
    - Large source/substrate and drain/substrate parasitic capacitances.

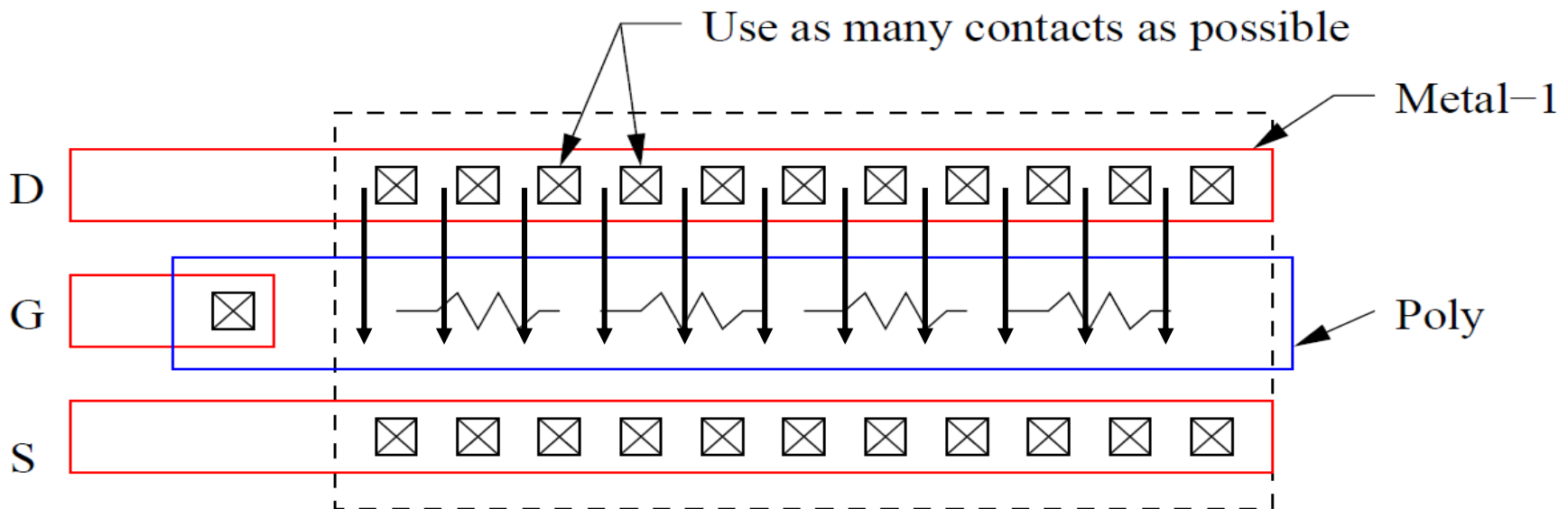




# Layout of MOS Transistors

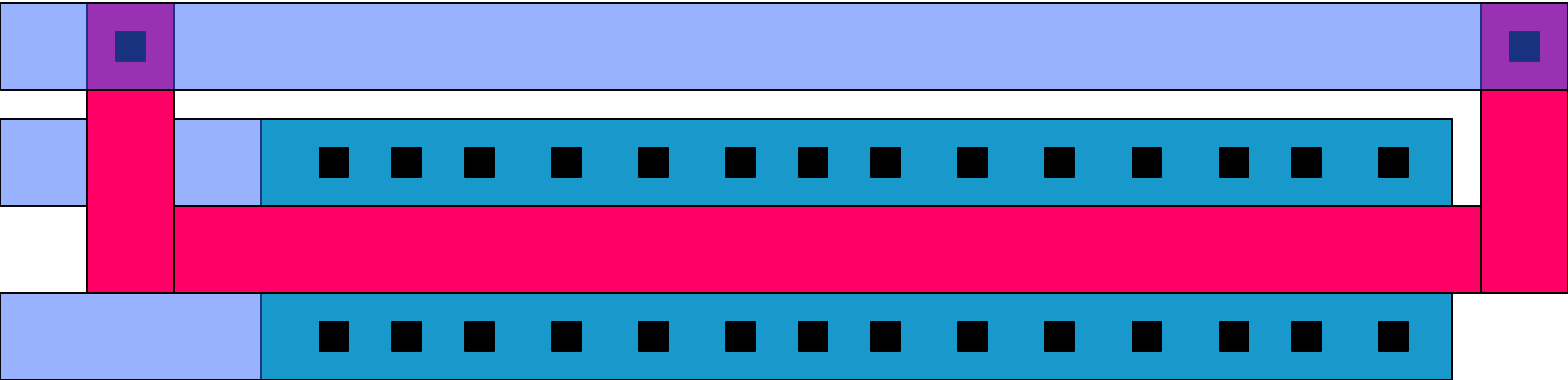
- **Parasitics in transistor**

- Large gate series resistance- Gate is too long.
- **Contacts are not allowed on the gate above the channel**
  - high temperature required to form contacts may destroy the thin gate oxide.



# Layout of MOS Transistors

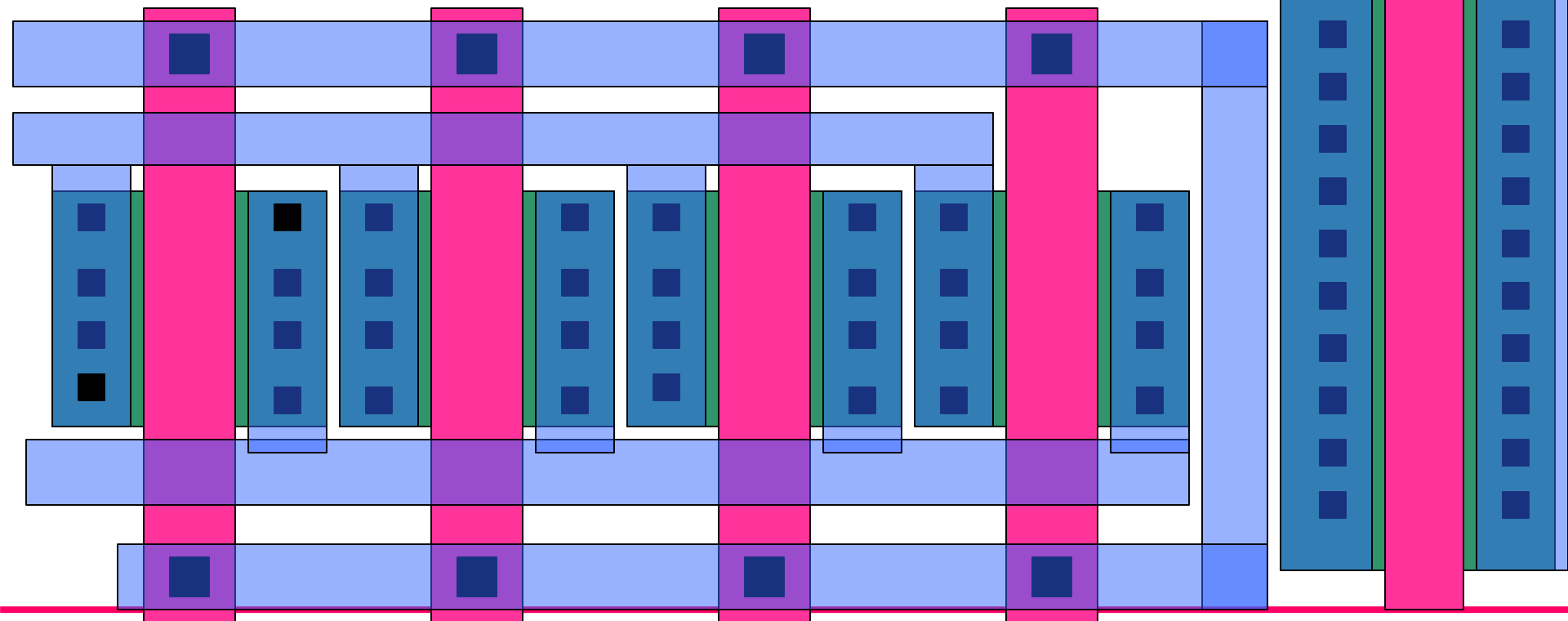
- Poly contact at both ends



## Wide transistors need to be split

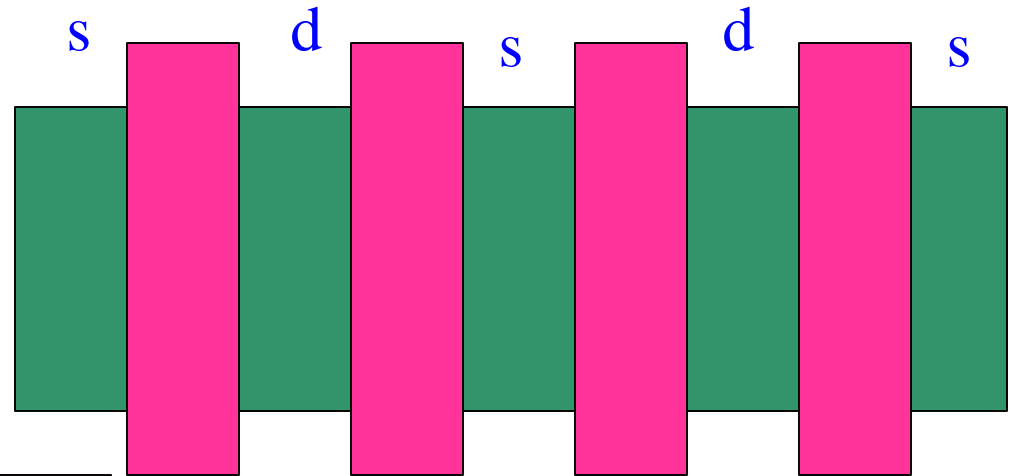
# MULTI-GATE FINGER LAYOUT

- Parallel connection of  $n$  elements ( $n = 4$  for this example)
  - Reduces the gate resistance of the poly-silicon
  - Capacitance unchanged, Large area



# Multifinger Layout-Shared sources/drains

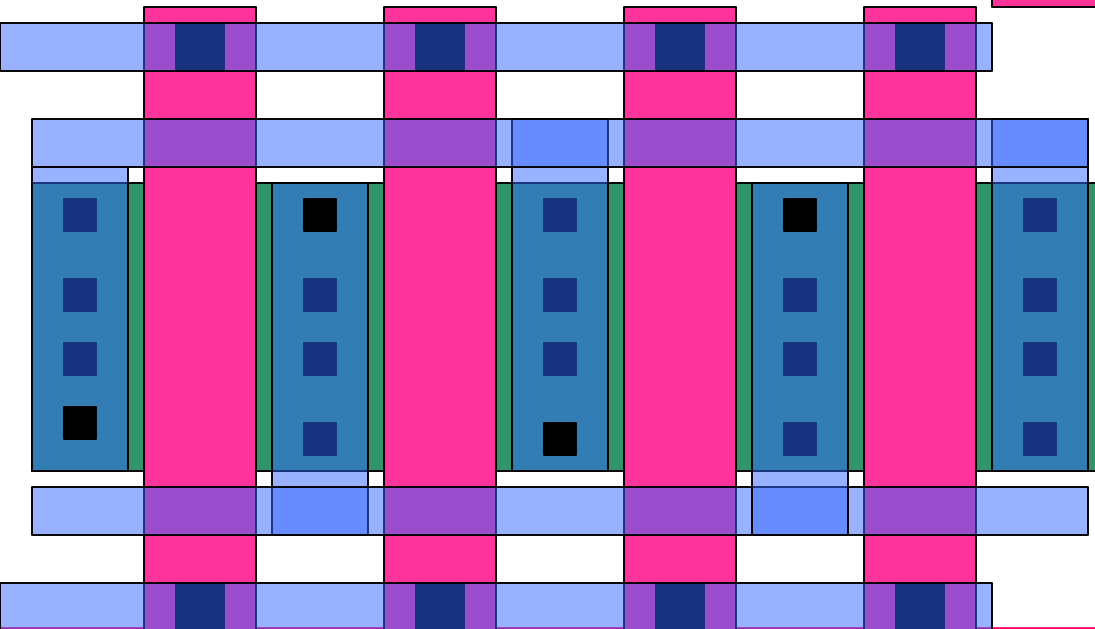
- Contact space is shared among transistors
- Reduced silicon area.
  - Minimizes source/substrate & drain/substrate parasitic capacitances.
- important for high speed



$$C_s = \frac{3}{4} C_s'$$

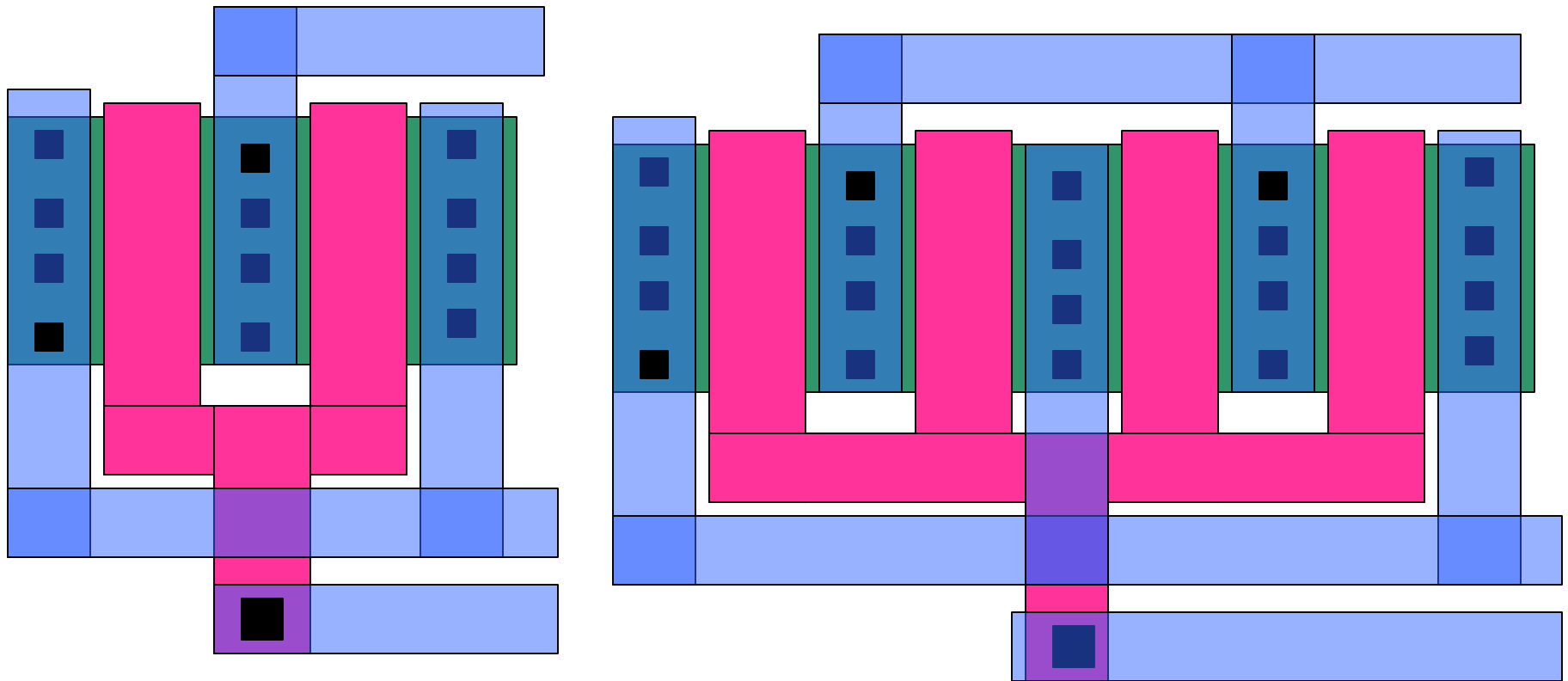
$$C_d = \frac{1}{2} C_d'$$

**Note that parasitic capacitors are lesser at the drain**



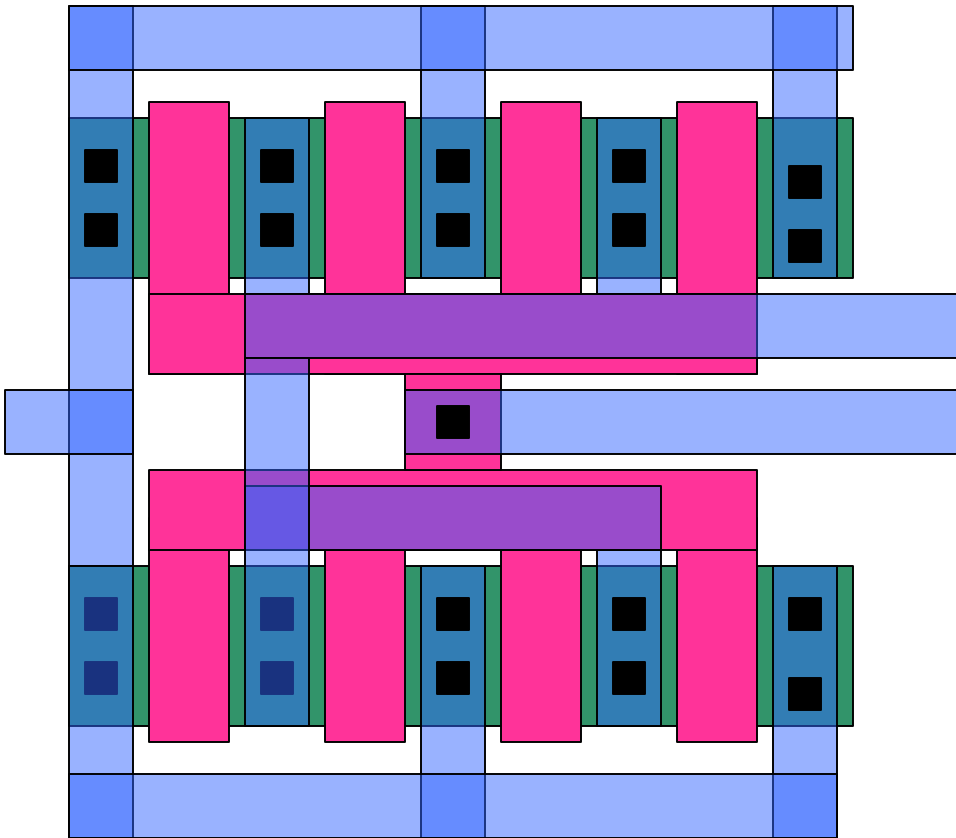
# Folding

- Folding reduces gate resistance
- Shared source/drain , Reduced silicon area.



# Layout of MOS Transistors

- Minimize Source/Substrate and Drain/Substrate Parasitic Capacitances
  - Shared sources/drains.



Another layout

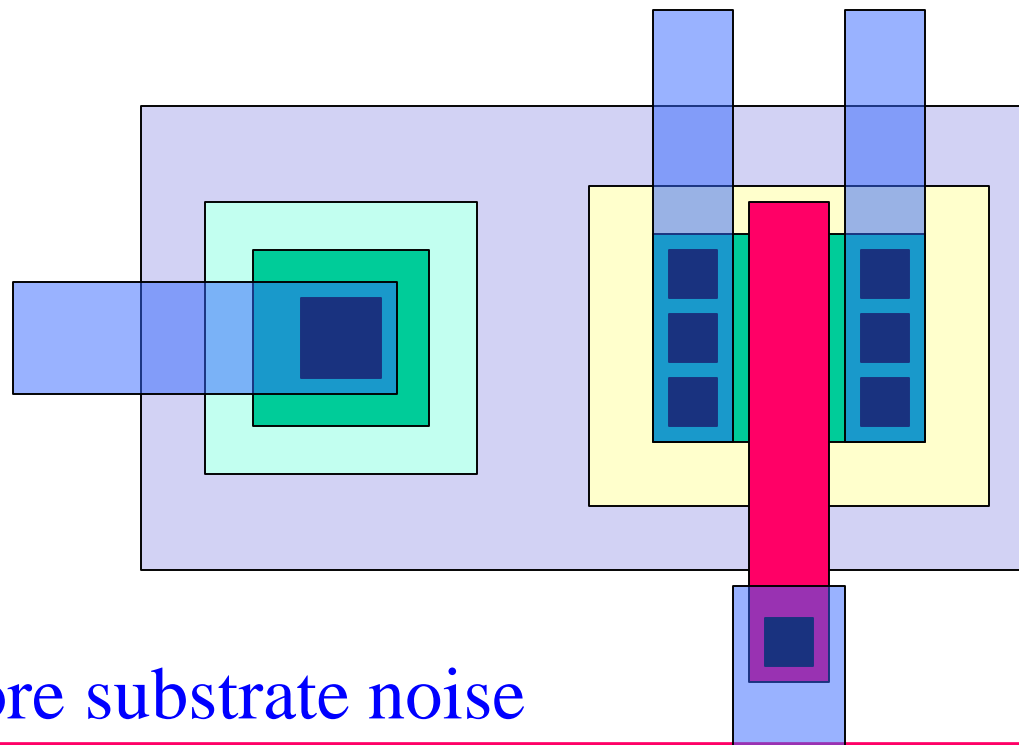
# Analog layout Issues

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- Noise is important in all analog circuits because it limits dynamic range.

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- Noise is important in all analog circuits because it limits dynamic range.
  - Body Contact
  - Higher neutral body resistance

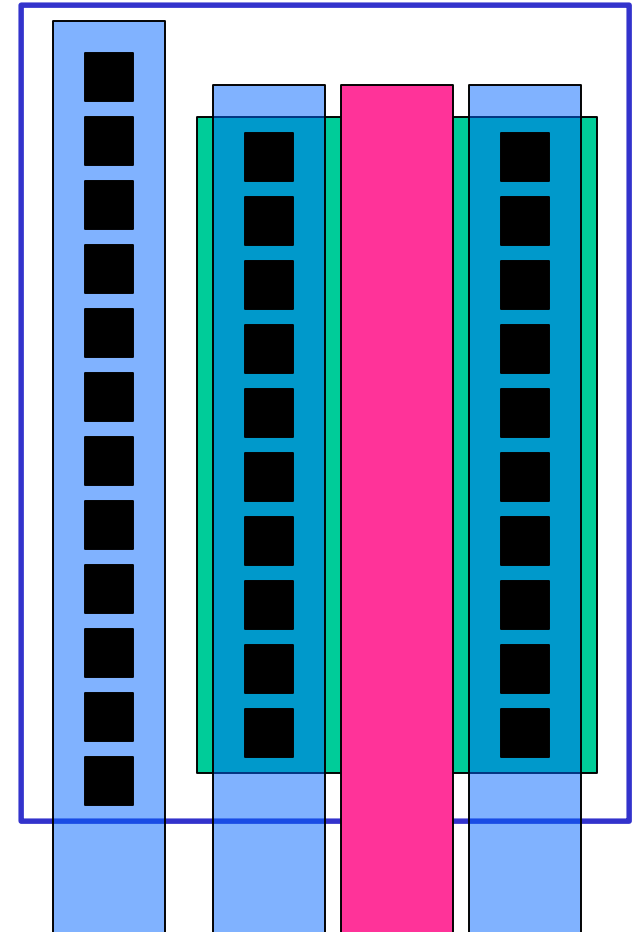


- Single Body Contact more substrate noise

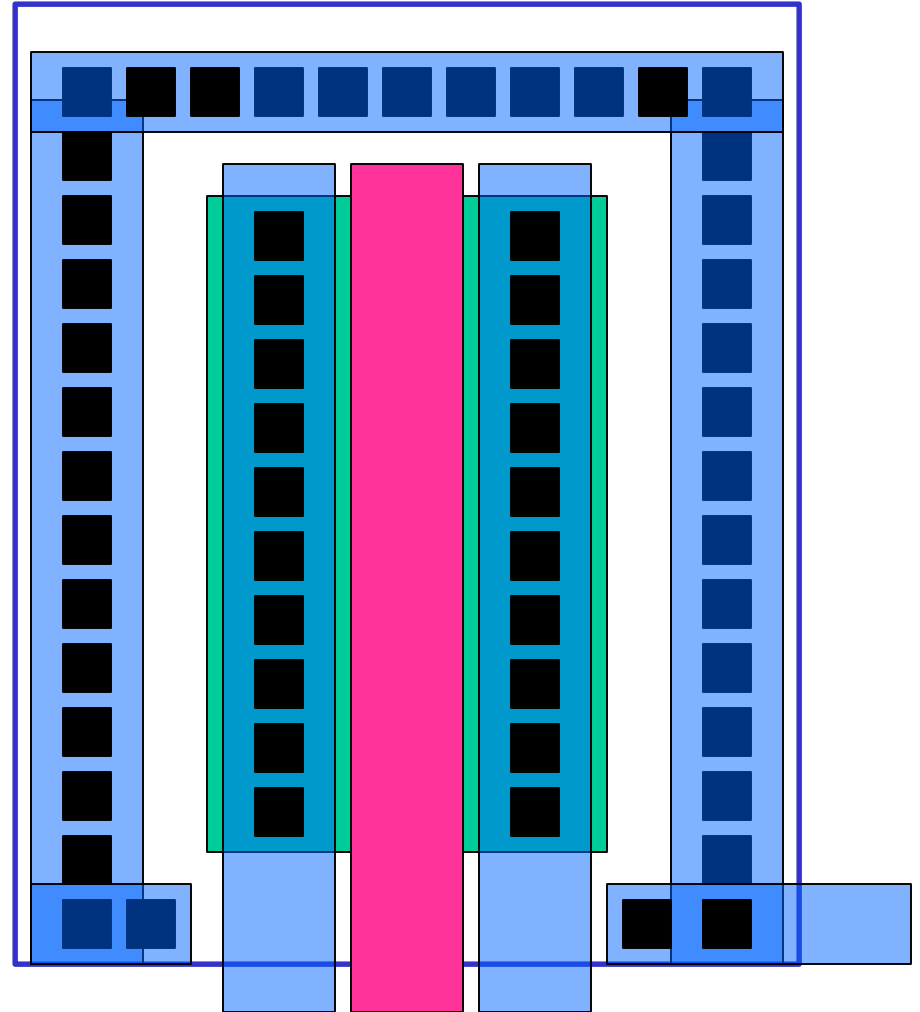
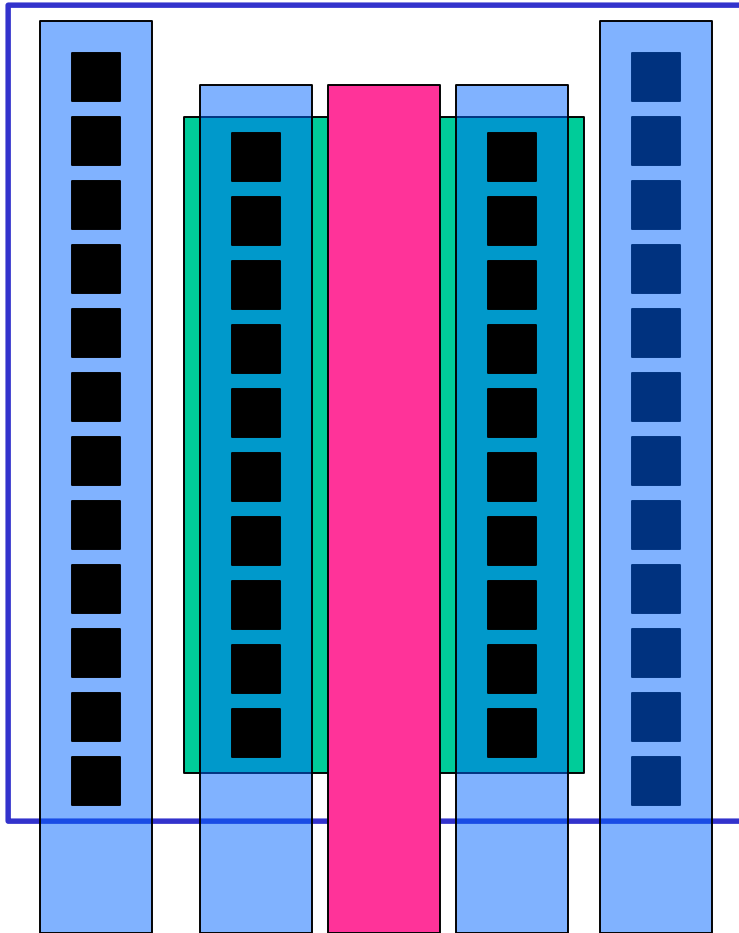


# Substrate contact

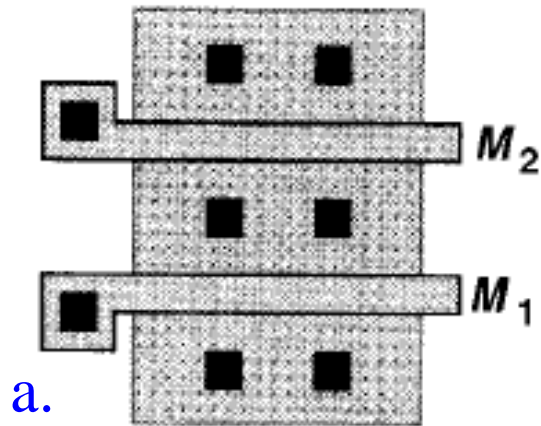
- Generous use of SUBSTRATE PLUGS
  - help to reduce the resistance of the neutral body region,
    - Minimizes the noise contributed by this resistance.
  - minimizes substrate noise because it provides a low impedance path to ground for the noise current



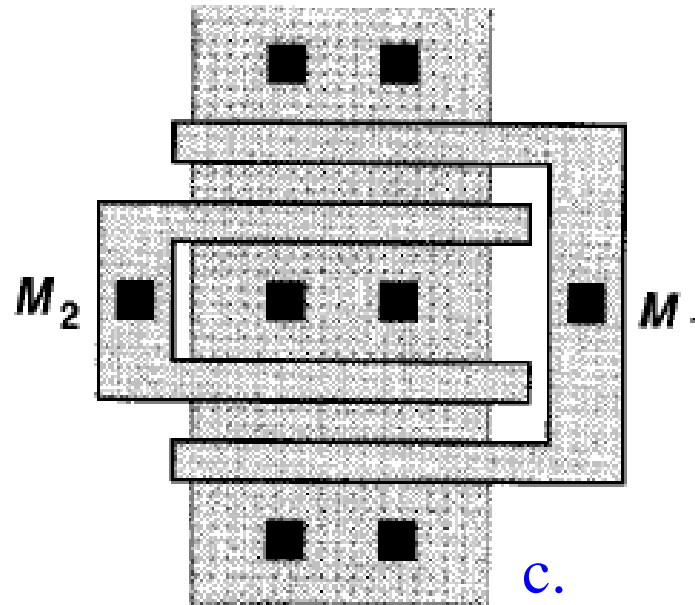
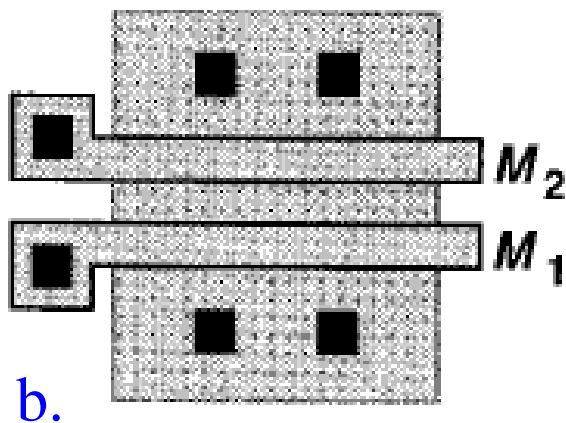
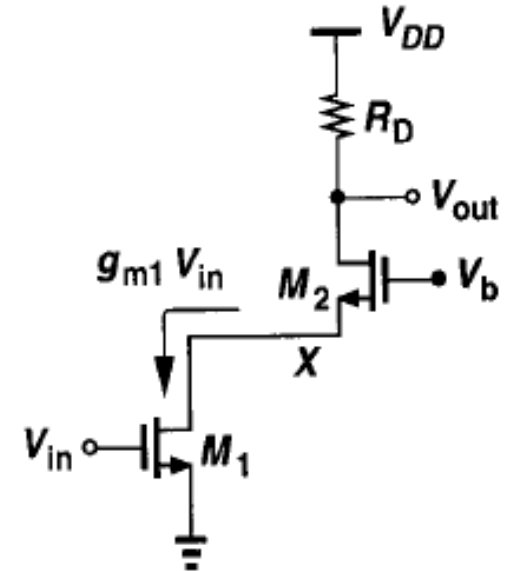
# Substrate contact



# Layout of a Cascode circuit

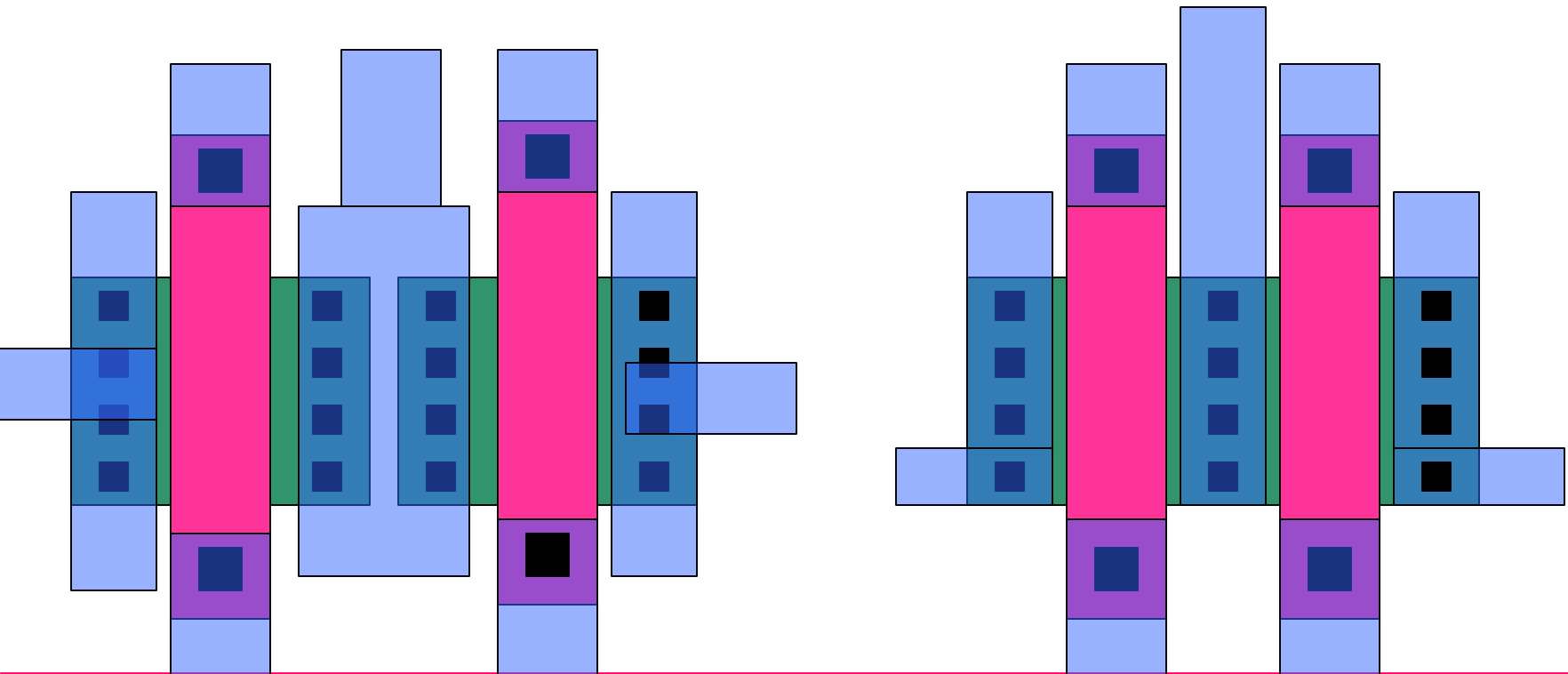
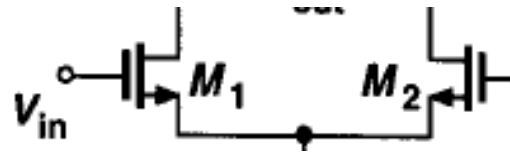


Shared Source  
Drain

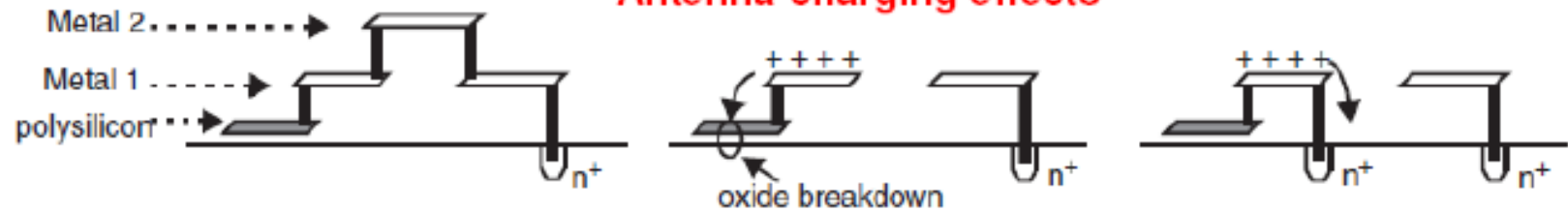


Shared Source  
Drain-multifinger  
Layout

# Common Terminal

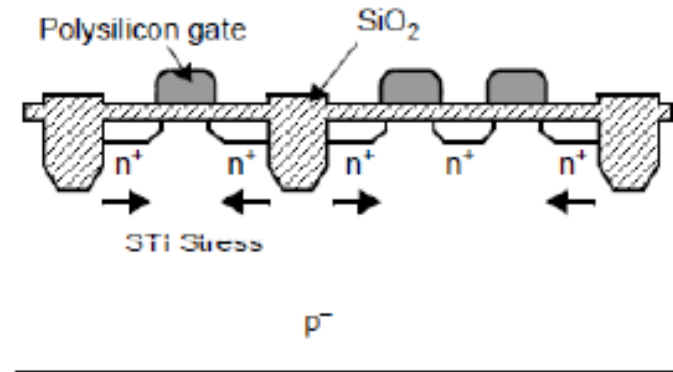


## Antenna charging effects



## Well proximity effects (WPE)

## Shallow Trench Isolation (STI) Stress



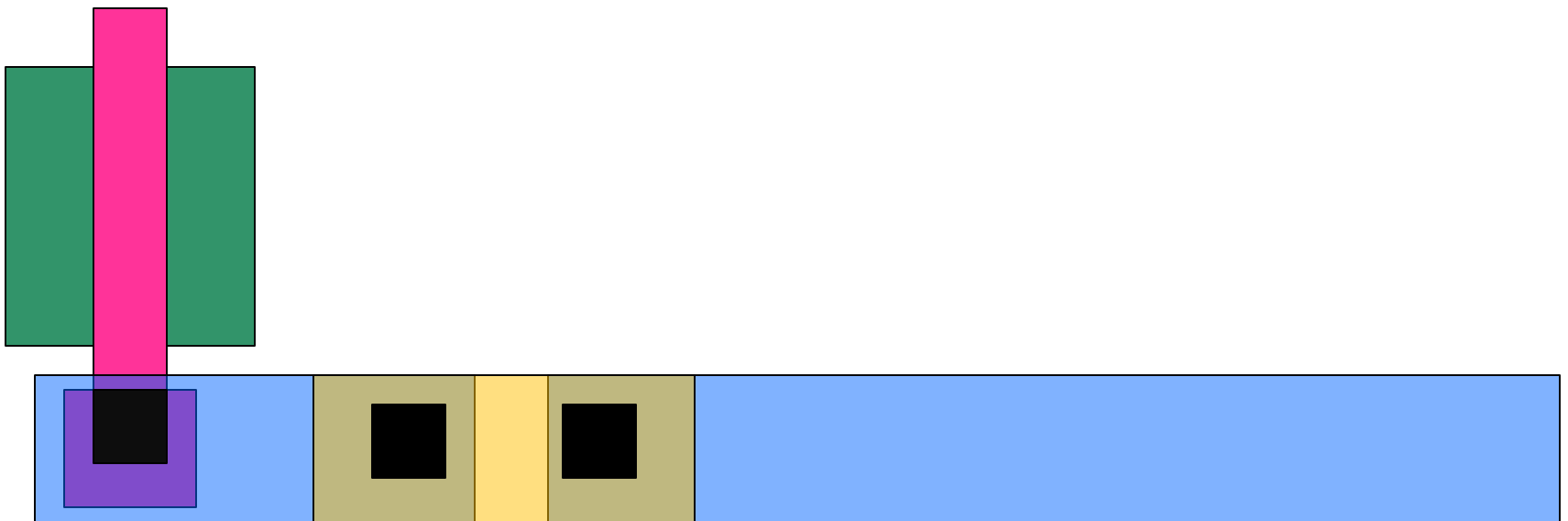
# Antenna Effect

- Metal Etching
  - There will be charge accumulation on Metal1 during plasma etching (of metal1) causing damage to thin gate oxide (Large metal area)



# Antenna Effect

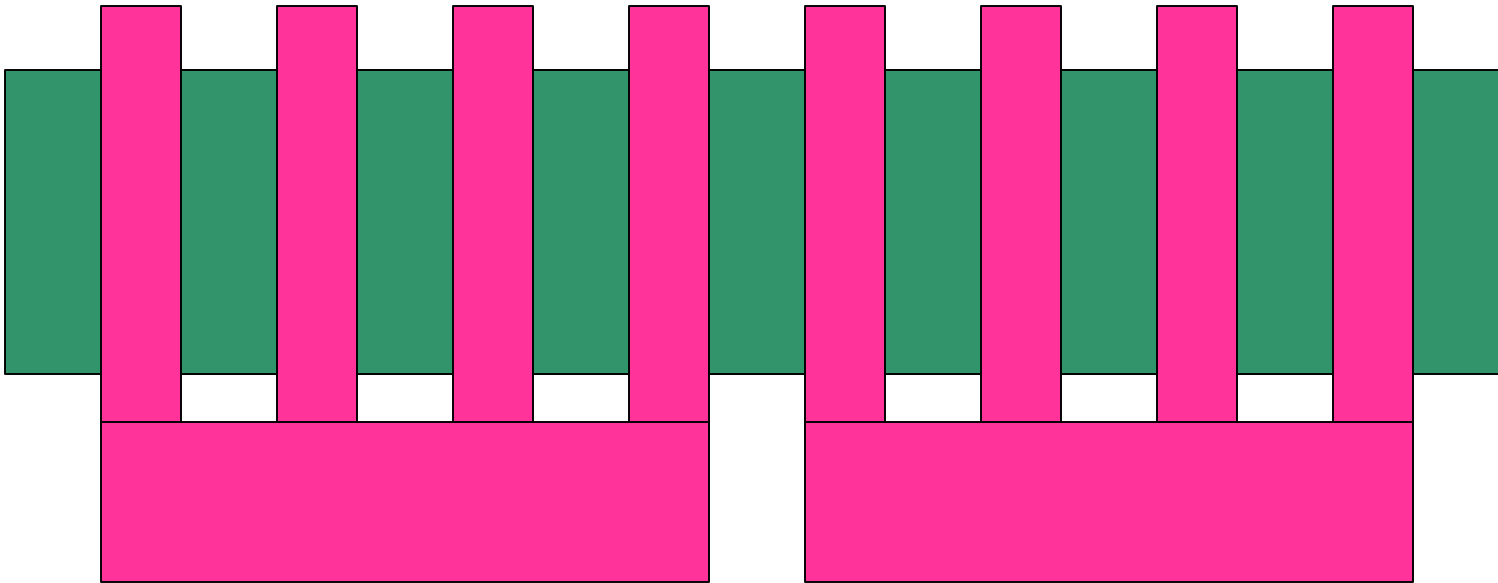
- Metal Etching
  - There will be charge accumulation on Metal1 during plasma etching (of metal1) causing damage to thin gate oxide (Large metal area)



Avoids antenna effect

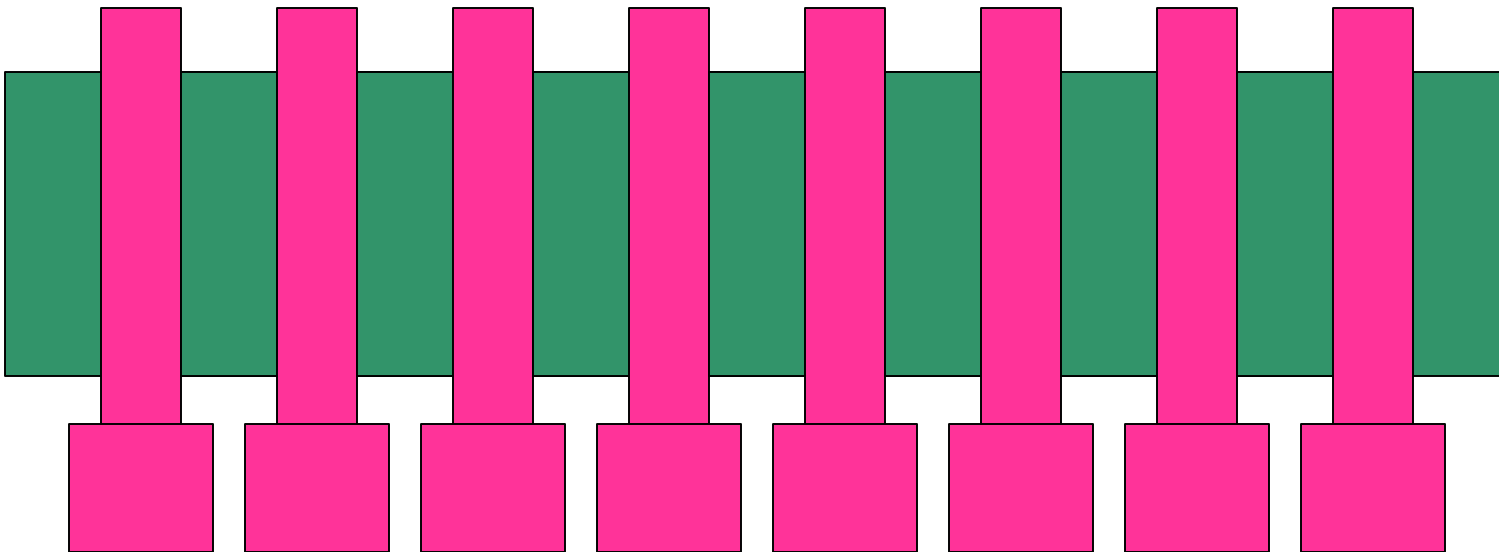
# Antenna Effect

- RIE of Poly silicon





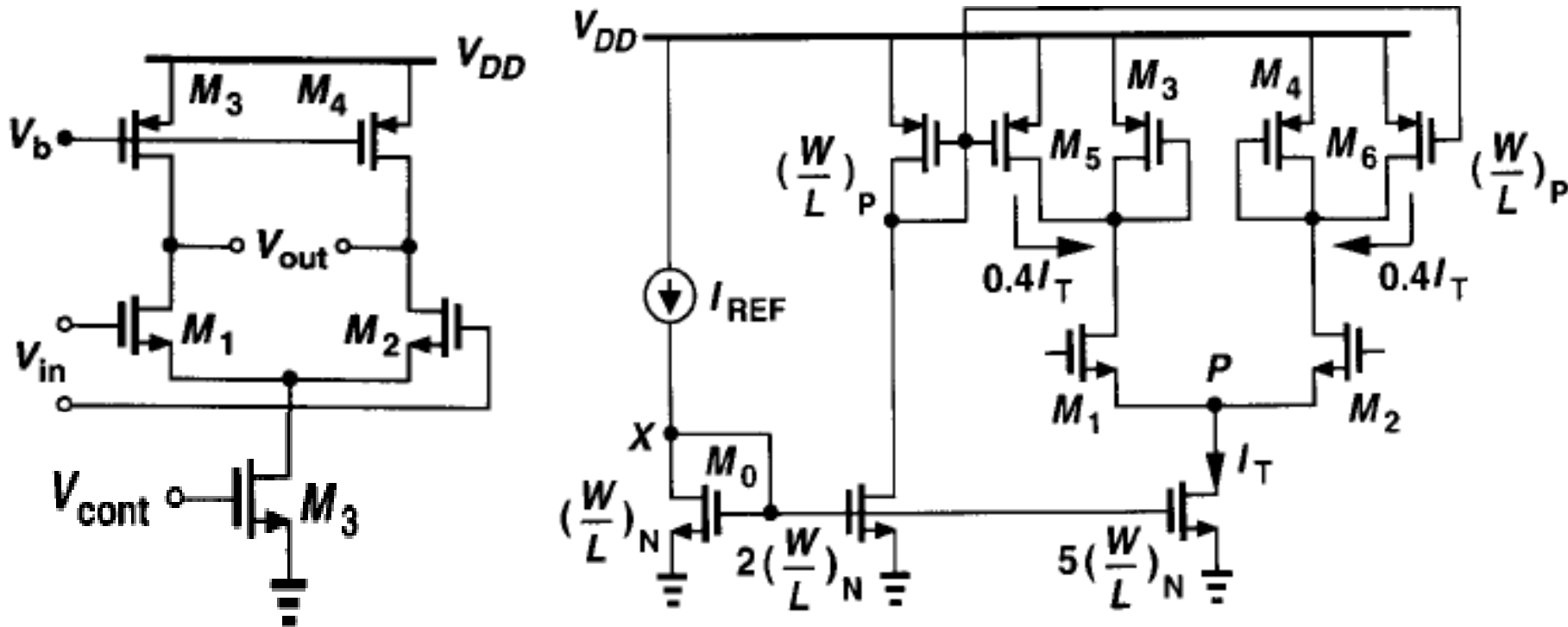
- Make connections at M1 level.



# Analog layout Issues

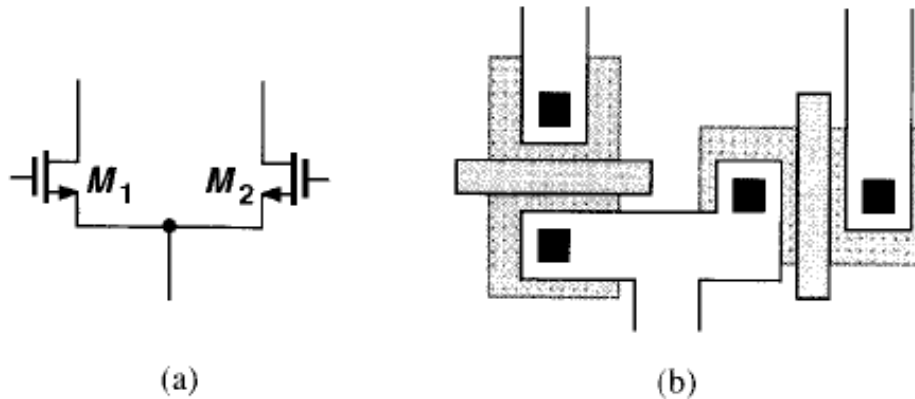
- Matching components

- In analog electronics it is often necessary to have matched pairs of devices with identical electrical properties, e.g. input transistors of a differential stage, and current mirror



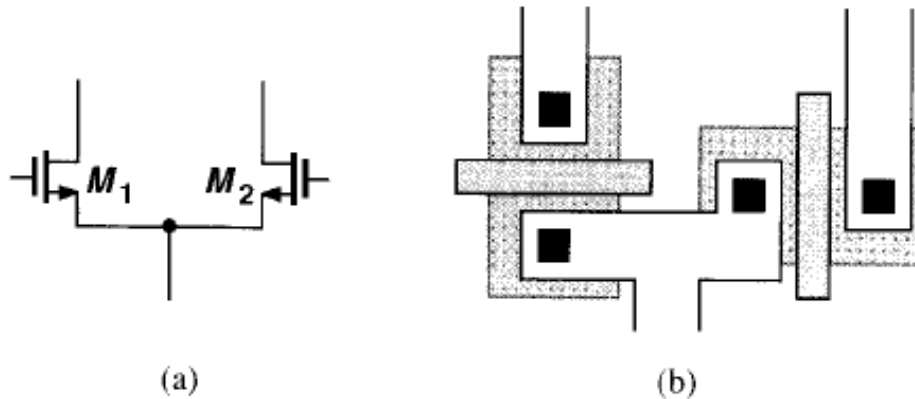
# Layout of Matched Transistors

- Matched transistors are used extensively in both analog and digital CMOS circuits.
  - In theory two device with the same size have the same electrical properties.



# Layout of Matched Transistors

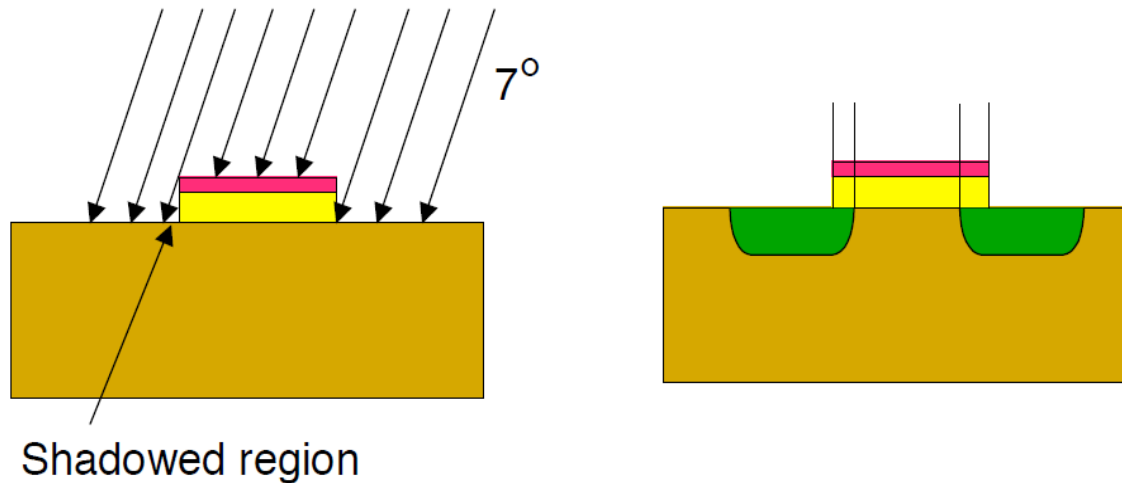
- Matched transistors are used extensively in both analog and digital CMOS circuits.
  - In theory two device with the same size have the same electrical properties.



**In reality there is always process variations**

# Silicon is anisotropic

- Ion implantation is performed at an angle causing shadow
- Source and drain may not be symmetric due to ion implantation angle,
  - necessary to avoid implant depth issues (channeling).



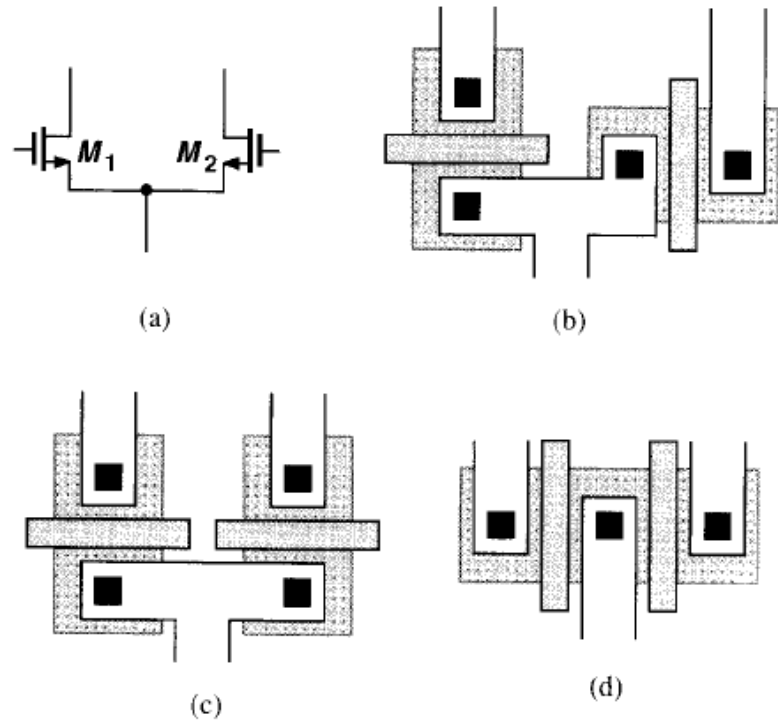
Source and drain are not equivalent

# Photo-lithographic invariance (PLI)

- Lithography effects are different in different direction.
- Orientation is important in analog circuits for matching purposes
  - C and D are better
  - Maintain orientation

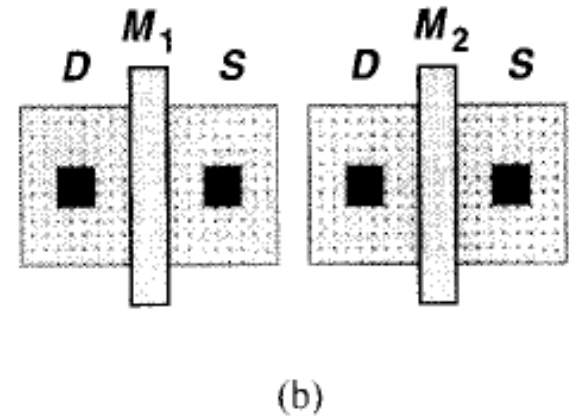
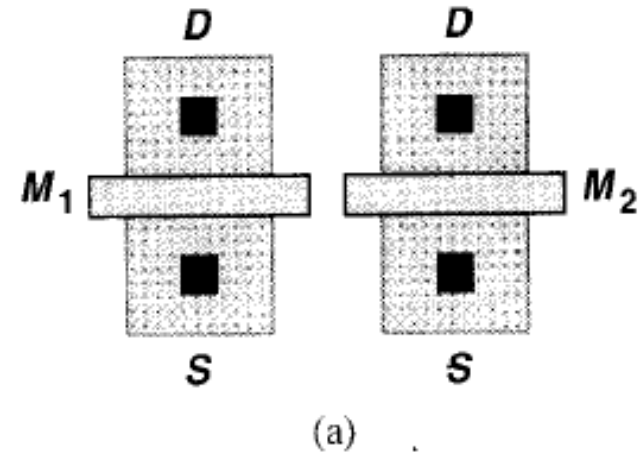
C. Gate aligned

D. Parallel gate:



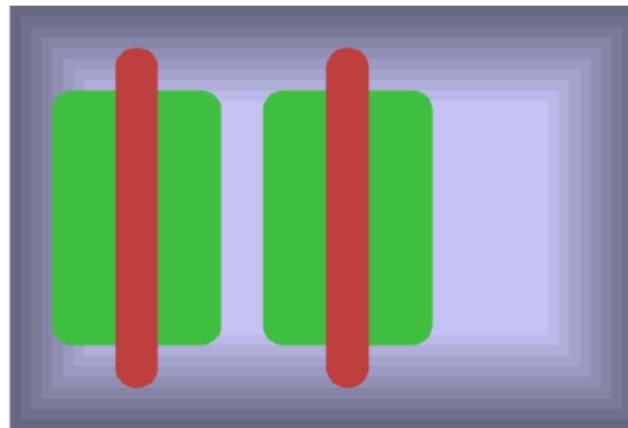
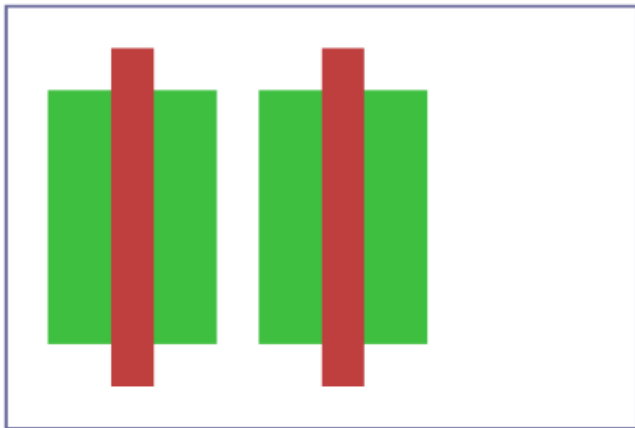
# Photo-lithographic invariance (PLI)

- Gate aligned
- Parallel gate:
  - Two drains have different surroundings
  - Two sources have different surroundings
- Current flows in the same direction



# Well Proximity Effect

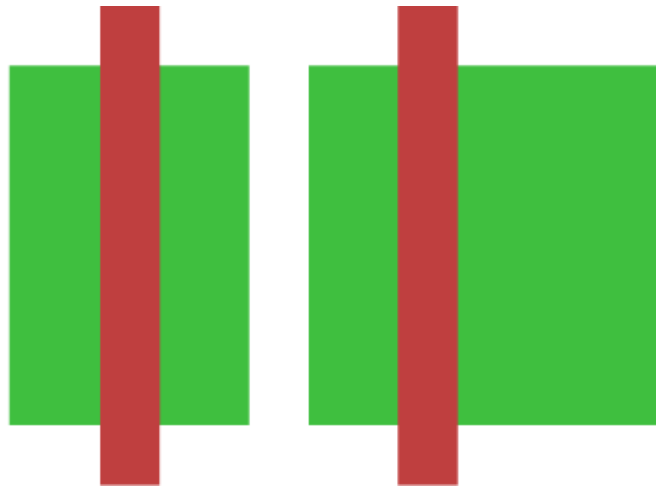
- High energy ion implants to form the well.
- Scattering from the edge of the photoresist mask, and embedding in the silicon surface (near well edge).
- Transistors close to the well edge will therefore have different properties.
- This is known as the well proximity effect (WPE). Important for matching.



As with S/D, implantation angle may render the scattering and doping asymmetric

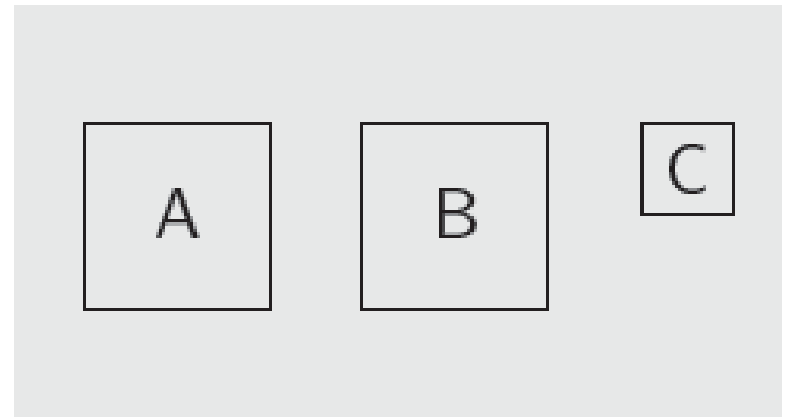


- Shallow trench isolation strains the active area of the transistor. Influences mobility and threshold voltage (stress induced enhancement or suppression of dopant diffusion).
- Distance between gate and STI impacts performance.
- Important for matching.



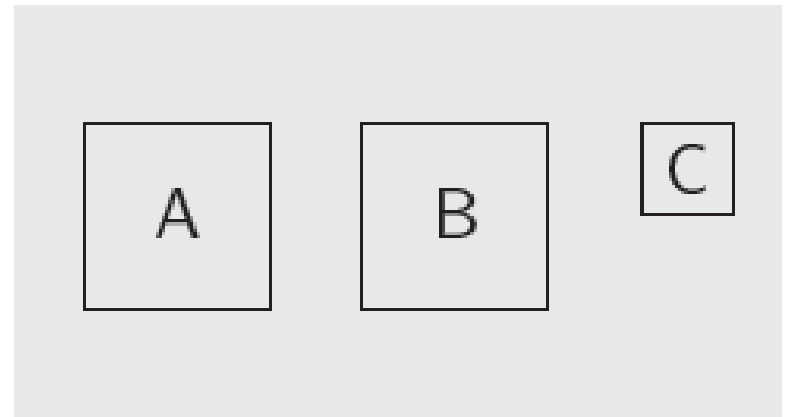
# Matching

- Layout techniques to minimize the errors introduced by process variations.
- Two electrically equivalent components: A and B
  - Drawn identically
  - A and B have same shape in area and perimeter
  - Are they Identical ?
  - Do they have the same surrounding?



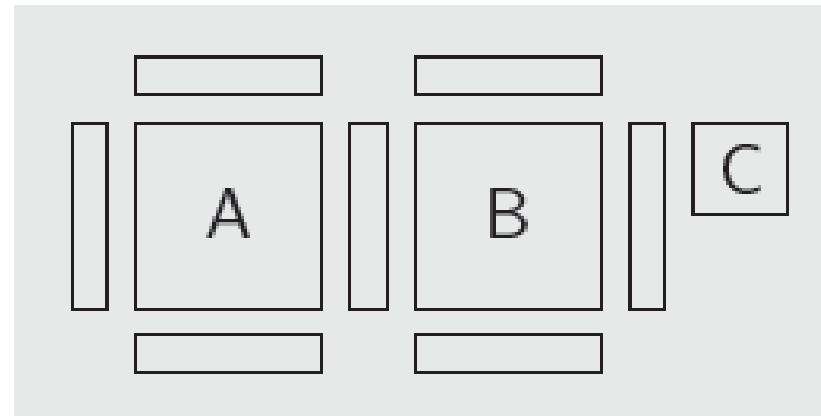
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  - Do they have the same surrounding?
  - **No?**



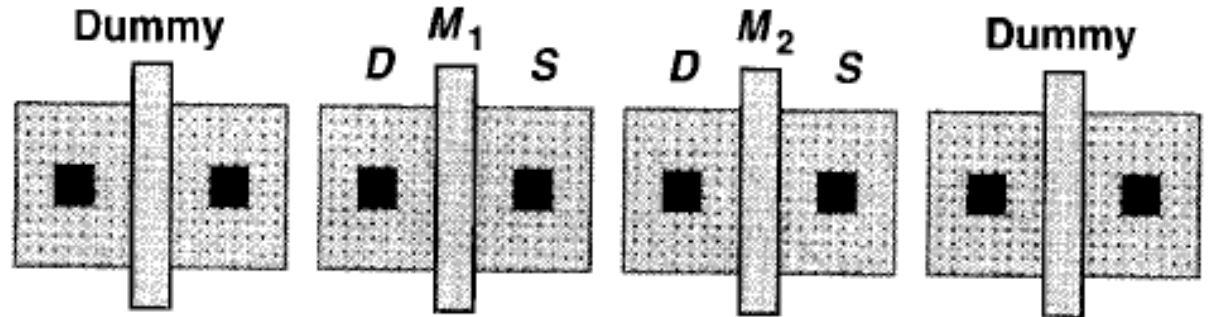
# Unit Matching

- Layout techniques to minimize the errors introduced by process variations.
- Two electrically equivalent components. A and B
  - Use Dummies to have identical surroundings

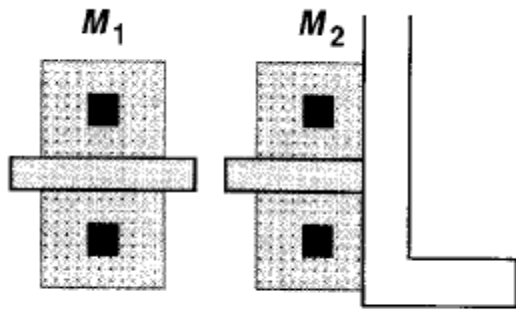


# Layout of Matched Transistors

- Add dummy transistors to improve symmetry

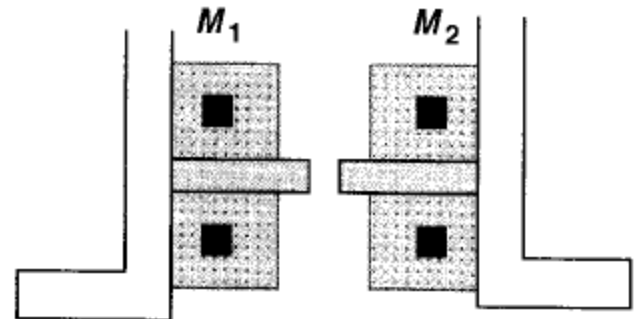


- Presence of Metal line over  $M_2$  destroys symmetry



(a)

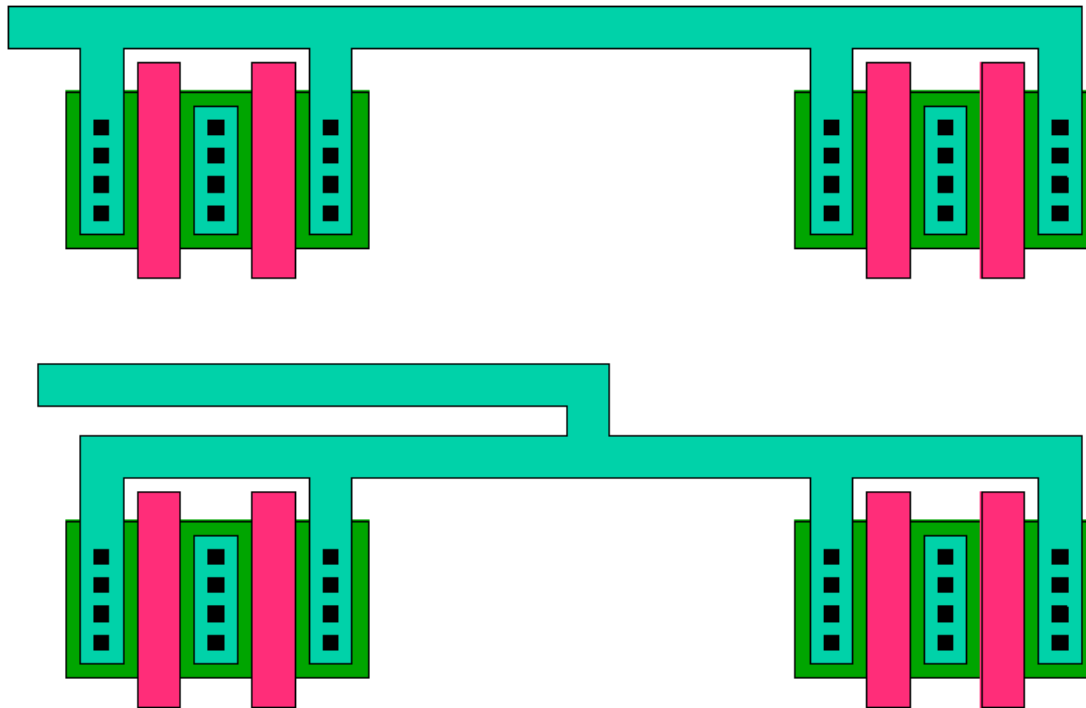
- Replicate Metal line over  $M_1$  improves symmetry



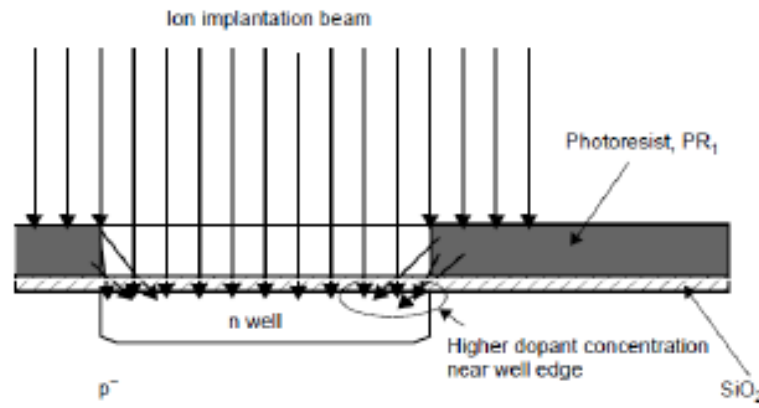
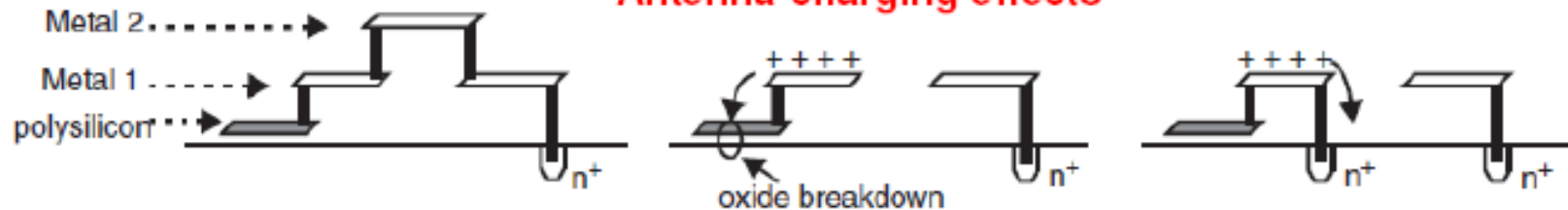
(b)

# Metal Interconnections

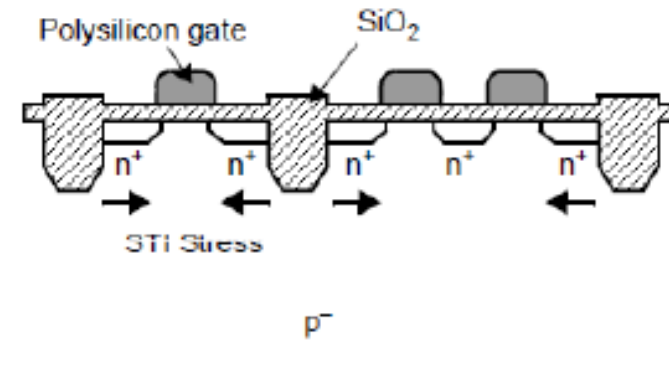
- Both the transistor should have same surrounding.
- Unbalanced metal routing will cause the transistors to see different source voltage.
- Also, distribute reference as current, not bias voltage.



## Antenna charging effects



## Well proximity effects (WPE)

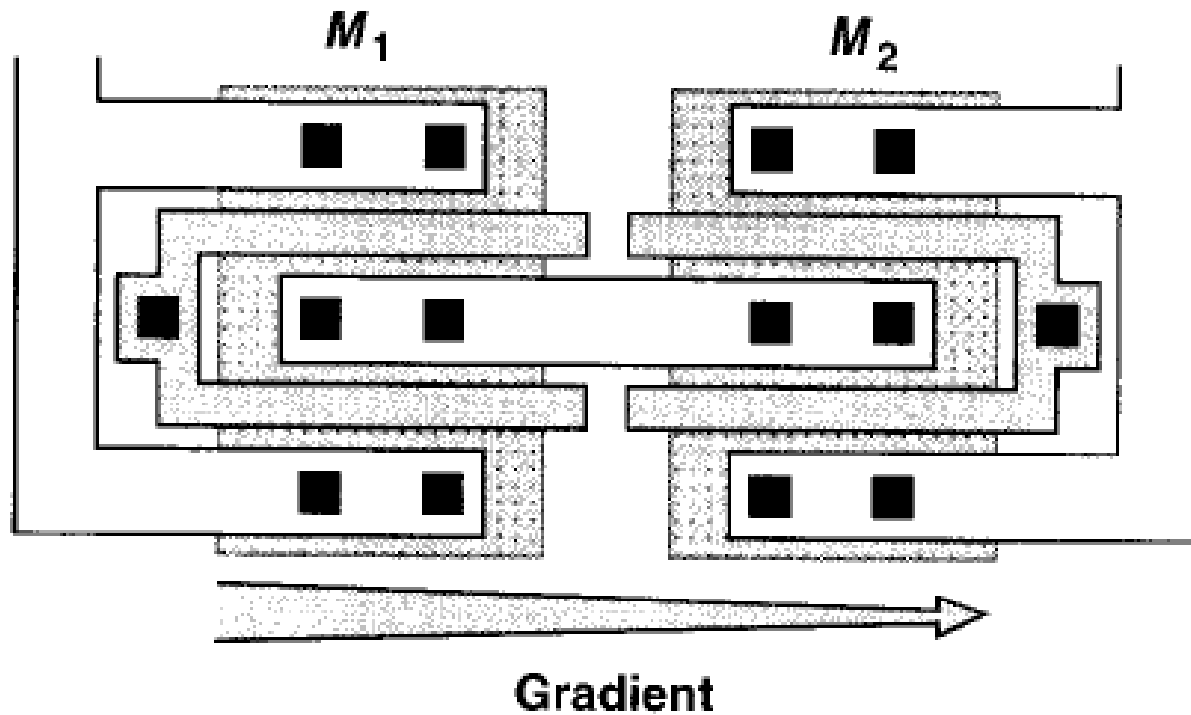


## Shallow Trench Isolation (STI) Stress

- **Planarity:** Optics requires planarity -> special local and global "fill" requirements -> density checks now standard like LVS/DRC.
- **Unintended Impact** of dummies on analog: matching, Inductor Q, Increased parasitics.
- **Antenna charging** : Connect diodes to prevent oxide damage during fabrication.
- **WPE:** Extra dopants due to scattering near well edge -> threshold voltage shifts -> minimize proximity to well edges
- **STI stress:** Affects mobility -> orient all devices the same way and use dummy devices

# Unit matching

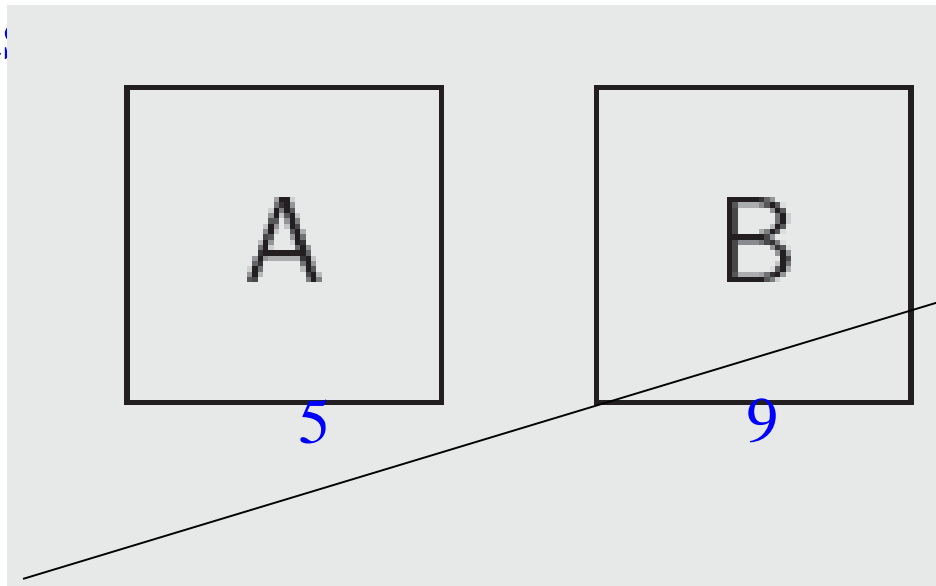
- Gradient along x-axis destroys symmetry





# Process Variation

- Process variations can locally be approximated with a linear gradient.
- Example: Desired Resistor values ;  $A = 7$  units and  $B = 7$  units
- Changed due to Gradient as follows.
- $A = 5$  units

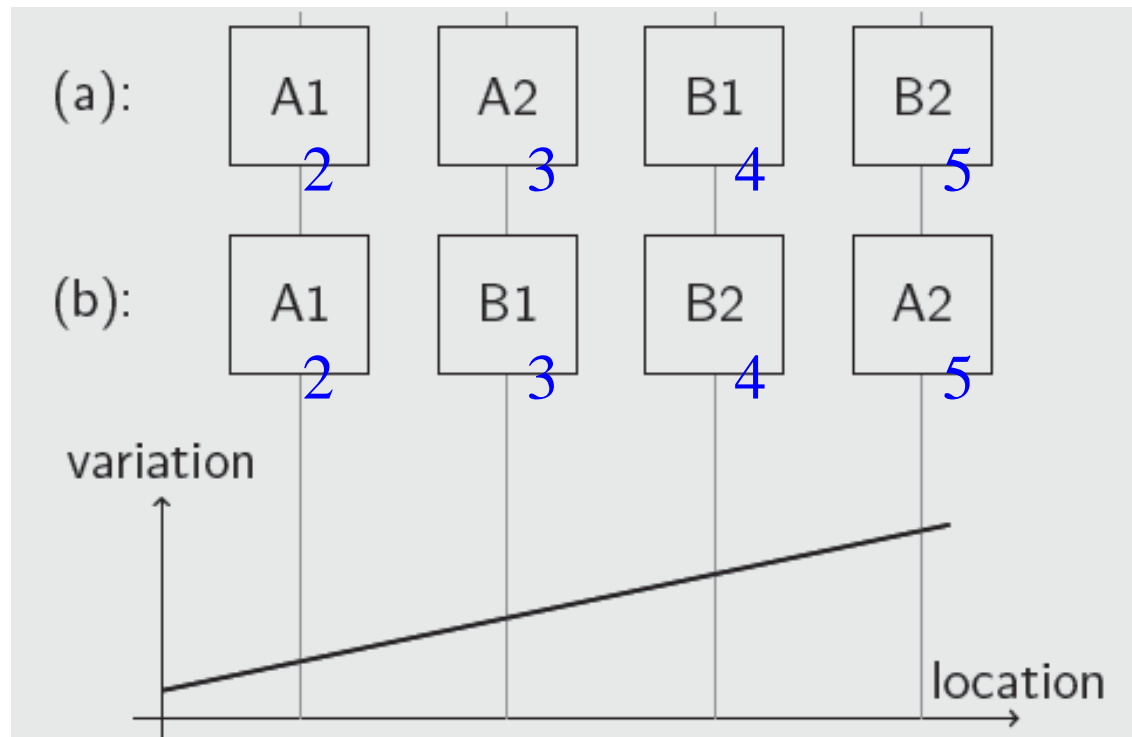


# Process variations

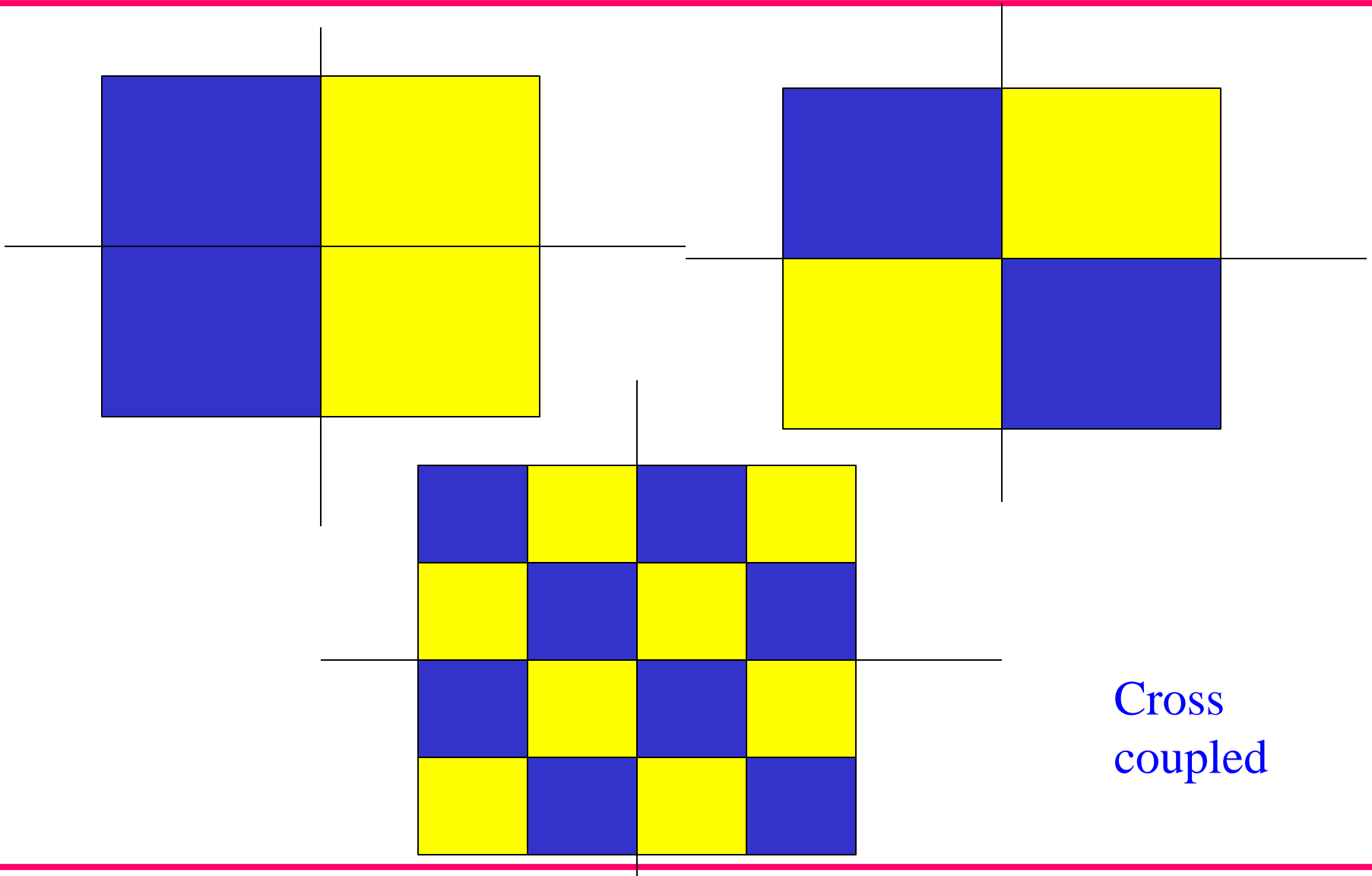
- can locally be approximated with a linear gradient.

(a):  $A1 + A2 < B1 + B2$

(b):  $A1 + A2 = B1 + B2$  (Common-centroid layout)

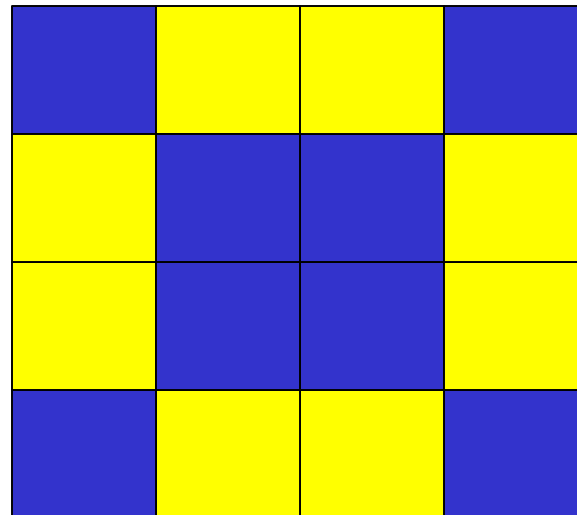
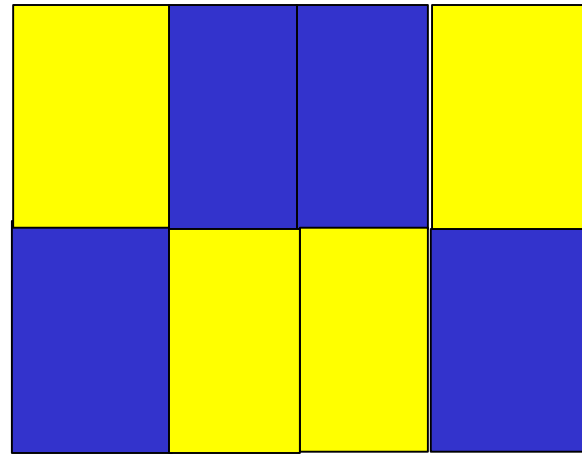
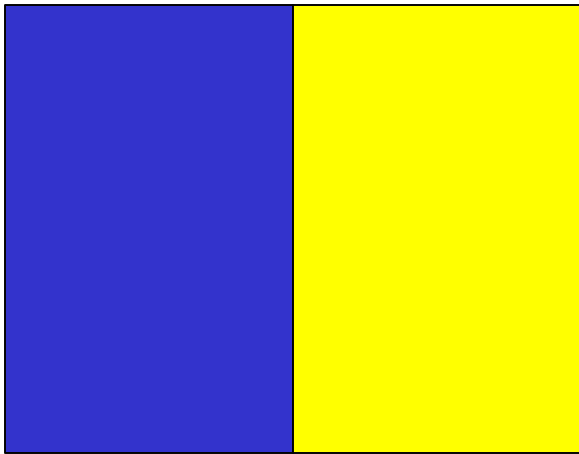


# Common Centroid Layouts



Cross  
coupled

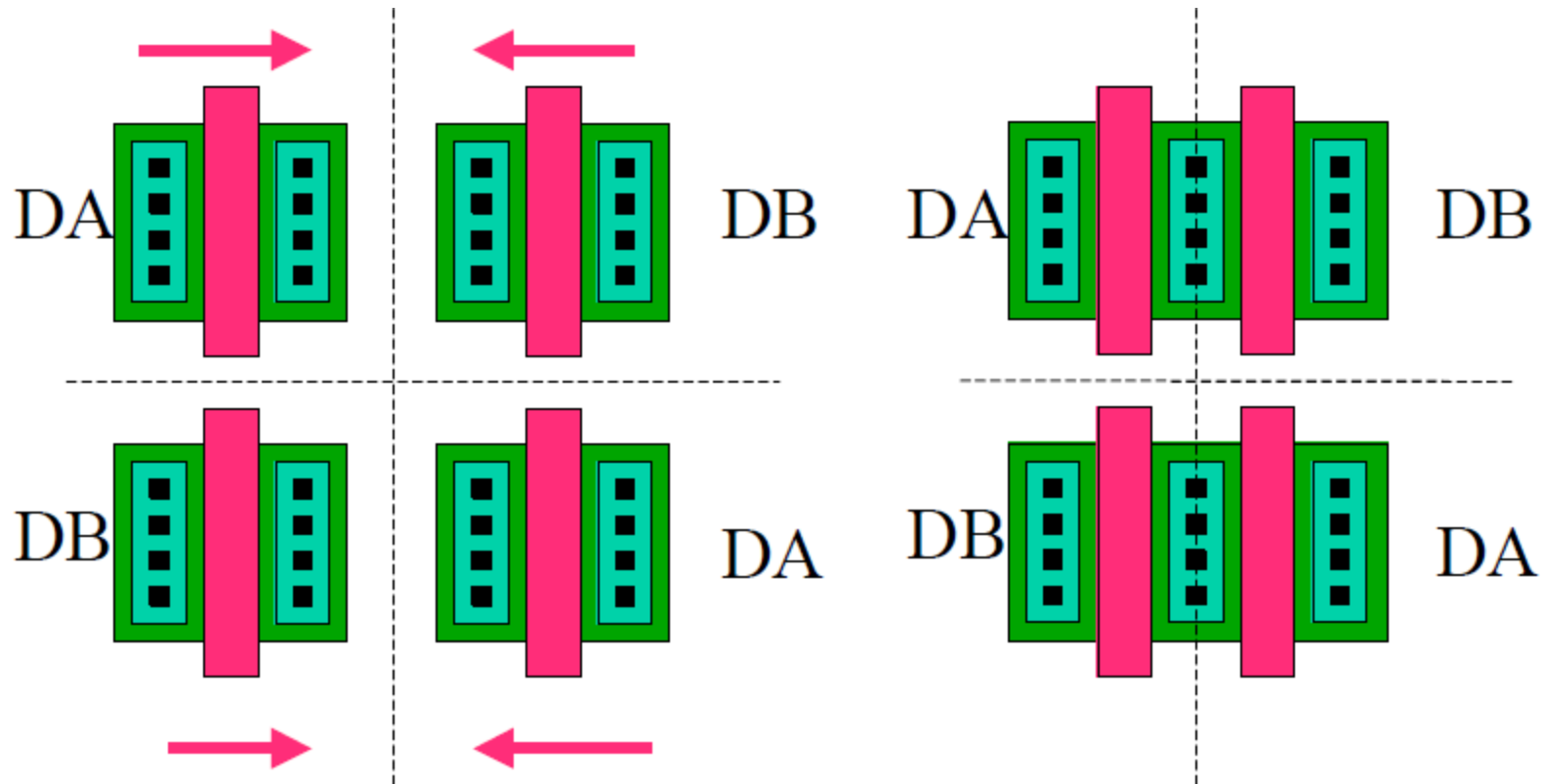
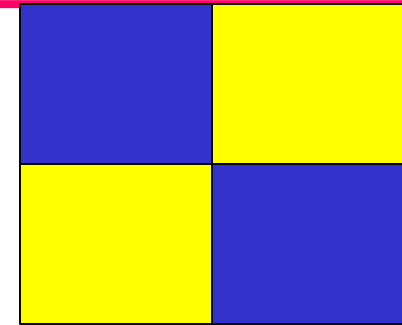
# Common Centroid Layouts

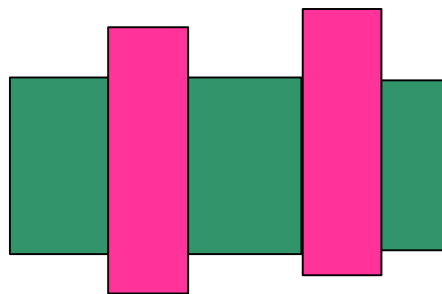
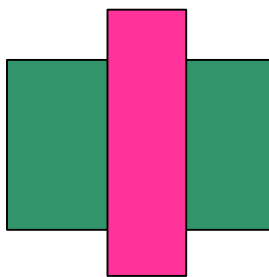
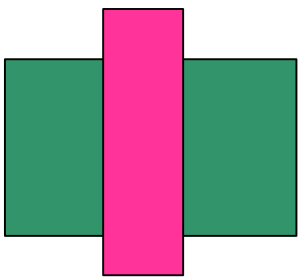
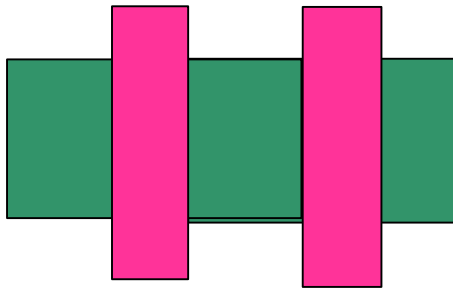
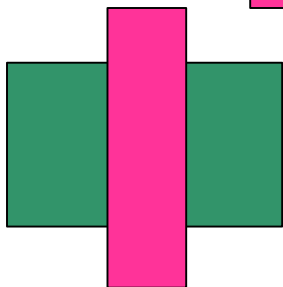
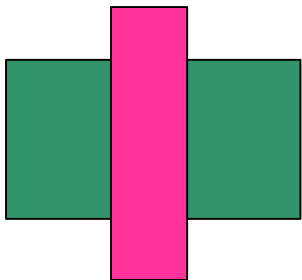
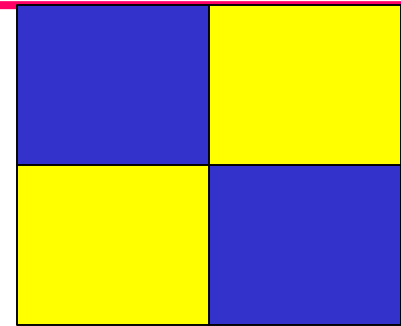
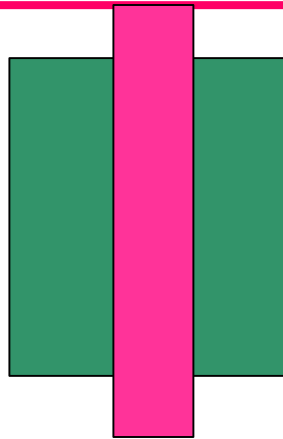
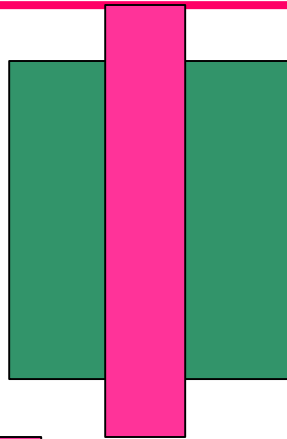
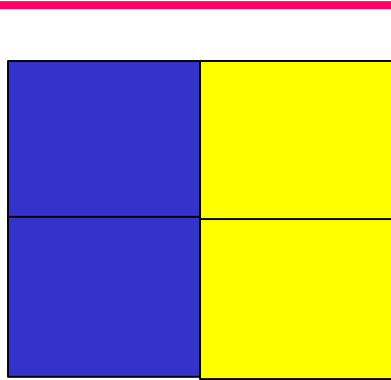


Tiled

# Common Centroid Layout

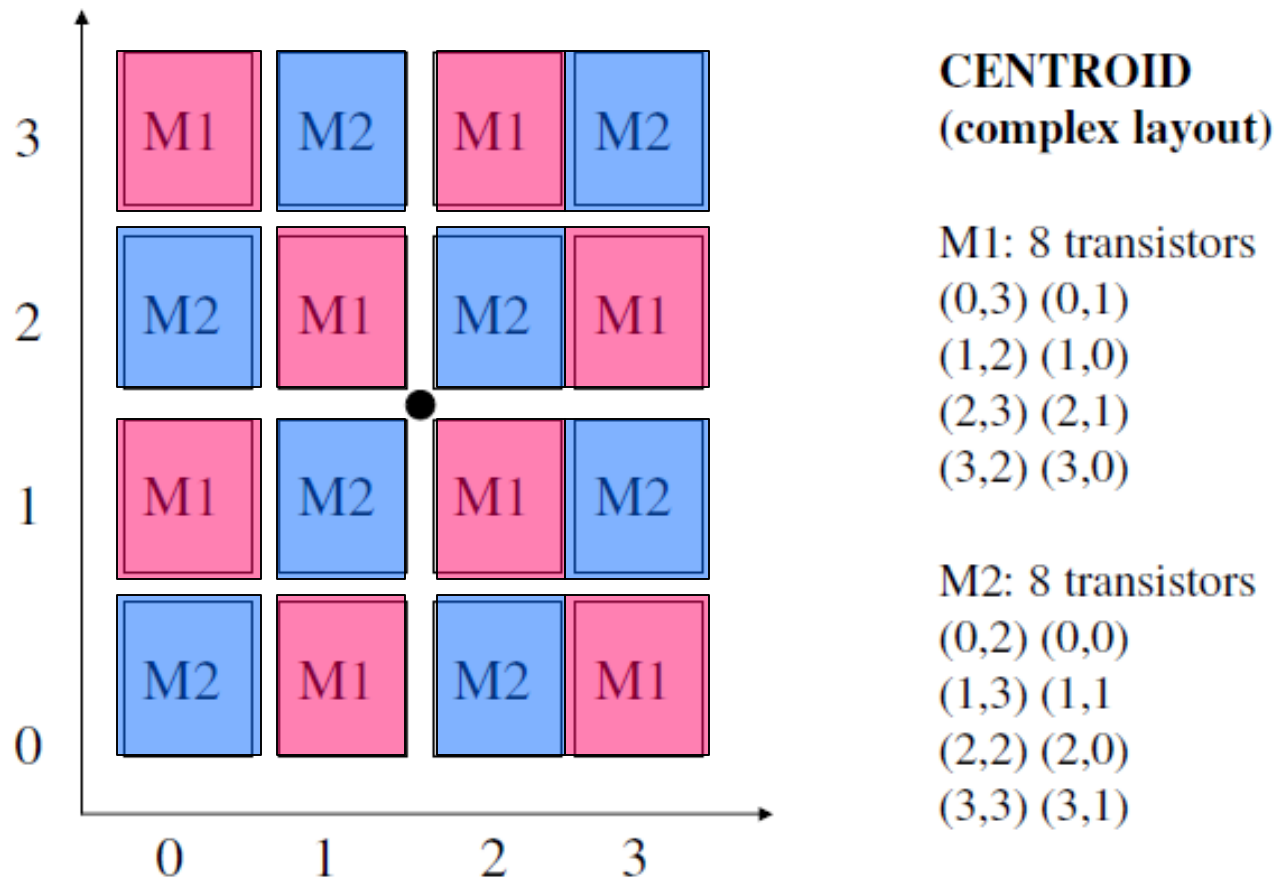
- Gradients are compensated
- Poly and metal interconnections are complex

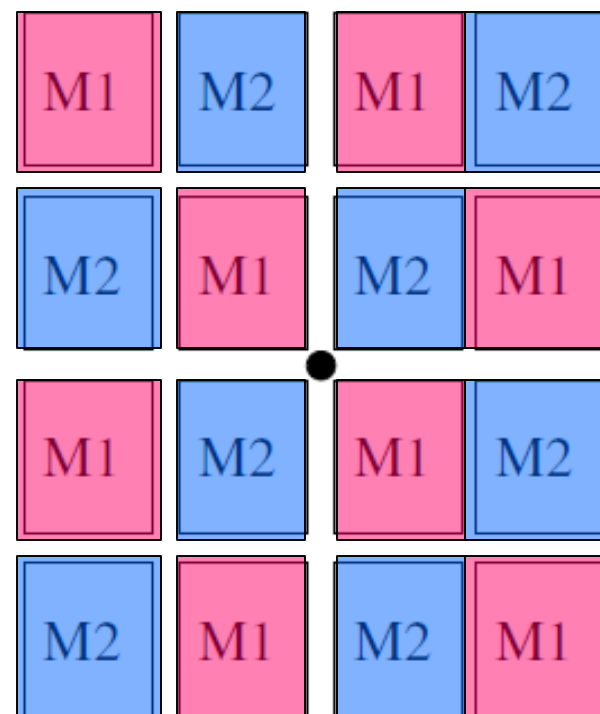
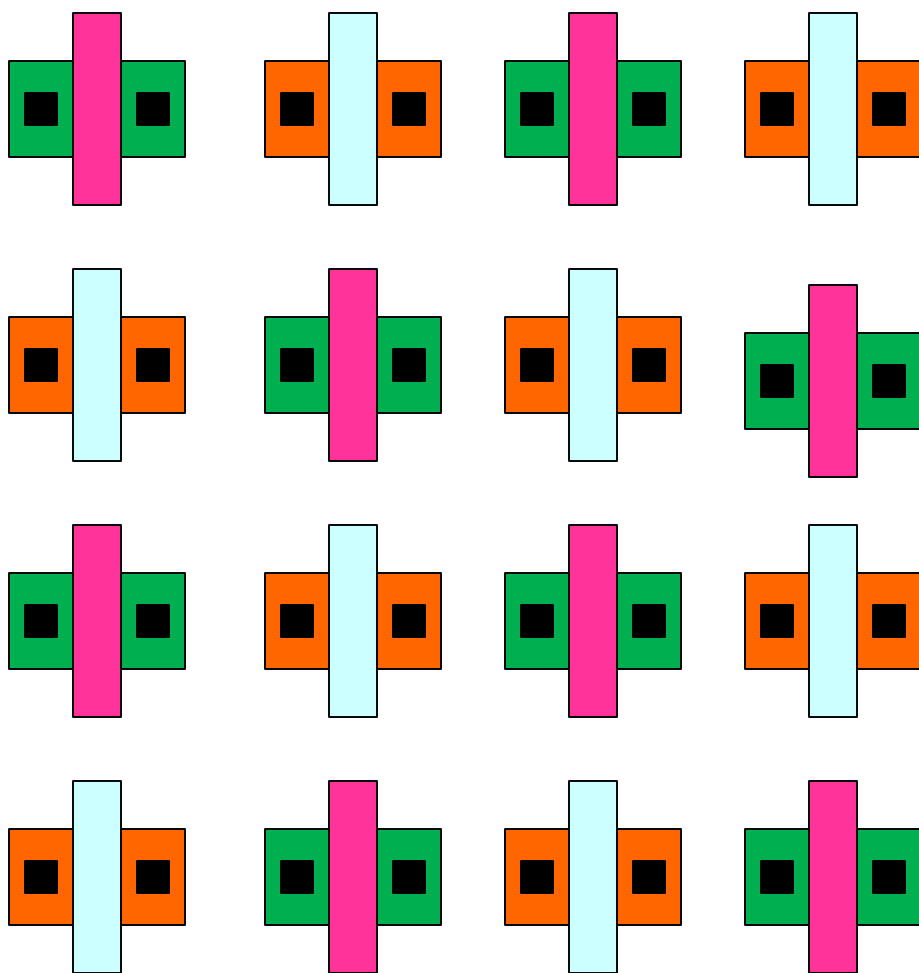




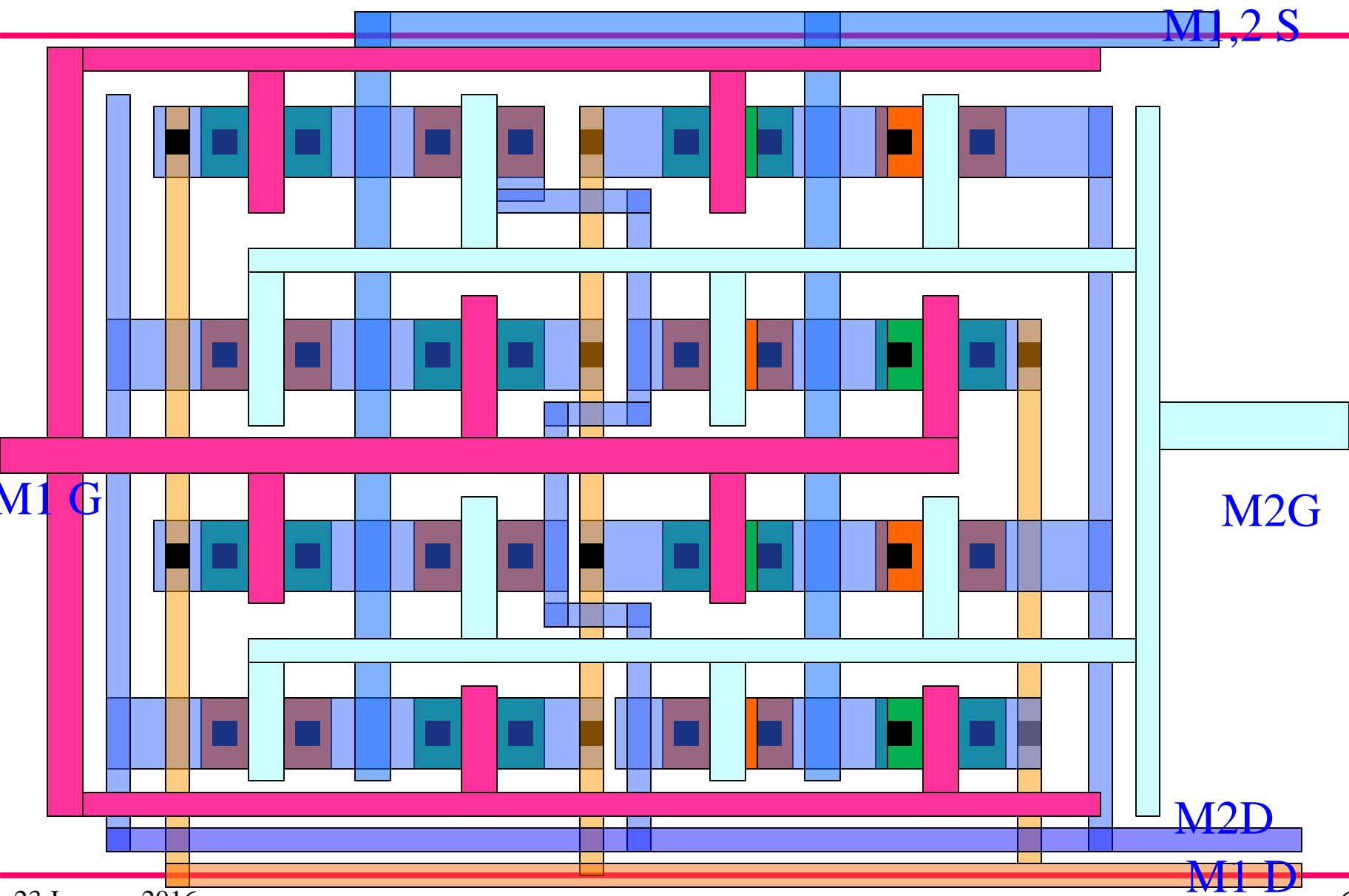
# Common Centroid Layouts

- Mitigates variation in both x and Y direction









# Common Centroid Layout

ABBA  
BAAB

ABBAABBA  
BAABBAAB

ABBAABBA  
BAABBAAB  
ABBAABBA

ABBAABBA  
BAABBAAB  
BAABBAAB  
ABBAABBA

ABA  
BAB

ABAABA  
BABBAB

ABAABA  
BABBAB  
ABAABA

ABAABAABA  
BABBABBAB  
BABBABBAB  
ABAABAABA

ABCCBA  
CBAABC

ABCCBAABC  
CBAABCCBA

ABCCBAABC  
CBAABCCBA  
ABCCBAABC

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CBAABCCBA  
CBAABCCBA  
ABCCBAABC

AAB  
BAA

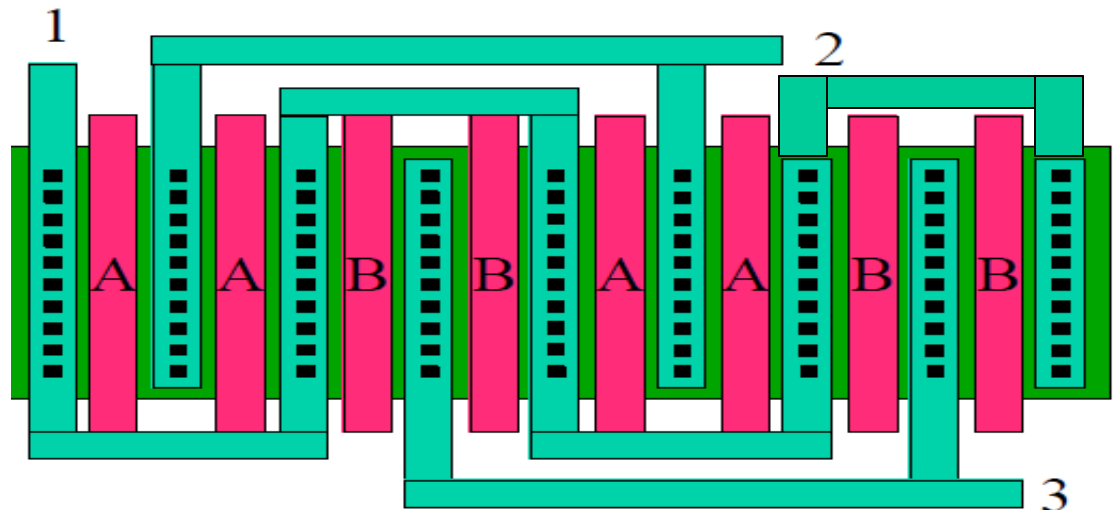
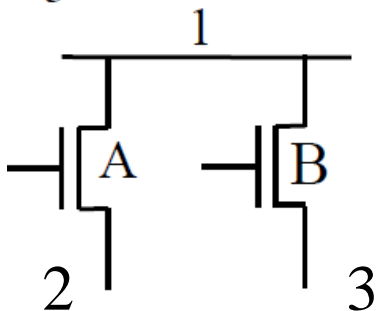
AABBAA  
BAAAAB

AABBAA  
BAAAAB  
AABBAA

AABBAA  
BAAAAB  
BAAAAB  
AABBAA

# Matched Transistors-Interdigitized Layout Style

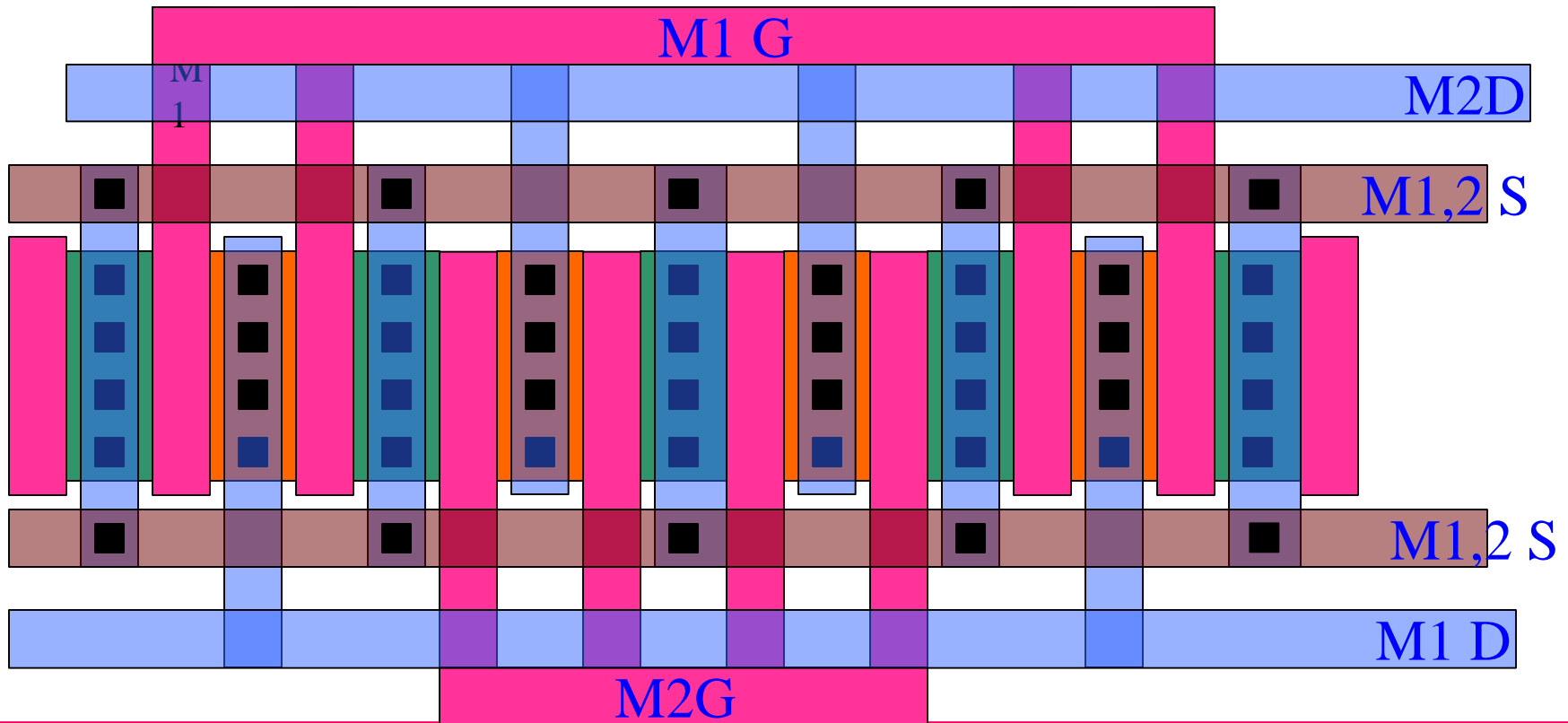
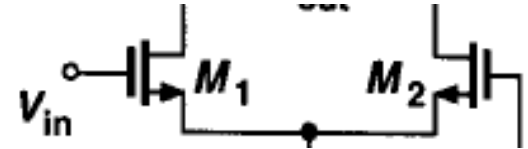
- Inter-digitized layout style Averages the process variations among transistors
  - Common terminal is like a serpentine
  - Two matched transistors with one common terminal
  - Split the transistor in two equal parts
  - 4 fingers for each transistors, Arrange AABBAABB



# Matched Transistors

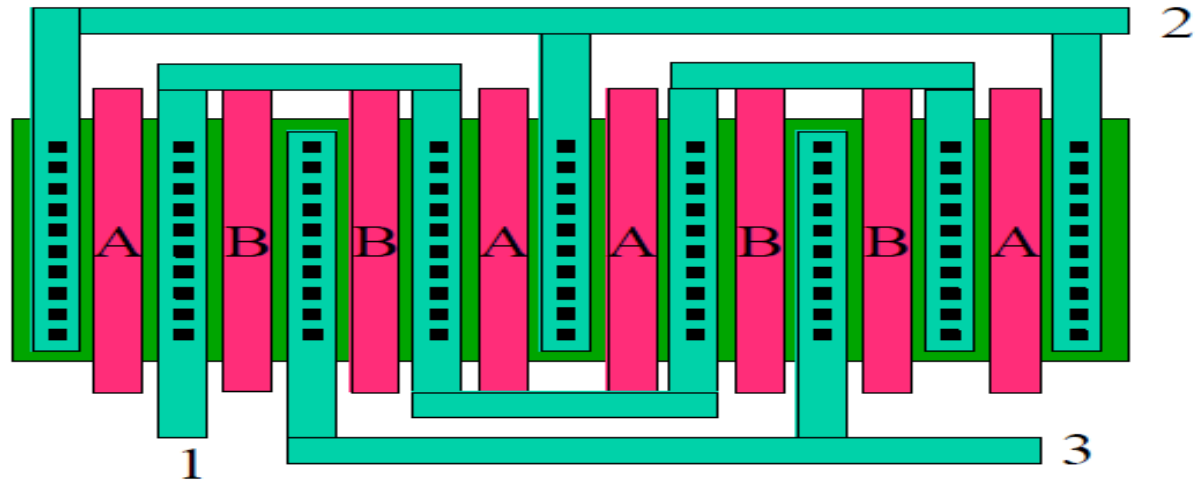
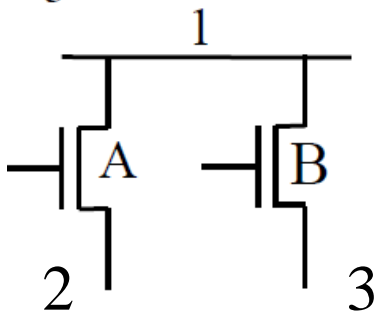
To achieve both common-centroid and PLI matched transistors has to be split into 4 fingers.

AABBBA



# Matched Transistors

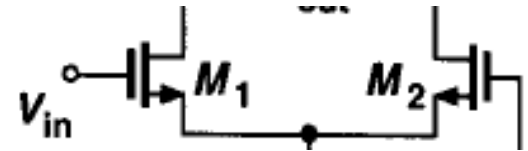
- Or ABBAABBA
- Use dummies if needed
- Uneven total drain area between A and B.
  - This is undesirable for ac conditions:
  - capacitors and other parameters may not be equal
  - A more robust approach



# Matched Transistors

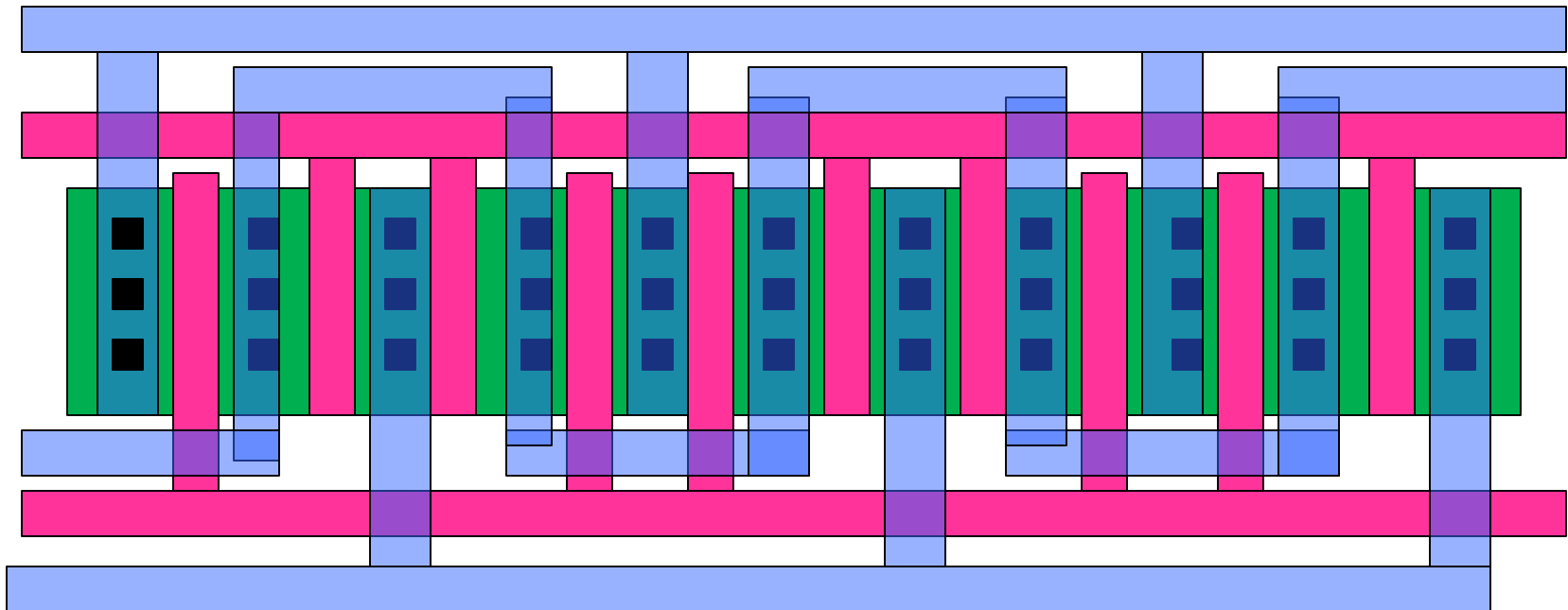
M1M2 M2M1 M1M2 M2M1 M1M2

1 2 3 4 5 6 7 8 9 10



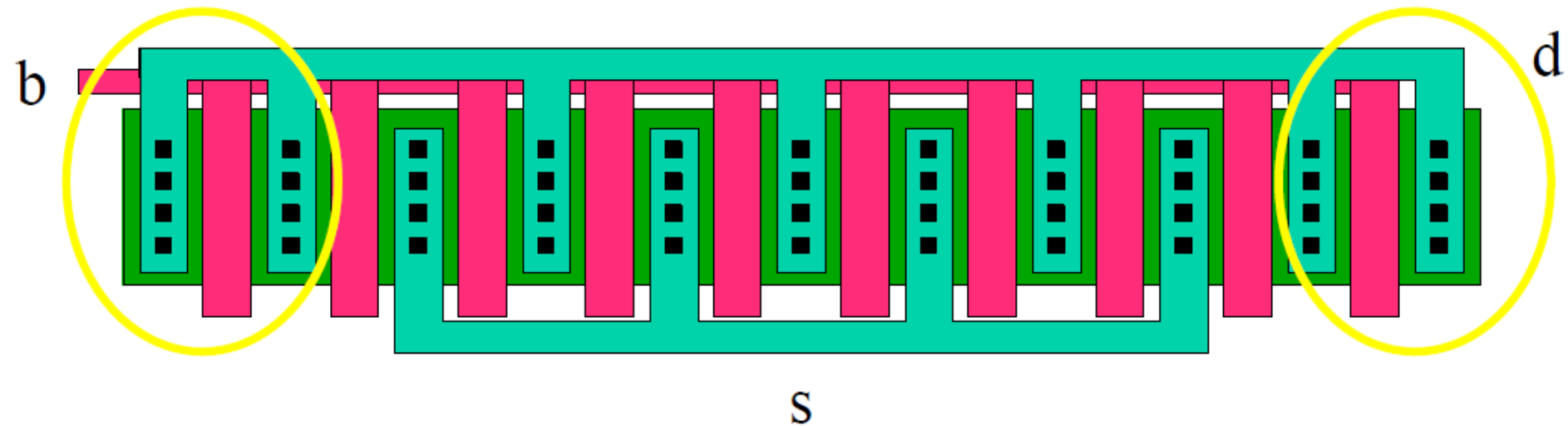
$$M1 \ 1+4+5+8+9 = 27$$

$$M2 \ 2+3+6+7+10 = 28$$



# Dummy Devices at the Ends

- ❖ Ending elements have different boundary conditions than the inner elements -> use dummy



- Dummies are shorted transistors
  - Adds to parasitics

# Interdigital layout

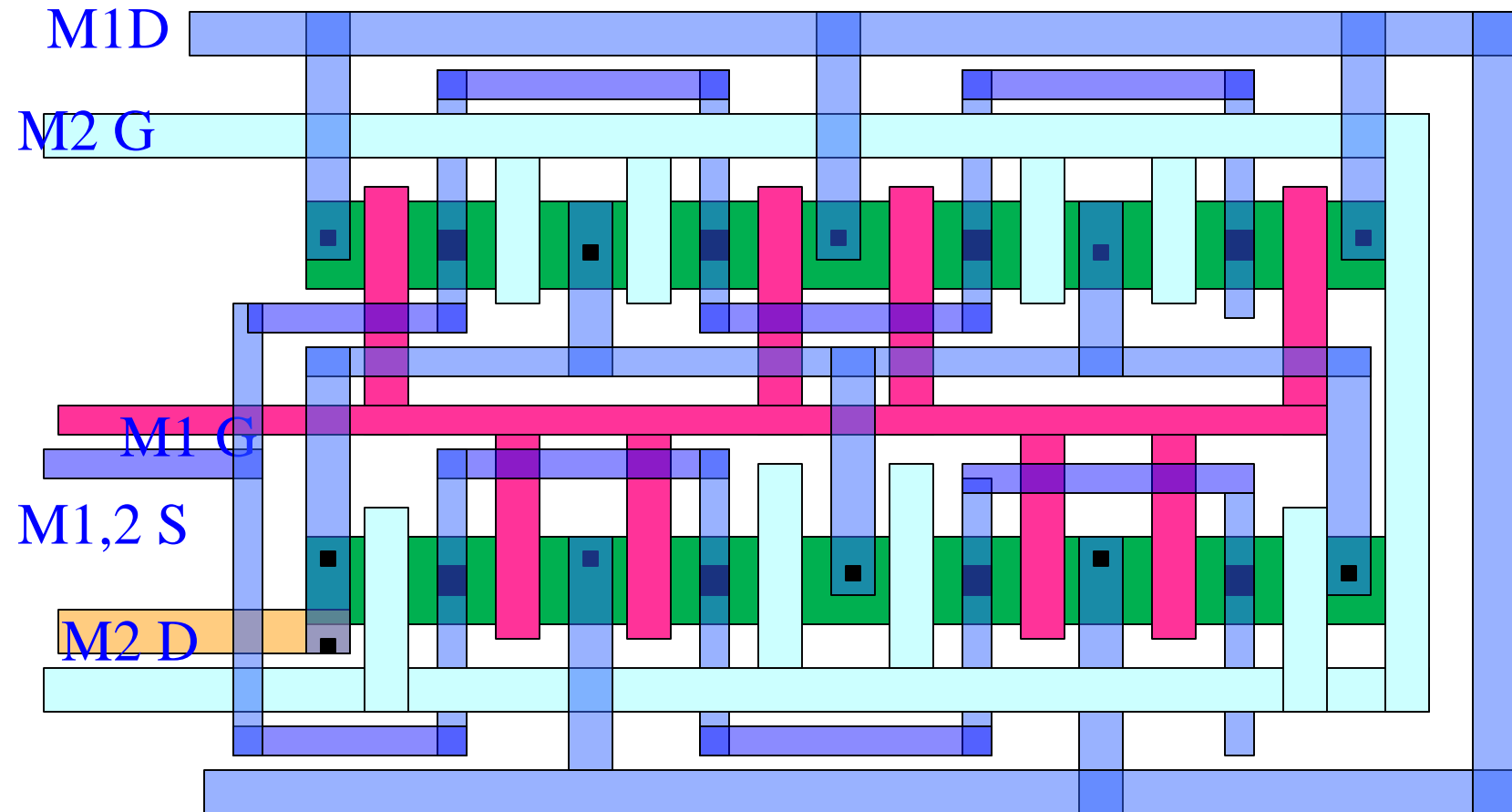
- Split into parallel connections of even parts,
- Half of them will have the drain at the right side and half at the left,
- Be careful how you route the common terminal

M2 M1 M1 M2 M2 M1 M1 M2

M1 M2 M2 M1 M1 M2 M2 M1



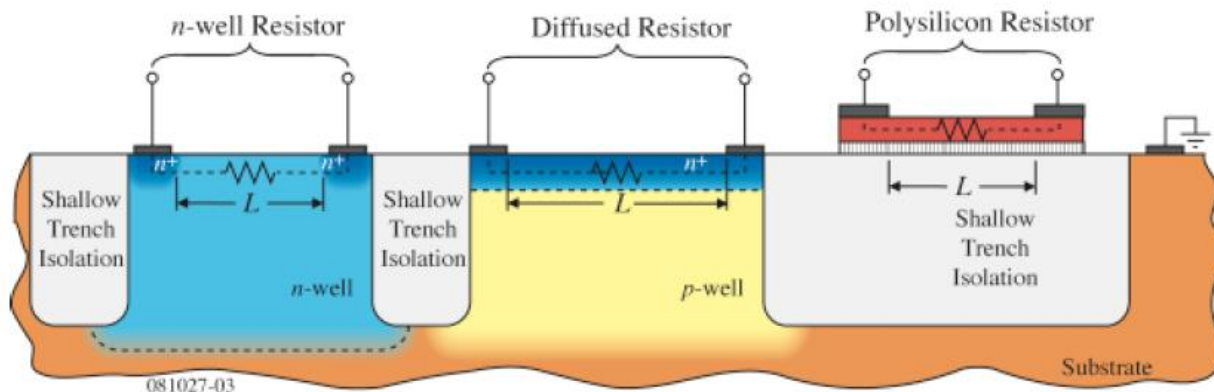
M2 M1 M1 M2 M2 M1 M1 M2  
M1 M2 M2 M1 M1 M2 M2 M1



A	AA	AAA	AAAA
AB*	ABBA	ABBAAB*	ABABBABA
ABC*	ABCCBA	ABCBACBCA*	ABCABCCBACBA
ABCD*	ABCDDCBA	ABCBCADBCDA*	ABCDDCBAABCDDCBA
ABA	ABAABA	ABAABAABA	ABAABAABAABA
ABABA	ABABAABABA	ABABAABABAABABA	ABABAABABAABABAABABA
AABA*	AABAABAA	AABAABAAABA*	AABAABAAAABAABAA
AABAA	AABAAAABAA	AABAAAABAAAABAA	AABAAAABAAAABAAAABAA

# Resistors

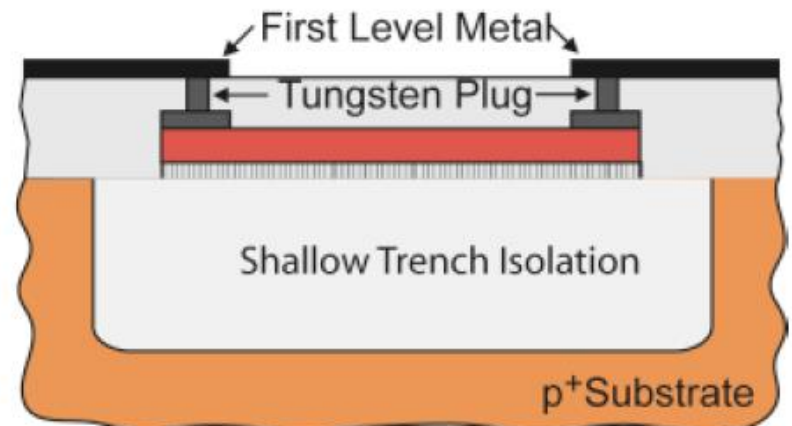
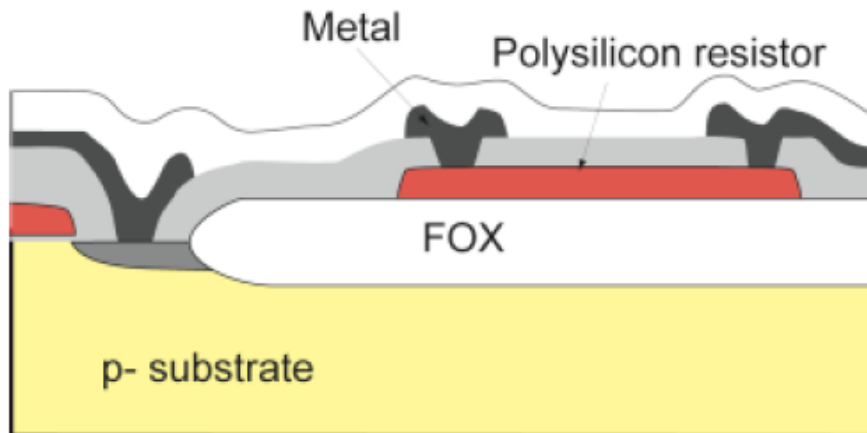
- All materials have a resistivity
- Typical resistivities
  - Metal layer : 0.1 Ohm/square
  - n/p-plus contacts and polysilicon: 10-100 Ohm/square
  - n-well: 1000 Ohm/square
  - low doped poly silicon: 10 k Ohm/square
    - more well defined than n-well, i.e. higher accuracy



# Poly-Resistors

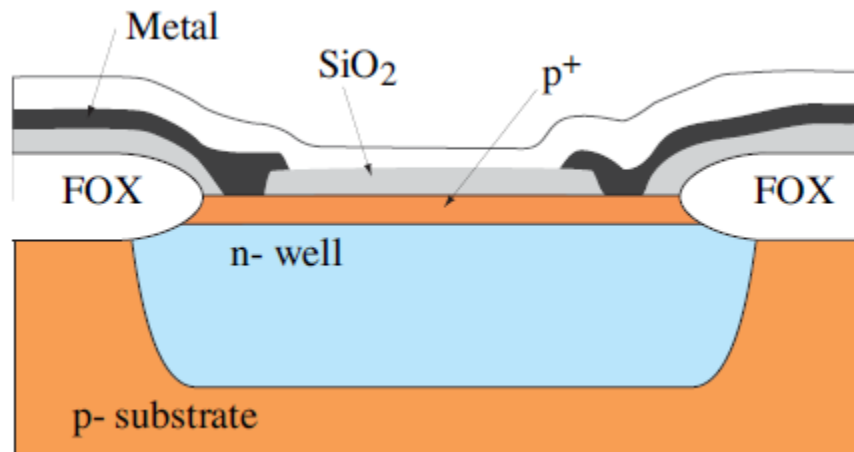
- Poly Resistors

- Silicidated poly resistors: 1 – 10 Ohm/sq.
  - $\approx \pm 30\%$
- Non-silicidated poly resistors: 50-1000 Ohms per sq.
  - $\approx \pm 20\%$
  - Small parasitic capacitances to substrate.
  - Superior linearity.
  - High cost due to the extra mask needed to block silicide layer.



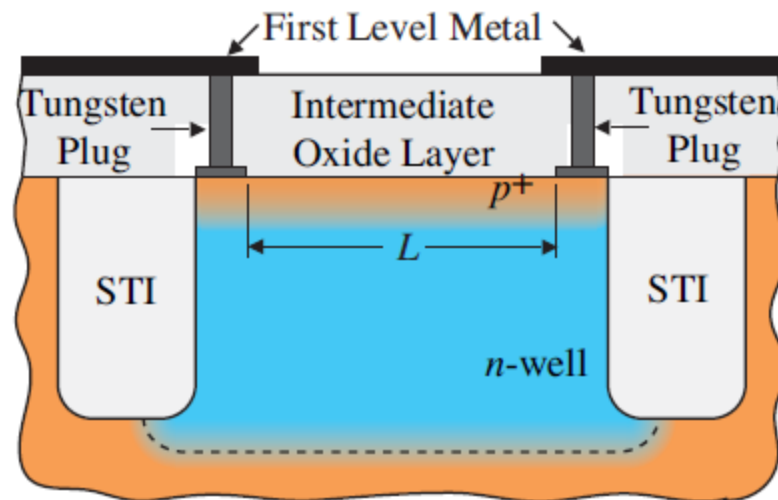
# Diffusion Resistors

- 100-1000 Ohm/sq
  - N-well
    - Large error :  $\approx \pm 40\%$
    - Resistance is strongly terminal voltage-dependent and highly nonlinear.
      - Depletion width varies with terminal voltages. The cross-section area varies with terminal voltages
    - noisy as all disturbances/noise from substrate can be coupled directly onto the resistors
    - Large parasitic capacitance between n-well and substrate.



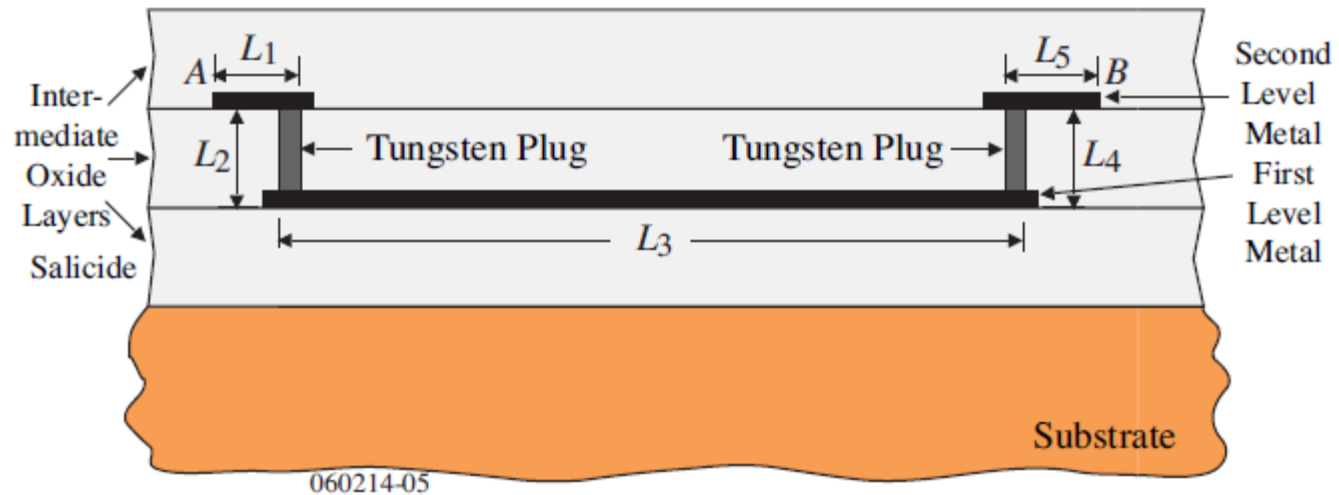
# Ion Implanted

- 500-2000 ohms/square
- Accuracy =  $\pm 15\%$
- Parasitic capacitance to substrate is voltage dependent.
- Piezoresistance effects occur due to chip strain from mounting



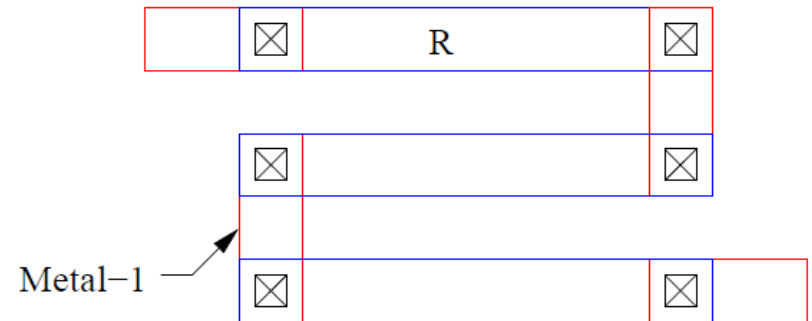
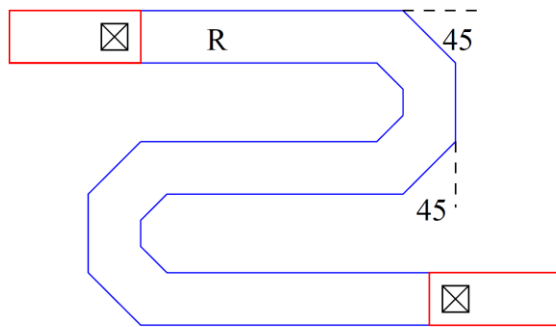
# Metal Resistor

- Low resistance



# Resistor Layout

- Standard Resistors: Avoid 90 degree angle. 45 degree is recommended

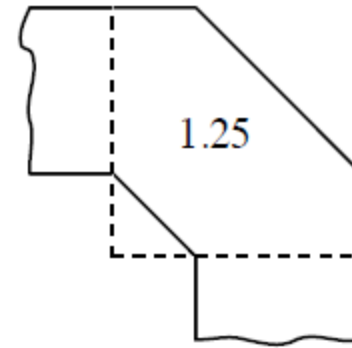
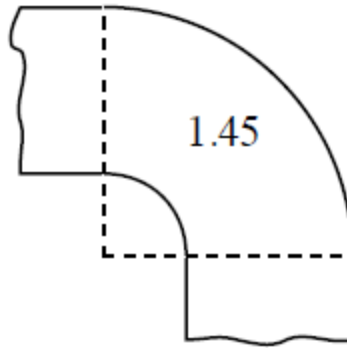
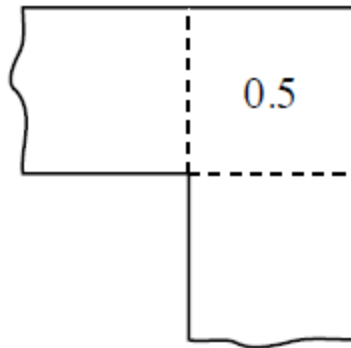


1. Resistance at the corners cannot be estimated accurately
2. Current flow at the corner is not uniform

Recommended resistor layout

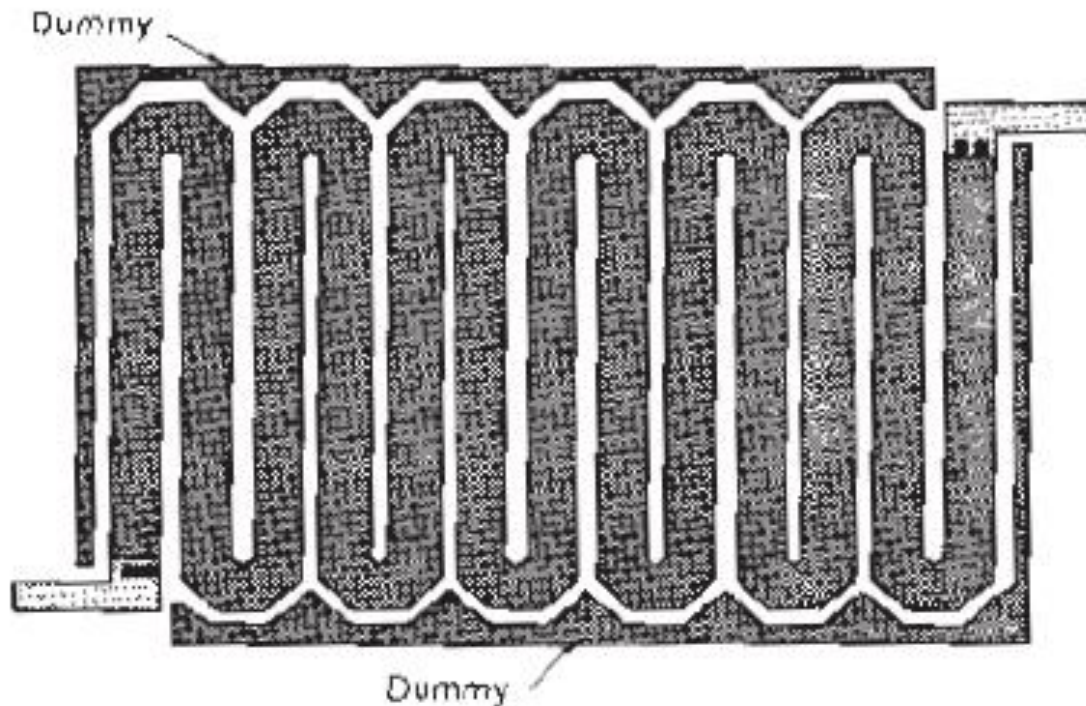


# Corner Correction



# Resistor Layout

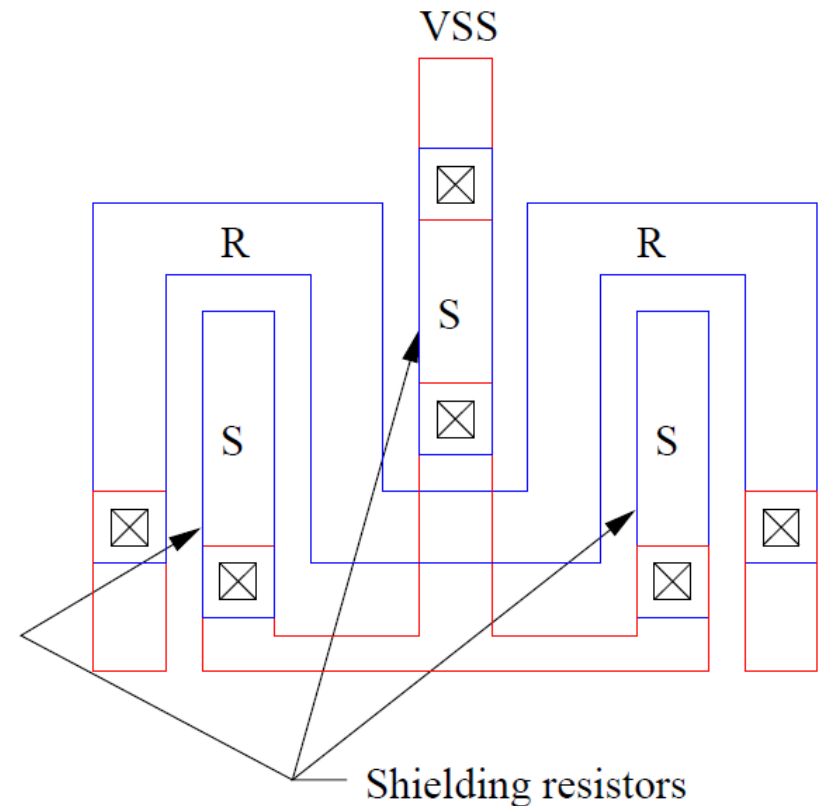
- Dummy resistors are added to minimize the effect of process variation



# Shielded Resistors

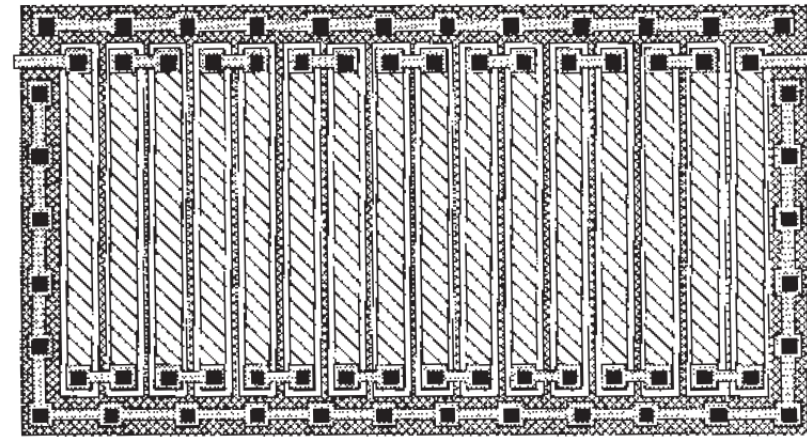
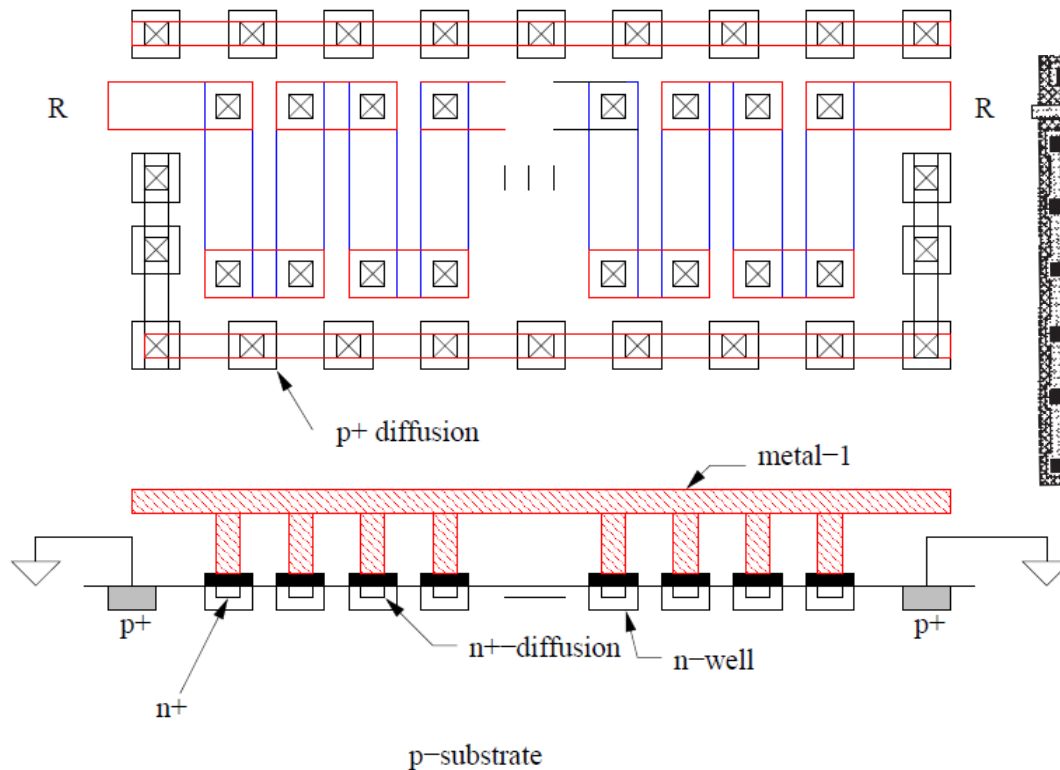
- Shielding resistors
  - Connected to a constant voltage source
  - Prevent self-coupling of the resistor R/inter-coupling with others.
- Widely used in analog/RF design.
- Caution
  - a mutual capacitance between the resistor and its shield exist.

Layout of shielded resistors  
(S = shielding resistors)



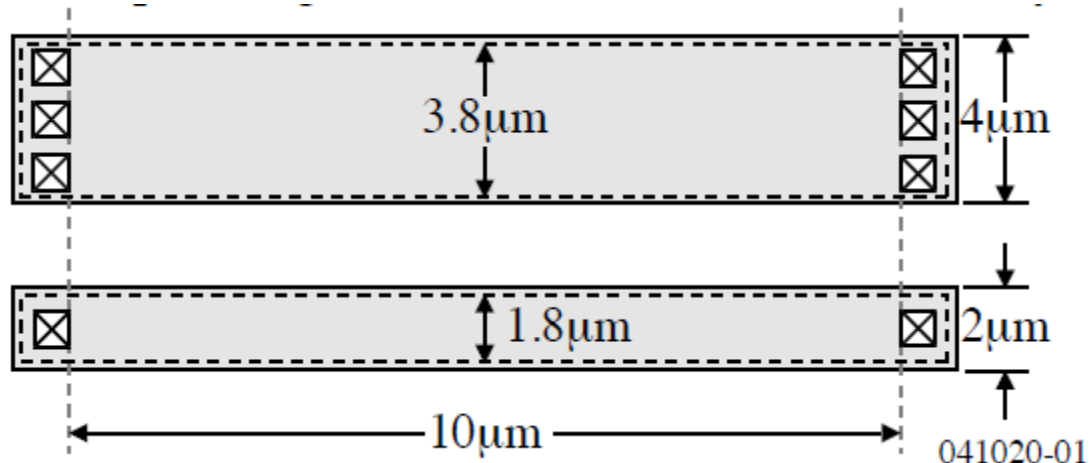
# Layout of Large Resistors

- Use n-well resistors
  - have a large sheet resistance.
- Enclosed by a substrate shielding ring, also known as guard ring, to isolate the resistors from neighboring devices.



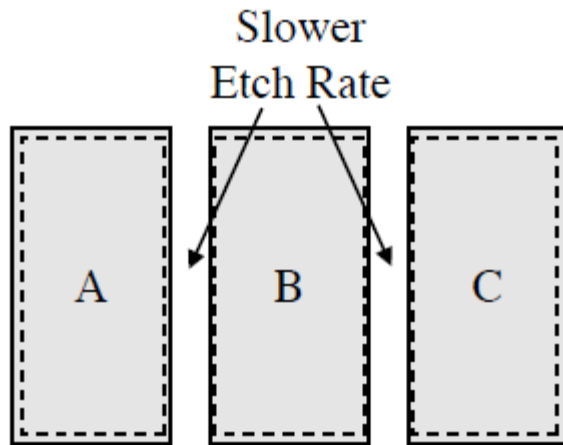
# Process Bias Influence on Resistors

- Process bias is where the dimensions of the fabricated geometries are not the same as the layout data base dimensions.
- Process biases introduce systematic errors.



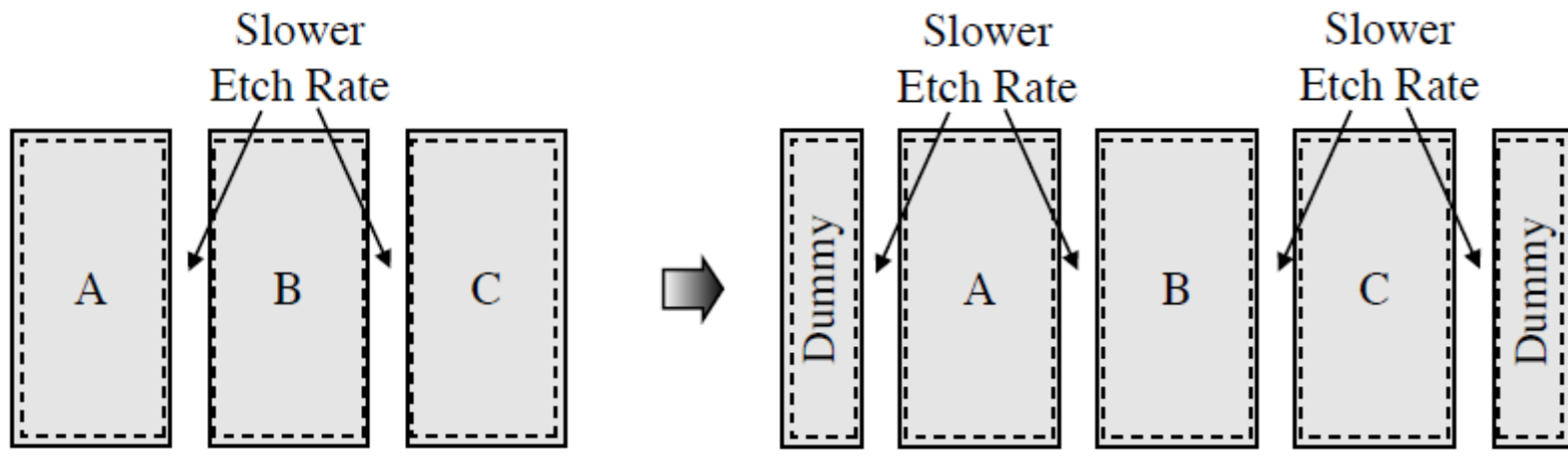
# Etch Rate Variations – Polysilicon Resistors

- The size of the area to be etched determines the etch rate. Smaller areas allow less access to the etchant while larger areas allow more access to the etchant.



# Etch Rate Variations – Polysilicon Resistors

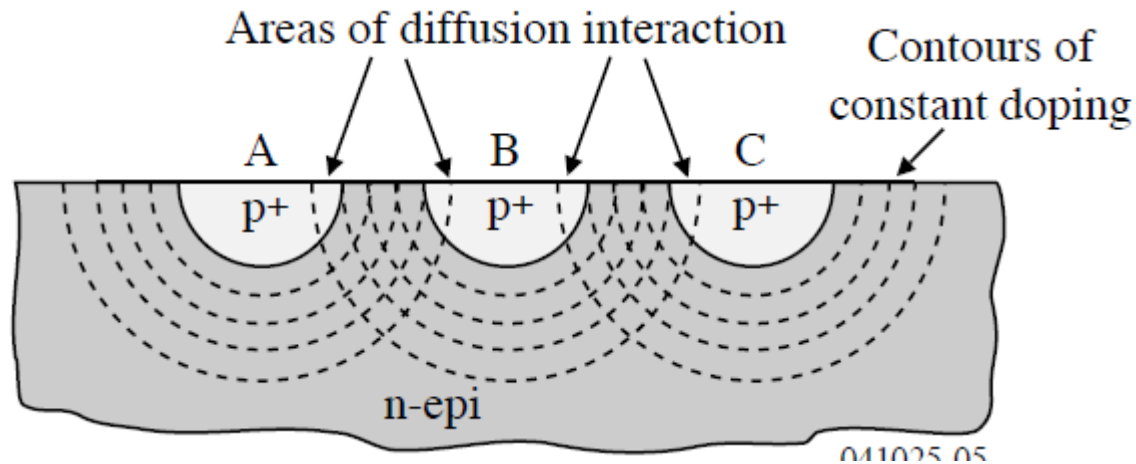
- The size of the area to be etched determines the etch rate. Smaller areas allow less access to the etchant while larger areas allow more access to the etchant.



It may be advisable to connect the dummy strips to ground or some other low impedance node to avoid static electrical charge buildup.

# Diffusion Interaction – Diffused Resistors

- Consider three adjacent  $p+$  diffusions into a  $n$  epitaxial region,

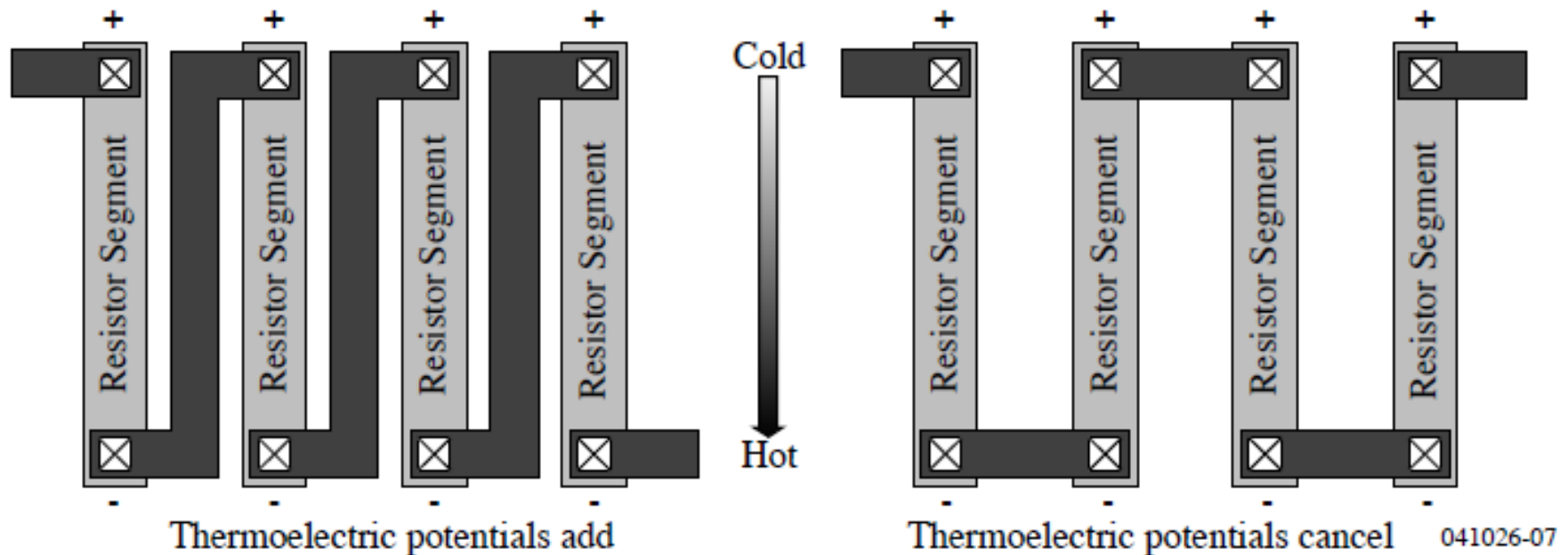


- If A, B, and C are resistors that are to be matched, we see that the effective concentration of B is larger than A or C because of diffusion interaction. This would cause the B resistor to be smaller even though the geometry is identical.
- Solution: Place identical dummy resistors to the left of A and right of C. Connect the dummy resistors to a low impedance to prevent the formation of floating diffusions that might increase the sensitivity to latchup.

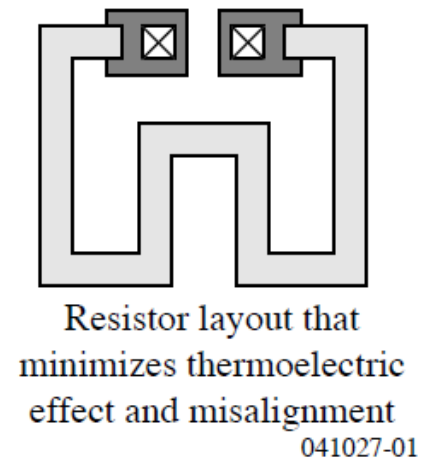
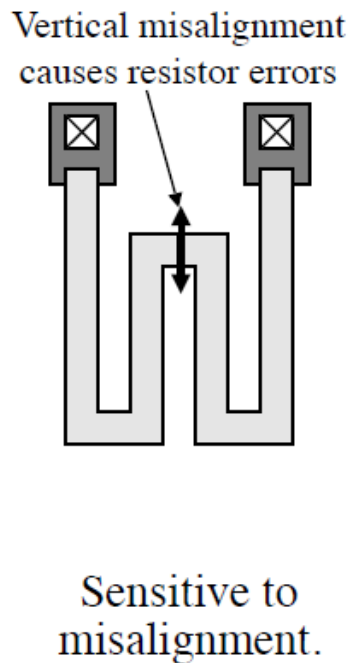
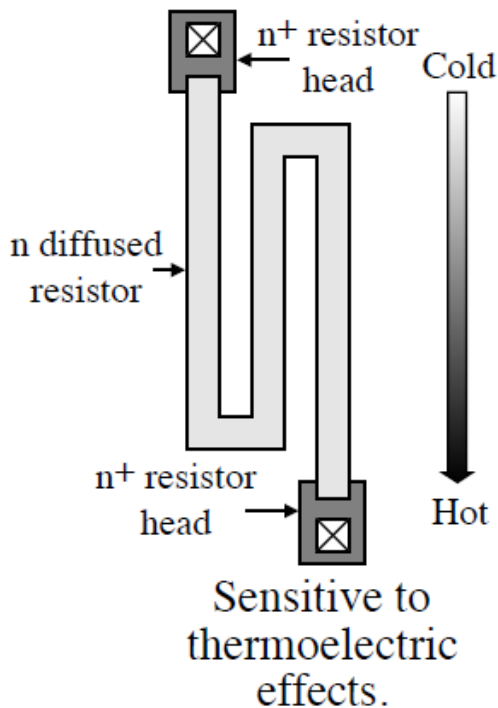


# Thermoelectric Effects

- The thermoelectric effect, also called the Seebeck effect, is a potential difference that is developed between two dissimilar materials that are at different temperatures.
- Two possible resistor layouts with regard to the thermoelectric effect:



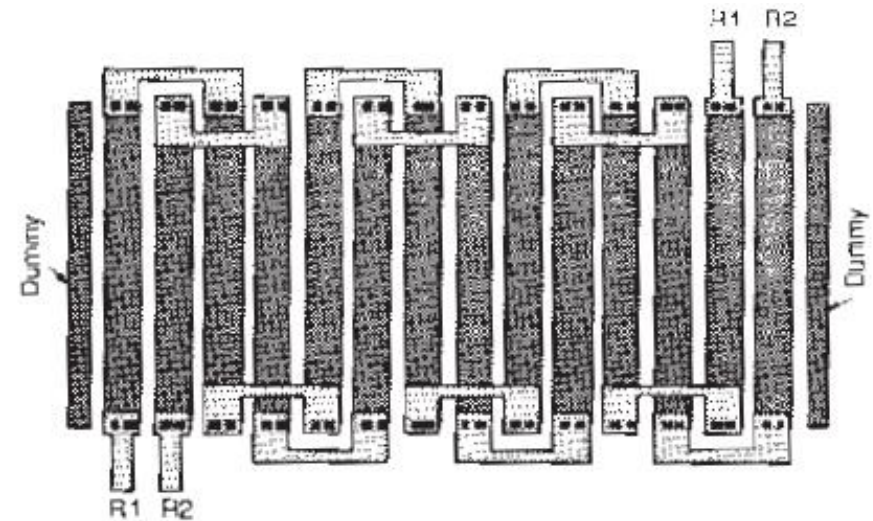
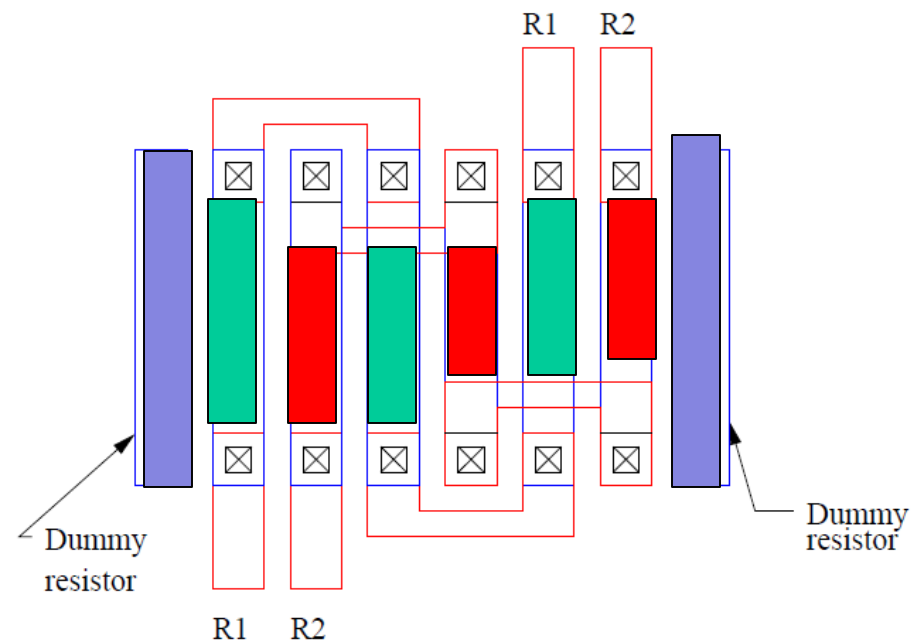
- High sheet resistivity resistors must use p+ or n+ in order to make contacts to metal. Thus, there is plenty of opportunity for the thermoelectric effect to cause problems if care is not taken. Below are three high sheet resistor layouts with differing thermoelectric performance.



041027-01

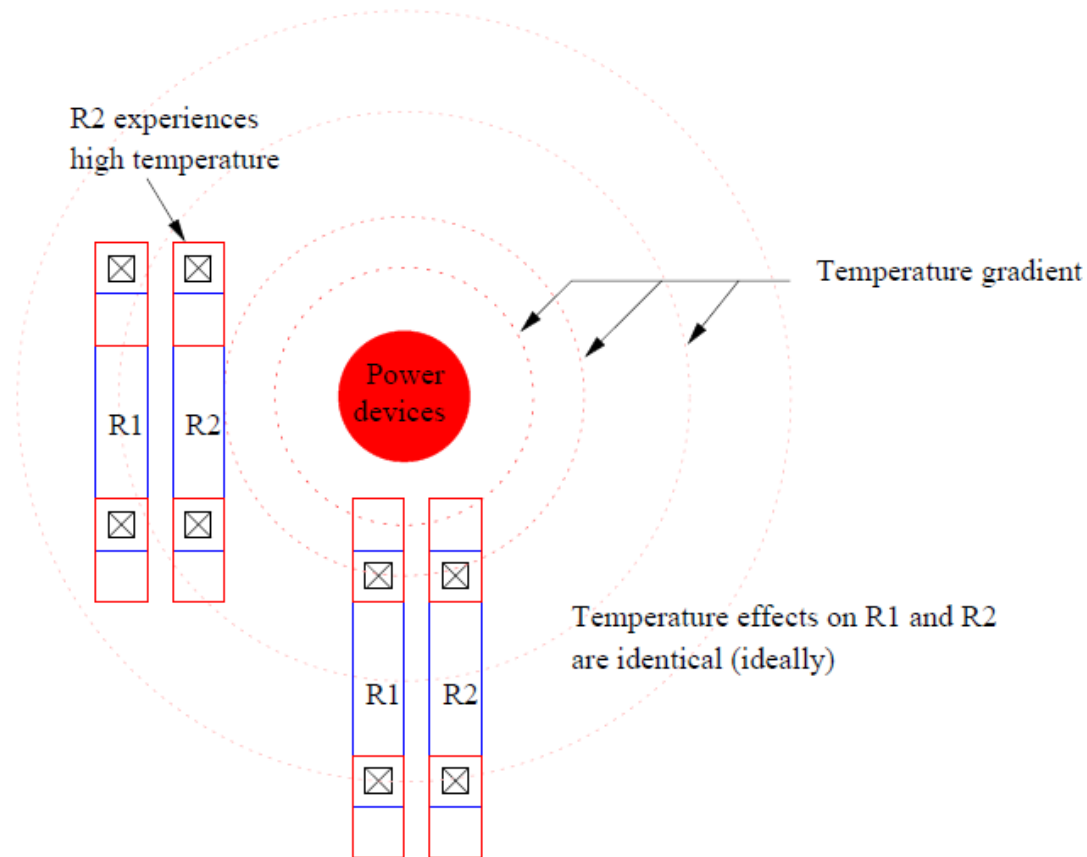
# Layout of Matched Resistors

- Inter-Digitized Layout
  - Minimizes the effect of process variation in x-direction.
- Dummy resistors are added to ensure both resistors have the exactly same environment.



# Matched Resistors with Temperature Consideration

- Keep away from power devices



# Resistor layout guidelines-Matched resistors

---

- Use same material
- Identical geometry, same orientation
- Close proximity, interdigitate arrayed resistors
- Use dummy elements
- Place resistors in Low stress area
- Place resistors away from power devices
- Use electrostatic shielding

# Capacitors

- There are naturally capacitors between each layer of metal, polysilicon or silicon
- Dielectrics between different metal layers have a thickness of 0.5-1 micron, which gives a rather large area for a given capacitance.
- Key Parameters
  - Capacitance per unit area
    - Larger specific capacitance (capacitance per unit area) gives smaller area
  - Linearity
  - Parasitic capacitance to substrate
  - Series resistance - resistance of capacitor plates

$$C = \epsilon \frac{A}{t}$$

# Types of IC Capacitors

- Poly-diffusion capacitors
  - .6-.8 fF/ $\mu\text{m}^2$  ( $\approx\pm 5\%$ ).
  - Matching 0.2%
  - Nonlinear bottom-plate parasitic capacitance.  $\approx 20\%$  of inter-plate capacitance.
- MOS capacitors
  - 0.6 - 0.8 fF/ $\mu\text{m}^2$ ; ( $\approx\pm 5\%$ ).
  - Matching 0.5%
  - Stable capacitance in strong inversion
  - Non-negligible channel resistance lowers the quality factor (Q) of the capacitor
- Poly-poly capacitors
  - 0.3 - 0.5 fF/ $\mu\text{m}^2$ ; ( $\approx\pm 10\%$ ). Matching 0.5%
  - Not available in standard CMOS processes
- Metal-poly capacitors
  - 0.03-0.05 fF/ $\mu\text{m}^2$ . ( $\approx\pm 25\%$ ). Matching 0.5%
  - Capacitance is small, area consuming.
- Metal-metal capacitors
  - 0.02-0.04 fF/ $\mu\text{m}^2$ ; ( $\approx\pm 25\%$ ). Matching 0.1%
  - Capacitance is small, area consuming

# Pn junction capacitor

- Generally made by diffusion into the well
- Layout: Minimize the distance between the p+ and n+ diffusions.

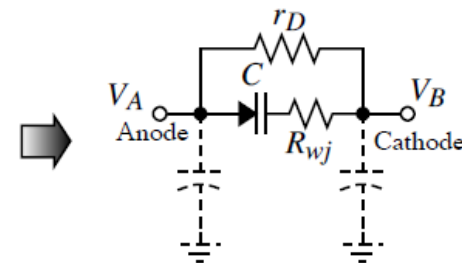
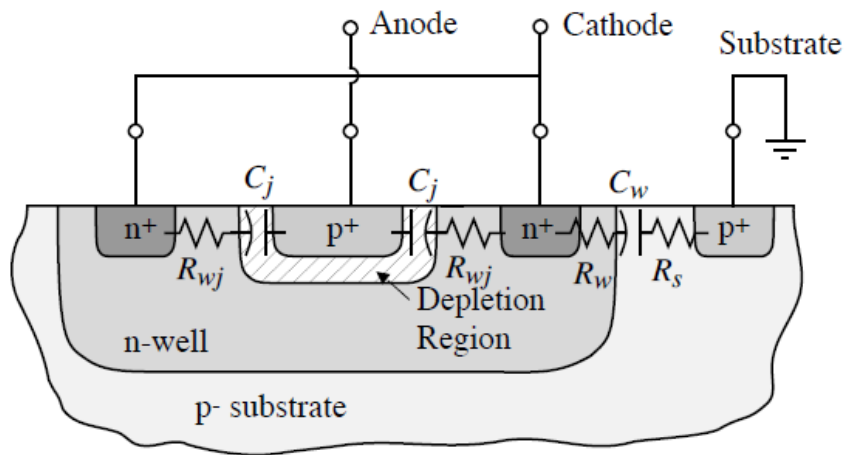
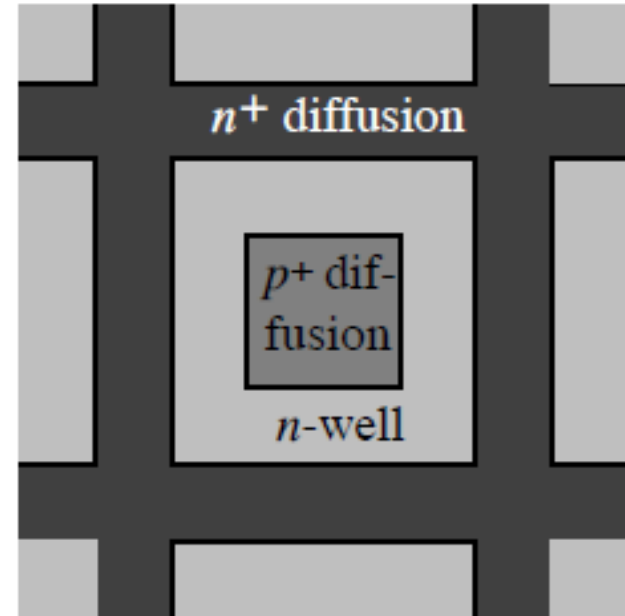
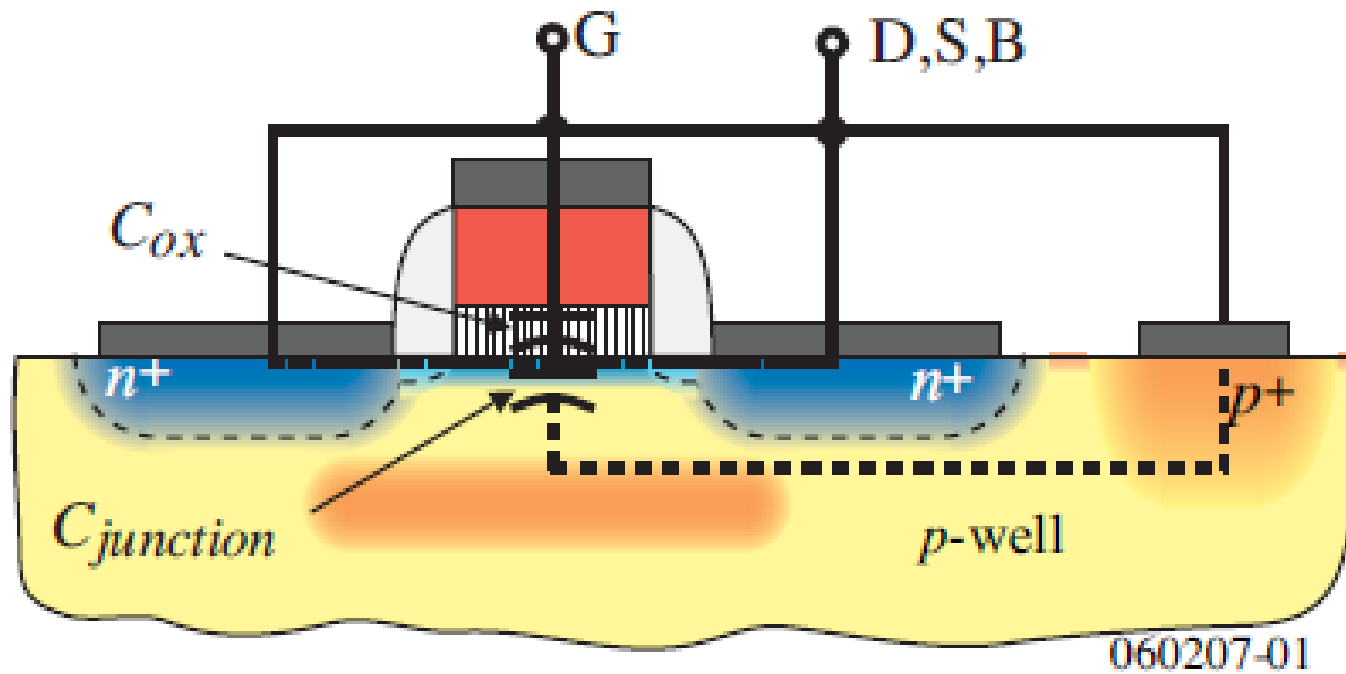


Fig. 2.5-011

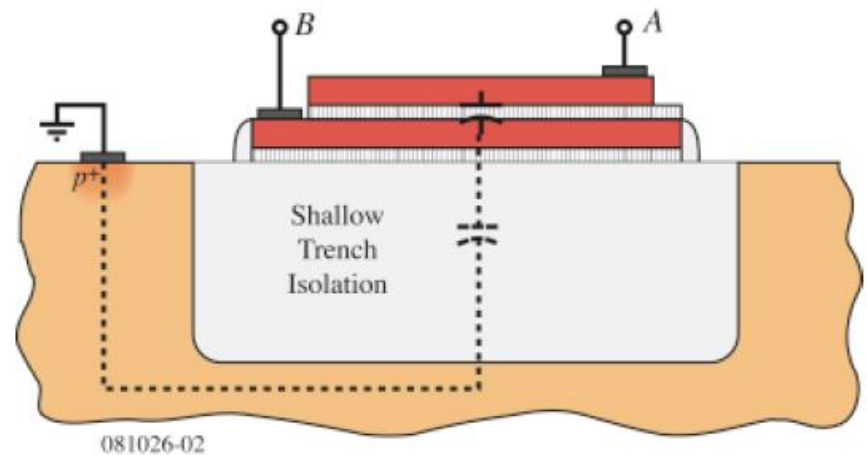
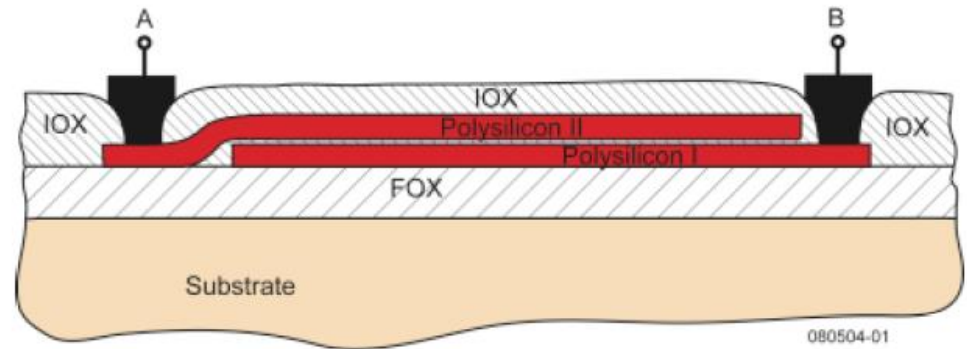


# MOS Gate Capacitor



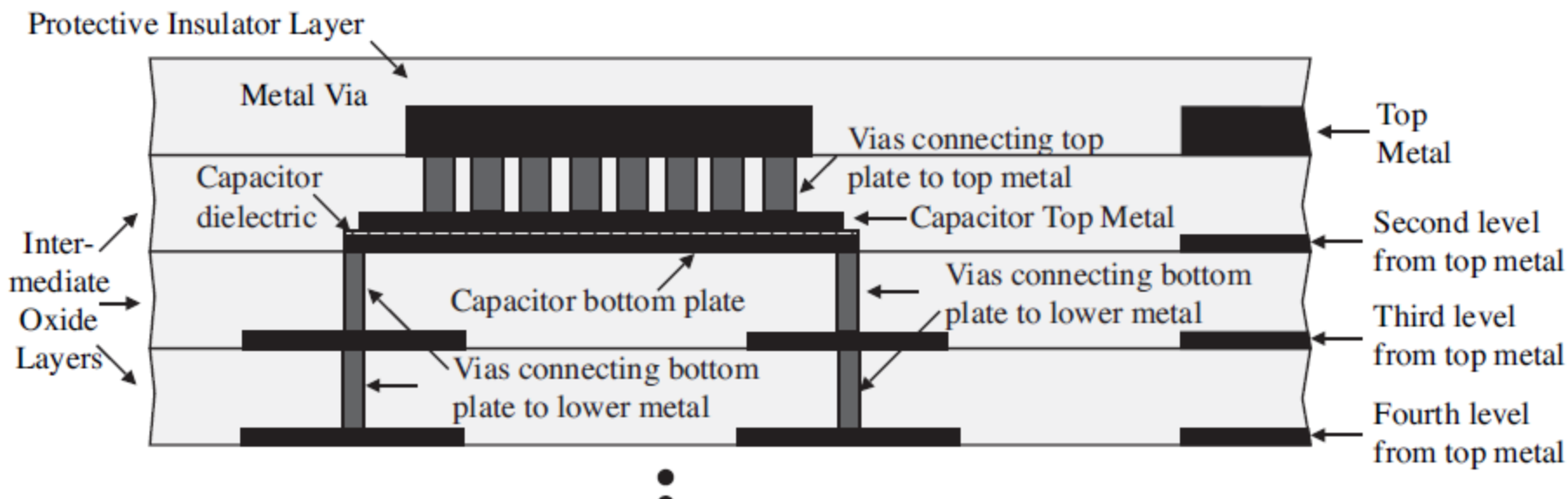
# Poly Poly Capacitors

- Highly stable capacitors
- small bottom plate parasitic



# Metal-Insulator-Metal (MiM) Capacitors

- In some processes, there is a thin dielectric between a metal layer and a special metal layer called “capacitor top metal”. Typically the capacitance is around  $1\text{ fF}/\mu\text{m}^2$  and is at the level below top metal.
- Good matching is possible with low parasitics



# Capacitor Errors

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- **Edge Effects**
- There will always be a randomness on the definition of the edge. However, etching can be influenced by the presence of adjacent structures.

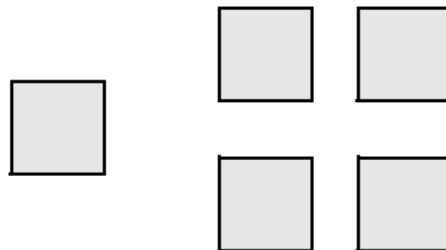
# NON-IDEAL EFFECTS- UNDER-CUT

- Non-uniform undercut &/or edge fringing field effects change the value of designed capacitors.
- The area and perimeter ratio is preserved if we use layout utilizing unit capacitors.

Case 1



Case 2

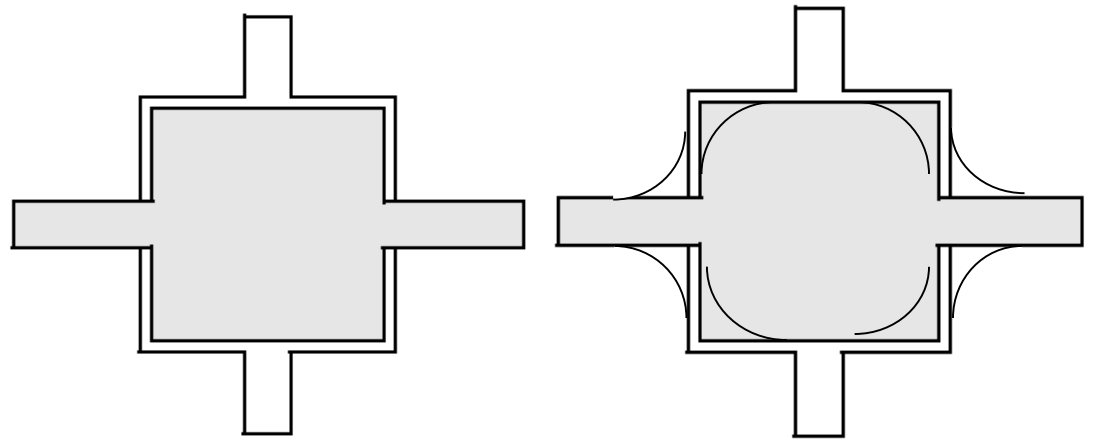
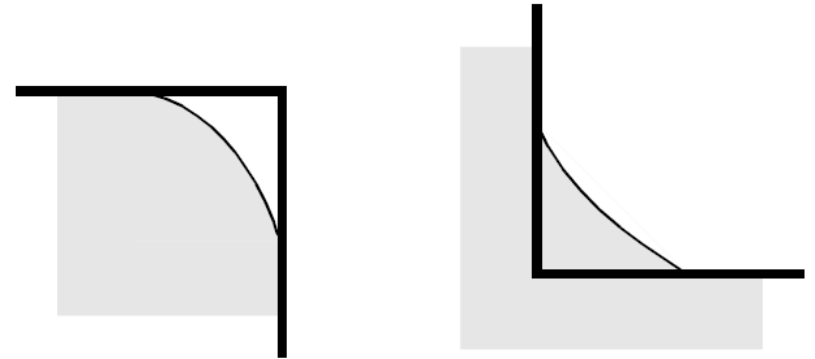


## Ideal case: no undercut

	Case 1	Case 2
Area	1:4	1:4
Perimeter	1:2	1:4
Typical case: 0.05 undercut		
	Case 1	Case 2
Area	1:4.46	1:4
Perimeter	1:2.1	1:4

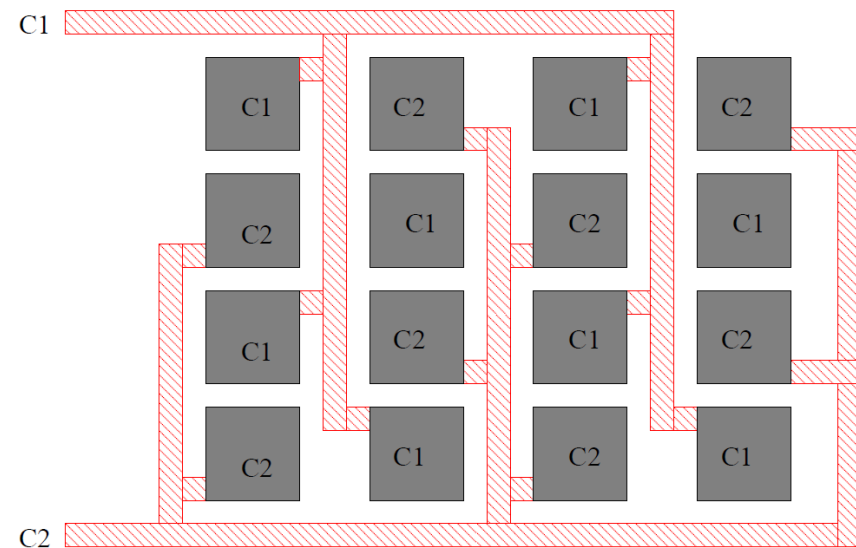
# NON-IDEAL EFFECTS-Corner Rounding

- Etching always causes corner rounding to some extent.
- This means that
  - $90^\circ$  corners will be eroded and
  - $270^\circ$  corners will be have incomplete removal of material
- In order to overcome this effect use an equal number of  $90^\circ$  &  $270^\circ$  corners



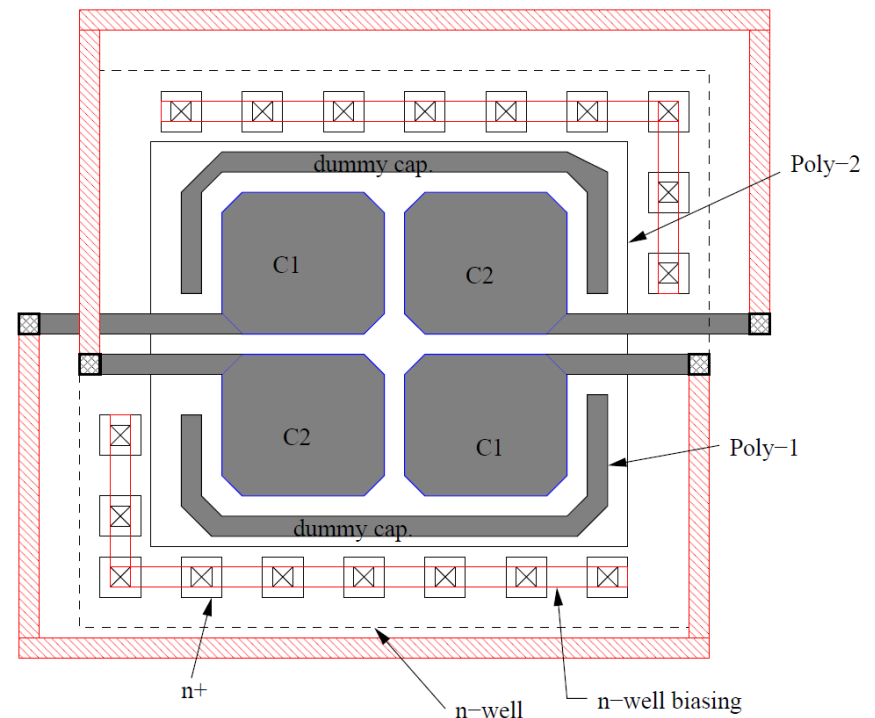
# Layout of Matched Capacitors

- **Oxide Gradients:** Error due to a variation in dielectric thickness across the wafer.
- Minimize the Effect of Oxide Thickness in both x and y-directions.
  - Common Centroid Structure.
- Dummy capacitors are needed to ensure the same environment for C1 and C2.

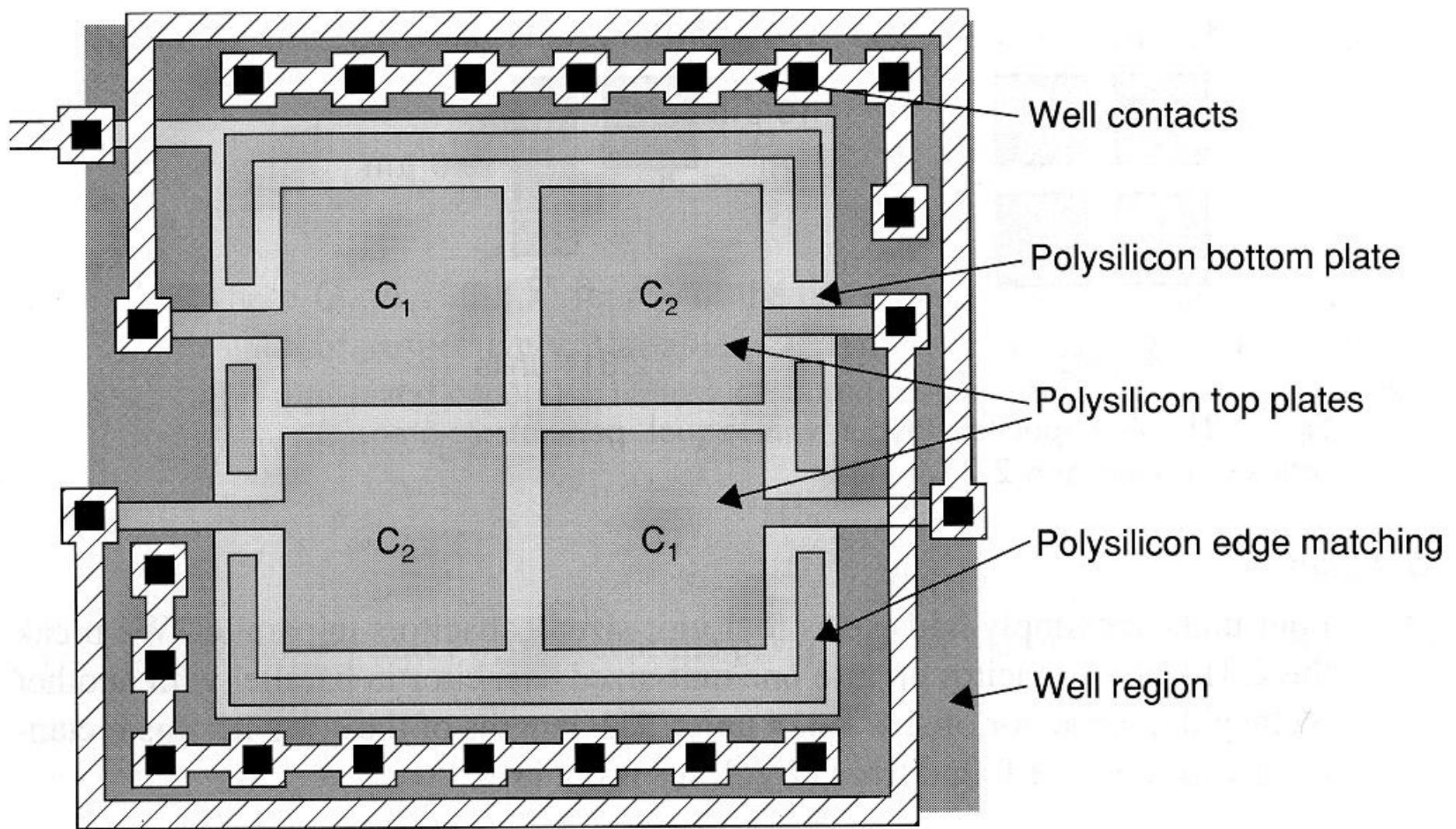


# Layout of Matched Capacitors

- C1 and C2 are 2-poly capacitors.
- n-well is employed as a charge collector to shield the interaction between the bottom plate and substrate.
- n-well is biased at multiple points and connected to a constant voltage source.



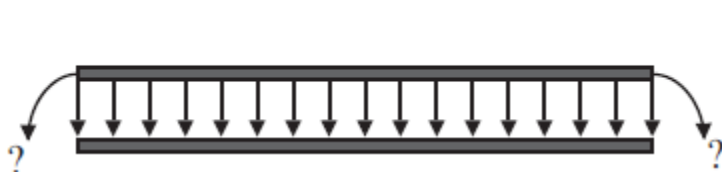




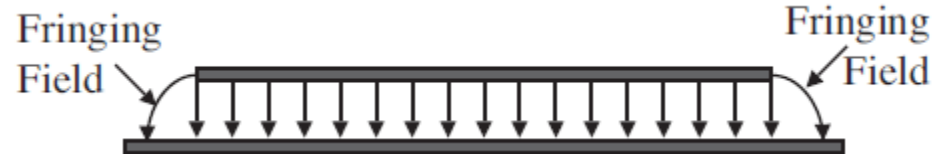
**Are there any thing else you can improve?**

**Is there full symmetry between  $C_1$  and  $C_2$ ?**

# Decreasing Sensitivity to Edge Variation

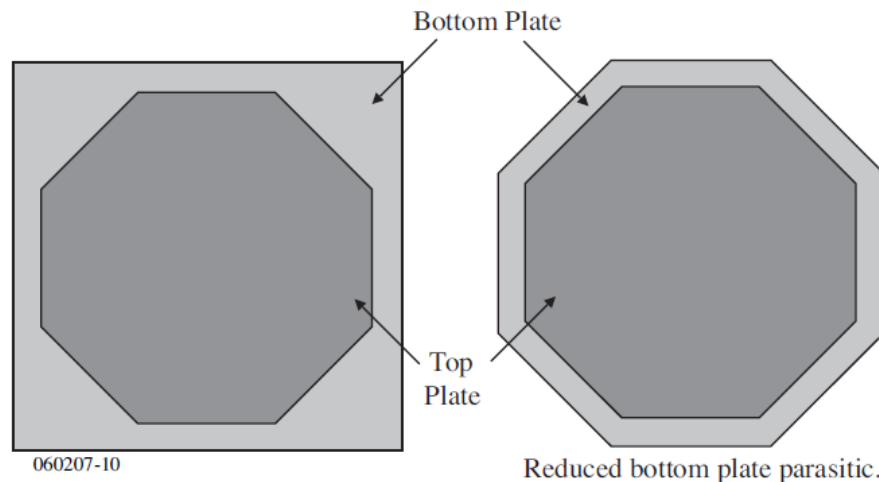


Sensitive to alignment errors in the upper and lower plates and loss of capacitance flux (smaller capacitance).



Insensitive to alignment errors and the flux reaching the bottom plate is larger resulting in large capacitance.

A structure that minimizes the ratio of perimeter to area (circle is best).



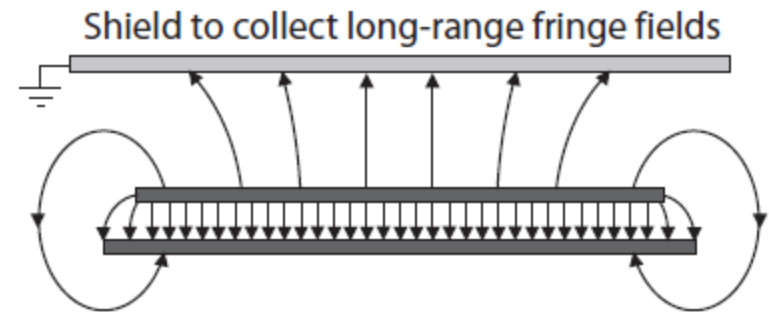
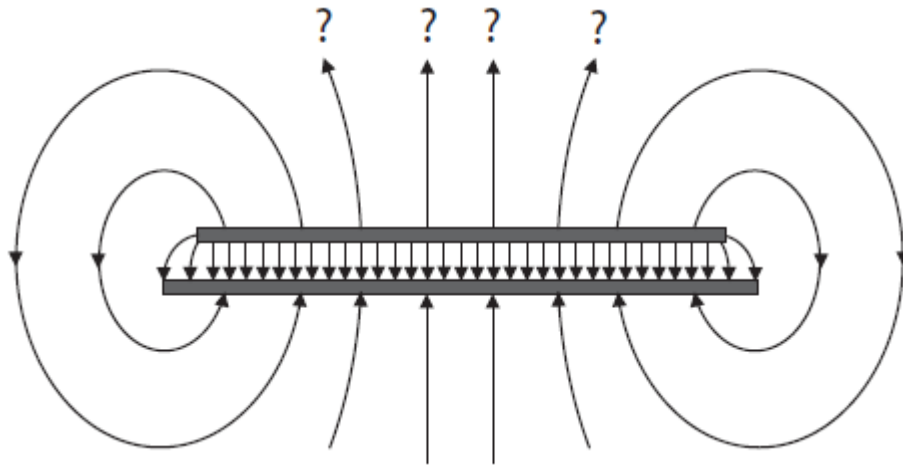
# Accurate Matching of Capacitors

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- Accurate matching of capacitors depends on the following influence:
  - Mismatched perimeter ratios
  - Proximity effects in unit capacitor photolithography
  - Mismatched long-range fringe capacitance
  - Mismatched interconnect capacitance
  - Parasitic interconnect capacitance

# Long-range fringe capacitance

- Long-range fringe capacitance



# References

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- A. Hastings, The Art of Analog Layout, Prentice-Hall, 2002.
- B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2001.

# Summary

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- Use large area to reduce random error
- Common Centroid layout to reduce linear gradient errors
- Use unit element arrays
- Interdigitize for matching
- Use of symmetry (photolithographic invariance)
- Dummy device for similar vicinity
- Guard rings for isolation

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**Thank You**