PCB design guidelines for Gbit-Ethernet interface

32-bit TriCore™ AURIX™ TC3xx microcontroller

About this document

Scope and purpose

The TC33x, TC35x, TC36x, TC37x, TC38x, and TC39xED are part of the AURIX™ TC3xx family of 32-bit microcontroller products. They are available in different packages and might require a PCB carefully designed for electromagnetic compatibility.

This document provides product-specific PCB design recommendations and guidelines for the Ethernet Interface (MAC – PHY) of the AURIX™ TC3xx, and should be read in conjunction with the Infineon PCB Design Guidelines for Microcontrollers (AP24026), AP32334 and AP32335, which give general design rule information for PCB design.

Attention: ***This document contains design recommendations from Infineon Technologies point of view. Effectiveness and performance of the final application implementation must be validated by the customer, based on their specific implementation choices.***

Intended audience

This document is intended for anyone who designs with the AURIX™ TC3xx microcontroller and needs design recommendations regarding to the EMC optimized PCB design.

Please read the sections "Important notice" and "Warnings" at the end of this document

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1   Supply domains

The microcontroller has the following supply domains which should be individually de-coupled:

- VDD = 1.25 V for Core
- VDDP3 = 3.3 V for Flash supply
- VFLEX, VFLEX2 = 3.3 V for Ethernet Port supply
- VEXT = 5 V for default GPIO supply
- VDDM = 3.3 V, or 5 V for ADC

The power supply feeding from the regulator outputs to each domain can be made on a supply layer (POWER).

The supply pin of the Gbit-Ethernet Module is pin VFLEX (D5 or J10).

1.1   Pinouts with one Gbit Ethernet interface

Figure 1   **BGA-516 and BGA-292 ballout**

1 Supply domains

1.2   Pinout with two Gbit Ethernet interfaces

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y
20	VSS_EXT	P15_0	P20_14	P20_13	P20_11	P20_8	P20_3	P20_0	P21_5	P21_4	VSS_OSC	XTAL1	VEXT_OSC	P22.10 TXD0	P22_2 COL	P23.4 TXD1	P23.3 TXD2	P23.2 TXD3	VEXT	VSS_EXT
19	VDDP3	VSS_EXT	P15_2	P20_12	P20_10	P20_7	P20_1	P20_2	P21_3	P21_2	TRST	XTAL2	VDD_OSC	P22.11 TCTL	P22_3	P22.12 TXCLK	P23_1	VFLEX2	VSS_EXT	P32_3
18	P15_1	VDDP3																	P32_4	P32_2
17	P15_4	P15_3		VSS_EXT	P20_9	P20_6	PORST	P21_6	P21_1	P21_0 PPS	P22.1 RXERR	P22.9 MDIO	P22.7 GREFCLK	P22.5 RXCLK	P23.6 RXD2	P23.5 RXD3	VSS_EXT		P32_1/ VG1P	P32_0/ VG1N
16	P15_6	P14_0		VDD	VSS_EXT	ESR0_N	ESR1_N	P21_7	TCK	TMS	P22.0 CRS	P22.8 MDC	P22.6 RCTL	P22.4 RXD0	P23.7 RXD1	VSS_EXT	P32_7		P33_12	P33_13
15	P14_1	P14_4		P15_7	VDD											P32_5	P32_6		P33_10	P33_11
14	P14_5	P14_3		P15_8	P15_5		VDD	VSS	NC4		VSS	VSS	VDD			P33_14	P33_15		P33_8	P33_9
13	P14_8	P14_6		P14_7	P14_2	VDD		VSS	VSS		VSS	VSS		VDD		P34_4	P34_5		P33_6	P33_7
12	P13_1	P13_0		P14_9	P12_0		VSS	VSS		VSS	VSS		VSS	VSS		P34_2	P34_3		P33_4	P33_5
11	P13_3	P13_2		P14_10	P12_1		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS		VEVRS B	P34_1		P33_2	P33_3
10	P11_2	P11_3		P11_4	P11_0		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS		AN0	AN1		P33_0	P33_1
9	P11_9	P11_10		P11_6	P11_1		VSS	VSS		VSS	VSS		VSS	VSS		AN4	AN3		AN2	AN5
8	P11_11	P11_12		P11_5	P11_7	VDD		VSS	VSS	VSS	VSS		VDD			AN6	AN7		AN8	AN10
7	P10_0	P10_1		P11_14	P11_8		VDD	VSS	VSS	VSS	VSS		VDD			AN12	AN9		AN11	VAGND 1
6	P10_3	P10_4		P11_15	P11_13											AN15	AN14		AN13	VAREF 1
5	P10_2	P10_5		VFLEX	VSS_EXT	P2_10	P1_3	P1_5	P1_7	P0_10	AN42	AN40	AN38	AN34	AN23	AN22	AN17		AN16	VDDM
4	P10_6	P10_8		VSS_EXT	P2_9	P2_11	P1_4	P1_6	P0_6	P0_8	AN43	AN41	AN36	AN32	AN31	AN30	NC3		AN18	VSSM
3	P10_7	VEXT																	AN19	AN20
2	VEXT	VSS_EXT	P2_1	P2_3	P2_5	P2_7	P0_1	P0_3	P0_5	P0_9	P0_12	AN47	AN45	AN37	AN35	VAGND 2	AN28	AN26	AN24	AN21
1	NC1	P2_0	P2_2	P2_4	P2_6	P2_8	P0_0	P0_2	P0_4	P0_7	P0_11	AN46	AN44	AN39	AN33	VAREF 2	AN29	AN27	AN25	NC2

Figure 2   BGA-292 ballout (only for TC377-TA)

2 PCB design

This chapter introduces some ground rules for EMC-friendly PCB layout for the Gbit-Ethernet interface.

Note: *More information is provided in the Infineon PCB Design Guidelines for Microcontrollers (AP24026), AP32334 and AP32335. These documents are recommended as an additional information source.*

2.1 Selection of stack-up

Selection of the correct stack-up for a high-speed board should be made at the beginning of the board design because the selection can have an effect on the routing and impedance control of the traces. Impedance control of the traces is one of the main parameters of the high-speed design.

The following issues must be considered:

- It should be guaranteed that high-speed lines have a solid GND reference without interruption of the impedance continuity.
- Signal lines must have minimum distance to reference the plane layer also in conjunction with controlled impedance.
- Ensure, as much as possible, a plane capacitance for the supply domains.
- Avoid vias or layer change on high-speed signals.

Since the discrete board de-coupling capacitors can only be effective up to 200 MHz, the plane de-coupling should be used where possible.

The stack-up should be selected so that you can build a power plane capacitance and have the benefit of the high frequency de-coupling effect which could be effective above 200 MHz. Figure 3 shows sample stack-up for six, and eight layer PCB.
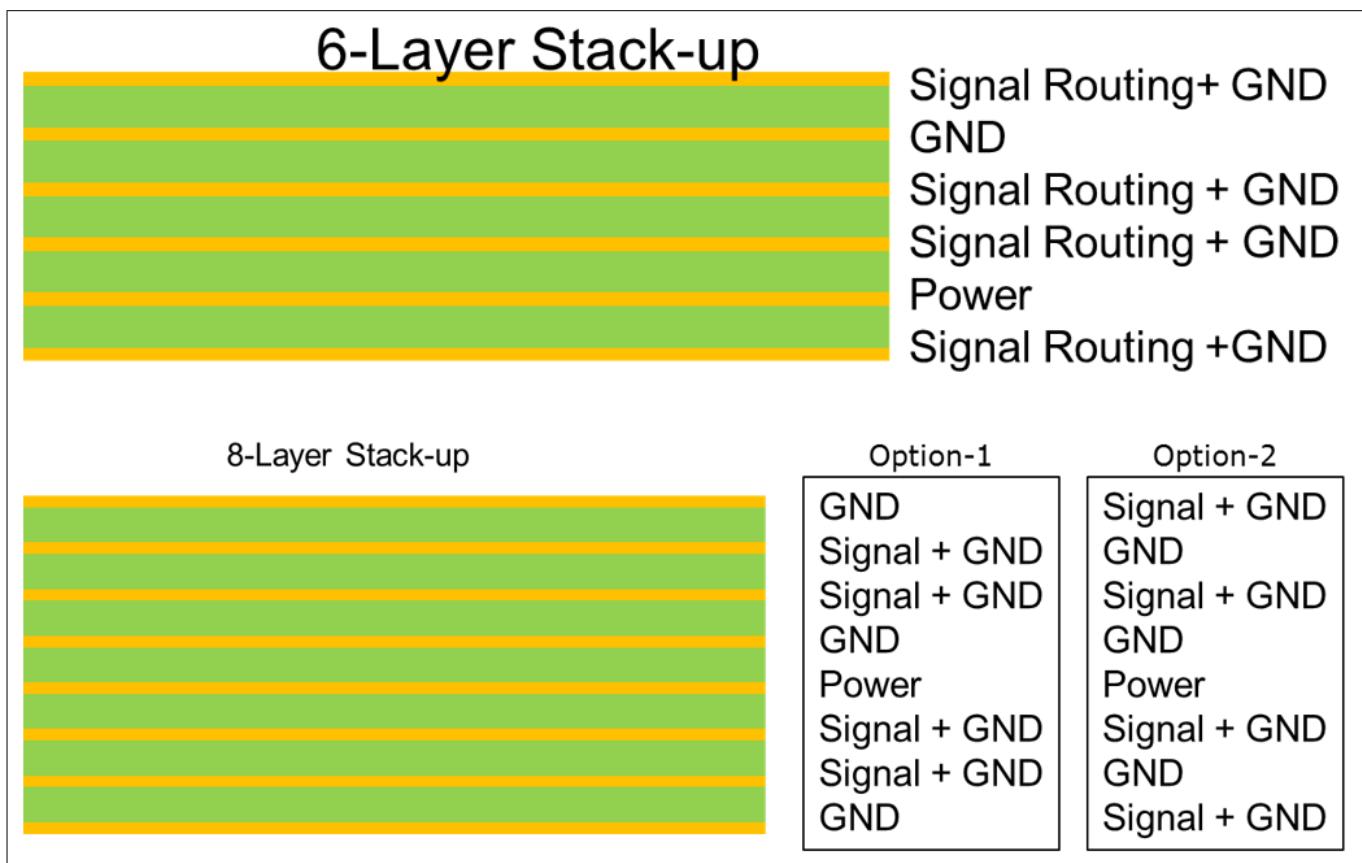
Figure 3   **Sample stack-up of 6 and 8-layer boards**

## 2.2 Impedance controlled design of traces

Design of traces for high-speed signals is critical. They should be designed to have a trace impedance of typically 50-60 Ohm.

There are two types of transmission lines for trace implementation:

- Microstrip
- Stripline

It is recommended to design GBit-Ethernet interface lines as stripline with controlled impedance of 50-60 Ohm. In special cases these impedance values can excide that recommendation. In this case simulations shell be done.

Striplines
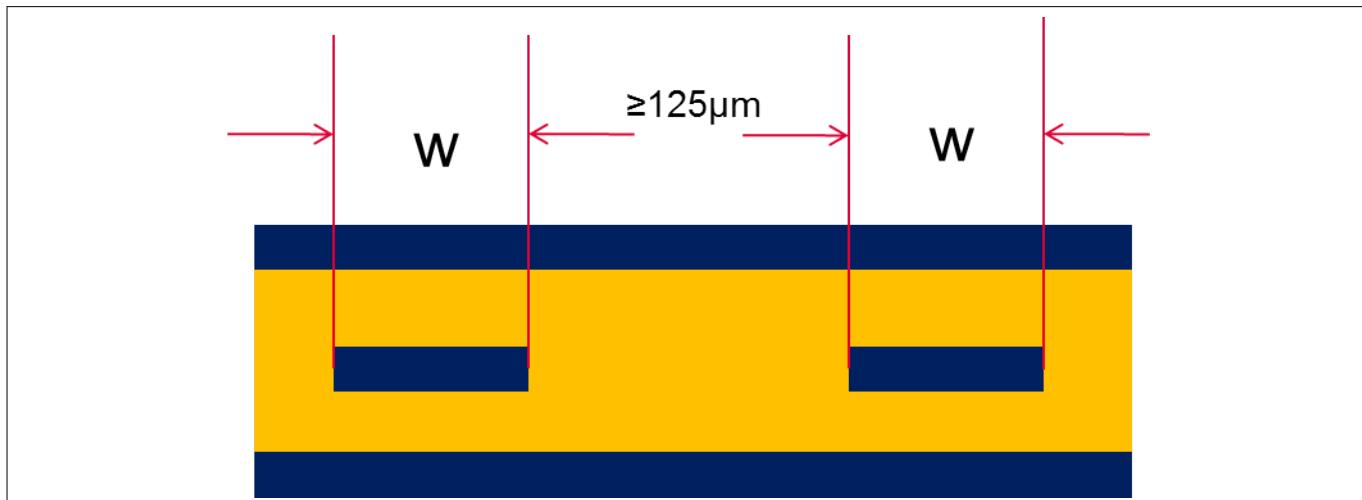
Figure 4   **Stripline transmission line**

The following points are design references:

- It is recommended to have a distance of two times the trace width between single-ended traces.
- Transmit and receive lines group should also be separated with a distance of >2 mm if possible.
- Do not route signal lines parallel to Tx/Rx signals on the adjacent layers to avoid coupling.
- Place possible noise sources or sensitive signals away from the high-speed signals.
- Keep the trace length of all Ethernet interface signals equal and as short as possible.
- It is recommended to keep the trace lengths within the Tx and Rx trace bundles at matching lengths and as short as possible (~250 – 400 um).
- The Tx_CLK transmit clock trace/stripline shall have a distance of at least >300 um from the neighboring signal traces. The data traces / striplines may have a distance of 125 um between each other.
- It is recommended to use a total trace length less of than 7.5 cm for this interface on the boards. If longer traces are required, always check with simulations.
- Always keep the return path of the high-frequency current (lowest inductance path) small.
  - Route the signals with adjacent ground reference and avoid signal and reference layer changes.
  - Routing ground on each side can help to reduce coupling to other signals.
  - Avoid cutting the GND plane by via groups. A solid and uninterrupted GND plane under critical signals must be designed.
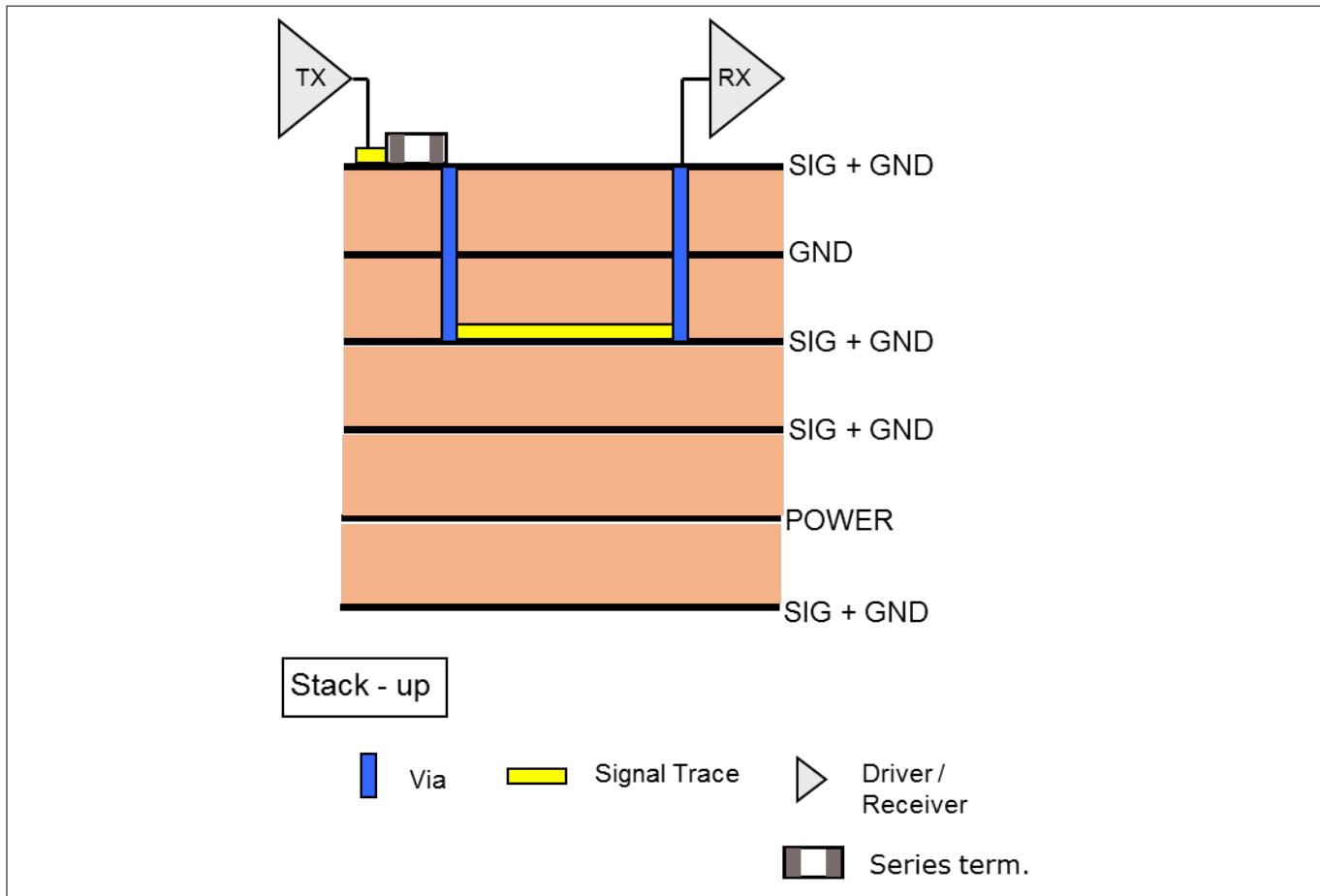
Figure 5 **Stripline transmission line**

- Route the clock line first and use a straight line for connection.
- Minimize the via count on signal lines (if possible, do not use any).

2.3 Termination of transmission lines

There are different types of termination techniques. It is recommended to use series termination (or source termination). The recommended start value is ~39 Ω. This value shell be confirmed by simulation of the customer PCB from the customer.

This is normally used by the single ended lines where the output driver has lower impedance than the transmission line. In this case the series termination is added to the output of the driver to match the line impedance.
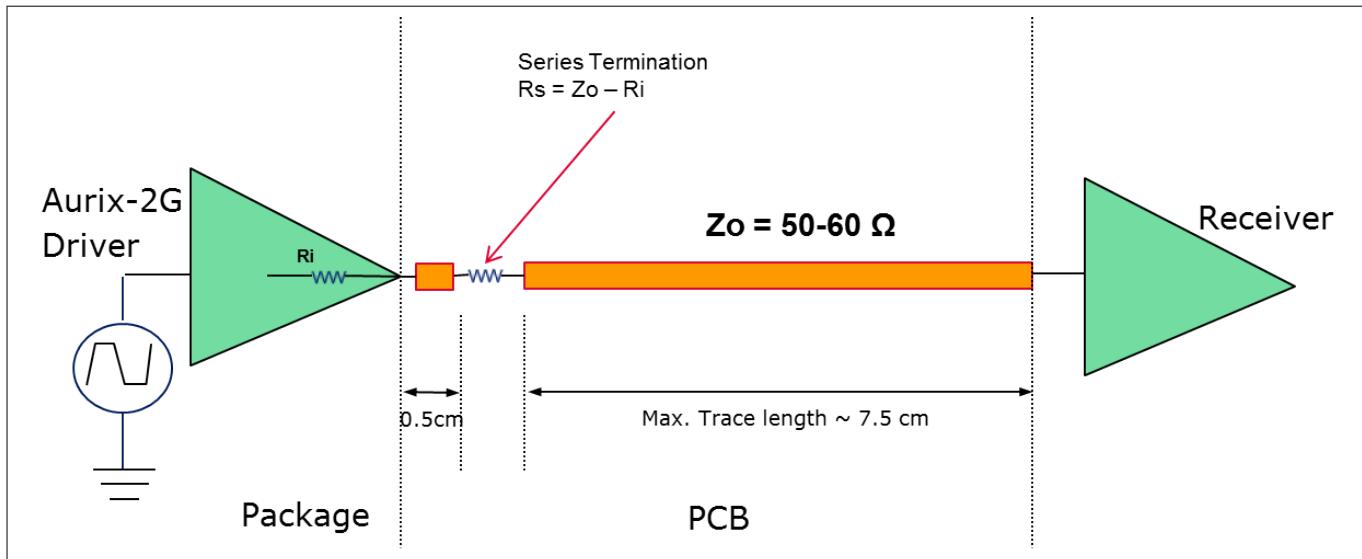
Figure 6   **Series (source) termination for single ended lines**

- Place the resistor very close to the source driver.
- Do not use daisy-chain topology.
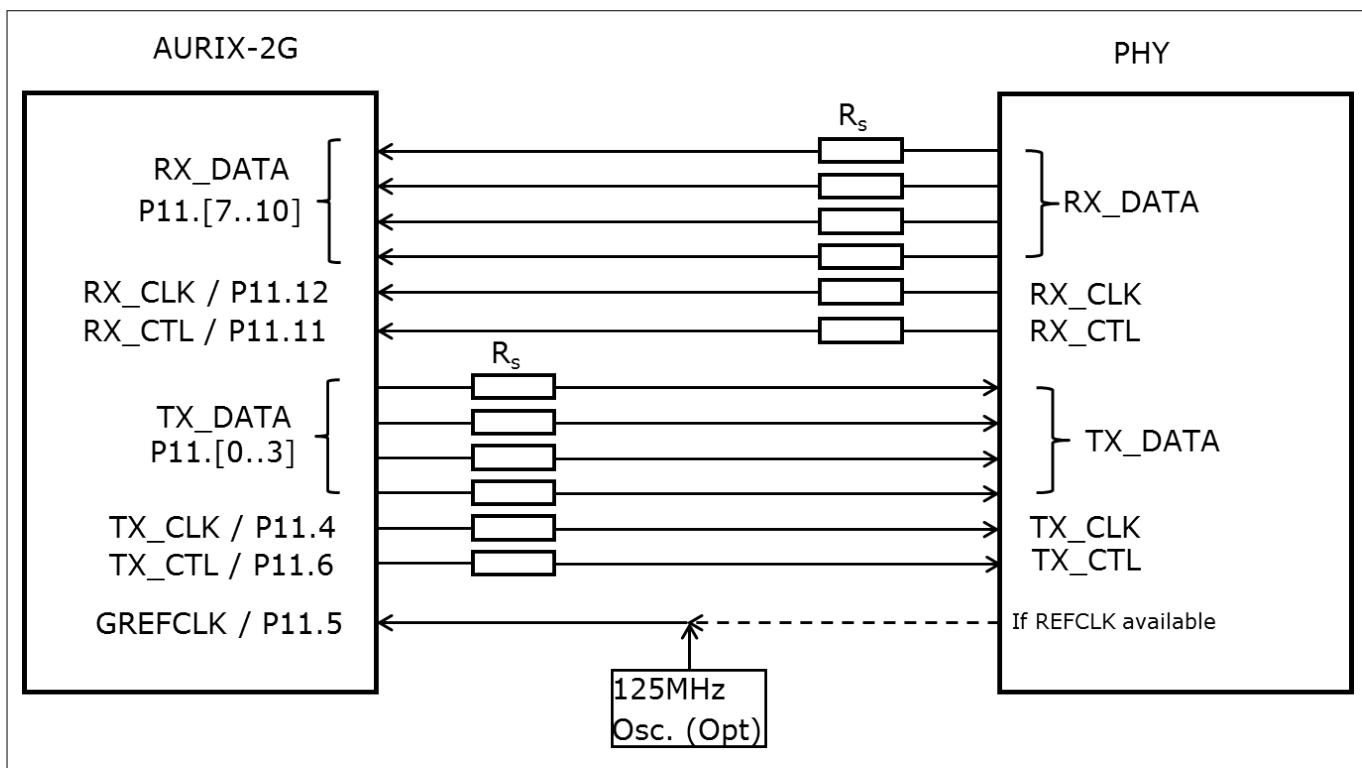
Figure 7   **Simple RGMII connection diagram with series termination resistors**

2.4   IBIS Simulation example

A high-speed simulation using IBIS files is a kind of standard during designs of PCBs. Infineon Technologies provides for each device of the TC3xx these kinds of files. The surrounding temperature is an aspect which shell be checked as well.

Out of the chapter before the following model was used for that example.
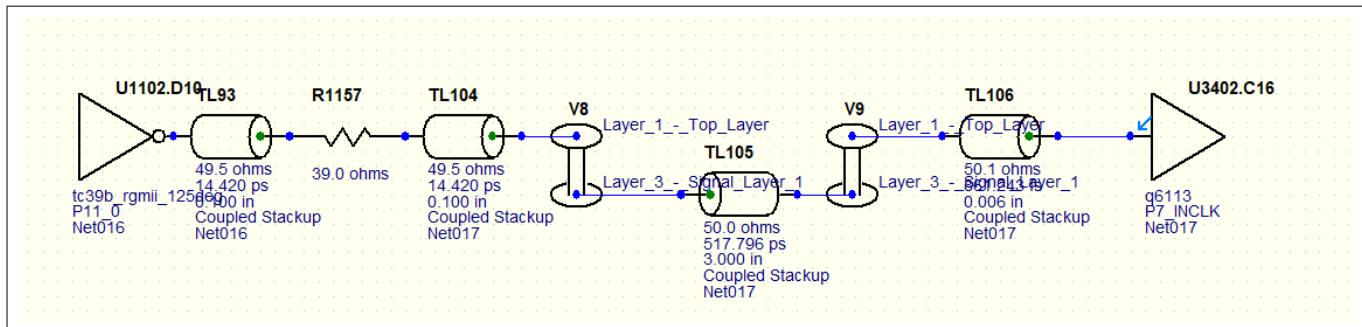
Figure 8   **Simple RGMII simulation example**

The simulated example results in the following waveform for a typical use case.
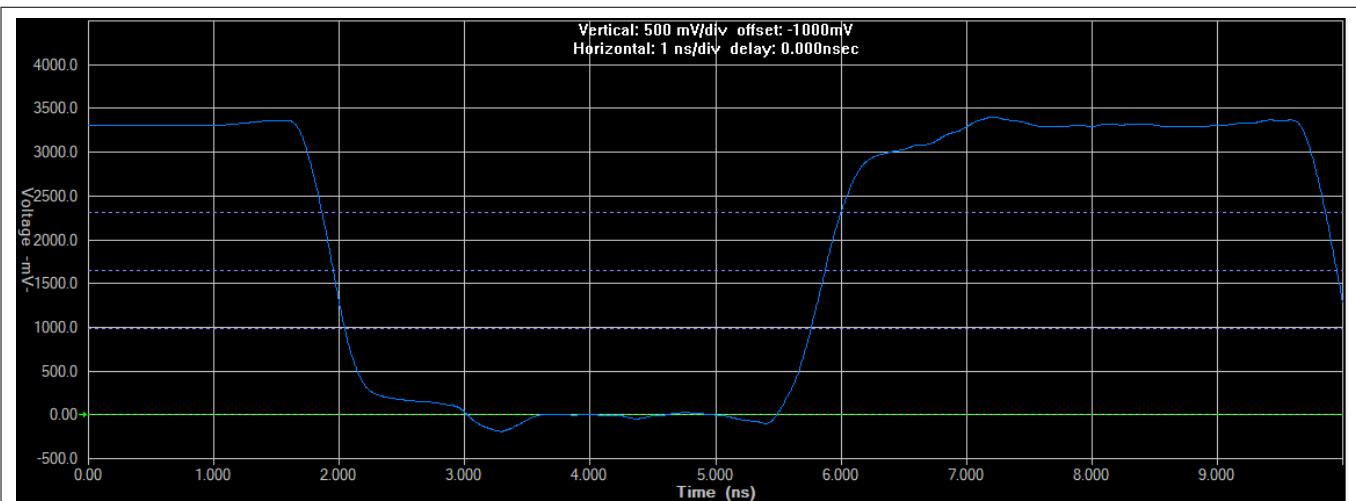
Figure 9   **Simple RGMII simulation result**

While looking to the slow and fast corner of that simulation, adaptions of the series termination or transmission line impedance value is required to meet timings and over/under shoot values of the connected device.

2.5   Board level filtering and de-coupling

De-coupling the Power Distribution Network of the microcontroller IC is critical to the PCB design process because careful selection of the de-coupling capacitors and placement has a big influence on the high-speed performance of the board, and can reduce the emissions. The on-board de-coupling capacitors have an effective range of 1 MHz – 200 MHz. The range above 200 MHz can be covered by using power plane capacitance.

The effectiveness of the de-coupling capacitors depends on the optimum placement and connection type.

- Place capacitors as close as possible to the microcontroller.
- Keep the interconnection inductance of capacitors to the microcontroller as low as possible.
- Use low effective series resistance and inductance (ESR and ESL) capacitors.
  - Since parasitic inductance is the limiting factor of the capacitor response to high frequency demand of current from the device, the ESL of the capacitor and the connection inductance should be selected so that the optimum value for the design is reached.
- Connect capacitors with vias close to the side of the pads as shown in Figure 10.
  - Use side placement of the vias to reduce the current loop.
  - If a solid power plane can be built (without cutting the plane and impedance discontinuity), the de-coupling capacitors can be connected directly to the plane and microcontroller for the case of double side placement.
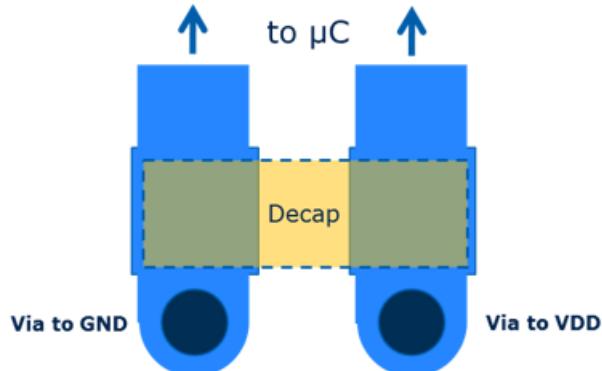
- Dual vias can be used to reduce the parasitic inductance.
- Solder lands, traces and vias should be optimized for capacitor placement.
- Do not use long traces to connect capacitors to GND or to VDD.
  - Always keep the return path of the high frequency current (lowest inductance path) small.
- Select the smallest package available for the capacitors.
- Select capacitors of type: ceramic multilayer X7R or X5R.
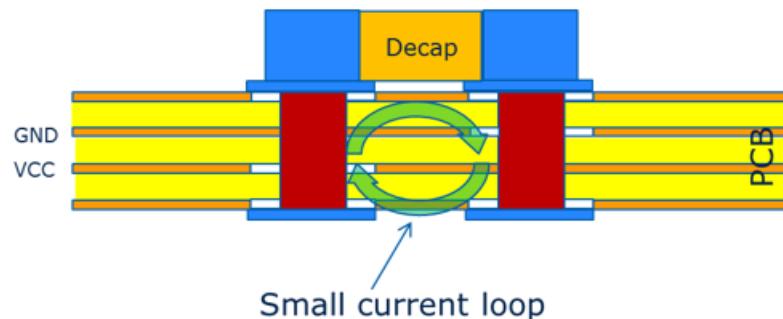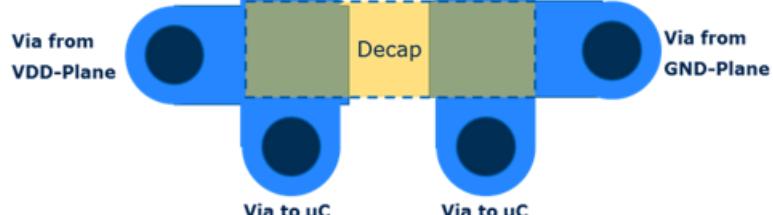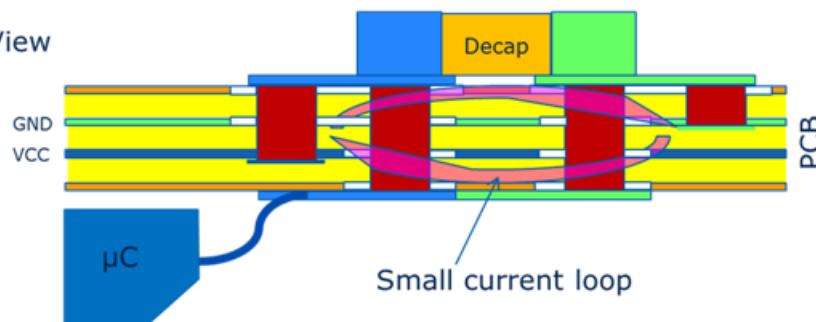
Figure 10   **Connection of decaps**

- Design a VFLEX / VFLEX2 plane on the power layer to generate a capacitance to filter the high frequency noise at VEXT net which is effective above 200 MHz.
- Use two 100 nF de-coupling capacitor for each VFLEX / VFLEX2 net. One should be connected directly to VFLEX (D5) / VFLEX2 (V19) and the VSS (D4/W19) balls of the BGA package with vias. The other 100nF

capacitor should be connected to plane area (see Figure 9 and 10). The second 100nF capacitor reduces the emission ~3 dB µV (towards to VR).

- Use at least 2 vias to connect VFLEX / VFLEX2 nets to VSS (D5/D4 pins/V19/W19) to the de-coupling capacitor on the bottom layer.

- Use a ferrite bead to de-couple the main supply line from the VFLEX (2) net (consider the design parameter like impedance at 100 MHz, rated current and DC-Resistance). The Ferrite Bead reduces the emission towards to VR ~20 dB µV.
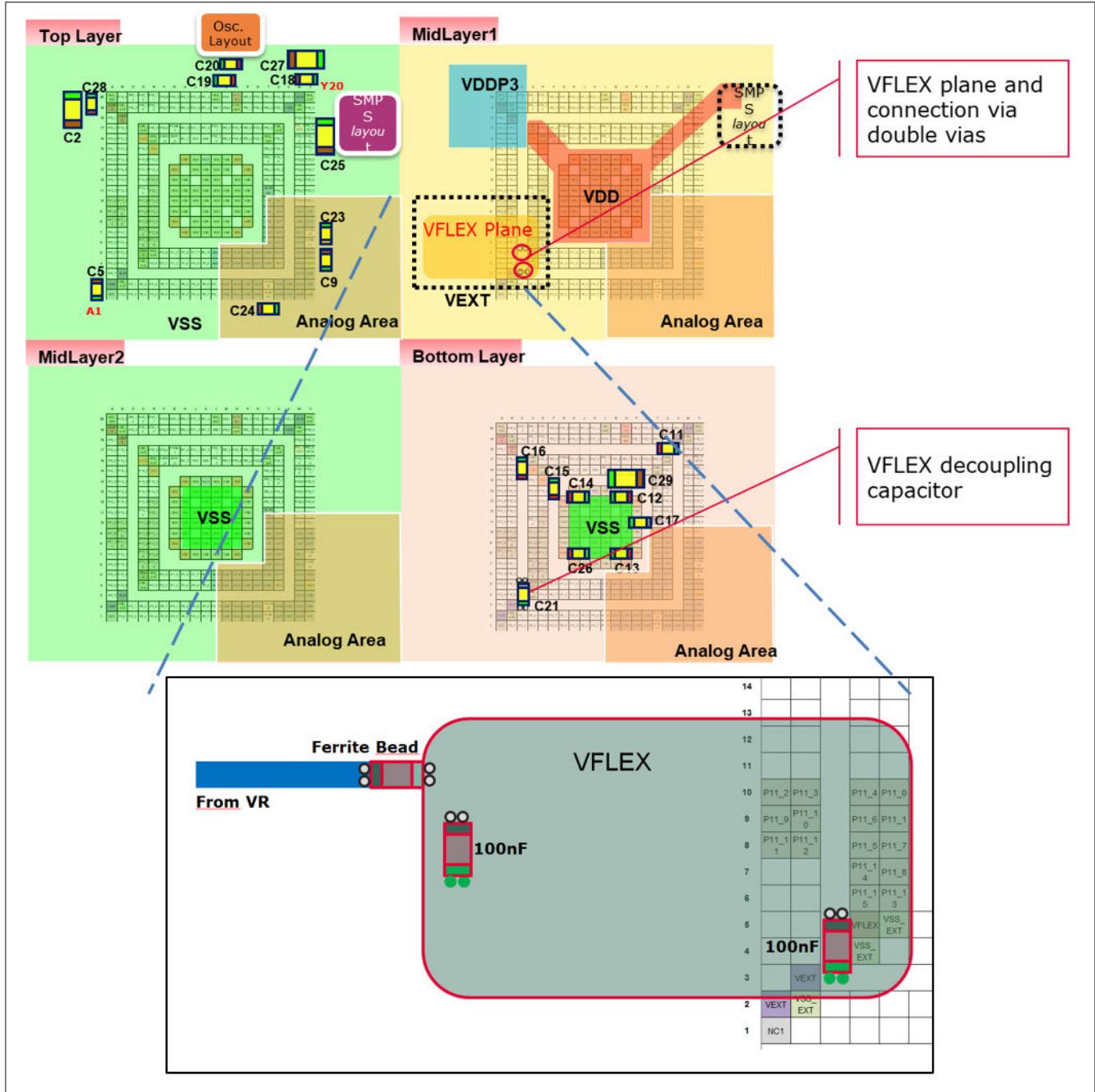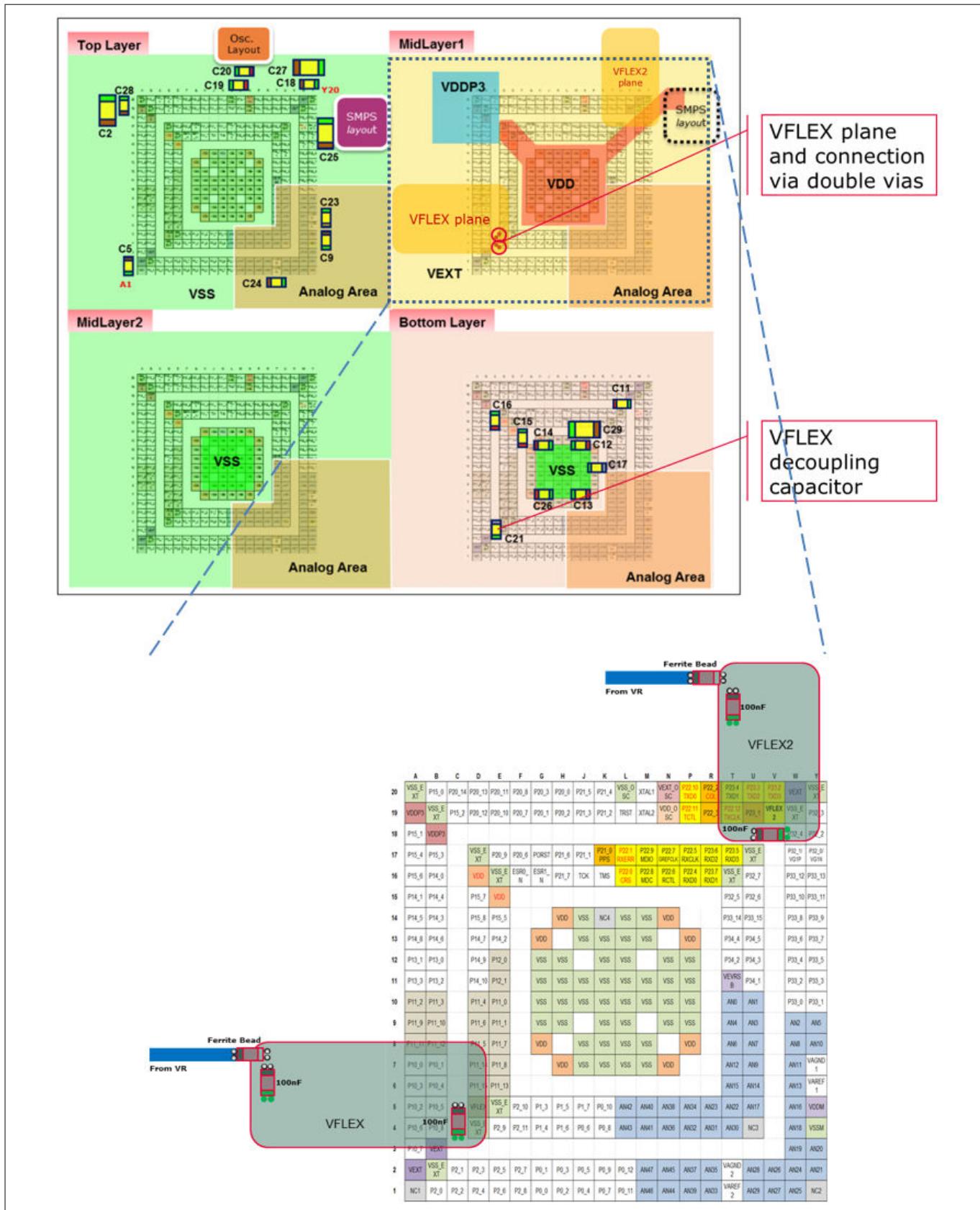
Figure 11   **VFLEX plane on power layer for one Gbit Ethernet version (BGA-292 version shown)**

Figure 12 **VFLEX / VFLEX2 plane on power Layer for two Gbit Ethernet (only for TC377….)**

Revision history

Document revision	Date	Description of change
V1.0		Initial version
V1.1		Figure-2, 6 and 8 updated, Ferrite bead and 2x100nF added to VFLEX net.
V1.2		Figure-5, -9, Impedance value and max. Trace length updated. Chapter 1.2 added.
V1.3		Figure -9 split in to Figure-9 and Figure-10
V1.4		Add new chapter 2.4, adaption of some text parts in chapter 2.2 and 2.3
V1.5	2024-04-17	Template update; no content update.

Trademarks

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