# Computer Architecture Homework #4

Verilog RISC-V controller

TA: Chi-Hung Weng (r08943010@ntu.edu.tw)

Due 2020/12/15 13:00 Tuesday (CEIBA, no late homework is allowed.)

## 1. Introduction

In this exercise, we follow the work done in HW3, using Verilog to design the controller in the RISC-V architecture. The controller generates control signals for registers, memory, ALU and PC(program counter) to do the correct operations based on the instructions decoded.

Control Signals are mainly based on the instruction type, so we make use of the output from the module you finished in HW3. After connecting the decoder and the controller, you almost finish the half of the implementation of the RISC-V architecture.

You have to rename the Verilog filename and the module name “CHIP” in HW3 to “HW3” for the use in this HW.

(Please use your HW3 module directly instead of doing this HW from scratch.)

We ask you to generate control signals from the classified results from HW3. The control signals format in this exercise is as below , where ALUOp is a 4-bit signal.

{ JAL, JALR, Branch, MemRead, MemWrite, MemtoReg, RegWrite, ALUSrc, **ALUOp**}

**ALUOp** for different operations assigned in this HW are listed in the table below:

| | | | | | |
|---|---|---|---|---|---|
| ADD | 0000 | SUB | 1000 | SLL | 0001 |
| SLT | 0010 | XOR | 0100 | SRL | 0101 |
| SRA | 1101 | OR | 0110 | AND | 0111 |

Since we skipped the immediate decoding in HW3, we also ask you to decode immediate in this HW. The immediate for different type of instructions stored in different bits of the instructions, you have to refer to the green sheet to finish this part.

(Note: For convenience, the immediate should also delay one cycle to output with other signals at the same time.)

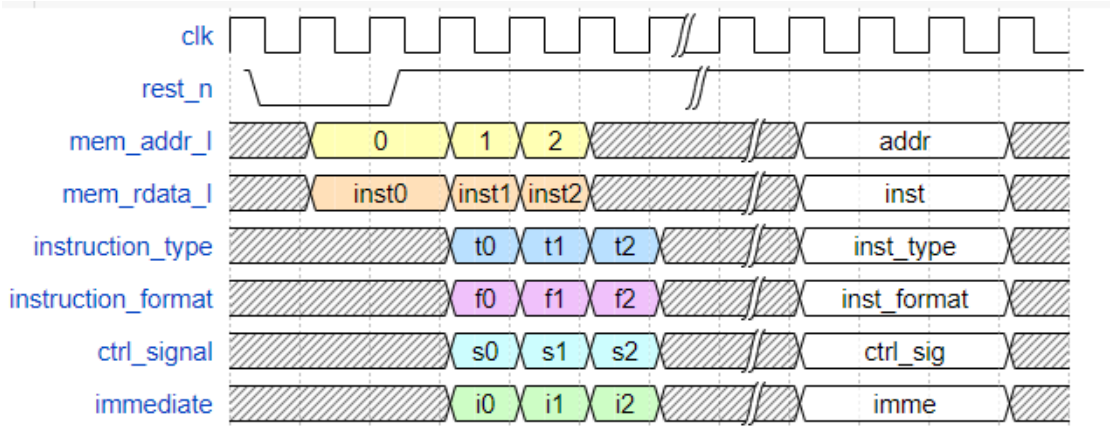
## 2. Specification

The input/output pins are defined in the table below:

| Signal name | I/O | Bit width | Description |
|---|---|---|---|
| **clk** | I | 1 | Clock signal.<br>Positive edge trigger. |
| **rst_n** | I | 1 | Active low **asynchronous** reset signal. |
| **mem_addr_I** | O | 30 | Output address of the instruction memory |
| **mem_rdata_I** | I | 32 | Instruction read from instruction memory |
| **ctrl_signal** | O | 12 | Controller output |
| **immediate** | O | 32 | Immediate decode from the instructions |

## 3. Waveform

The design waveform is shown as below.




Since the instruction type/format delay one cycle in HW3, the required outputs in this HW also delay one cycle. (For the Single Cycle RISC-V implementation, this delay should be removed if you want to use these modules directly in your final project)

## 4. Simulation Scripts

4.1 RTL Simulation

**ncverilog tb_HW4.v +define+RTL +access+r**

4.2 Gate-level Simulation

**ncverilog tb_HW4.v +define+SYN +access+r**

4.3 Debug

**nWave &**

## 5. Files

- The deadline for this exercise is 13:00, Dec. 15th. Your work should be submitted in a compressed file following the naming convention, HW4_yourID.zip (for example, HW4_b07901999.zip). The file should look like: **(5% penalty for wrong format)** There's a 10% penalty for incorrect upload format. No late submission is accepted.
- HW4_yourID.zip
  - HW4_yourID/
    - HW3.v (HW3 RTL file)
    - HW4.v (HW4 RTL file)
    - HW4_syn.v (synthesized gate-level netlist)
    - HW4_syn.ddc (Design database generated by Synopsys Design Compiler)
    - HW4_syn.sdf (Pre-layout gate-level sdf)
    - yourID.pdf (Report)
    - cycle.txt (cycle time that you can pass tb)

## 6. Grading Criteria

| Item | Description |
|---|---|
| RTL correctness(25%) | Your HW4.v should pass RTL simulation. |
| Using HW3 module (15%) | Connect to your previous design. |
| Gate-level correctness (20%) | Your HW4_syn.v should pass Gate-level simulation and without latches |
| Hidden tb (10%+10%) | Should pass simulations of the hidden tb. |
| Report (20%) | Snapchat:<br>1. RTL(Pass)<br>2. SYN(Pass)<br>3. no latch<br>4. Timing report → report_timing<br>5. Area report → report_area<br>6. Cycle time in cycle.txt |

If you cannot use your own HW3 file(something wrong), we can provide you HW3 answer, but the grade in "Using HW3 module" is at most 10pts.

Ref:

RTL:

```
Success! Execution 23                    10000                    10000
Success! Execution 23   00000000000000000001  00000000000000000001
=========================================The RTL result is PASS==========================================
```

SYN:

```
Success! Execution 20   00000000000000000001000  00000000000000000001000
Success! Execution 21                    10000                    10000
Success! Execution 21   00000000000000000100  00000000000000000100
Success! Execution 22                    10000                    10000
Success! Execution 22   00000000000000000010  00000000000000000010
Success! Execution 23                    10000                    10000
Success! Execution 23   00000000000000000001  00000000000000000001
=========================================The SYN result is PASS==========================================
```

No latch:

```
Inferred memory devices in process
        in routine CHIP line 76 in file
                '/home/raid7_2/user08/r08016/Test_HW3/v1_2/CHIP.v'.
===============================================================================
|     Register Name      |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|  instruction_type_reg  | Flip-flop |  23   |  Y  | N  | Y  | N  | N  | N  | N  |
| instruction_format_reg | Flip-flop |   5   |  Y  | N  | Y  | N  | N  | N  | N  |
|         PC_reg         | Flip-flop |  32   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
Presto compilation completed successfully.
Current design is now '/home/raid7_2/user08/r08016/Test_HW3/v1_2/CHIP.db:CHIP'
Loaded 1 design.
Current design is 'CHIP'.
Current design is 'CHIP'.
```

Timing report:

```
CHIP              tsmc13_wl10           slow

Point                                   Incr       Path
-----------------------------------------------------------
clock CLK (rise edge)                   0.00       0.00
clock network delay (ideal)             0.50       0.50
input external delay                    0.10       0.60 f
mem_rdata_I[3] (in)                     0.02       0.62 f
U65/Y (CLKINVX8)                        0.03       0.66 r
U69/Y (AND3X8)                          0.09       0.75 r
U43/Y (NOR3BX4)                         0.11       0.86 r
U66/Y (BUFX16)                          0.09       0.96 r
U121/Y (NAND3X8)                        0.09       1.05 f
U175/Y (NOR3X1)                         0.20       1.25 r
instruction_type_reg_10_/D (DFFRX1)     0.00       1.25 r
data arrival time                                  1.25

clock CLK (rise edge)                   1.00       1.00
clock network delay (ideal)             0.50       1.50
clock uncertainty                      -0.10       1.40
instruction_type_reg_10_/CK (DFFRX1)    0.00       1.40 r
library setup time                     -0.15       1.25
data required time                                 1.25
-----------------------------------------------------------
data required time                                 1.25
data arrival time                                 -1.25
-----------------------------------------------------------
slack (MET)                                        0.00
```

Area report:

```
****************************************
Report : area
Design : CHIP
Version: N-2017.09-SP2
Date   : Fri Nov 13 23:57:26 2020
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CE

Number of ports:                          153
Number of nets:                           438
Number of cells:                          354
Number of combinational cells:            290
Number of sequential cells:                63
Number of macros/black boxes:               0
Number of buf/inv:                        134
Number of references:                      48

Combinational area:            3376.128590
Buf/Inv area:                  1363.012206
Noncombinational area:         2393.333981
Macro/Black Box area:             0.000000
Net Interconnect area:        32993.498932

Total cell area:               5769.462571
Total area:                   38762.961503
```

Cycle time:

```
1  cycle time: 5
```