Computer Architecture Final Project

Verilog Single Cycle RISC-V

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If you have any problem, contact us by email first.

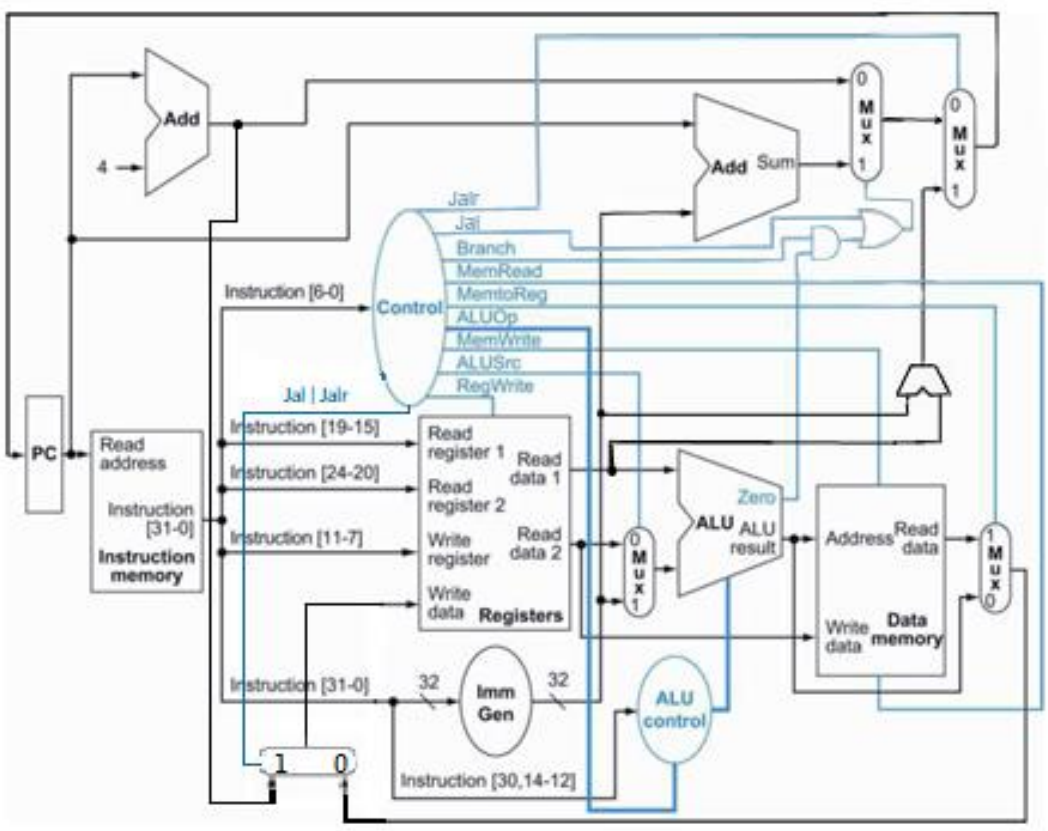
Due 2021/1/9 13:00 Saturday (CEIBA, no late homework is allowed.)

統一公告網址: **https://tinyurl.com/2020-CA-Final**

1. Introduction

Microprocessor without Interlocked Pipeline Stages (RISCV) is a widely used instruction set architecture. We've already had comprehensive understandings of it in our Computer Architecture course. In this exercise, we're going to implement the single-cycle RISCV architecture using Verilog. This exercise will give you a hardware viewpoint to this architecture.

The RISCV architecture is shown in Fig. 1. In this exercise, the instruction memory and data memory are implemented in the testbench. Except the memories, you need to implement everything else by yourself.



2. Specification

The input/output pins are defined in Table. 1. The required instructions you need to support in the baseline are “JAL, JALR, BEQ, BNE, LD, SD, ADDI, SLTI, XORI, ORI, ANDI, SLLI, SRLI, SRAI, ADD, SUB, SLL, SLT, XOR, SRL, SRA, OR, AND”. The complete machine codes for the required instructions are not listed in this document. Please refer to your textbook or RISCV Green Sheet for the full machine code, our testbench follows the standard machine code rules.

The input/output pins are defined in Table1:

Tabel. 1 :I/O pins specification

Signal name	I/O	Bit width	Description
clk	I	1	Clock signal. Positive edge trigger.
rst_n	I	1	Active low **asynchronous** reset signal.
mem_addr_I	O	30	Output address of the instruction memory
mem_rdata_I	I	32	Instruction read from instruction memory
mem_wen_D	O	1	Write-enable Set it high to write data into memory.
mem_addr_D	O	30	Decode and output R/I/S/B/J type
mem_wdata_D	O	64	Signals read from data memory.
mem_rdata_D	I	64	Data store to data memory.

Note the instruction and data memory is stored in little Endian.

3. Files

- Your work should be submitted in a compressed file following the naming convention, Final_Group#.zip (for example, Final_Group1.zip). There’s a 20% penalty for incorrect upload format. No late submission is accepted.
  - Final_Group#.zip
    - Final_Group#/
      - RISCV.v (RTL file)
      - RISCV_syn.v (synthesized gate-level netlist)
      - RISCV_syn.ddc (Design database generated by Synopsys Design Compiler)
      - RISCV_syn.sdf (Pre-layout gate-level sdf)
      - Report_Group#.pdf (Report, replace with your index)
      - Outcome.txt

4. Grading Criteria

We encourage you to generate testing file by RARS.

Make sure to check signed executions for some instructions.

Plagiarism is prohibited!

Item	Description
RTL tb1/tb2/tb3 correctness (30%)	Your RISCV.v should give correct answer. (no latch and non-negative slack) No timing violation after reset.
RTL (hidden) (10%)	Additional test case besides the provided files
Gate-level tb1/tb2/tb3 correctness (30%)	Your RISCV_syn.v should give correct answer.
Outcome.txt	See the reference below
Report (10%)	1. no latch 2. Timing report → report_timing 3. Area report → report_area 4. Please describe how you design this single cycle RISCV (Architecture and some analysis for your A*T improvement) 5. Work distribution
Performance (20%)	Top 5 group: 20, 17, 14, 12, 10 Others: max(0, 15-rank)

Performance

When designing a digital system, there are some metrics to verify how well it performs, the common metrics are timing, area and power. We will use timing and area in this final project.

All groups in class will compete their A*T value(cost).

Grade A: Pass synthesis testbench (tb1+tb2+tb3) → A*T

Grade B: Pass RTL testbench (tb1+tb2+tb3) → A*T

Grade A > Grade B

Ref:

Outcome.txt

A: From area report (Total cell area)

T: Clock cycle you use to synthesis and pass gate-level simulation(tb1&tb2&tb3)

If you use 10 to synthesis but pass simulation at 12, please use 12 to calculate and also write 12 in Outcome.txt . We will run your gate-level simulation on the cycle time you provide.

```
RTL pass cycle: 10.0
SYN pass cycle: 10.0
Total cell area: 171861.744619
A*T(Area*SYN pass cycle): 1718617.44619
```

No latch:

```
Inferred memory devices in process
        in routine RISCV line 156 in file
                '/home/raid7_2/user08/r08016/Test_Final/v5/RISCV.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|       PC_reg        | Flip-flop |  32   |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
Warning:  /home/raid7_2/user08/r08016/Test_Final/v5/RISCV.v:189: signed to unsig

Inferred memory devices in process
        in routine reg_file line 192 in file
                '/home/raid7_2/user08/r08016/Test_Final/v5/RISCV.v'.
===============================================================================
|    Register Name    |   Type    | Width | Bus | MB | AR | AS | SR | SS | ST |
===============================================================================
|       mem_reg       | Flip-flop | 2048  |  Y  | N  | Y  | N  | N  | N  | N  |
===============================================================================
```

Timing report:

```
alu0/out[54] (alu)                       0.00       4.59 r
U615/Y (AO22X4)                          0.15       4.74 r
reg0/d[54] (reg_file)                    0.00       4.74 r
reg0/U212/Y (INVX12)                     0.06       4.81 f
reg0/U256/Y (CLKBUFX2)                   0.16       4.96 f
reg0/U254/Y (INVX6)                      0.08       5.04 r
reg0/U255/Y (CLKINVX12)                  0.07       5.11 f
reg0/U4437/Y (MXI2X1)                    0.14       5.25 r
reg0/mem_reg_9__54_/D (DFFRX1)           0.00       5.25 r
data arrival time                                   5.25

clock CLK (rise edge)                    5.00       5.00
clock network delay (ideal)              0.50       5.50
clock uncertainty                       -0.10       5.40
reg0/mem_reg_9__54_/CK (DFFRX1)          0.00       5.40 r
library setup time                      -0.15       5.25
data required time                                  5.25
-----------------------------------------------------------
data required time                                  5.25
data arrival time                                  -5.25
-----------------------------------------------------------
slack (MET)                                         0.00
```

Area report:

```
dc_shell> report_area

****************************************
Report : area
Design : RISCV
Version: N-2017.09-SP2
Date   : Sun Dec 13 15:26:39 2020
****************************************

Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CE

Number of ports:                         1495
Number of nets:                         15498
Number of cells:                        12141
Number of combinational cells:          10092
Number of sequential cells:              2040
Number of macros/black boxes:               0
Number of buf/inv:                       2006
Number of references:                      79

Combinational area:             106724.023813
Buf/Inv area:                    17958.492030
Noncombinational area:           65137.722805
Macro/Black Box area:                0.000000
Net Interconnect area:         1602121.526459

Total cell area:                 171861.746619
Total area:                     1773983.273077
1
```