FPGA Design Guide

guide-fpga

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Jinzhi Cai

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1 Introduction

In this guide, we will discuss FieldProgrammable Gate Array and System on Chip technologies and relative application. Due to the need, ORBiT Avionics department desided to create next generation bus system for the rocket. For help club member to learn and understand this technology, this guide will introdute the basic knowledge of FPGA and SoC.

1.1 FPGA and SoC

FPGA

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SoC FPGA

SoC FPGA is a new kind of FPGA chip which embedded a hardware processor inside to improve performent. In a SoC FPGA, there are two parts. Programmable Logic(PL) is the part that use FPGA technology which allow user to create costum logic, and Processor System(PS) is an embedded hardware processor to provide computing power. Cyclone V(Intel) and ZYNQ 7000(Xilinux) are two most known SoC FPGA platform. They both use ARM Cortex processor and its AXI bus system.

1.2 What is VHDL

Basic Structure

The example following is a example format entity in VHDL. When writing entity, the name for the entity should be unique and match with the name in the architecture. Architecture name and port name should also unique.

```
library ieee; -- import libraries
use ieee.std_logic_1164.all; -- use standard library

entity <entity_name> is port(

        <name>   : <in/out/inout> <type>;
        <name>   : <in/out/inout> <type>

);
end <entity_name>;

architecture <arch_name> of <entity_name> is
```

```
        -- this is a comment
        -- add signals and other variables
begin

        -- VHDL sentence

end <arch_name>;
```

This is a example design for a Single port RAM.

```
-- Quartus Prime VHDL Template
-- Single port RAM with single read/write address

library ieee;
use ieee.std_logic_1164.all;

entity single_port_ram is

        generic
        (
                DATA_WIDTH : natural := 8;
                ADDR_WIDTH : natural := 6
        );

        port
        (
                clk: in std_logic;
                addr: in natural range 0 to 2**ADDR_WIDTH - 1;
                data: in std_logic_vector((DATA_WIDTH-1) downto 0);
                we: in std_logic := '1';
                q: out std_logic_vector((DATA_WIDTH -1) downto 0)
        );

end entity;

architecture rtl of single_port_ram is

        -- Build a 2-D array type for the RAM
        subtype word_t is std_logic_vector((DATA_WIDTH-1) downto 0);
        type memory_t is array(2**ADDR_WIDTH-1 downto 0) of word_t;

        -- Declare the RAM signal.
        signal ram : memory_t;

        -- Register to hold the address
        signal addr_reg : natural range 0 to 2**ADDR_WIDTH-1;
```

```
begin

        process(clk)
        begin
        if(rising_edge(clk)) then
                if(we = '1') then
                        ram(addr) <= data;
                end if;

                -- Register the address for reading
                addr_reg <= addr;
        end if;
        end process;

        q <= ram(addr_reg);

end rtl;
```

1.3 Introduction of Quartus Prime

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2 Quartus Prime SoC FPGA Development

2.1 Hello World for FPGA

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2.2 Create a Complex Entity

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