OA-II VEH TAM System Design

DR00004

Rev: A01

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Table of Contents

1 Introduction **2**
1.1 Scope 2
1.2 Purpose 2
1.3 Relevant Documents 2
1.4 Revision History 2

2 Requirement Analysis **3**
2.1 General Requirement Analysis 3
2.2 Bridge Requirement Analysis 3
2.3 Control Requirement Analysis 3

3 Current Controller Analysis **4**
3.1 Microcontroller 4
3.2 FPGA Soft Core Processor 4
3.3 SoC FPGA 4

4 Recommand Design **5**

1 Introduction

1.1 Scope

This document analyze the requirement of ORBiT Avionics System II Vehicle Electronics Telecommunication and Acquisition Module(OA-II VEH TAM) and come up with recommand design for it.

1.2 Purpose

The goal of this document is use to analyze the current sensor technology and come up with a recommand design.

1.3 Relevant Documents

ER00002 ORBiT Avionics System II Requirements

ES00002 ORBiT Avionics System II Architecture

ES00003 OA-II Vehicle Electronics (VEH) System Architecture

DR00001 OA-II Backplane Bus System

DR00002 OA-II VEH Camera System Design

1.4 Revision History

Rev	Author	Approver	Changes	Date
A01	Jinzhi Cai	Jinzhi Cai	Initial draft	2019-7-22

Table 1: Summary of Revision History

2 Requirement Analysis

2.1 General Requirement Analysis

The TAM system requirement mainly can be divide to two part. The first part is bridge which is transfer data from low speed parallel sensor connection to high speed serial backplane. The second part is control which configure all the sensor connect to the board and execute basic unit transformation.

2.2 Bridge Requirement Analysis

The TAM sensor unit need to be have to bridge different data bus to the backplane data bus. The TAM sensor unit need to support:

2.3 Control Requirement Analysis

The TAM sensor unit need to be able to configure the sensor to correct status and execute basic data transformation to transfer data to real physical value. The delay should not more than 100ms and should support up to 32 channel.

3 Current Controller Analysis

3.1 Microcontroller

It do come with a lot of different interface. However, it do not have a high speed interface what can use to connect between different system. It usually have a lot of different interface in a few number. It is different with the requirement that need a few kind of interface with high speed.

3.2 FPGA Soft Core Processor

A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by a customer or a designer after manufacturing – hence the term "field-programmable".[**?**] Almost every FPGA company will have it own soft core processor. Those processor existing in code form and allow user to rebuild them in the FPGA chip as long as the chip have enough resource. Even the soft core processor allow user to costume the structure, the speed of soft core processor will not as fast as the SoC processor. However, it is fairly easy to interface to other system.

3.3 SoC FPGA

The SoC FPGA basicly also is a kind of FPGA. The only different it embedded a powerful processor as know as hard core processor. It help fuse the benefit between the SoC chip and FPGA chip. On one hand, it allow big system running in the powerful hard core processor. In the same time, the flexibility of FPGA chip allow costume interface and upgrade ability. However, SoC FPGA have less logic resource compare with the classic FPGA and weak proessing power compare with SoC which in the same price. In the TAM system, the computing power is not nessary.

4 Recommand Design

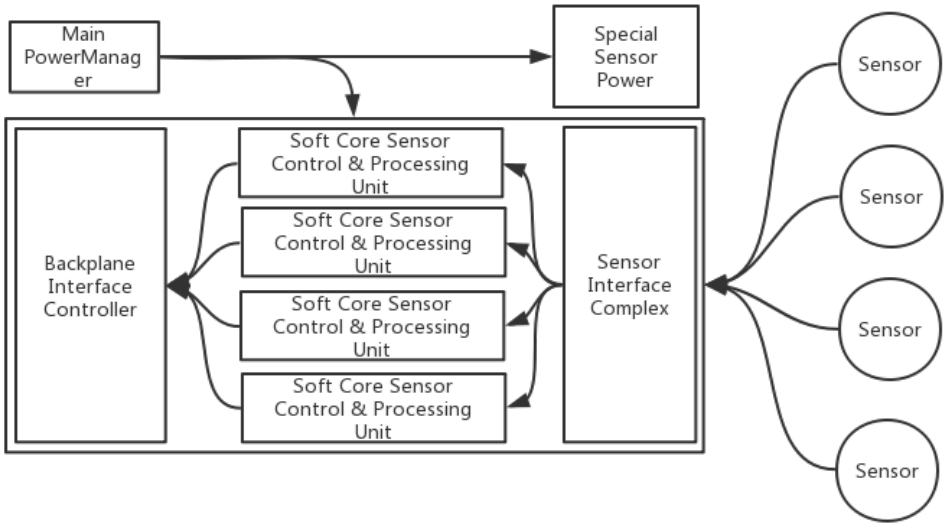

Figure 1: Block Diagram For TAM System