OA-II VEH Camera System Design

DR00002

Rev: A01

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1 Introduction

1.1 Scope

This document discuss the current camera technology and construct a design that will fulfill the need for OA-II VEH system.

1.2 Purpose

The goal for this document is come up with a design that will provide four 1080p 60Hz video steam and storage to a central storage media by research the current camera technology.

2 Revision History

Rev#	Editor	Delta	Date
A01	Jinzhi Cai	Initialize	2019-7-10

Table 1: Summary of Revision History

3 General Structure of Camera System

3.1 Introduction

The most basic camera system have three part. The camera sensor is the device that will receive data from the environment and transfer it via the camera interface. The data that flow out from the sensor is call raw data. It contain all the information that the camera get from the environment. A 1080p 60Hz camera have $1920 * 1080 = 2073600 pixels$. One pixels usually take $3 Bytes$ to save. For each second, $2073600 * 3 * 60 = 373248000 Bytes$ will be created. That will be $355.96 MB/s$ for one single camera.The encoder is use to compress the video steam smaller for it to transmission via long distence data link(usually with in $1 MB/s$). The storage unit is use to save the video steam to a file and allow future replay.

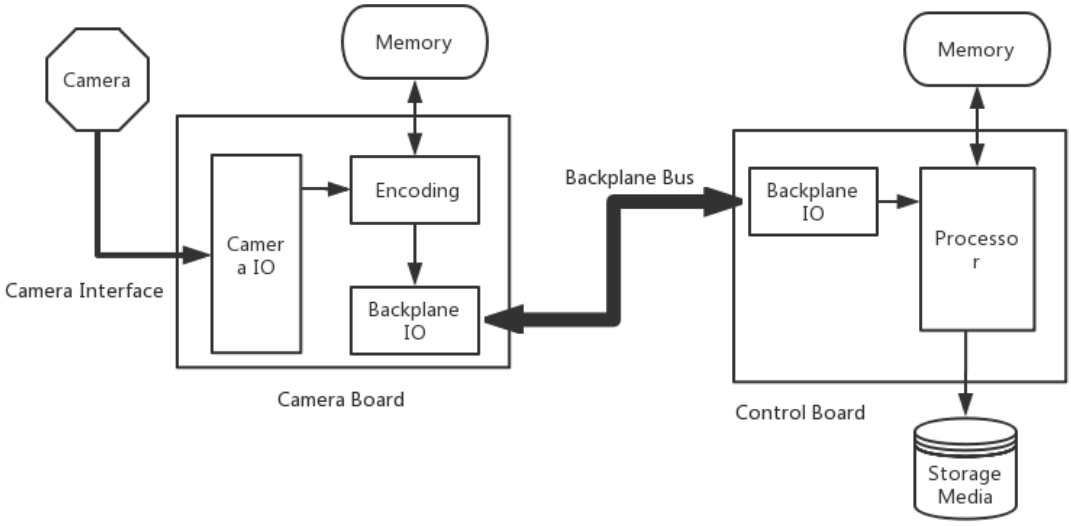

Figure 1: General Structure of Camera System

4 Camera Sensor and Relative Interface

4.1 Introduction

The camera sensor is the most improtant part in the camera system. The classic camera interface is use the same way to output the video signal as a monitor do. For each pixel clock, data of a pixel is been sended. After few clock(depend on the resolution), Line Sync rise to indecate one line data is finish transmission. The Frame Sync is indecate a frame of pixel data is sended. However, modern camera sensor usually use one of those three camera interface. Some of the is samiliar with the classic one, and other improve it.

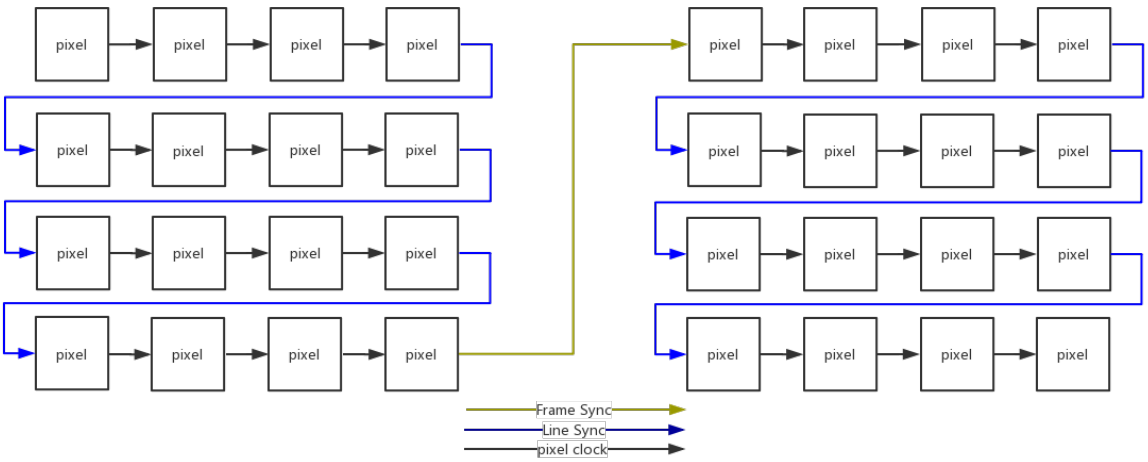

Figure 2: Classic Video Stream

4.2 DVP Interface

The DVP interface is use the classic video interface to transmit data out from the sensor. The I2C bus(SCK, SDA) that inside the interface is use to config the camera. The main clock is use to provide a clock for the camera. The VSYNC, HSYNC, PCLK is the clock system that help processor to indecate the weight and height of frame. The D OUT is data that comming out from the camera. It have low requirement on the trace and sample interface design. However, it can not offer long distence transmission and high speed clock. It usually use at low end 240p camera.

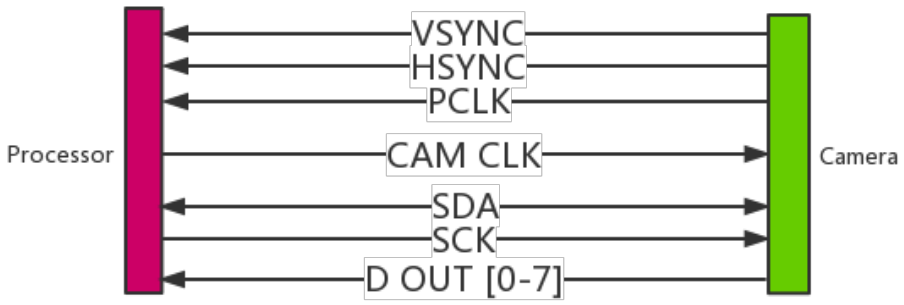

Figure 3: Physical Layer for DVP Interface

D OUT Data out put

VSYNC Lane Sync Signal

HSYNC Frame Sync Signal

PCLK Pixel Clock

CAM CLK Main Camera Clock

SDA I2C Data Line

SCK I2C Clock Line

4.3 LVDS Interface

The LVDS camera interface is use LVDS technology to improve classic DVP interface. It use differential signal to transmitting data. It increase the lane it need to send data, but differential signal can prevent common mode interference which limit the DVP clock for increasing.

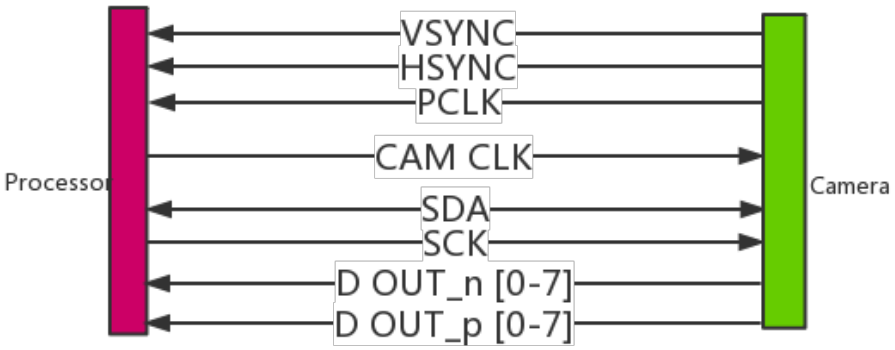

Figure 4: Physical Layer for LVDS Interface

DOUT n/p Differential Data Lane

VSYNC Lane Sync Signal

HSYNC Frame Sync Signal

PCLK Pixel Clock

CAM CLK Main Camera Clock

SDA I2C Data Line

SCK I2C Clock Line

4.4 MIPI CSI-2 Interface

The MIPI CSI-2 camera inferface[1] is different from the old one. The goal for this bus is to cut down the lane count for camera module and allow more data flow to the processor. In structure, the MIPI CSI-2 camera interface use different way to communicate. The MIPI interface use package as the data communication unit. Inside the sensor, data will be pack into a package and send it via the two or four data lane. The same process will reverse and output the raw camera data. MIPI camera will allow 1080p 60Hz or 4K 30Hz.

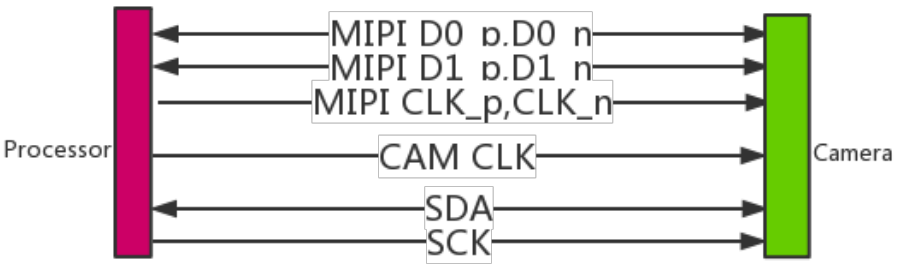

Figure 5: Physical Layer for 2 Lane MIPI Interface

MIPI D0n/p MIPI Data Lane 0

MIPI D1n/p MIPI Data Lane 1

MIPI CLKn/p MIPI Clock

CAM CLK Main Camera Clock

SDA I2C Data Line

SCK I2C Clock Line

4.5 USB Interface (UVC)

The USB camera interface[2] is different with the rest of the interface. In those camera, it include DSP chip that already finish the video compression. It is easy to use but do not support 60fps.

[1] Might only avaliable in high-end chip.
[2] It do have success example by using ZYNQ SoC FPGA.

5 Camera Interface Bridge Chip

5.1 Lattice CrossLink

The CrossLink is Lattice made small scale MIPI bridge FPGA.[3] It include two MIPI D-PHY and up to 8 mipi data lane. It also support interface translation (MIPI CSI-2 -> DVP).

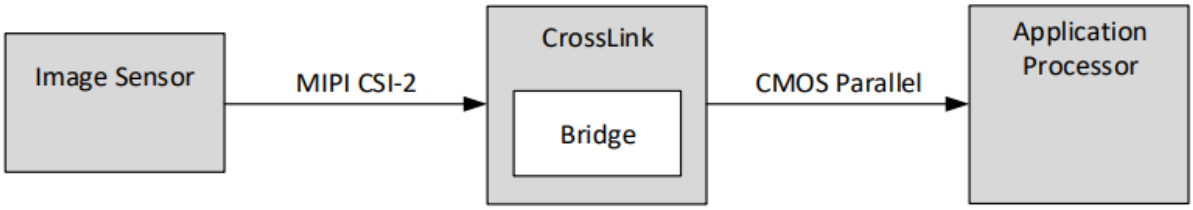

Figure 6: Block Diagram for CrossLink

5.2 Toshiba Camera Interface Bridge

The Toshiba Camera Interface Bridge is a stand alone chip that can converse MIPI CSI-2 bus to DVP bus. It also offer I2C bus to configure chip setting.

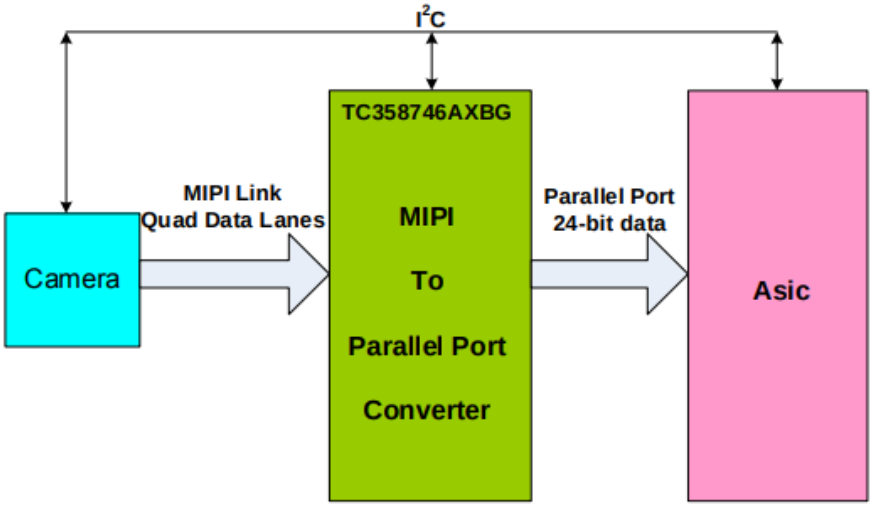

Figure 7: Block Diagram for Toshiba

[3] Too small for hardware encoder

6 H.264 Video Steam Encoding

6.1 Introduction

The H.264 Encoder is another important unit in the camera system. Due to the data flow of a camera sensor is too much for the backplane bus, compression is nessary.

6.2 IP Core Description

SoC Technology

This IP core fit for both **Intel** and **Xilinx**

Version	LUT use	Test Platform	Price for Platform
Standard Version	110k	Zynq-7 Z7045	$1000
Slim Version	50k	Artix-7 XC7A200T	$300
I-Frame Version	45k	Spartan-6 LX150	$200

Table 2: SoC Summary

A2E Technology

Version	LUT use	Test Platform	Price for Platform
Xilinx(1080p 30Hz)	11K	Zynq-7 Z7020	$300
Xilinx(1080p 60Hz)	11K	Kintex-7	$500
Xilinx(1080p 180Hz)	11K	Zynq UltraScale	$1000
Intel(1080p 30Hz)	8K	Cyclone V SoC	$500

Table 3: SoC Summary

6.3 Encoding SoC Chip

HiSilicon Hi3559

Hi3559 is HiSilicon made new generation mobile camera soc. It support MIPI interface and H.264 Video encoding. It can output video via USB 2.0 bus.

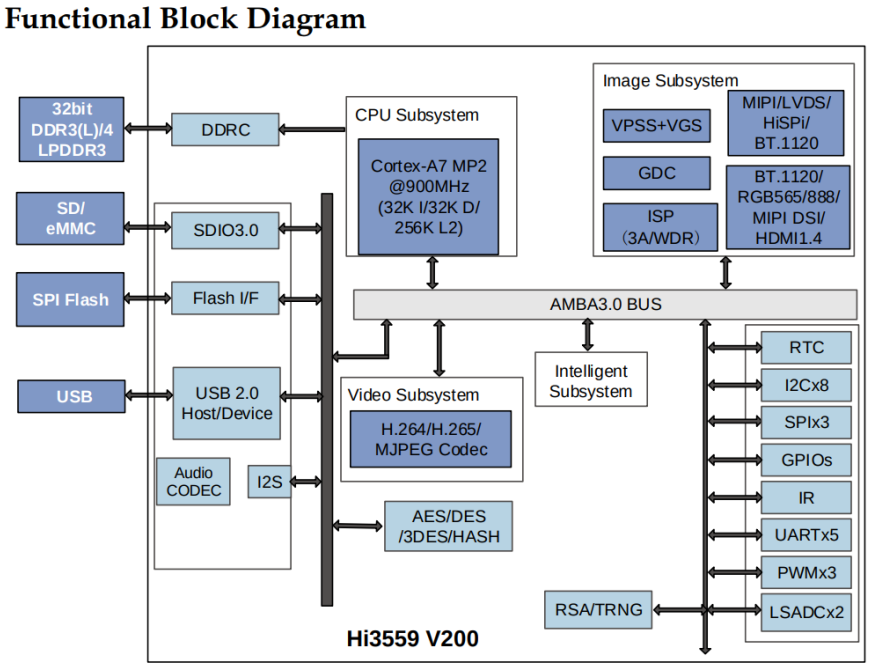

Figure 8: Block Diagram for Hi3559

OmniVision OV798

7 File System and Video Storage

7.1 Introduction

7.2 NVME Drive

7.3 Flash (QSPI Mode)

7.4 SD Cord(SPI Mode)

7.5 SD Cord(SD Mode)

8 System Diagram