OA-II VEH Camera System Design

DR00002

Rev: A01

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1 Introduction

1.1 Scope

This document discuss the current camera technology and construct a design that will fullfill the need for OA-II VEH system.

1.2 Purpose

The goal for this document is come up with a design that will provide four 1080p 60Hz video steam and storage to a central storage media by research the current camera technology.

2 Revision History

Rev#	Editor	Delta	Date
A01	Jinzhi Cai	Initialize	2019-7-10

Table 1: Summary of Revision History

3 General Structure of Camera System

3.1 Introduction

The most basic camera system have three part. The camera sensor is the device that will receive data from the environment and transfer it via the camera interface. The data that flow out from the sensor is call raw data. It contain all the information that the camera get from the environment. A 1080p 60Hz camera have $1920 * 1080 = 2073600 pixels$. One pixels usually take $3 Bytes$ to save. For each second, $2073600 * 3 * 60 = 373248000 Bytes$ will be created. That will be $355.96 MB/s$ for one single camera.The encoder is use to compress the video steam smaller for it to transmission via long distence data link(usually with in $1 MB/s$). The storage unit is use to save the video steam to a file and allow future replay.

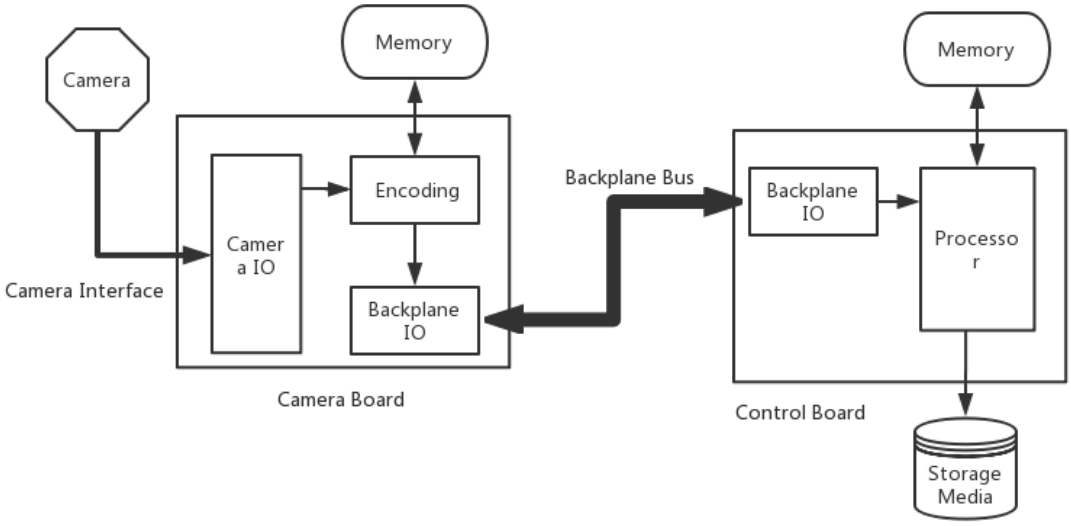

Figure 1: General Structure of Camera System

4 Camera Sensor and Relative Interface

4.1 Introduction

The camera sensor is the most improtant part in the camera system. The classic camera interface is use the same way to output the video signal as a monitor do. For each pixel clock, data of a pixel is been sended. After few clock(depend on the resolution), Line Sync rise to indecate one line data is finish transmission. The Frame Sync is indecate a frame of pixel data is sended. However, modern camera sensor usually use one of those three camera interface. Some of the is samiliar with the classic one, and other improve it.

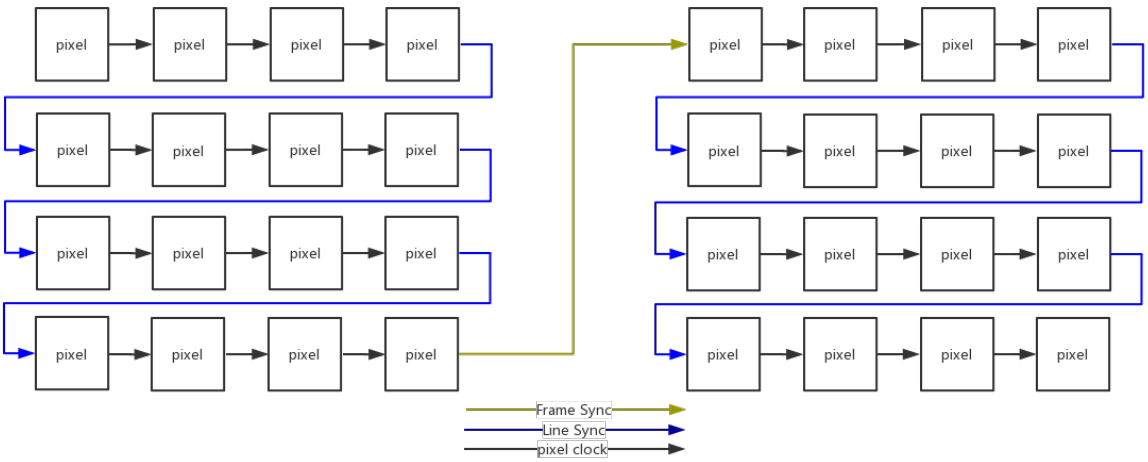

Figure 2: Classic Video Stream

4.2 DVP Interface

The DVP interface is use the classic video interface to transmit data out from the sensor. The I2C bus(SCK, SDA) that inside the interface is use to config the camera. The main clock is use to provide a clock for the camera. The VSYNC, HSYNC, PCLK is the clock system that help processor to indecate the weight and height of frame. The D OUT is data that comming out from the camera. It have low requirement on the trace and sample interface design. However, it can not offer long distence transmission and high speed clock. It usually use at low end 240p camera.

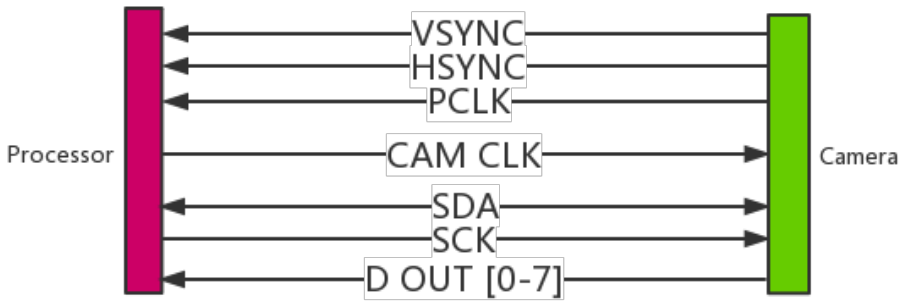

Figure 3: Physical Layer for DVP Interface

4.3 LVDS Interface

The LVDS camera interface is use LVDS technology to improve classic DVP interface. It use differential signal to transmitting data. It increase the lane it need to send data, but differential signal can prevent common mode interference which limit the DVP clock for increasing.

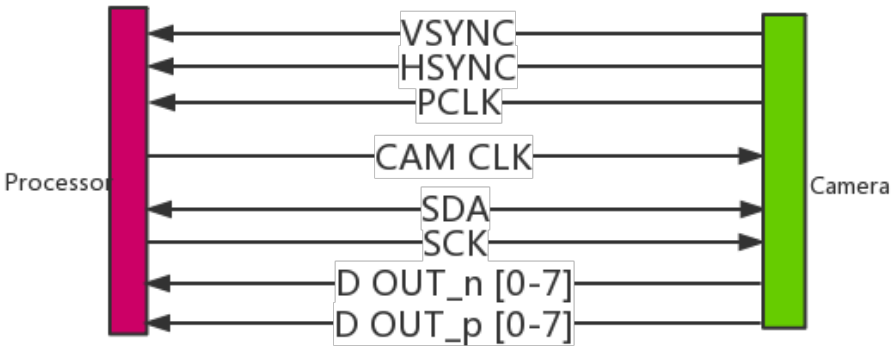

Figure 4: Physical Layer for LVDS Interface

4.4 MIPI CSI-2 Interface

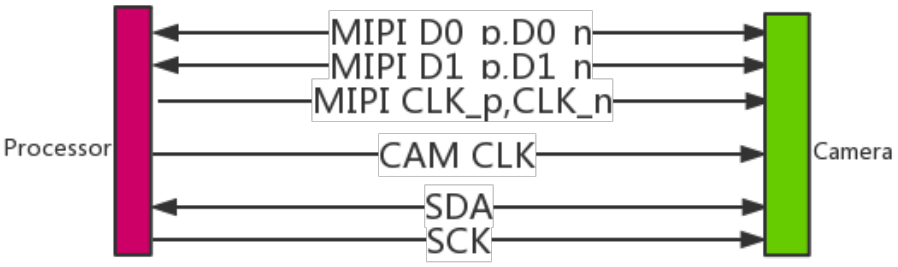

Figure 5: Physical Layer for 2 Lane MIPI Interface

5 H.264 Video Steam Encoding

5.1 Introduction

5.2 IP core Description

6 File System and Video Storage

6.1 Introduction

6.2 NVME Drive

6.3 Flash (QSPI Mode)

6.4 SD Cord(SPI Mode)

6.5 SD Cord(SD Mode)

7 System Diagram