



# ORBIT Avionics System II Architecture

Sys-Arch

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# 1 General Software System Architecture

The software system for OA-II can be divided to three layers: data link layer, Transport layer, and application layer.

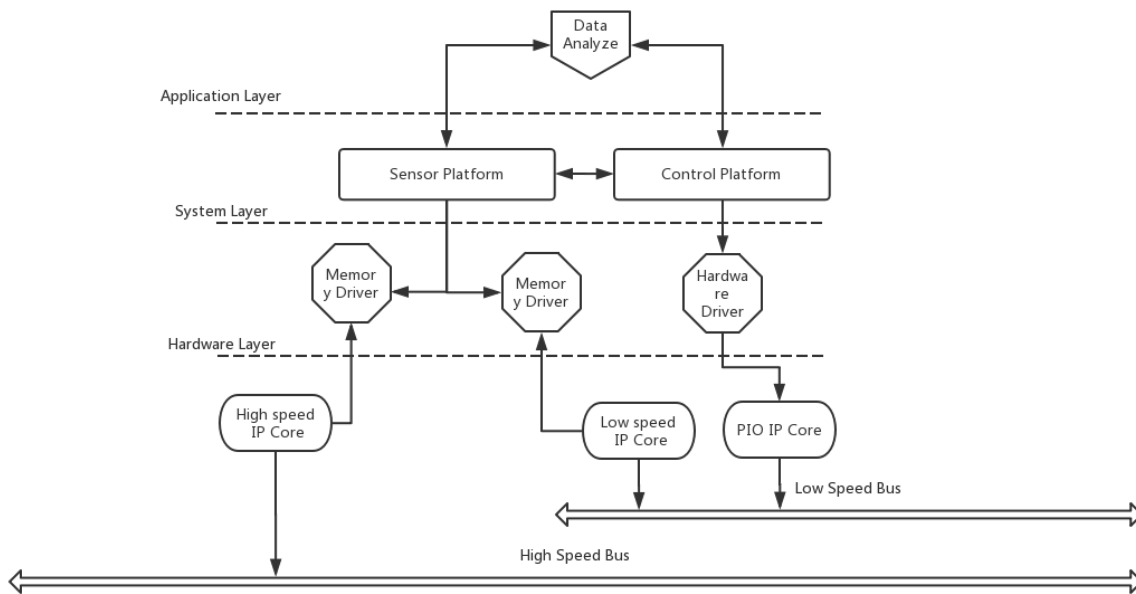


Figure 1: Software Architecture

## 1.1 Data Link Layer

The data link layer directly interacts with hardware memory. It include drivers for all hardware buses. It also includes programs which execute direction on the CPU.

## 1.2 Transport Layer

The transport layer connects the data link and application layers. It receives data from different data link layer sources and packetizes it. It will feed all the packetized data to relevant application program. It provides critical control before and during the flight. Finally, the transport layer records all data to onboard storage.

## 1.3 Application Layer

The application layer is used to process data provided by the transport layer, as well as to provide information that will be sent back to OA-II BAS.

## 2 General Hardware System Architecture

### 2.1 Payload Catalog

#### Critical Payload

The critical payload controls basic launch and recovery operations. It will attach directly to the Compute Module (CM). Any failure of the critical payload will result in a launch abort. The critical payload contains:

- Power management
- GPS receiver
- Low speed IMU
- Storage media
- Radio system

#### High Speed Payload

- The high speed payload contains non-critical devices, in particular sensors. This payload is primarily for research purposes. These devices will be located in the Telemetry Module (TM), and include:

- Static and dynamic air pressure sensors
- High speed IMU
- Cameras
- Temperature sensors
- Pressure sensors

#### Low Speed Payload

- The low speed payload contains non-critical devices which are significant EMI sources. The low speed payload must be fully galvanically isolated from the rest of the system. This includes:

- Actuators
- Pyrotechnics

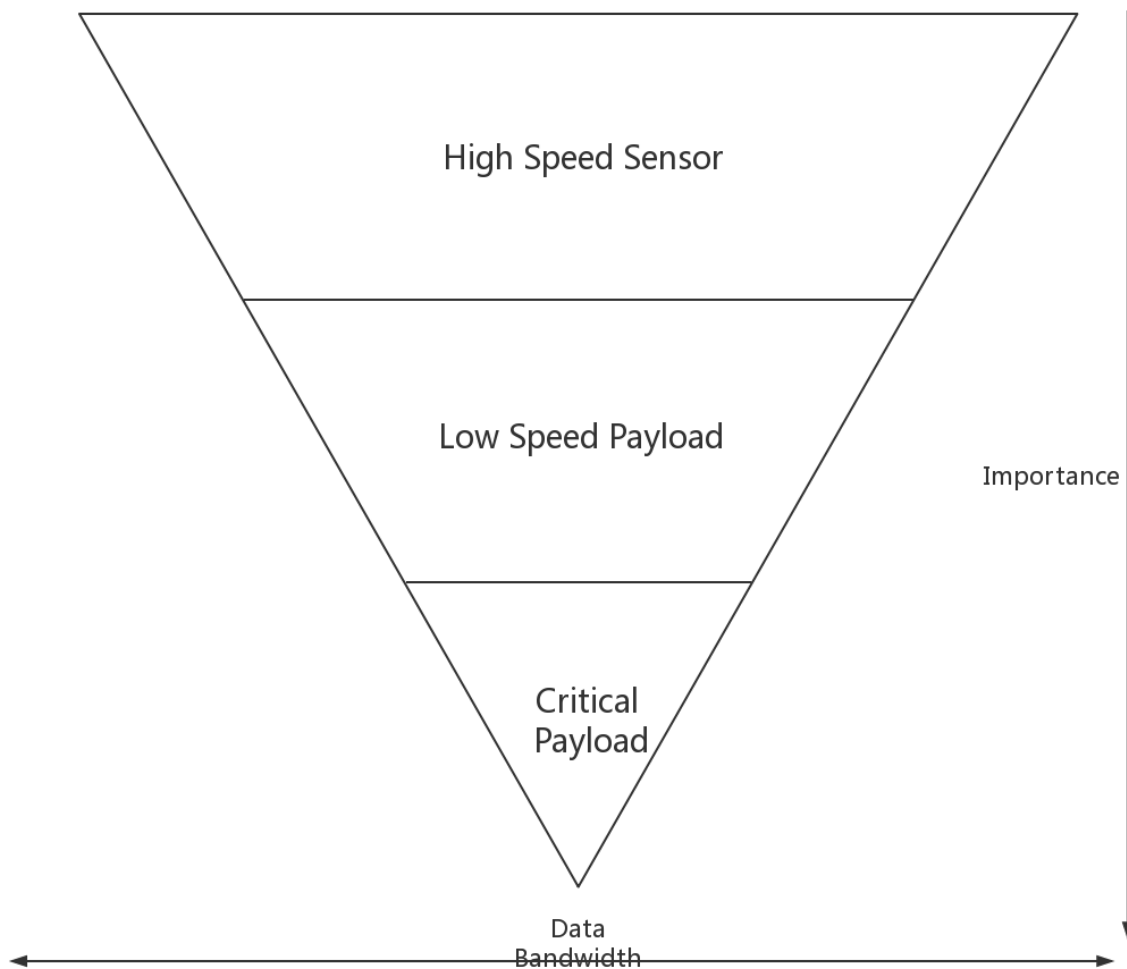


Figure 2: Payload Diagram

## 2.2 PCB Layout

## 2.3 High Speed Lane Protection

## 3 Vehicle Electronics (VEH) System Architecture

### 3.1 Description

The OA-II VEH is a compact, modular system which is tightly integrated with the flight vehicle.

### 3.2 Payload Frame (PF)

The Payload Frame (PF) contains interchangeable modules and provides a high speed bus controller and power supply. The PF should be a four layer board.

### 3.3 Payload Modules (PM)

Payload Modules are specialized circuits which slot into the Payload Frame. They can be divided into three primary types: Computing Modules (CM), Telemetry Modules (TM), and Actuator Modules (AM).

#### Compute Module (CM)

The Compute Module (CM) has several purposes. It controls other modules and monitors the vehicle status. It collects data from Telemetry Modules, and contains long-term storage for collected data.

#### Telemetry Module (TM)

The Telemetry Module (TM) is an interface to both sensors and radios. The TM connects to both low and high speed sensors. The TM also FIFO buffers for high speed sensors.

#### Actuator Module (AM)

TBD

## 4 Base Station Electronics (BAS) System Architecture

### 4.1 General Description

The OA-II BAS is a modular launch pad and flight control center. It performs three major functions: launch control operations, live data analysis and display, and vehicle status indication.

### 4.2 Launch Control

The Launch Control Module monitors and controls the vehicle before, during, and after flight. This includes ignition and oxidizer control, parameter tuning, and launch abort functionality.

### 4.3 Live Data

The Live Data Module shows vehicle information during flight. This includes a 3D map of the flight path, propulsion system temperatures and pressures, and IMU data.

### 4.4 Vehicle Status

The Vehicle Status Module performs basic analysis on the live telemetry data. This includes displaying a Range Safe/Range Live indication, vehicle orientation from sensor fusion, flight profile stages, and error monitoring.



## 5 Backplane System (BPS) Architecture

### 5.1 General Description

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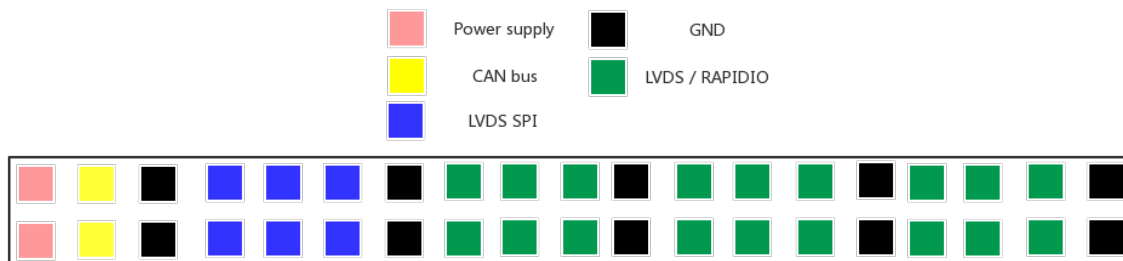


Figure 3: Example Pin Out

### 5.2 Software System Structure

### 5.3 Hardware System Structure

## **6 Wireless System (WLS) Architecture**

### **6.1 General Description**

**High Speed Wireless Connection Protocol**

**Low Power Wireless Connection Protocol**