OA-II Payload Modules Architecture

ES00005

Rev: A01
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1 Introduction

1.1   Scope

This document include the design detail of ORBiT Avionics System II Vehicle Electronics Payload Modules such as software and hardware structure and block diagram.

1.2   Purpose

The goal for this document is to come up a big picture for the OA-II system building.

1.3   Relevant Documents

ER00002 ORBiT Avionics System II Requirements

ES00002 ORBiT Avionics System II Architecture

ES00003 OA-II Vehicle Electronics (VEH) System Architecture

DR00001 OA-II Backplane Bus System

DR00002 OA-II VEH Camera System Design

DR00003 OA-II VEH COM System Design

DR00004 OA-II VEH TAM System Design

DR00005 OA-II VEH PAM System Design

1.4   Revision History

Rev	Author	Approver	Changes	Date
A01	Jinzhi Cai	Jinzhi Cai	Initial draft	2019-7-22

Table 1: Summary of Revision History

2 Computing and Operation Module

2.1   Main Control Unit

Main Control Unit contain:

- SoC FPGA that contain 80K LUT and 800MHz to 1GHz processor

- Power manager chip that convert 48V main power to the processor required standard

- Four low temperture sensors for electronics

- Three axis IMU for Spare

- Barometer for Spare

- 2Gbit DRAM for SoC

- 64GB Storage Media(SD card)

- Diagnosis Connector

The SoC FPGA will be use as the main processor and come with few sensor attach with it. Those sensor is monitor the status of the SoC FPGA and spare

2.2   Failure Recovery Unit

Failure Recovery Unit contain: [1]

- SoC FPGA that contain 80K LUT and 800MHz to 1GHz processor

- Power manager chip that convert 48V main power to the processor required standard

- Four low temperture sensors for electronics

- Three axis IMU for Spare

- Barometer for Spare

- 2Gbit DRAM for SoC

- 64GB Storage Media(SD card)

- Diagnosis Connector

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[1] The same with the MCU

2.3 Sensor Fusion Unit

TBD

3 Telecommunication and Acquisition Module

4 Power and Actuator Module