OA-II Backplane Bus System Design

DR00001

Rev: A01

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1 Introduction

1.1 Scope

This document analyze the requirement for OA-II VEH system data transmission, and current bus technology in the field, come up with a system design to fullfill the need of OA-II VEH system.

1.2 Purpose

The goal for the OA-II backplane bus system is constructure a high speed, high compatibility, and high robustness backplane data transmission system.

2 Revision History

Rev#	Editor	Delta	Date
A01	Jinzhi Cai	Initialize	2019-7-15

Table 1: Summary of Revision History

3 BUS System Requirement

3.1 Hardware Requirement

Backplane Bus The bus need to suppport swappable module

Vribation-proof The bus need to have stronge support to the module on the frame.

Size The size need to fit into the rocket.

Topology The hardware structure need to support out-of-order locating.

3.2 Software Requirement

Point to Point & Broadcast The bus need to support broadcast.

Bandwidth The bus need to support the max bandwidth.

Topology The bus need to allow change in software topology.

Real Time The bus need to support message priority level.

Various Speed The bus need to allow low end device connect into the system.

3.3 Bandwidth Calculation

Low Speed Payload Each low speed payload it sensing in 10kHz 16bit

- 4 high pressure sensors for propulsion system
- 2 low pressure sensors for pitot tube
- 4 high temperature sensors for propulsion system
- 4 low temperature sensors for electronics
- 4 low temperature sensors for batteries
- 2 low temperature sensor for ambient

$$4 + 2 + 4 + 4 + 4 + 2 = 20chennals$$
$$10kHz = 10000Hz$$
$$16bit = 2byte$$
$$10000Hz \times 2byte = 20000byte/s = 20Kbyte/s$$
$$20Kbyte/s \times 20 = 400Kbyte/s$$

High Speed Payload

- 9 axis IMU
- GNSS
- 4x cameras

9 axis IMU in 10kHz is

$$9 \times 10000Hz \times 2byte = 180000byte/s = 180Kbyte/s$$

GNSS module[1]

UTC launch time 4byte

Latitude 4byte

Longitude 4byte

Height 4byte

Direction+Ground speed 4byte

$$4byte \times 5 = 20byte$$

$$10Hz \times 20byte = 200byte/s$$

Camera, set the bitrate to 8Mbps[2]

$$8Mbps = 1Mbyte/s$$

$$1Mbyte/s \times 4 = 4Mbyte/s$$

Total bandwidth

$$(180Kbyte/s + 4Mbyte/s + 200byte/s + 400Kbyte/s) \times 2 \approx 10Mbyte/s$$

[1] Did not include any fixing factor

[2] High bitrate is nessary for high virbation environment

4 Current Bus Analyze

4.1 I2C

I2C is a serial protocol for two-wire interface to connect low-speed devices like microcontrollers, EEPROMs, A/D and D/A converters, I/O interfaces and other similar peripherals in embedded systems. It was invented by Philips and now it is used by almost all major IC manufacturers.[**?**]

I2C is a great low speed communication bus, however it do not support hardware priority level and change software topology.

4.2 SPI

Serial Peripheral Interface (SPI) is an interface bus commonly used to send data between microcontrollers and small peripherals such as shift registers, sensors, and SD cards.[**?**]

Serial Peripheral Interface allow device to increase the bandwidth by increase the data clock rate. However, it also not support hardware priority level and change software topology.

4.3 UART

A universal asynchronous receiver-transmitter is a computer hardware device for asynchronous serial communication in which the data format and transmission speeds are configurable.[**?**]

UART bus do not require clock line to transmit data. It also have different bitrate allow device to change. However it is a point to point communication, so it need switch for more than two devices. It also too low to meet the bandwidth requirement.

4.4 CAN

A Controller Area Network (CAN bus) is a robust vehicle bus standard designed to allow microcontrollers and devices to communicate with each other in applications without a host computer.[**?**]

The CAN bus have hardware priority level and support 500kbps[3] bandrate. It also allow group boardcast and point to point communication.

[3] About 62.5Kbyte/s

4.5 PCIe

PCI Express, officially abbreviated as PCIe or PCI-e, is a high-speed serial computer expansion bus standard, designed to replace the older PCI, PCI-X and AGP bus standards. It is the common motherboard interface for personal computers' graphics cards, hard drives, SSDs, Wi-Fi and Ethernet hardware connections.[**?**]

The PCI Express is a common use buses in personal computer. However, the topology of this bus is mostly tree structure. It will increase difficulty when a second master need to add into the system.

4.6 RapidIO

The RapidIO architecture is a high-performance packet-switched interconnect technology. RapidIO supports messaging, read/write and cache coherency semantics.[**?**]

The RapidIO is a high speed connection that support up to 5Gbps[4] by a single lane. It also support multi-master structrue. By using RapidIO switch, it could change the software topology. However, the rapidIO is a new bus technology that mainly use in DSP, high speed FPGA, and SoC. It require heavy hardware resource compare with the other kind of buses.

4.7 SpaceWire

SpaceWire is defined in the European Cooperation for Space Standardization standard ECSS-E-ST-50-12C (replaces ECSS-E50-12A). The SpaceWire standard was authored by Steve Parkes, University of Dundee with contributions from many individuals within the SpaceWire Working Group from European Space Agency (ESA), European Space Industry, Academia and NASA.[**?**]

The SpaceWire is use LVDS voltage standard which is a commonly use voltage standard in FPGA. The PHY for SpaceWire is relativly simple and require less resource for constructe the PHY. The newest SpaceWire bus support 400Mbps for one lane[5].

4.8 Interlaken

Interlaken was invented by Cisco Systems and Cortina Systems in 2006, optimized for high-bandwidth and reliable packet transfers. It builds on the channelization and per channel flow control features of SPI-4.2, while reducing the number of integrated circuit (chip) I/O pins by using high speed SerDes technology.[**?**]

Interlaken is a bus deisgn for the replace the ethernet. It also support port division and flow

[4] About 625Mbyte/s
[5] About 50Mbyte/s

control. However, the Interlaken PHY do not support in most of the FPGA. It mean it will require extra chip for PHY. It have the similar speed with RapidIO[6].

[6] About 625Mbyte/s

5 OA-II Bus Structure

Base on the requirement of the bus, the OA-II Bus System will include two part, the command bus which incharge of the initialization of another bus and the prioritize data transmission, the data bus which incharge the transmission of large amout of data and program.

5.1 CAN + SpaceWire

Command Bus CAN

Data Bus SpaceWire

In this plan, the command bus is using CAN. It provide prioritize data transmission for small amount data transmission. Up to 500kbps bandwidth provide enough bandwidth for command data transmission. The data bus is using the SpaceWire which provide enough bandwidth for high speed data transmission. It also include timestamp feature that will help for the future sensor fusion.

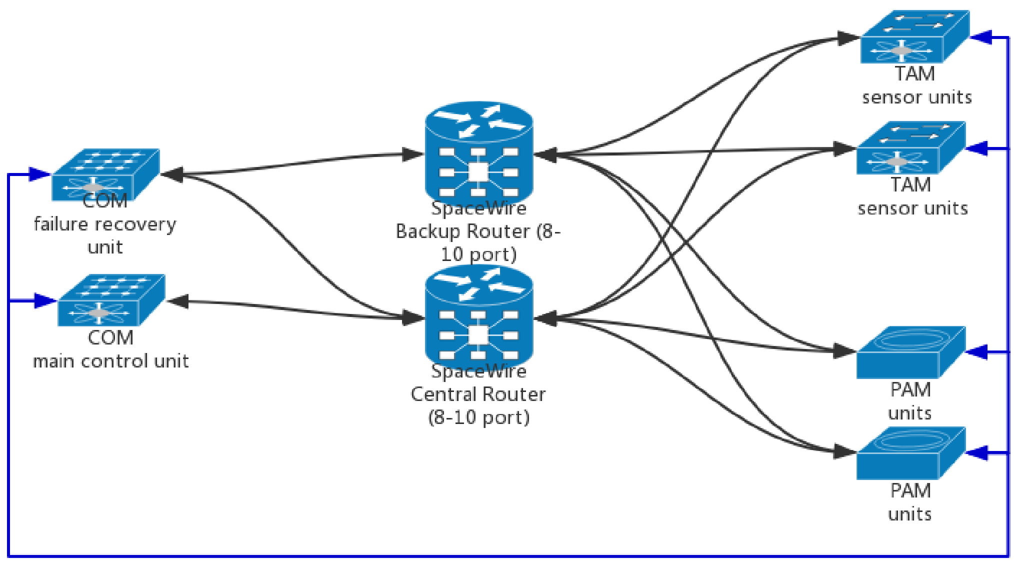

Figure 1: Physical Layer for DVP Interface

5.2 CAN + RapidIO

Command Bus CAN

Data Bus RapidIO

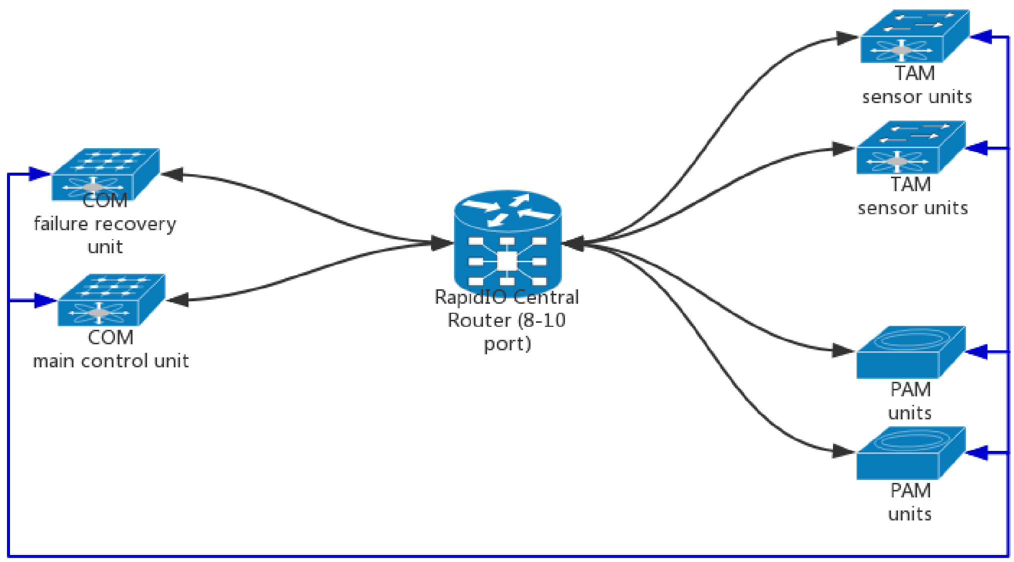

Figure 2: Physical Layer for DVP Interface