GMSL Camera Board Hardware Design Guide

1、Gemini 335Lg Camera

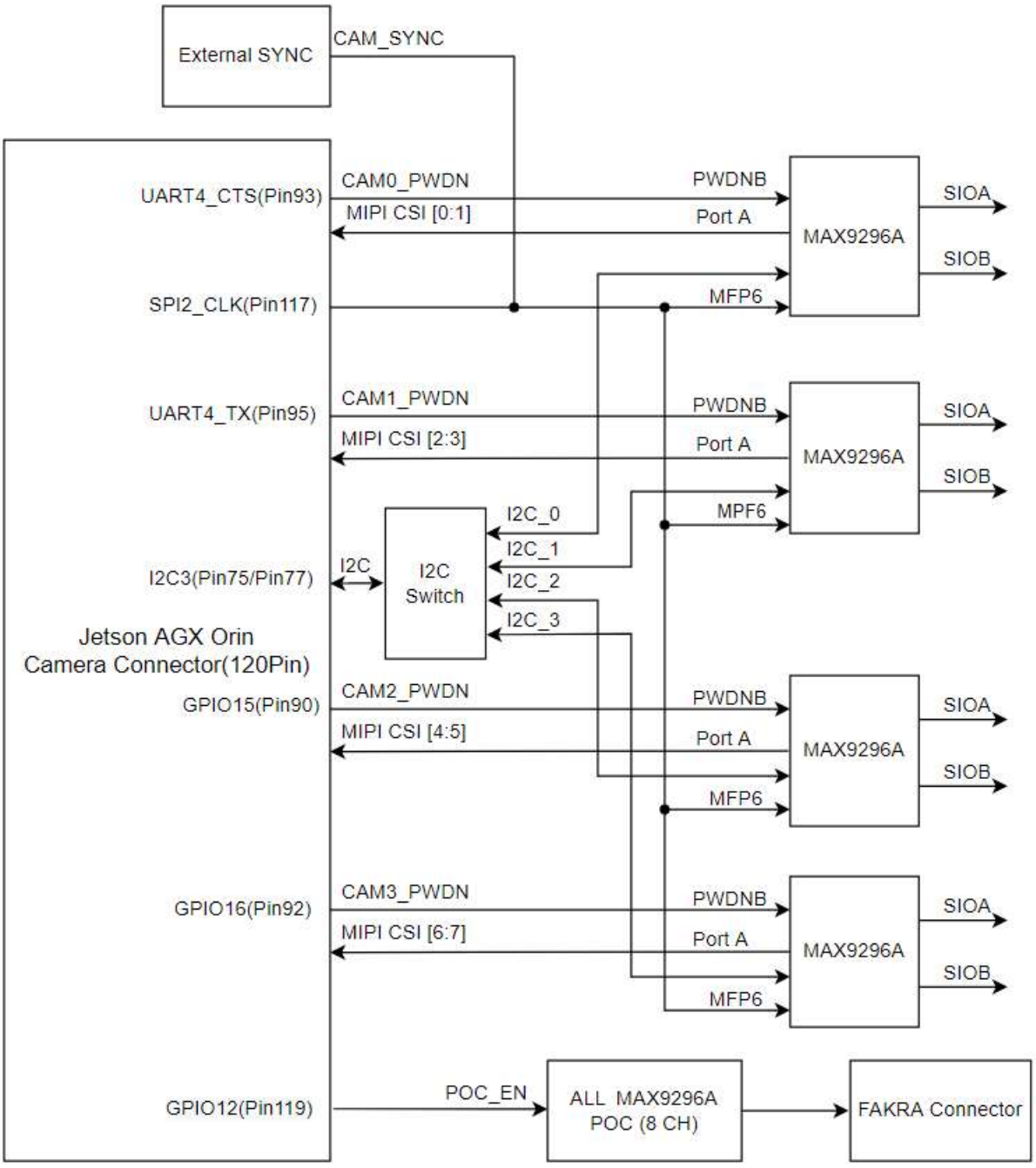
（1）Hardware Setting

Serializer IC： MAX9295D
Communication interface：I2C
I2C address：0x80
Link type：Coaxial
GMSL：GMSL2
Rate：6Gbps
Power supply：POC power supply, voltage 12 ± 1V, current ≥ 750mA.

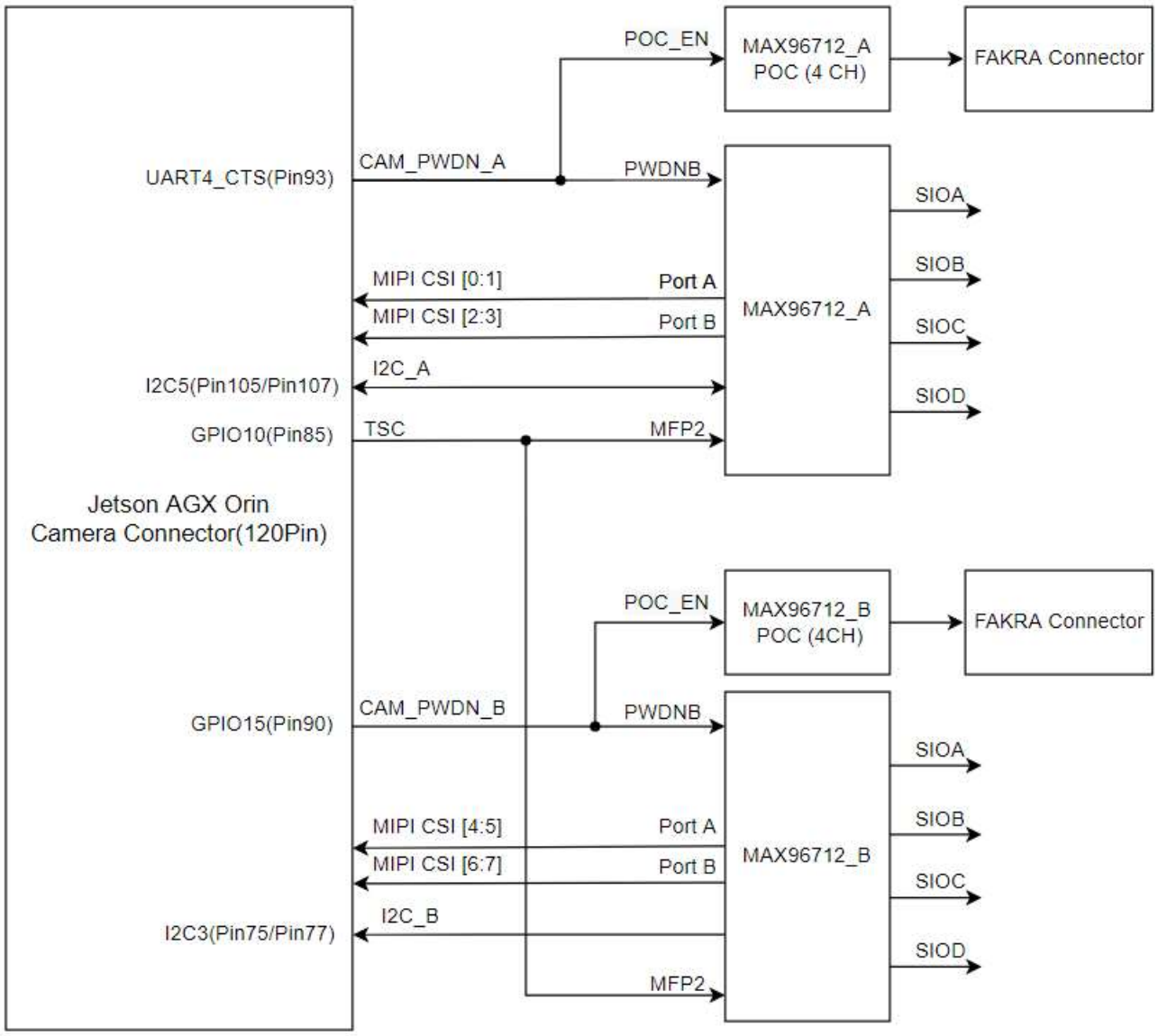
（2）Serializer IC MAX9295D GPIO description

Pin name	I/O	Definition	Function Description
MFP0	O	SPI_CLK	SPI clock, with The serializer IC acts as the master and the camera ASIC acts as the slave.
MFP1	O	SPI_MOSI	Master output，slave input. The serializer IC acts as the master, while the camera ASIC acts as the slave.
MFP2	I	SPI_MISO	Slave output，master input. The serializer IC acts as the master, while the camera ASIC acts as the slave.
MFP3	O	WAKE	Camera enters sleep mode and wakes up when the high level is active.
MFP4	I	CFG0	Configuration of the working mode of The serializer IC.
MFP5	I	CFG1	Configuration of the working mode of The serializer IC.
MFP6	O	SYNC_IN	Multi-machine synchronization SYNC_IN, The serializer IC outputs to the ASIC, high pulse valid, pulse width ≥ 1ms.
MFP7	O	PPS	PPS second pulse signal, high pulse valid, pulse width ≥ 1ms.
MFP8	O	RESTART	Camera power switch control: Low level turns on the camera power, high level turns off the camera power. Power-on defaults to turning on the camera.
MFP9	I	SYNC_OUT	Multi-machine synchronization SYNC_OUT,The ASIC outputs to The serializer IC,high pulse valid, pulse width ≥ 1ms.
MFP10	O	SPI_CS	SPI chip select. The serializer IC acts as the master, while the ASIC acts as the slave.
MFP11	I	Timer_OUT	Timestamp reset Timer_OUT, The ASIC outputs to The serializer IC.
MFP12	O	Timer_IN	Timestamp reset Timer_IN, The serializer IC outputs to The ASIC.
MFP13	/	/	/
MFP14	/	/	/
MFP15	O/I	I2C_SDA	I2C_SDA(Master)
MFP16	O	I2C_SCL	I2C_SCL(Master)

2、GMSL Camera Board Hardware Design Guide



MAX9296A GMSL Camera Board block diagram



MAX96712 GMSL Camera Board block diagram

（1）The MIPI CSI 4-lane output of the MAX9296A Port A interface is connected to the Jetson AGX orin (the specific connection method can be referred to in the schematic diagram or the reference driver code device tree). The MIPI CSI 4-lane outputs of the MAX96712 Port A and Port B interfaces are also connected to the Jetson AGX orin (the specific connection method can be referred to in the schematic diagram or the reference driver code device tree). The reference driver code is configured as 4 lanes, with a rate of 1.5 Gbps per lane, and the data lanes D0 to D3 are connected in sequence without any reversal, and the differential polarity does not flip. (Note: If the MIPI CSI is configured as 2 lanes, there may be a risk of insufficient bandwidth.)

（2） The POC power switch control of the GMSL port can be implemented through either centralized control or independent control methods. In the centralized control method, only one IO resource is required to control all the GMSL port POC power switches. In the independent control method, for each GMSL output port, several IO ports are needed to independently control the power switch of each GMSL output port.

Centralized control method: If the number of GMSL ports is greater than 2, it is recommended to design a ramp-up circuit for POC power supply, with the ramp-up time not less than 5ms. At the same time, for each POC output, it is recommended to design a current-limiting IC (such as TPS25961 from IT company) to prevent short

circuits in the subsequent stage from damaging the circuit board. The recommended current-limiting value is 1A (note: the current-limiting value needs to be adjusted according to the selection of the POC inductor).

Independent control mode: It is necessary to use a software to control the GMSL port POC power to be turned on in a time-sharing manner, with an interval time greater than 20ms.

（3）For the selection of POC inductors, please refer to the official recommendation list of ADI. For details, please see *gmsl2-hardware-design-guide* pages 49-50. If you choose the inductors by yourself, you need to comply with the ADI GMSL design specifications. Since the POC circuit is a combination of multiple inductors, the load capacity of each inductor must not be lower than 800mA (12±1V).

（4）The hardware design of the GMSL channel must comply with Analog Devices' design specifications outlined in the *gmsl2-channel-specification--guide* and *gmsl2-hardware-design-guide*.

（5）For the selection of Fakra cables, please refer to the "Cable Design Guide" in the *Gemini-335Lg-Datasheet* document.