2.1)
Total clock cycles = 45,000 + 64,000 + 30,000 + 16,000 = 155,000 cycles
Effective CPI = Total instructions/Total clock cycles = 155,000/100,000 = 1.55

So, the **effective CPI** is **1.55 cycles per instruction**.

F = 40MHz = 40×10^6Hz = 40,000,000cycles/second
Execution time (T) = Total clock cycles / Frequency = 155,000/ 40,000,000 seconds
0.003875seconds × 1000 = 3.875milliseconds(ms)
So, the **execution time** is **3.875 ms**.
MIPS = Frequency / CPI × 10^ 6
MIPS = (40×10^6)/(1.55×10^6) = 40/1.5540
MIPS ≈ 25.8

Final Answers:

- **Effective CPI**: **1.55 cycles per instruction**
- **MIPS rate**: **25.8 million instructions per second**
- **Execution time**: **3.875 milliseconds**

2.2)

Metric	Machine A	Machine B
Instruction mix	8 M ALU, 4 M LS, 2 M BR, 4 M Other	10 M ALU, 8 M LS, 2 M BR, 4 M Other
Total instructions	8+4+2+4 = 18 M	10+8+2+4 = 24 M
Total cycles	8·1 + 4·3 + 2·4 + 4·3 = 40 M	10·1 + 8·2 + 2·4 + 4·3 = 46 M
Effective CPI	40 M / 18 M ≈ 2.22	46 M / 24 M ≈ 1.92
MIPS rating	200 MHz / 2.22 ≈ 90 MIPS	200 MHz / 1.92 ≈ 104 MIPS
Execution time	40 M cycles / (200 M cycles/s) = 0.20 s	46 M cycles / (200 M cycles/s) = 0.23 s

Comment on the results:

- **Machine B** has the lower CPI (1.92 vs. 2.22) and so boasts a higher MIPS rating (≈104 MIPS vs. 90 MIPS).
- **However**, it also requires more instructions (24 M vs. 18 M), so its total execution time (0.23 s) is actually **longer** than Machine A's (0.20 s).

- **Takeaway:** MIPS (or CPI alone) can be misleading when comparing different ISAs or code mixes. The true performance metric is **wall-clock time**, which depends on both **instruction count** and **CPI**.

2.7)

Instr. class	Mix	Orig. CPI	New CPI
Arithmetic & logic	60%	1	1
Load/store (cache hit)	18%	2	2
Branch	12%	4	4
Memory reference (cache miss)	10%	8	12

a. Average CPI

$\mathbf{CPI_{avg}} = 1 \times 0.60 + 2 \times 0.18 + 4 \times 0.12 + 12 \times 0.10 = 0.60 + 0.36 + 0.48 + 1.20 = \mathbf{2.64}$

b. MIPS rate

MIPS = clock(MHz) / $CPI_{avg} = 2.64\ 400 \approx \mathbf{151.5MIPS}$

c. Speedup factor

- **Single-core time**

$\mathbf{T_1} = IC / MIPS_{orig} \times 106 = 178 \times 1062000000 \approx 0.01124s$

- **Eight-core time**: each core executes

$\mathbf{T_8} = 400 \times 106 \times 275000 / CPI_{avg} = 400 \times 1062.64 \times 275000 \approx 0.001815s$

- **Speedup**

$\mathbf{S} = T_1 / T_8 \approx 0.01124 / 0.001815 \approx \mathbf{6.19}$

d. Amdahl's-law comparison

With perfect parallelism (no overhead), an 8-core system would give an ideal $S = 8$. Here the actual speedup is ≈ 6.19, i.e. about 77 % of the theoretical maximum. This loss comes from extra coordination instructions and increased memory-access latency under contention.

2.9)

By Little's Law ($L = \lambda W$), the average time in system is

$W = L / \lambda = 8$ customers/(18 customers/hour) = 0.444hours ≈ 26.7minutes.

So on average each customer spends about **26 minutes 40 seconds** in the shop.