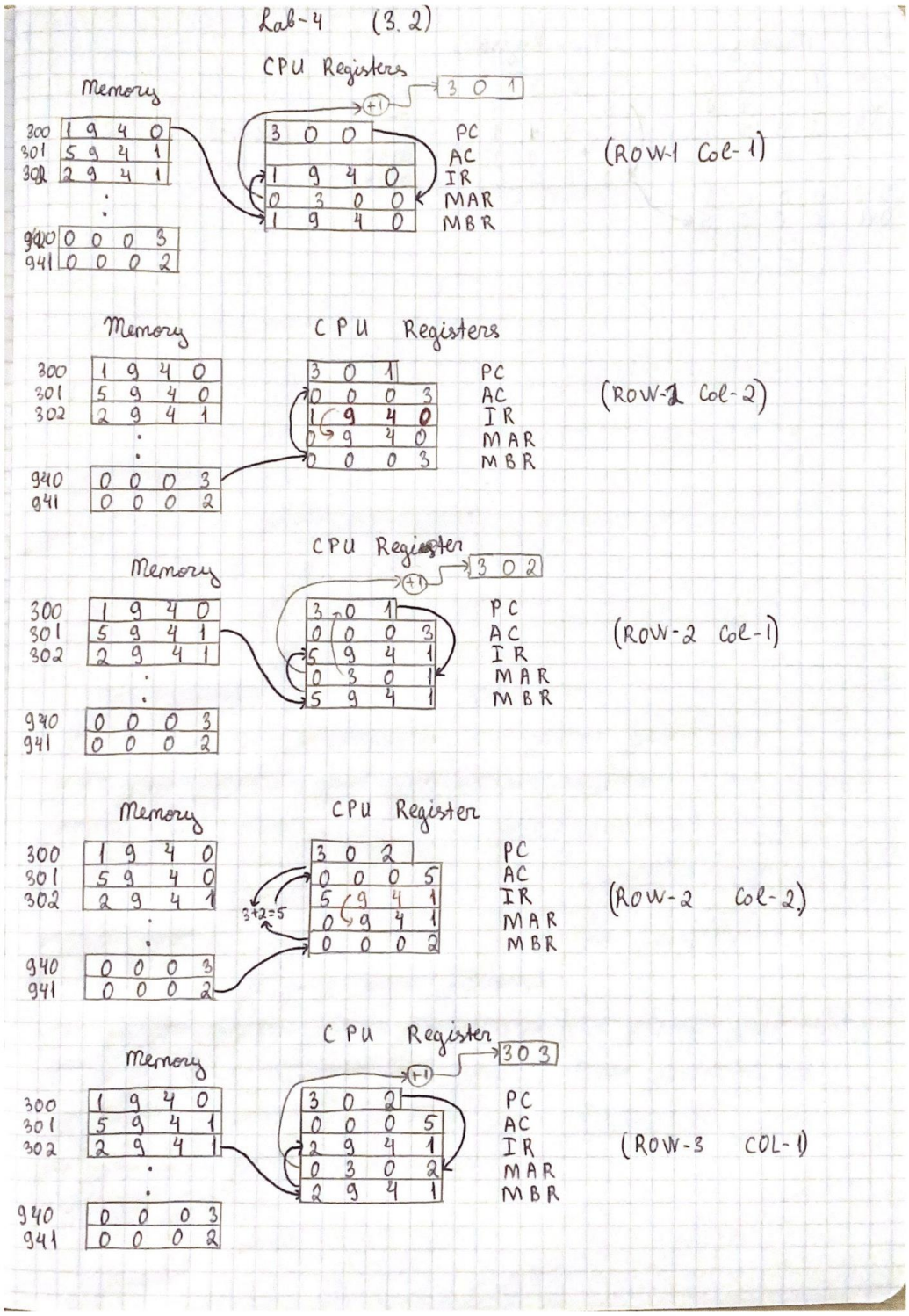
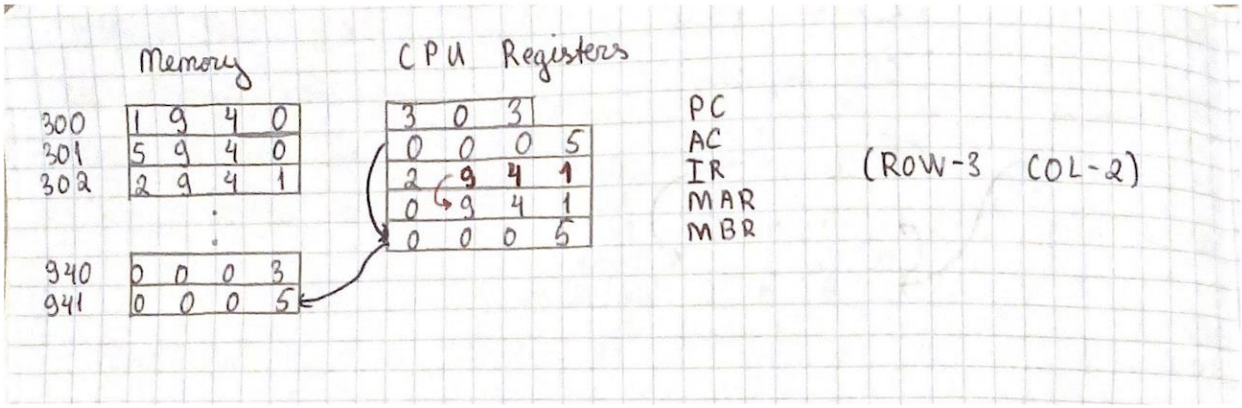
3.2)


Lab-4 (3.2)
CPU Registers
Memory
300 1 9 4 0
301 5 9 4 1
302 2 9 4 1
940 0 0 0 3
941 0 0 0 2
3 0 1
3 0 0
1 9 4 0
0 3 0 0
1 9 4 0
PC
AC
IR
MAR
MBR
(ROW-1 Col-1)
Memory
CPU Registers
300 1 9 4 0
301 5 9 4 0
302 2 9 4 1
940 0 0 0 3
941 0 0 0 2
3 0 1
0 0 0 3
1 9 4 0
0 9 4 0
0 0 0 3
PC
AC
IR
MAR
MBR
(ROW-2 Col-2)
Memory
CPU Register
300 1 9 4 0
301 5 9 4 1
302 2 9 4 1
940 0 0 0 3
941 0 0 0 2
3 0 2
3 0 1
0 0 0 3
5 9 4 1
0 3 0 1
5 9 4 1
PC
AC
IR
MAR
MBR
(ROW-2 Col-1)
Memory
CPU Register
300 1 9 4 0
301 5 9 4 0
302 2 9 4 1
940 0 0 0 3
941 0 0 0 2
3+2=5
3 0 2
0 0 0 5
5 9 4 1
0 9 4 1
0 0 0 2
PC
AC
IR
MAR
MBR
(ROW-2 Col-2)
Memory
CPU Register
300 1 9 4 0
301 5 9 4 1
302 2 9 4 1
940 0 0 0 3
941 0 0 0 2
3 0 3
3 0 2
0 0 0 5
2 9 4 1
0 3 0 2
2 9 4 1
PC
AC
IR
MAR
MBR
(ROW-3 COL-1)



3.3)

a) 2^24 = 16 Mega Bytes

b) 1. If the address bus spans 32 bits, the processor can put the entire address on the bus in a single cycle for memory decoding. But because the data bus is limited to 16 bits, fetching a 32-bit instruction or operand still takes two consecutive data-transfer cycles.

2. Because only 16 address lines are available, you can't send the full 24-bit address at once. The memory interface must therefore capture the upper half of the address, then the lower half, before it can locate the word. After the complete address is assembled, the 16-bit data bus still requires two back-to-back transfers to retrieve the full 32-bit instruction or operand.

3. The program counter requires a minimum width of 24 bits. The instruction register is normally 32 bits wide.

3.6)

a) The teletype places an incoming character into INPR only when FGI=0. Once the character arrives, INPR is loaded and FGI is raised to 1. The CPU repeatedly polls FGI (since interrupts are disabled): when it sees FGI=1, it moves the byte

from INPR into the accumulator and resets FGI to 0. For output, the CPU watches FGO: if FGO=0, the printer is busy and the CPU waits; once FGO=1, the CPU writes the accumulator's contents into OUTR and then clears FGO to 0.

b) Polling in (a) forces the fast CPU to loop endlessly reading FGI and FGO, even though the teletype works much more slowly. By turning on interrupts via the IEN bit, the I/O module itself will signal the CPU whenever the teletype is ready to send or receive data, so the processor no longer has to waste time checking those flags.