EE5134: Digital IC Design

Final Project: Interim Report

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Selected Standard Cells:

1. INVX4 (Completed)
2. NOR2X1 (Completed)
3. AOI21X1 (Completed)
4. DFFPOSX1 (In Progress)

Procedure Adopted:

- The spice net-list of the base inverter.mag file that was provided was extracted in order to find the drive strength of the reference inverter. It is this drive strength (rise and fall time) which needs to be matched for in the cells that are being designed.
- To find the drive strength of the inverter we need to choose a value for the load capacitance, this value has been chosen to be 500fF, a value which is much greater than the diffusion capacitances of the transistors used in the cells. This is because the drive strength of a unit is defined on the basis of the load which is being driven by it, and a dominant load, with respect to the internal capacitances, would be the correct way to go about calculating the same.
- After the load capacitor value is set to 500fF the inverter is analyzed for its rise and fall time. The average of this rise and fall time is calculated and is set as the value for the drive strength. It is this value (in its near proximity) that is needed to be obtained by the cell that is being designed in order for it to qualify as an acceptable design.
- To qualify any standard cell as X2, it should produce the worst case rise and fall times close to the reference inverter values, for a load that is two times that used for the reference inverter (i.e. 1pF). Similar procedure is used to qualify a standard cell as X4, X8 etc.
- The value of the drive strength is noted and the design of the cell is initially done on SpiceOpus. Various parameters such as the widths of the PMOSs and NMOSs are varied so as to match the drive strength of the cell to that of the inverter.
- When an acceptable value for the drive strength is seen, the dimensions of the transistors are noted and the circuit layout is then designed in Magic.
- After the circuit design is done in Magic, the spice net-list of the same is extracted and is put back in SpiceOpus and is tested for various combinations of inputs so as to verify the drive strength that has been initially obtained by simulating it in SpiceOpus alone.
- If there is any unacceptable margin of change between the drive strengths of the basic inverter and the drive strength of the cell then the sizes are changed again so as to obtain a better value and the process is repeated. This sort of iteration is done until the value obtained for the drive strength is acceptable.
- Once we obtain the required design the cell is tested for various parameters such as power, rise time and fall time, by testing it for all the possible combinations of inputs. This is also done across different values of load capacitances and input pulse rise times.The values that are obtained are tabulated.

Reference Inverter:

The Inverter of size X1 was provided with PMOS size 20λ and NMOS size 10λ. For 500fF load, the rise time of the reference inverter = 0.83852ns and the fall time 0.8886ns.

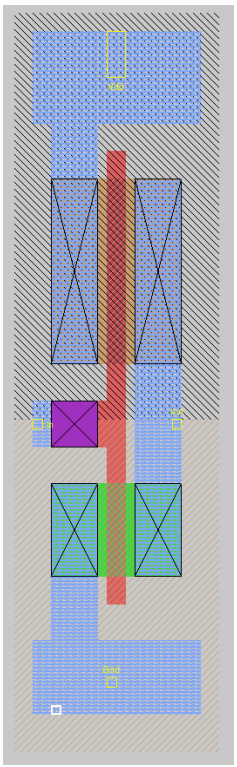

Figure 1: Layout of the inverter in MAGIC

1. INVX4:

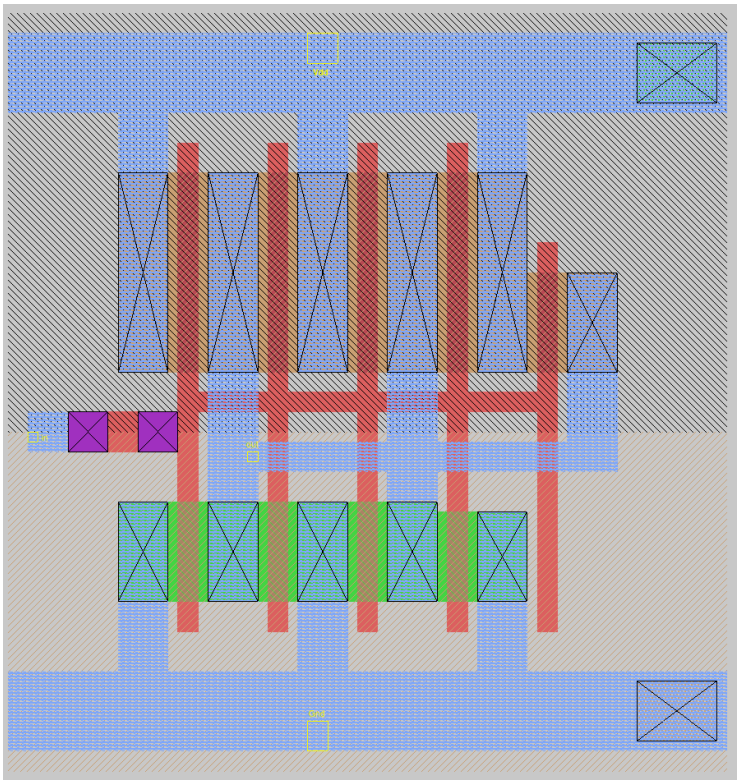

Figure 1: Layout of the INVX4 in MAGIC

Logic Expression: $Y = \bar{A}$

Truth Table

A	Y
0	1
1	0

Port Definitions

A	Input
Y	Output

Timing characterization (all delays are in ns)

	A:0 to 1			A:1 to 0		
$T \downarrow \backslash C_L \rightarrow$	0.005pF	0.025pF	0.15pF	0.005pF	0.025pF	0.15pF
0.06ns	0.02447	0.03498	0.09134	0.02715	0.03695	0.09389
0.42ns	0.03329	0.05493	0.14268	0.0603	0.08165	0.16785
1.2ns	0.02782	0.06084	0.19017	0.1071	0.1405	0.2682

Power characterization (all entries are in pJ)

	A:0 to 1			A:1 to 0		
$T \downarrow \backslash C_L \rightarrow$	0.005pF	0.025pF	0.15pF	0.005pF	0.025pF	0.15pF
0.06ns	0.0375	0.0403	0.0464	0.1058	0.1715	0.5826
0.42ns	0.0721	0.0636	0.0381	0.1457	0.2049	0.5972
1.2ns	0.1705	0.1600	0.1203	0.2512	0.3053	0.6756

Static Power Dissipation:

A	Static Power (pW)
0	131.352
1	73.848
Average Power	102.6

Extracted and modified SPICE Netlist:

```
SIMULATION OF INVERTER

* Reference inverter simulation

* Include
.include tsmc180.lib

.option scale=0.09u

.param TESTTS=2n
.param TESTTON=1n
.param TDELAY=200p
.param TESTRISE=0.06n

* Voltage sources
Vs Vdd 0  dc 1.8v
Vt in 0  pulse ( 0, 1.8, {TDELAY}, {TESTRISE}, {TESTRISE}, {TESTTON}, {TESTTS} )

* CMOS inverter

M1000 out in Vdd  Vdd  cmosp w=20 l=2
+ ad=270 pd=108 as=320 ps=138
M1001 Vdd  in out Vdd  cmosp w=20 l=2
+ ad=0 pd=0 as=0 ps=0
M1002 out in Vdd  Vdd  cmosp w=20 l=2
+ ad=0 pd=0 as=0 ps=0
M1003 Vdd  in out Vdd  cmosp w=10 l=2
+ ad=0 pd=0 as=0 ps=0
M1004 out in 0 0 cmosn w=10 l=2
+ ad=130 pd=66 as=130 ps=66
M1005 0 in out 0 cmosn w=10 l=2
+ ad=0 pd=0 as=0 ps=0
M1006 out in 0 0 cmosn w=10 l=2
+ ad=0 pd=0 as=0 ps=0

c1 out 0 500f

* Control area
.control

destroy all
```

```
tran 1p 20n

let c1=0
let c2=0
let c3=0
let c4=0
let midpoint=1.8/2.0

plot v(out) v(in) vs time

cursor c1 right v(out) midpoint 1 falling
cursor c2 right v(in) midpoint 1 rising
print time[%c2]- time[%c1]
cursor c3 right v(out) midpoint 1 rising
cursor c4 right v(in) midpoint 1 falling
print time[%c4]- time[%c3]

.endc

.end
```

2. NOR2X1:

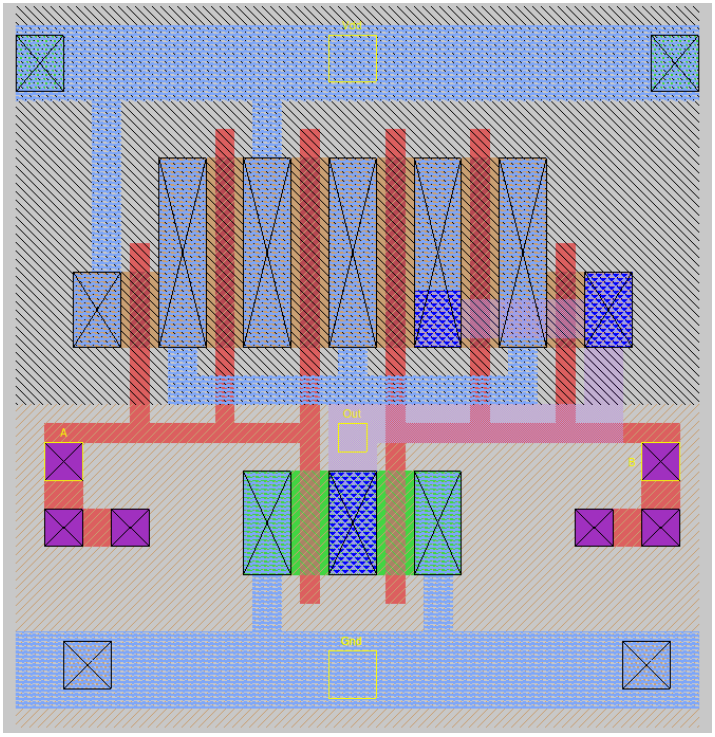

Figure 1: Layout of the NOR2X2 in MAGIC

Logic Expression: $Y = \overline{A + B}$

Truth Table

A	B	Y
0	0	1
0	0	0
0	1	0
0	1	0

Port Definitions

A	Input
B	Input
Y	Output

Timing characterization (all delays are in ps)

	A:0 to 1, B= 0			A:1 to 0, B= 0		
$C_L \downarrow \backslash T \rightarrow$	.06ns	.42ns	1.2ns	.06ns	.42ns	1.2ns
0.005pF	43.558	76.025	274.461	48.270	82.521	282.526
0.025pF	61.190	109.385	318.815	86.200	134.100	340.950
0.15pF	75.700	148.205	409.245	130.650	196.850	470.700

	B:0 to 1, A= 0			B:1 to 0, A= 0		
$C_L \downarrow \backslash T \rightarrow$	.06ns	.42ns	1.2ns	.06ns	.42ns	1.2ns
0.005pF	36.143	69.727	269.665	36.127	71.092	272.236
0.025pF	66.850	122.155	334.580	58.600	114.450	328.700
0.15pF	104.610	186.575	476.855	77.150	159.450	452.750

Power characterization (all entries are in pJ)

	A:0 to 1, B= 0			A:1 to 0, B= 0		
$C_L \downarrow \backslash T \rightarrow$	.06ns	.42ns	1.2ns	.06ns	.42ns	1.2ns
0.005pF	0.02107	0.02177	0.05407	0.08291	0.08878	0.12443
0.025pF	0.02102	0.01816	0.04747	0.14874	0.15177	0.18207
0.15pF	0.02120	0.01774	0.02835	0.55498	0.55544	0.57157

	B:0 to 1, A= 0			B:1 to 0, A= 0		
$C_L \downarrow \backslash T \rightarrow$	.06ns	.42ns	1.2ns	.06ns	.42ns	1.2ns
0.005pF	0.01994	0.02128	0.05141	0.05881	0.06962	0.10334
0.025pF	0.01650	0.01793	0.04412	0.12452	0.13118	0.16041
0.15pF	0.01281	0.01277	0.02634	0.53238	0.53314	0.54961

Static Power Dissipation:

A	B	Static Power (pW)
0	0	67.8741
0	0	41.9351
0	1	54.0486
0	1	22.2120
Average Power		46.5175

Extracted and modified SPICE Netlist:

```
.include tsmc180.lib

.option scale=0.09u

* Voltage sources
Vs Vdd 0  dc 1.8v
Vq B 0 dc 0v
vin A 0 pulse ( 1.8, 0, 200p, .06n, .06n, 25n, 50n )

M1000 a_n50_n17 A Vdd Vdd cmosp w=8 l=2
+ ad=396 pd=162 as=188 ps=82
M1001 Vdd A a_n50_n17 Vdd cmosp w=20 l=2
+ ad=0 pd=0 as=0 ps=0
M1002 a_n50_n17 A Vdd Vdd cmosp w=20 l=2
+ ad=0 pd=0 as=0 ps=0
M1003 Out B a_n50_n17 Vdd cmosp w=20 l=2
+ ad=188 pd=82 as=0 ps=0
M1004 a_n50_n17 B Out Vdd cmosp w=20 l=2
```

```
+ ad=0 pd=0 as=0 ps=0
M1005 Out B a_n50_n17 Vdd cmosp w=8 l=2
+ ad=0 pd=0 as=0 ps=0
M1006 Out A 0 0 cmosn w=11 l=2
+ ad=77 pd=36 as=132 ps=68
M1007 0 B Out 0 cmosn w=11 l=2
+ ad=0 pd=0 as=0 ps=0

c1 Out 0 500f

* Control area
.control

destroy all
tran 1p 100n

let c1=0
let c2=0
let midpoint=1.8/2.0

plot v(Out) v(A) vs time

cursor c1 right v(Out) midpoint 1 rising
cursor c2 right v(A) midpoint 1 falling
print time[%c2] - time[%c1]

cursor c1 right v(Out) midpoint 1 falling
cursor c2 right v(A) midpoint 1 rising
print time[%c2]- time[%c1]

.endc

.end
```

3. AOI21X1

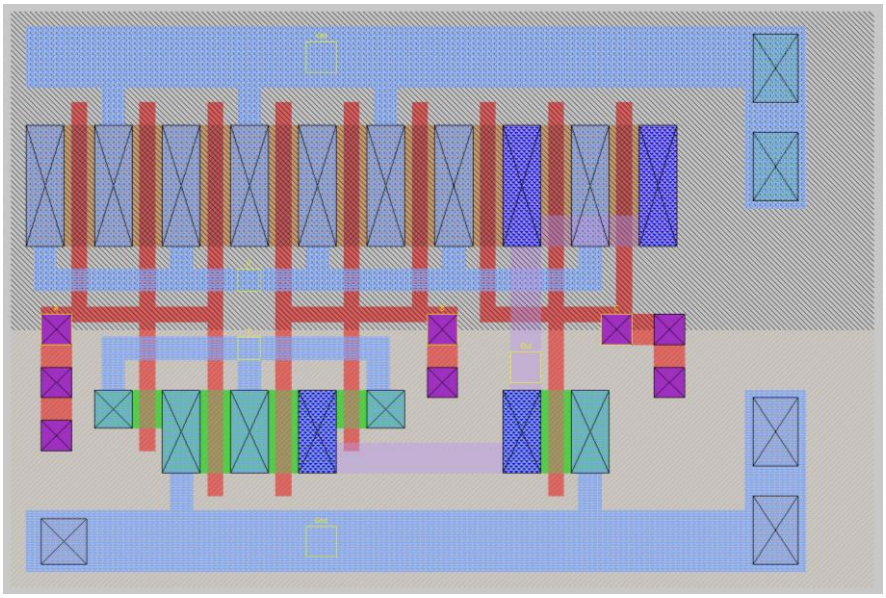

Figure 1: Layout of the AOI21X1 in MAGIC

Logic Expression: $Y = \overline{AB + C}$

Truth Table

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Port Definitions

A	Input
B	Input
C	Input
Y	Output

Timing characterization (all delays are in ns)

	A:0 to 1, B = 1, C =0			A:1 to 0, B = 1, C =0		
$T \downarrow \backslash C_L \rightarrow$	0.005pF	0.025pF	0.15pF	0.005pF	0.025pF	0.15pF
0.06ns	0.0607	0.0943	0.2903	0.0604	0.0933	0.2932
0.42ns	0.0812	0.1220	0.3230	0.0909	0.0132	0.3377
1.2ns	0.1026	0.1587	0.3973	0.1361	0.1925	0.4355

	B:0 to 1, A = 1, C =0			B:1 to 0, A = 1, C =0		
$T \downarrow \backslash C_L \rightarrow$	0.005pF	0.025pF	0.15pF	0.005pF	0.025pF	0.15pF
0.06ns	0.0552	0.0889	0.2850	0.0511	0.0843	0.2838
0.42ns	0.0927	0.1375	0.3390	0.0748	0.1199	0.3283
1.2ns	0.1343	0.1956	0.4595	0.1008	0.1672	0.4225

	C:0 to 1, A = 0 , B = 0			C:1 to 0, A = 0 , B = 0		
$T \downarrow \backslash C_L \rightarrow$	0.005pF	0.025pF	0.15pF	0.005pF	0.025pF	0.15pF
0.06ns	0.005	0.025	0.15	0.0346	0.0595	0.2094
0.42ns	0.0400	0.0743	0.2752	0.0652	0.1111	0.2800
1.2ns	0.0692	0.1210	0.3319	0.0962	0.1665	0.4164

Power characterization (all entries are in pJ)

	A:0 to 1, B = 1, C =0			A:1 to 0, B = 1, C =0		
$T \downarrow \backslash C_L \rightarrow$	0.005pF	0.025pF	0.15pF	0.005pF	0.025pF	0.15pF
0.06ns	0.02175	0.02243	0.02131	0.11507	0.18051	0.58664
0.42ns	0.02247	0.01918	0.01766	0.11979	0.18309	0.58728
1.2ns	0.05831	0.05116	0.03127	0.15953	0.21720	0.60639

$T \downarrow \backslash C_L \rightarrow$	B:0 to 1, A = 1, C =0			B:1 to 0, A = 1, C =0		
	0.005pF	0.025pF	0.15pF	0.005pF	0.025pF	0.15pF
0.06ns	0.02116	0.02084	0.02322	0.10059	0.16647	0.57425
0.42ns	0.02175	0.01836	0.01723	0.10502	0.16860	0.57390
1.2ns	0.05308	0.05005	0.02993	0.14193	0.19962	0.59092

$T \downarrow \backslash C_L \rightarrow$	C:0 to 1, A = 0 , B = 0			C:1 to 0, A = 0 , B = 0		
	0.005pF	0.025pF	0.15pF	0.005pF	0.025pF	0.15pF
0.06ns	0.0204	0.01772	0.01468	0.06867	0.1341	0.5419
0.42ns	0.02162	0.01861	0.01382	0.07959	0.14132	0.54324
1.2ns	0.05354	0.04652	0.02872	0.11541	0.17267	0.56141

Static Power Dissipation:

A	B	C	Static Power (pW)
0	0	0	53.3228
0	0	1	41.5181
0	1	0	98.6855
0	1	1	41.5181
1	0	0	101.51
1	0	1	41.5181
1	1	0	89.6182
1	1	1	27.4454
Average Static Power			61.892025

Extracted and modified SPICE Netlist:

```
SIMULATION OF AOI21X1

* And-Or-Invert : 3 inputs

* Include
.include tsmc180.lib

.option scale=0.09u

.param TESTTS=10n
.param TESTTON=5n
.param TDELAY=200p
.param TESTRISE=0.06n

.subckt aoi A B C Out Vdd Gnd
M1000 Vdd A a_n29_n14 Vdd cmosp w=16 l=2
+ ad=352 pd=140 as=544 ps=228
M1001 a_n29_n14 A Vdd Vdd cmosp w=16 l=2
+ ad=0 pd=0 as=0 ps=0
M1002 Vdd A a_n29_n14 Vdd cmosp w=16 l=2
+ ad=0 pd=0 as=0 ps=0
M1003 a_n29_n14 B Vdd Vdd cmosp w=16 l=2
+ ad=0 pd=0 as=0 ps=0
M1004 Vdd B a_n29_n14 Vdd cmosp w=16 l=2
+ ad=0 pd=0 as=0 ps=0
M1005 a_n29_n14 B Vdd Vdd cmosp w=16 l=2
+ ad=0 pd=0 as=0 ps=0
M1006 Out C a_n29_n14 Vdd cmosp w=16 l=2
+ ad=208 pd=90 as=0 ps=0
M1007 a_n29_n14 C Out Vdd cmosp w=16 l=2
+ ad=0 pd=0 as=0 ps=0
M1008 Out C a_n29_n14 Vdd cmosp w=16 l=2
+ ad=0 pd=0 as=0 ps=0
M1009 Gnd A a_n20_n38 Gnd cmosn w=5 l=2
+ ad=137 pd=70 as=137 ps=80
M1010 a_n20_n38 A Gnd Gnd cmosn w=11 l=2
+ ad=0 pd=0 as=0 ps=0
M1011 Out B a_n20_n38 Gnd cmosn w=11 l=2
+ ad=144 pd=72 as=0 ps=0
M1012 a_n20_n38 B Out Gnd cmosn w=5 l=2
+ ad=0 pd=0 as=0 ps=0
M1013 Gnd C Out Gnd cmosn w=11 l=2
+ ad=0 pd=0 as=0 ps=0
.ends

* Voltage sources
Vs Vddp 0 dc 1.8v
V1 1 0 dc 0v
V2 2 0 dc 0v
*V3 3 0 dc 0v
Vt 3 0 dc 1.8v pulse (1.8v, 0, {TDELAY}, {TESTRISE}, {TESTRISE}, {TESTTON}, {TESTTS})

* AOI stages
X1 1 2 3 out Vddp 0 aoi

c1 out 0 0.005p

* Control area
.control

op
print i(Vs)*v(Vddp)
```

```
destroy all
tran 1p 5n

let c1=0
let c2=0
let midpoint=1.8/2.0

plot v(out) v(3) vs time
plot abs(v(Vddp)*i(Vs)) vs time

print integrate(abs(v(Vddp)*i(Vs)))

cursor c1 right v(out) midpoint 1 falling
cursor c2 right v(3) midpoint 1 rising
print time[%c1] - time[%c2]

cursor c1 right v(out) midpoint 1 rising
cursor c2 right v(3) midpoint 1 falling
print time[%c1] - time[%c2]

.endc

.end
```

4. **DFFPOSX1**

We had initially chosen DFFSRX1. We had made SPICE preliminary simulations of the same. But later, it was informed to us that the test conditions for DFFSRX1 as not the same as the ones given for the other sequential circuits. Hence, we changed our sequential cell to DFFPOSX1.

However, due to the confusion regarding DFFSR, we have not done much with regard to the sequential element, and we just concentrated on the combinational logic circuits.