EE5134: Digital IC Design

Standard Cell Design: Project Report

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Selected Standard Cells:

1. INVX4
2. NOR2X1
3. AOI21X1
4. DFFPOSX1

Description of Procedure:

1. Criteria used to qualify a logic gate as X1, X2 etc.

The *inverter.mag* file that has been provided was taken as a reference inverter $X1$. To qualify any logic gate to have a drive strength of $X1$, $X2$ etc. we need to choose a value of load capacitance. We have chosen a value of the capacitance to be 500fF, much greater than the overall diffusion capacitance present at the output, to characterize the drive strength.

The a logic circuit is said to have a drive strength of Xn if it is able to drive a load of nC with the same rise and fall delays as compared to a reference inverter driving a load capacitance of C. In case of sequential circuits, the delays that are matched to the reference inverter delay are the clock to Q and the clock to $\bar{Q}$ delays.

As mentioned, the rise and fall delays are optimized for a load capacitance of 500fF. It should be noted that for smaller values of load capacitances, the rise and the fall delays is not necessary around the same value and may not be comparable to that of the reference inverter in accordance with the definition of drive strength. This is because the associated diffusion capacitances of a logic circuit are not necessarily the same as that of the reference inverter.

2. Rise and fall delays

The provided reference inverter has unequal rise and fall delays. In our case, we have tried to bring down the rise and fall delays of the logic circuit to lie between the rise and fall delays of the reference inverter. Moreover, the rise and fall delays are optimized to be almost equal for a load capacitance of 500fF (much greater than the diffusion capacitance). For other load capacitances (comparable to the diffusion capacitances) for which the circuit needs to be characterized, the rise and fall delays may slightly be different. As the load capacitance is increases, the time constant and hence the RC delay of a circuit increases. This is seen as increased rise/fall delays in all circuits as load capacitance is increased.

3. Process Flow

- The initial sizing of the transistors is chosen based on the logic and drive strength requirement, and the circuit thus obtained is simulated in *SpiceOpus*. We try to match the X1 inverter's delay and also try to have equal rise and fall delays with a 500fF load.
- Using SPICE level simulations, various parameters such as the widths of the PMOSs and NMOSs are varied so as to match the drive strength of the cell to that of the inverter.
- When an acceptable value for the drive strength is seen, the dimensions of the transistors are noted and the circuit layout is then designed in Magic.
- Once the layout is done in Magic, the spice net-list of the same is extracted and is parsed back to *SpiceOpus* and is tested for various combinations of inputs so as to verify the drive strength that has been initially obtained by simulating it in *SpiceOpus* alone.

- In case of any deviations in the drive strength, the magic layout is suitably edited to resize particular transistors. Again, the netlist is extracted and performance is verified. This kind of iteration is done until the value obtained for the drive strength is acceptable.
- Once we obtain the required design the cell is tested for various parameters such as power, rise time, fall time, setup time and hold time by testing it for all the possible combinations of inputs. This is also done across different values of load capacitances and input rise/fall times. The values that are obtained are tabulated.

4. Measurement of rise/fall delays

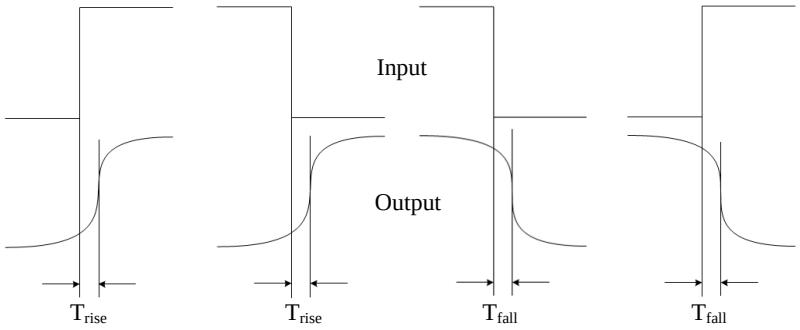

Figure 1: Rise and fall time measurement technique

The cases where the input toggle created a corresponding output toggle was analyzed for rise/fall delays. The $V_{dd}/2$ point was considered as shown in Figure 1 to measure the rise and fall delays of the output. This is done for different values of load capacitance and input rise/fall times and the results are tabulated as rise/fall delays of the output. Here, we are considering only one input toggle at a time. A situation where more than one input toggles simultaneously has not been analyzed.

5. Measurement of Setup time and Hold time(For DFFPOS)

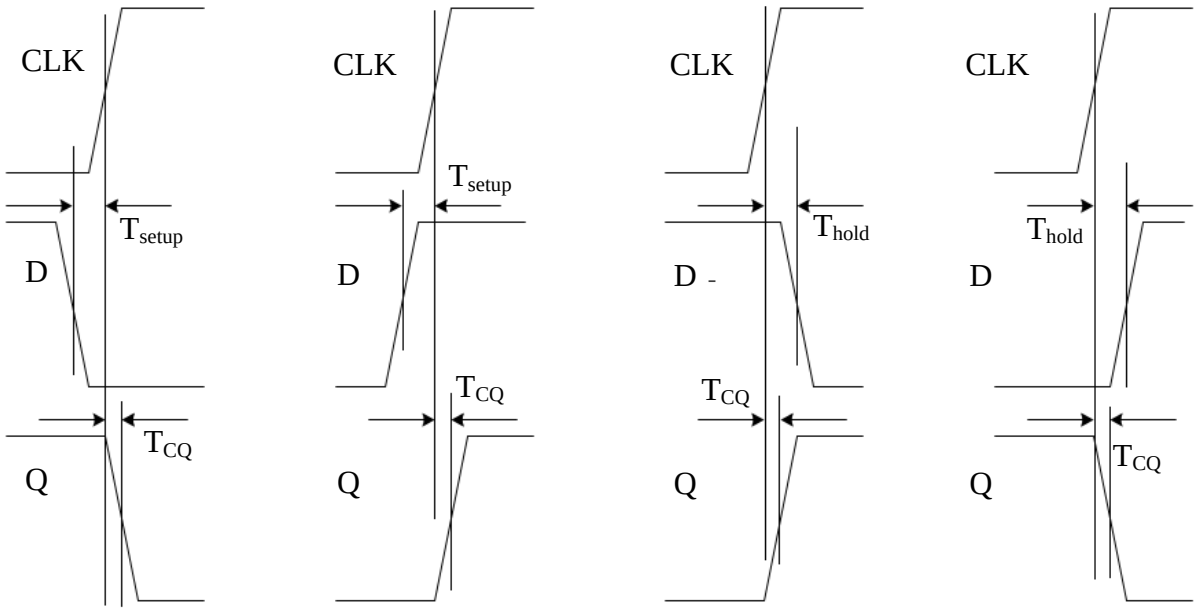

Figure 2: setup and hold time measurement technique a, b, c and d (left to right)

The setup time is the least time before the clock edge after which the D signal is not allowed to change. Failing to do this would result in Q not changing its value. It is found by gradually pushing the starting edge (10D) of the D-pulse closer to the rising edge (01Clk) of the clock. The point just after which the Q (10Q) value doesn't change according to the change in the value of D is taken as the setup time.

The hold time is the least time after the clock edge before which the D signal is not allowed to change. Failing to do this would result in Q not changing its value. The hold time is found by gradually pushing the ending edge (10D) of the D-pulse closer to the rising edge (01Clk) of the clock. The point just before which the Q (01Q) value doesn't change according to the change in the value of D is taken as the hold time.

The difference in times are taken from the $V_{dd}/2$ points of the D signal and Clock signal. When the hold time is negative, as it is in the case of our DFFPOS, it may seem like both the above techniques give us the same result. But note that the two techniques are different because though in both cases we are ultimately pushing the pulse edge of D close to the clock edge the initial state of Q is different. Basically

For example (refer to Figure 2a and Figure 2c): the setup time 10D=>01Clk: push the 10D closer to 01Clk till the value of Q=1 (initially) doesn't change to Q=0. The hold time of 01Clk=>10D: push the 10D closer to 01Clk till the value of Q=0 (initially) doesn't change to Q=1. The initial states of Q are different hence the results are not the same indicating different setup and hold times.

Calculations for both the setup and hold times would require us to continuously change the D-voltage source. As *SpiceOpus* doesn't allow for such a thing to be done automatically we have written a Perl script that will: run in a loop and change the setup/hold time in the .spice file → simulate the .spice file in batch mode of the *SpiceOpus* and store the result of whether the Q value changed or not in a file 'gen.txt'→ parse the 'gen.txt' file and print the result for each value of the setup/hold time. So we look for the point where the Q just transitions (result of this Perl script goes from 0 to 1 for setup or 1 to 0 for hold). There are times where the Perl script throws error because *SpiceOpus* seems to be overloaded at times. We can rectify this by rerunning the program and shifting our initial trial value of setup/hold time to the value up to which the code worked properly. We used binary search to speed up the process.

6. Measurement of Dynamic Energy consumption

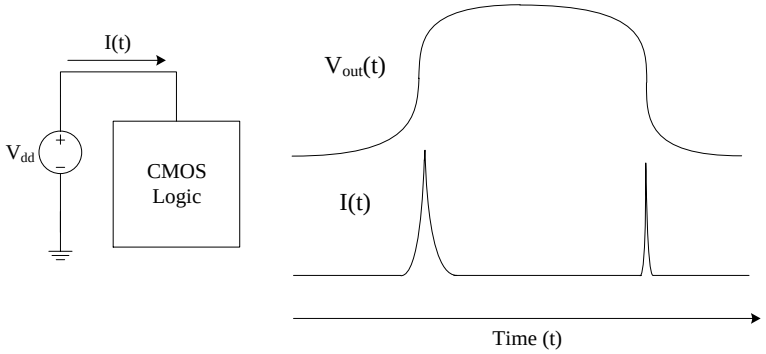

Figure 2: Typical output current characteristic as a function of time

Dynamic power consumption varies because of two main reasons during switching of the output: charging of the output capacitance, and short circuit current. Charging of the output capacitance occurs only when the output goes from low to high. In this case, the pull-up network is ON and power is drawn out of the supply rail. In the case when output goes from high to low, the pull-down network is ON and no power is drawn out of the supply rail.

On the contrary, short-circuit current flows during both the output switching cases. This is because, both the pull-up network and the pull-down network are momentarily in the ON state during switching, causing a short between the supply rail and ground.

There are several implications that one can infer from the above nature of power dissipation:

i. During the output voltage rise, since both factors contribute to the dissipation of energy, the energy consumed for this transition is much higher than the case where the output voltage falls.
ii. As the input rise/fall time is increased, the duration for which the 'shorting' of V_{dd} and GND rails happens is larger. This means that the contribution of short circuit energy dissipation increases with the increase in the input rise/fall time. Further, considering only the first order effects, the short circuit current does not have a direct proportionality relationship with the load capacitance.
iii. On the contrary, the capacitor can hold a fixed amount of charge which depends on the value of its capacitance. Hence, the charging contribution to energy dissipation is independent of the rise and fall times of the input that triggers a rise in the output. But, as the value of the capacitance is increased, higher is the energy is stored in the capacitor, leading to an increase in the charging contribution to the energy dissipation.

All the above mentioned effects can be seen across all the standard cell libraries that are characterized. For measuring the switching energy that is consumed, the following procedure was adopted. Only the cases where the input toggle created a corresponding output toggle was analyzed as only there cases contribute to dynamic power. A switching frequency in such cases was considered to be 100MHz with equal ON and OFF times. The energy dissipated from the source is integrated over half the switching frequency separately for output rise and output fall. This is done for different values of load capacitance and input rise/fall times and the results are tabulated as dynamic energy consumption during switching.

Note that we are assuming that static power dissipated is extremely small when compared to the dynamic power and hence, during the dynamic power measurements, the contribution of static power is neglected.

7. Measurement of Static Power consumption

Due to the phenomena of sub-threshold conduction and gate leakage currents, the supply currents do not go to zero, even when there is no change in the input states. We have considered the static power consumption to be the average of quiescent power consumed under all possible input combinations. For computing the static power consumption, we need to do an operating point analysis, rather than doing a transient analysis.

Reference Inverter:

The Inverter of size X1 was provided with PMOS size 20λ and NMOS size10λ. For 500 fF load, the rise delay of the reference inverter = 0.83852 ns and the fall delay 0.8886 ns.

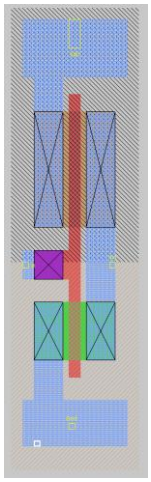

Figure 3: Layout of the inverter in MAGIC

1. INVX4:

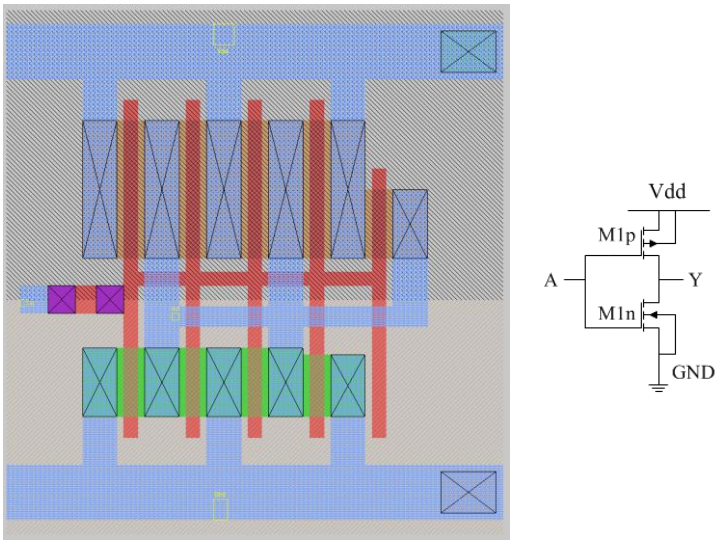

Figure 4: Layout of the INVX4 in MAGIC (left) and its transistor level circuit diagram (right).

Logic Expression: $Y = \bar{A}$

Truth Table

A	Y
0	1
1	0

Port Definitions

A	Input
Y	Output

Transistor sizing: (Wn/Ln)

i. Initial sizing: To match the pull up and pull down resistance to that of a reference inverter.
   a. M1p: $80\lambda/2\lambda$
   b. M1n: $40\lambda/2\lambda$

ii. After iteration to optimize rise/fall times:
   a. M1p: $90\lambda/2\lambda$
   b. M1n: $39\lambda/2\lambda$

Width of the standard cell: 72λ

Timing characterization (all delays are in ns)

	A:0 to 1			A:1 to 0		
T ↓ \ C_L →	0.005pF	0.025pF	0.15pF	0.005pF	0.025pF	0.15pF
0.06ns	0.02447	0.03498	0.09134	0.02715	0.03695	0.09389
0.42ns	0.03329	0.05493	0.14268	0.0603	0.08165	0.16785
1.2ns	0.02782	0.06084	0.19017	0.1071	0.1405	0.2682

Dynamic switching energy characterization (all entries are in pJ)

	A:0 to 1			A:1 to 0		
$T \downarrow \backslash C_L \rightarrow$	0.005pF	0.025pF	0.15pF	0.005pF	0.025pF	0.15pF
0.06ns	0.0375	0.0403	0.0464	0.1058	0.1715	0.5826
0.42ns	0.0721	0.0636	0.0381	0.1457	0.2049	0.5972
1.2ns	0.1705	0.1600	0.1203	0.2512	0.3053	0.6756

Static Power Dissipation:

A	**Static Power (pW)**
0	131.352
1	73.848
Average Power	**102.600**

2. NOR2X1:

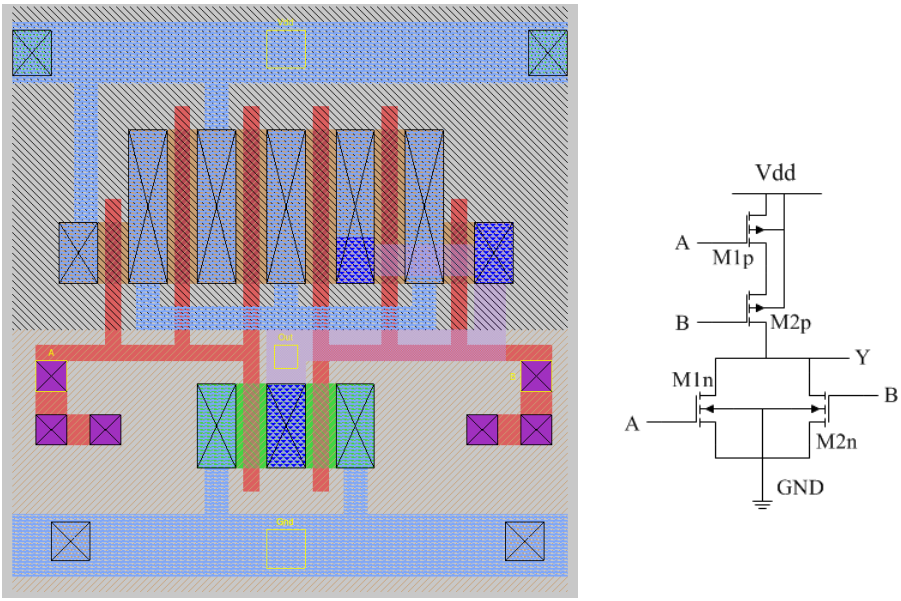

Figure 5: Layout of the NOR2X2 in MAGIC (left) and its transistor level circuit diagram (right).

Logic Expression: $Y = \overline{A + B}$

Truth Table

A	B	Y
0	0	1
0	0	0
0	1	0
0	1	0

Port Definitions

A	Input
B	Input
Y	Output

Transistor sizing: (Wn/Ln)

i. Initial sizing: To match the pull up and pull down resistance to that of a reference inverter.
   a. M1p: $40\lambda/2\lambda$
   b. M1n: $10\lambda/2\lambda$
   c. M2p: $40\lambda/2\lambda$
   d. M2n: $10\lambda/2\lambda$

ii. After iteration to optimize rise/fall times:
   a. M1p: $48\lambda/2\lambda$
   b. M1n: $11\lambda/2\lambda$
   c. M2p: $48\lambda/2\lambda$
   d. M2n: $11\lambda/2\lambda$

Width of the standard cell: 72λ

Timing characterization (all delays are in ps)

	A:0 to 1, B= 0			A:1 to 0, B= 0		
$C_L \downarrow \backslash T \rightarrow$	.06ns	.42ns	1.2ns	.06ns	.42ns	1.2ns
0.005pF	43.558	76.025	274.461	48.270	82.521	282.526
0.025pF	61.190	109.385	318.815	86.200	134.100	340.950
0.15pF	75.700	148.205	409.245	130.650	196.850	470.700

	B:0 to 1, A= 0			B:1 to 0, A= 0		
$C_L \downarrow \backslash T \rightarrow$	.06ns	.42ns	1.2ns	.06ns	.42ns	1.2ns
0.005pF	36.143	69.727	269.665	36.127	71.092	272.236
0.025pF	66.850	122.155	334.580	58.600	114.450	328.700
0.15pF	104.610	186.575	476.855	77.150	159.450	452.750

Dynamic switching energy characterization (all entries are in pJ)

	A:0 to 1, B= 0			A:1 to 0, B= 0		
$C_L \downarrow \backslash T \rightarrow$	.06ns	.42ns	1.2ns	.06ns	.42ns	1.2ns
0.005pF	0.02107	0.02177	0.05407	0.08291	0.08878	0.12443
0.025pF	0.02102	0.01816	0.04747	0.14874	0.15177	0.18207
0.15pF	0.02120	0.01774	0.02835	0.55498	0.55544	0.57157

	B:0 to 1, A= 0			B:1 to 0, A= 0		
$C_L \downarrow \backslash T \rightarrow$	.06ns	.42ns	1.2ns	.06ns	.42ns	1.2ns
0.005pF	0.01994	0.02128	0.05141	0.05881	0.06962	0.10334
0.025pF	0.01650	0.01793	0.04412	0.12452	0.13118	0.16041
0.15pF	0.01281	0.01277	0.02634	0.53238	0.53314	0.54961

Static Power Dissipation:

A	B	Static Power (pW)
0	0	67.8741
0	0	41.9351
0	1	54.0486
0	1	22.2120
Average Power		**46.5175**

3. AOI21X1

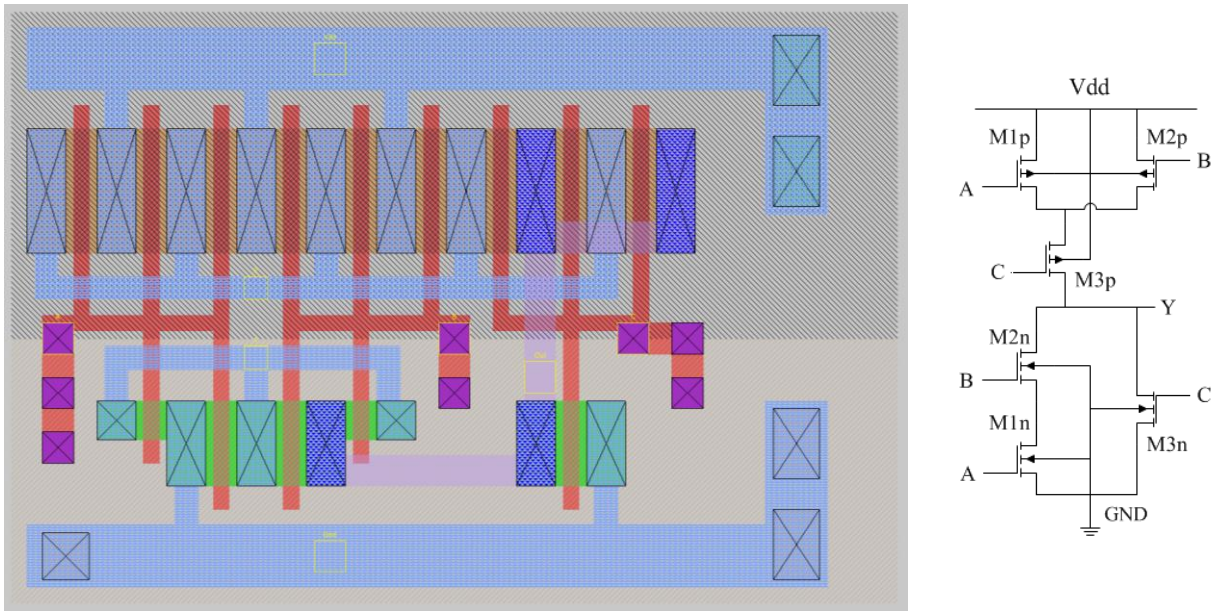

Figure 6: Layout of the AOI21X1 in MAGIC (left) and its transistor level circuit diagram (right).

Logic Expression: $Y = \overline{AB + C}$

Truth Table

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Port Definitions

A	Input
B	Input
C	Input
Y	Output

Transistor sizing: (Wn/Ln)

i. Initial sizing: To match the pull up and pull down resistance to that of a reference inverter.
   a. M1p: $40\lambda/2\lambda$
   b. M1n: $20\lambda/2\lambda$
   c. M2p: $40\lambda/2\lambda$
   d. M2n: $20\lambda/2\lambda$
   e. M3p: $10\lambda/2\lambda$

f. M3n: $40\lambda/2\lambda$

ii. After iteration to optimize rise/fall times:

a. M1p: $48\lambda/2\lambda$
b. M1n: $16\lambda/2\lambda$
c. M2p: $48\lambda/2\lambda$
d. M2n: $16\lambda/2\lambda$
e. M3p: $48\lambda/2\lambda$
f. M3n: $11\lambda/2\lambda$

Width of the standard cell: 102λ

Timing characterization (all delays are in ns)

	A:0 to 1, B = 1, C =0			A:1 to 0, B = 1, C =0		
T ↓ \ C_L →	0.005pF	0.025pF	0.15pF	0.005pF	0.025pF	0.15pF
0.06ns	0.0607	0.0943	0.2903	0.0604	0.0933	0.2932
0.42ns	0.0812	0.1220	0.3230	0.0909	0.0132	0.3377
1.2ns	0.1026	0.1587	0.3973	0.1361	0.1925	0.4355

	B:0 to 1, A = 1, C =0			B:1 to 0, A = 1, C =0		
T ↓ \ C_L →	0.005pF	0.025pF	0.15pF	0.005pF	0.025pF	0.15pF
0.06ns	0.0552	0.0889	0.2850	0.0511	0.0843	0.2838
0.42ns	0.0927	0.1375	0.3390	0.0748	0.1199	0.3283
1.2ns	0.1343	0.1956	0.4595	0.1008	0.1672	0.4225

	C:0 to 1, A = 0 , B = 0			C:1 to 0, A = 0 , B = 0		
T ↓ \ C_L →	0.005pF	0.025pF	0.15pF	0.005pF	0.025pF	0.15pF
0.06ns	0.005	0.025	0.15	0.0346	0.0595	0.2094
0.42ns	0.0400	0.0743	0.2752	0.0652	0.1111	0.2800
1.2ns	0.0692	0.1210	0.3319	0.0962	0.1665	0.4164

Dynamic switching energy characterization (all entries are in pJ)

	A:0 to 1, B = 1, C =0			A:1 to 0, B = 1, C =0		
T ↓ \ C_L →	0.005pF	0.025pF	0.15pF	0.005pF	0.025pF	0.15pF
0.06ns	0.02175	0.02243	0.02131	0.11507	0.18051	0.58664
0.42ns	0.02247	0.01918	0.01766	0.11979	0.18309	0.58728
1.2ns	0.05831	0.05116	0.03127	0.15953	0.21720	0.60639

T ↓ \ C_L →	B:0 to 1, A = 1, C =0			B:1 to 0, A = 1, C =0		
	0.005pF	0.025pF	0.15pF	0.005pF	0.025pF	0.15pF
0.06ns	0.02116	0.02084	0.02322	0.10059	0.16647	0.57425
0.42ns	0.02175	0.01836	0.01723	0.10502	0.16860	0.57390
1.2ns	0.05308	0.05005	0.02993	0.14193	0.19962	0.59092

$T \downarrow \backslash C_L \rightarrow$	C:0 to 1, A = 0 , B = 0			C:1 to 0, A = 0 , B = 0		
	0.005pF	0.025pF	0.15pF	0.005pF	0.025pF	0.15pF
0.06ns	0.0204	0.01772	0.01468	0.06867	0.1341	0.5419
0.42ns	0.02162	0.01861	0.01382	0.07959	0.14132	0.54324
1.2ns	0.05354	0.04652	0.02872	0.11541	0.17267	0.56141

Static Power Dissipation:

A	B	C	Static Power (pW)
0	0	0	53.3228
0	0	1	41.5181
0	1	0	98.6855
0	1	1	41.5181
1	0	0	101.51
1	0	1	41.5181
1	1	0	89.6182
1	1	1	27.4454
Average Static Power			**61.892025**

4. DFFPOSX1

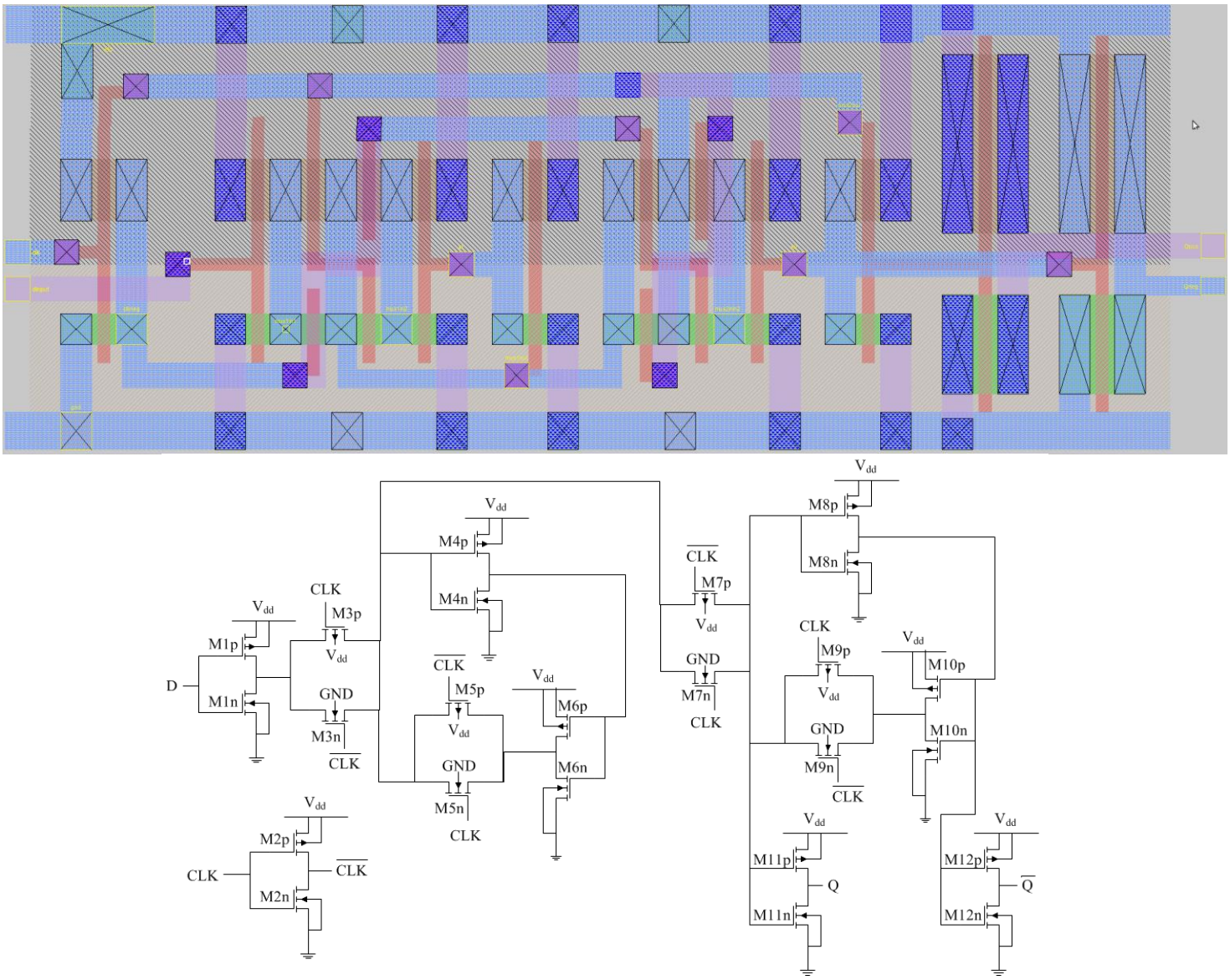

Figure 7: Layout of the DFFPOSX1 in MAGIC (top) and its transistor level circuit diagram (bottom).

Transistor sizing: (Wn/Ln) (refer to Figure 7)

i. Initial sizing done to match the rise time and fall time delays to that of a reference inverter with a load of 500fF. And also to make the rise time delay= fall time delay. This is done on a preliminary spice file.
   a. M[1:10]p: $10\lambda/2\lambda$
   b. M[1:10]n: $5\lambda/2\lambda$
   c. M[11:12]p: $28\lambda/2\lambda$
   d. M[11:12]n: $15\lambda/2\lambda$

ii. After iteration on the spice file extracted from the magic file to optimize rise and fall times:

a. M[1:10]p: $10\lambda/2\lambda$
b. M[1:10]n: $5\lambda/2\lambda$
c. M[11:12]p: $29\lambda/2\lambda$
d. M[11:12]n: $16\lambda/2\lambda$

The sizes of the transistors that form the D flip flop are made large enough to give enough drive strength to the output inverters. We observed that increasing the sizes of these M[1:10] transistors will not greatly affect the delay times. The delay times are majorly affected by the output inverters M[11:12]. Hence the sizes of these transistors are made large enough to match the delays got with those got for the inverter. The fall delay was larger than the rise delay for W_p/W_n=2/1 hence we choose W_p/W_n=29/16 (<2/1).

Function
FLIPFLOP{
DATA=D
CLOCK=CLK
Q=DS0000
QN=P0002
}
Q=DS0000

Width of the standard cell: 102λ

Static Power:

When	Static Power [nW]
CLK=0; D=0	0.374
CLK=0; D=1	0.262
CLK=1; D=0	0.502
CLK=1; D=1	0.369
Average	0.37675

Port:

Pin	Direction	Signal type	Polarity
CLK	INPUT	CLOCK	RISING_EDGE
D	INPUT	DATA	-
Q	OUTPUT	-	-

(01CLK=>01Q)
DELAY [ns]

Cl[pF] → **ts(ns) ↓**	0.005	0.0125	0.025	0.075	0.15
0.06	0.1490	0.1670	0.1945	0.2836	0.3987
0.24	0.1770	0.1952	0.2215	0.3108	0.4260
0.48	0.2106	0.2286	0.2555	0.3441	0.4590
0.9	0.2495	0.2468	0.2949	0.3847	0.5011
1.2	0.2704	0.2893	0.3169	0.4072	0.5237
1.8	0.3029	0.3232	0.3519	0.4440	0.5605

(01CLK=>01Q)
ENERGY [pJ]

Cl[pF] → / **ts(ns) ↓**	0.005	0.0125	0.025	0.075	0.15
0.06	0.2070	0.2299	0.2686	0.4293	0.6729
0.24	0.2147	0.2375	0.2765	0.4367	0.6796
0.48	0.2355	0.2577	0.2958	0.4547	0.6969
0.9	0.2765	0.2974	0.3343	0.4910	0.7320
1.2	0.3071	0.3273	0.3634	0.5186	0.7589
1.8	0.3698	0.3887	0.4230	0.5756	0.8144

(01CLK=>10Q)
DELAY [ns]

Cl[pF] → / **ts(ns) ↓**	0.005	0.0125	0.025	0.075	0.15
0.06	0.2173	0.2390	0.2693	0.3604	0.4699
0.24	0.2496	0.2713	0.3015	0.3929	0.5023
0.48	0.2824	0.3030	0.3321	0.4223	0.5313
0.9	0.3162	0.3349	0.3619	0.4486	0.5555
1.2	0.3202	0.3390	0.3660	0.4531	0.5598
1.8	0.3177	0.3365	0.3634	0.4503	0.5573

(01CLK=>10Q)
ENERGY10 [pJ]

Cl[pF] → / **ts(ns) ↓**	0.005	0.0125	0.025	0.075	0.15
0.06	0.2382	0.2339	0.2283	0.2176	0.2154
0.24	0.2446	0.2410	0.2349	0.2257	0.2223
0.48	0.2528	0.2493	0.2435	0.2353	0.2325
0.9	0.2787	0.2748	0.2691	0.2614	0.2588
1.2	0.2991	0.2950	0.2895	0.2817	0.2790
1.8	0.3405	0.3366	0.3310	0.3234	0.3209

Timing Constraints:
SETUP (01D=>01CLK)

re [ns] → / **co [ns] ↓**	**0.06**	**0.3**	**0.6**	**1.2**
0.06	110	94	101	129
0.3	142	123	127	151
0.6	165	142	144	165
1.2	190	164	164	181

SETUP (10D=>01CLK)

re [ns] → / **co [ns] ↓**	**0.06**	**0.3**	**0.6**	**1.2**

0.06	149	198	241	312
0.3	200	249	290	361
0.6	252	302	342	412
1.2	333	386	426	497

HOLD (01CLK=>01D)

re [ns] → **co [ns] ↓**	**0.06**	**0.3**	**0.6**	**1.2**
0.06	-52	-36	-38	-53
0.3	-79	-56	-53	-65
0.6	-94	-64	-58	-66
1.2	-104	-67	-56	-56

HOLD (01CLK=>10D)

re [ns] → **co [ns] ↓**	**0.06**	**0.3**	**0.6**	**1.2**
0.06	-114	-148	-183	-242
0.3	-164	-197	-231	-293
0.6	-212	-244	-279	-345
1.2	-287	-319	-354	-425