HW III

32-bit Ripple Carry Adder Design

The simplest way to build an N-bit carry propagate adder is to chain together *N* full adders. The Cout of one stage acts as the Cin of the next stage, as shown in ***Figure*** below for 32-bit addition. This is called a ripple-carry adder. It is a good application of modularity and regularity: the full adder module is reused many times to form a larger system. The ripple-carry adder has the disadvantage of being slow when N is large. S31 depends on C30, which depends on C29, which depends on C28, and so forth all the way back to Cin, as shown in blue in ***Figure***. We say that the carry ripples through the carry chain. The delay of the adder, t_{ripple},grows directly with the number of bits, given as $t_{ripple} = N * t_{FA}$ where t_{FA} is the delay of a full adder.

a) Write VHDL code to design and simulate a 32-bit ripple carry adder with full adders. Do not instantiate all full adder by hand. Use another method.

b) Suppose that we have 20ns delay for XOR gate and 15ns for and & or gates, then calculate overall delay for final result. Try to obtain the same result through simulation. Explain your results.

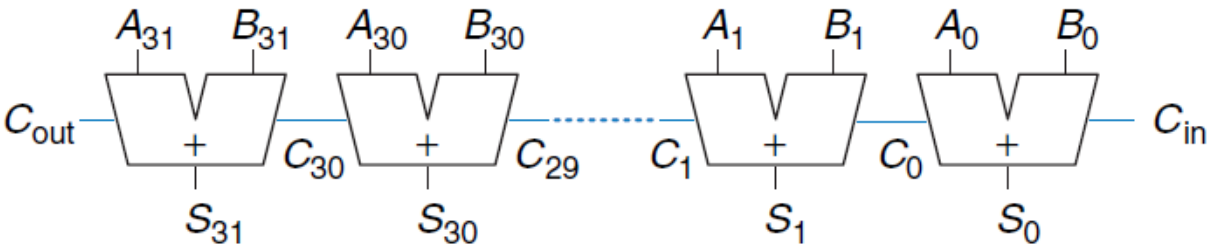

Figure. Ripple Carry Adder