HW IV

Design a serial adder. It takes 8-bit inputs *A* and *B* and adds them in a serial fashion when the ***go(start)*** input is set to 1. The result of the operation is stored in a 9-bit *sum* register.

A block diagram of the circuit is shown in **Figure** below. It consists of three shift registers, a full-adder, a flip-flop to store carry-out signal from the full adder and a finite state machine (FSM). The shift registers *A* and *B* are loaded with the values of *A* and *B.* After the ***start*** signal is set high, these registers are shifted right one bit at a time. At the same time the least-significant bits of *A* and *B* are added and the result is stored into the shift register *sum.* Once all bits of *A* and *B* have been added, the circuit stops and displays the *sum* until a new addition is requested.

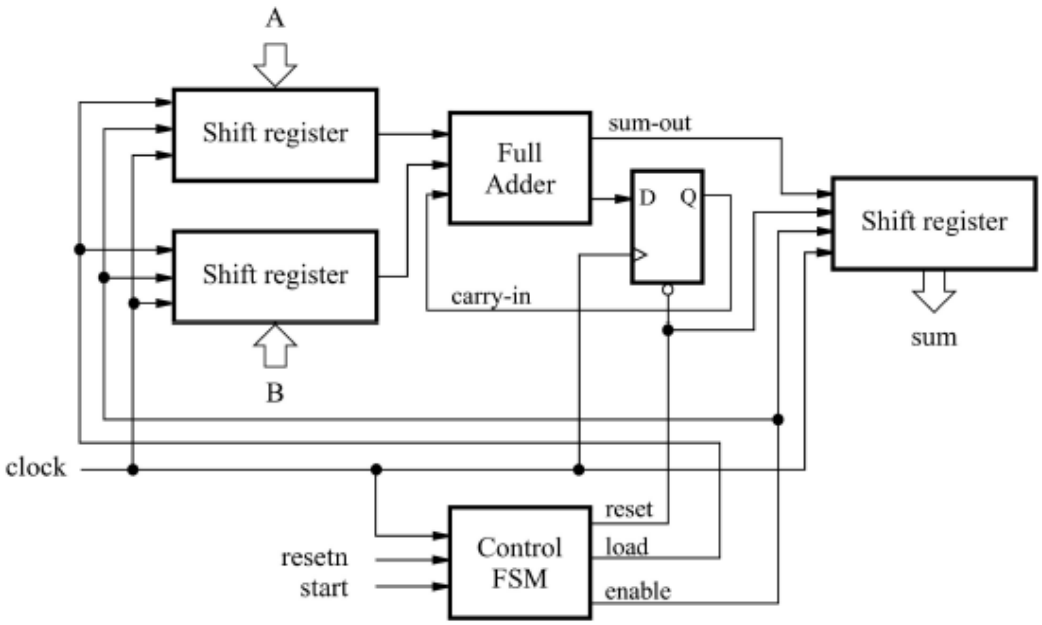

Figure. Block diagram of a serial adder circuit