The Implementation of a Continuous Flow Multithreading Microprocessor

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1. Abstract:

Switch on Event Multithreading (SoE MT) processors run multiple threads on a pipeline machine, while the thread switch occur on memory stall events. The thread switch penalty is determined by the number of stages in the pipeline that are flushed of in-flight instructions.

In this project, Continuous Flow Multithreading (CFMT), a new architecture of SoE MT, is introduced. In CFMT, a multistate pipeline register (MPR) holds the microarchitectural state of multiple different threads within the execution pipeline stages, where only one thread is active at a time. The MPRs eliminate the need to flush in-flight instructions and therefore significantly improve performance. The MPR is located near the pipeline and that can be theoretically be implemented thanks to immerging memory technologies called memristors. Memristors are power efficient, dense, and fast as compared to other standard memories and therefore provide the opportunity to place the MPRs physically within the pipeline stages.

Our preliminary, conceptual, performance analysis of CFMT when compared to conventional SoE MT processors, is found to have up to approximately 1.7X performance improvement in our benchmarks, and shows potential for up to 1.8X improvement in far longer benchmarks. The simulation results on the finished design, affirmed the preliminary results.