GC9107

a-Si TFT LCD Single Chip Driver
128RGBx160 Resolution and 262K color

Datasheet

V1.3

2021-09-10

GENERATION REVISION HISTORY

Version.	Effective Date	Description of Changes	Prepared by
V1.0	2019-11-2	Document Release	Evie
V1.1	2021-1-8	Application Circuit Adjusted	Evie
V1.2	2021-1-22	Command Adjusted	Evie
V1.3	2021-09-10	Display Inversion Control	Xin

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1. Introduction

The GC9107 is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 128RGBx160dots, comprising a 384-channel source driver, a 160-channel gate driver, 46,080 bytes GRAM for graphic display data of 128RGBx160 dots, and power supply circuit.

The GC9107 supports parallel 8-bit data bus MCU interface, and 3-/4-line serial peripheral interface (SPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

The GC9107 can operate with 1.65V ~ 3.3V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. GC9107 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the GC9107 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

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2. Features

- No need for external electronic component.
- Display resolution: [128xRGB](H) x 160(V)
- Output:
  - 384 source outputs
  - 160 gate outputs
  - Common electrode output (VCOM)
- a-TFT LCD driver with on-chip full display RAM: 46,080 bytes
- System Interface
  - 8-bits interface with 8080 MCU
  - 3-line / 4-line serial interface
- Driving Algorithm Support
  - Row Inversion
  - Frame Inversion
- Display mode:
  - Full color mode (Idle mode OFF): 262K-color
  - Reduce color mode (Idle mode ON): 8-color
- Power saving mode:
  - 8-color mode
  - Standby mode
- On chip functions:
  - Timing generator
  - Oscillator
  - DC/DC converter
- Support partial display
- Window address function to specify a rectangular area for internal GRAM access
- Low -power consumption architecture
  - Low operating power supplies:
    - IOVCC = 1.65V ~ 3.3V (logic)
    - VCI = 2.5V ~ 3.3V (analog)
- On-Chip Power System
  - Source Voltage(VREG): +2.92V ~ +5.19V
  - VCOM level(VCOMH、VCOML): +3.08V ~ +4.50V、-2.50V ~ 0V
  - Gate driver HIGH level (VGH): +10V ~ +15V
  - Gate driver LOW level (VGL): -13V ~ -7.5V
- Operate temperature range: -40℃to 80℃
- a-Si TFT LCD storage capacitor : Cst on Common structure only
- Package COG

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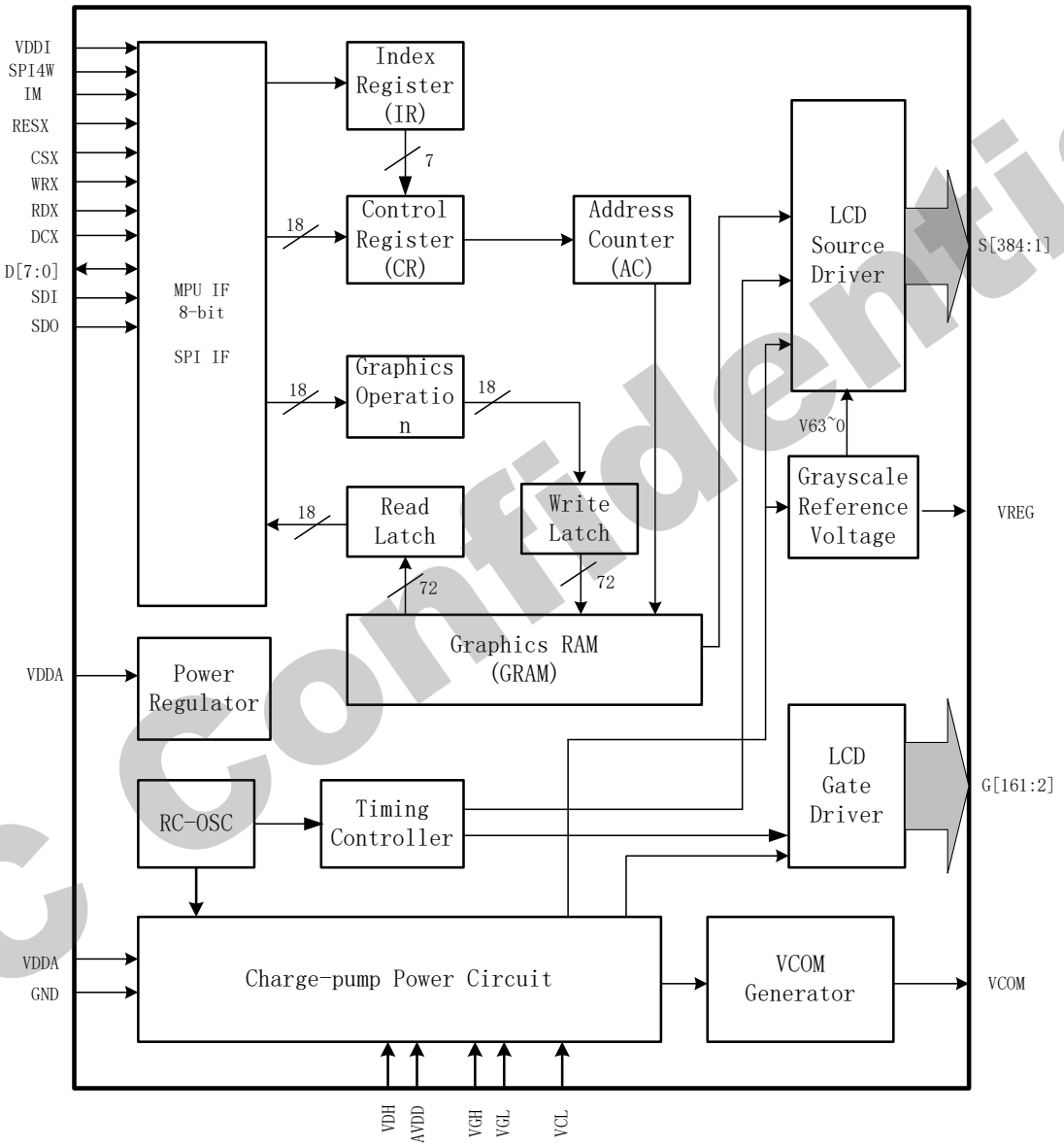
3. Block Diagram

3.1. Block diagram



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3.2. Pin descriptions

Power Supply Pins			
Pin Name	I/O	Type	Descriptions
VDDA（VCI）	I	Power	Power supply for analog, digital system and booster circuit
VDDI(IOVCC)	I	Power	Low voltage power supply for interface logic circuits(1.65~3.3V)
VSSA	I	Analog Ground	System ground level for analog circuit blocks
VSSR	I	Digital Ground	System ground level for logic circuit blocks

Interface Logic Signals			
Pin Name	I/O	Type	Descriptions
IM	I	(VDDI/VSSR)	MCU Parallel interface bus and Serial interface select - IM='1';Parallel-8bit Interface - IM='0';Serial Interface
SPI4W	I	(VDDI/VSSR)	SPI interface selection pin SPI4W='0': 3-wire SPI. (default) SPI4W='1': 4-wire SPI. This pin is internal pull low.
RESX	I	MCU (VDDI/VSSR)	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
CSX	I	MCU (VDDI/VSSR)	Chip select input pin ("Low" enable). This pin can be permanently fixed "Low" in MPU interface mode only. *note1,2
DCX（**SCL**）	I	MCU (VDDI/VSSR)	This pin is used to select "Data or Command" in the parallel interface。When DCX='1', data is selected. When DCX='0', command is selected. This pin is used serial interface clock in 3-wire 9-bit/4-write 8-bit serial data interface. If not used, this pin should be connected to VDDI or VSSR.
RDX	I	MCU (VDDI/VSSR)	8080 system (RDX): Serves as a read signal and MCU read data at the rising edge.
WRX (**RS**)	I	MCU (VDDI/VSSR)	8080 system (WRX): Serves as a write signal and writes data at the rising edge. 4-write 8-bit serial data interface: serves as **RS**(data/command selection). Fix to VDDI level when not in use
D[7:1] **D0/SDA**	I/O	MCU (VDDI/VSSR)	8-bit parallel bi-directional data bus for MCU system and D0 is also the serial input/output signal in SPI interface mode.

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<table>
<tr><td></td><td></td><td></td><td>Fix to VSSR level when not in use</td></tr>
<tr><td>GM[1:0]</td><td>I</td><td>(VDDI/VSSR)</td><td>Panel Resolution selection pins
<table>
<tr><th>GM1</th><th>GM0</th><th>Resolution</th><th>Source gate</th><th>Window set
(2ah 2bh)</th></tr>
<tr><td>0</td><td>0</td><td>128X128</td><td>S1-S384,
G2-G129</td><td>(0x00,0x7f)
(0x00,0x7f)</td></tr>
<tr><td>0</td><td>1</td><td>128X128</td><td>S1-S384,
G2-G129</td><td>(0x00,0x83)
(0x00,0x83)</td></tr>
<tr><td>0</td><td>1</td><td>128X128</td><td>S1-S384,
G2-G129</td><td>(0x02,0x81)
(0x01,0x80)</td></tr>
<tr><td>1</td><td>0</td><td>128X160</td><td>S1-S384,
G2-G161</td><td>(0x00,0x83)
(0x00,0xa1)</td></tr>
<tr><td>1</td><td>0</td><td>128X160</td><td>S1-S384,
G2-G161</td><td>(0x02,0x81)
(0x01,0xa0)</td></tr>
<tr><td>1</td><td>1</td><td>128X160</td><td>S1-S384,
G2-G161</td><td>(0x00,0x7f)
(0x00,0x9f)</td></tr>
</table></td></tr>
<tr><td>TE</td><td>O</td><td>MCU
(VDDI/VSSR)</td><td>Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.</td></tr>
</table>

Note.

1. If CSX is connected to VSSR in Parallel interface mode, there will be no abnormal visible effect to the display module. Also there will be no restriction on using the Parallel Read/Write protocols, Power On/Off Sequences or other functions. Furthermore there will be no influence to the Power Consumption of the display module.

2. When CSX='1', there is no influence to the parallel and serial interface.

LCD Driver Input/Output Pins			
Pin Name	I/O	Type	Descriptions
S384~S1	O	Source	Source output signals.. Leave the pin to open when not in use.
G161~G2	O	Gate	Gate output signals. Leave the pin to open when not in use.
AVDD	O	OPEN	Power pad for analog circuit, A power supply pin for generating VREG
VGH	O	Power	Power supply for the gate driver. Adjust the VGH level with the VGHS[2:0] bits.
VGL	O	Power	Power supply for the gate driver. Adjust the VGL level with the VGLS[2:0] bits.
VCL	O	Power	Power supply for VCOML.

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			VCL=0~-VDD
VREG_TEST	O	OPEN	High reference voltage for grayscale voltage generator. Internal register can be used to adjust the voltage.
VCOM	O	Power	Power supply pad for the TFT-display counter electrode. Connect this pad to the TFT-display counter electrode.

Test Pins			
Pin Name	I/O	Type	Descriptions
TEST	O	Open	These test pins for driver vender test used Please leave these pins open
OSC_IN	I	Open	These test pins for driver vender test used Please leave these pins open
OSC_TEST	O	Open	These test pins for driver vender test used Please leave these pins open
VREF2P0_TEST	O	Open	These test pins for driver vender test used Please leave this pin open
DUMMY	-	Open	These pins are dummy. During normal operation, leave these pads open.

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Liquid crystal power supply specifications Table

No.	Item		Description
1	TFT Source Driver		384 pins (128*RGB)
2	TFT Gate Driver		160pins
3	TFT Display's Capacitor Structure		Cst structure only (Cs on Common)
4	Liquid Crystal Drive Output	S1~S384	V0~V63 grayscales
		G2~G161	VGH-VGL
		VCOM	-2.50V ~ +4.50V
5	Input Voltage	IOVCC	+1.65V ~ +3.30V
		VCI	+2.50V ~ +3.30V
6	Liquid Crystal Drive Voltages	VCOMH	+3.08V ~ +4.50V
		VCOML	-2.50V ~ 0V
		VGH	+10.00V ~ +15.00V
		VGL	-13.00V ~ -7.50V

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3.3. PAD coordinates

No	Pad	X	Y
1	DUMMY	-4750	-216.5
2	DUMMY	-4700	-216.5
3	DUMMY	-4650	-216.5
4	DUMMY	-4600	-216.5
5	DUMMY	-4550	-216.5
6	DUMMY	-4500	-216.5
7	DUMMY	-4450	-216.5
8	DUMMY	-4400	-216.5
9	DUMMY	-4350	-216.5
10	DUMMY	-4300	-216.5
11	DUMMY	-4250	-216.5
12	DUMMY	-4200	-216.5
13	DUMMY	-4150	-216.5
14	DUMMY	-4100	-216.5
15	DUMMY	-4050	-216.5
16	DUMMY	-4000	-216.5
17	DUMMY	-3950	-216.5
18	DUMMY	-3900	-216.5
19	DUMMY	-3850	-216.5
20	DUMMY	-3800	-216.5
21	DUMMY	-3750	-216.5
22	DUMMY	-3700	-216.5
23	DUMMY	-3650	-216.5
24	DUMMY	-3600	-216.5
25	DUMMY	-3550	-216.5
26	DUMMY	-3500	-216.5
27	DUMMY	-3450	-216.5
28	DUMMY	-3400	-216.5
29	DUMMY	-3350	-216.5
30	DUMMY	-3300	-216.5
31	DUMMY	-3250	-216.5
32	DUMMY	-3200	-216.5
33	DUMMY	-3150	-216.5
34	DUMMY	-3100	-216.5
35	DUMMY	-3050	-216.5
36	DMY	-3000	-216.5

No.	Pad	X	Y
51	VDDA	-2250	-216.5
52	VDDA	-2200	-216.5
53	VDDA	-2150	-216.5
54	VDDA	-2100	-216.5
55	VDDA	-2050	-216.5
56	VDDA	-2000	-216.5
57	VSSA	-1950	-216.5
58	VSSA	-1900	-216.5
59	VSSA	-1850	-216.5
60	VSSA	-1800	-216.5
61	VSSA	-1750	-216.5
62	VSSA	-1700	-216.5
63	RDX	-1630	-216.5
64	DCX	-1570	-216.5
65	DUMMY	-1510	-216.5
66	DUMMY	-1450	-216.5
67	DUMMY	-1390	-216.5
68	DUMMY	-1330	-216.5
69	DUMMY	-1270	-216.5
70	DUMMY	-1210	-216.5
71	DUMMY	-1150	-216.5
72	DUMMY	-1090	-216.5
73	DUMMY	-1030	-216.5
74	DUMMY	-970	-216.5
75	DUMMY	-910	-216.5
76	DUMMY	-850	-216.5
77	D<1>	-790	-216.5
78	D<3>	-730	-216.5
79	D<5>	-670	-216.5
80	D<7>	-610	-216.5
81	TE	-550	-216.5
82	RESX	-490	-216.5
83	CSX	-430	-216.5
84	D<6>	-370	-216.5
85	D<4>	-310	-216.5
86	D<2>	-250	-216.5

No.	Pad	X	Y
101	VSSR	550	-216.5
102	VSSR	600	-216.5
103	VDDI	650	-216.5
104	VDDI	700	-216.5
105	VDDI	750	-216.5
106	VDDI	800	-216.5
107	VDDI	850	-216.5
108	VDDI	900	-216.5
109	VPP	950	-216.5
110	VPP	1000	-216.5
111	VPP	1050	-216.5
112	VREF2P0_TEST	1100	-216.5
113	VREF2P0_TEST	1150	-216.5
114	VREF2P0_TEST	1200	-216.5
115	DVDD	1250	-216.5
116	DVDD	1300	-216.5
117	DVDD	1350	-216.5
118	TEST	1400	-216.5
119	TEST	1450	-216.5
120	AVDD	1500	-216.5
121	AVDD	1550	-216.5
122	AVDD	1600	-216.5
123	AVDD	1650	-216.5
124	AVDD	1700	-216.5
125	VREG_TEST	1750	-216.5
126	VREG_TEST	1800	-216.5
127	VREG_TEST	1850	-216.5
128	DMY	1900	-216.5
129	DMY	1950	-216.5
130	DUMMY	2000	-216.5
131	DUMMY	2050	-216.5
132	DUMMY	2100	-216.5
133	DUMMY	2150	-216.5
134	DUMMY	2200	-216.5
135	DUMMY	2250	-216.5
136	DUMMY	2300	-216.5

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37	GM<1>	-2950	-216.5
38	DMY	-2900	-216.5
39	GM<0>	-2850	-216.5
40	DMY	-2800	-216.5
41	DUMMY	-2750	-216.5
42	DUMMY	-2700	-216.5
43	SPI4W	-2650	-216.5
44	DMY	-2600	-216.5
45	OSC_IN	-2550	-216.5
46	DMY	-2500	-216.5
47	DMY	-2450	-216.5
48	VDH	-2400	-216.5
49	DMY	-2350	-216.5
50	DMY	-2300	-216.5

87	IM	-190	-216.5
88	D<0>	-130	-216.5
89	WRX	-70	-216.5
90	DUMMY	0	-216.5
91	DUMMY	50	-216.5
92	DUMMY	100	-216.5
93	DUMMY	150	-216.5
94	DUMMY	200	-216.5
95	OSC_TEST	250	-216.5
96	DUMMY	300	-216.5
97	VSSR	350	-216.5
98	VSSR	400	-216.5
99	VSSR	450	-216.5
100	VSSR	500	-216.5

137	DUMMY	2350	-216.5
138	DUMMY	2400	-216.5
139	DUMMY	2450	-216.5
140	DUMMY	2500	-216.5
141	DUMMY	2550	-216.5
142	DUMMY	2600	-216.5
143	DUMMY	2650	-216.5
144	DUMMY	2700	-216.5
145	DUMMY	2750	-216.5
146	VSSA	2800	-216.5
147	VSSA	2850	-216.5
148	VSSA	2900	-216.5
149	VCL	2950	-216.5
150	VCL	3000	-216.5

No.	Pad	X	Y
151	VCL	3050	-216.5
152	DUMMY	3100	-216.5
153	DUMMY	3150	-216.5
154	DUMMY	3200	-216.5
155	DUMMY	3250	-216.5
156	DUMMY	3300	-216.5
157	DUMMY	3350	-216.5
158	DUMMY	3400	-216.5
159	DUMMY	3450	-216.5
160	DUMMY	3500	-216.5
161	DMY	3550	-216.5
162	DMY	3600	-216.5
163	DMY	3650	-216.5
164	DMY	3700	-216.5
165	DMY	3750	-216.5
166	DMY	3800	-216.5
167	DMY	3850	-216.5
168	DMY	3900	-216.5
169	DMY	3950	-216.5
170	VGL	4000	-216.5
171	VGL	4050	-216.5
172	VGL	4100	-216.5
173	VGH	4150	-216.5
174	VGH	4200	-216.5

No.	Pad	X	Y
201	G<136>	4532	202
202	G<134>	4516	101
203	G<132>	4500	202
204	G<130>	4484	101
205	G<128>	4468	202
206	G<126>	4452	101
207	G<124>	4436	202
208	G<122>	4420	101
209	G<120>	4404	202
210	G<118>	4388	101
211	G<116>	4372	202
212	G<114>	4356	101
213	G<112>	4340	202
214	G<110>	4324	101
215	G<108>	4308	202
216	G<106>	4292	101
217	G<104>	4276	202
218	G<102>	4260	101
219	G<100>	4244	202
220	G<98>	4228	101
221	G<96>	4212	202
222	G<94>	4196	101
223	G<92>	4180	202
224	G<90>	4164	101

No.	Pad	X	Y
251	G<36>	3732	202
252	G<34>	3716	101
253	G<32>	3700	202
254	G<30>	3684	101
255	G<28>	3668	202
256	G<26>	3652	101
257	G<24>	3636	202
258	G<22>	3620	101
259	G<20>	3604	202
260	G<18>	3588	101
261	G<16>	3572	202
262	G<14>	3556	101
263	G<12>	3540	202
264	G<10>	3524	101
265	G<8>	3508	202
266	G<6>	3492	101
267	G<4>	3476	202
268	G<2>	3460	101
269	Dummy	3444	202
270	Dummy	3428	101
271	Dummy	3412	202
272	Dummy	3396	101
273	Dummy	3380	202
274	Dummy	3364	101

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175	VGH	4250	-216.5
176	VCOMH	4300	-216.5
177	VCOMH	4350	-216.5
178	VCOMH	4400	-216.5
179	VCOML	4450	-216.5
180	VCOML	4500	-216.5
181	VCOML	4550	-216.5
182	VCOM	4600	-216.5
183	VCOM	4650	-216.5
184	VCOM	4700	-216.5
185	DUMMY	4750	-216.5
186	Dummy	4772	101
187	Dummy	4756	202
188	G<162>	4740	101
189	G<160>	4724	202
190	G<158>	4708	101
191	G<156>	4692	202
192	G<154>	4676	101
193	G<152>	4660	202
194	G<150>	4644	101
195	G<148>	4628	202
196	G<146>	4612	101
197	G<144>	4596	202
198	G<142>	4580	101
199	G<140>	4564	202
200	G<138>	4548	101

225	G<88>	4148	202
226	G<86>	4132	101
227	G<84>	4116	202
228	G<82>	4100	101
229	G<80>	4084	202
230	G<78>	4068	101
231	G<76>	4052	202
232	G<74>	4036	101
233	G<72>	4020	202
234	G<70>	4004	101
235	G<68>	3988	202
236	G<66>	3972	101
237	G<64>	3956	202
238	G<62>	3940	101
239	G<60>	3924	202
240	G<58>	3908	101
241	G<56>	3892	202
242	G<54>	3876	101
243	G<52>	3860	202
244	G<50>	3844	101
245	G<48>	3828	202
246	G<46>	3812	101
247	G<44>	3796	202
248	G<42>	3780	101
249	G<40>	3764	202
250	G<38>	3748	101

275	Dummy	3348	202
276	Dummy	3332	101
277	Dummy	3316	202
278	Dummy	3300	101
279	S<384>	3284	202
280	S<383>	3268	101
281	S<382>	3252	202
282	S<381>	3236	101
283	S<380>	3220	202
284	S<379>	3204	101
285	S<378>	3188	202
286	S<377>	3172	101
287	S<376>	3156	202
288	S<375>	3140	101
289	S<374>	3124	202
290	S<373>	3108	101
291	S<372>	3092	202
292	S<371>	3076	101
293	S<370>	3060	202
294	S<369>	3044	101
295	S<368>	3028	202
296	S<367>	3012	101
297	S<366>	2996	202
298	S<365>	2980	101
299	S<364>	2964	202
300	S<363>	2948	101

No.	Pad	X	Y
301	S<362>	2932	202
302	S<361>	2916	101
303	S<360>	2900	202
304	S<359>	2884	101
305	S<358>	2868	202
306	S<357>	2852	101
307	S<356>	2836	202
308	S<355>	2820	101
309	S<354>	2804	202
310	S<353>	2788	101
311	S<352>	2772	202

No.	Pad	X	Y
351	S<312>	2132	202
352	S<311>	2116	101
353	S<310>	2100	202
354	S<309>	2084	101
355	S<308>	2068	202
356	S<307>	2052	101
357	S<306>	2036	202
358	S<305>	2020	101
359	S<304>	2004	202
360	S<303>	1988	101
361	S<302>	1972	202

No.	Pad	X	Y
401	S<262>	1332	202
402	S<261>	1316	101
403	S<260>	1300	202
404	S<259>	1284	101
405	S<258>	1268	202
406	S<257>	1252	101
407	S<256>	1236	202
408	S<255>	1220	101
409	S<254>	1204	202
410	S<253>	1188	101
411	S<252>	1172	202

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312	S<351>	2756	101
313	S<350>	2740	202
314	S<349>	2724	101
315	S<348>	2708	202
316	S<347>	2692	101
317	S<346>	2676	202
318	S<345>	2660	101
319	S<344>	2644	202
320	S<343>	2628	101
321	S<342>	2612	202
322	S<341>	2596	101
323	S<340>	2580	202
324	S<339>	2564	101
325	S<338>	2548	202
326	S<337>	2532	101
327	S<336>	2516	202
328	S<335>	2500	101
329	S<334>	2484	202
330	S<333>	2468	101
331	S<332>	2452	202
332	S<331>	2436	101
333	S<330>	2420	202
334	S<329>	2404	101
335	S<328>	2388	202
336	S<327>	2372	101
337	S<326>	2356	202
338	S<325>	2340	101
339	S<324>	2324	202
340	S<323>	2308	101
341	S<322>	2292	202
342	S<321>	2276	101
343	S<320>	2260	202
344	S<319>	2244	101
345	S<318>	2228	202
346	S<317>	2212	101
347	S<316>	2196	202
348	S<315>	2180	101
349	S<314>	2164	202
350	S<313>	2148	101

362	S<301>	1956	101
363	S<300>	1940	202
364	S<299>	1924	101
365	S<298>	1908	202
366	S<297>	1892	101
367	S<296>	1876	202
368	S<295>	1860	101
369	S<294>	1844	202
370	S<293>	1828	101
371	S<292>	1812	202
372	S<291>	1796	101
373	S<290>	1780	202
374	S<289>	1764	101
375	S<288>	1748	202
376	S<287>	1732	101
377	S<286>	1716	202
378	S<285>	1700	101
379	S<284>	1684	202
380	S<283>	1668	101
381	S<282>	1652	202
382	S<281>	1636	101
383	S<280>	1620	202
384	S<279>	1604	101
385	S<278>	1588	202
386	S<277>	1572	101
387	S<276>	1556	202
388	S<275>	1540	101
389	S<274>	1524	202
390	S<273>	1508	101
391	S<272>	1492	202
392	S<271>	1476	101
393	S<270>	1460	202
394	S<269>	1444	101
395	S<268>	1428	202
396	S<267>	1412	101
397	S<266>	1396	202
398	S<265>	1380	101
399	S<264>	1364	202
400	S<263>	1348	101

412	S<251>	1156	101
413	S<250>	1140	202
414	S<249>	1124	101
415	S<248>	1108	202
416	S<247>	1092	101
417	S<246>	1076	202
418	S<245>	1060	101
419	S<244>	1044	202
420	S<243>	1028	101
421	S<242>	1012	202
422	S<241>	996	101
423	S<240>	980	202
424	S<239>	964	101
425	S<238>	948	202
426	S<237>	932	101
427	S<236>	916	202
428	S<235>	900	101
429	S<234>	884	202
430	S<233>	868	101
431	S<232>	852	202
432	S<231>	836	101
433	S<230>	820	202
434	S<229>	804	101
435	S<228>	788	202
436	S<227>	772	101
437	S<226>	756	202
438	S<225>	740	101
439	S<224>	724	202
440	S<223>	708	101
441	S<222>	692	202
442	S<221>	676	101
443	S<220>	660	202
444	S<219>	644	101
445	S<218>	628	202
446	S<217>	612	101
447	S<216>	596	202
448	S<215>	580	101
449	S<214>	564	202
450	S<213>	548	101

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No.	Pad	X	Y
452	S<211>	516	101
453	S<210>	500	202
454	S<209>	484	101
455	S<208>	468	202
456	S<207>	452	101
457	S<206>	436	202
458	S<205>	420	101
459	S<204>	404	202
460	S<203>	388	101
461	S<202>	372	202
462	S<201>	356	101
463	S<200>	340	202
464	S<199>	324	101
465	S<198>	308	202
466	S<197>	292	101
467	S<196>	276	202
468	S<195>	260	101
469	S<194>	244	202
470	S<193>	228	101
471	GAM_TEST_P	212	202
472	OTP_TEST	-212	202
473	S<192>	-228	101
474	S<191>	-244	202
475	S<190>	-260	101
476	S<189>	-276	202
477	S<188>	-292	101
478	S<187>	-308	202
479	S<186>	-324	101
480	S<185>	-340	202
481	S<184>	-356	101
482	S<183>	-372	202
483	S<182>	-388	101
484	S<181>	-404	202
485	S<180>	-420	101
486	S<179>	-436	202
487	S<178>	-452	101
488	S<177>	-468	202
489	S<176>	-484	101
490	S<175>	-500	202

No.	Pad	X	Y
501	S<164>	-676	101
502	S<163>	-692	202
503	S<162>	-708	101
504	S<161>	-724	202
505	S<160>	-740	101
506	S<159>	-756	202
507	S<158>	-772	101
508	S<157>	-788	202
509	S<156>	-804	101
510	S<155>	-820	202
511	S<154>	-836	101
512	S<153>	-852	202
513	S<152>	-868	101
514	S<151>	-884	202
515	S<150>	-900	101
516	S<149>	-916	202
517	S<148>	-932	101
518	S<147>	-948	202
519	S<146>	-964	101
520	S<145>	-980	202
521	S<144>	-996	101
522	S<143>	-1012	202
523	S<142>	-1028	101
524	S<141>	-1044	202
525	S<140>	-1060	101
526	S<139>	-1076	202
527	S<138>	-1092	101
528	S<137>	-1108	202
529	S<136>	-1124	101
530	S<135>	-1140	202
531	S<134>	-1156	101
532	S<133>	-1172	202
533	S<132>	-1188	101
534	S<131>	-1204	202
535	S<130>	-1220	101
536	S<129>	-1236	202
537	S<128>	-1252	101
538	S<127>	-1268	202
539	S<126>	-1284	101

No.	Pad	X	Y
551	S<114>	-1476	101
552	S<113>	-1492	202
553	S<112>	-1508	101
554	S<111>	-1524	202
555	S<110>	-1540	101
556	S<109>	-1556	202
557	S<108>	-1572	101
558	S<107>	-1588	202
559	S<106>	-1604	101
560	S<105>	-1620	202
561	S<104>	-1636	101
562	S<103>	-1652	202
563	S<102>	-1668	101
564	S<101>	-1684	202
565	S<100>	-1700	101
566	S<99>	-1716	202
567	S<98>	-1732	101
568	S<97>	-1748	202
569	S<96>	-1764	101
570	S<95>	-1780	202
571	S<94>	-1796	101
572	S<93>	-1812	202
573	S<92>	-1828	101
574	S<91>	-1844	202
575	S<90>	-1860	101
576	S<89>	-1876	202
577	S<88>	-1892	101
578	S<87>	-1908	202
579	S<86>	-1924	101
580	S<85>	-1940	202
581	S<84>	-1956	101
582	S<83>	-1972	202
583	S<82>	-1988	101
584	S<81>	-2004	202
585	S<80>	-2020	101
586	S<79>	-2036	202
587	S<78>	-2052	101
588	S<77>	-2068	202
589	S<76>	-2084	101

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491	S<174>	-516	101
492	S<173>	-532	202
493	S<172>	-548	101
494	S<171>	-564	202
495	S<170>	-580	101
496	S<169>	-596	202
497	S<168>	-612	101
498	S<167>	-628	202
499	S<166>	-644	101
500	S<165>	-660	202
452	S<211>	516	101

540	S<125>	-1300	202
541	S<124>	-1316	101
542	S<123>	-1332	202
543	S<122>	-1348	101
544	S<121>	-1364	202
545	S<120>	-1380	101
546	S<119>	-1396	202
547	S<118>	-1412	101
548	S<117>	-1428	202
549	S<116>	-1444	101
550	S<115>	-1460	202

590	S<75>	-2100	202
591	S<74>	-2116	101
592	S<73>	-2132	202
593	S<72>	-2148	101
594	S<71>	-2164	202
595	S<70>	-2180	101
596	S<69>	-2196	202
597	S<68>	-2212	101
598	S<67>	-2228	202
599	S<66>	-2244	101
600	S<65>	-2260	202

No.	Pad	X	Y
601	S<64>	-2276	101
602	S<63>	-2292	202
603	S<62>	-2308	101
604	S<61>	-2324	202
605	S<60>	-2340	101
606	S<59>	-2356	202
607	S<58>	-2372	101
608	S<57>	-2388	202
609	S<56>	-2404	101
610	S<55>	-2420	202
611	S<54>	-2436	101
612	S<53>	-2452	202
613	S<52>	-2468	101
614	S<51>	-2484	202
615	S<50>	-2500	101
616	S<49>	-2516	202
617	S<48>	-2532	101
618	S<47>	-2548	202
619	S<46>	-2564	101
620	S<45>	-2580	202
621	S<44>	-2596	101
622	S<43>	-2612	202
623	S<42>	-2628	101
624	S<41>	-2644	202
625	S<40>	-2660	101
626	S<39>	-2676	202
627	S<38>	-2692	101
628	S<37>	-2708	202

No.	Pad	X	Y
651	S<14>	-3076	101
652	S<13>	-3092	202
653	S<12>	-3108	101
654	S<11>	-3124	202
655	S<10>	-3140	101
656	S<9>	-3156	202
657	S<8>	-3172	101
658	S<7>	-3188	202
659	S<6>	-3204	101
660	S<5>	-3220	202
661	S<4>	-3236	101
662	S<3>	-3252	202
663	S<2>	-3268	101
664	S<1>	-3284	202
665	Dummy	-3300	101
666	Dummy	-3316	202
667	Dummy	-3332	101
668	Dummy	-3348	202
669	Dummy	-3364	101
670	Dummy	-3380	202
671	Dummy	-3396	101
672	Dummy	-3412	202
673	Dummy	-3428	101
674	Dummy	-3444	202
675	G<1>	-3460	101
676	G<3>	-3476	202
677	G<5>	-3492	101
678	G<7>	-3508	202

No.	Pad	X	Y
701	G<53>	-3876	101
702	G<55>	-3892	202
703	G<57>	-3908	101
704	G<59>	-3924	202
705	G<61>	-3940	101
706	G<63>	-3956	202
707	G<65>	-3972	101
708	G<67>	-3988	202
709	G<69>	-4004	101
710	G<71>	-4020	202
711	G<73>	-4036	101
712	G<75>	-4052	202
713	G<77>	-4068	101
714	G<79>	-4084	202
715	G<81>	-4100	101
716	G<83>	-4116	202
717	G<85>	-4132	101
718	G<87>	-4148	202
719	G<89>	-4164	101
720	G<91>	-4180	202
721	G<93>	-4196	101
722	G<95>	-4212	202
723	G<97>	-4228	101
724	G<99>	-4244	202
725	G<101>	-4260	101
726	G<103>	-4276	202
727	G<105>	-4292	101
728	G<107>	-4308	202

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629	S<36>	-2724	101
630	S<35>	-2740	202
631	S<34>	-2756	101
632	S<33>	-2772	202
633	S<32>	-2788	101
634	S<31>	-2804	202
635	S<30>	-2820	101
636	S<29>	-2836	202
637	S<28>	-2852	101
638	S<27>	-2868	202
639	S<26>	-2884	101
640	S<25>	-2900	202
641	S<24>	-2916	101
642	S<23>	-2932	202
643	S<22>	-2948	101
644	S<21>	-2964	202
645	S<20>	-2980	101
646	S<19>	-2996	202
647	S<18>	-3012	101
648	S<17>	-3028	202
649	S<16>	-3044	101
650	S<15>	-3060	202

679	G<9>	-3524	101
680	G<11>	-3540	202
681	G<13>	-3556	101
682	G<15>	-3572	202
683	G<17>	-3588	101
684	G<19>	-3604	202
685	G<21>	-3620	101
686	G<23>	-3636	202
687	G<25>	-3652	101
688	G<27>	-3668	202
689	G<29>	-3684	101
690	G<31>	-3700	202
691	G<33>	-3716	101
692	G<35>	-3732	202
693	G<37>	-3748	101
694	G<39>	-3764	202
695	G<41>	-3780	101
696	G<43>	-3796	202
697	G<45>	-3812	101
698	G<47>	-3828	202
699	G<49>	-3844	101
700	G<51>	-3860	202

729	G<109>	-4324	101
730	G<111>	-4340	202
731	G<113>	-4356	101
732	G<115>	-4372	202
733	G<117>	-4388	101
734	G<119>	-4404	202
735	G<121>	-4420	101
736	G<123>	-4436	202
737	G<125>	-4452	101
738	G<127>	-4468	202
739	G<129>	-4484	101
740	G<131>	-4500	202
741	G<133>	-4516	101
742	G<135>	-4532	202
743	G<137>	-4548	101
744	G<139>	-4564	202
745	G<141>	-4580	101
746	G<143>	-4596	202
747	G<145>	-4612	101
748	G<147>	-4628	202
749	G<149>	-4644	101
750	G<151>	-4660	202

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No.	Pad	X	Y
751	G<153>	-4676	101
752	G<155>	-4692	202
753	G<157>	-4708	101
754	G<159>	-4724	202
755	G<161>	-4740	101
756	Dummy	-4756	202
757	Dummy	-4772	101

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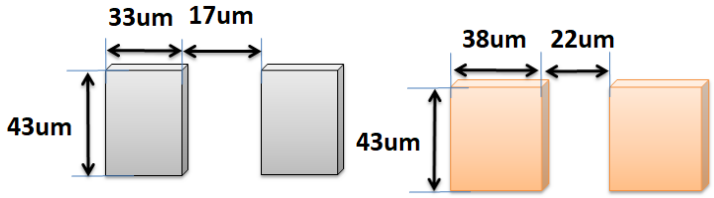
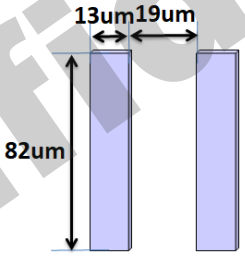
Input Pad



ILB Information				
X	Y	Area	Pad	Total Area
33	43	1419	158	224,202
38	43	1634	27	44,118
(um)	(um)	(um²)	counts	(um²)

Output Pad



OLB Information				
X	Y	Area	Pad	Total Area
13	82	1066	572	609,752
(um)	(um)	(um²)	counts	(um²)

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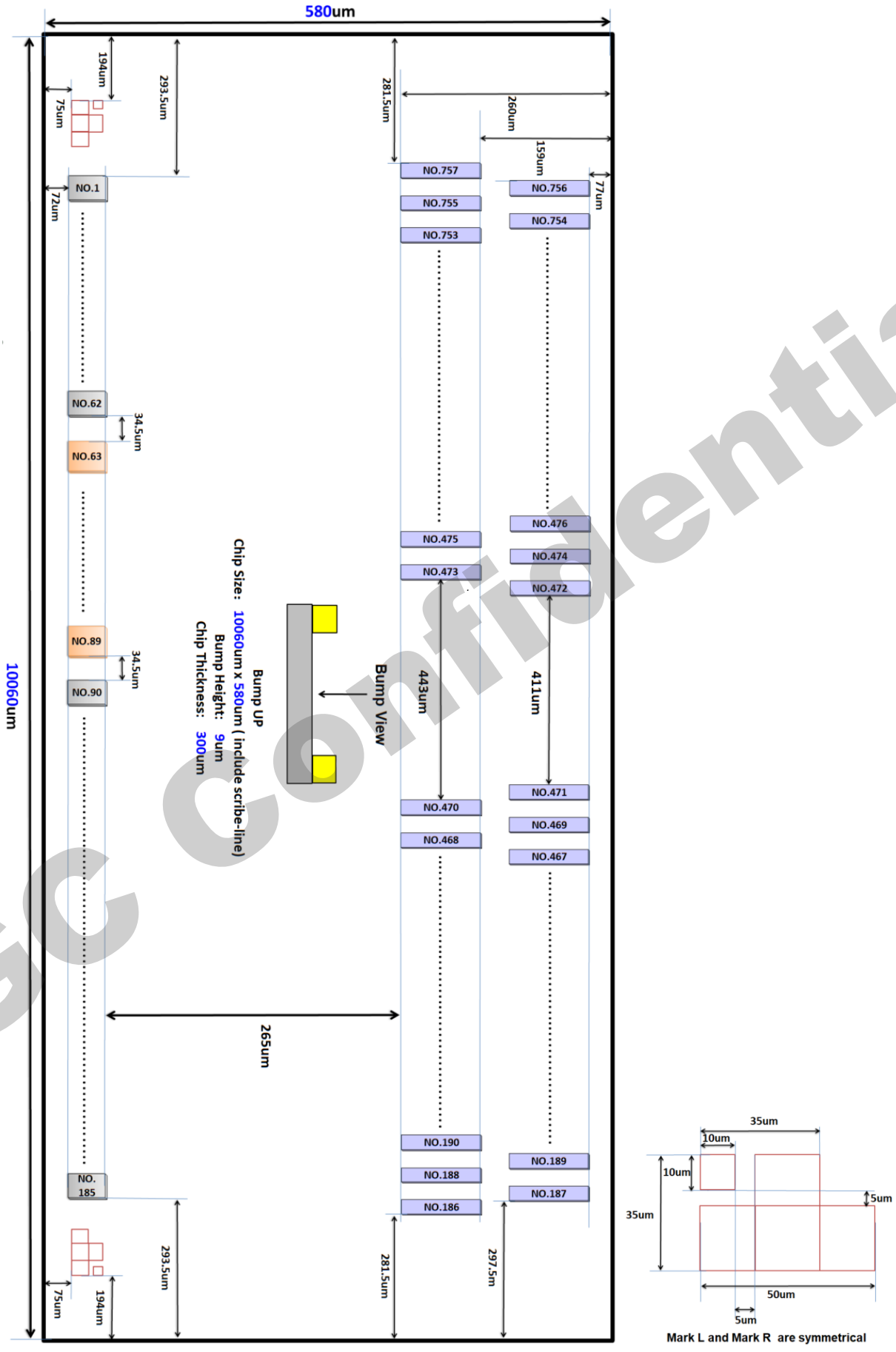

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4. Interface setting

4.1. MCU interfaces

GC9107 provides the 8-bit parallel system interface for 8080, and 3-/4-line serial system interface for serial data input. The input system interface is selected by external pins IM [2] and the bit formal per pixel color order is selected by IFPF [2:0] bits of 3Ah register.

4.1.1. MCU interface selection

The selection of interface is done by setting external pins SPI4W, IM, as shown in the following table.

SPI4W	IM	MCU-Interface Mode	Pins in use	
			Register/Content	GRAM
X	1	8080 MCU 8-bit bus interface	D[7:0]	D[7:0],WRX,RDX,CSX,D/CX
0	0	serial interface 3 line	SCL,SDA,CSX	
1	0	serial interface 4 line	SCL,SDA,CSX,RS	

4.1.2. 8080 Series Parallel Interface

GC9107 can be accessed via 8-bit MCU 8080 series parallel interface. The chip select CSX (active low) is used to enable or disable GC9107 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and
D [7:0] is parallel data bus.

GC9107 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [7:0] bits are display RAM data or command's parameters. When D/CX='0', D [7:0] bits are commands.
The 8080 series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080 Interface selection is done when P68 pin is low state (VSSR level). The selection of 8080 series parallel interface is shown as the table in the following.

SPI4W	IM	MPU-interface	CSX	WRX	RDX	D/CX	Function
X	1	8-bit parallel	"L"	↑	"H"	"L"	Write command code.
			"L"	"H"	↑	"H"	Read internal status.
			"L"	↑	"H"	"H"	Write parameter or display data.
			"L"	"H"	↑	"H"	Reads parameter or display data.

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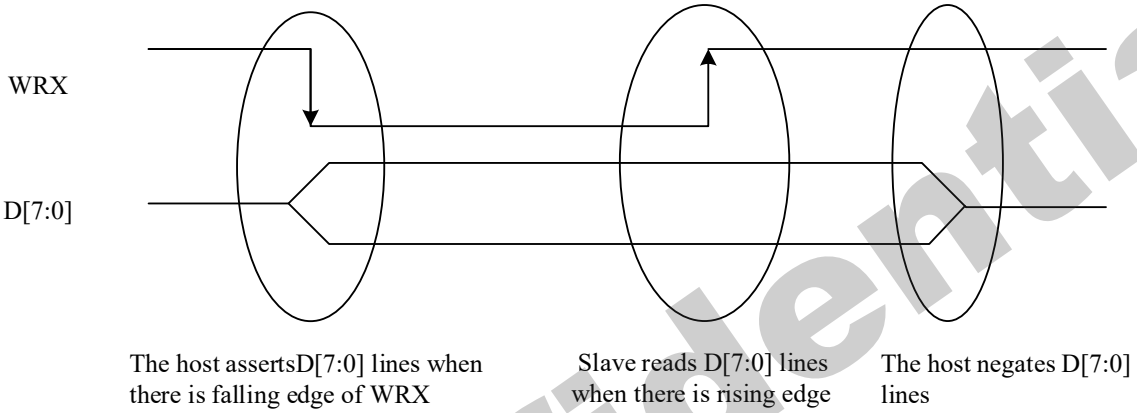
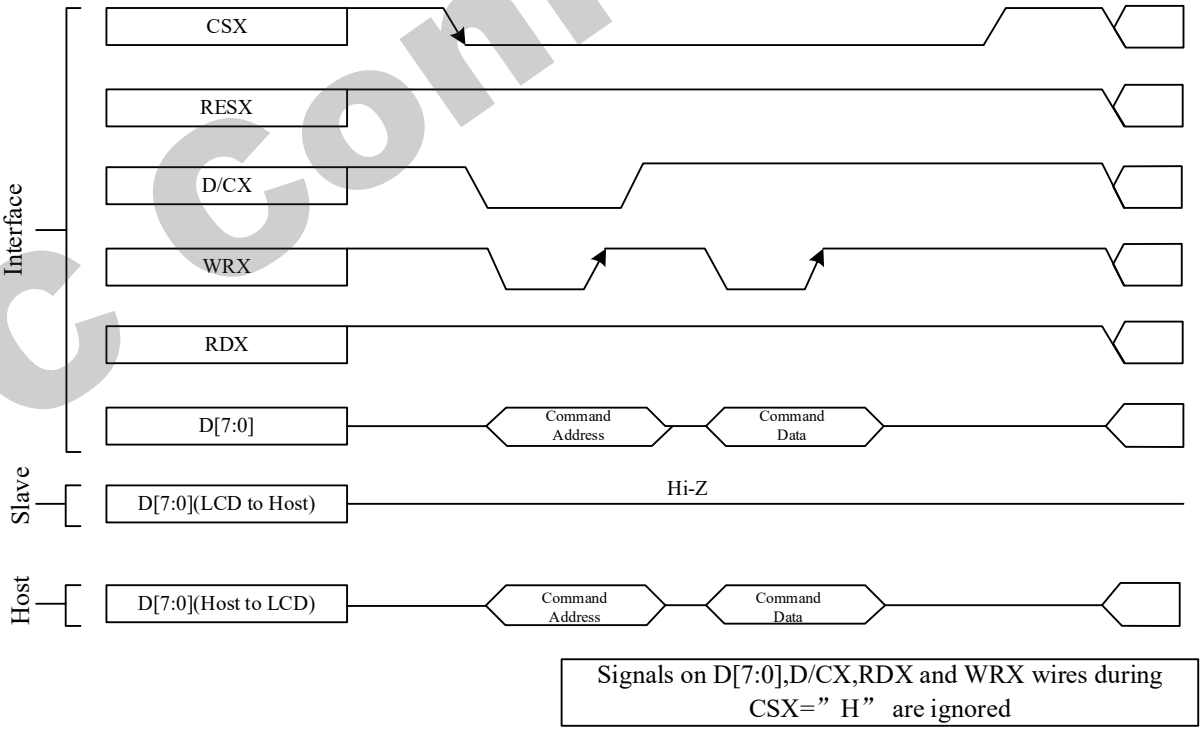
4.1.3. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080 MCU interface.



Note: WRX is an unsynchronized signal (It can be stopped)



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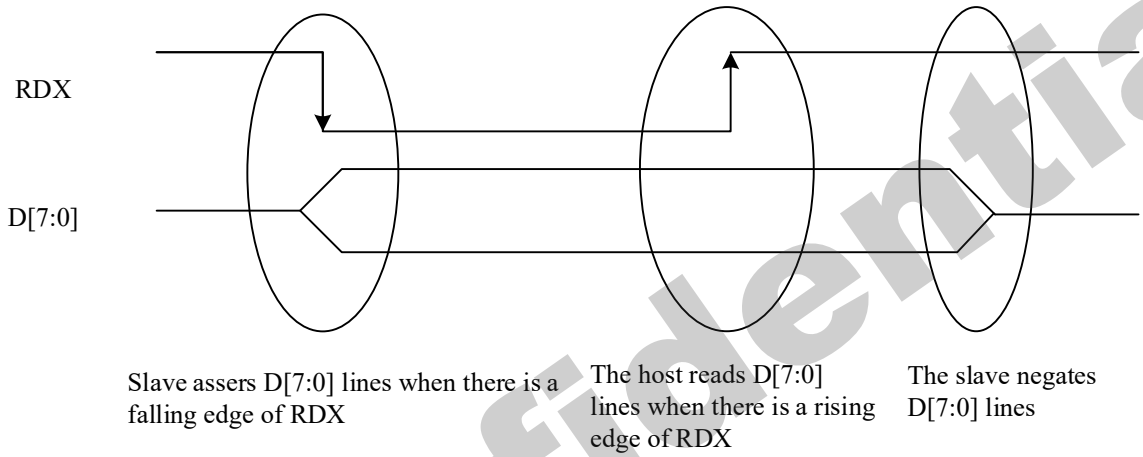
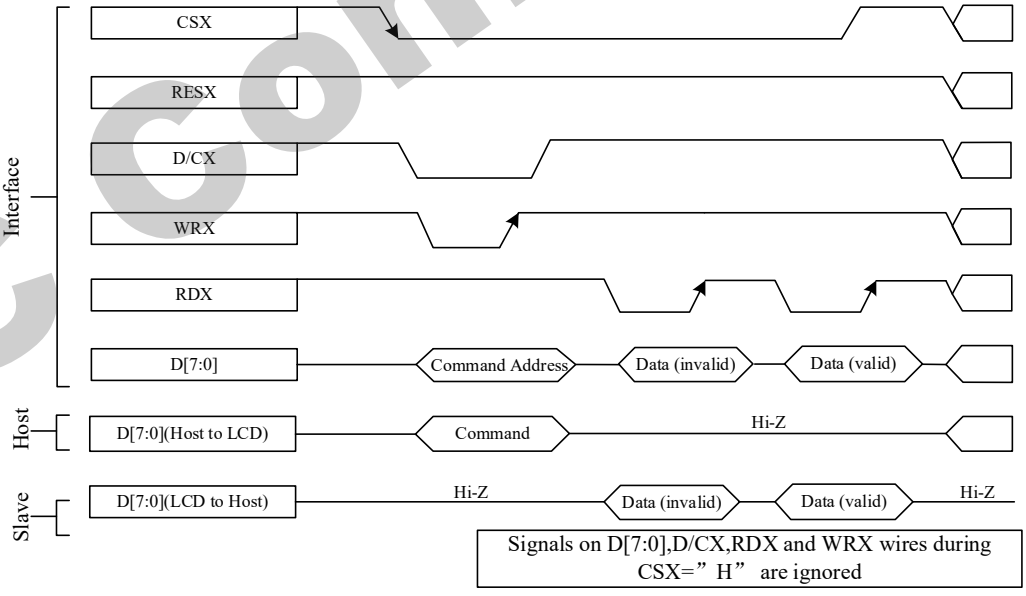
4.1.4. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080 MCU interface.



Note: RDX is an unsynchronized signal (It can be stopped).



Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.

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4.1.5. Serial Interface

The selection of interface is done by IM bit. Please refer to the Table in the following.

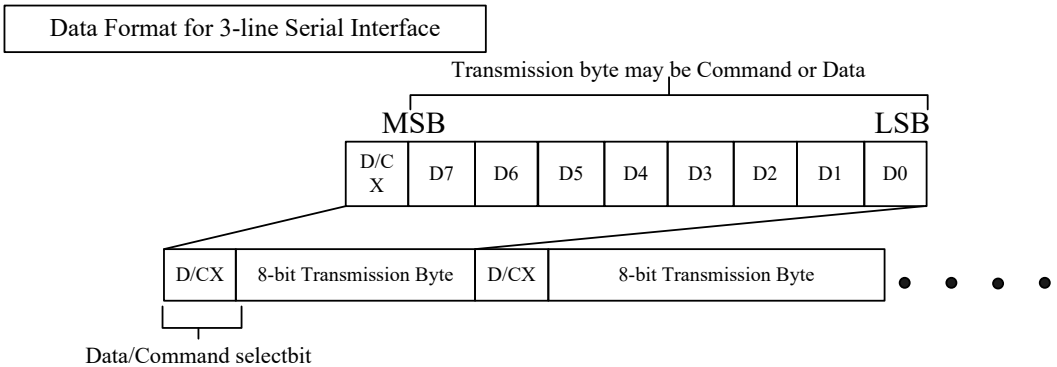
IM	SPI4W	MCU-Interface Mode	CSX	D/CX	SCL	Function
0	0	3-line serial interface	“L”	-	↑	Read/Write command, parameter or display data.
0	1	4-line serial interface	“L”	"H/L"	↑	Read/Write command, parameter or display data.

GC9107 supplies 3-lines/ 9-bit and 4-line/8-bit bi-directional serial interfaces for communication between host and GC9107. The 3-line serial mode consists of the chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (D0/SDA). The 4-line serial mode consists of the Data/Command selection input (D/CX), chip enable input (CSX), the serial clock input (SCL) and serial data Input/Output (D0/SDA) for data transmission. The data bus (D [7:1]), which are not used, must be connected to GND. Serial clock (SCL) is used for interface with MCU only, so it can be stopped when no communication is necessary.

4.1.6. Write Cycle Sequence

The write mode of the interface means that host writes commands or data to GC9107. The 3-lines serial data packet contains a data/command select bit (D/CX) and a transmission byte. If the D/CX bit is “low”, the transmission byte is interpreted as a command byte. If the D/CX bit is “high”, the transmission byte is stored as the display data RAM (Memory write command),or command register as parameter.

Any instruction can be sent in any order to GC9107 and the MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse and SDA data are no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission. See the detailed data format for 3-/4-line serial interface.



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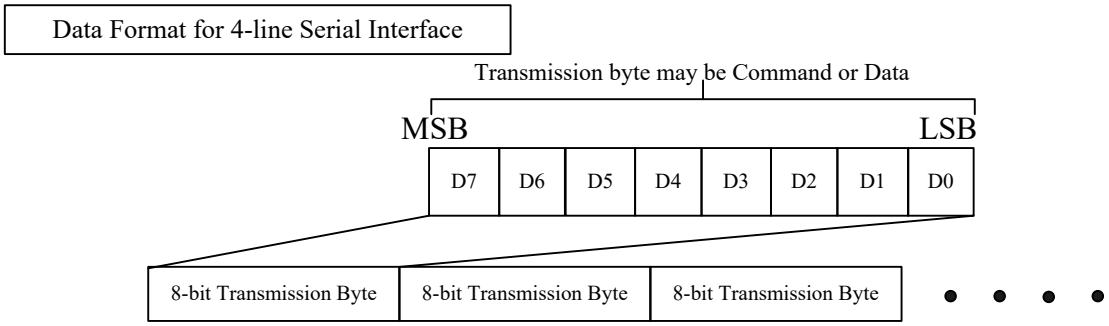
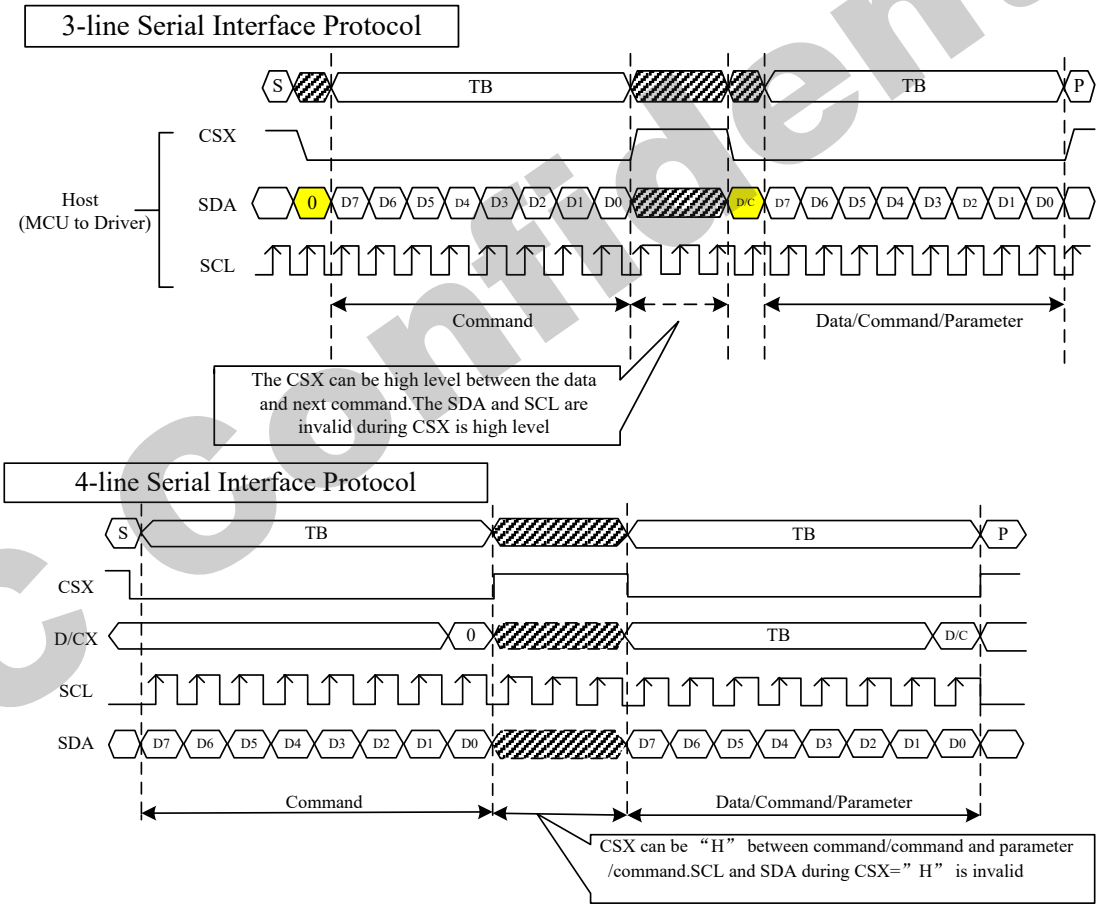


Host processor drives the CSX pin to low and starts by setting the D/CX bit on SDA. The bit is read by GC9107 on the first rising edge of SCL signal. On the next falling edge of SCL, the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL, the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle width. The 3/4-line serial interface writes sequence described in the figure as below.



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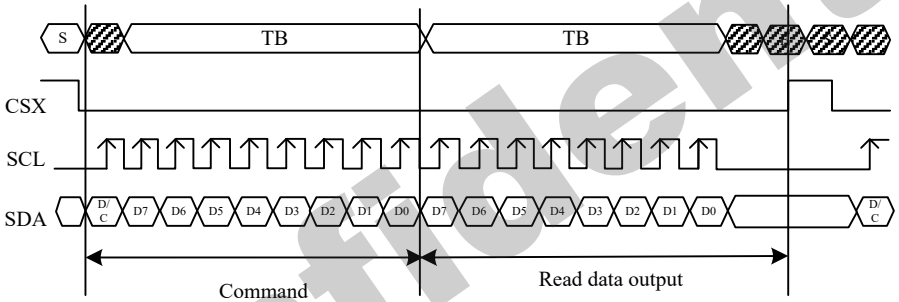
4.1.7. Read Cycle Sequence

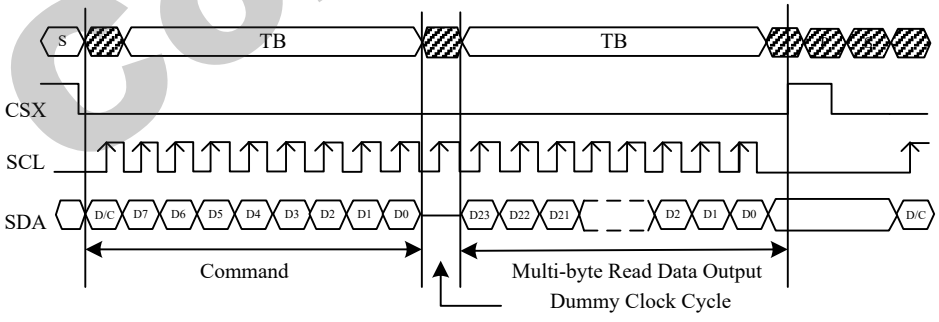
The read mode of interface means that the host reads register's parameter from GC9107. The host has to send a command (Read ID or register command) and then the following byte is transmitted in the opposite direction. GC9107 latches the SDA (input data) at the rising edges of SCL (serial clock), and then shifts SDA (output data) at falling edges of SCL (serial clock). After the read status command has been sent, the SDA line must be set to tri-state and no later than at the falling edge of SCL of the last bit. The read mode has three types of transmitted command data (8-/24-/32-bit) according command code.

3-wire Serial Interface Protocol

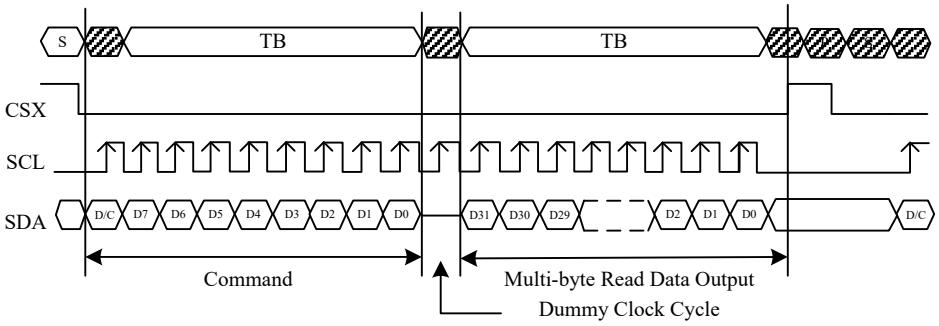
3-wire Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command:8-bit read)



3-wire Serial Protocol (for RDDID command:24-bit read)



3-wire Serial Protocol (for RDDST command:32-bit read)



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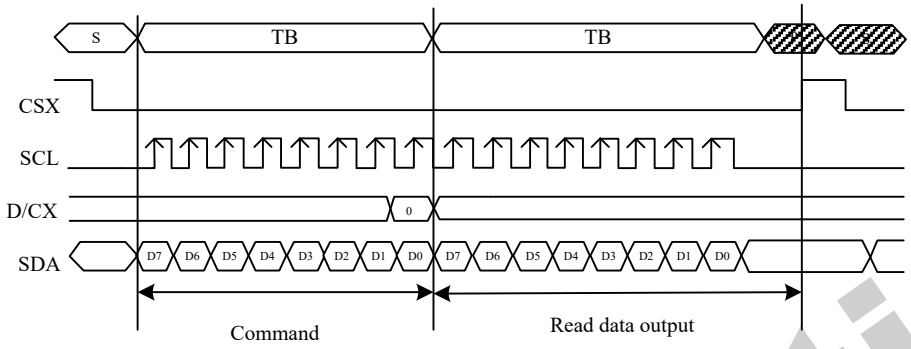
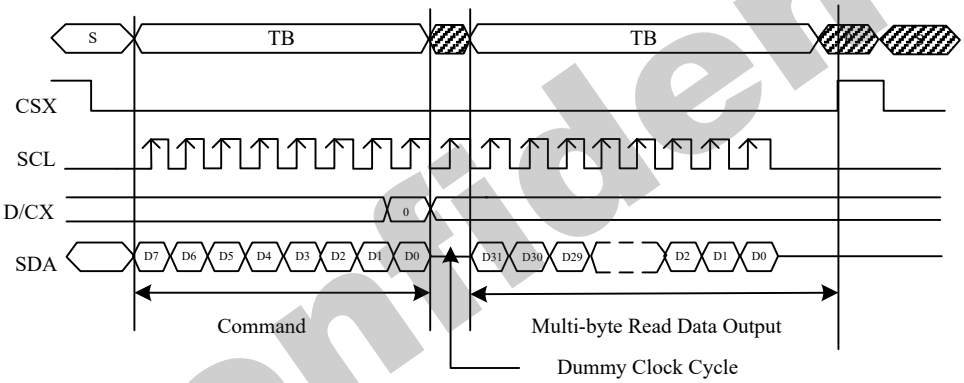
4-wire Serial Interface Protocol

4-wire Serial Protocol (for RDID1/RDID2/RDID3/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh command:8-bit read)



4-wire Serial Protocol (for RDDST command:32-bit read)



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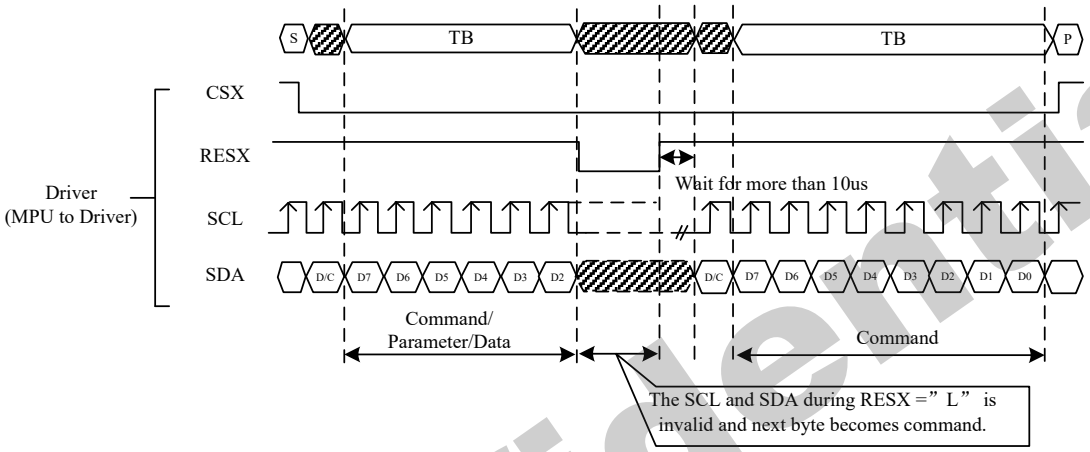
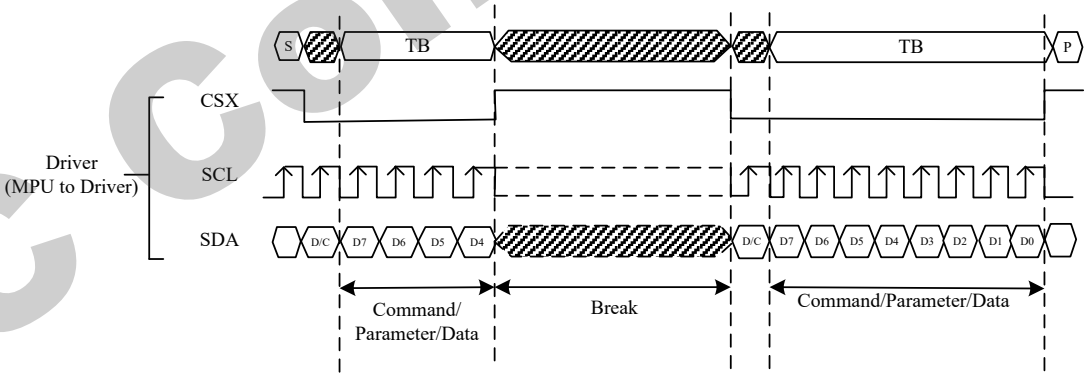
4.1.8. Data Transfer Break and Recovery

If there is a break in data transmission by RESX pulse, while transferring a command or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive command data again when the chip select pin (CSX) is activated after RESX have been high state.



If there is a break in data transmission by CSX pulse, while transferring a command or frame memory data or multiple parameter command data, before Bit D0 of the byte has been completed, then the driver will reject the previous bits and have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select pin (CSX) is next activated.



If a two or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than continue to send the remained parameters that was interrupted, then the parameters which had been successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown below.

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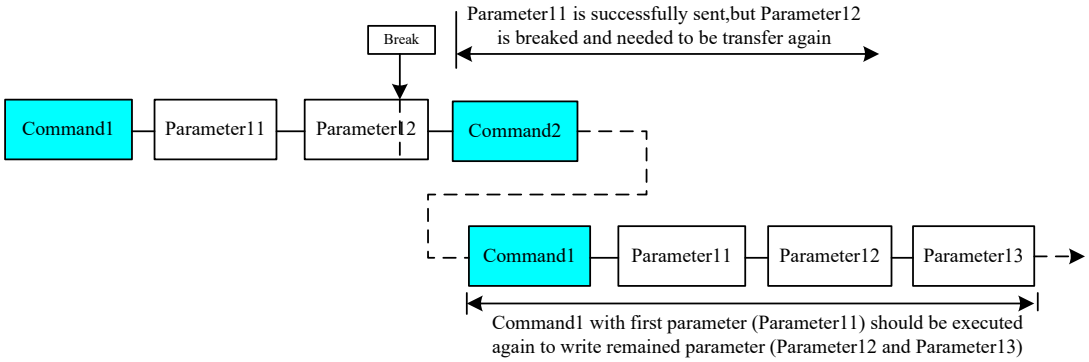
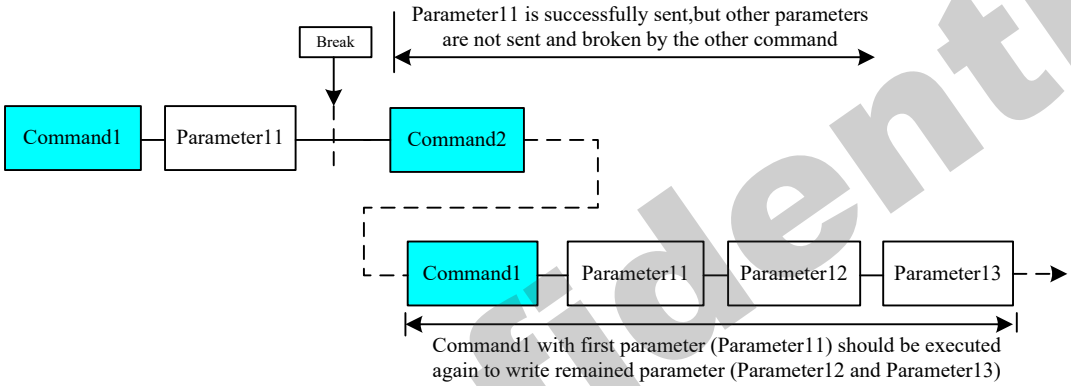


If a two or more parameter command is being sent and a break occurs by the other command before the last one is sent, then the parameters which had been successfully sent are stored and the other parameter of that command remains previous value.



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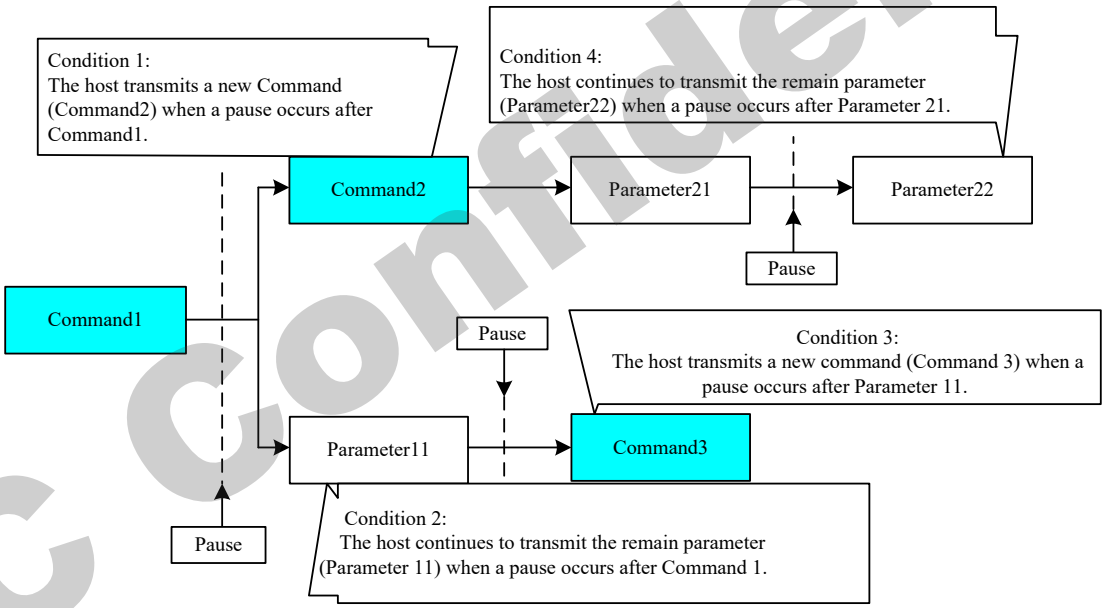
4.1.9. Data Transfer Pause

It will be possible when transferring a command, frame memory data or multiple parameter data to invoke a pause in the data transmission. If the chip select pin (CSX) is released to high state after a whole byte of a frame memory data or multiple parameter data has been completed, then GC9107 will wait and continue the frame memory data or parameter data transmission from the point where it was paused. If the chip select pin is released after a whole byte of a command has been completed, then the display module will receive either the command's parameters (if appropriate) or a new command when the chip select pin is next enabled as shown below.

This applies to the following 4 conditions:
1) Command-Pause-Command
2) Command-Pause-Parameter
3) Parameter-Pause-Command
4) Parameter-Pause-Parameter



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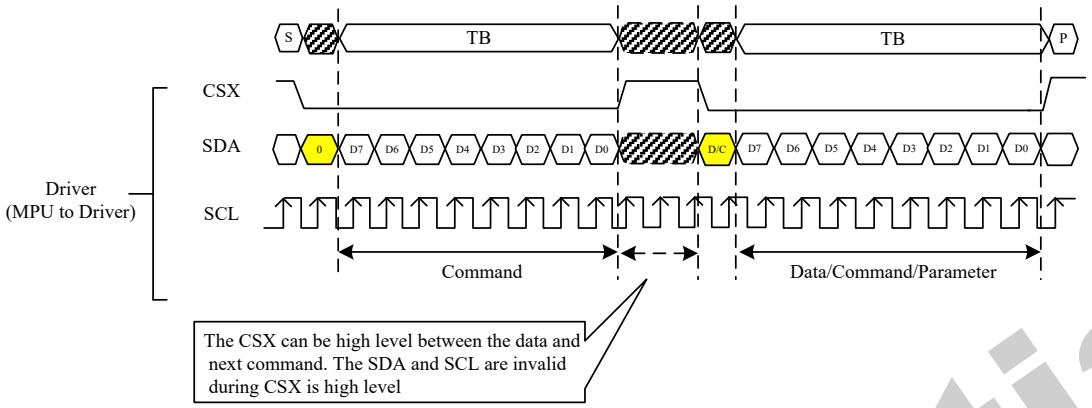
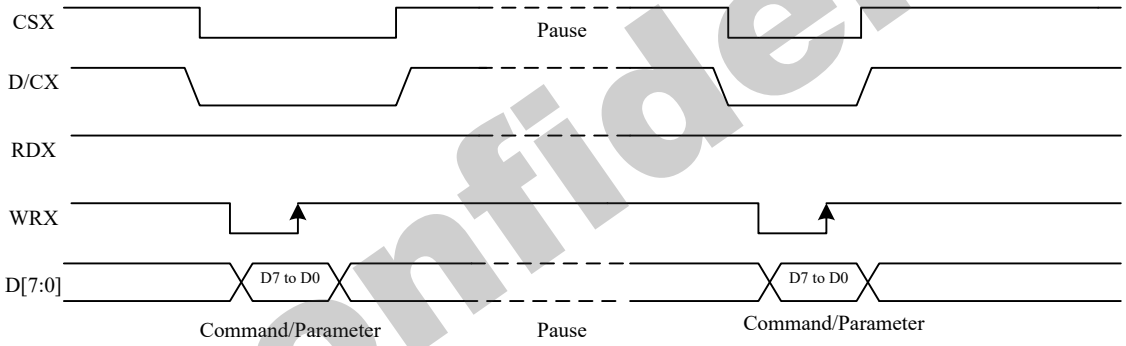
4.1.10. Serial Interface Pause



4.1.11. Parallel Interface Pause

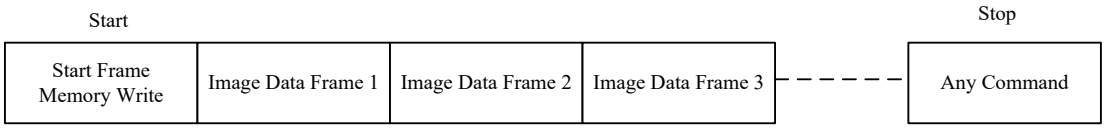


4.1.12. Data Transfer Mode

GC9107 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

4.1.13. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.



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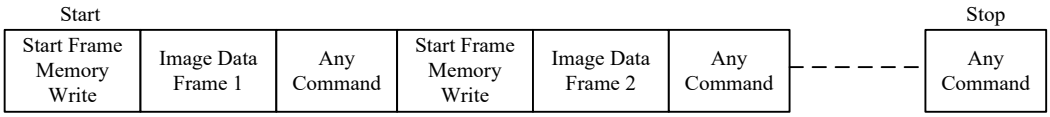
4.1.14. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.



Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.
Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.

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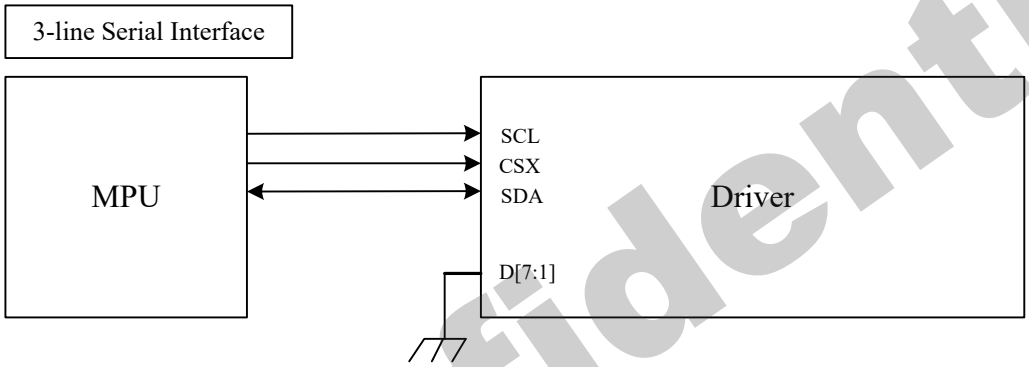
4.2. Display Data Format

GC9107 supplies 8-bit parallel MCU interface with 8080 series, 3-/4-line serial interface. The parallel MCU interface and serial interface mode can be selected by external pins IM and SPI4W.

4.2.1. 3-line Serial Interface

The 3-line/9-bit serial bus interface of GC9107 can be used by setting external pin as IM to “0” and SPI4W to “0”. The shown figure is the example of 3-line SPI interface.

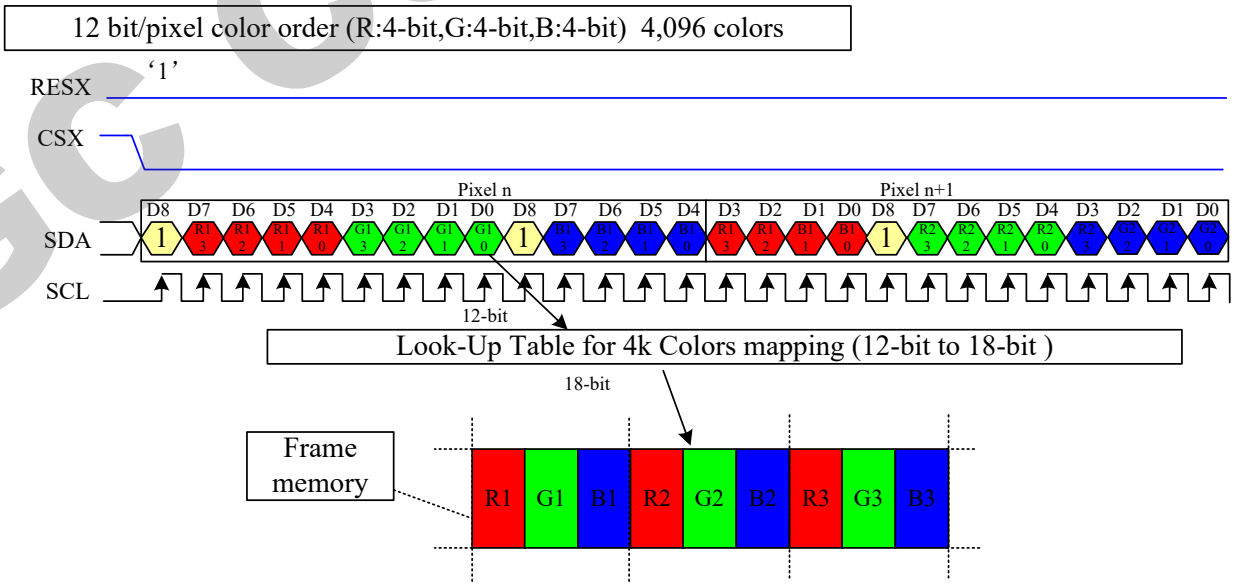


In 3-line serial interface, different display data format is available for three color depths supported by the LCM listed below.

-4k color, RGB 4, 4, 4, -bits input

-65k colors, RGB 5, 6, 5 -bits input

-262k colors, RGB 6, 6, 6 -bits input.



Two pixel (3 sub-pixels) display data is sent by 3 byte transfers when IFPF [2:0] bits of 3Ah register are set to “011”.

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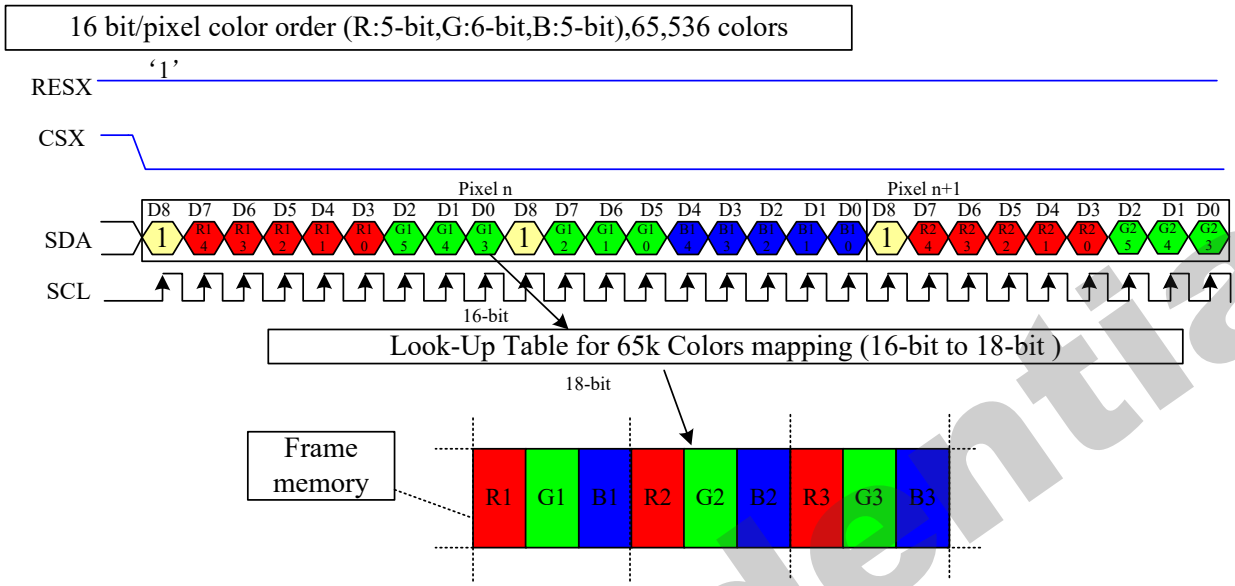
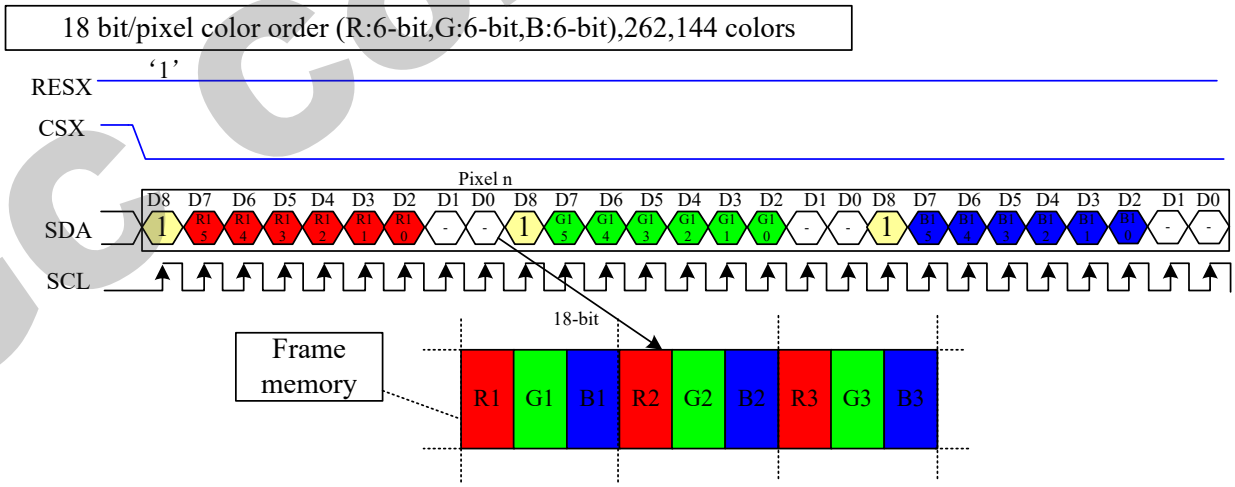
Note 1: The pixel data with 12-bit color depth information.
Note 2: The most significant bits are: Rx3, Gx3 and Bx3.
Note 3: The least significant bits are: Rx0, Gx0 and Bx0.
Note 4: '-'= don't care –Can be set "0" or "1".



One pixel (3 sub-pixels) display data is sent by 2 byte transfers when IFPF [2:0] bits of 3Ah register are set to "101".

Note 1: The pixel data with 16-bit color depth information.
Note 2: The most significant bits are: Rx4, Gx5 and Bx4.
Note 3: The least significant bits are: Rx0, Gx0 and Bx0.
Note 4: '-'= don't care –Can be set "0" or "1".



One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when IFPF [2:0] bits of 3Ah register are set to "110".

Note 1: The pixel data with 18-bit color depth information.
Note 2: The most significant bits are: Rx5, Gx5 and Bx5.
Note 3: The least significant bits are : Rx0, Gx0 and Bx0.
Note 4: '-'= don't care - Can be set "0" or "1".

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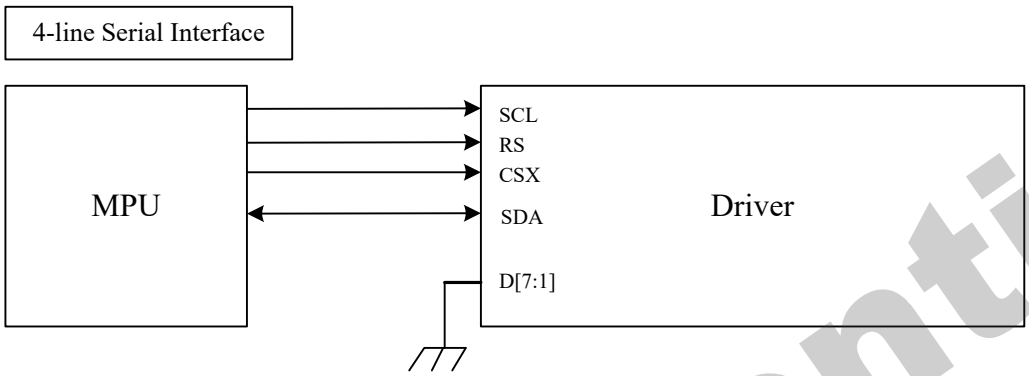
4.2.2. 4-line Serial Interface

The 4-line/8-bit serial bus interface of GC9107 can be used by setting external pin as IM to “0” and SPI4W to “1”. The shown figure is the example of 4-line SPI interface.

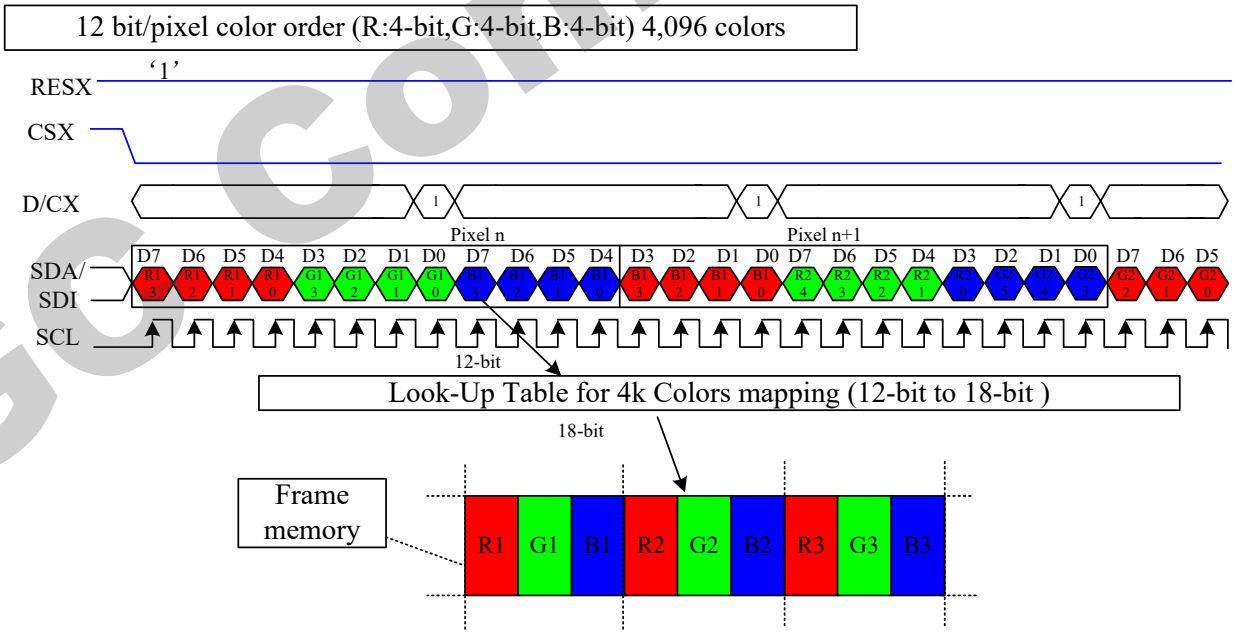


In 4-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-4Kk color, RGB 4, 4, 4 -bits input.

-65k colors, RGB 5, 6, 5 -bits input.

-262k colors, RGB 6, 6, 6 -bits input.



Two pixel (3 sub-pixels) display data is sent by 3 byte transfers when IFPF [2:0] bits of 3Ah register are set to “011”.

Note 1: The pixel data with 12-bit color depth information.

Note 2: The most significant bits are: Rx3, Gx3 and Bx3.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

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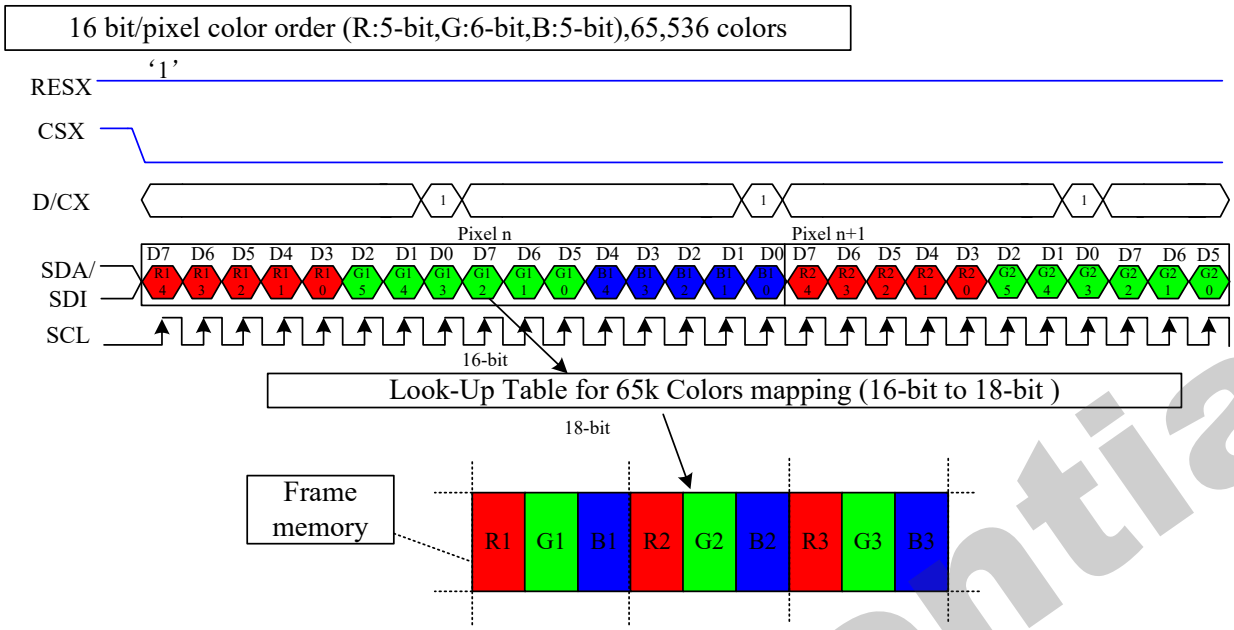
Note 4: '-'= don't care –Can be set "0" or "1".



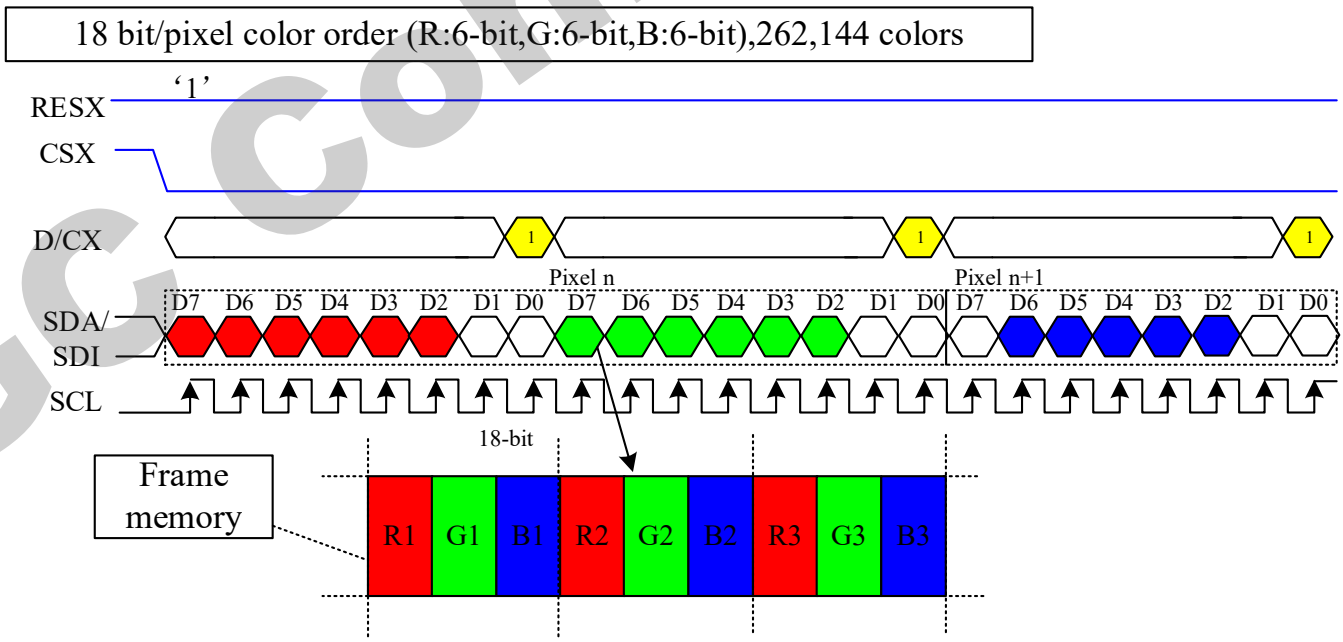
One pixel (3 sub-pixels) display data is sent by 2 byte transfers when IFPF [2:0] bits of 3Ah register are set to "101".

Note 1: The pixel data with 16-bit color depth information.

Note 2: The most significant bits are: Rx4, Gx5 and Bx4.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

Note 4: '-'= don't care –Can be set "0" or "1".



One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when IFPF [2:0] bits of 3Ah register are set to "110".

Note 1: The pixel data with 18-bit color depth information.

Note 2: The most significant bits are: Rx5, Gx5 and Bx5.

Note 3: The least significant bits are: Rx0, Gx0 and Bx0.

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Note 4: '-'= don't care –Can be set "0" or "1".

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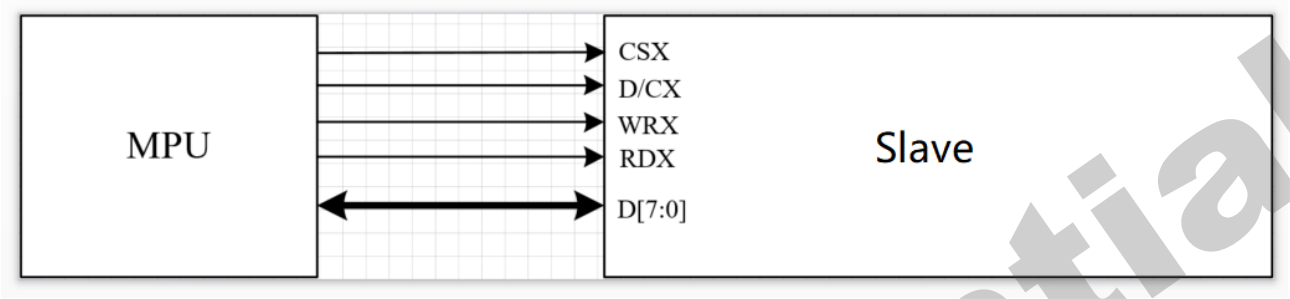
4.2.3. 8-bit Parallel MCU Interface

The 8-bit parallel bus interface of GC9107 can be used by setting external pin as IM [2:0] to“000”.The following shown figure is the example of interface with 8-bits MCU system interface.



Different display data formats are available for three color depths supported by listed below.
- 4K-Color, RGB 4, 4, 4, -bits input data.
- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

4K color: 12-bit/pixel (RGB 4-4-4 bits input)

Two pixel (3 sub-pixels) display data is sent by 3 byte transfers when IFPF [2:0] bits of 3Ah register are set to “011”.

Count	0	1	2	3	4	5	6	…
D/CX	0	1	1	1	1	1	1	…
D7	C7	0R3	0B3	1G3	2R4	2R3	3G3	…
D6	C6	0R2	0B2	1G2	2R3	2R2	3G2	…
D5	C5	0R1	0B1	1G1	2R2	2R1	3G1	…
D4	C4	0R0	0B0	1G0	2R1	2R0	3G0	…
D3	C3	0G3	1R3	1B3	2G3	3R3	3B3	…
D2	C2	0G2	1R2	1B2	2G2	3R2	3B2	…
D1	C1	0G1	1R1	1B1	2G1	3R1	3B1	…
D0	C0	0G0	1R0	1B0	2G0	3R0	3B0	…

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65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when IFPF [2:0] bits of 3Ah register are set to “101”.

Count	0	1	2	3	4	…
D/CX	0	1	1	1	1	…
D7	C7	0R4	0G2	1R4	1G2	…
D6	C6	0R3	0G1	1R3	1G1	…
D5	C5	0R2	0G0	1R2	1G0	…
D4	C4	0R1	0B4	1R1	1B4	…
D3	C3	0R0	0B3	1R0	1B3	…
D2	C2	0G5	0B2	1G5	1B2	…
D1	C1	0G4	0B1	1G4	1B1	…
D0	C0	0G3	0B0	1G3	1B0	…

262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when IFPF [2:0] bits of 3Ah register are set to “110”.

Count	0	1	2	3	4	5	6	…
D/CX	0	1	1	1	1	1	1	…
D7	C7	0R5	0G5	0B5	1R5	1G5	1B5	…
D6	C6	0R4	0G4	0B4	1R4	1G4	1B4	…
D5	C5	0R3	0G3	0B3	1R3	1G3	1B3	…
D4	C4	0R2	0G2	0B2	1R2	1G2	1B2	…
D3	C3	0R1	0G1	0B1	1R1	1G1	1B1	…
D2	C2	0R0	0G0	0B0	1R0	1G0	1B0	…
D1	C1							…
D0	C0							…

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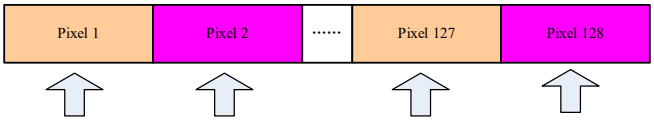
5. Function Description

5.1. Display data GRAM mapping

5.1.1. 128RGBx128 resolution (GM = “01”)



Gate Out	Source Out		S1	S2	S3	S4	S5	S6	……	S379	S380	S381	S382	S383	S384		
			RGB = 0		RGB = 1	RGB = 0		RGB = 1	……	RGB = 0		RGB = 1	RGB = 0		RGB = 1		
	RA								……							SA	
	MY= ‘0’	MY= ‘1’							……							ML= ‘0’	ML= ‘1’
2	0	127	R0	G0	B0	R1	G1	B1	……	R127	G127	B127	R128	G128	B128	0	127
3	1	126							……							1	126
4	2	125							……							2	125
5	3	124							……							3	124
6	4	123							……							4	123
7	5	122							……							5	122
8	6	121							……							6	121
9	7	120							……							7	120
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
122	120	7							……							120	7
123	121	6							……							121	6
124	122	5							……							122	5
125	123	4							……							123	4
126	124	3							……							124	3
127	125	2							……							125	2
128	126	1							……							126	1
129	127	0							……							127	0
	CA	MX= ‘0’	0			1			……	126			127				
		MX= ‘1’	127			126			……	1			0				

Note

RA = Row Address

CA = Col Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

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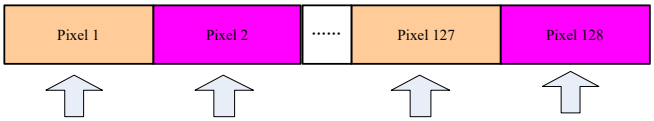
5.1.2. 128RGBx160 resolution (GM = “11”)



Gate Out	Source Out		S1	S2	S3	S4	S5	S6	.....	S379	S380	S381	S382	S383	S384		
	RA		RGB = 0 / RGB = 1			RGB = 0 / RGB = 1			.....	RGB = 0 / RGB = 1			RGB = 0 / RGB = 1			SA	
	MY= ‘0’	MY= ‘1’							.....							ML= ‘0’	ML= ‘1’
2	0	159	R0	G0	B0	R1	G1	B1	.....	R126	G126	B126	R127	G127	B127	0	159
3	1	158							.....							1	158
4	2	157							.....							2	157
5	3	156							.....							3	156
6	4	155							.....							4	155
7	5	154							.....							5	154
8	6	153							.....							6	153
9	7	152							.....							7	152
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
154	152	7							.....							152	7
155	153	6							.....							153	6
156	154	5							.....							154	5
157	155	4							.....							155	4
158	156	3							.....							156	3
159	157	2							.....							157	2
160	158	1							.....							158	1
161	159	0							.....							159	0
	CA	MX= ‘0’	0			1			.....	126			127				
		MX= ‘1’	127			126			.....	1			0				

Note

RA = Row Address

CA = Col Address

SA = Scan Address

MX = Mirror X-axis (Column address direction parameter), D6 parameter of MADCTL command

MY = Mirror Y-axis (Row address direction parameter), D7 parameter of MADCTL command

ML = Scan direction parameter, D4 parameter of MADCTL command

RGB = Red, Green and Blue pixel position change, D3 parameter of MADCTL command

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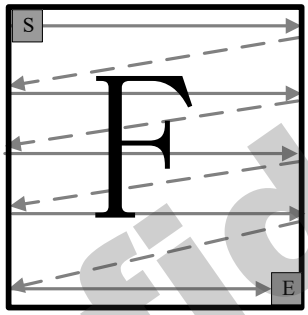
5.2. Address Counter (AC) of GRAM

The GC9107 contains an address counter (AC) which assigns address for writing/reading pixel data to/from GRAM. The address pointers set the position of GRAM. Every time when a pixel data is written into the GRAM, the X address or Y address of AC will be automatically increased by 1 (or decreased by 1), which is decided by the register (**MV, MX** and **MY** bits) setting.

To simplify the address control of GRAM access, the window address function allows for writing data only to a window area of GRAM specified by registers. After data being written to the GRAM, the AC will be increased or decreased within setting window address-range which is specified by the (start: **SC**, end: **EC**) and the (start: **SP**, end: **EP**). Therefore, the data can be written consecutively without thinking a data wrap by those bit function.

Image data sending order from host and data stream update as shown in the following figure



The data is written in the order illustrated above. The counter which dictates where in the physical memory the data is to be written is controlled by **MV, MX** and **MY** bits setting

Image data writing control:

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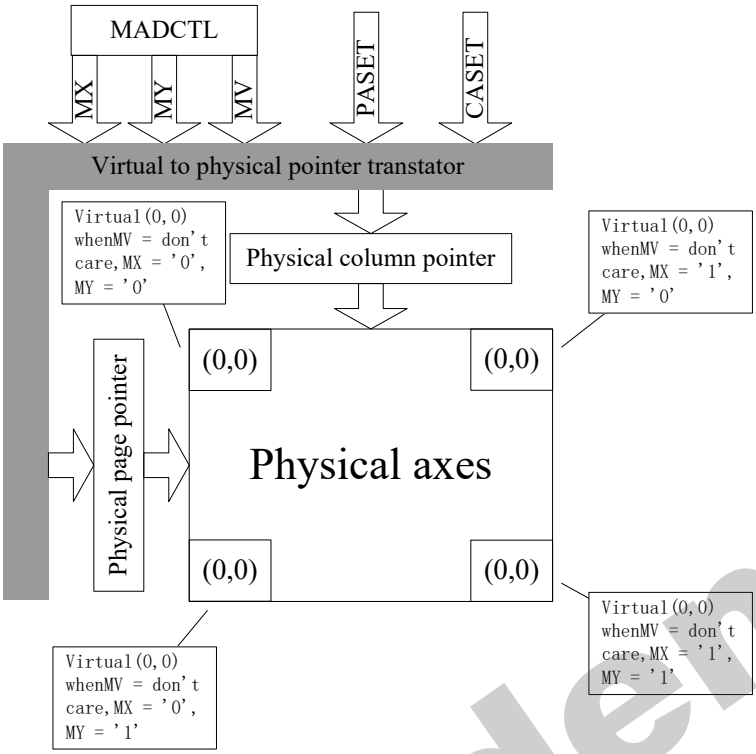

For each image orientation, the controls for the column and page counters apply as below:

condition	Column Counter	Page Counter
When RAMWR/RAMRD command is accepted	Return to "Start Column"	Return to "Start Page"
Complete Pixel Pair Write/Read action	Increment by 1	No change
The Column counter value is larger than "End column."	Return to "Start Column"	Increment by 1
The Page counter value is larger than "End page".	Return to "Start column"	Return to "Start Page"

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5.2.1. 128RGBx160 (GM == '11')

CASET and PASET control for physical column/page pointers:

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (161 - Physical Page Pointer)
0	1	0	Direct to (127 - Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (127 - Physical Column Pointer)	Direct to (161 - Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (161 - Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (127 - Physical Column Pointer)
1	1	1	Direct to (161 - Physical Page Pointer)	Direct to (127 - Physical Column Pointer)

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5.2.2. 128RGBx128 (GM == '01')

MV	MX	MY	CASET	PASET
0	0	0	Direct to Physical Column Pointer	Direct to Physical Page Pointer
0	0	1	Direct to Physical Column Pointer	Direct to (127 - Physical Page Pointer)
0	1	0	Direct to (127 - Physical Column Pointer)	Direct to Physical Page Pointer
0	1	1	Direct to (127 - Physical Column Pointer)	Direct to (127 - Physical Page Pointer)
1	0	0	Direct to Physical Page Pointer	Direct to Physical Column Pointer
1	0	1	Direct to (127 - Physical Page Pointer)	Direct to Physical Column Pointer
1	1	0	Direct to Physical Page Pointer	Direct to (127 - Physical Column Pointer)
1	1	1	Direct to (127 - Physical Page Pointer)	Direct to (127 - Physical Column Pointer)

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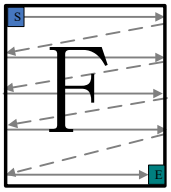
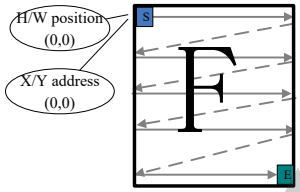
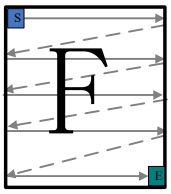
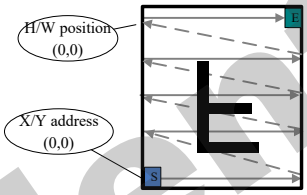
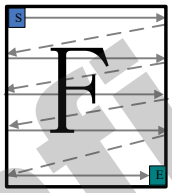
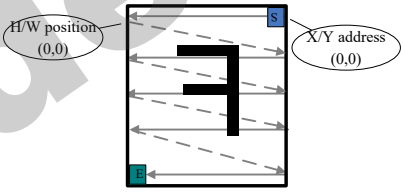
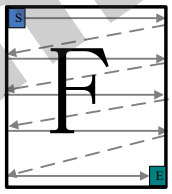
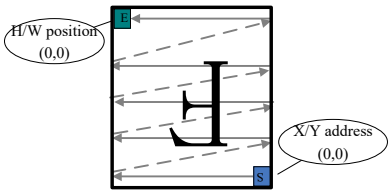
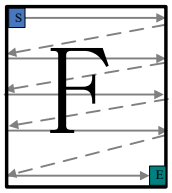
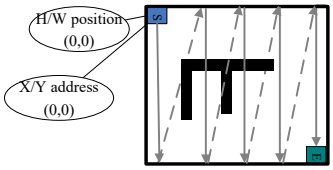
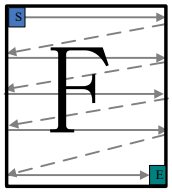
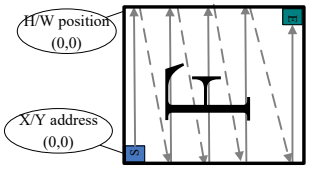
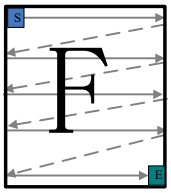
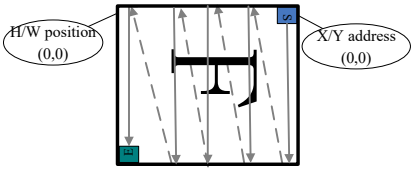
5.2.3. Frame Data Write Direction

The following figure depicts the GRAM address update method with MV, MX and MY bit setting.

Display data direction	MV	MX	MY	Image in the Host	Image in the Driver (GRAM)
normal	0	0	0		
Y-invert	0	0	1		
X-ivert	0	1	0		
Y-invert X-invert	0	1	1		
X-Y exchange	1	0	0		
X-Y exchange Y-invert	1	0	1		
X-Y exchange X-invert	1	1	0		

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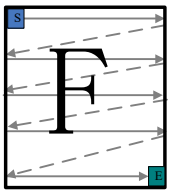
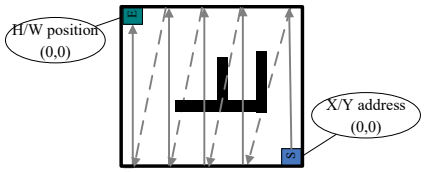
X-Y exchange Y-invert X-invert	1	1	1		

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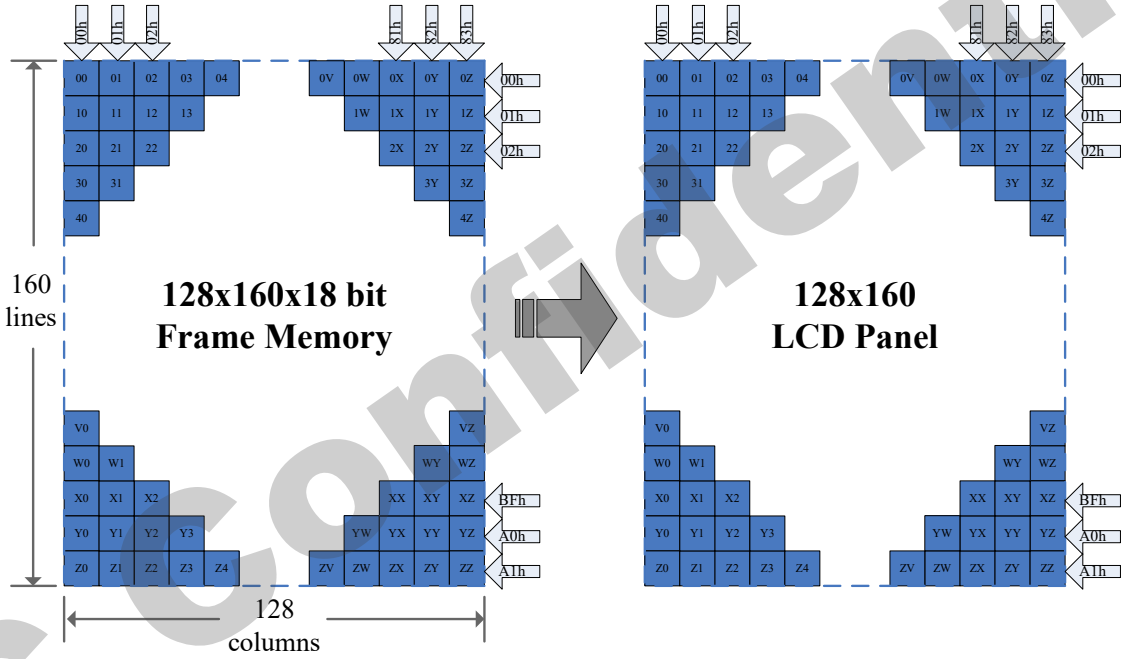
5.3. GRAM to display address mapping

GC9107 supports three kinds of display mode: one is Normal Display Mode, one is the other is Partial Display Mode, and Scrolling Display Mode.

5.3.1. Normal display on or partial mode on, vertical scroll off

In this mode, content of the frame memory within an area where column pointer is 0000h to 007fh and page pointer is 0000h to 009fh is displayed.
To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0,0)



Example1:
(1) Partial mode on (setting 12h)
(2) SR [15:0] =’20d’, ER [15:0] =’50d’, MADCTL’s **B4(ML)= ‘0’**.

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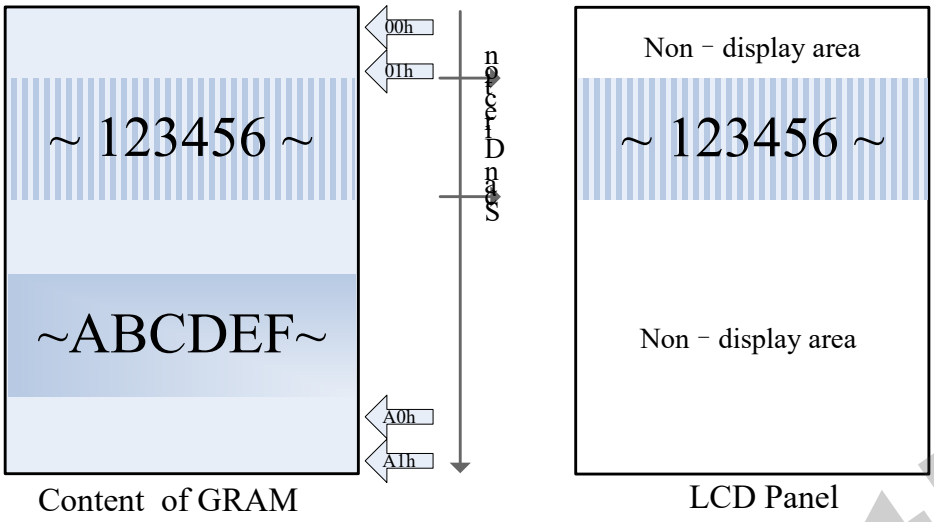
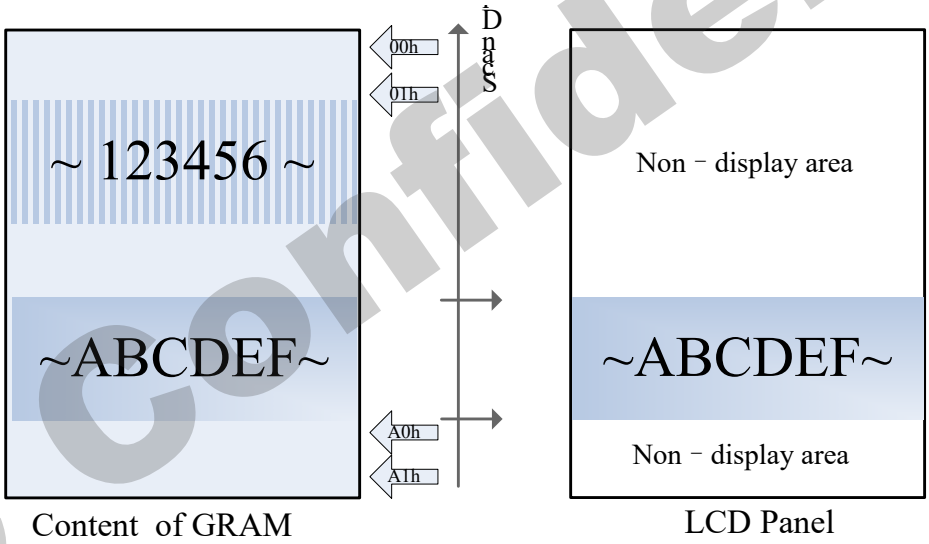


Example2:

(1) Partial mode on (setting 12h)

(2) SR [15:0] =’20d’, ER [15:0] =’50d’, MADCTL’s **B4(ML)= ‘1’**.



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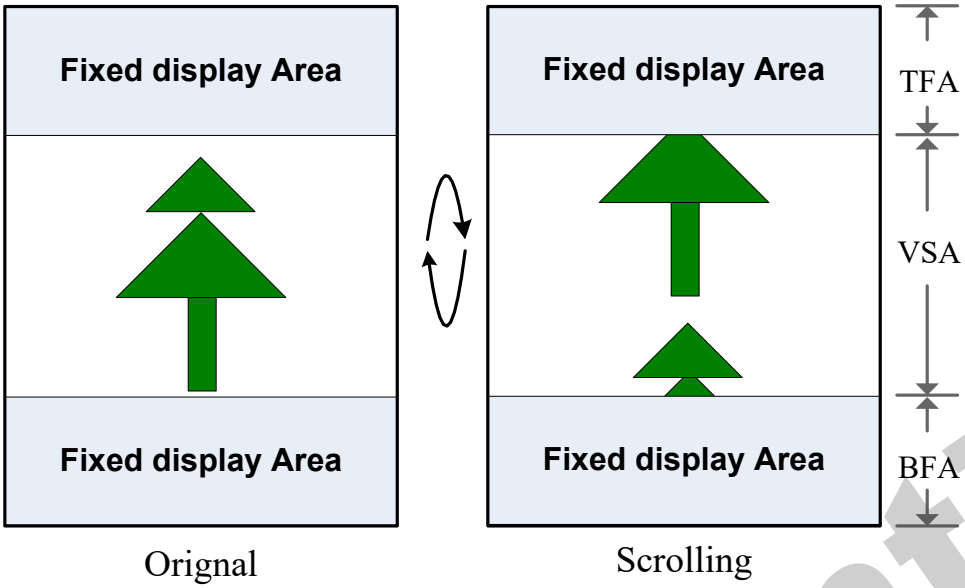
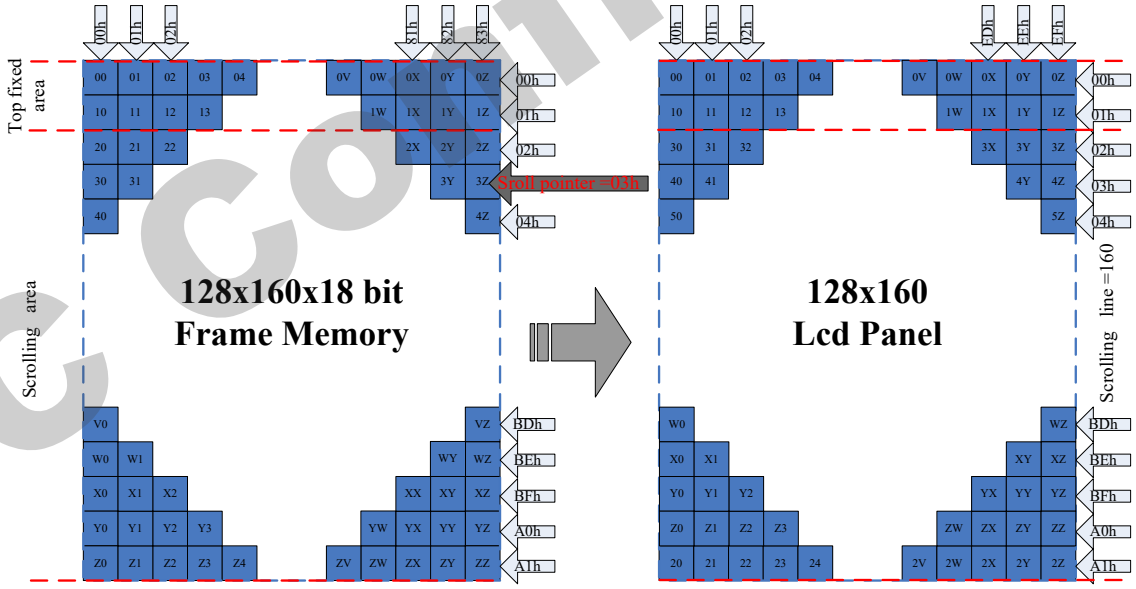
5.3.2. Vertical scroll display mode

When setting R37h, the scrolling display mode is active, and the vertical scrolling display is specified by **TFA, VSA ,BFA** bits (R33h) and **SSA** bits (R37h).



When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) =160. In this case, scrolling is applied as shown below.

Example 1 .TFA=’2d’, VSA=’160d’, BFA=’0d’, SSA=’3d’ (SS=’0’, GS=’0’)
Memory map of vertical scrolling 1:



Example 2 .TFA=’2d’, VSA=’158d’, BFA=’2d’, SSA=’3d’ (SS=’0’, GS=’0’)
Memory map of vertical scrolling 2:

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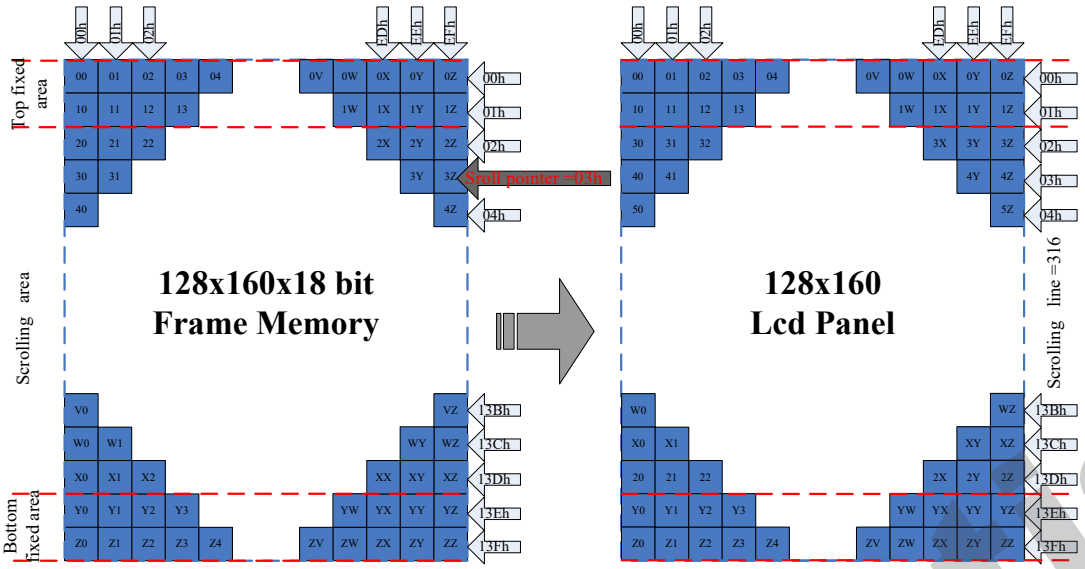
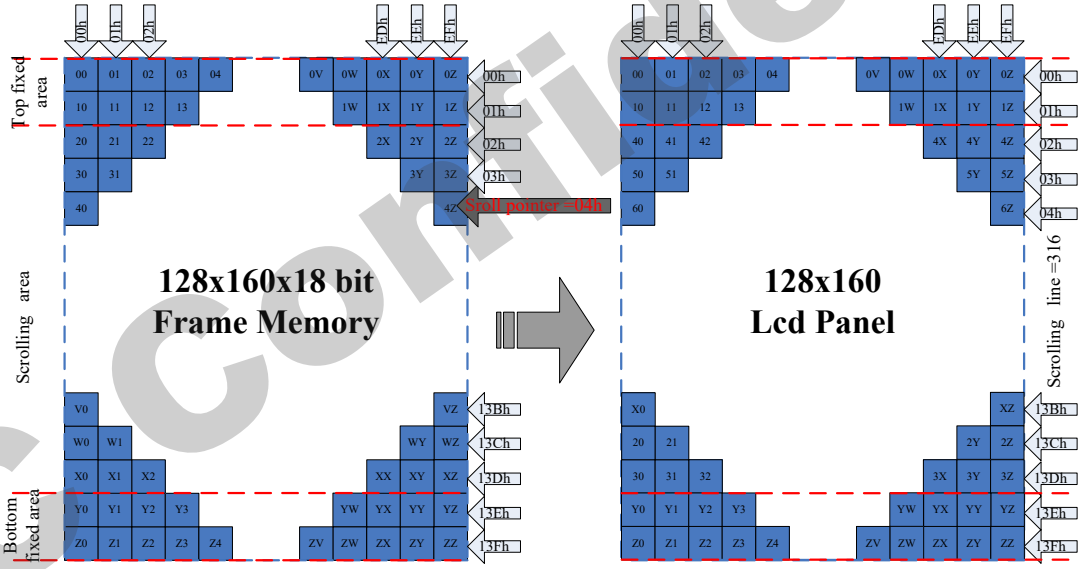


Example 3 .TFA='2d', VSA='158d', BFA='2d', SSA='4d' (SS='0', GS='0')

Memory map of vertical scrolling 3:



Vertical scroll example

There are 2 types of vertical scrolling, which are determined by the **TFA, VSA, BFA** bits and **SSA** bits

Case 1: TFA + VSA + BFA ≠ '160d'

N/A: Do not set TFA + VSA + BFA ≠ '160d'. In that case, unexpected picture will be shown.

Case 2: TFA + VSA + BFA = '160d' (Scrolling)

Example (1) When TFA='0d', VSA='160d', BFA='0d' and SSA1='40d' & SSA2='100d' (SS ='0', GS='0')

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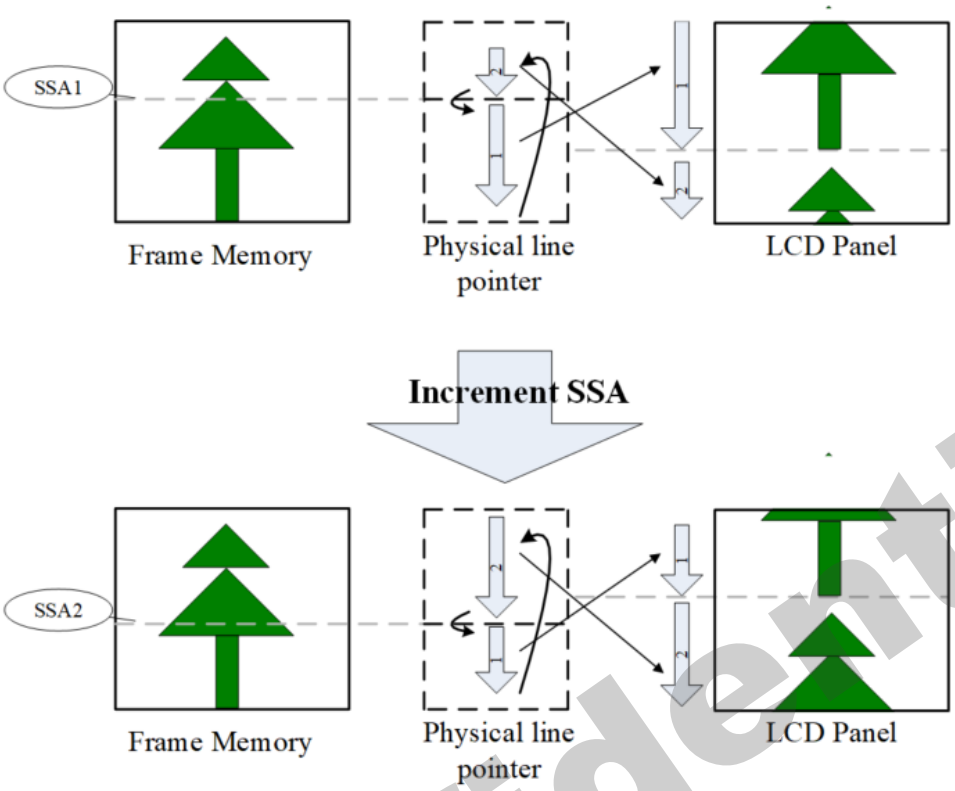

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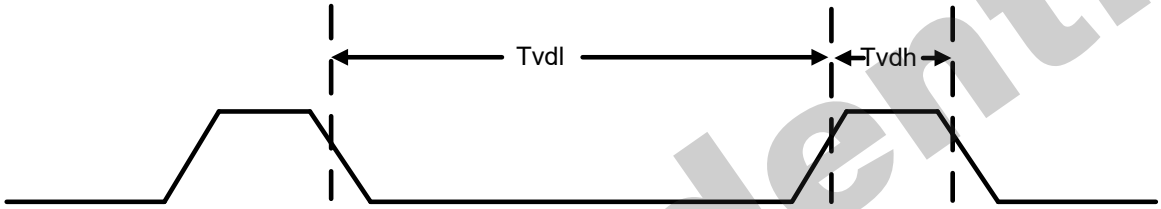
5.4. Tearing effect output line

The Tearing Effect output line supplies to the MPU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize Frame Memory writing when displaying video images.

5.4.1. Tearing effect line modes

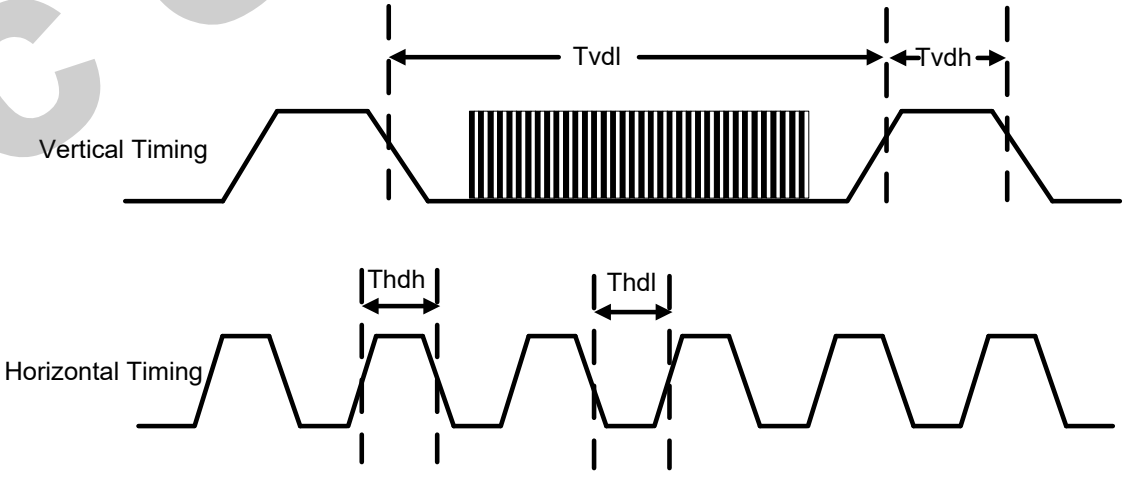
Mode 1, The Tearing Effect Output signal consists of V-Blanking Information only:



T_{line} is the display time of every line
TVdh=(181-128)*T_{line} when GM[1:0]=01，**TVdh=**(181-160)*T_{line} when GM[1:0]=11.
TVdl=128*T_{line} when GM[1:0]=01，**TVdl=**160*T_{line} when GM[1:0]=11.

5.4.2. Tearing effect line timing

The Tearing Effect signal is described below.



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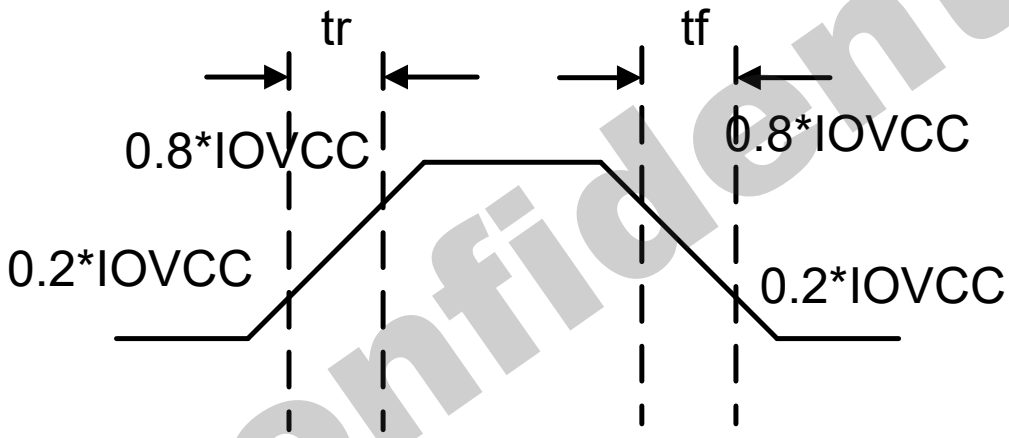
Idle Mode Off (Frame Rate = 60 Hz)

Symbol	Parameter	Spec.			Description
		Min.	Max.	Unit	
tvdl	Vertical Timing Low Duration	TBD	-	ms	-
tvdh	Vertical Timing High Duration	1000	-	us	-
thdl	Horizontal Timing Low Duration	TBD	-	us	-
thdh	Horizontal Timing High Duration	TBD	500	us	-

Note: Idle Mode Off (Frame Rate = 60 Hz) ,The signal's rise and fall times (tf, tr) are stipulated to be equal to or less than 15ns.



The Tearing Effect Output Line is fed back to the MCU and should be used to avoid Tearing Effect.

5.5. Source driver

The GC9107 contains a 384 channels of source driver (S1~S384) which is used for driving the source line of TFT LCD panel. The source driver converts the digital data from GRAM into the analog voltage for 384 channels and generates corresponding gray scale voltage output, which can realize a 262K colors display simultaneously.

Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

5.6. Gate driver

The GC9107 contains a 160 gate channels of gate driver (G2~G161) which is used for driving the gate. The gate driver level is VGH when scan some line, VGL the other lines.

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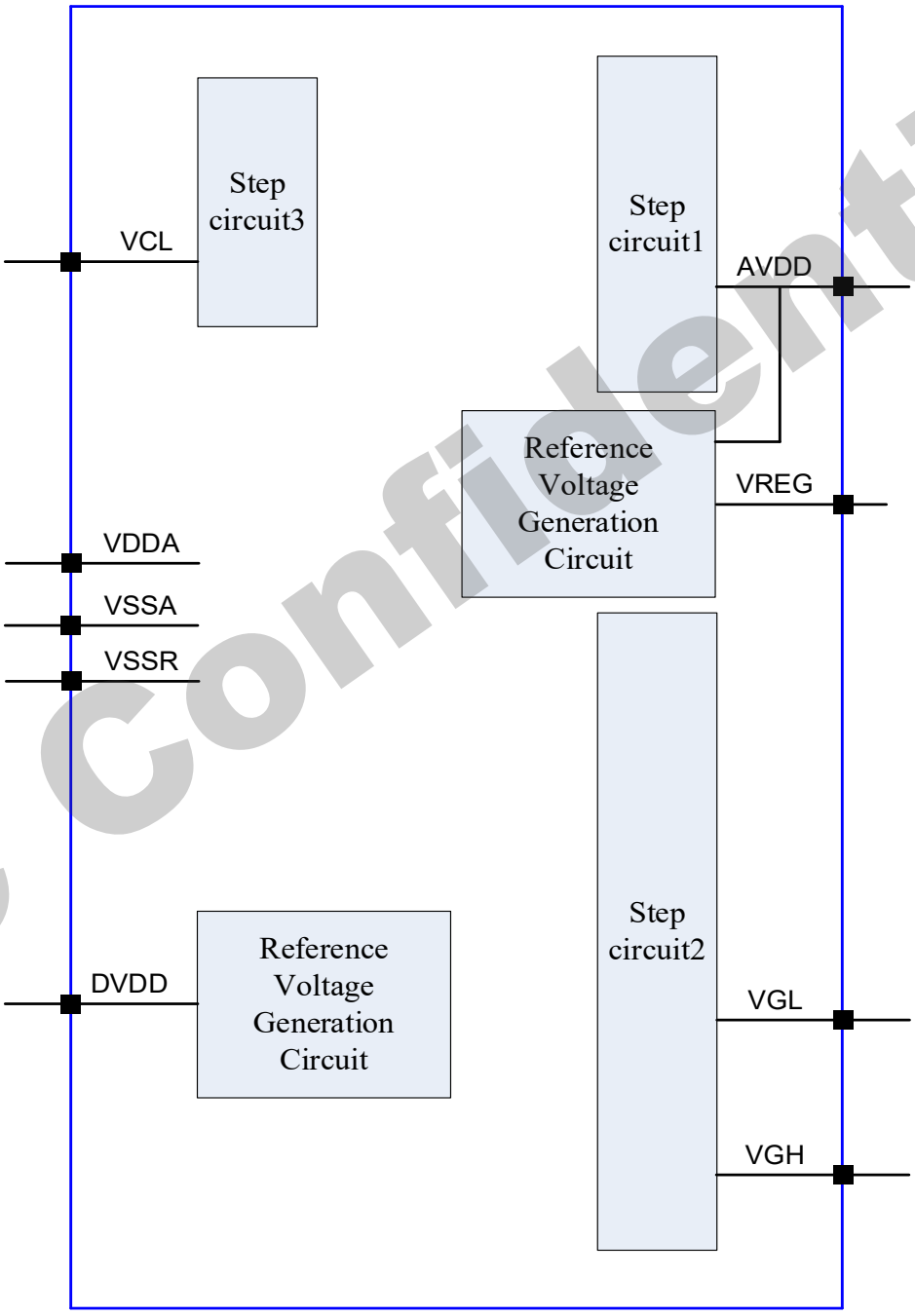
5.7. LCD power generation circuit

5.7.1. Power supply circuit

The power circuit of GC9107 is used to generate supply voltages for LCD panel driving.



Block diagram of GC9107 power circuit

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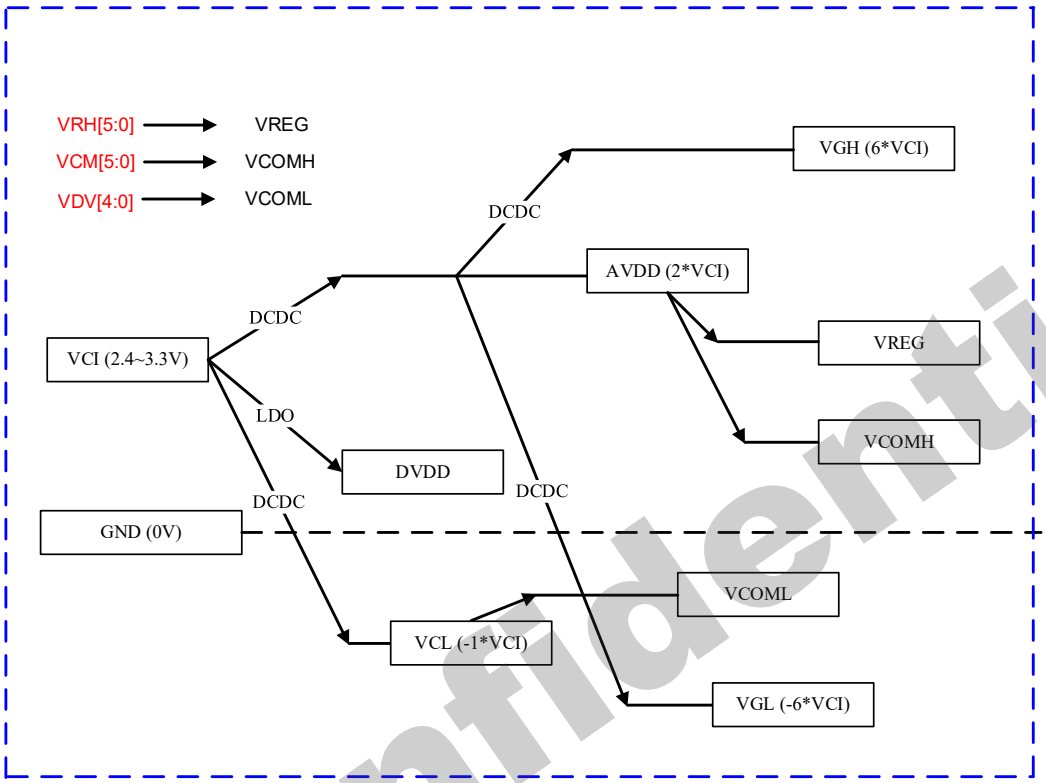
5.7.2. LCD power generation scheme

The boost voltage generated is shown as below.



LCD power generation scheme

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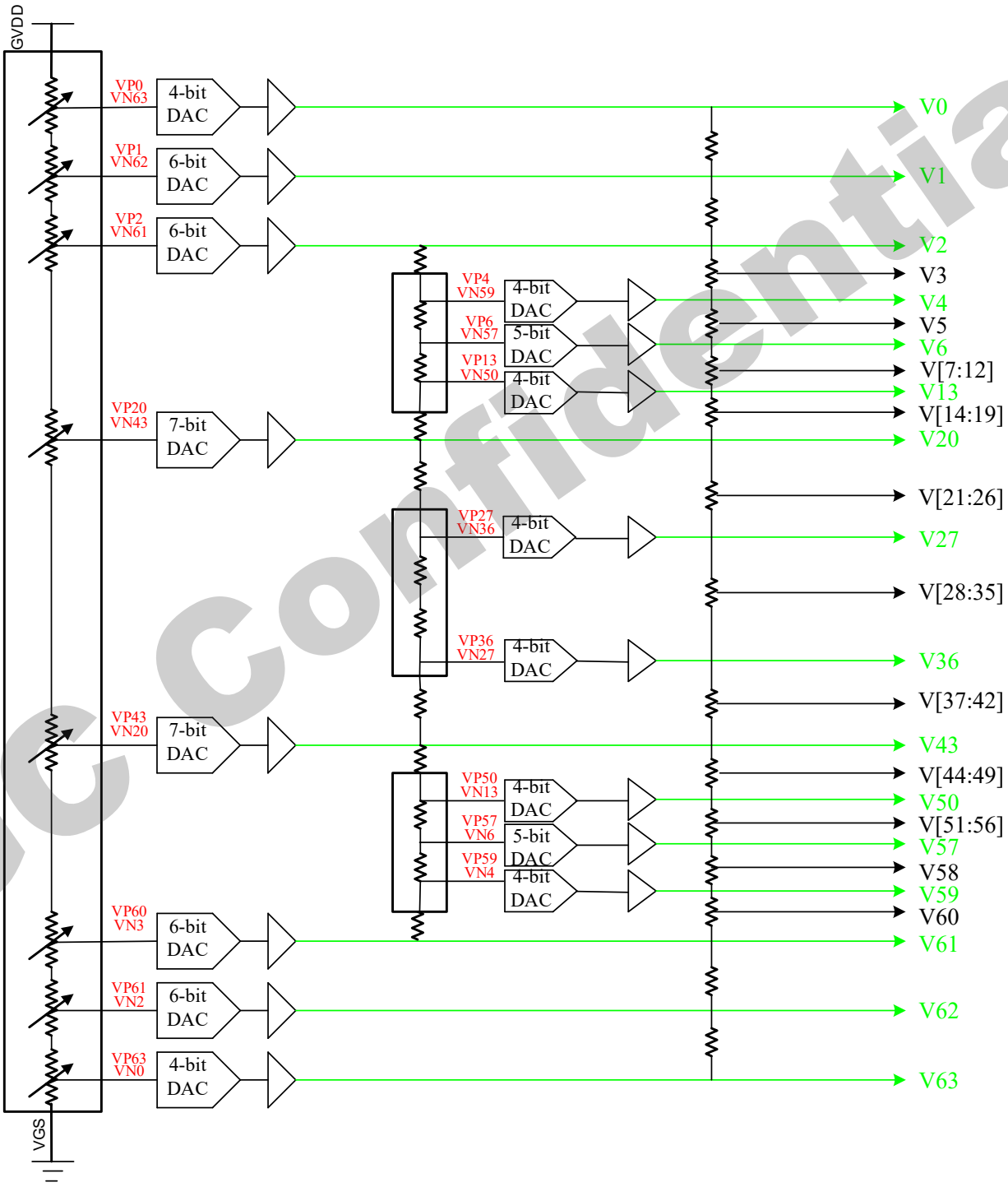
5.8. Gamma Correction

GC9107 incorporates the γ-correction function to display 262,144 colors for the LCD panel. The γ-correction is performed with 32 registers determining 16 reference grayscale levels, whitch make GC9107 available with liquid crystal panels of various characteristics.



Grayscale Voltage Generation

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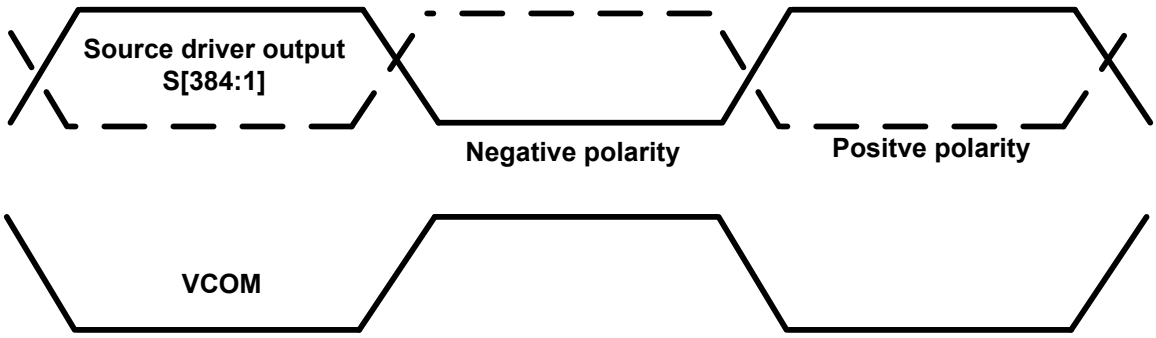
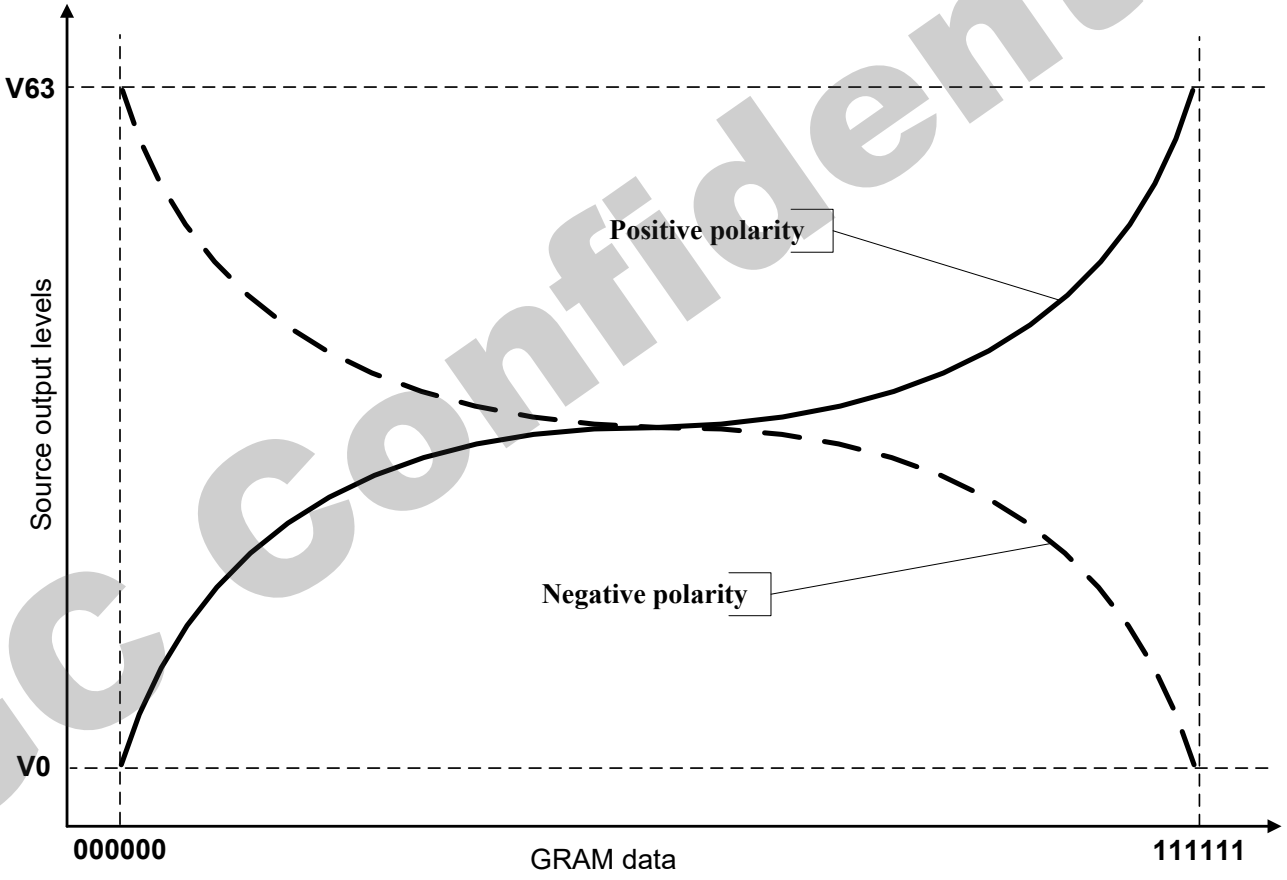


Relationship between Source Output and VCOM



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5.9. Power Level Definition

5.9.1. Power Levels

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
   In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out.
   In this mode part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
   In this mode, the full display area is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out.
   In this mode, part of the display is used but with 8 colors.
5. Sleep In Mode.
   In this mode, the DC : DC converter, Internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.
6. Power Off Mode.
   In this mode, both VDD and VDDI are removed.

Note1: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

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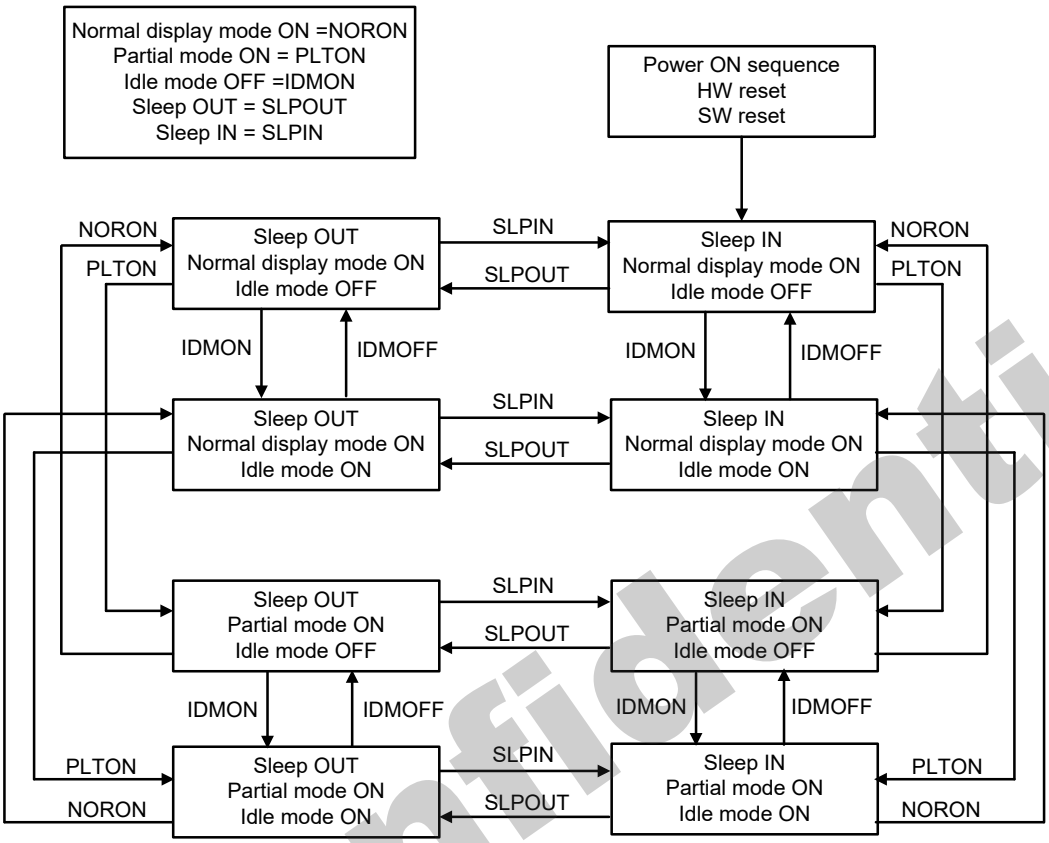
5.9.2. Power Flow Chart



Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by User, when there is changing from one power mode to another power mode.

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6. Command

6.1. Command List

6.1.1. USER REG

Regulative Command Set												
Command Function	**D/CX**	**RDX**	**WRX**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Read Manufactory Programming Identification	0	1	↑	0	0	0	0	0	1	0	0	04
	1	↑	1	X	X	X	X	X	X	X	X	XX
	1	↑	1	Man_ID1_1[7:0]								00
	1	↑	1	Man_ID1_2[7:0]								91
	1	↑	1	Man_ID1_3[7:0]								07
Read Display Status	0	1	↑	0	0	0	0	1	0	0	1	09
	1	↑	1	X	X	X	X	X	X	X	X	XX
	1	↑	1	BSTON	MY	MX	MV	ML	BGR	0	0	00
	1	↑	1	0	IFPF[2:0]			IDMON	PTLON	SLPOUT	NORON	61
	1	↑	1	0	0	INVON	0	0	DISON	TEON	0	00
	1	↑	1	0	0	TEM	0	0	0	0	0	00
Read Display Power Mode	0	1	↑	0	0	0	0	1	0	1	0	0A
	1	↑	1	X	X	X	X	X	X	X	X	XX
	1	↑	1	BSTON	IDMON	PTLON	SLPON	NORON	DISPON	0	0	08
Read Display MADCTL	0	1	↑	0	0	0	0	1	0	1	1	0B
	1	↑	1	X	X	X	X	X	X	X	X	XX
	1	↑	1	MY	MX	MV	ML	BRG	0	0	0	00
Read Display Pixel Format	0	1	↑	0	0	0	0	1	1	0	0	0C
	1	↑	1	X	X	X	X	X	X	X	X	XX
	1	↑	1	0	0	0	0	0	IFPF [2:0]			06
Read Display Image Form	0	1	↑	0	0	0	0	1	1	0	1	0D
	1	↑	1	X	X	X	X	X	X	X	X	XX

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	1	↑	1	VSS ON	0	INV ON	0	0	0	0	0	00
Read Display Signal Mode	0	1	↑	0	0	0	0	1	1	1	0	0E
	1	↑	1	X	X	X	X	X	X	X	X	XX
	1	↑	1	TE ON	TE M	0	0	0	0	0	0	00
Read Display Self-Diagnostic Result	0	1	↑	0	0	0	0	1	1	1	1	0F
	1	↑	1	X	X	X	X	X	X	X	X	XX
	1	↑	1	1	1	1	1	0	0	0	0	F0
Sleep In	0	1	↑	0	0	0	1	0	0	0	0	10
Sleep OUT	0	1	↑	0	0	0	1	0	0	0	1	11
Partial Mode ON	0	1	↑	0	0	0	1	0	0	1	0	12
Normal Display Mode ON	0	1	↑	0	0	0	1	0	0	1	1	13
Display Inversion OFF	0	1	↑	0	0	1	0	0	0	0	0	20
Display Inversion ON	0	1	↑	0	0	1	0	0	0	0	1	21
Display OFF	0	1	↑	0	0	1	0	1	0	0	0	28
Display ON	0	1	↑	0	0	1	0	1	0	0	1	29
Column Address Set	0	1	↑	0	0	1	0	1	0	1	0	2A
	1	1	↑	SC[15:8]								-
	1	1	↑	SC[7:0]								-
	1	1	↑	EC[15:8]								-
	1	1	↑	EC[7:0]								-
Page Address Set	0	1	↑	0	0	1	0	1	0	1	1	2B
	1	1	↑	SP[15:8]								-
	1	1	↑	SP[7:0]								-
	1	1	↑	EP[15:8]								-
	1	1	↑	EP[7:0]								-
Memory Write	0	1	↑	0	0	1	0	1	1	0	0	2C
	1	1	↑	D[17:0]								XX
Partial Area	0	1	↑	0	0	1	1	0	0	0	0	30
	1	1	↑	SR[15:8]								00
	1	1	↑	SR[7:0]								00
	1	1	↑	ER[15:8]								00
	1	1	↑	ER[7:0]								A1
Vertical Scrolling Definition	0	1	↑	0	0	1	1	0	0	1	1	33
	1	1	↑	TFA[15:8]								00
	1	1	↑	TFA[7:0]								00
	1	1	↑	VSA[15:8]								00
	1	1	↑	VSA[7:0]								A2

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	1	1	↑	BFA[15:8]								00
	1	1	↑	BFA[7:0]								00
Tearing Effect Line OFF	0	1	↑	0	0	1	1	0	1	0	0	34
Tearing Effect Line ON	0	1	↑	0	0	1	1	0	1	0	1	35
	1	1	↑	0	0	0	0	0	0	0	M	00
Memory Access Control	0	1	↑	0	0	1	1	0	1	1	0	36
	1	1	↑	MY	MX	MV	ML	BGR	0	0	0	00
Vertical Scrolling Start Address	0	1	↑	0	0	1	1	0	1	1	1	37
	1	1	↑	00								00
	1	1	↑	SSA[7:0]								00
Idle Mode OFF	0	1	↑	0	0	1	1	1	0	0	0	38
Idle Mode ON	0	1	↑	0	0	1	1	1	0	0	1	39
Pixel Format Set	0	1	↑	0	0	1	1	1	0	1	0	3A
	1	1	↑	0	0	0	0	0	IFPF[2:0]			06
TEST Scanline Set	0	1	↑	0	1	0	0	0	1	0	0	44
	1	1	↑	SCNL[7:0]								00
TEST Scanline Get	0	1	↑	0	1	0	0	0	1	0	1	45
	1	↑	1	SCNL[7:0]								00
Customized display identification information	0	1	↑	1	1	0	1	0	0	1	1	D3
	1	↑	1	X	X	X	X	X	X	X	X	XX
	1	↑	1	Customized_ID1_1[7:0]								XX
	1	↑	1	Customized_ID1_2[7:0]								XX
	1	↑	1	Customized_ID1_3[7:0]								XX
Read ID1	0	1	↑	1	1	0	1	1	0	1	0	DA
	1	↑	1	X	X	X	X	X	X	X	X	XX
	1	↑	1	Man_ID1_1[7:0]								00
Read ID2	0	1	↑	1	1	0	1	1	0	1	1	DB
	1	↑	1	X	X	X	X	X	X	X	X	XX
	1	↑	1	Man_ID1_2[7:0]								91
Read ID3	0	1	↑	1	1	0	1	1	1	0	0	DC
	1	↑	1	X	X	X	X	X	X	X	X	XX
	1	↑	1	Man_ID1_3[7:0]								07

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6.1.2. INTER REG

Internal Command Set												
Command Function	**D/CX**	**RDX**	**WRX**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Inter register enable 1	0	1	↑	1	1	1	1	1	1	1	0	FE
Inter register enable 2	0	1	↑	1	1	1	0	1	1	1	1	EF
Complement Principle of RGB 5, 6, 5	0	1	↑	1	0	1	0	1	1	0	0	AC
	1	1	↑	epf[1:0]		0	0	0	0	0	0	C0
Blanking Porch Control	0	1	↑	1	0	1	0	1	1	0	1	AD
	1	1	↑	0	fp[6:0]							12
	1	1	↑	0	bp[6:0]							0A
Display Inversion Control	0	1	↑	1	0	1	1	0	1	0	0	B4
	1	1	↑	0	0	0	0	0	inv_ctl[2:0]			02
AVDD_VCL_CLK	0	1	↑	1	1	1	0	0	0	1	1	E3
	1	1	↑	0	AVDD_CLK_AD<2:0>			0	VCL_CLK_AD<2:0>			22
VGH_VGL_CLK	0	1	↑	1	1	1	0	1	0	1	0	EA
	1	1	↑	VGH_CLK_DIV [3:0]				VGL_CLK_DIV [3:0]				94
FRS	0	1	↑	1	0	1	0	1	0	0	0	A8
	1	1	↑	0	RTN[6:0]							16
VREG CTL	0	1	↑	1	1	1	0	0	1	1	1	E7
	1	1	↑	0	VREG_AD[6:0]							50
VGH_SET	0	1	↑	1	1	1	0	1	0	0	0	E8
	1	1	↑	0	0	1	0	0	D2A_VGHS [2:0]			23
VGL_SET	0	1	↑	1	1	1	0	1	0	0	1	E9
	1	1	↑	0	0	1	0	0	D2A_VGLS [2:0]			43
AVDD_VCL_SET	0	1	↑	1	1	1	0	0	0	1	0	E2
	1	1	↑	0	1	1	0	1	1	0	1	6D
	1	1	↑	0	1	1	0	1	1	1	0	6E
	1	1	↑	0	AVDD_AD [2:0]			0	VCL_AD [2:0]			45

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Command Function	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SET_GAMMA0	0	1	↑	1	1	1	1	0	0	0	0	F0
	1	1	↑	0	0	vr2_n[5:0]						03
	1	1	↑	0	vr20_n[6:0]							2E
	1	1	↑	0	0	vr36_n[2:0]		vr27_n[2:0]				2C
	1	1	↑	0	vr43_n[6:0]							3F
	1	1	↑	vr50_n[3:0]				vr13_n[3:0]				C8
	1	1	↑	0	0	vr61_n[5:0]						14
	1	1	↑	0	0	vr62_n[5:0]						18
	1	1	↑	j0_n[1:0]		j1_n[1:0]		vr0_n[3:0]				60
	1	1	↑	0	0	vr1_n[5:0]						00
	1	1	↑	0	0	0	vr4_n[4:0]					08
	1	1	↑	0	0	0	vr6_n[4:0]					0D
	1	1	↑	0	0	0	vr57_n[4:0]					18
	1	1	↑	0	0	0	vr59_n[4:0]					14
	1	1	↑	0	0	0	vr63_p[4:0]					1F
SET_GAMMA1	0	1	↑	1	1	1	1	0	0	0	1	F1
	1	1	↑	0	0	vr2_p[5:0]						03
	1	1	↑	0	vr20_p[6:0]							2B
	1	1	↑	0	0	vr36_p[2:0]		vr27_p[2:0]				24
	1	1	↑	0	vr43_p[6:0]							41
	1	1	↑	vr50_[3:0]				vr13_p[3:0]				C5
	1	1	↑	0	0	vr61_p[5:0]						13
	1	1	↑	0	0	vr62_p[5:0]						17
	1	1	↑	j0_p[1:0]		j1_p[1:0]		vr0_p[3:0]				A0
	1	1	↑	0	0	vr1_p[5:0]						01
	1	1	↑	0	0	0	vr4_p[4:0]					0B
	1	1	↑	0	0	0	vr6_p[4:0]					0C
	1	1	↑	0	0	0	vr57_p[4:0]					19
	1	1	↑	0	0	0	vr59_p[4:0]					16
	1	1	↑	0	0	0	vr63_p[4:0]					1F

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6.2. Description of User Command

6.2.1. Read Manufactory Programming Identification (04h)

<table>
<tr><td>04h</td><td colspan="12">Read Manufactory Programming Identification</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>04</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td colspan="8">Man_ID1_1 [7:0]</td><td>00</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>↑</td><td>1</td><td colspan="8">Man_ID1_2 [7:0]</td><td>91</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>↑</td><td>1</td><td colspan="8">Man_ID1_3[7:0]</td><td>07</td></tr>
<tr><td>Description</td><td colspan="12">This read byte returns 24 bits display identification information.
The 1st parameter is dummy data.
The 2nd parameter (Man_ID1_1 [7:0]): LCD module’s manufacturer ID.
The 3rd parameter (Man_ID1_2 [7:0]): LCD module’s manufacturer ID.
The 4th parameter (Man_ID1_3 [7:0]): LCD module’s manufacturer ID.</td></tr>
<tr><td>Restriction</td><td colspan="12">The value of 04h is changed by OTP writing if OTP enable. When the OTP disable, the value of 04h is 0x009107. When the OTP enable, the value of 04h is the same as the OTP writing.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>24’h009107</td></tr><tr><td>HW Reset</td><td>24’h009107</td></tr></table></td></tr>
</table>

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6.2.2. Read Display Status (09h)

09h	Read Display Status											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	1	0	0	1	09
1st Parameter	1	↑	1	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	BSTON	MY	MX	MV	ML	BGR	0	0	00
3rd Parameter	1	↑	1	0	IFPF[2:0]			IDMON	PTLON	SLPOUT	NORON	61
4th Parameter	1	↑	1	0	0	INVON	0	0	DISON	TEON	0	00
5th Parameter	1	↑	1	0	0	TEM	0	0	0	0	0	00

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value	Status
BSTON	Booster voltage status	0	Booster OFF
		1	Booster ON
MY	Row address□order	0	Top to Bottom (When MADCTL B7='0')
		1	Bottom to Top (When MADCTL B7='1')
MX	Column address order	0	Left to Right (When MADCTL B6='0').
		1	Right to Left (When MADCTL B6='1').
MV	Row/column exchange	0	Normal Mode (When MADCTL B5='0').
		1	Reverse Mode (When MADCTL B5='1').
ML	Vertical refresh	0	LCD Refresh Top to bottom (When MADCTL B4='0')
		1	LCD Refresh bottom to Top (When MADCTL B4='1').
BGR	RGB/BGR order	0	RGB (When MADCTL B3='0')
		1	BGR (When MADCTL B3='1')
IFPF	Interface color pixel format definition	011	12-bit/pixel
		101	16-bit/pixel
		110	18-bit/pixel
IDMON	Idle mode ON/OFF	0	Idle Mode OFF
		1	Idle Mode ON

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Description

Bit	Description	Value	Status
PTLON	Partial mode ON/OFF	0	Partial Mode OFF
		1	Partial Mode ON
SLPOUT	Sleep IN/OUT	0	Sleep IN Mode
		1	Sleep OUT Mode
NORON	Display normal mode ON/OFF	0	Display Normal Mode OFF.
		1	Display Normal Mode ON.
INVON	Inversion status	0	Inversion off
		1	Inversion on
DISON	Display ON/OFF	0	Display is OFF
		1	Display is ON
TEON	Tearing effect line ON/OFF	0	Tearing Effect Line OFF
		1	Tearing Effect ON
TEM	Tearing effect line mode	0	Mode 1, V-Blanking only
		1	Mode 2, both H-Blanking and V-Blanking

- = Don't care.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	32'h00610000
HW Reset	32'h00610000

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6.2.3. Read Display Power Mode (0Ah)

<table>
<tr><td>0Ah</td><td colspan="12">Read Display Power Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0A</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>BSTON</td><td>IDMON</td><td>PTLON</td><td>SLPON</td><td>NORON</td><td>DISON</td><td>0</td><td>0</td><td>08</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td rowspan="2">BSTON</td><td>Booster Off or has a fault.</td><td>0</td></tr>
<tr><td>Booster On and working OK.</td><td>1</td></tr>
<tr><td rowspan="2">IDMON</td><td>Idle Mode Off.</td><td>0</td></tr>
<tr><td>Idle Mode On.</td><td>1</td></tr>
<tr><td rowspan="2">PTLON</td><td>Partial Mode Off.</td><td>0</td></tr>
<tr><td>Partial Mode On.</td><td>1</td></tr>
<tr><td rowspan="2">SLPON</td><td>Sleep In Mode</td><td>0</td></tr>
<tr><td>Sleep Out Mode</td><td>1</td></tr>
<tr><td rowspan="2">NORON</td><td>Display Normal Mode Off.</td><td>0</td></tr>
<tr><td>Display Normal Mode On</td><td>1</td></tr>
<tr><td rowspan="2">DISON</td><td>Display is Off.</td><td>0</td></tr>
<tr><td>Display is On</td><td>1</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12"></td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h08</td></tr>
<tr><td>HW Reset</td><td>8’h08</td></tr>
</table></td></tr>
</table>

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6.2.4. Read Display MADCTL (0Bh)

<table>
<tr><td>0Bh</td><td colspan="12">Read Display MADCTL</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0B</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>MY</td><td>MX</td><td>MV</td><td>ML</td><td>BGR</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td rowspan="2">MY</td><td>Top to Bottom(When M□DCTL B7=’0’).</td><td>0</td></tr>
<tr><td>Bottom to Top(When MADCTL B7=’1’).</td><td>1</td></tr>
<tr><td rowspan="2">MX</td><td>Left to Right (When MADCTL B6=’0’)</td><td>0</td></tr>
<tr><td>Right to Left (When MADCTL B6=’1’)</td><td>1</td></tr>
<tr><td rowspan="2">MV</td><td>Normal Mode (When MADCTL B5=’0’)</td><td>0</td></tr>
<tr><td>Reverse Mode (When MADCTL B5=’1’)</td><td>1</td></tr>
<tr><td rowspan="2">ML</td><td>LCD Refresh Top to Bottom
(When MADCTL B4=’0’)</td><td>0</td></tr>
<tr><td>LCD Refresh Bottom to Top
(When MADCTL B4=’1’).</td><td>1</td></tr>
<tr><td rowspan="2">BGR</td><td>RGB (When MADCTL B3=’0’)</td><td>0</td></tr>
<tr><td>BGR (When MADCTL B3=’1’).</td><td>1</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12"></td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00h</td></tr>
<tr><td>HW Reset</td><td>8’h00h</td></tr>
</table></td></tr>
</table>

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6.2.5. Read Display Pixel Format (0Ch)

<table>
<tr><td>0Ch</td><td colspan="12">Read Display Pixel Format</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0C</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="3">IFPF[2:0]</td><td>06</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>IFPF [2:0]</th><th>MCU（SPI） Interface Format</th></tr>
<tr><td>0□0</td><td>12 bits / pixel</td></tr>
<tr><td>101</td><td>16 bits / pixel</td></tr>
<tr><td>110</td><td>18 bits / pixel</td></tr>
<tr><td>others</td><td>Not used</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12"></td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>IFPF [2:0]</th></tr>
<tr><td>Power On Sequence</td><td>8’h06h</td></tr>
<tr><td>HW Reset</td><td>8’h06h</td></tr>
</table></td></tr>
</table>

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6.2.6. Read Display Image Format (0Dh)

<table>
<tr><td>0Dh</td><td colspan="12">Read Display Image Format</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0D</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>VSSON</td><td>0</td><td>INVON</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Description</th><th>Value</th></tr>
<tr><td rowspan="2">VSSON</td><td>Vertical mode off</td><td>0</td></tr>
<tr><td>Vertical mode on</td><td>1</td></tr>
<tr><td rowspan="3">INVON</td><td>Inversion off</td><td>0</td></tr>
<tr><td>Inversion on</td><td>1</td></tr>
<tr><td>other</td><td>Not define</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12"></td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00</td></tr>
<tr><td>HW Reset</td><td>8’h00</td></tr>
</table></td></tr>
</table>

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6.2.7. Read Display Signal Mode (0Eh)

<table>
<tr><td>0Eh</td><td colspan="12">Read Display Signal Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0E</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>TEON</td><td>TEM</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>00</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates the current status of the display as described in the table below:
<table>
<tr><th>Bit</th><th>Value</th><th>Description</th></tr>
<tr><td rowspan="2">TEON</td><td>0</td><td>Tearing effect line OFF</td></tr>
<tr><td>1</td><td>Tearing effect line ON</td></tr>
<tr><td rowspan="2">TEM</td><td>0</td><td>Tearing effect line mode 1</td></tr>
<tr><td>1</td><td>Tearing effect line mode 2</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12"></td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00h</td></tr>
<tr><td>HW Reset</td><td>8’h00h</td></tr>
</table></td></tr>
</table>

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6.2.8. Read Display Self-Diagnostic Result (0Fh)

<table>
<tr><td>0Fh</td><td colspan="12">Read Display Self-Diagnostic Result</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0F</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>F0</td></tr>
<tr><td>Description</td><td colspan="12">In sleep-in state, the value of 0fh is 0xF0. In sleep out state, the value of 0fh is 0xF0 or 0x0F alternately.</td></tr>
<tr><td>Restriction</td><td colspan="12"></td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’hF0</td></tr><tr><td>HW Reset</td><td>8’hF0</td></tr></table></td></tr>
</table>

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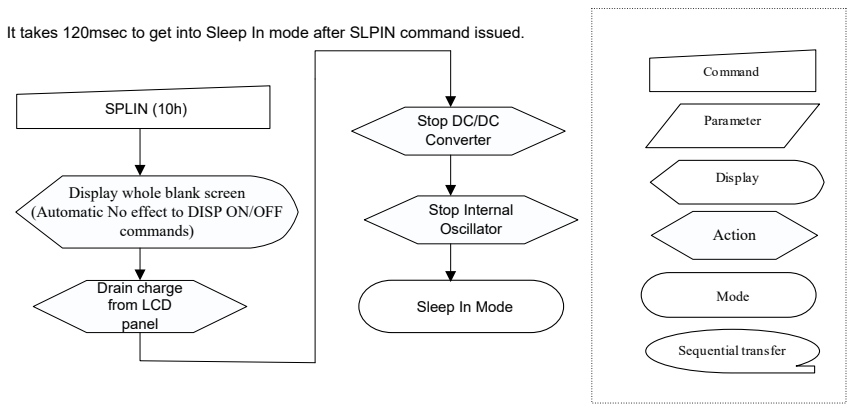
6.2.9. Sleep In (10h)

<table>
<tr><td>10h</td><td colspan="12">Enter Sleep Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>10</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command causes the LCD module to enter the minimum power consumption mode.
In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped
MCU interface and memory are still working and the memory keeps its contents.</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next to command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep IN Mode</td></tr><tr><td>HW Reset</td><td>Sleep IN Mode</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

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6.2.10. Sleep Out (11h)

<table>
<tr><td>11h</td><td colspan="12">Sleep Out Mode</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>11</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command turns off sleep mode.
the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h).
It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits stabilize.
The display module loads all display supplier’s factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode.
The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep IN Mode</td></tr><tr><td>HW Reset</td><td>Sleep IN Mode</td></tr></table></td></tr>
</table>

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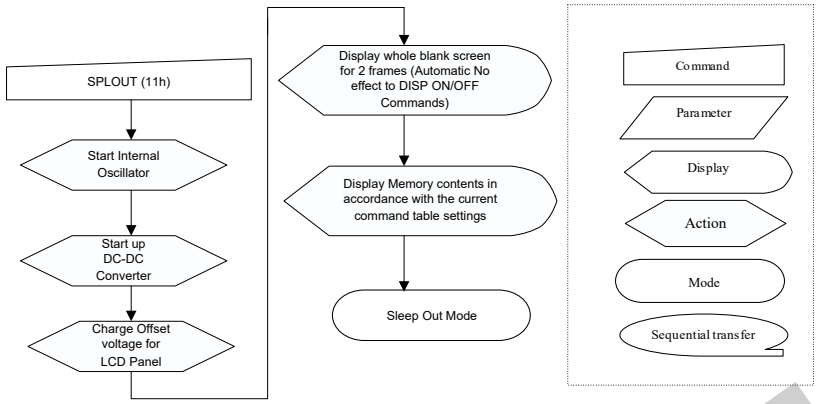
Flow Chart	

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6.2.11. Partial Mode ON (12h)

<table>
<tr><td>12h</td><td colspan="12">Partial Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>12</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command turns on partial mode The partial mode window is described by the Partial Area command (30H). To leave Partial mode, the Normal Display Mode On command (13H) should be written.</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when Partial mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12">See Partial Area (30h)</td></tr>
</table>

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6.2.12. Normal Display Mode ON (13h)

<table>
<tr><td>13h</td><td colspan="12">Normal Display Mode ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command returns the display to normal mode.
Normal display mode on means Partial mode off.
Exit from NORON by the Partial mode On command (12h)</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when Normal Display mode is active.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Normal Display Mode ON</td></tr><tr><td>HW Reset</td><td>Normal Display Mode ON</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12">See Partial Area (30h)</td></tr>
</table>

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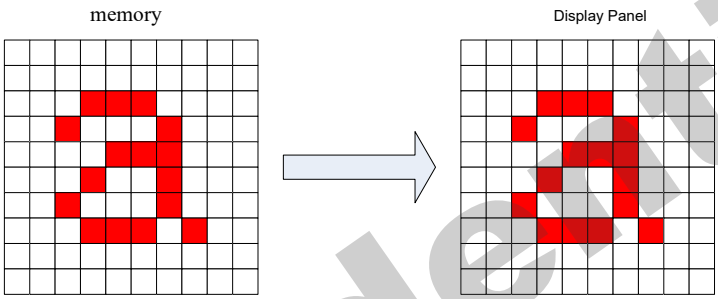
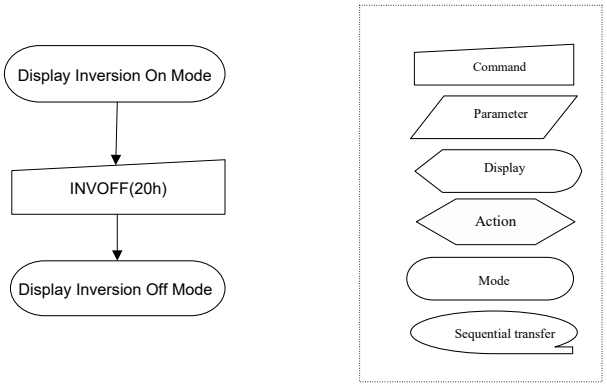
6.2.13. Display Inversion OFF (20h)

<table>
<tr><td>20h</td><td colspan="12">Display Inversion OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>20</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to recover from display inversion mode.
This command makes no change of the content of frame memory.
This command doesn’t change any other status.
  </td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module already is inversion OFF mode.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion OFF</td></tr><tr><td>HW Reset</td><td>Display Inversion OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12">  </td></tr>
</table>

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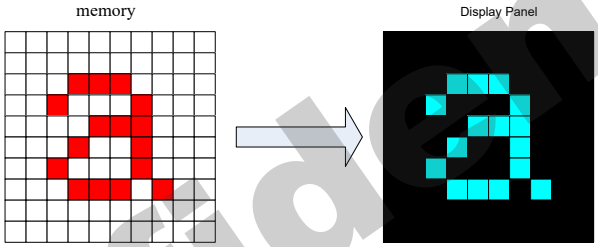
6.2.14. Display Inversion ON (21h)

<table>
<tr><td>21h</td><td colspan="12">Display Inversion ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>21</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to enter into display inversion mode.
This command makes no change of the content of frame memory. Every bit is inverted from the frame memory to the display.
This command doesn’t change any other status.
To exit Display inversion mode, the Display inversion OFF command (20h) should be written..
  </td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module already is inversion ON mode.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion OFF</td></tr><tr><td>HW Reset</td><td>Display Inversion OFF</td></tr></table></td></tr>
</table>

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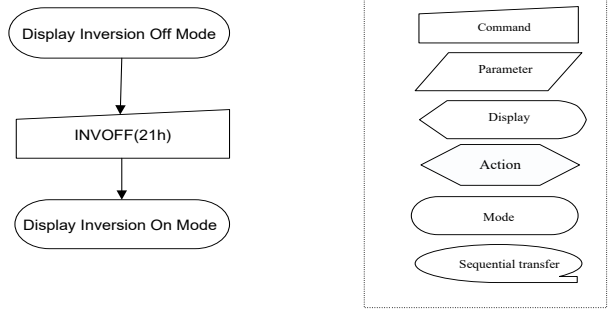
Flow Chart	

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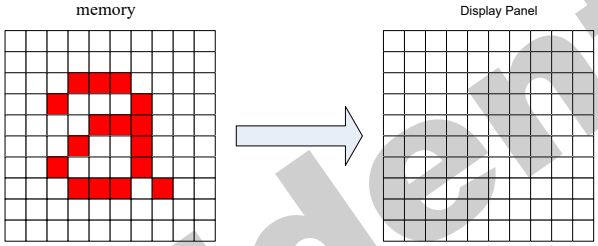
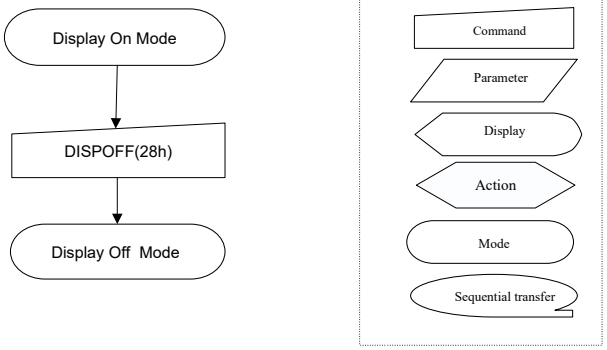
6.2.15. Display OFF (28h)

<table>
<tr><td>28h</td><td colspan="12">Display OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>28</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.
This command makes no change of contents of frame memory.
This command does not change any other status.
There will be no abnormal visible effect on the display.
  </td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module is already in display off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display OFF</td></tr><tr><td>HW Reset</td><td>Display OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12">  </td></tr>
</table>

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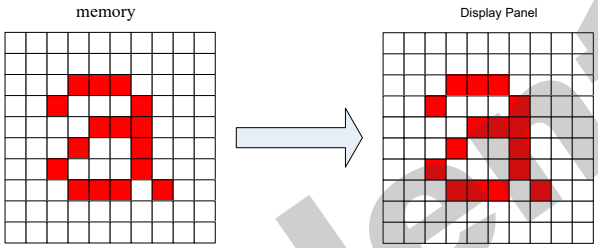
6.2.16. Display ON (29h)

<table>
<tr><td>29h</td><td colspan="12">Display ON</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>29</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.
This command makes no change of contents of frame memory.
This command does not change any other status.
  </td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module is already in display on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Display OFF</td></tr><tr><td>HW Reset</td><td>Display OFF</td></tr></table></td></tr>
</table>

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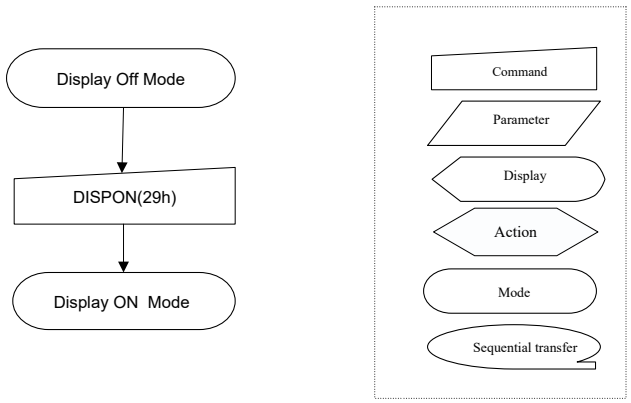
Flow Chart	

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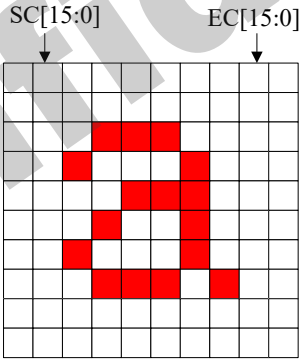
6.2.17. Column Address Set (2Ah)

2Ah	Column Address Set											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	0	1	0	1	0	2A
1st Parameter	1	1	↑	SC15	SC14	SC13	SC12	SC11	SC10	SC9	SC8	Note1
2nd Parameter	1	1	↑	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	Note1
3rd Parameter	1	1	↑	EC15	EC14	EC13	EC12	EC11	EC10	EC9	EC8	Note1
4th Parameter	1	1	↑	EC7	EC6	EC5	EC4	EC3	EC2	EC1	EC0	Note1
Description	This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SC [15:0] and EC [15:0] are referred when RAMWR command comes. Each value represents one column line in the Frame Memory.  											
Restriction	SC [15:0] always must be equal to or less than EC [15:0]. When SC [15:0] or EC [15:0] is greater than maximum address like below, data of out of range will be ignored Note1： 1. 128X128 memory base (GM = ‘01’) (Parameter range: 0 ≤ SC [15:0] ≤ EC [15:0] ≤ 127 (007Fh)): MV=”0”) (Parameter range: 0 ≤ SC [15:0] ≤ EC [15:0] ≤ 127 (007Fh)): MV=”1”) 2. 128X160 memory base (GM = ‘11’) (Parameter range: 0 ≤ SC [15:0] ≤ EC [15:0] ≤ 127 (007Fh)): MV=”0”) (Parameter range: 0 ≤ SC [15:0] ≤ EC [15:0] ≤ 159 (009Fh)): MV=”1”)											

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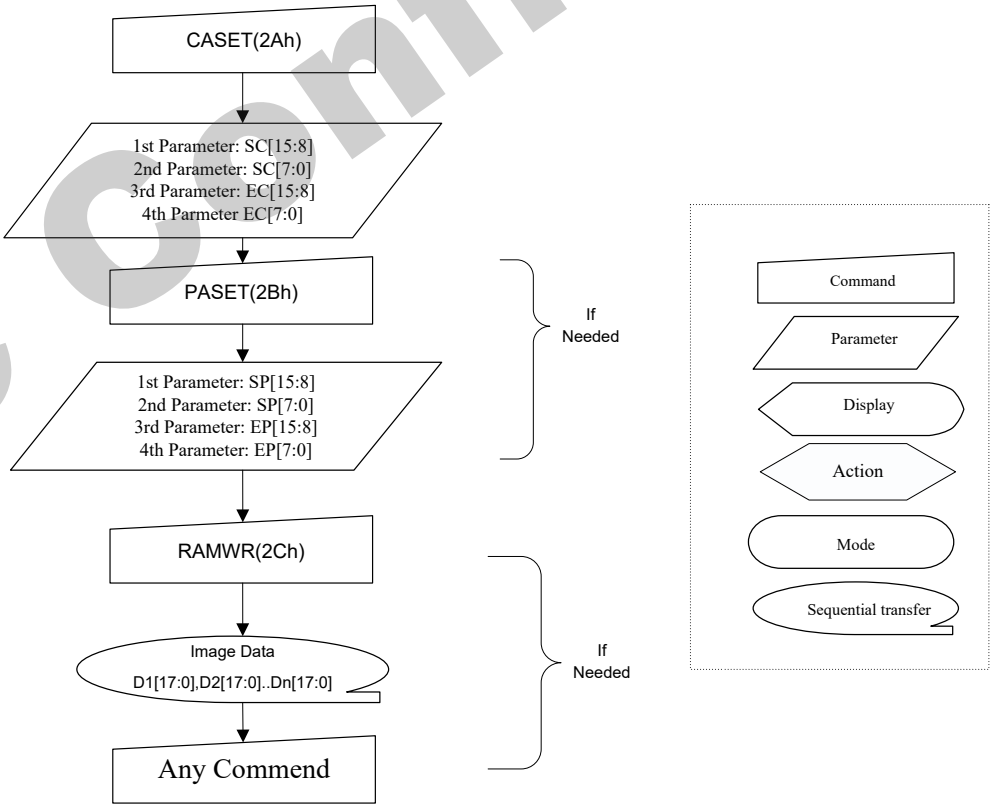
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

GM	Status	Default Value		
		SC	EC (MV=0)	EC (MV=1)
GM= '01' (128x128 Memory Base)	Power On Sequence	0000h	007Fh (127)	
	HW Reset	0000h	007Fh (127)	
GM= '11' (128x160 memory base)	Power On Sequence	0000h	007Fh (127)	
	HW Reset	0000h	007Fh (127)	

Flow Chart



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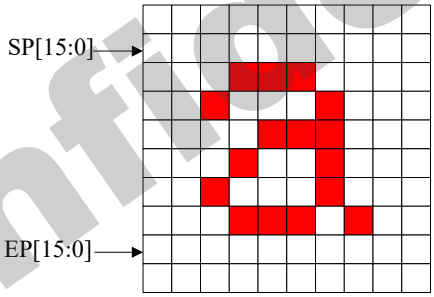
6.2.18. Row Address Set (2Bh)

2Bh	Row Address Set												
	D/CX	RDX	WRX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	XX	0	0	1	0	1	0	1	1	2B
1st Parameter	1	1	↑	XX	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8	Note2
2nd Parameter	1	1	↑	XX	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	Note2
3rd Parameter	1	1	↑	XX	EP15	EP14	EP13	EP12	EP11	EP10	EP9	EP8	Note2
4th Parameter	1	1	↑	XX	EP7	EP6	EP5	EP4	EP3	EP2	EP1	EP0	Note2
Description	This command is used to define area of frame memory where MCU can access. This command makes no change on the other driver status. The values of SP [15:0] and EP [15:0] are referred when RAMWR command comes. Each value represents one Page line in the Frame Memory.  												
Restriction	SP [15:0] always must be equal to or less than EP [15:0]. When SP [15:0] or EP [15:0] is greater than maximum address like below, data of out of range will be ignored. Note2： 1. 128X128 memory base (GM = ’01’) (Parameter range: 0 < SP [15:0] < EP [15:0] < 127 (007Fh)): MV=”0” (Parameter range: 0 < SP [15:0] < EP [15:0] < 127 (007F h)): MV=”1” 2. 128X160 memory base (GM = ’11’) (Parameter range: 0 < SP [15:0] < EP [15:0] < 159 (009Fh)): MV=”0” (Parameter range: 0 < SP [15:0] < EP [15:0] < 127 (007Fh)): MV=”1”												
Register Availability													

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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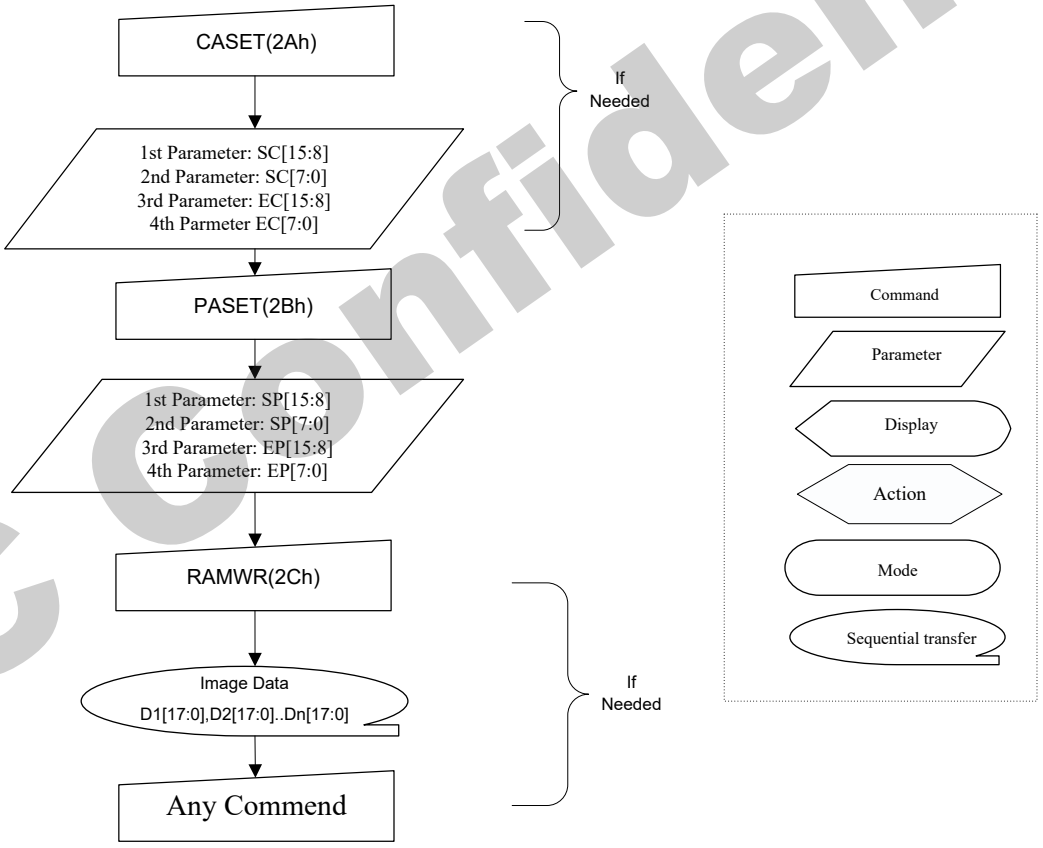
Default

GM	Status	Default Value		
		SC	EC (MV=0)	EC (MV=1)
GM= '01' (128x128 Memory Base)	Power On Sequence	0000h	007Fh (127)	
	HW Reset	0000h	007Fh (127)	
GM= '11' (128x160 memory base)	Power On Sequence	0000h	009Fh (159)	
	HW Reset	0000h	009Fh (159)	

Flow Chart



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6.2.19. Memory Write (2Ch)

<table>
<tr><td>2Ch</td><td colspan="12">Memory Write</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>2C</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td colspan="8">D1 [17:0]</td><td>XX</td></tr>
<tr><td>:</td><td>1</td><td>1</td><td>↑</td><td colspan="8">Dx [17:0]</td><td>XX</td></tr>
<tr><td>Nth Parameter</td><td>1</td><td>1</td><td>↑</td><td colspan="8">Dn [17:0]</td><td>XX</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column/Start Page positions are different in accordance with MADCTL setting.) Then D [17:0] is stored in frame memory and the column register and the page register incremented. Sending any other command can stop frame Write. X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="12"></td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Contents of memory is set randomly</td></tr><tr><td>HW Reset</td><td>Contents of memory is not cleared</td></tr></table></td></tr>
</table>

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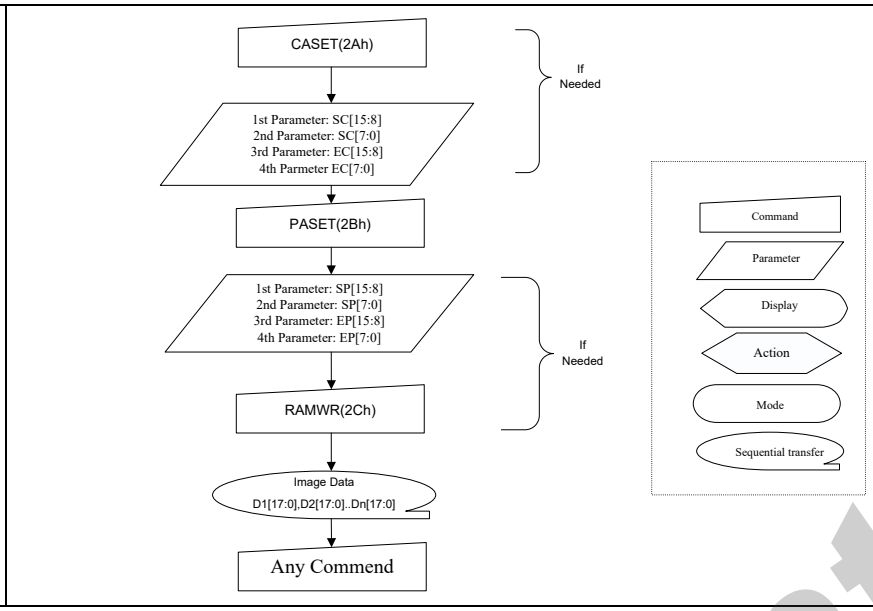
Flow Chart	

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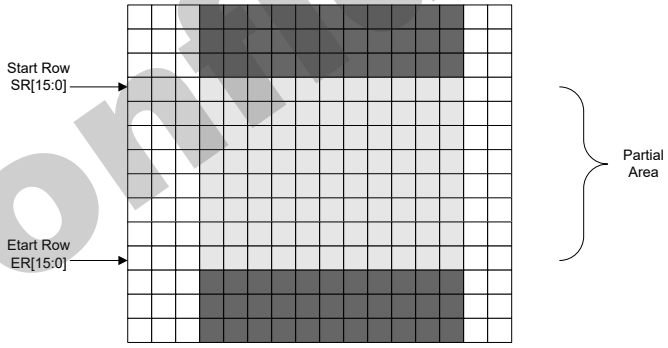
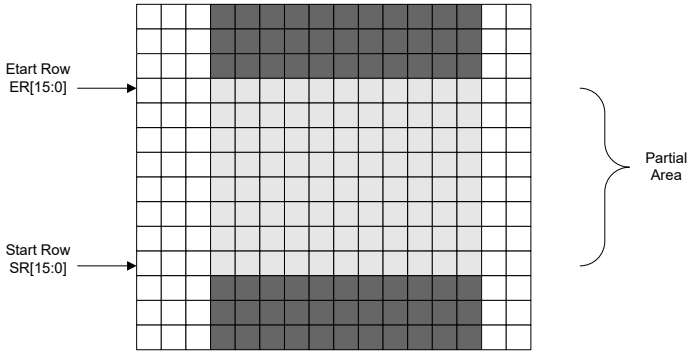
6.2.20. Partial Area (30h)

30h	Partial Area											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	0	0	0	30h
1st Parameter	1	1	↑	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	00
2nd Parameter	1	1	↑	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00
3rd Parameter	1	1	↑	ER15	ER14	ER13	ER12	ER11	ER10	ER9	ER8	00
4th Parameter	1	1	↑	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	A1
Description	This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the Frame Memory Line Pointer. If End Row>Start Row when ML=0:  If End Row>Start Row when ML=1:  If End Row<Start Row when ML =0:											

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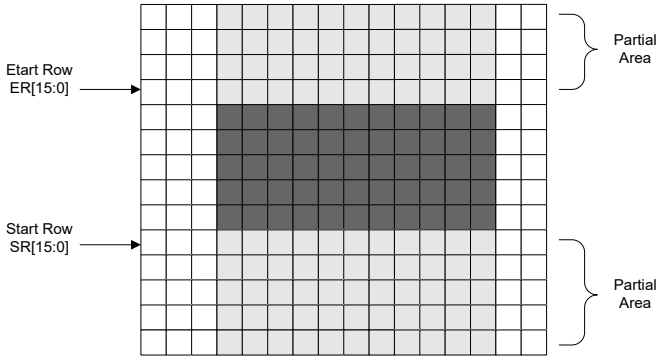

If End Row = Start Row then the Partial Area will be one row deep.

X = Don't care.

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
	SR [15:0]	ER [15:0]	
GM[1:0]	xx	GM = '01'	GM = '11'
Power On Sequence	16'h0000	16'h007F	16'h009F
HW Reset	16'h0000	16'h007F	16'h009F

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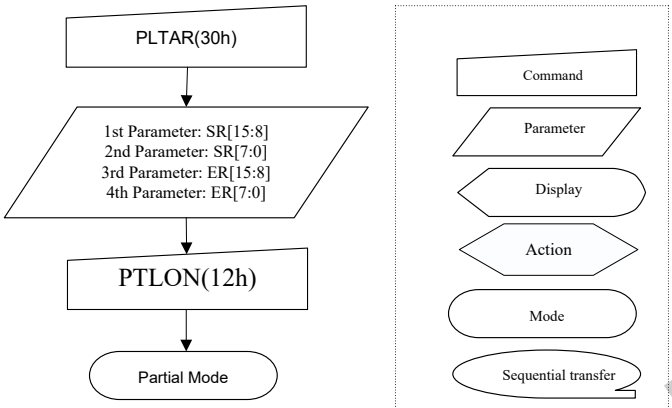
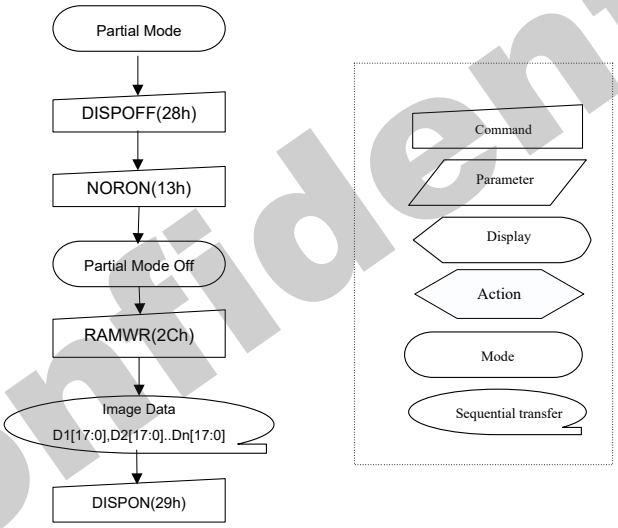
Flow Chart

1. To Enter Partial Mode



2. To Leave Partial Mode



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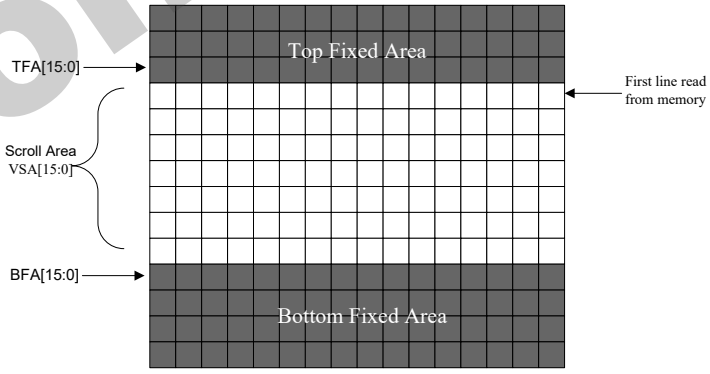
6.2.21. Vertical Scrolling Definition (33h)

33h	Vertical Scrolling Definition											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	0	1	1	33h
1st Parameter	1	1	↑	TFA [15:8]								00
2nd Parameter	1	1	↑	TFA [7:0]								00
3rd Parameter	1	1	↑	VSA [15:8]								00
4th Parameter	1	1	↑	VSA [7:0]								A0
5th Parameter	1	1	↑	BFA [15:8]								00
6th Parameter	1	1	↑	BFA [7:0]								00

Description

This command defines the Vertical Scrolling Area of the display.
When MADCTL B4=0
The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Top of the Frame Memory and Display).
The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.
The 5th & 6th parameter BFA [15:0] describes the Bottom Fixed Area (in No. of lines from Bottom of the Frame Memory and Display). TFA, VSA and BFA refer to the Frame Memory Line Pointer.



When MADCTL B4=1
The 1st & 2nd parameter TFA [15:0] describes the Top Fixed Area (in No. of lines from Bottom of the Frame Memory and Display).
The 3rd & 4th parameter VSA [15:0] describes the height of the Vertical Scrolling Area (in No. of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.
The 5th & 6th parameter BFA [15:0] describes the Bottom Fixed Area (in No. of lines from Top of the
Frame Memory and Display).

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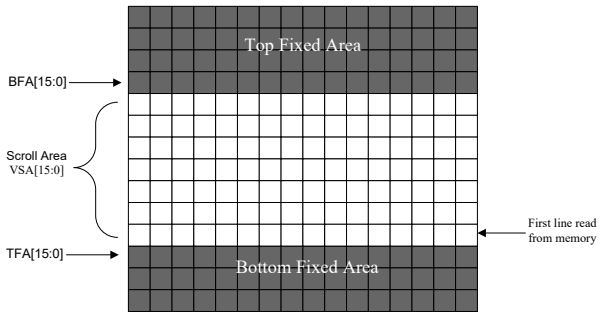

X = Don’t care.

Restriction

The condition is (TFA+VSA+BFA)=128 in 128RGBx128 (GM=”01”)
The condition is (TFA+VSA+BFA)=160 in 128RGBx160 (GM=”11”)
Otherwise Scrolling mode is undefined.
In Vertical Scroll Mode, MADCTR parameter MV should be set to ‘0’, this only affects the Frame Memory Write.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value	
	TFA [15:0]	VSA [15:0]
Power On Sequence	16’h0000	16’h00A0
HW Reset	16’h0000	16’h00A0

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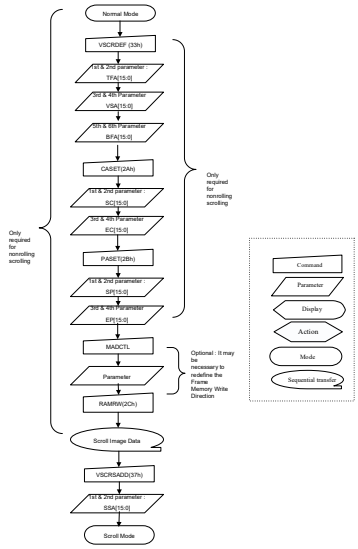
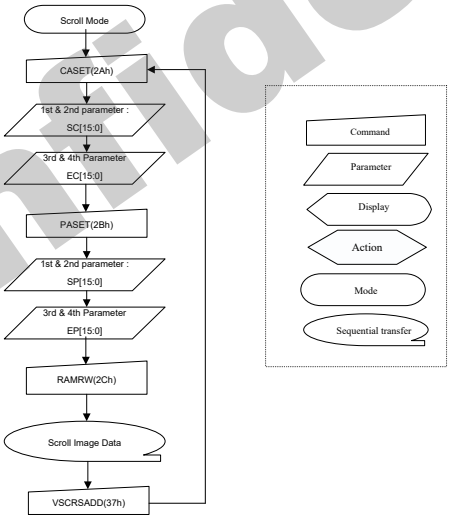
Flow Chart

1. To enter Vertical Scroll Mode :

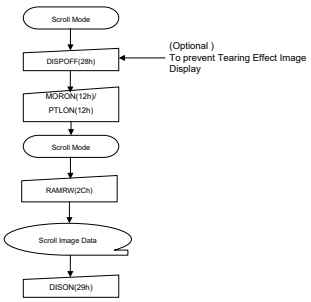


Note : The Frame Memory Window size ,must be defined correctly otherwise undesirable image will be displayed.

2.Continuous Scroll :



3.To Leave Vertical Scroll Mode:



Note: Scroll Mode can be left by both the Normal Display Mode ON (13h) and Partial Mode ON (12h) commands.

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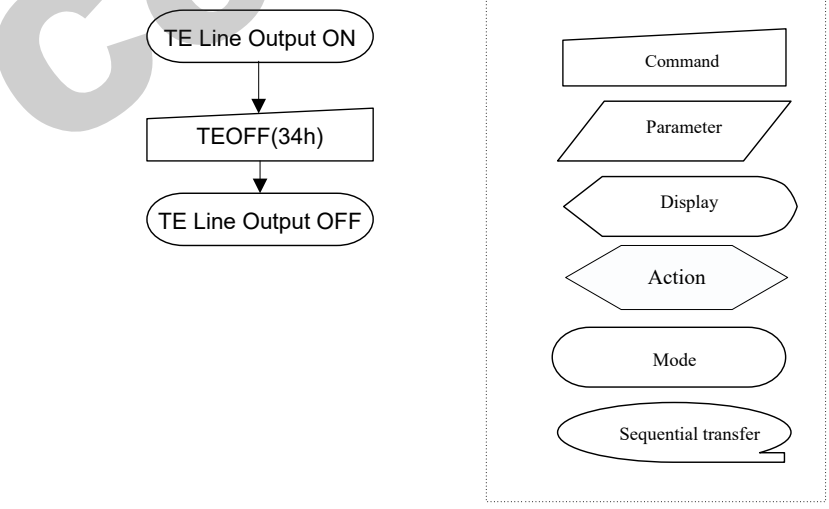
6.2.22. Tearing Effect Line OFF (34h)

<table>
<tr><td>34h</td><td colspan="12">Tearing Effect Line OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>34</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when Tearing Effect output is already OFF.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>OFF</td></tr><tr><td>HW Reset</td><td>OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

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6.2.23. Tearing Effect Line ON (35h)

35h	Tearing Effect Line ON											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	1	0	1	35
Parameter	1	1	↑	0	0	0	0	0	0	0	M	00

Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by
changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.

When **M=0**:
The Tearing Effect Output line consists of V-Blanking information only:

When **M=1**:
The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:

Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.
X = Don't care.

Restriction

This command has no effect when Tearing Effect output is already ON

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value

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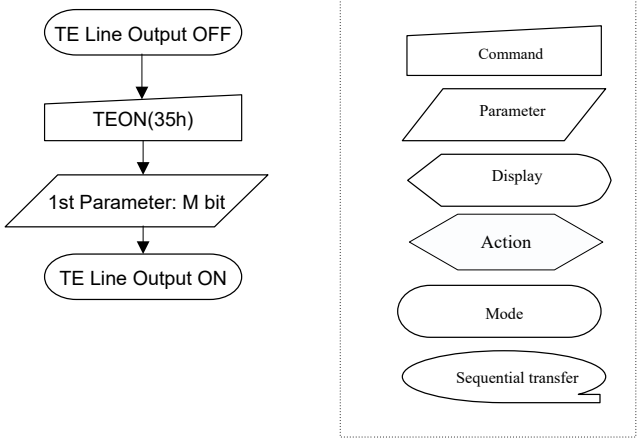
Power On Sequence	OFF
HW Reset	OFF

Flow Chart



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6.2.24. Memory Access Ctrl (36h)

36h	Tearing Effect Line ON											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	1	1	0	36
Parameter	1	1	↑	MY	MX	MV	ML	BGR	0	0	0	00

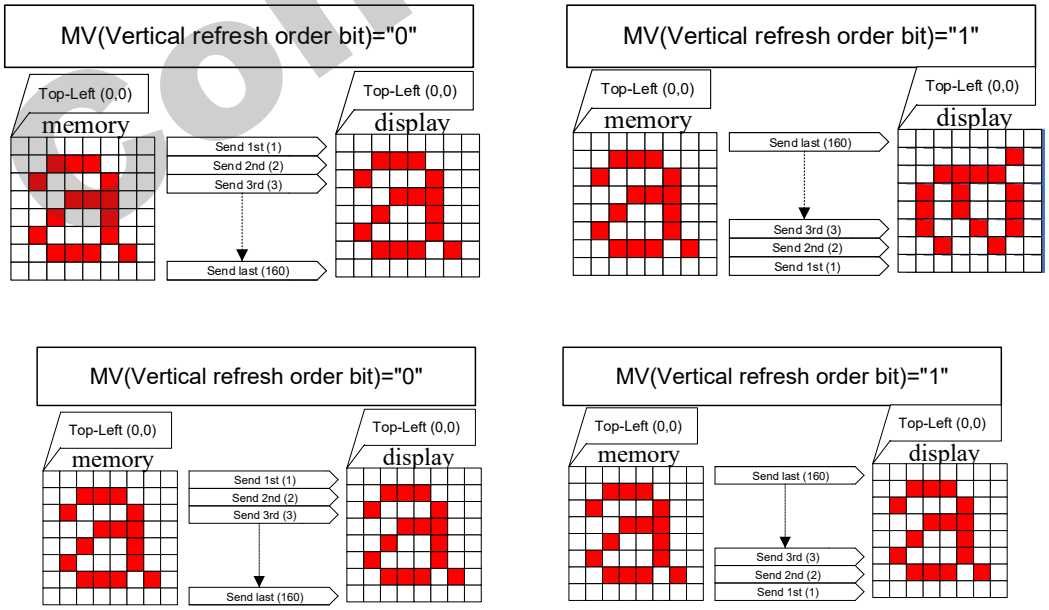
Description

This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.

Bit	Name	Description
MY	Row Address Ord□r	These 3 bits control MCU to memory write/read direction.
MX	Column Address Order	
MV	Row / Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control.
BGR	RGB-BGR Order	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)

Note: When BGR bit is changed, the new setting is active immediately without update the content in Frame Memory again.

X = Don't care.



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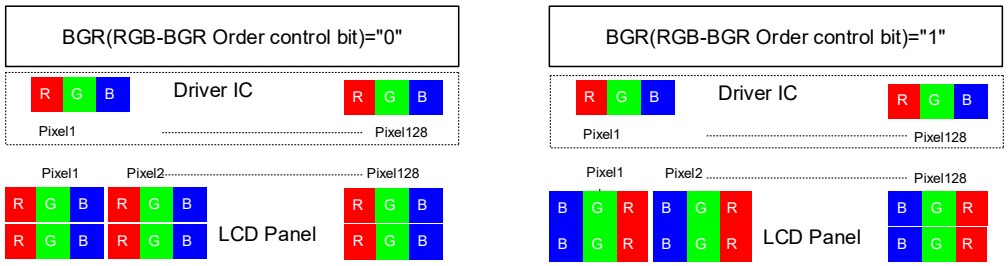
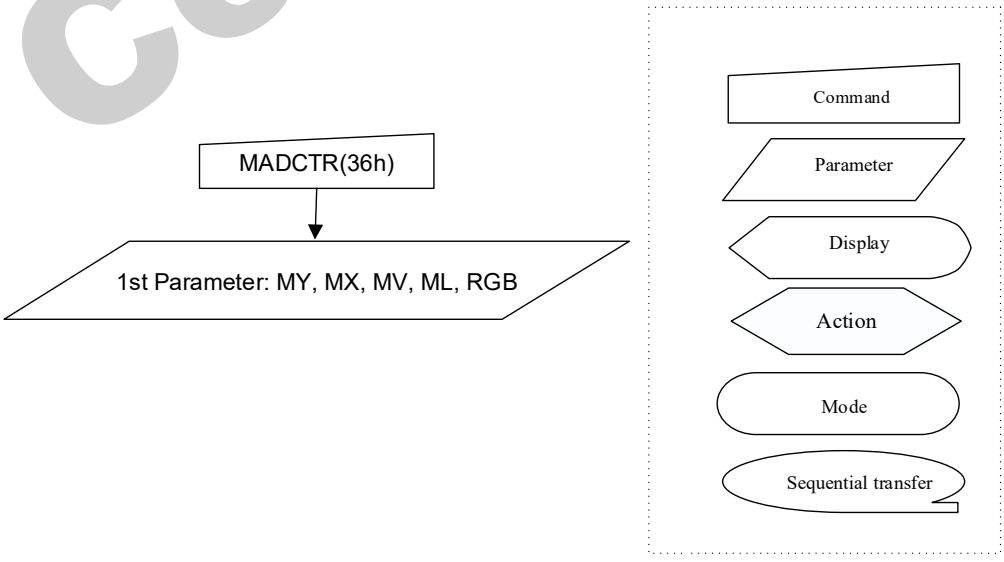
<table>
<tr><td>Description</td><td>


Note: Top-Left (0,0) means a physical memory location.
</td></tr>
<tr><td>Restriction</td><td>This command has no effect when Tearing Effect output is already ON</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h00h</td></tr>
<tr><td>HW Reset</td><td>8’h00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>


</td></tr>
</table>

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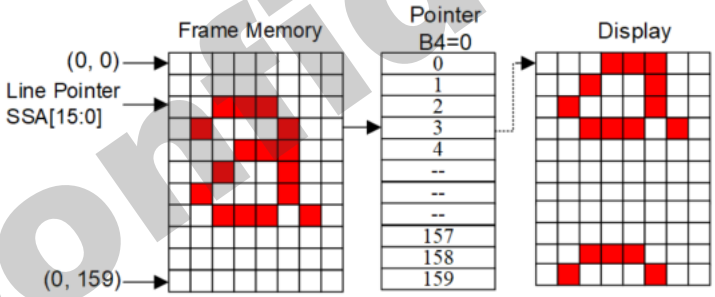
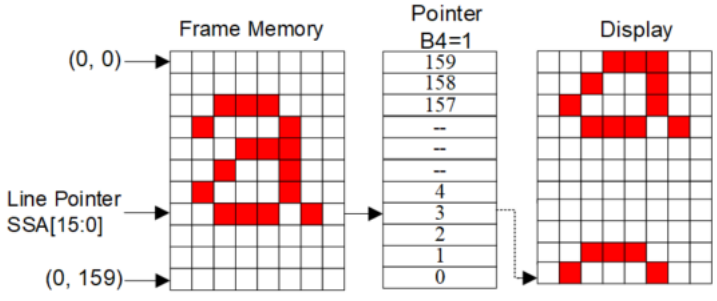
6.2.25. Vertical Scrolling Start Address (37h)

37h	VSCRSADD (Vertical Scrolling Start Address)											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	1	1	1	37
1st Parameter	1	1	↑	00								00
2nd Parameter	1	1	↑	SSA [7:0]								00
Description	This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode. The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below: When MADCTL B4=0 Example: When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 160 and SSA='3'.											
Description	 When MADCTL B4=1 Example: When Top Fixed Area = Bottom Fixed Area = 00, Vertical Scrolling Area = 160 and SSA='3'.  *Note: (1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. SSA refers to the Frame Memory line Pointer.* *(2) This command is ignored when the GC9107 enters Partial mode.* X = Don't care											

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<table>
<tr><td>Restriction</td><td>This command has no effect when Tearing Effect output is already ON</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>No</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>No</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>SSA [7:0]</th></tr>
<tr><td>Power On Sequence</td><td>8’h00</td></tr>
<tr><td>HW Reset</td><td>8’h00</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td>See Vertical Scrolling Definition (33h) description.</td></tr>
</table>

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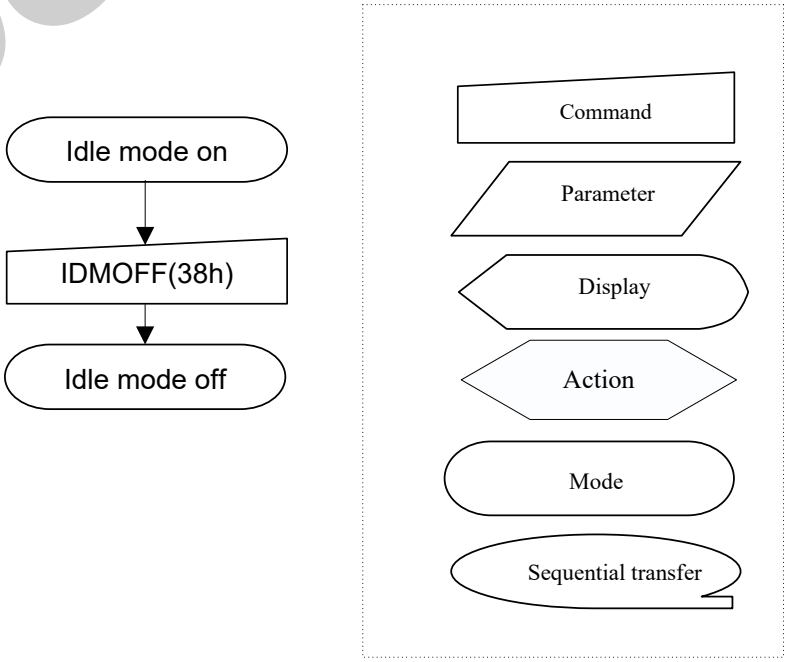
6.2.26. Idle Mode OFF (38h)

<table>
<tr><td>38h</td><td colspan="12">Idle Mode OFF</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>38</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to recover from Idle mode on.
In the idle off mode, LCD can display maximum 262,144 colors.
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Idle mode OFF</td></tr><tr><td>HW Reset</td><td>Idle mode OFF</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="12"> 
</td></tr>
</table>

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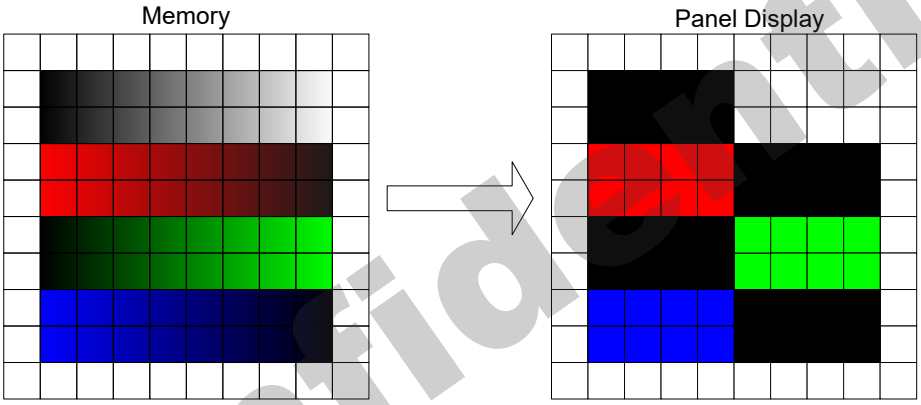
6.2.27. Idle Mode ON (39h)

39h	Idle Mode ON											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	1	0	0	1	39
Parameter	No Parameter											

Description

This command is used to enter into Idle mode on.

In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.



	Memory Contents vs. Display Color		
	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B2 B1 B0
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XX□XX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magenta	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

X = Don't care.

Restriction

This command has no effect when module is already in idle off mode.

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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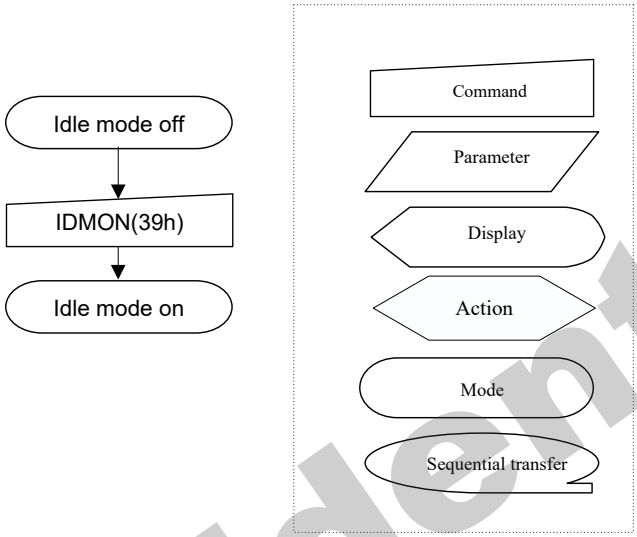
Default

Status	Default Value
Power On Sequence	Idle mode OFF
HW Reset	Idle mode OFF

Flow Chart



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6.2.28. COLMOD: Pixel Format Set (3Ah)

<table>
<tr><td>3Ah</td><td colspan="12">Pixel Format Set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3A</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td colspan="3">IFPF [2:0]</td><td>06</td></tr>
<tr><td>Description</td><td colspan="12">This command sets the pixel format for the RGB image data used by the interface. IFPF [2:0] is the pixel format of MCU interface. The pixel format is shown in the table below.
<table>
<tr><th colspan="3">IFPF [2:0]</th><th>MCU Interface Format</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>12 bits / pixel</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>16 bits / pixel</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>18 bits / pixel</td></tr>
<tr><td colspan="3">others</td><td>Reserved</td></tr>
</table>
X = Don’t care.</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module is already in idle off mode.</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th rowspan="2">Status</th><th>Default Value</th></tr>
<tr><th>IFPF [2:0]</th></tr>
<tr><td>Power On Sequence</td><td>8’h06</td></tr>
<tr><td>HW Reset</td><td>8’h06</td></tr>
</table>
</td></tr>
</table>

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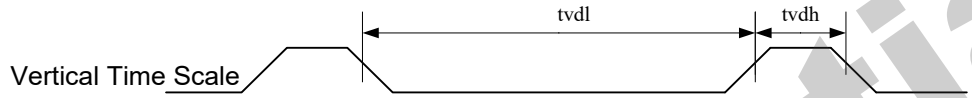
6.2.29. Test Scanline Set (44h)

<table>
<tr><td>3Ah</td><td colspan="12">Test Scanline Set</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>44</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td colspan="8">SCNL[7:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="12">This command turns on the display Tearing Effect output signal on the TE signal line when the display reaches line equal the value of SCNL [7:0]
 

Note:that set_tear_scanline with STS is equivalent to set_tear_on with bp+GateN-2(N=1、2、3...220)
eg:when the SCNL [7:0]=6,the TE will output at the position of (8-bp)
when the SCNL [7:0]=7,the TE will output at the position of (9-bp)
when the SCNL [7:0]=8,the TE will output at the position of (10-bp)
…….</td></tr>
<tr><td>Restriction</td><td colspan="12">The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>HW Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

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6.2.30. Test Scanline Get (45h)

<table>
<tr><td>3Ah</td><td colspan="12">Test Scanline Get</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>45</td></tr>
<tr><td>Parameter</td><td>1</td><td>↑</td><td>1</td><td colspan="8">SCNL[7:0]</td><td>--</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates the current status of CMD 44h(SCNL[7:0])</td></tr>
<tr><td>Restriction</td><td colspan="12">The Tearing Effect Output line shall be active low when the display module is in Sleep mode.</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h00</td></tr><tr><td>HW Reset</td><td>8’h00</td></tr></table></td></tr>
</table>

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6.2.31. Customized display identification information(D3h)

<table>
<tr><td>D3h</td><td colspan="12">6.2.29. Customized display identification information</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>D3</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>XX</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td colspan="8">Customized_ID1_1 [7:0]</td><td>XX</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>↑</td><td>1</td><td colspan="8">Customized_ID1_2 [7:0]</td><td>XX</td></tr>
<tr><td>4th Parameter</td><td>1</td><td>↑</td><td>1</td><td colspan="8">Customized_ID1_3[7:0]</td><td>XX</td></tr>
<tr><td>Description</td><td colspan="12">This is a custom identification information register specially open to customers
The 1st parameter is dummy data.
The 2nd parameter (Man_ID1_1 [7:0]): Customized ID.
The 3rd parameter (Man_ID1_2 [7:0]): Customized ID.
The 4th parameter (Man_ID1_3 [7:0]): Customized ID.</td></tr>
<tr><td>Restriction</td><td colspan="12"></td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>24’hXXXXXX</td></tr><tr><td>HW Reset</td><td>24’hXXXXXX</td></tr></table></td></tr>
</table>

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6.2.32. Read ID1 (DAh)

<table>
<tr><td>DAh</td><td colspan="12">Read ID1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>DA</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td colspan="8">ID1 [7:0]</td><td>00</td></tr>
<tr><td>Description</td><td colspan="12">This read byte identifies the LCD module’s manufacturer ID and it is specified by User
The 1st parameter is dummy data.
The 2nd parameter is LCD module’s manufacturer ID.
The ID2 can be programmed by MTP function.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="12">None</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value (Before MTP program)</th><th>Default Value (After MTP program)</th></tr><tr><td>Power On Sequence</td><td>8’h00</td><td>8’h00</td></tr><tr><td>HW Reset</td><td>8’h00</td><td>8’h00</td></tr></table></td></tr>
</table>

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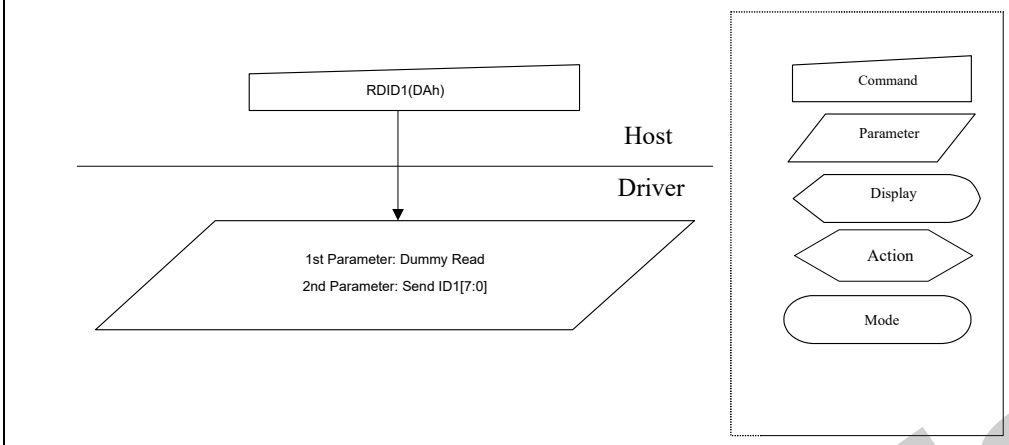
Flow Chart	

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6.2.33. Read ID2 (DBh)

<table>
<tr><td>DBh</td><td colspan="12">Read ID2</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>DB</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td colspan="8">ID2 [7:0]</td><td>91</td></tr>
<tr><td>Description</td><td colspan="12">This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User’s agreement) and changes each time a revision is made to the display, material or construction specifications.
The 1st parameter is dummy data.
The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh.
The ID2 can be programmed by MTP function.
X = Don’t care</td></tr>
<tr><td>Restriction</td><td colspan="12">None</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value (Before MTP program)</th><th>Default Value (After MTP program)</th></tr><tr><td>Power On Sequence</td><td>8’h91</td><td>8’h91</td></tr><tr><td>HW Reset</td><td>8’h91</td><td>8’h91</td></tr></table></td></tr>
</table>

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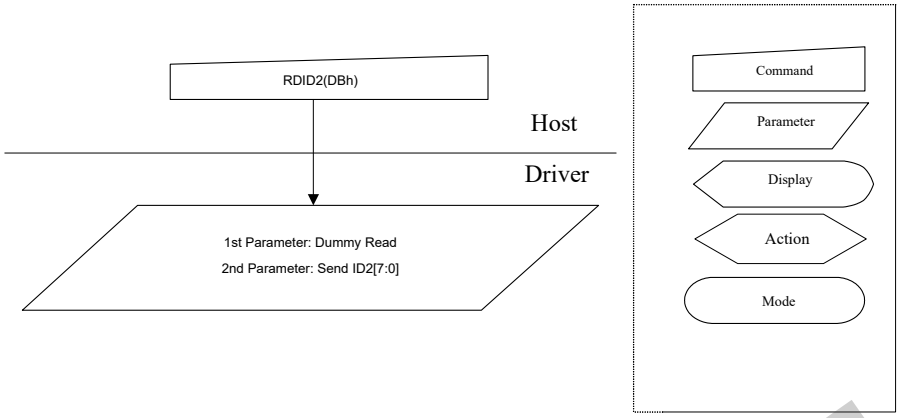
Flow Chart	

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6.2.34. Read ID3 (DCh)

DCh	Read ID3											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	1	0	0	DC
1st Parameter	1	↑	1	X	X	X	X	X	X	X	X	X
2nd Parameter	1	↑	1	ID3 [7:0]								07
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier (with User's agreement) and changes each time a revision is made to the display, material or construction specifications. The 1st parameter is dummy data. The 2nd parameter is LCD module/driver version ID and the ID parameter range is from 80h to FFh. The ID3 can be programmed by MTP function. X = Don't care											
Restriction	None											

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value (Before MTP program)	Default Value (After MTP program)
Power On Sequence	8'h04	8'h07
HW Reset	8'h04	8'h07

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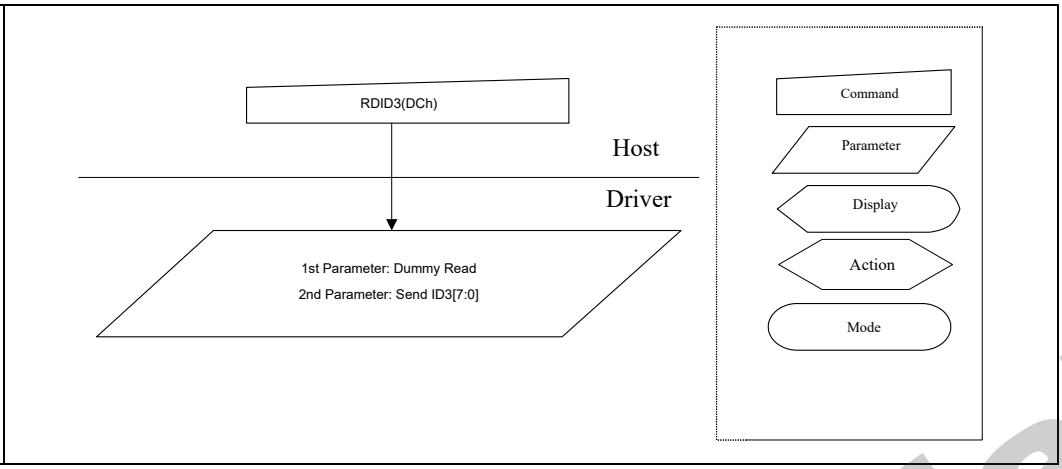
Flow Chart	

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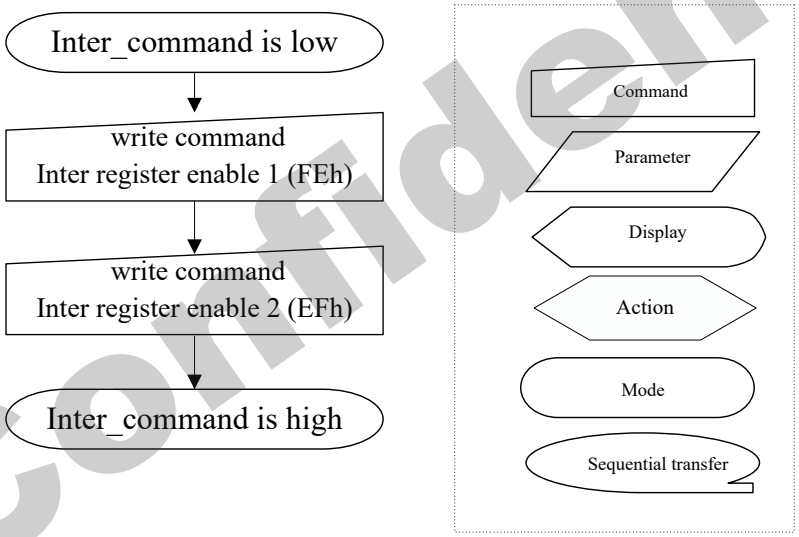
6.3. Description of Internal Command

6.3.1. Inter register enable 1 (FEh)

<table>
<tr><td>FEh</td><td colspan="12">Inter register enable 1</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>FEh</td></tr>
<tr><td>Parameter</td><td colspan="12">No Parameter</td></tr>
<tr><td>Description</td><td colspan="12">This command is used for Inter_command controlling.
To set Inter_command high, you should write Inter register enable 1 (FEh) and Inter register enable 2 (EFh) continuously.
Once Inter_command is set high, only hardware or software reset can turn it to low.
 
</td></tr>
<tr><td>Restriction</td><td colspan="12"></td></tr>
<tr><td>Register Availability</td><td colspan="12"><table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
</table>

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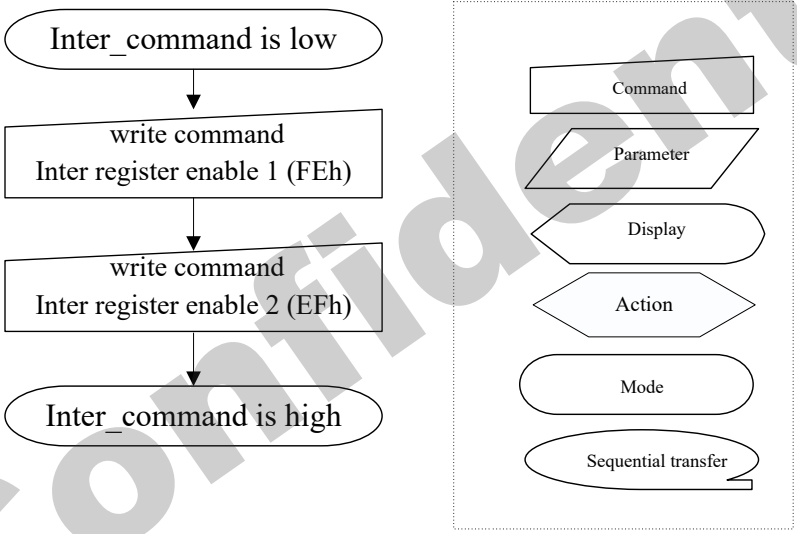
6.3.2. Inter register enable 2 (EFh)

EFh	Inter register enable 2											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	1	1	1	1	EFh
Parameter	No Parameter											
Description	This command is used for Inter_command controlling. To set Inter_command high, you should write Inter register enable 1 (FEh) and Inter register enable 2 (EFh) continuously. Once Inter_command is set high, only hardware or software reset can turn it to low. 											
Restriction												
Register Availability												

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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6.3.3. Complement Principle of RGB 5, 6, 5（ACh）

<table>
<tr><td>ACh</td><td colspan="12">Principle of complement of RGB 5, 6, 5</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>AC</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td colspan="2">epf[1:0]</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>C0</td></tr>
<tr><td>Description</td><td colspan="12">
To have access to “ACh” , bit [4] of “B6h” need be set to 1
RGB 6,6,6: R0~R5,G0~G5,B0~B5
When the RGB data format is 5,6,5, mainly R0 and B0 need special complement. The corresponding complement principle is shown in the table below
<table>
<tr><th>epf[1:0]</th><th>Description</th><th>Exception</th></tr>
<tr><td>0</td><td>R0=B0=0</td><td>When the data is FFh,
R0=B0=1</td></tr>
<tr><td>1</td><td>R0=B0=1</td><td>When the data is 00h,
R0=B0=0</td></tr>
<tr><td>2</td><td>R0=R5，B0=B5</td><td>-</td></tr>
<tr><td>3</td><td>R0=B0=G0</td><td>-</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="12"></td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode□On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’hC0</td></tr>
<tr><td>HW Reset</td><td>8’hC0</td></tr>
</table>
</td></tr>
</table>

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6.3.4. Blanking Porch Control（ADh）

ADh	Blanking Porch Control											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	0	1	1	0	1	AD
1st Parameter	1	1	↑	0	fp[6:0]							12
2nd Parameter	1	1	↑	0	bp[6:0]							0A

Description

To have access to "ADh" , bit [5] of "B6h" need be set to 1

fp[6:0] / bp [6:0]: The line number of vertical front and back porch period respectively.

fp [6:0]/ bp [6:0]	Number of T_{line} of front/back porch	fp [6:0]/ bp [6:0]	Number of T_{line} of front/back porch
0000000	Setting inhibited	1000000	64
0000001	Setting inhibited	1000001	65
0000010	2	1000010	66
0000011	3	1000011	67
:	:	:	:
0001010	10	:	:
:	:	:	:
0010010	18	:	:
:	:	:	:
0111110	62	1111110	126
0111111	63	1111111	127

Restriction

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	16'h120A
HW Reset	16'h120A

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6.3.5. Display Inversion Control (B4h)

<table>
<tr><td>B4h</td><td colspan="12">Frame Rate and Display Inversion Control</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>B4</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="3">inv_ctl[2:0]</td><td>02</td></tr>
<tr><td>Description</td><td colspan="12">Display inversion mode set
inv_ctl[2:0]: Inversion setting in full colors normal mode(Normal mode on)
<table><tr><th>inv_ctl[2:0]</th><th>Inversion</th></tr><tr><td>0</td><td>Row inversion</td></tr><tr><td>1</td><td>Frame inversion</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="12">Inter_command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h02</td></tr><tr><td>HW Reset</td><td>8’h02</td></tr></table></td></tr>
</table>

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6.3.6. AVDD_VCL_CLK (E3h)

<table>
<tr><th>E3h</th><th colspan="12">AVDD_CLK</th></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>E3</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>0</td><td colspan="3">AVDD_CLK_AD<2:0></td><td>0</td><td colspan="3">VCL_CLK_AD<2:0></td><td>22</td></tr>
<tr><td>Description</td><td colspan="12">
To have access to “E3h” , bit [3] of “B1h” need be set to 1

AVDD_CLK_AD<2:0>：
<table>
<tr><th>AVDD_CLK_AD</th><th>Period AVDD
T=50ns</th></tr>
<tr><td>0</td><td>2T</td></tr>
<tr><td>1</td><td>3T</td></tr>
<tr><td>2</td><td>4T</td></tr>
<tr><td>3</td><td>5T</td></tr>
<tr><td>4</td><td>6T</td></tr>
<tr><td>5</td><td>7T</td></tr>
<tr><td>6</td><td>8T</td></tr>
<tr><td>7</td><td>9T</td></tr>
</table>
VCL_CLK_AD<2:0>：
<table>
<tr><th>VCL_CLK_AD</th><th>Period VCL
T=50ns</th></tr>
<tr><td>0</td><td>2T</td></tr>
<tr><td>1</td><td>3T</td></tr>
<tr><td>2</td><td>4T</td></tr>
<tr><td>3</td><td>5T</td></tr>
<tr><td>4</td><td>6T</td></tr>
<tr><td>5</td><td>7T</td></tr>
<tr><td>6</td><td>8T</td></tr>
<tr><td>7</td><td>9T</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="12">Inter command should be set high to enable this command</td></tr>
</table>

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<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle □ode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h22</td></tr>
<tr><td>HW Reset</td><td>8’h22</td></tr>
</table>
</td></tr>
</table>

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6.3.7. VGH_VGL_CLK (EAh)

EAh	VGH_VGL_CLK											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	0	1	0	1	0	EA
1st Parameter	1	1	↑	VGH_CLK_DIV [3:0]				VGL_CLK_DIV [3:0]				94

Description

To have access to "EAh" , bit [2] of "B2h" need be set to 1

VGH_CLK_DIV [3:0]:

Value	DIV	VGH Operation (MHZ)	Value	DIV	VGH Operation (MHZ)
0	2	6.0	**8**	10	1.2
1	3	4.0	**9**	12	1.0
2	4	3.0	**10**	15	0.8
3	5	2.4	**11**	20	0.6
4	6	2.0	**12**	24	0.5
5	7	1.7	**13**	30	0.4
6	8	1.5	**14**	40	0.3
7	9	1.3	**15**	60	0.2

VGL_CLK_DIV [3:0]:

Value	DIV	VGL Operation (MHZ)	Value	DIV	VGL Operation (MHZ)
0	2	6.0	**8**	10	1.2
1	3	4.0	**9**	12	1.0
2	4	3.0	**10**	15	0.8
3	5	2.4	**11**	20	0.6
4	6	2.0	**12**	24	0.5
5	7	1.7	**13**	30	0.4
6	8	1.5	**14**	40	0.3
7	9	1.3	**15**	60	0.2

Restriction	Inter command should be set high to enable this command

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<table>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h94</td></tr>
<tr><td>HW Reset</td><td>8’h94</td></tr>
</table>
</td></tr>
</table>

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6.3.8. Frame Rate Set(A8h)

A8h	Frame Rate set											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	0	1	0	0	0	A8
1st Parameter	1	1	↑	0	RTN1 [6:0]							16

Description

To have access to "A8h" , bit [0] of "B6h" need be set to 1

Rtn1	FR (HZ)	Rtn1	FR (HZ)	Rtn1	FR (HZ)	Rtn1	FR (HZ)
0x00	123	0x10	82	0x20	62	0x30	49
0x01	120	0x11	81	0x21	61	0x31	49
0x02	116	0x12	79	0x22	60	0x32	48
0x03	113	0x13	77	0x23	59	0x33	48
0x04	110	0x14	76	0x24	58	0x34	47
0x05	107	0x15	74	0x25	57	0x35	46
0x06	104	0x16	73	0x26	56	0x36	46
0x07	101	0x17	72	0x27	56	0x37	45
0x08	99	0x18	70	0x28	55	0x38	45
0x09	96	0x19	69	0x29	54	0x39	44
0x0a	94	0x1a	68	0x2a	53	0x3a	44
0x0b	92	0x1b	67	0x2b	53	0x3b	43
0x0c	90	0x1c	66	0x2c	52	0x3c	43
0x0d	88	0x1d	65	0x2d	51	0x3d	42
0x0e	86	0x1e	64	0x2e	51	0x3e	42
0x0f	84	0x1f	63	0x2f	50	0x3f	42
Rtn1	**FR HZ)**	**Rtn1**	**FR (HZ)**	**Rtn1**	**FR (HZ)**	**Rtn1**	**FR (HZ)**
0x40	41	0x50	35	0x60	31	0x70	27
0x41	41	0x51	35	0x61	31	0x71	27
0x42	40	0x52	35	0x62	30	0x72	27
0x43	40	0x53	34	0x63	30	0x73	27
0x44	39	0x54	34	0x64	30	0x74	27
0x45	39	0x55	34	0x65	30	0x75	26
0x46	39	0x56	33	0x66	29	0x76	26
0x47	38	0x57	33	0x67	29	0x77	26
0x48	38	0x58	33	0x68	29	0x78	26
0x49	38	0x59	33	0x69	29	0x79	26
0x4a	37	0x5a	32	0x6a	29	0x7a	26
0x4b	37	0x5b	32	0x6b	28	0x7b	25
0x4c	37	0x5c	32	0x6c	28	0x7c	25

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	0x4d	36	0x5d	32	0x6d	28	0x7d	25
	0x4e	36	0x5e	31	0x6e	28	0x7e	25
	0x4f	36	0x5f	31	0x6f	28	0x7f	25

Frame Rate=osc/(bp+fp+162)/（(256*(rtn1[6:4]+2)+16*rtn1[3:0]）

Default: osc=12Mhz; fp=18; bp=10; rtn1=22; Frame Rate=74Hz

Restriction: Inter command should be set high to enable this command

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	8’h16
HW Reset	8’h16

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6.3.9. VREG_CTL (E7h)

<table>
<tr><td>E7h</td><td colspan="12">VREG_CTL</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>E7</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>0</td><td colspan="7">VREG_AD[6:0]</td><td>50</td></tr>
<tr><td>Description</td><td colspan="12">To have access to “E7h” , bit [7] of “B1h” need be set to 1

VREG_AD[6:0]：
<table><tr><th>VREG_AD</th><th>VREG</th></tr><tr><td>0</td><td>2.921V</td></tr><tr><td>…</td><td>26mV/STEP</td></tr><tr><td>42</td><td>4.013V</td></tr><tr><td>…</td><td>13mV/STEP</td></tr><tr><td>50</td><td>4.117V</td></tr><tr><td>…</td><td>13mV/STEP</td></tr><tr><td>121</td><td>5.036V</td></tr><tr><td>...</td><td>26mV/STEP</td></tr><tr><td>127</td><td>5.192V</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="12">Inter command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h50</td></tr><tr><td>HW Reset</td><td>8’h50</td></tr></table></td></tr>
</table>

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6.3.10. VGH_SET(E8h)

<table>
<tr><td>E8h</td><td colspan="12">VGH_SET</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>E8</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td colspan="3">D2A_VGHS [2:0]</td><td>23</td></tr>
<tr><td>Description</td><td colspan="12">To have access to “E8h” , bit [0] of “B2h” need be set to 1

D2A_VGHS [2:0]
<table>
<tr><th>VGH_AD</th><th>VGH (V)</th><th>VGH _AD</th><th>VGH (V)</th></tr>
<tr><td>0</td><td>10</td><td>4</td><td>14</td></tr>
<tr><td>1</td><td>11</td><td>5</td><td>15</td></tr>
<tr><td>2</td><td>12</td><td>6</td><td>Reserved</td></tr>
<tr><td>3</td><td>13</td><td>7</td><td>Reserved</td></tr>
</table></td></tr>
<tr><td>Restriction</td><td colspan="12">Inter command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>8’h23</td></tr>
<tr><td>HW Reset</td><td>8’h23</td></tr>
</table></td></tr>
</table>

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6.3.11. VGL_SET (E9h)

<table>
<tr><td>E9h</td><td colspan="12">VGL_SET</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>E9</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td colspan="3">D2A_VGLS [2:0]</td><td>43</td></tr>
<tr><td>Description</td><td colspan="12">To have access to “E9h” , bit [1] of “B2h” need be set to 1

D2A_VGLS [2:0]
<table><tr><th>VGL_AD</th><th>VGL (V)</th><th>VGL_AD</th><th>VGL (V)</th></tr><tr><td>0</td><td>-7.5</td><td>4</td><td>-10.5</td></tr><tr><td>1</td><td>-8.5</td><td>5</td><td>-11.0</td></tr><tr><td>2</td><td>-9.5</td><td>6</td><td>-12.0</td></tr><tr><td>3</td><td>-10.0</td><td>7</td><td>-13.0</td></tr></table></td></tr>
<tr><td>Restriction</td><td colspan="12">Inter command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>8’h43</td></tr><tr><td>HW Reset</td><td>8’h43</td></tr></table></td></tr>
</table>

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6.3.12. AVDD_VCL_SET (E2h)

<table>
<tr><td>E2h</td><td colspan="12">AVDD_SET</td></tr>
<tr><td></td><td>D/CX</td><td>RDX</td><td>WRX</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>E2</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>6D</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>6E</td></tr>
<tr><td>3rd Parameter</td><td>1</td><td>1</td><td>↑</td><td>0</td><td colspan="3">AVDD_AD [2:0]</td><td>0</td><td colspan="3">VCL_AD [2:0]</td><td>45</td></tr>
<tr><td>Description</td><td colspan="12">
To have access to “E2h” , bit [2] of “B1h” need be set to 1
AVDD_AD[2:0]：
<table>
<tr><th>AVDD_AD</th><th>AVDD (V)</th><th>AVDD_AD</th><th>AVDD (V)</th></tr>
<tr><td>0</td><td>4.3</td><td>4</td><td>5.0</td></tr>
<tr><td>1</td><td>4.5</td><td>5</td><td>5.1</td></tr>
<tr><td>2</td><td>4.7</td><td>6</td><td>5.2</td></tr>
<tr><td>3</td><td>4.9</td><td>7</td><td>5.3</td></tr>
</table>
VCL_AD [2:0]：
<table>
<tr><th>VCL_AD</th><th>VCL(V)</th><th>VCL_AD</th><th>VCL(V)</th></tr>
<tr><td>0</td><td>-1.5</td><td>4</td><td>-1.9</td></tr>
<tr><td>1</td><td>-1.6</td><td>5</td><td>-2.0</td></tr>
<tr><td>2</td><td>-1.7</td><td>6</td><td>-2.1</td></tr>
<tr><td>3</td><td>-1.8</td><td>7</td><td>-2.2</td></tr>
</table>
</td></tr>
<tr><td>Restriction</td><td colspan="12">Inter command should be set high to enable this command</td></tr>
<tr><td>Register Availability</td><td colspan="12">
<table>
<tr><th>Status□</th><th>Availability</th></tr>
<tr><td>Normal Mode□On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>24’h6D6E45</td></tr>
<tr><td>HW Reset</td><td>24’h6D6E45</td></tr>
</table>
</td></tr>
</table>

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6.3.13. SET_GAMMA1 (F0h)

F1h	SET_GAMMA1											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	0	0	0	03
1st Parameter	1	1	↑	0	0	vr2_n[5:0]						2E
2nd Parameter	1	1	↑	0	vr20_n[6:0]							2C
3rd Parameter	1	1	↑	0	0	vr36_n[2:0]			vr27_n[2:0]			3F
4th Parameter	1	1	↑	0	vr43_n[6:0]							C8
5th Parameter	1	1	↑	vr50_n[3:0]				vr13_n[3:0]				14
6th Parameter	1	1	↑	0	0	vr61_n[5:0]						18
7th Parameter	1	1	↑	0	0	vr62_n[5:0]						60
8th Parameter	1	1	↑	j0_n[1:0]		j1_n[1:0]		vr0_n[3:0]				00
9th Parameter	1	1	↑	0	0	vr1_n[5:0]						08
10th Parameter	1	1	↑	0	0	0	vr4_n[4:0]					0D
11th Parameter	1	1	↑	0	0	0	vr6_n[4:0]					18
12th Parameter	1	1	↑	0	0	0	vr57_n[4:0]					14
13th Parameter	1	1	↑	0	0	0	vr59_n[4:0]					1F
14th Parameter	1	1	↑	0	0	0	vr63_n[4:0]					03
Description	***To have access to "F0h" , bit [0] of "B3h" need be set to 1*** Set the positive voltage to adjust the gamma characteristics of the TFT panel.											
Restriction	Inter_command should be set high to enable this command											

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Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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6.3.14. SET_GAMMA2 (F1h)

F1h	SET_GAMMA2											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	0	0	0	1	03
1st Parameter	1	1	↑	0	0	vr2_p[5:0]						2B
2nd Parameter	1	1	↑	0	vr20_p[6:0]							24
3rd Parameter	1	1	↑	0	0	vr36_p[2:0]		vr27_p[2:0]				41
4th Parameter	1	1	↑	0	vr43_p[6:0]							C5
5th Parameter	1	1	↑	vr50_p[3:0]				vr13_p[3:0]				13
6th Parameter	1	1	↑	0	0	vr61_p[5:0]						17
7th Parameter	1	1	↑	0	0	vr62_p[5:0]						A0
8th Parameter	1	1	↑	j0_p[1:0]		j1_p[1:0]		vr0_p[3:0]				01
9th Parameter	1	1	↑	0	0	vr1_p[5:0]						0B
10th Parameter	1	1	↑	0	0	0	vr4_p[4:0]					0C
11th Parameter	1	1	↑	0	0	0	vr6_p[4:0]					19
12th Parameter	1	1	↑	0	0	0	vr57_p[4:0]					16
13th Parameter	1	1	↑	0	0	0	vr59_p[4:0]					1F
14th Parameter	1	1	↑	0	0	0	vr63_p[4:0]					03
Description	***To have access to "F1h" , bit [1] of "B3h" need be set to 1*** Set the negetive voltage to adjust the gamma characteristics of the TFT panel.											
Restriction	Inter_command should be set high to enable this command											

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Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Partial Mode On, Idle Mode Off, Sleep Out	Yes
Partial Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

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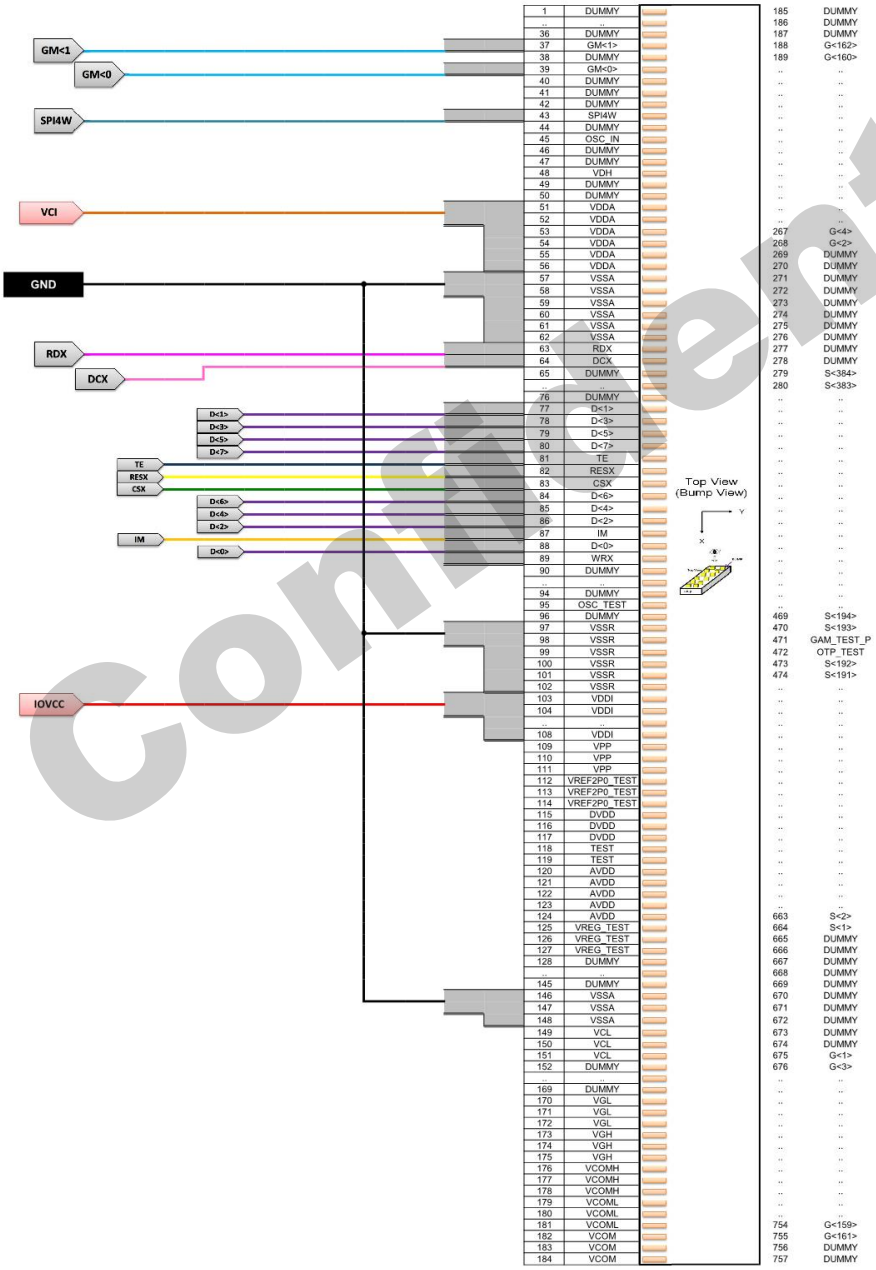
7. Application

7.1. APPLICATION CIRCUIT



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8. Electrical Characteristics

8.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When GC9107 is used out of the absolute maximum ratings, GC9107 may be permanently damaged. To use GC9107 within the following electrical characteristics limitation is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, GC9107 will malfunction and cause poor reliability.

Item	Symbol	Unit	Value
Supply voltage	VCI	V	-0.3~+4.6
Supply voltage(Logic)	IOVCC	V	-0.3~+4.6
Digital Operating voltage	VCORE	V	-0.3~+2.0
Driver supply voltage	VGH-VGL	V	17.5~+28.0
Logic input voltage range	VIN	V	-0.3~VDDI+0.3
Logic output voltage range	VO	V	-0.3~VDDI+0.3
Operation temperature	Topr	℃	-40~+80
Storage temperature	Tstg	℃	-55~+110

Note: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

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8.2. Power ON/OFF Sequence

IOVCC and VCI can be applied in any order.
VCI and IOVCC can be power down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down minimum

120msec after RESX has been released.

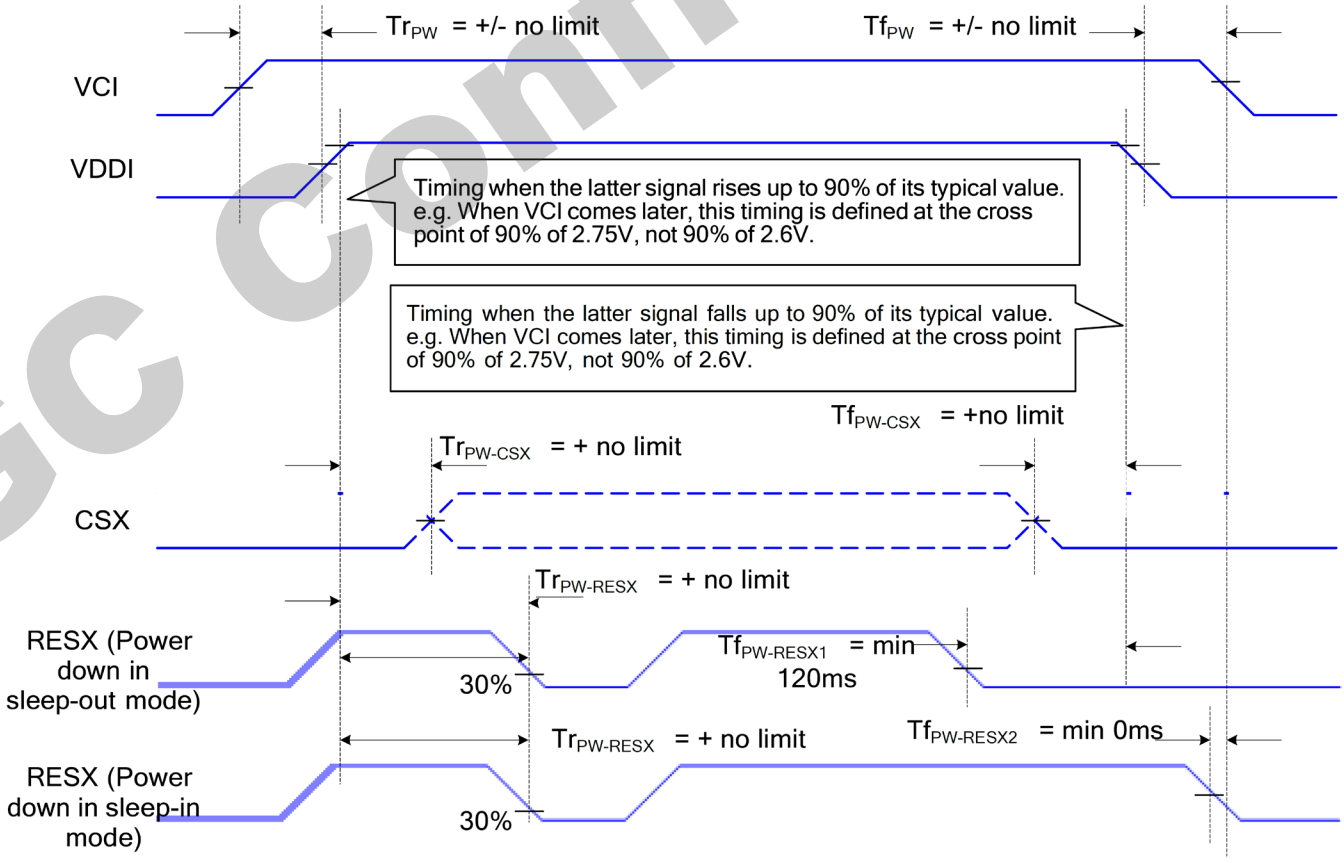
During power off, if LCD is in the Sleep In mode, IOVCC or VCI can be powered down minimum 0msec after RESX has been released.
CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Note 1: There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

Note 2: There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

Note 3: If RESX line is not held stable by host during Power On Sequence as defined in the sequence below, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

The power on/off sequence is illustrated below



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8.3. DC Characteristics

General DC Characteristics

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
Power and Operation Voltage							
Analog Operating Voltage	VCI	V	Operating voltage	2.5	2.8	3.3	Note2
Logic Operating Voltage	IOVCC	V	I/O supply voltage	1.65	2.8	3.3	Note2
Digital Operating voltage	VCORE	V	Digital supply voltage	-	1.8	-	Note2
Gate Driver High Voltage	VGH	V	-	10.0	-	15.0	Note3
Gate Driver Low Voltage	VGL	V	-	-13.0	-	-7.5	Note3
Driver Supply Voltage	-	V	|VGH-VGL|	17.5	-	28.0	Note3
Input and Output							
Logic High Level Input Voltage	VIH	V	-	0.7*VDDI	-	VDDI	Note1,2,3
Logic Low Level Input Voltage	VIL	V	-	VSS	-	0.3*VDDI	Note1,2,3
Logic High Level Output Voltage	VOH	V	IOL=-1.0mA	0.8*VDDI	-	VDDI	Note1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	VSSR	-	0.2*VDDI	Note1,2,3
Logic High Level Input Current	IIH	uA	-	-	-	1	Note1,2,3
Logic Low Level Input Current	IIL	uA	-	-1	-	-	Note1,2,3
Logic Input Leakage Current	ILEA	uA	VIN=VDDI or VSSR	-0.1	-	+0.1	Note1,2,3
Source Driver							
Gamma Reference Voltage	VREG	V	-	2.92	-	5.19	-

Note 1: VDDI=1.65 to 3.3V, VDD=2.5 to 3.3V, VSSA=VSSR=0V, Ta=-30 to 70 (to +85 no damage)℃

Note2: Please supply digital VDDI voltage equal or less than analog VDD voltage.

Note3 When the measurements are performed with LCD module. Measurement Points are like Note3.

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Note4 VDD=2.6V

Note5 VDD=3.3V

Note6 The Max. Value is between with Note 4 measure point and Gamma setting value

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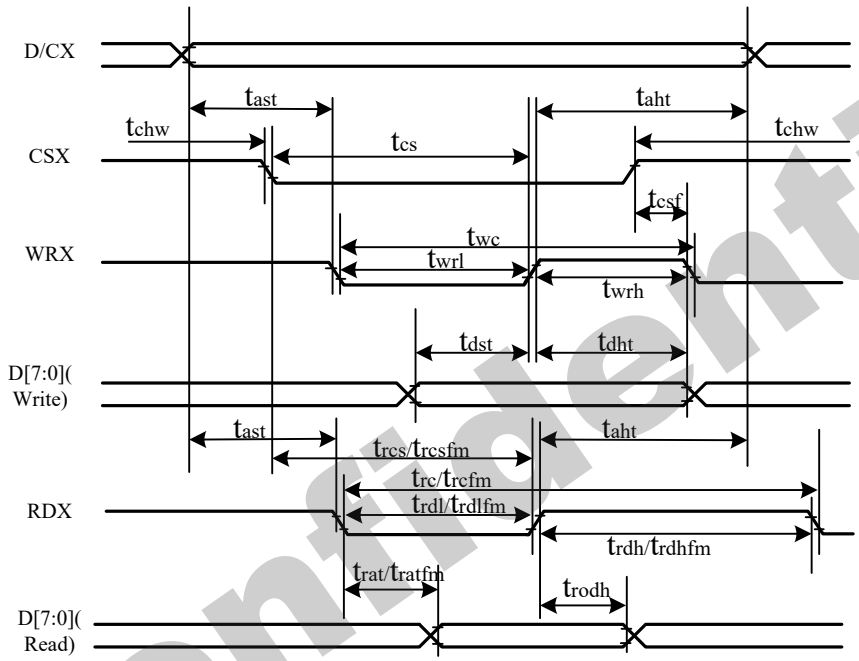
8.4. AC Characteristics

8.4.1. Display Parallel 8-bit Interface Timing Characteristics (8080)



Signal	Symbol	Parameter	min	max	Unit	Description
DCX	tast	Address setup time	0	-	ns	
	taht	Address hold time(Write/Read)	0	-	ns	
CSX	tchw	CSX "H" pulse width	0	-	ns	
	tcs	Chip Select setup time(Write)	15	-	ns	
	trcs	Chip Select setup time(Read ID)	45	-	ns	
	trcsfm	Chip Select setup time(Read FM)	355	-	ns	
	tcsf	Chip Select Wait time (Write/Read)	10	-	ns	
WRX	twc	Write Cycle	34	-	ns	
	twrh	Write Control pulse H duration	17	-	ns	
	twrl	Write Control pulse L duration	17	-	ns	
RDX(FM)	trcfm	Read Cycle (FM)	450	-	ns	
	trdhfm	Read Control H duration(FM)	90	-	ns	
	trdlfm	Read Control L duration(FM)	355	-	ns	

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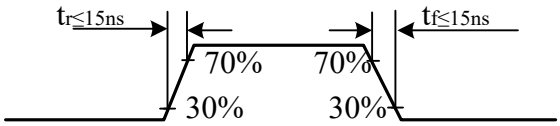
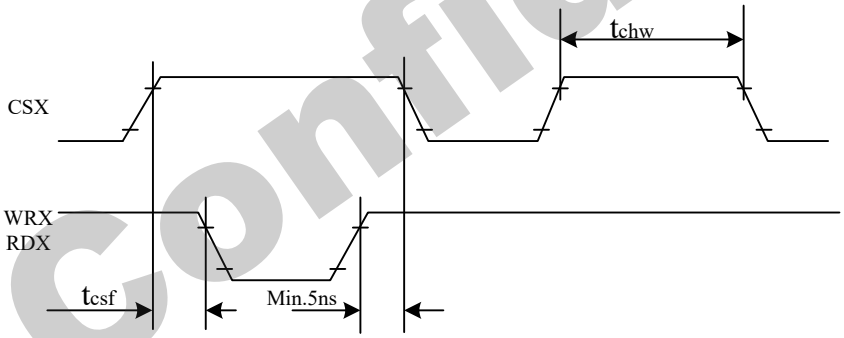
RDX(ID)	trc	Read Cycle (ID)	160	-	ns	
	trdh	Read Control H pulse duration	90	-	ns	
	trdl	Read Control L pulse duration	45	-	ns	
D[7:0]	tdst	Write data setup time	10	-	ns	For maximum CL=30pF For minimum CL=8pF
	tdht	Write data hold time	10	-	ns	
	trat	Read access time	-	40	ns	
	tratfm	Read access time	-	340	ns	
	trod	Read output disable time	20	80	ns	

Note: Ta = -30 to 70 °C, VDDI=1.65V to 3.3V, VDD=2.5V to 3.3V, VSSR=0V

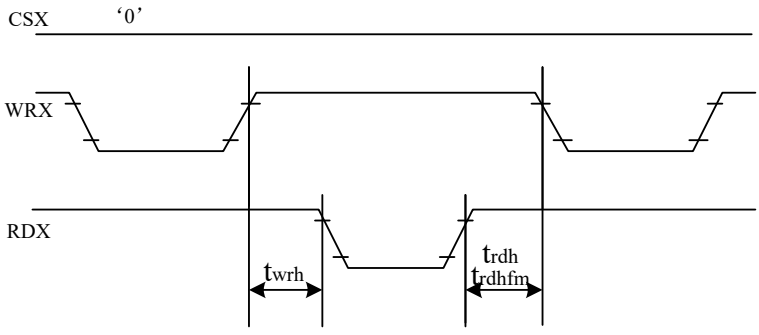


CSX timings :



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

Write to read or read to write timings:



Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

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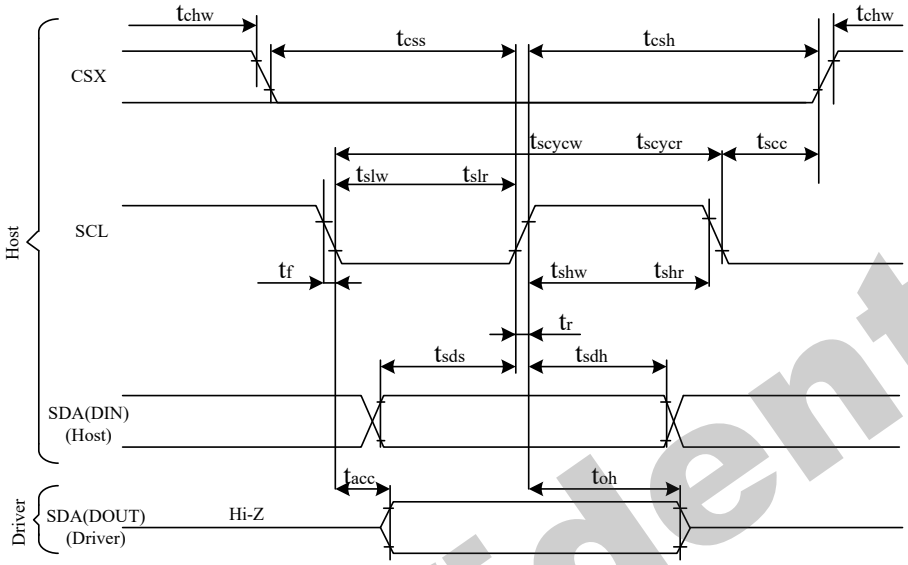
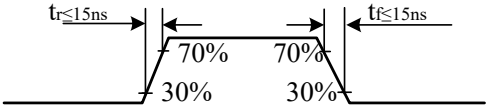
8.4.2. Display Serial Interface Timing Characteristics (3-line SPI system)



Signal	Symbol	Parameter	min	max	Unit	Description
SCL	tscycw	Serial Clock Cycle (Write)	10	-	ns	
	tshw	SCL "H" Pulse Width (Write)	5	-	ns	
	tslw	SCL "L" Pulse Width (Write)	5	-	ns	
	tscycr	Serial Clock Cycle (Read)	150	-	ns	
	tshr	SCL "H" Pulse Width (Read)	60	-	ns	
	tslr	SCL "L" Pulse Width (Read)	60	-	ns	
SDA/SDI (Input)	tsds	Data setup time (Write)	5	-	ns	
	tsdh	Data hold time (Write)	5	-	ns	
SDA/SD0 (Output)	tacc	Access time (Read)	10	-	ns	
	toh	Output disable time (Read)	10	50	ns	
CSX	tscc	SCL-CSX	10	-	ns	
	tchw	CSX "H" Pulse Width	20	-	ns	
	tcss	CSX-SCL Time	40	-	ns	
	tcsh		10	-	ns	

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VDD=2.5V to 3.3V, VSSA=VSSR=0V



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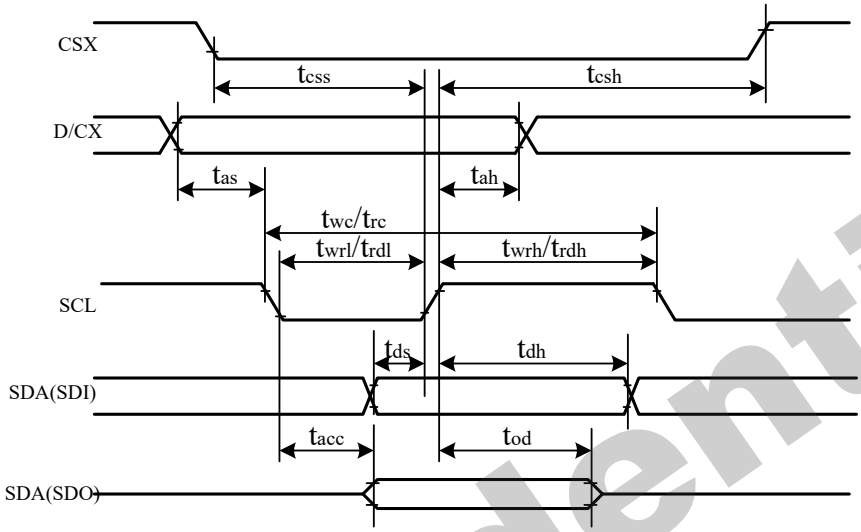
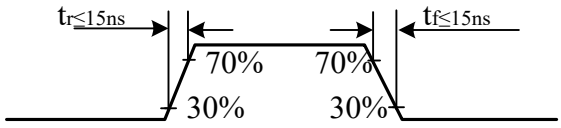
8.4.3. Display Serial Interface Timing Characteristics (4-line SPI system)



Signal	Symbol	Parameter	min	max	Unit	Description
CSX	tcss	Chip select time (Write)	20	-	ns	
	tcsh	Chip select hold time (Read)	40	-	ns	
SCL	twc	Serial Clock Cycle (Write)	10	-	ns	
	twrh	SCL "H" Pulse Width (Write)	5	-	ns	
	twrl	SCL "L" Pulse Width (Write)	5	-	ns	
	trc	Serial Clock Cycle (Read)	150	-	ns	
	trdh	SCL "H" Pulse Width (Read)	60	-	ns	
	trdl	SCL "L" Pulse Width (Read)	60	-	ns	
D/CX	tas	D/CX setup time	10	-	ns	
	tah	D/CX hold time (Write/Read)	10	-	ns	
SDA/SDI (Input)	tds	Data setup time (Write)	5	-	ns	
	tdh	Data hold time (Write)	5	-	ns	
SDA/SD0 (Output)	tacc	Access time (Read)	10	-	ns	For maximum CL=30pF For minmum CL=8pF
	toh	Output disable time (Read)	20	50	ns	

Note: Ta = 25 °C, VDDI=1.65V to 3.3V, VDD=2.5V to 3.3V, VSSA=VSSR=0V



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