

## NV3023A Datasheet

A-Si TFT LCD Single Chip Driver  
132RGBx162 Resolution and 262K color

Version 0.2  
Sep, 2020

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## Introduction

NV3023A is a 262,144-color one-chip SoC driver for a-TFT liquid crystal display with resolution of 132RGBx162 dots, comprising a 396-channel source driver, a 162-channel gate driver, 48,114 bytes GRAM for graphic data of 132RGBx162 dots, and power supply circuit.

The NV3023A supports 18-/16-/9-/8-bit data bus interface and serial peripheral interfaces (SPI). It also supplies 18-bit, 16-bit or 6-bit RGB interface for driving video signal directly from application controller. The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

NV3023A can operate with 1.65V I/O interface voltage, and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The NV3023A also supports a function to display in 8 colors idle mode, allowing for precise power control by software. So these features make the NV3023A an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP, on which long battery life is a major concern.

## 1. Features

- ◆ Display resolution options
  - 120(RGB) (H) X 160 (V)
  - 128(RGB) (H) X 128 (V)
  - 128(RGB) (H) X 160 (V)
  - 130(RGB) (H) X 130 (V)
  - 132(RGB) (H) X 132(V)
  - 132(RGB) (H) X 162 (V)
- ◆ LCD Driver Output Circuits
  - 396 source outputs
  - 162 gate outputs
  - Common electrode output
- ◆ AM-LCD driver with on-chip full display RAM: 34,749 bytes
- ◆ System Interfaces
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080-series MCU
  - 8-bits, 9-bits, 16-bits, 18-bits interface with 6800-series MCU
  - 6-bits, 16-bits, 18-bits RGB interface
  - 3-pin/4-pin serial interface
- ◆ Display color modes
  - Full color mode (idle mode off): 262K-colors
  - Reduced color modes (idle mode on): 8-colors
- ◆ On Chip Functions
  - VCOM generator and adjustment
  - Timing generator
  - Oscillator
  - DC/DC converter
  - Line/frame inversion
  - Factory default value (Maker ID, Version ID, Module ID, etc) are stored on the display module

- ◆ Low-Power Consumption
  - Low operating power supplies
    - IOVCC = 1.65V ~ 3.6 V (interface I/O)
    - VCI = 2.5V ~ 4.8 V (analog)
- ◆ LCD Voltage Drive
  - Source/VCOM power supply voltage
    - AVDD – VSS = 4.5V ~ 5.0V
    - VCL – VSS = -1.0V ~ -3.0V
    - VCI – VCL  $\leq$  5.0V
  - Gate driver output voltage
    - VGH – VSS = 10V ~ 16V
    - VGL – VSS = -6V ~ -12V
    - VGH – VGL  $\leq$  30V
  - VCOM driver output voltage
    - VCOMH = 3.1725V ~ 4.41V
    - VCOML = -0.36V ~ -1.8225V
- ◆ Operate Temperature Range: -30°C to 85°C

## 2. Pin Descriptions

Pin Name	I/O	Descriptions																																			
<b>Power Supply Pin</b>																																					
IOVCC	I	Power supply for interface logic circuits (1.65 ~ 3.6V)																																			
VCI	I	Power supply for analog circuit. Could connect to external power supply (VCI=2.5~4.8V).																																			
VSSA	I	System Ground for Analog System and Booster Circuit.																																			
VSS	I	System Ground for I/O System and Digital System.																																			
<b>Interface Logic Pin</b>																																					
P68	I	8080/6800 MCU Interface Mode Selection P68 = '1' : Select 6800-MCU parallel interface P68 = '0' : Select 8080-MCU parallel interface Note: If not used, please fix this pin at VSS level.																																			
IM2 IM1 IM0	I	MCU Parallel interface bus and Serial interface select : <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>IM2</th><th>IM1</th><th>IM0</th><th>SPI4W</th><th>Interface Type</th></tr> <tr> <td>1</td><td>0</td><td>0</td><td>X</td><td>MCU 8-bit Parallel</td></tr> <tr> <td>1</td><td>0</td><td>1</td><td>X</td><td>MCU 16-bit Parallel</td></tr> <tr> <td>1</td><td>1</td><td>0</td><td>X</td><td>MCU 9-bit Parallel</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>X</td><td>MCU 18-bit Parallel</td></tr> <tr> <td>0</td><td>X</td><td>X</td><td>1</td><td>SPI 4 Wire Serial</td></tr> <tr> <td>0</td><td>X</td><td>X</td><td>0</td><td>SPI 3 Wire Serial(or 2 Data Line SPI)</td></tr> </table>	IM2	IM1	IM0	SPI4W	Interface Type	1	0	0	X	MCU 8-bit Parallel	1	0	1	X	MCU 16-bit Parallel	1	1	0	X	MCU 9-bit Parallel	1	1	1	X	MCU 18-bit Parallel	0	X	X	1	SPI 4 Wire Serial	0	X	X	0	SPI 3 Wire Serial(or 2 Data Line SPI)
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1	1	1	X	MCU 18-bit Parallel																																	
0	X	X	1	SPI 4 Wire Serial																																	
0	X	X	0	SPI 3 Wire Serial(or 2 Data Line SPI)																																	
SPI4W		SPI4W='0', 3-line SPI or 2 Data Line SPI Enable. SPI4W='1', 4-line SPI Enable. If Not Used, Please fix this Pin at VSS Level.																																			
RESX	I	Chip Reset Pin ("Low Active") Note: Keep this pin without glitch																																			
CSX	I	Chip Select Pin ("Low Active") Pull down when chip accessable																																			
DCX	I	Reuse Pin according parallel and serial interface: <ul style="list-style-type: none"> <li>➤ MCU Interface: Distinguish Data ('1') or Command ('0').</li> <li>➤ SPI Interface: Used as 'SCL' clock pin.</li> </ul> If not used, please connect this pin to VSS.																																			
RDX	I	<ul style="list-style-type: none"> <li>➤ 8080-parallel interface: used as 'Read' enable.</li> <li>➤ 6800-parallel interface: <ol style="list-style-type: none"> <li>1. when WRX='0', RDX used as 'write' enable;</li> <li>2. When WRX='1', RDX used as 'Read' enable.</li> </ol> </li> </ul>																																			
WRX	I	<ul style="list-style-type: none"> <li>➤ 8080-parallel interface, used as write enable.</li> <li>➤ 6800-parallel interface, used to distinguish 'write' or 'read' operation.</li> <li>➤ SPI 4-wire interface, used as D/CX.</li> <li>➤ 2 Data Line SPI as RS;</li> </ul>																																			

Pin Name	I/O	Descriptions																												
D[17:0]	I/O	<ul style="list-style-type: none"> <li>➤ SPI without RGB interface : D[0] used as SDI/O, others don't care;</li> <li>➤ SPI with RGB interface : D[17:0] used as data bus;</li> <li>➤ MCU interface : D[17:0] used as data bus;</li> </ul> <p>Note : When RGB interface enable , SPI should use 'SDA' pin as SDI/O</p>																												
TE	O	Tearing effect output pin to synchronize MCU to frame writing																												
TEST12/SDA	I/O	When RCM[1]='1',SDA is used for SPI write/read data line; When RCM[0]='0',SDA is not used;																												
RCM[0]	I	"RCM0" has no function, dont use.																												
RCM[1]	I	"RCM1" internal with pull low , pull high will enable RGB interface.																												
TEST8/PCLK	I	RGB interface pixel clock signal																												
TEST10/HS	I	RGB interface horizontal synchronization signal																												
TEST11/VS	I	RGB interface vertical synchronization signal																												
TEST9/DE	I	RGB interface data enable signal																												
OSC	O	OSC waveform output pin, for test purpose.																												
Mode Selection Pin																														
GM2 GM1 GM0	I	GM2 internal with pulllow function.if no used, please floating it. GM1、GM0 internal with pullhigh function.if no used, please floating it. Panel Resolution Selection Pins. <table border="1" style="margin-top: 5px;"> <thead> <tr> <th>GM2</th><th>GM1</th><th>GM0</th><th>Descriptions</th></tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>132RGBX162(S1~396 and G1~G162 output)</td></tr> <tr><td>0</td><td>0</td><td>1</td><td>128RGBX128(S7~390 and G2~G129 output)</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>120RGBX160(S7~366 and G2~G161 output)</td></tr> <tr><td>0</td><td>1</td><td>1</td><td>128RGBX160(S7~390 and G2~G161 output)</td></tr> <tr><td>1</td><td>0</td><td>0</td><td>130RGBX130(S7~396 and G2~G131 output)</td></tr> <tr><td>1</td><td>0</td><td>1</td><td>132RGBX132(S1~396 and G2~G133 output)</td></tr> </tbody> </table>	GM2	GM1	GM0	Descriptions	0	0	0	132RGBX162(S1~396 and G1~G162 output)	0	0	1	128RGBX128(S7~390 and G2~G129 output)	0	1	0	120RGBX160(S7~366 and G2~G161 output)	0	1	1	128RGBX160(S7~390 and G2~G161 output)	1	0	0	130RGBX130(S7~396 and G2~G131 output)	1	0	1	132RGBX132(S1~396 and G2~G133 output)
GM2	GM1	GM0	Descriptions																											
0	0	0	132RGBX162(S1~396 and G1~G162 output)																											
0	0	1	128RGBX128(S7~390 and G2~G129 output)																											
0	1	0	120RGBX160(S7~366 and G2~G161 output)																											
0	1	1	128RGBX160(S7~390 and G2~G161 output)																											
1	0	0	130RGBX130(S7~396 and G2~G131 output)																											
1	0	1	132RGBX132(S1~396 and G2~G133 output)																											
VPP	I	When writing NVM, it needs external power supply voltage (7.5V).																												
Driver Output pins																														
S1~S396	O	Source driver output pins.																												
G1~G162	O	Gate driver output pins.																												
VDD	O	Test pin for internal digital logic Power supply																												
GVDD	O	A power supply for Grayscale Voltage Generator																												
DDVDH	O	A power supply pin for source driver block that is generated from power block. Output of booster 1 circuit (output of 2-times output of VCI).																												
VCL	O	A power supply pin for generating VCOML																												
VGH	O	Power supply for Gate Driver																												
VGL	O	Negative power supply for Gate Driver																												
VCOMH	O	The high level of VCOM AC voltage.																												
VCOML	O	The low level of VCOM AC voltage.																												
VCOM	O	TFT display common electrode power supply. Alternates between voltage levels between VCOMH-VCOML. Registers set the alternating cycle for operating or halting VCOM.																												
TEST_C<3:0>	O	Digital function test outputs, it is not accessible to user.must be open.																												
TESTOP[8:1]	O	Analog function test outputs, it is not accessible to user.must be open.																												
SMX SMY		Dummy pin.if no used, please floating it.																												
DDVDHAC	O	Internal charge pump output voltage, default value is 5V.																												

## NV3023A—132RGB x162 dot, 262k-color TFT LCD Single-Chip Driver

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Pin Name	I/O	Descriptions
TVBG、T1UA		Internal analog reference test pin, normal output is Hiz state, if no used, please floating it.

### 3. Bump Arrangement and Coordination

### 3.1. Bump Arrangement

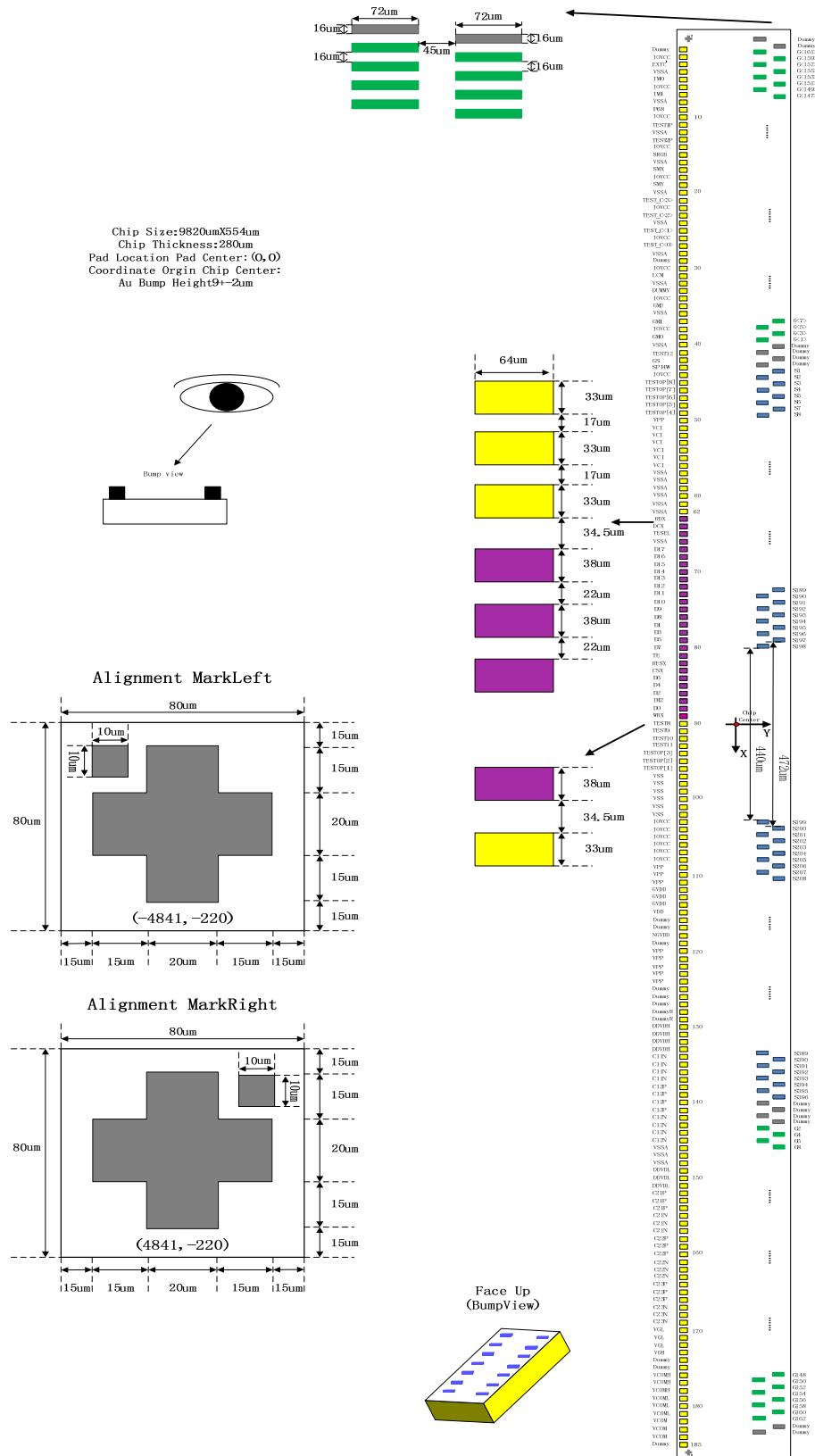


Figure 3-1 Pad Arrangement

### 3.2. Pin Connection

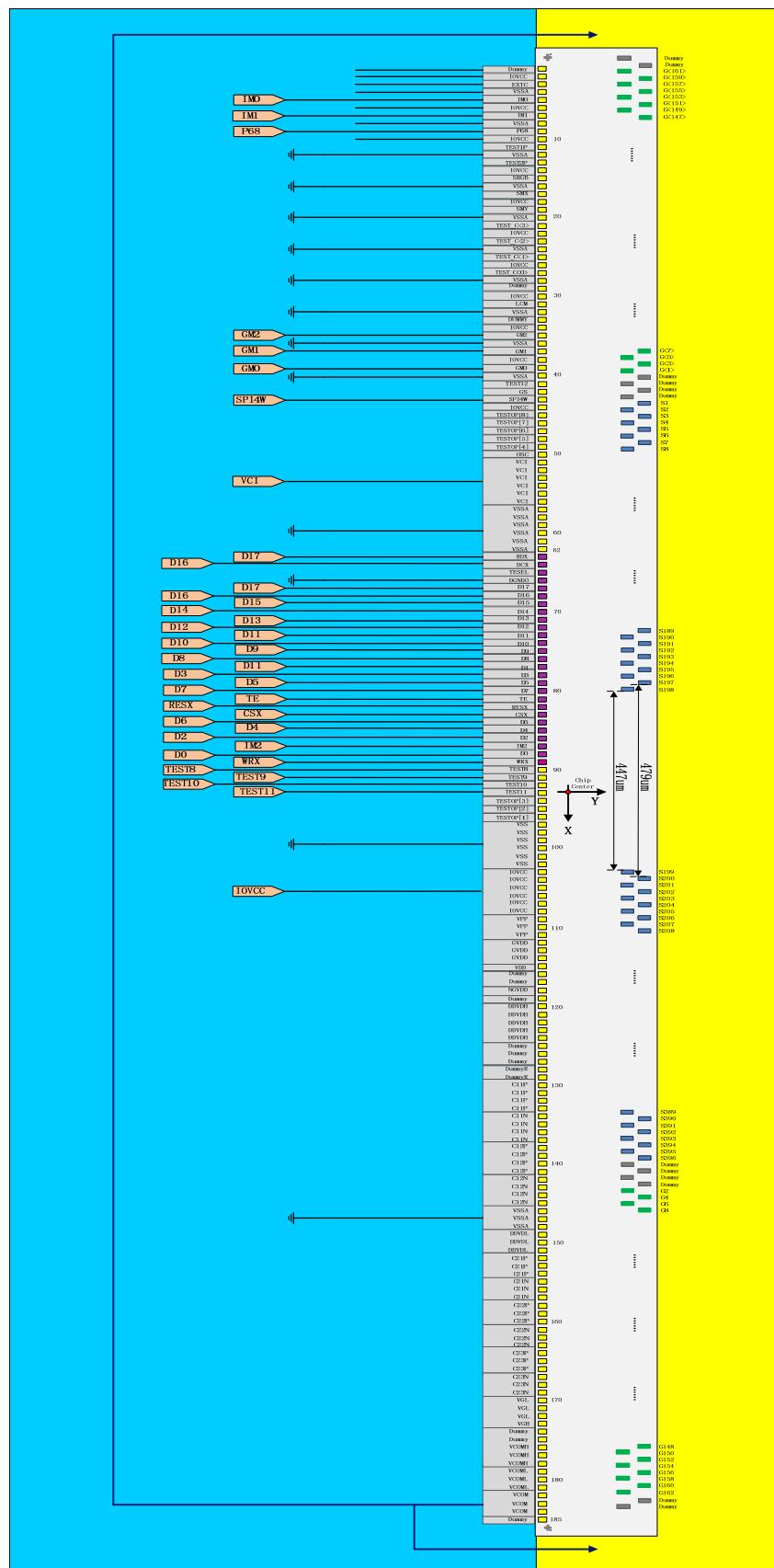


Figure 3-2 Pad Connection

### 3.3. Pad Coordination

No.	PAD Name	X	Y								
1	DUMMY	-4750	-231	72	D12	-1090	-231	144	DDVDHAC	2700	-231
2	IOVCC	-4700	-231	73	D11	-1030	-231	145	DDVDHAC	2750	-231
3	EXTC	-4650	-231	74	D10	-970	-231	146	AGND	2800	-231
4	GND	-4600	-231	75	D9	-910	-231	147	AGND	2850	-231
5	IM0	-4550	-231	76	D8	-850	-231	148	AGND	2900	-231
6	IOVCC	-4500	-231	77	D1	-790	-231	149	TVBG	2950	-231
7	IM1	-4450	-231	78	D3	-730	-231	150	TVBG	3000	-231
8	GND	-4400	-231	79	D5	-670	-231	151	TVBG	3050	-231
9	P68	-4350	-231	80	D7	-610	-231	152	T1UA	3100	-231
10	IOVCC	-4300	-231	81	TE	-550	-231	153	T1UA	3150	-231
11	RCM<0>	-4250	-231	82	RESX	-490	-231	154	T1UA	3200	-231
12	GND	-4200	-231	83	CSX	-430	-231	155	GVDD	3250	-231
13	RCM<1>	-4150	-231	84	D6	-370	-231	156	GVDD	3300	-231
14	IOVCC	-4100	-231	85	D4	-310	-231	157	GVDD	3350	-231
15	SRGB	-4050	-231	86	D2	-250	-231	158	C22P	3400	-231
16	GND	-4000	-231	87	IM2	-190	-231	159	C22P	3450	-231
17	SMX	-3950	-231	88	D0	-130	-231	160	C22P	3500	-231
18	IOVCC	-3900	-231	89	WRX	-70	-231	161	C22N	3550	-231
19	SMY	-3850	-231	90	TEST8	0	-231	162	C22N	3600	-231
20	GND	-3800	-231	91	TEST9	50	-231	163	C22N	3650	-231
21	TEST_C<3>	-3750	-231	92	TEST10	100	-231	164	DDVDL	3700	-231
22	IOVCC	-3700	-231	93	TEST11	150	-231	165	DDVDL	3750	-231
23	TEST_C<2>	-3650	-231	94	TESTOP[3]	200	-231	166	DDVDL	3800	-231
24	GND	-3600	-231	95	TESTOP[2]	250	-231	167	VCL	3850	-231
25	TEST_C<1>	-3550	-231	96	TESTOP[1]	300	-231	168	VCL	3900	-231
26	IOVCC	-3500	-231	97	GND	350	-231	169	VCL	3950	-231
27	TEST_C<0>	-3450	-231	98	GND	400	-231	170	VGL	4000	-231
28	GND	-3400	-231	99	GND	450	-231	171	VGL	4050	-231
29	DUMMY	-3350	-231	100	GND	500	-231	172	VGL	4100	-231
30	IOVCC	-3300	-231	101	GND	550	-231	173	VGH	4150	-231
31	LCM	-3250	-231	102	GND	600	-231	174	DUMMY	4200	-231
32	GND	-3200	-231	103	IOVCC	650	-231	175	DUMMY	4250	-231
33	DUMMY	-3150	-231	104	IOVCC	700	-231	176	VCOMH	4300	-231
34	IOVCC	-3100	-231	105	IOVCC	750	-231	177	VCOMH	4350	-231
35	GM2	-3050	-231	106	IOVCC	800	-231	178	VCQMH	4400	-231
36	GND	-3000	-231	107	IOVCC	850	-231	179	VCOML	4450	-231
37	GM1	-2950	-231	108	IOVCC	900	-231	180	VCOML	4500	-231
38	IOVCC	-2900	-231	109	VPP	950	-231	181	VCOML	4550	-231
39	GM0	-2850	-231	110	VPP	1000	-231	182	VCOM	4600	-231
40	GND	-2800	-231	111	VPP	1050	-231	183	VCOM	4650	-231
41	TEST12	-2750	-231	112	DUMMY	1100	-231	184	VCOM	4700	-231
42	GS	-2700	-231	113	DUMMY	1150	-231	185	DUMMY	4750	-231
43	SPI4W	-2650	-231	114	DUMMY	1200	-231	186	DUMMY	4772	112.5
44	IOVCC	-2600	-231	115	VDD	1250	-231	187	DUMMY	4756	224.5
45	TESTOP[8]	-2550	-231	116	DUMMY	1300	-231	188	G162	4740	112.5
46	TESTOP[7]	-2500	-231	117	DUMMY	1350	-231	189	G160	4724	224.5
47	TESTOP[6]	-2450	-231	118	DUMMY	1400	-231	190	G158	4708	112.5
48	TESTOP[5]	-2400	-231	119	DUMMY	1450	-231	191	G156	4692	224.5
49	TESTOP[4]	-2350	-231	120	VPP	1500	-231	192	G154	4676	112.5
50	VPP	-2300	-231	121	VPP	1550	-231	193	G152	4660	224.5
51	VCI	-2250	-231	122	VPP	1600	-231	194	G150	4644	112.5
52	VCI	-2200	-231	123	VPP	1650	-231	195	G148	4628	224.5
53	VCI	-2150	-231	124	VPP	1700	-231	196	G146	4612	112.5
54	VCI	-2100	-231	125	DUMMY	1750	-231	197	G144	4596	224.5
55	VCI	-2050	-231	126	DUMMY	1800	-231	198	G142	4580	112.5
56	VCI	-2000	-231	127	DUMMY	1850	-231	199	G140	4564	224.5
57	AGND	-1950	-231	128	DummyR	1900	-231	200	G138	4548	112.5
58	AGND	-1900	-231	129	DummyR	1950	-231	201	G136	4532	224.5
59	AGND	-1850	-231	130	C11P	2000	-231	202	G134	4516	112.5
60	AGND	-1800	-231	131	C11P	2050	-231	203	G132	4500	224.5
61	AGND	-1750	-231	132	C11P	2100	-231	204	G130	4484	112.5
62	AGND	-1700	-231	133	C11P	2150	-231	205	G128	4468	224.5
63	RDX	-1630	-231	134	C11N	2200	-231	206	G126	4452	112.5
64	DCX	-1570	-231	135	C11N	2250	-231	207	G124	4436	224.5
65	TESEL	-1510	-231	136	C11N	2300	-231	208	G122	4420	112.5
66	GND	-1450	-231	137	C11N	2350	-231	209	G120	4404	224.5
67	D17	-1390	-231	138	C12P	2400	-231	210	G118	4388	112.5
68	D16	-1330	-231	139	C12P	2450	-231	211	G116	4372	224.5
69	D15	-1270	-231	140	C12P	2500	-231	212	G114	4356	112.5
70	D14	-1210	-231	141	C12P	2550	-231	213	G112	4340	224.5
71	D13	-1150	-231	142	DDVDHAC	2600	-231	214	G110	4324	112.5
				143	DDVDHAC	2650	-231	215	G108	4308	224.5

## NV3023A—132RGB x162 dot, 262k-color TFT LCD Single-Chip Driver

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216	G106	4292	112.5
217	G104	4276	224.5
218	G102	4260	112.5
219	G100	4244	224.5
220	G98	4228	112.5
221	G96	4212	224.5
222	G94	4196	112.5
223	G92	4180	224.5
224	G90	4164	112.5
225	G88	4148	224.5
226	G86	4132	112.5
227	G84	4116	224.5
228	G82	4100	112.5
229	G80	4084	224.5
230	G78	4068	112.5
231	G76	4052	224.5
232	G74	4036	112.5
233	G72	4020	224.5
234	G70	4004	112.5
235	G68	3988	224.5
236	G66	3972	112.5
237	G64	3956	224.5
238	G62	3940	112.5
239	G60	3924	224.5
240	G58	3908	112.5
241	G56	3892	224.5
242	G54	3876	112.5
243	G52	3860	224.5
244	G50	3844	112.5
245	G48	3828	224.5
246	G46	3812	112.5
247	G44	3796	224.5
248	G42	3780	112.5
249	G40	3764	224.5
250	G38	3748	112.5
251	G36	3732	224.5
252	G34	3716	112.5
253	G32	3700	224.5
254	G30	3684	112.5
255	G28	3668	224.5
256	G26	3652	112.5
257	G24	3636	224.5
258	G22	3620	112.5
259	G20	3604	224.5
260	G18	3588	112.5
261	G16	3572	224.5
262	G14	3556	112.5
263	G12	3540	224.5
264	G10	3524	112.5
265	G8	3508	224.5
266	G6	3492	112.5
267	G4	3476	224.5
268	G2	3460	112.5
269	DUMMY	3444	224.5
270	DUMMY	3428	112.5
271	DUMMY	3412	224.5
272	DUMMY	3396	112.5
273	S396	3380	224.5
274	S395	3364	112.5
275	S394	3348	224.5
276	S393	3332	112.5
277	S392	3316	224.5
278	S391	3300	112.5
279	S390	3284	224.5
280	S389	3268	112.5
281	S388	3252	224.5
282	S387	3236	112.5
283	S386	3220	224.5
284	S385	3204	112.5
285	S384	3188	224.5
286	S383	3172	112.5
287	S382	3156	224.5
288	S381	3140	112.5
289	S380	3124	224.5
290	S379	3108	112.5
291	S378	3092	224.5

292	S377	3076	112.5
293	S376	3060	224.5
294	S375	3044	112.5
295	S374	3028	224.5
296	S373	3012	112.5
297	S372	2996	224.5
298	S371	2980	112.5
299	S370	2964	224.5
300	S369	2948	112.5
301	S368	2932	224.5
302	S367	2916	112.5
303	S366	2900	224.5
304	S365	2884	112.5
305	S364	2868	224.5
306	S363	2852	112.5
307	S362	2836	224.5
308	S361	2820	112.5
309	S360	2804	224.5
310	S359	2788	112.5
311	S358	2772	224.5
312	S357	2756	112.5
313	S356	2740	224.5
314	S355	2724	112.5
315	S354	2708	224.5
316	S353	2692	112.5
317	S352	2676	224.5
318	S351	2660	112.5
319	S350	2644	224.5
320	S349	2628	112.5
321	S348	2612	224.5
322	S347	2596	112.5
323	S346	2580	224.5
324	S345	2564	112.5
325	S344	2548	224.5
326	S343	2532	112.5
327	S342	2516	224.5
328	S341	2500	112.5
329	S340	2484	224.5
330	S339	2468	112.5
331	S338	2452	224.5
332	S337	2436	112.5
333	S336	2420	224.5
334	S335	2404	112.5
335	S334	2388	224.5
336	S333	2372	112.5
337	S332	2356	224.5
338	S331	2340	112.5
339	S330	2324	224.5
340	S329	2308	112.5
341	S328	2292	224.5
342	S327	2276	112.5
343	S326	2260	224.5
344	S325	2244	112.5
345	S324	2228	224.5
346	S323	2212	112.5
347	S322	2196	224.5
348	S321	2180	112.5
349	S320	2164	224.5
350	S319	2148	112.5
351	S318	2132	224.5
352	S317	2116	112.5
353	S316	2100	224.5
354	S315	2084	112.5
355	S314	2068	224.5
356	S313	2052	112.5
357	S312	2036	224.5
358	S311	2020	112.5
359	S310	2004	224.5
360	S309	1988	112.5
361	S308	1972	224.5
362	S307	1956	112.5
363	S306	1940	224.5
364	S305	1924	112.5
365	S304	1908	224.5
366	S303	1892	112.5
367	S302	1876	224.5

368	S301	1860	112.5
369	S300	1844	224.5
370	S299	1828	112.5
371	S298	1812	224.5
372	S297	1796	112.5
373	S296	1780	224.5
374	S295	1764	112.5
375	S294	1748	224.5
376	S293	1732	112.5
377	S292	1716	224.5
378	S291	1700	112.5
379	S290	1684	224.5
380	S289	1668	112.5
381	S288	1652	224.5
382	S287	1636	112.5
383	S286	1620	224.5
384	S285	1604	112.5
385	S284	1588	224.5
386	S283	1572	112.5
387	S282	1556	224.5
388	S281	1540	112.5
389	S280	1524	224.5
390	S279	1508	112.5
391	S278	1492	224.5
392	S277	1476	112.5
393	S276	1460	224.5
394	S275	1444	112.5
395	S274	1428	224.5
396	S273	1412	112.5
397	S272	1396	224.5
398	S271	1380	112.5
399	S270	1364	224.5
400	S269	1348	112.5
401	S268	1332	224.5
402	S267	1316	112.5
403	S266	1300	224.5
404	S265	1284	112.5
405	S264	1268	224.5
406	S263	1252	112.5
407	S262	1236	224.5
408	S261	1220	112.5
409	S260	1204	224.5
410	S259	1188	112.5
411	S258	1172	224.5
412	S257	1156	112.5
413	S256	1140	224.5
414	S255	1124	112.5
415	S254	1108	224.5
416	S253	1092	112.5
417	S252	1076	224.5
418	S251	1060	112.5
419	S250	1044	224.5
420	S249	1028	112.5
421	S248	1012	224.5
422	S247	996	112.5
423	S246	980	224.5
424	S245	964	112.5
425	S244	948	224.5
426	S243	932	112.5
427	S242	916	224.5
428	S241	900	112.5
429	S240	884	224.5
430	S239	868	112.5
431	S238	852	224.5
432	S237	836	112.5
433	S236	820	224.5
434	S235	804	112.5
435	S234	788	224.5
436	S233	772	112.5
437	S232	756	224.5
438	S231	740	112.5
439	S230	724	224.5
440	S229	708	112.5
441	S228	692	224.5
442	S227	676	112.5
443	S226	660	224.5

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444	S225	644	112.5
445	S224	628	224.5
446	S223	612	112.5
447	S222	596	224.5
448	S221	580	112.5
449	S220	564	224.5
450	S219	548	112.5
451	S218	532	224.5
452	S217	516	112.5
453	S216	500	224.5
454	S215	484	112.5
455	S214	468	224.5
456	S213	452	112.5
457	S212	436	224.5
458	S211	420	112.5
459	S210	404	224.5
460	S209	388	112.5
461	S208	372	224.5
462	S207	356	112.5
463	S206	340	224.5
464	S205	324	112.5
465	S204	308	224.5
466	S203	292	112.5
467	S202	276	224.5
468	S201	260	112.5
469	S200	244	224.5
470	S199	228	112.5
471	S198	-228	112.5
472	S197	-244	224.5
473	S196	-260	112.5
474	S195	-276	224.5
475	S194	-292	112.5
476	S193	-308	224.5
477	S192	-324	112.5
478	S191	-340	224.5
479	S190	-356	112.5
480	S189	-372	224.5
481	S188	-388	112.5
482	S187	-404	224.5
483	S186	-420	112.5
484	S185	-436	224.5
485	S184	-452	112.5
486	S183	-468	224.5
487	S182	-484	112.5
488	S181	-500	224.5
489	S180	-516	112.5
490	S179	-532	224.5
491	S178	-548	112.5
492	S177	-564	224.5
493	S176	-580	112.5
494	S175	-596	224.5
495	S174	-612	112.5
496	S173	-628	224.5
497	S172	-644	112.5
498	S171	-660	224.5
499	S170	-676	112.5
500	S169	-692	224.5
501	S168	-708	112.5
502	S167	-724	224.5
503	S166	-740	112.5
504	S165	-756	224.5
505	S164	-772	112.5
506	S163	-788	224.5
507	S162	-804	112.5
508	S161	-820	224.5
509	S160	-836	112.5
510	S159	-852	224.5
511	S158	-868	112.5
512	S157	-884	224.5
513	S156	-900	112.5
514	S155	-916	224.5
515	S154	-932	112.5
516	S153	-948	224.5
517	S152	-964	112.5
518	S151	-980	224.5
519	S150	-996	112.5

520	S149	-1012	224.5
521	S148	-1028	112.5
522	S147	-1044	224.5
523	S146	-1060	112.5
524	S145	-1076	224.5
525	S144	-1092	112.5
526	S143	-1108	224.5
527	S142	-1124	112.5
528	S141	-1140	224.5
529	S140	-1156	112.5
530	S139	-1172	224.5
531	S138	-1188	112.5
532	S137	-1204	224.5
533	S136	-1220	112.5
534	S135	-1236	224.5
535	S134	-1252	112.5
536	S133	-1268	224.5
537	S132	-1284	112.5
538	S131	-1300	224.5
539	S130	-1316	112.5
540	S129	-1332	224.5
541	S128	-1348	112.5
542	S127	-1364	224.5
543	S126	-1380	112.5
544	S125	-1396	224.5
545	S124	-1412	112.5
546	S123	-1428	224.5
547	S122	-1444	112.5
548	S121	-1460	224.5
549	S120	-1476	112.5
550	S119	-1492	224.5
551	S118	-1508	112.5
552	S117	-1524	224.5
553	S116	-1540	112.5
554	S115	-1556	224.5
555	S114	-1572	112.5
556	S113	-1588	224.5
557	S112	-1604	112.5
558	S111	-1620	224.5
559	S110	-1636	112.5
560	S109	-1652	224.5
561	S108	-1668	112.5
562	S107	-1684	224.5
563	S106	-1700	112.5
564	S105	-1716	224.5
565	S104	-1732	112.5
566	S103	-1748	224.5
567	S102	-1764	112.5
568	S101	-1780	224.5
569	S100	-1796	112.5
570	S99	-1812	224.5
571	S98	-1828	112.5
572	S97	-1844	224.5
573	S96	-1860	112.5
574	S95	-1876	224.5
575	S94	-1892	112.5
576	S93	-1908	224.5
577	S92	-1924	112.5
578	S91	-1940	224.5
579	S90	-1956	112.5
580	S89	-1972	224.5
581	S88	-1988	112.5
582	S87	-2004	224.5
583	S86	-2020	112.5
584	S85	-2036	224.5
585	S84	-2052	112.5
586	S83	-2068	224.5
587	S82	-2084	112.5
588	S81	-2100	224.5
589	S80	-2116	112.5
590	S79	-2132	224.5
591	S78	-2148	112.5
592	S77	-2164	224.5
593	S76	-2180	112.5
594	S75	-2196	224.5
595	S74	-2212	112.5

596	S73	-2228	224.5
597	S72	-2244	112.5
598	S71	-2260	224.5
599	S70	-2276	112.5
600	S69	-2292	224.5
601	S68	-2308	112.5
602	S67	-2324	224.5
603	S66	-2340	112.5
604	S65	-2356	224.5
605	S64	-2372	112.5
606	S63	-2388	224.5
607	S62	-2404	112.5
608	S61	-2420	224.5
609	S60	-2436	112.5
610	S59	-2452	224.5
611	S58	-2468	112.5
612	S57	-2484	224.5
613	S56	-2500	112.5
614	S55	-2516	224.5
615	S54	-2532	112.5
616	S53	-2548	224.5
617	S52	-2564	112.5
618	S51	-2580	224.5
619	S50	-2596	112.5
620	S49	-2612	224.5
621	S48	-2628	112.5
622	S47	-2644	224.5
623	S46	-2660	112.5
624	S45	-2676	224.5
625	S44	-2692	112.5
626	S43	-2708	224.5
627	S42	-2724	112.5
628	S41	-2740	224.5
629	S40	-2756	112.5
630	S39	-2772	224.5
631	S38	-2788	112.5
632	S37	-2804	224.5
633	S36	-2820	112.5
634	S35	-2836	224.5
635	S34	-2852	112.5
636	S33	-2868	224.5
637	S32	-2884	112.5
638	S31	-2900	224.5
639	S30	-2916	112.5
640	S29	-2932	224.5
641	S28	-2948	112.5
642	S27	-2964	224.5
643	S26	-2980	112.5
644	S25	-2996	224.5
645	S24	-3012	112.5
646	S23	-3028	224.5
647	S22	-3044	112.5
648	S21	-3060	224.5
649	S20	-3076	112.5
650	S19	-3092	224.5
651	S18	-3108	112.5
652	S17	-3124	224.5
653	S16	-3140	112.5
654	S15	-3156	224.5
655	S14	-3172	112.5
656	S13	-3188	224.5
657	S12	-3204	112.5
658	S11	-3220	224.5
659	S10	-3236	112.5
660	S9	-3252	224.5
661	S8	-3268	112.5
662	S7	-3284	224.5
663	S6	-3300	112.5
664	S5	-3316	224.5
665	S4	-3332	112.5
666	S3	-3348	224.5
667	S2	-3364	112.5
668	S1	-3380	224.5
669	DUMMY	-3396	112.5
670	DUMMY	-3412	224.5
671	DUMMY	-3428	112.5

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672	DUMMY	-3444	224.5
673	G1	-3460	112.5
674	G3	-3476	224.5
675	G5	-3492	112.5
676	G7	-3508	224.5
677	G9	-3524	112.5
678	G11	-3540	224.5
679	G13	-3556	112.5
680	G15	-3572	224.5
681	G17	-3588	112.5
682	G19	-3604	224.5
683	G21	-3620	112.5
684	G23	-3636	224.5
685	G25	-3652	112.5
686	G27	-3668	224.5
687	G29	-3684	112.5
688	G31	-3700	224.5
689	G33	-3716	112.5
690	G35	-3732	224.5
691	G37	-3748	112.5
692	G39	-3764	224.5
693	G41	-3780	112.5
694	G43	-3796	224.5
695	G45	-3812	112.5
696	G47	-3828	224.5
697	G49	-3844	112.5
698	G51	-3860	224.5
699	G53	-3876	112.5
700	G55	-3892	224.5

701	G57	-3908	112.5
702	G59	-3924	224.5
703	G61	-3940	112.5
704	G63	-3956	224.5
705	G65	-3972	112.5
706	G67	-3988	224.5
707	G69	-4004	112.5
708	G71	-4020	224.5
709	G73	-4036	112.5
710	G75	-4052	224.5
711	G77	-4068	112.5
712	G79	-4084	224.5
713	G81	-4100	112.5
714	G83	-4116	224.5
715	G85	-4132	112.5
716	G87	-4148	224.5
717	G89	-4164	112.5
718	G91	-4180	224.5
719	G93	-4196	112.5
720	G95	-4212	224.5
721	G97	-4228	112.5
722	G99	-4244	224.5
723	G101	-4260	112.5
724	G103	-4276	224.5
725	G105	-4292	112.5
726	G107	-4308	224.5
727	G109	-4324	112.5
728	G111	-4340	224.5
729	G113	-4356	112.5

730	G115	-4372	224.5
731	G117	-4388	112.5
732	G119	-4404	224.5
733	G121	-4420	112.5
734	G123	-4436	224.5
735	G125	-4452	112.5
736	G127	-4468	224.5
737	G129	-4484	112.5
738	G131	-4500	224.5
739	G133	-4516	112.5
740	G135	-4532	224.5
741	G137	-4548	112.5
742	G139	-4564	224.5
743	G141	-4580	112.5
744	G143	-4596	224.5
745	G145	-4612	112.5
746	G147	-4628	224.5
747	G149	-4644	112.5
748	G151	-4660	224.5
749	G153	-4676	112.5
750	G155	-4692	224.5
751	G157	-4708	112.5
752	G159	-4724	224.5
753	G161	-4740	112.5
754	DUMMY	-4756	224.5
755	DUMMY	-4772	112.5

## 4. Interface Description

### 4.1. Interface Type Selection

The selection of a given interfaces are done by setting P68, IM2, IM1, and IM0 pins as show in below tables.

Table 4-1 Interface Type Selection

P68	IM2	IM1	IM0	Interface	Read Back Selection
X	0	X	X	Serial interface	Via the read instruction ( 8-bit , 24-bit and 32-bit read parameter)
0	1	0	0	8080 MCU 8-bit Parallel	RDX strobe ( 8-bit read data and 8-bit read parameter)
0	1	0	1	8080 MCU 16-bit Parallel	RDX strobe (16-bit read data and 8-bit read parameter)
0	1	1	0	8080 MCU 9-bit Parallel	RDX strobe (9-bit read data and 8-bit read parameter)
0	1	1	1	8080 MCU 18-bit Parallel	RDX strobe (18-bit read data and 8-bit read parameter)
1	1	0	0	6800 MCU 8-bit Parallel	RDX strobe (8-bit read data and 8-bit read parameter)
1	1	0	1	6800 MCU 16-bit Parallel	RDX strobe (9-bit read data and 8-bit read parameter)
1	1	1	0	6800 MCU 9-bit Parallel	RDX strobe (16-bit read data and 8-bit read parameter)
1	1	1	1	6800 MCU 18-bit Parallel	RDX strobe (18-bit read data and 8-bit read parameter)

### 4.2. Serial Interface

The Module uses a 3-wire 9-bit serial interface or 4-pins/8-bit bi-directional interface for communication between the micro controller and the LCD driver chip. The 3-pins serial use: CSX (chip enable), SCL (serial clock) and SDA (serial data input/output) and the 4-pins serial use: CSX (chip enable), D/CX (data/ command select), SCL (serial clock), and SDA (serial data input/output).

Table 4-2 Serial Interface Type Selection

IM2	4WSPI	Interface	Read back selection
0	0	3-Pins Serial Interface(or 2 Data Line SPI)	Via the read instruction ( 8-bit , 24-bit and 32-bit read parameter)
0	1	4-Pins Serial Interface	Via the read instruction (8-bit , 24-bit and 32-bit read parameter)

### 4.2.1 Command/Data Write

The write mode of the interface means the micro controller writes commands and data to the LCD driver. 3-pins serial data packet contains a control bit D/CX and a transmission byte, but in 4-pins serial case, data packet contains just transmission byte and control bit D/CX is transferred by the D/CX pin. If D/CX is “low”, the transmission byte is interpreted as a command byte. If D/CX is “high”, the transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.

Any instruction can be sent in any orders to the Driver. The MSB is transmitted first. The serial interface is initialized when CSX is high status. In this state, SCL clock pulse or SDA data have no effect. A falling edge on CSX enables the serial interface and indicated the start of data transmission.

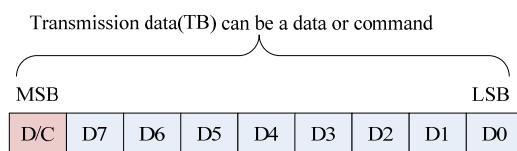


Figure 4-2-1-1 SPI 3-Wire Write Data Format

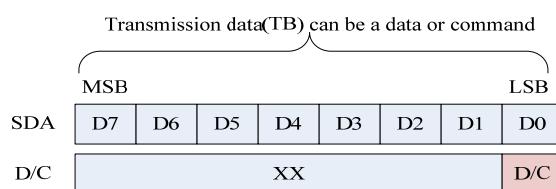


Figure 4-2-1-2 SPI 4-Wire Write Data Format

When CSX is “high”, SCL clock is ignored. At the falling edge of CSX, SCL can be high or low. SDA is sampled at the rising edge of SCL. D/CX indicates, whether the byte is command code (D/CX=’0’) or parameter/RAM data (D/CX=’1’). If CSX stays low after the last bit of command/data byte, the serial interface expects the D/CX bit (3-pin serial interface) or D7 (4-pins serial interface) of the next byte at the next rising edge of SCL.

#### 4.2.2 Command/Data Read

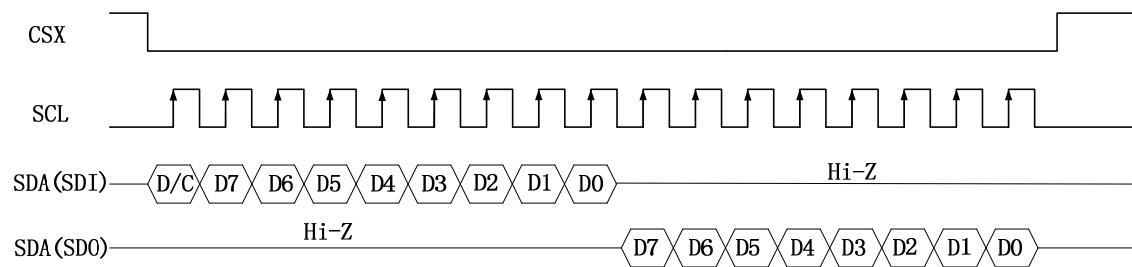


Figure 4-2-2-1 SPI 3-Wire 8-bit Read Operation  
(For ‘DAH/DBH/DCH/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh’ Command)

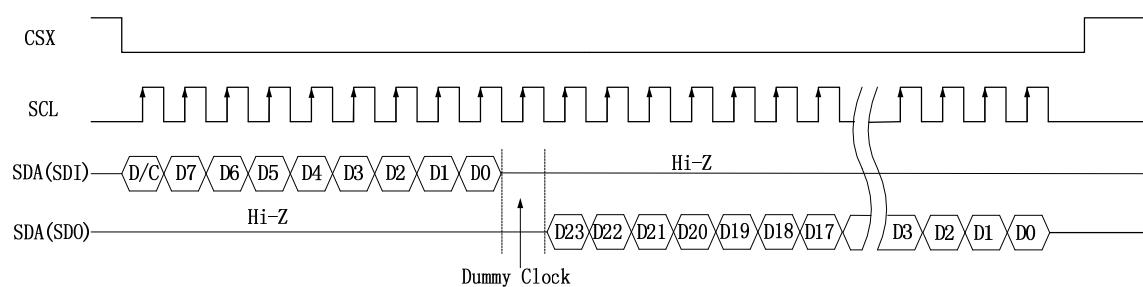


Figure 4-2-2-2 SPI 3-Wire 24-bit Read Operation  
(For ‘04H’ Command with one dummy clock)

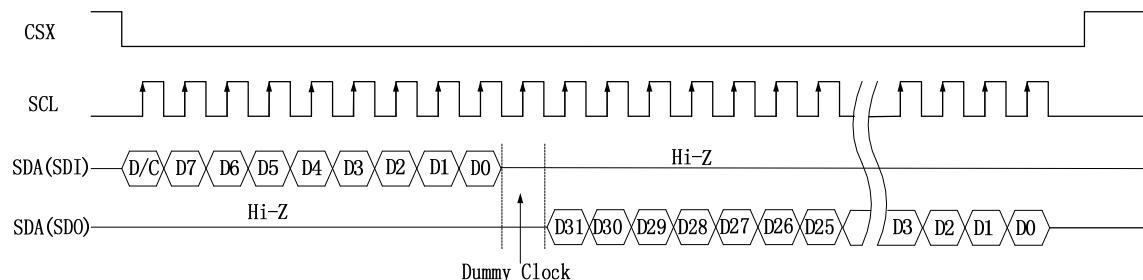


Figure 4-2-2-3 SPI 3-Wire 32-bit Read Operation  
(For ‘09H’ Command with one dummy clock)

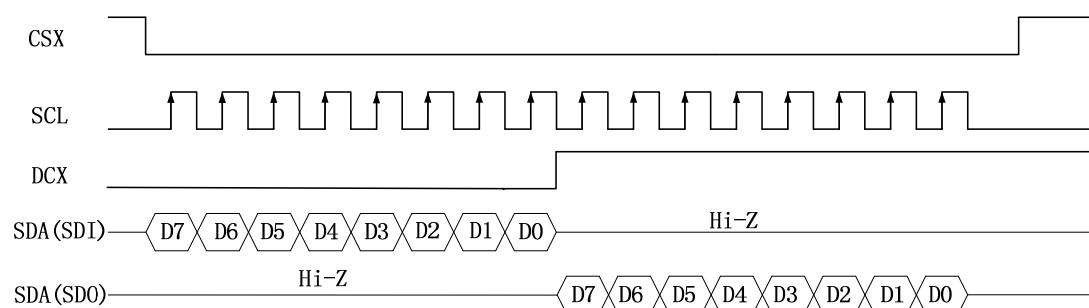


Figure 4-2-2-4 SPI 4-Wire 8-bit Read Operation  
(For ‘DAH/DBH/DCH/0Ah/0Bh/0Ch/0Dh/0Eh/0Fh’ Command)

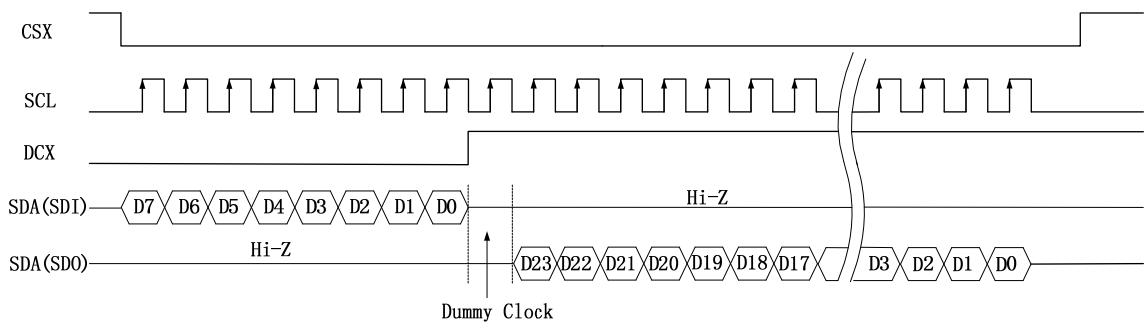


Figure 4-2-2-5 SPI 4-Wire 24-bit Read Operation  
(For ‘04H’ Command with one dummy clock)

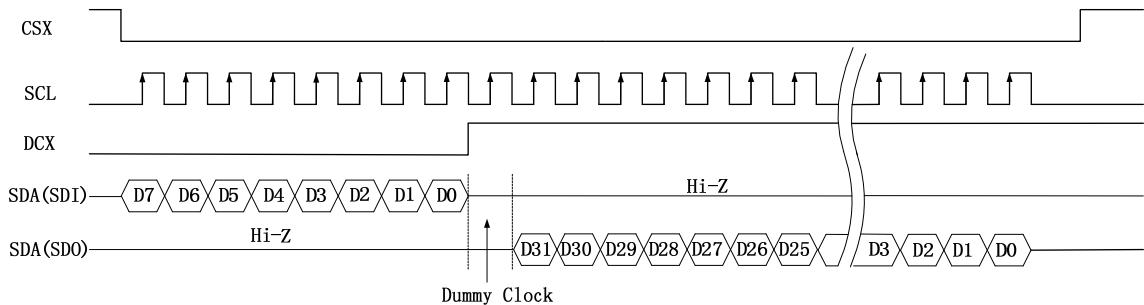


Figure 4-2-2-6 SPI 4-Wire 32-bit Read Operation  
(For ‘09H’ Command with one dummy clock)

#### 4.3. 8080-Series Parallel Interface (P68='0')

The MCU uses an 11-wires 8-data parallel interface or 12-wires 9-data parallel interface or 19-wires 16-data parallel interface or 21-wires 18-data parallel interface. The chip-select CSX (active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. WRX is the parallel data write, RDX is the parallel data read and D[17:0] is parallel data.

The graphics controller chip reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits are display RAM data or command parameters. When D/C='0', D[17:0] bits are commands.

The 8080-series bi-direction interface can be used for communication between the micro-controller and LCD driver chip. The selection of this interface is done when P68 pin is low state (VSS). Interface bus width can be selected with IM2, IM1 and IM0. The interface functions of 8080-series parallel interface are given in Table 4-3-1.

Table 4-3-1 8080 MCU Operation

P68	IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Function
0	1	0	0	8-bit parallel	L	H	R	Write 8-bit command
					H	H	R	Write 8-bit display data or 8-bit parameter
					H	R	H	Read 8-bit display data or 8-bit parameter
0	1	0	1	16-bit parallel	L	H	R	Write 8-bit command
					H	H	R	Write 16-bit display data or 8-bit parameter
					H	R	H	Read 16-bit display data or 8-bit parameter
0	1	1	0	9-bit parallel	L	H	R	Write 8-bit command
					H	H	R	Write 9-bit display data or 8-bit parameter
					H	R	H	Read 9-bit display data or 8-bit parameter
0	1	1	1	18-bit parallel	L	H	R	Write 8-bit command
					H	H	R	Write 18-bit display data or 8-bit parameter
					H	R	H	Read 18-bit display data or 8-bit parameter

Note: Reading operation applied for command code: DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh

## 4.3.1. Write Cycle/Sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control (D/CX, RDX, WRX) and data signals (D[17...0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are a command if the control signal is low (= ‘0’) and vice versa it is data (= ‘1’). The write cycle is described in the following figure.

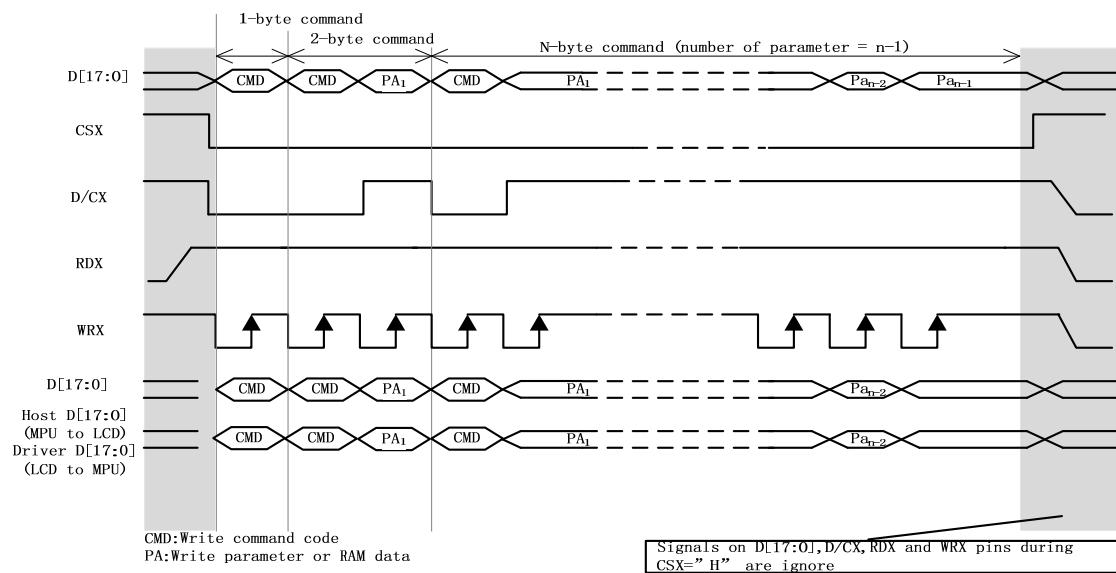


Figure 4-3-1 8080 MCU Write sequence

## 4.3.2. Read Cycle/Sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from the display via interface. The display sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

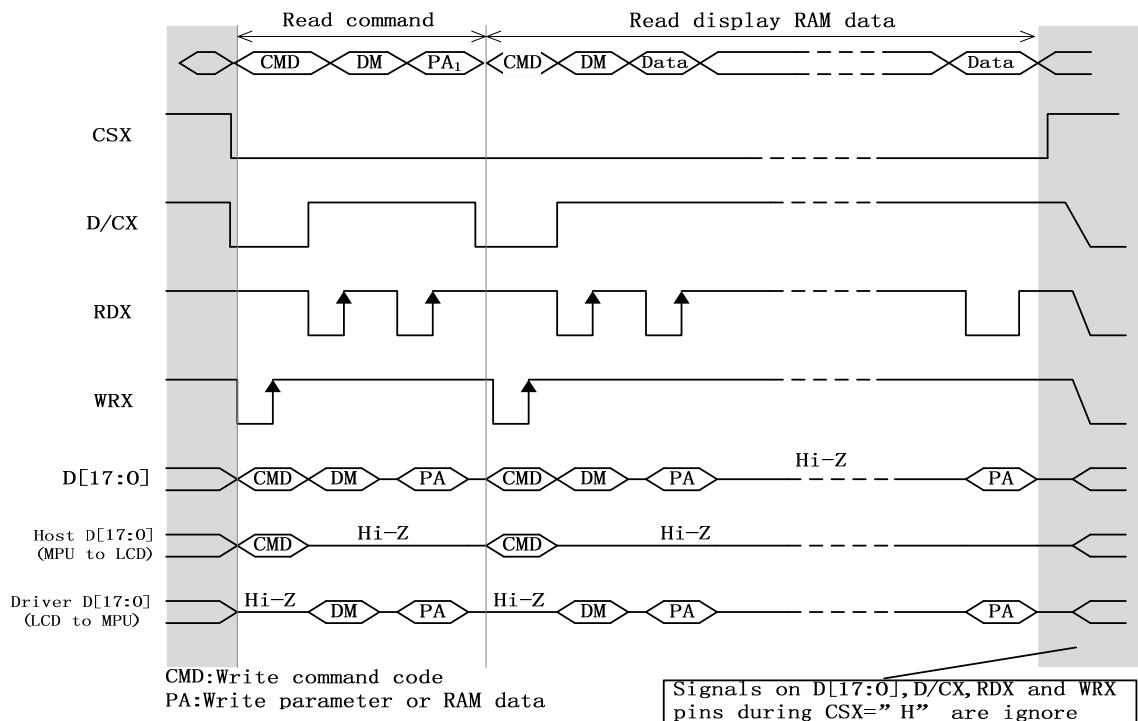


Figure 4-3-2 8080 Read sequence

#### 4.4. 6800-Series Parallel Interface (P68='1')

The MCU uses a 11-wires 8-data parallel interface or 12-wires 9-data parallel interface or 19-wires 16-data parallel interface or 21-wires 18-data parallel interface. The chip-select CSX (active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. WRX is read/write flag, RDX is the parallel data read/write enable and D[17:0] is parallel data.

The Graphics Controller Chip reads the data at the falling edge of RDX signal when WRX = '1' and writes the data at the falling of the RDX signal when R/WX='0'. The D/CX is the data or command flag. When D/CX='1', D[17:0] bits are display RAM data or command parameters. When D/C='0', D[17:0] bits are commands.

The 6800-series bi-direction interface can be used for communication between the micro- controller and LCD driver chip. The selection of this interface is done when P68 pin is high state (IOVCC). Interface bus width can be selected with IM2, IM1 and IM0. The interface functions of 6800-series parallel interface are given in Table 4-4-1.

Table 4-4-1 6800 MCU Operation

P68	IM2	IM1	IM0	Interface	D/CX	WRX	RDX	Function
1	1	0	0	8-bit parallel	L	L	F	Write 8-bit command
					H	L	F	Write 8-bit display data or 8-bit parameter
					H	H	F	Read 8-bit display data or 8-bit parameter
1	1	0	1	16-bit parallel	L	L	F	Write 8-bit command
					H	L	F	Write 16-bit display data or 8-bit parameter
					H	H	F	Read 16-bit display data or 8-bit parameter
1	1	1	0	9-bit parallel	L	L	F	Write 8-bit command
					H	L	F	Write 9-bit display data or 8-bit parameter
					H	H	F	Read 9-bit display data or 8-bit parameter
1	1	1	1	18-bit parallel	L	L	F	Write 8-bit command
					H	L	F	Write 18-bit display data or 8-bit parameter
					H	H	F	Read 18-bit display data or 8-bit parameter

Note: Reading operation applied for command code: DAh, DBh, DCh, 04h, 09h, 0Ah, 0Bh, 0Ch, 0Dh, 0Eh, 0Fh

## 4.4.1. Write Cycle Sequence

The write cycle means that the host writes information (command or/and data) to the display via the interface. Each write cycle consists of 3 control (D/CX, RDX, WRX) and data signals (D[17:0]). D/CX bit is a control signal, which tells if the data is a command or a data. The data signals are a command if the control signal is low (D/CX= '0'), vice versa, it is data (D/CX= '1').WRX work as write or read flag, WRX='0' stands for write operation, WRX='1' means read operation.The detail write cycle is described in the Figure 4-4-1.

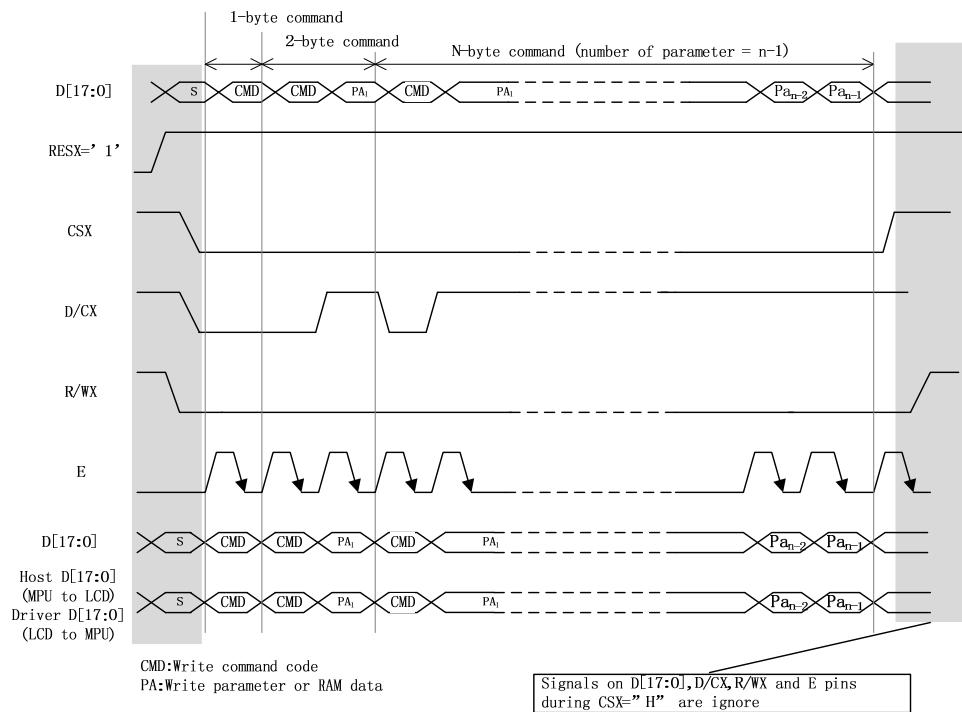


Figure 4-4-1 6800 Write Sequence

## 4.4.2. Read Cycle Sequence

The read cycle means that the host reads information (command or/and data) to the display via the interface. Each read cycle consists of 3 control (D/CX, WRX, RDX) and data (D[17:0]). D/CX bit is control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low and vice versa it is data .WRX work as write or read flag,WRX='0' stands for write operation,WRX='1' means read operation.The detail read cycle is described in the figure Figure 4-4-2.

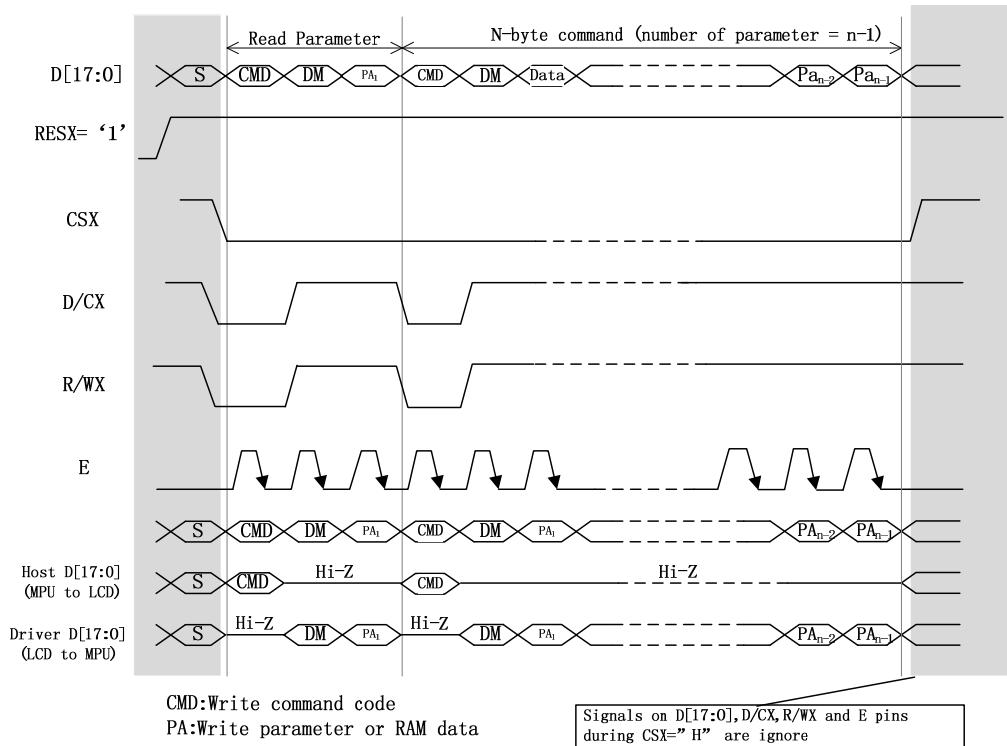


Figure 4-4-2 6800 Read Sequence

#### 4.5. Serial Interface Recovery Function

If there is a break in data transmission by RESX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, then Driver will reject the previous bits and should reset the interface that it will be ready to receive command data again when the chip select line (CSX) is next activated after RESX have been High state. See the following example.

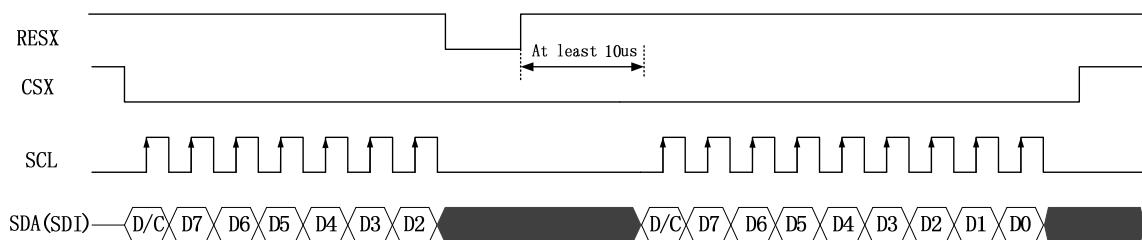


Figure 4-5-1 Serial interface recovery

If there is a break in data transmission by CSX pulse, while transferring a Command or Frame Memory Data or Multiple Parameter command Data, before Bit D0 of the byte has been completed, Then the Driver will reject the previous bits and should reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following example.

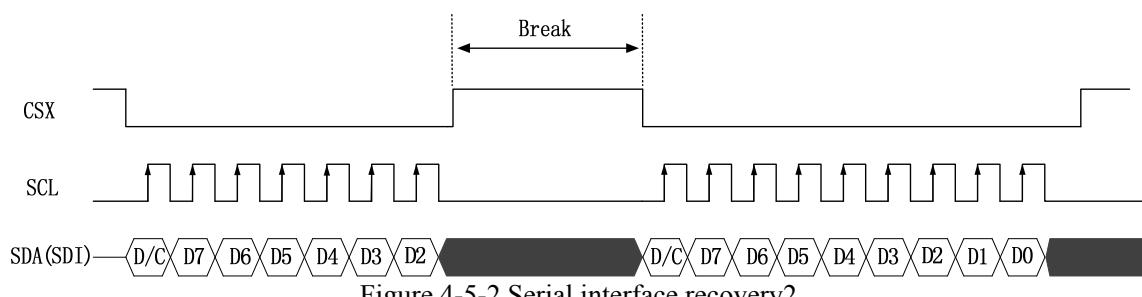


Figure 4-5-2 Serial interface recovery2

If 1, 2 or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than re-transmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as show below.

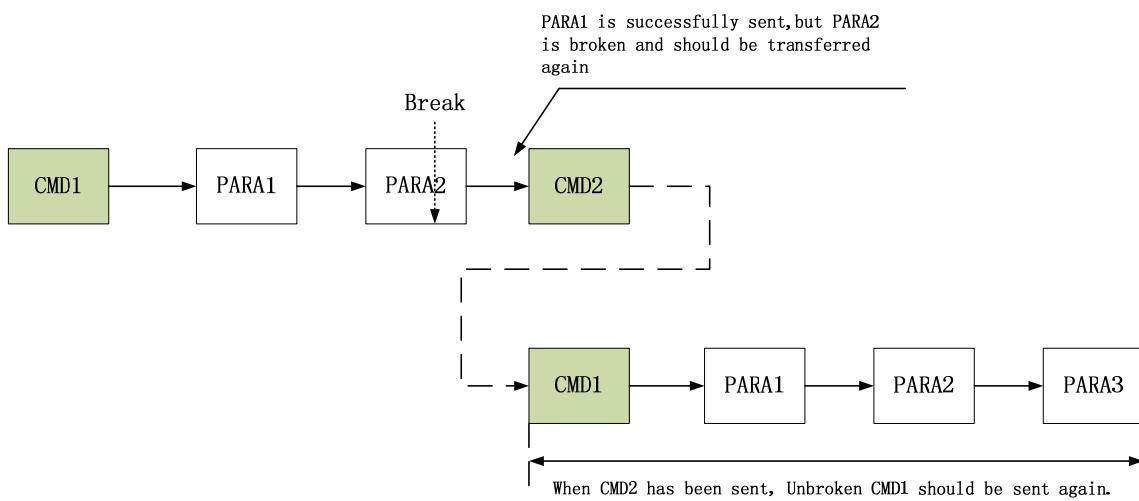


Figure 4-5-3 Serial interface recovery3

### 4.6. Display Data Transmission Pause

It will be possible when transferring a Command, Frame Memory Data or Multiple Parameter Data to invoke a pause in the data transmission. If the Chip Select Line is released after a whole byte of a Frame Memory Data or Multiple Parameter Data has been completed, then the Display Module will wait and continue the Frame Memory Data or Parameter Data Transmission from the point where it was paused. If the Chip Select Line is released after a whole byte of a command has been completed, then the Display Module will receive either the command's parameters (if appropriate) or a new command when the Chip Select Line is next enabled as shown below:

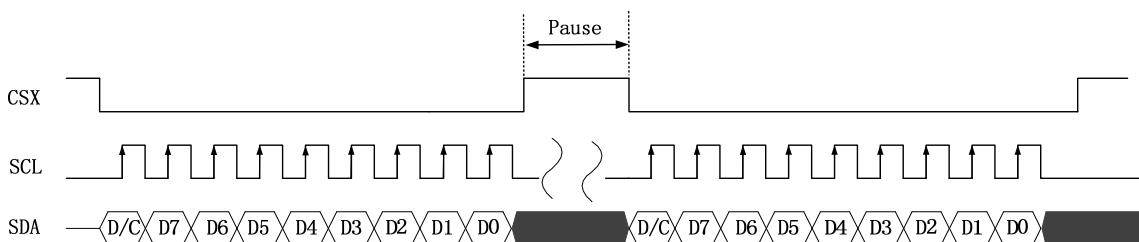


Figure 4-6 Serial interface recovery3

### 4.7. Display Data Transfer Mode

The data format is described for each interface. Data can be downloaded to the Frame Memory by 2 methods.

Method1:

The Image data is sent to the Frame Memory in successive Frame writes, each time the Frame Memory is filled, the Frame Memory pointer is reset to the start point and the next Frame is written.

Start Frame Write	Image Data Frame1	Image Data Frame2	Image Data Frame3
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Method2:

After image data is sent and at the end of each Frame Memory download, a command is sent to stop Frame Memory Write. Then Start Memory Write command is sent, and a new Frame is downloading.

Start Frame Write	Image Data Frame1	Any Command	Start Frame Write	Image Data Frame2	Any Command	. . .	Any Command
-------------------	-------------------	-------------	-------------------	-------------------	-------------	-------	-------------

## 4.8. RGB Interface

### 4.8.1. RGB Interface Selection

The RGB interface mode is available for NV3023A and the interface is selected by setting the VIPF[3:0] bits as following table.

Table 4-8-1 RGB Interface Selection

VIPF[3:0]				RGB Interface				Data Bus							
0	1	1	0	18-bit RGB interface				D[17:0]							
0	1	0	1	16-bit RGB interface				D[17:13],D[11:1]							
1	1	1	0	6-bit RGB interface				D[7:2]							
Others				Setting prohibited											

The display operation via RGB interface is synchronized with the VS, HS and PCLK signals. The RGB interface transfers the updated data to GRAM and the update area is defined by the window address function. The back porch and back porch are used to set the RGB interface timing.

- ◆ 18-bit data bus interface (D[17:0] is used) , VIPF[3:0] = 0110

D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

- ◆ 16-bit data bus interface (D[17:13] and D[11:1] are used) , VIPF[3:0] = 0101

D17	D16	D15	D14	D13	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1		
R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[4]	B[3]	B[2]	B[1]	B[0]		

- ◆ 6-bit data bus interface (D[7:2] is used) , VIPF[3] = 1110

First Transmission						Second Transmission						Third Transmission					
D7	D6	D5	D4	D3	D2	D7	D6	D5	D4	D3	D2	D7	D6	D5	D4	D3	D2
R[5]	R[4]	R[3]	R[2]	R[1]	R[0]	G[5]	G[4]	G[3]	G[2]	G[1]	G[0]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

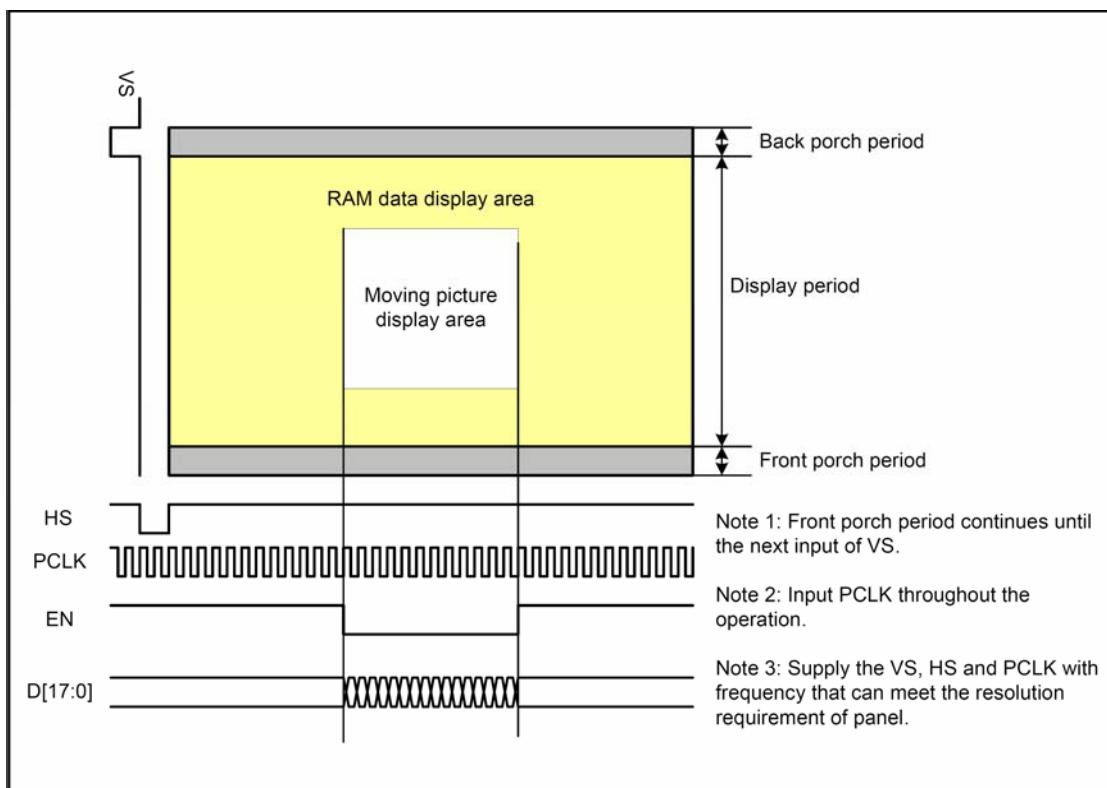
Pixel clock (PCLK) is running all the time without stopping and it is used to entering VS, HS, EN and D[17:0] states when there is a rising edge of the PCLK. The PCLK can not be used as continues internal clock for other functions of the display module.

Vertical synchronization (VS) is used to tell when there is received a new

frame of the display. This is high enable and its state is read to the display module by a rising edge of the PCLK signal.

Horizontal synchronization (HS) is used to tell when there is received a new line of the frame. This is low enable and its state is read to the display module by a rising edge of the PCLK signal.

Data Enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is a high enable and its state is read to the display module by a rising edge of the PCLK signal. D[17:0] are used to tell what is the information of the image that is transferred on the display (When EN= '1' and there is a rising edge of PCLK). D[17:0] can be '0' (low) or '1' (high). These lines are read by a rising edge of the PCLK signal.



### 4.8.2. RGB Interface Timing

The timing chart of Signals in 18-/16-bit RGB interface mode is shown as below:

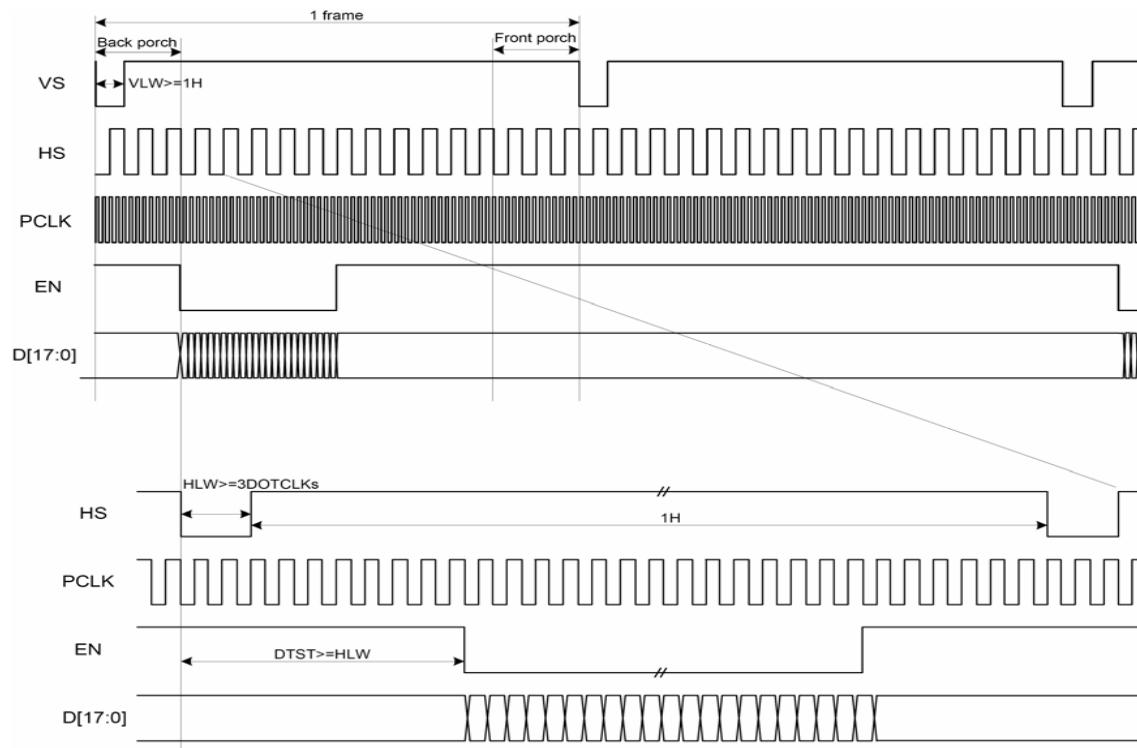


Figure 4-8-2-1 Timing Chart of Signals in 18-/16-bit RGB Interface Mode

The timing chart of 6-bit RGB interface mode is shown as below:

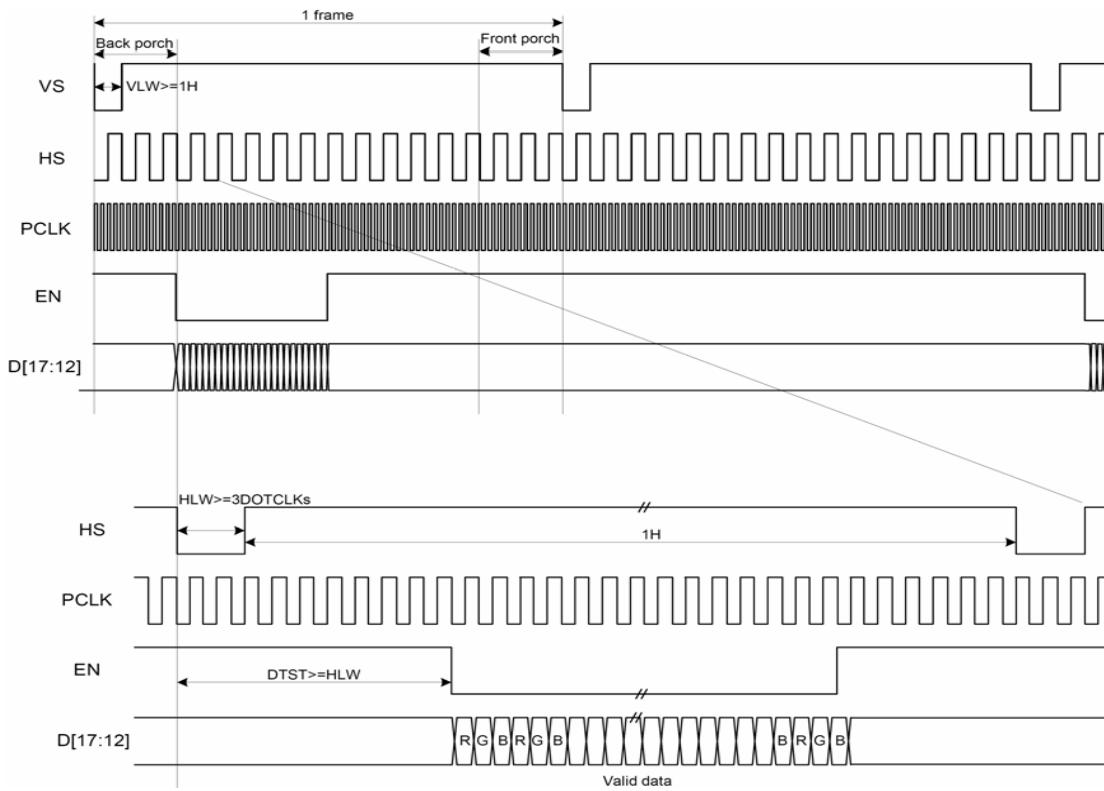


Figure 4-8-2-2 Timing Chart of Signals in 6-bit RGB Interface Mode

Note 1: In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with PCLK.

Note 2: In 6-bit RGB interface mode, set the cycles of VS, HS and EN to 3 multiples of PCLK.

### 4.8.3 RGB Interface Mode Selection

NV3023A supplies a RGB interface with DE mode and can be selected by pull high external “RCM” pad.

When use RGB interface, writing data to frame memory is done by “PCLK” and Video Data Bus. So, controller (host) needn’t always transfer PCLK, VS, HS and DE signals to driver.

## 4.9. Display Data Color Coding

### 4.9.1. Serial Interface

Different display data formats are available for three colors depth supported by the LCM listed below.

- ◆ 4k colors, RGB 4-4-4-bits input
- ◆ 65K colors, RGB 5-6-5-bits input
- ◆ 262K colors, RGB 6-6-6-bits input

Data format and Reconstruct ways are shown as follow figures:

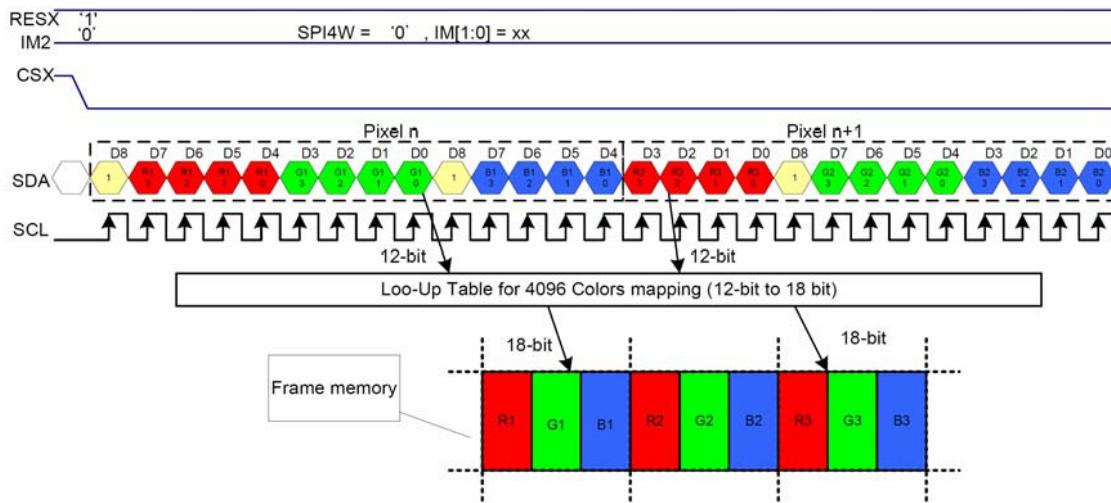


Figure 4-9-1-1 SPI 3-Wire 9-bit RGB4-4-4 Write Data Format

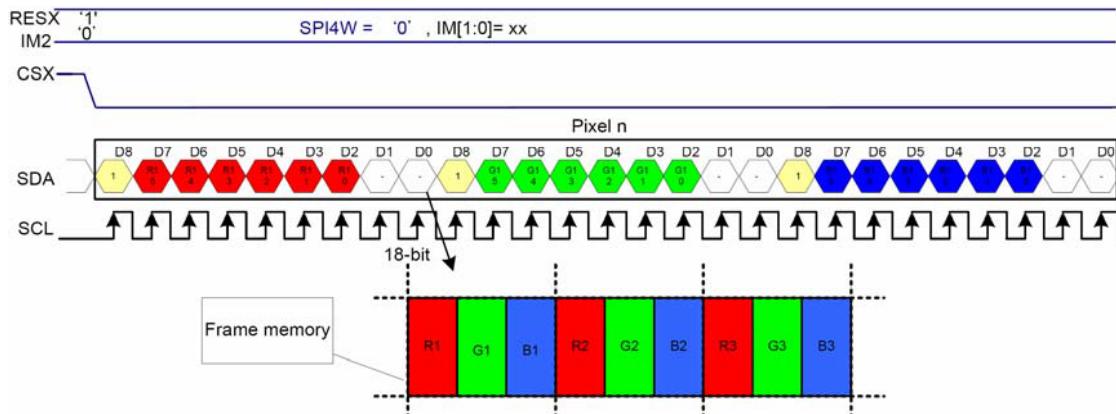


Figure 4-9-1-2 SPI 3-Wire 9-bit RGB6-6-6 Write Data Format

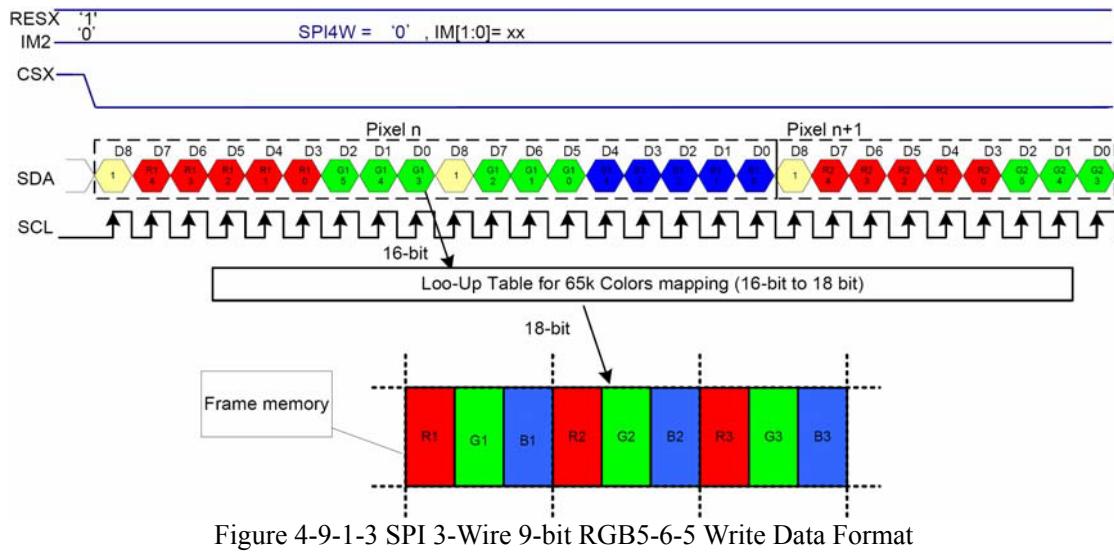


Figure 4-9-1-3 SPI 3-Wire 9-bit RGB5-6-5 Write Data Format

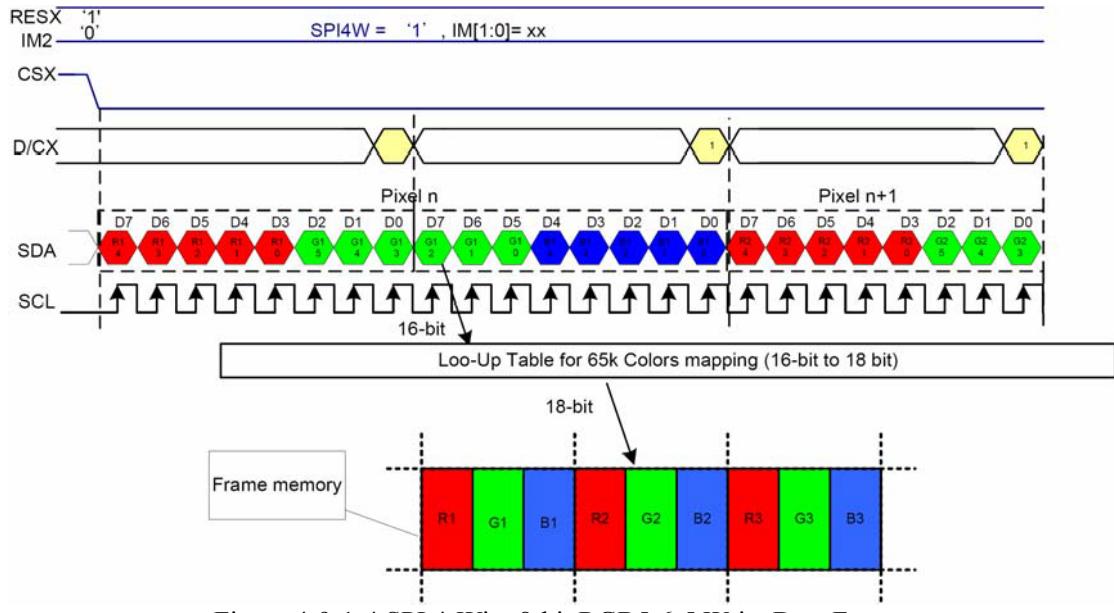


Figure 4-9-1-4 SPI 4-Wire 8-bit RGB5-6-5 Write Data Format

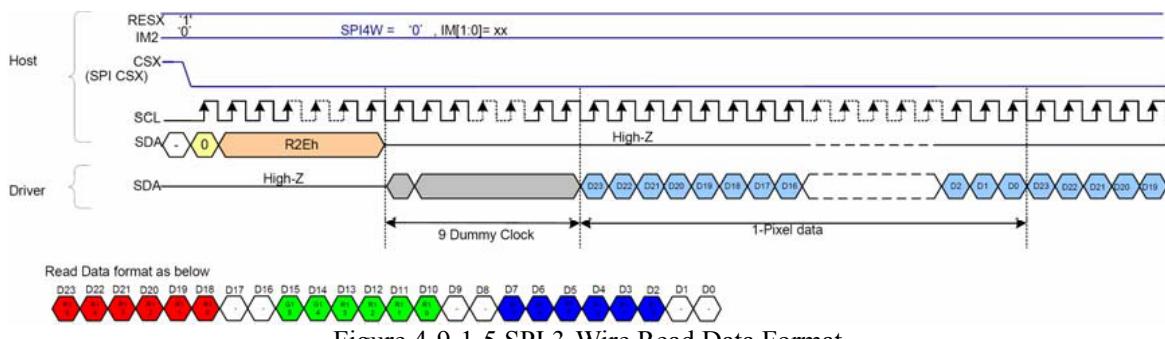


Figure 4-9-1-5 SPI 3-Wire Read Data Format

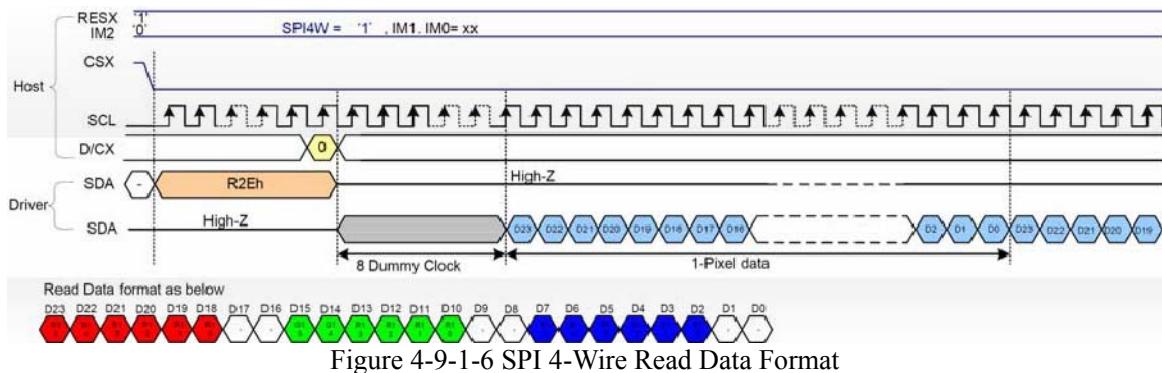


Figure 4-9-1-6 SPI 4-Wire Read Data Format

#### 4.9.2. Parallel 8-bit Interface ( IM="100" )

Different display data formats are available for three colors depth supported by the LCM listed below.

- ◆ 4k colors, RGB 4-4-4-bits input
- ◆ 65K colors, RGB 5-6-5-bits input
- ◆ 262K colors, RGB 6-6-6-bits input

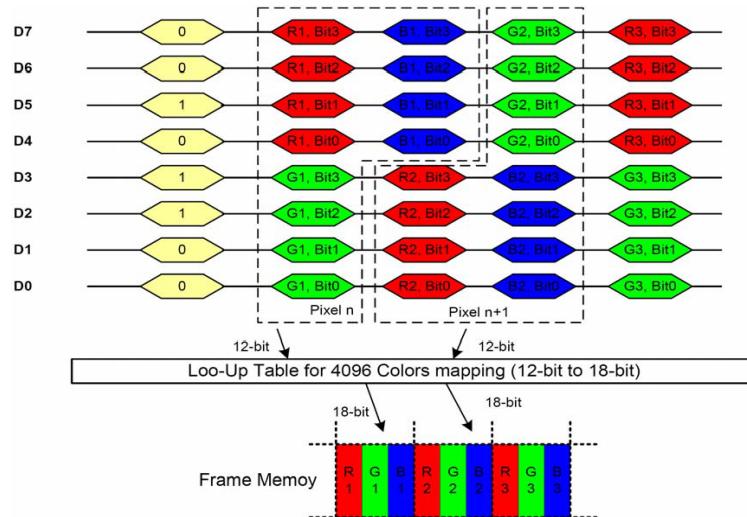


Figure 4-9-2-1 Two pixel (RGB4-4-4) in each three 8-bit write data packets

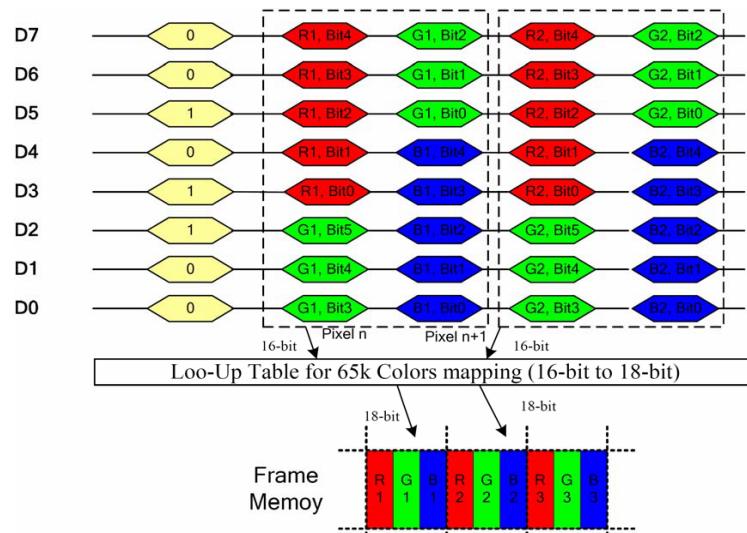


Figure 4-9-2-2 One pixel (RGB5-6-5) in each two 8-bit write data packets

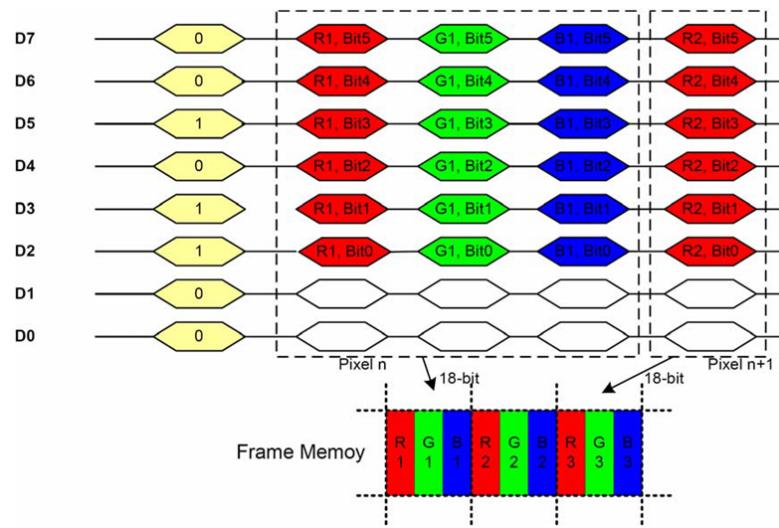


Figure 4-9-2-3 One pixel (RGB6-6-6) in each three 8-bit write data packets

#### 4.9.3. Parallel 9-bit Interface ( IM='110' )

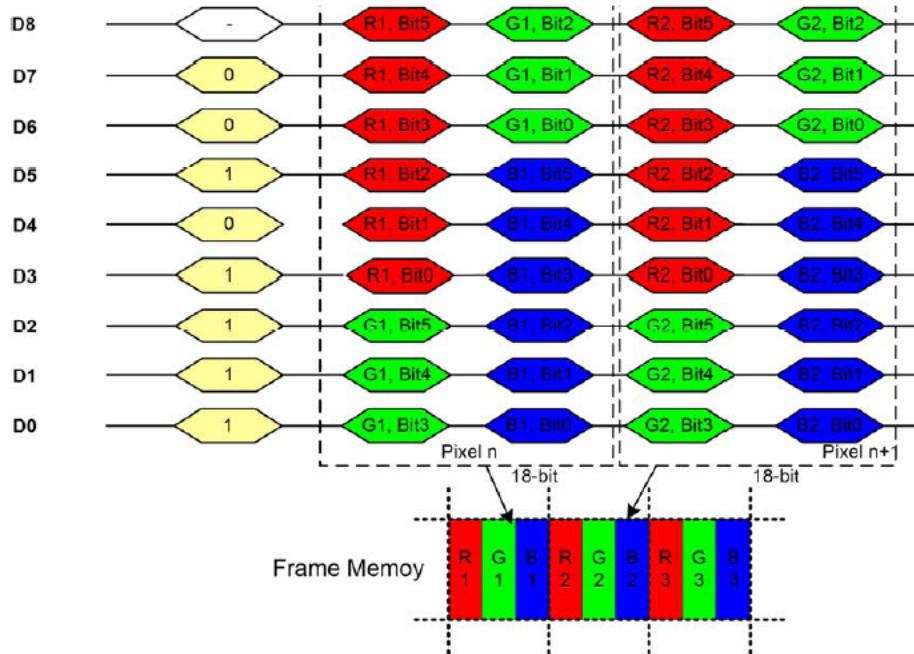


Figure 4-9-3 One pixel (RGB6-6-6) in each two 9-bit write data packets

#### 4.9.4. Parallel 16-bit Interface ( IM="101" )

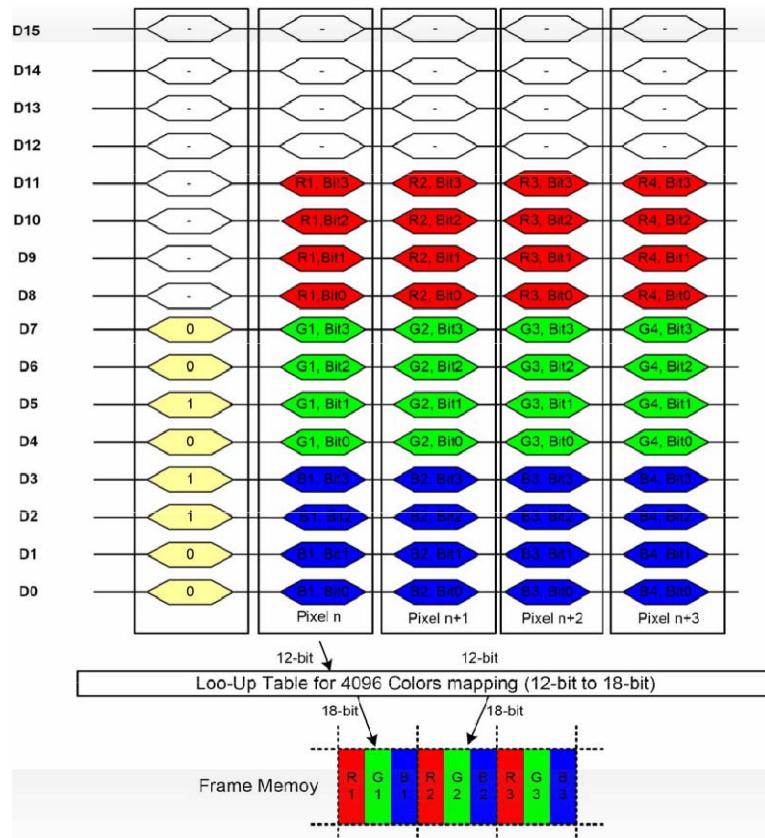


Figure 4-9-4-1 One pixel (RGB4-4-4) in each 16-bit write data packets

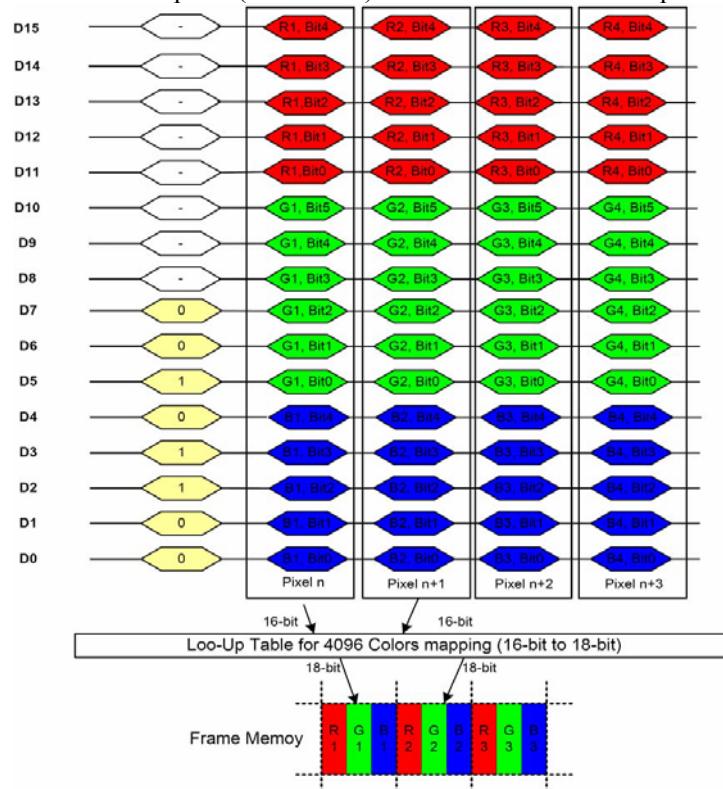


Figure 4-9-4-2 One pixel (RGB5-6-5) in each 16-bit write data packets

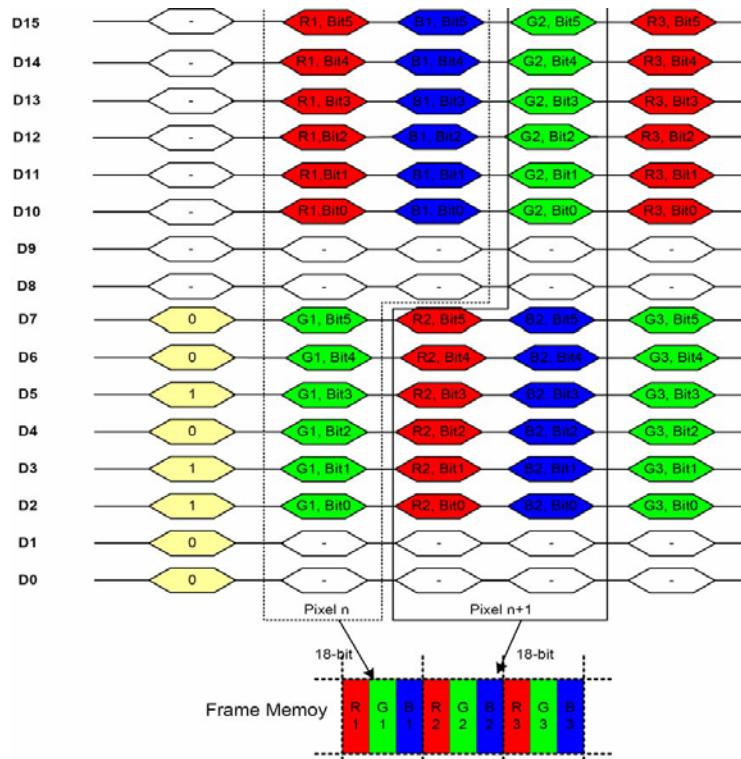


Figure 4-9-4-3 Two pixel (RGB6-6-6) in three 16-bit write data packets

#### 4.9.5. Parallel 18-bit Interface ( IM="111" )

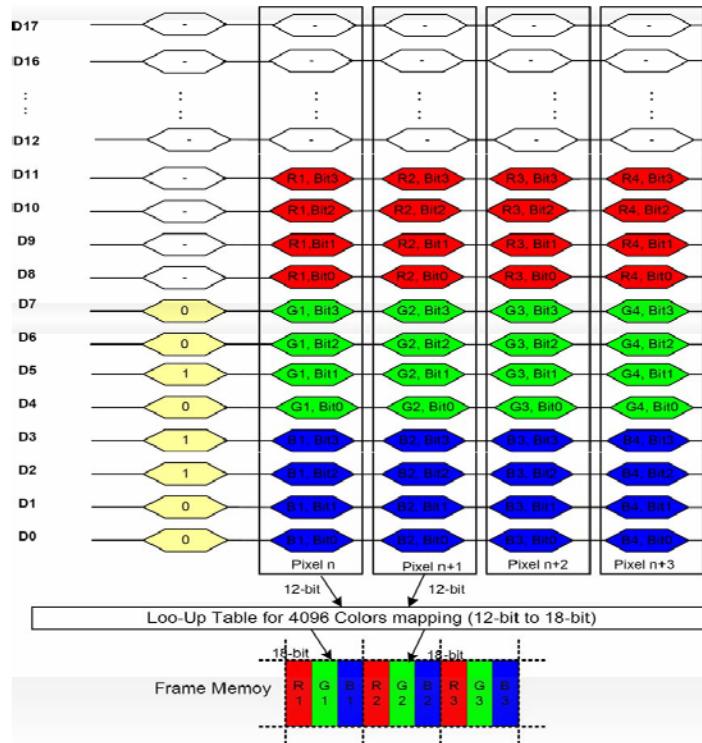


Figure 4-9-5-1 One pixel (RGB4-4-4) in one 18-bit write data packets

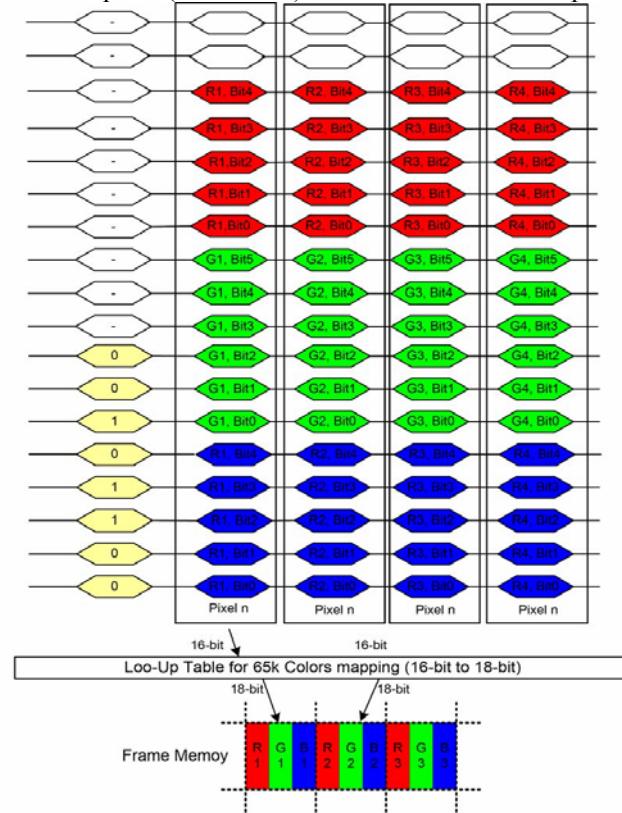


Figure 4-9-5-2 One pixel (RGB5-6-5) in one 18-bit write data packets

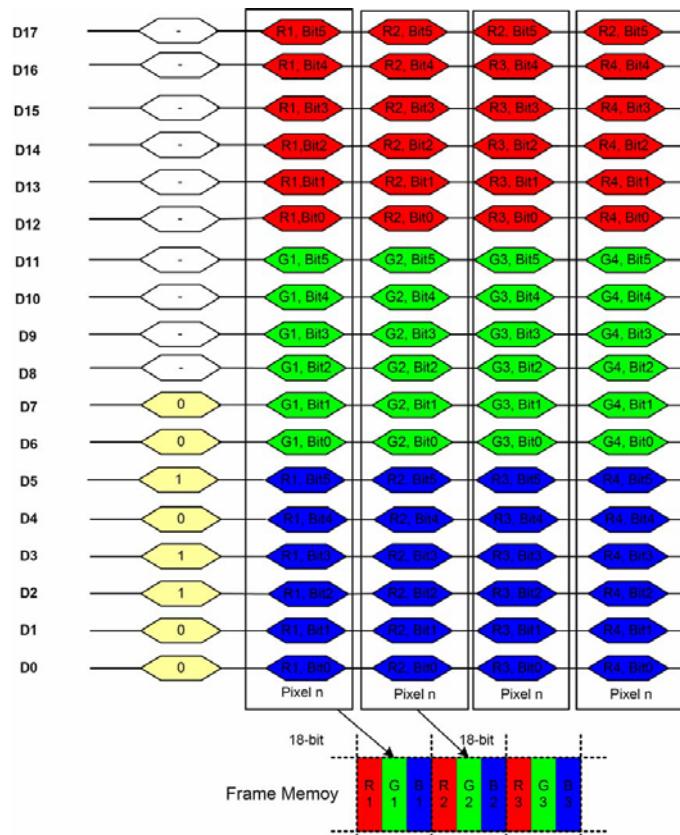
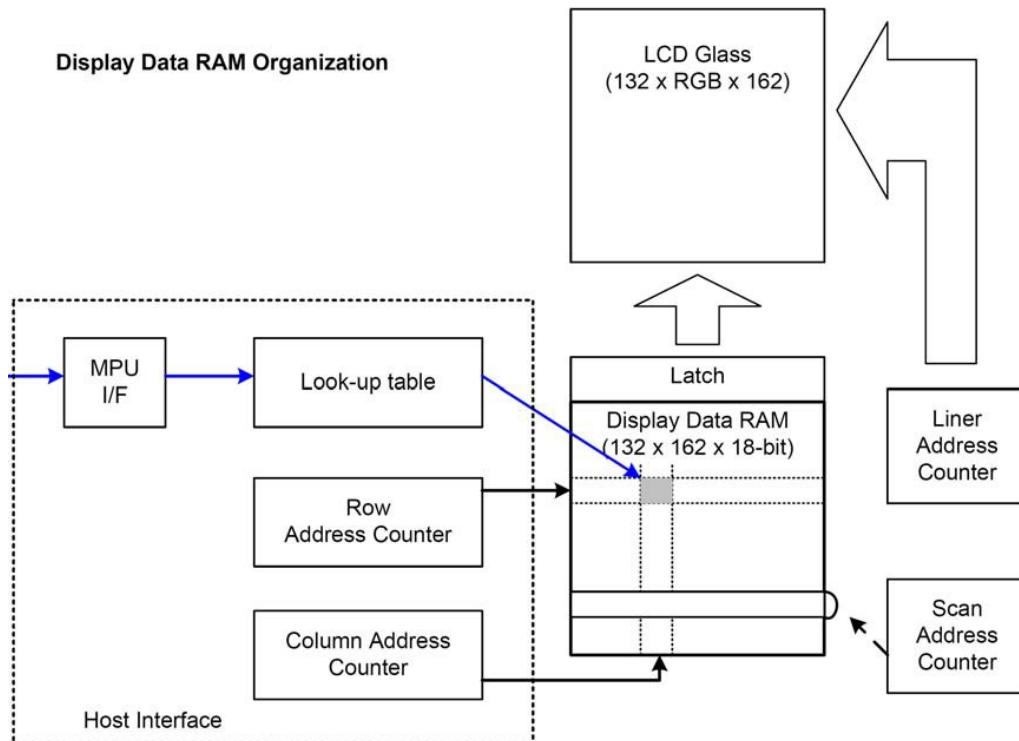


Figure 4-9-5-3 One pixel (RGB5-6-5) in one 18-bit write data packets

## 5. Display Data with SRAM

### 5.1. SRAM Organization

The display data SRAM stores display dots and consists of 384,912 bits (132x18x162 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to “Source”. There will be no abnormal visible effect on the display when there is a simultaneous Panel Read and Interface Read or Write to the same location of the Frame Memory.



## 5.2. Memory To Display Mapping

Display data are written in different direction according to different MX/MY settings, and scan read from SRAM also controlled by ML configuration. The detail as below figure shows:

Gate	Source Out	Pixel			Pixel2			Pixel131			Pixel132			SA			
		S1	S2	S3	S4	S5	S6	---	S391	S392	S393	S394	S395	S396	ML=0	ML=1	
		RA			RGB#				RGB#			RGB#					
		MY=0/MY=1			RGB#				RGB#			RGB#					
1	1	132	R1	G1	B1	R2	G2	B2	---	R131	G131	B131	R132	G132	B132	1	132
2	2	131														2	131
3	3	130														3	130
4	4	129														4	129
5	5	128														5	128
6	6	127														6	127
7	7	126														7	126
8	8	125														8	125
9	9	124														9	124
10	10	123														10	123
11	11	122														11	122
12	12	121														12	121
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	
125	125	8														125	8
126	126	7														126	7
127	127	6														127	6
128	128	5														128	5
129	129	4														129	4
130	130	3														130	3
131	131	2														131	2
132	132	1														132	1
CA	MX-0	1			2					131		132					
	MX-1	132			131					2		1					

Figure 5-2 Display Data Mapping in SRAM

Note:

RA: Row Address

CA: Column Address

SA: Scan Address

MX: Mirror X-axis (Column address direction parameter), configured by MADCTL command

MY: Mirror Y-axis (Row address direction parameter), configured by MADCTL command

ML: Scan direction parameter, configured by MADCTL command

RGB: Red, Blue subpixel position change, configured by MADCTL command

### 5.3. MCU To SRAM Access Direction

The address counter set the addresses of the display data RAM for writing and reading. Data is written pixel-wise into the RAM matrix of DRIVER. The data for one pixel or two pixels is collected (RGB 6-6-6-bit), according to the data formats. As soon as this pixel-data information is complete the “Write access” is activated on the RAM. The locations of RAM are addressed by the address pointers. When GM=011, 132RGB x 162, the address ranges are X=0 to X=131 (83h) and Y=0 to Y=161 (A1h). Addresses outside these ranges are not allowed. Before writing to the RAM a window must be defined into which will be written. The window is programmable via the command register XS, YS designating the start address and XE, YE designating the end address.

For example, the whole display contents will be written, the window is defined by the following values: XS=0(0h) YS=0(0h) and XE=131(83h), YE=161(A1h) In vertical addressing mode (MV=1), the Y-address increments after each byte, after the last Y-address (Y=YE), Y wraps around to YS and X increments to address the next column. In horizontal addressing mode (V=0), the X-address increments after each byte, after the last X-address(X=XE), X wraps around to XS and Y increments to address the next row. After every last address (X=XE and Y=YE) the address pointers wrap around to address (X=XS and Y=YS).

For flexibility in handling a wide variety of display architectures, the commands “CASET, RASET” and “MADCTR”, define flags MX and MY, which allows mirroring of the X-address and Y-address. All combinations of flags are allowed. Below table shows the available combinations of writing to the display RAM. When MX, MY and MV will be changed the data bust be rewritten to the display RAM. For each image orientation, the controls for the column and page counters apply as below:

Condition	Column Counter	Row Counter
When RAMWR/RAMRD command is accepted	Return to “Start Column (XS)”	Return to “Start Row (YS)”
	Column (XS)	
Complete Pixel Read/Write action	Increment by 1	No change
The Column counter value is larger than “End Column (XE)”	Return to “Start Column (XS)”	Increment by 1
The Column counter value is larger than “End Column (XE)” and the Row counter value is larger than “End Row (YE)”	Return to “Start Column (XS)”	Return to “Start Row (YS)”

Table 5-3 Frame Data Write Direction According to the MADCTR parameters (MV, MX and MY)

Display Data Direction	MADCTR Parameter			Image in the Memory (MPU)	Image in the Driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
XY Exchange	1	1	0		
XY Exchange	1	1	1		

## 6. Tearing Effect

The Tearing Effect output line supplies to the MCU a Panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command. The signal can be used by the MCU to synchronize Frame Memory Writing when displaying video images.

### 6.1. Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Sync information only:



Tvdh = The LCD display is not updated from the Frame Memory.

Tvdl = The LCD display is updated from the Frame Memory (except Invisible Line – see below).

Mode 2, the Tearing Effect Output signal consists of V-Sync and H-Sync information, There are one V-sync and 162 H-sync pulses per field:

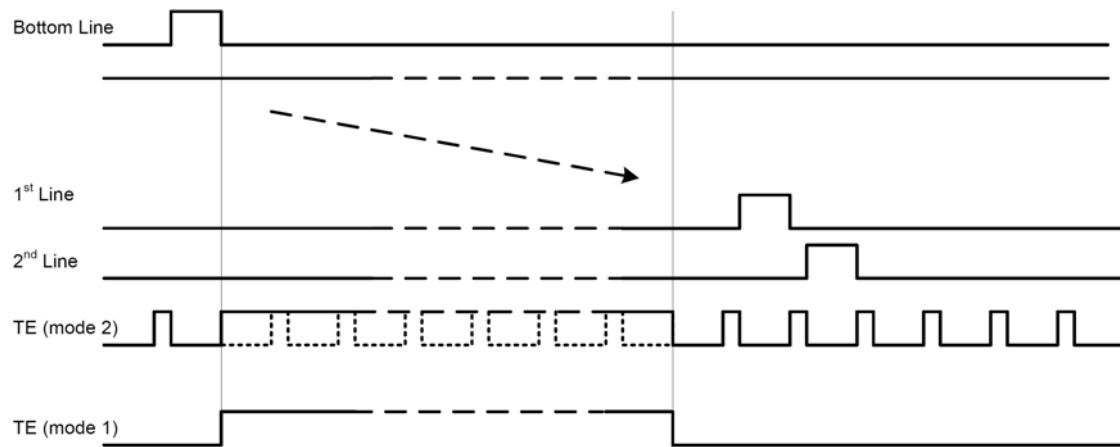


Thdh = The LCD display is not updated from the Frame Memory.

Thdl = The LCD display is updated from the Frame Memory (except Invisible Line – see above).

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Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

## 6.2. Tearing Effect Line Timing

The Tearing Effect signal is described below:

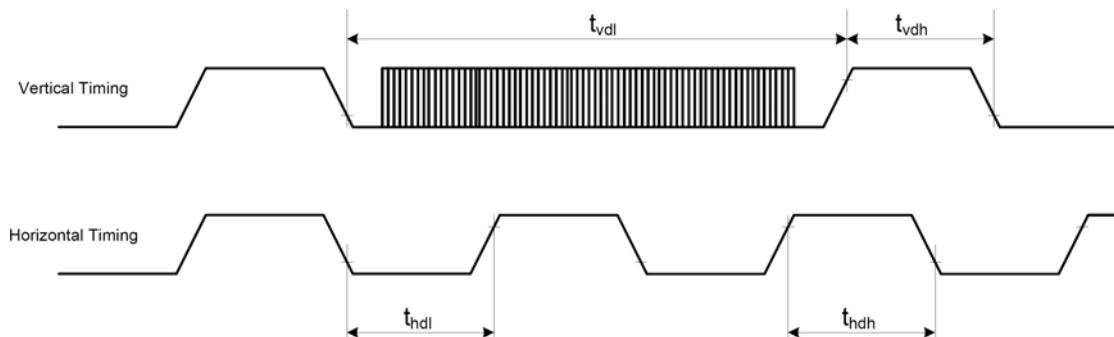


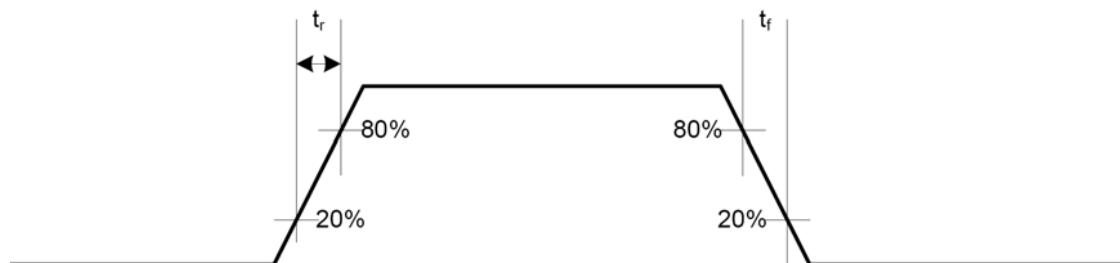
Table 6-2 AC characteristics of Tearing Effect Signal Idle Mode Off/On (Frame Rate = 58.9Hz)

Symbol	Parameter	MIN	MAX	Unit	Description
$t_{vdl}$	Vertical Timing Low Duration	13	-	Ms	
$t_{vdh}$	Vertical Timing High Duration	1000	-	$\mu$ s	
$t_{hdl}$	Horizontal Timing Low Duration	33	-	$\mu$ s	
$t_{hdh}$	Horizontal Timing High Duration	25	500	$\mu$ s	

Notes:

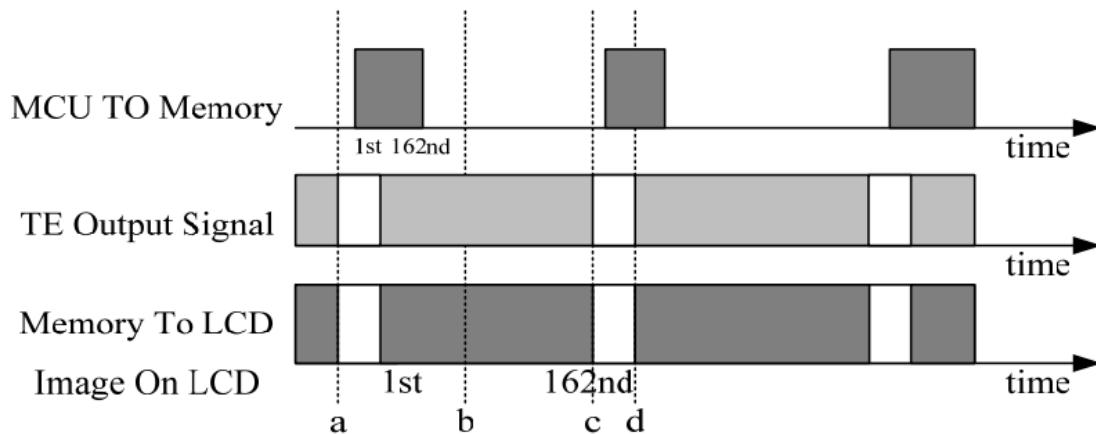
The timings in Table 7-2 apply when MADCTL B4=0

The signal's rise and fall times ( $t_f$ ,  $t_r$ ) are stipulated to be equal to or less than 15ns.



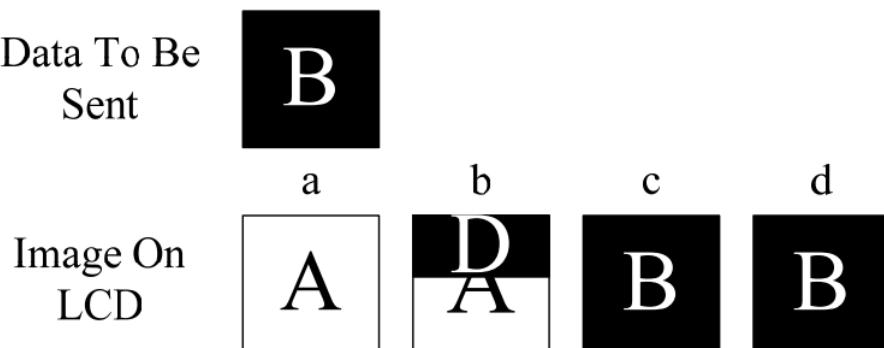
The Tearing Effect Output Line is fed back to the MCU and should be used as shown below to avoid Tearing Effect:

### 6.2.1. Example 1 MCU Write is Faster than Panel Read

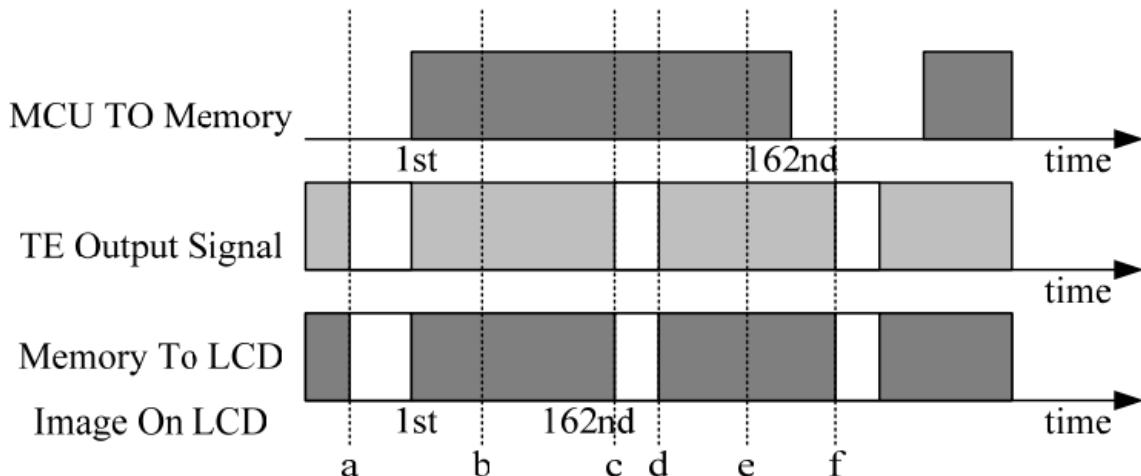


The MCU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MCU to Frame memory write position.

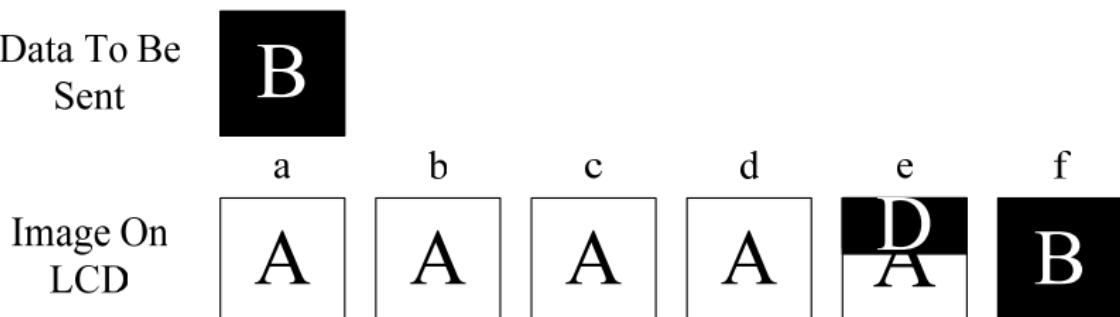
Frame refresh has a complete new image:



### 6.2.2. Example 2 MCU Write is slower than Panel Read



The MCU to Frame Memory write begins just after Panel Read has commenced i.e. after one horizontal sync pulse of the Tearing Effect Output Line. This allows time for the image to download behind the Panel Read pointer and finishing download during the subsequent Frame before the Read Pointer “catches” the MCU to Frame memory write position.



## 7. Power ON/OFF Sequence

IOVCC and VCI can be applied in any order.

VCI and IOVCC can be powered down in any order.

During power off, if LCD is in the Sleep Out mode, VCI and IOVCC must be powered down minimum 120 msec after RESX has been released.

During power off, if LCD is in the Sleep In Mode, IOVCC or VCI can be powered down minimum 0 msec after RESX has been released.

CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX.

Notes:

There will be no damage to the display module if the power sequences are not met.

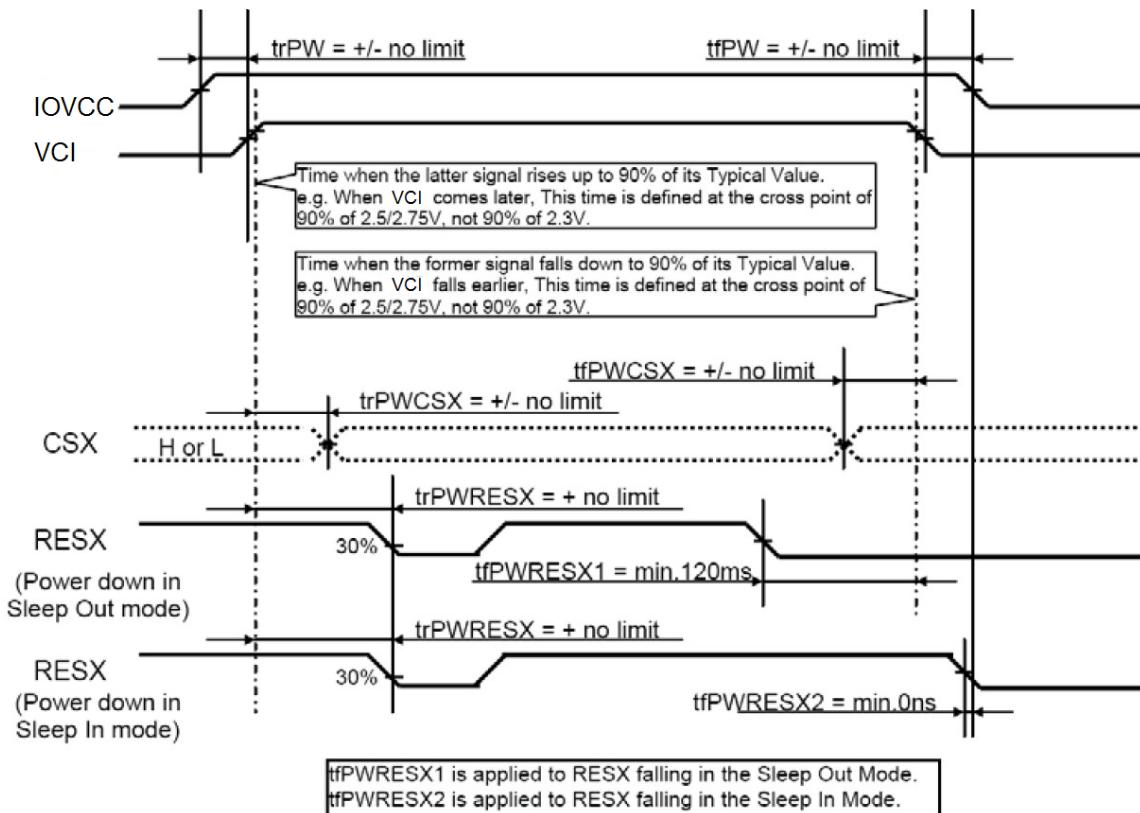
There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.

There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

If RESX line is not held stable by host during Power On Sequence as defined in Sections 8.1 and 8.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed.

## 7.1. Case 1 - RESX line is held high or Unstable by Host at Power On

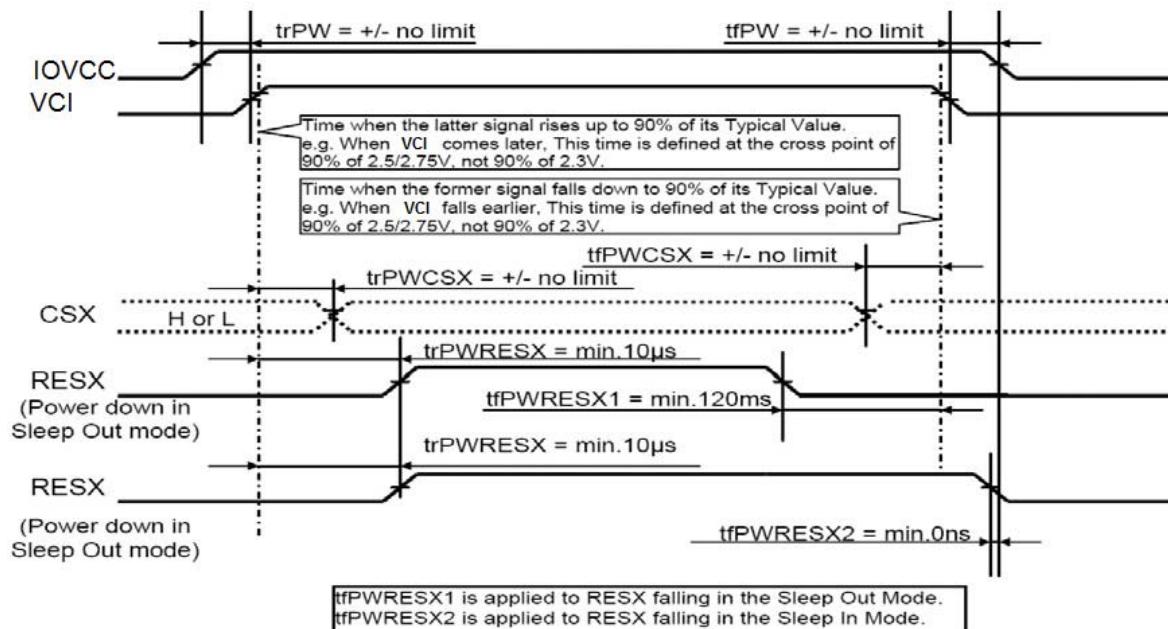
If RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

## 7.2. Case 2 - RESX line is held low by Host at Power On

If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10  $\mu$ sec after both VCI and IOVCC have been applied.



Note: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

## 7.3. Uncontrolled Power Off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. The display module must meet following requirements:

There cannot be any damages for the display module or the display module cannot cause any damages for the host or lines of the interface.

There cannot be any abnormal visible effects (= Display must be blank) within 1 second on the display and remains blank until “Power On Sequence” powers it up.

## 8. Power Level Definition

### 8.1. Power Levels

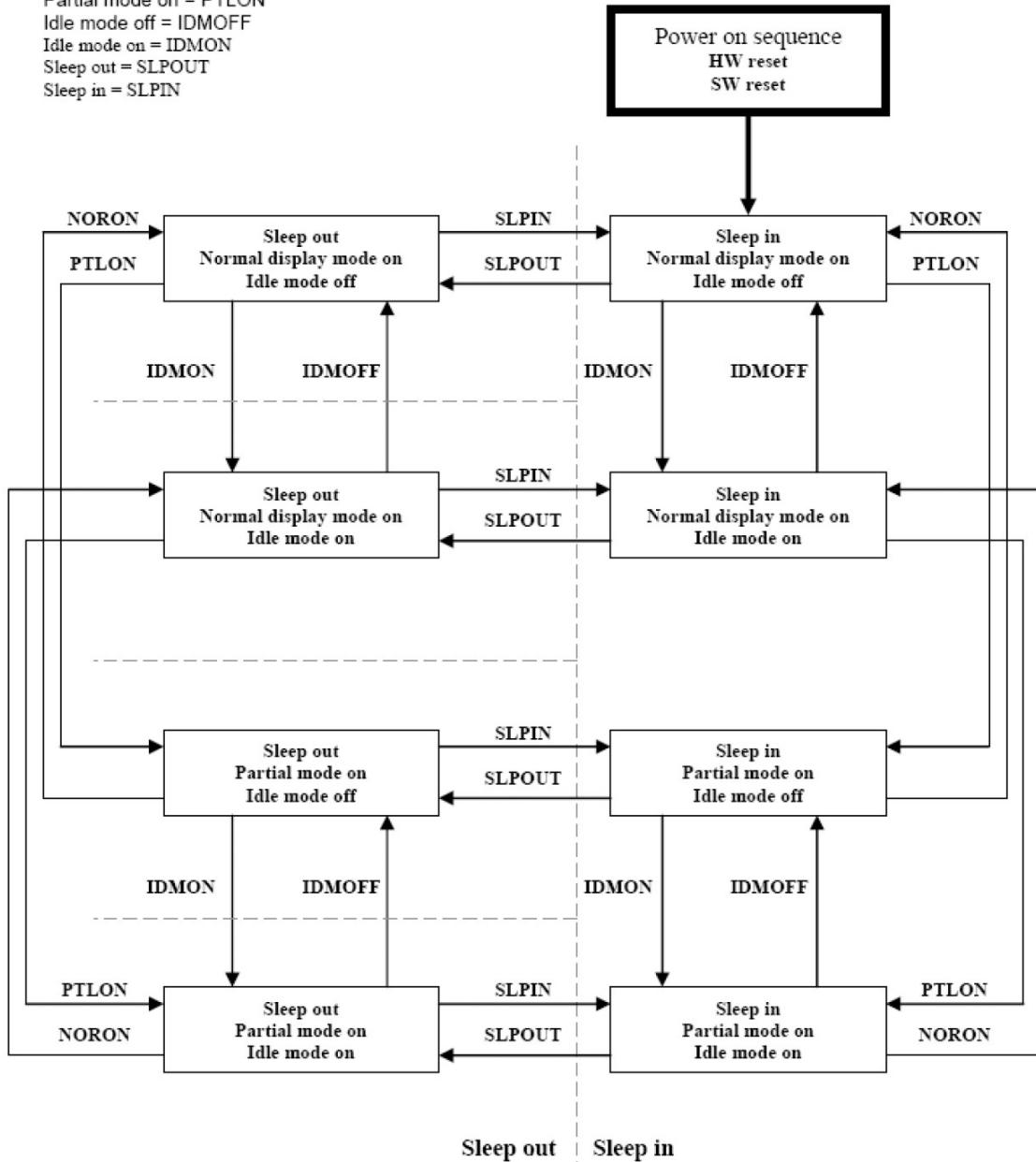
6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption:

1. Normal Mode On (full display), Idle Mode Off, Sleep Out. In this mode, the display is able to show maximum 262,144 colors.
2. Partial Mode On, Idle Mode Off, Sleep Out. In this mode part of the display is used with maximum 262,144 colors.
3. Normal Mode On (full display), Idle Mode On, Sleep Out. In this mode, the full display area is used but with 8 colors.
4. Partial Mode On, Idle Mode On, Sleep Out. In this mode, part of the display is used but with 8 colors.
5. Sleep In Mode. In this mode, the DC/DC converter, internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with IOVCC power supply. Contents of the memory are safe.
6. Power Off Mode. In this mode, both VCI and IOVCC are removed.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed. If RESX line is held high or unstable by the host during Power On, then a Hardware Reset must be applied after both VCI and IOVCC have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon

## 8.2. Power Flow Chart

Normal display mode on = NORON  
Partial mode on = PTLON  
Idle mode off = IDMOFF  
Idle mode on = IDMON  
Sleep out = SLPOUT  
Sleep in = SLPIN



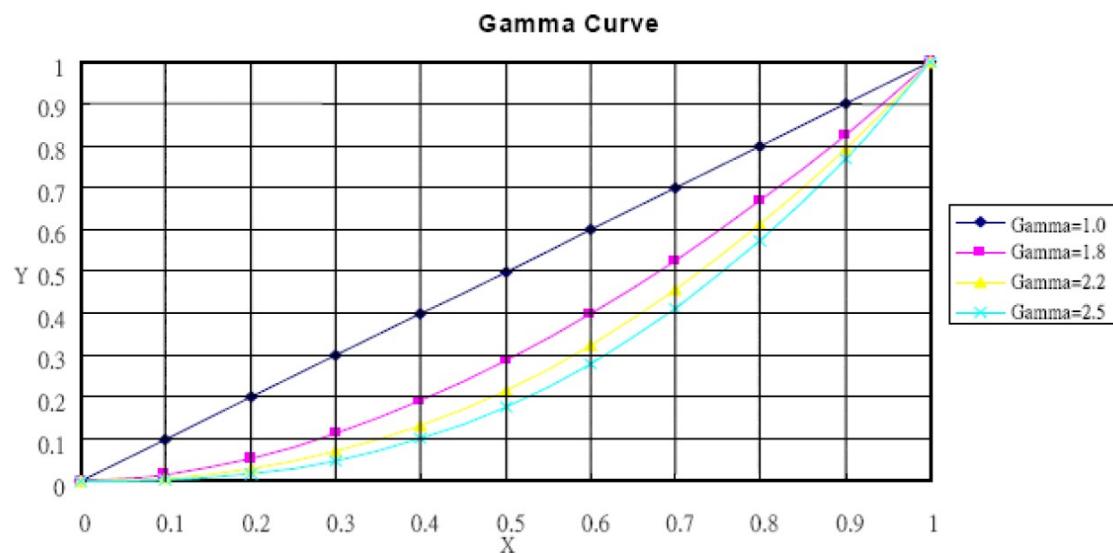
Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by Nokia, when there is changing from one power mode to another power mode.

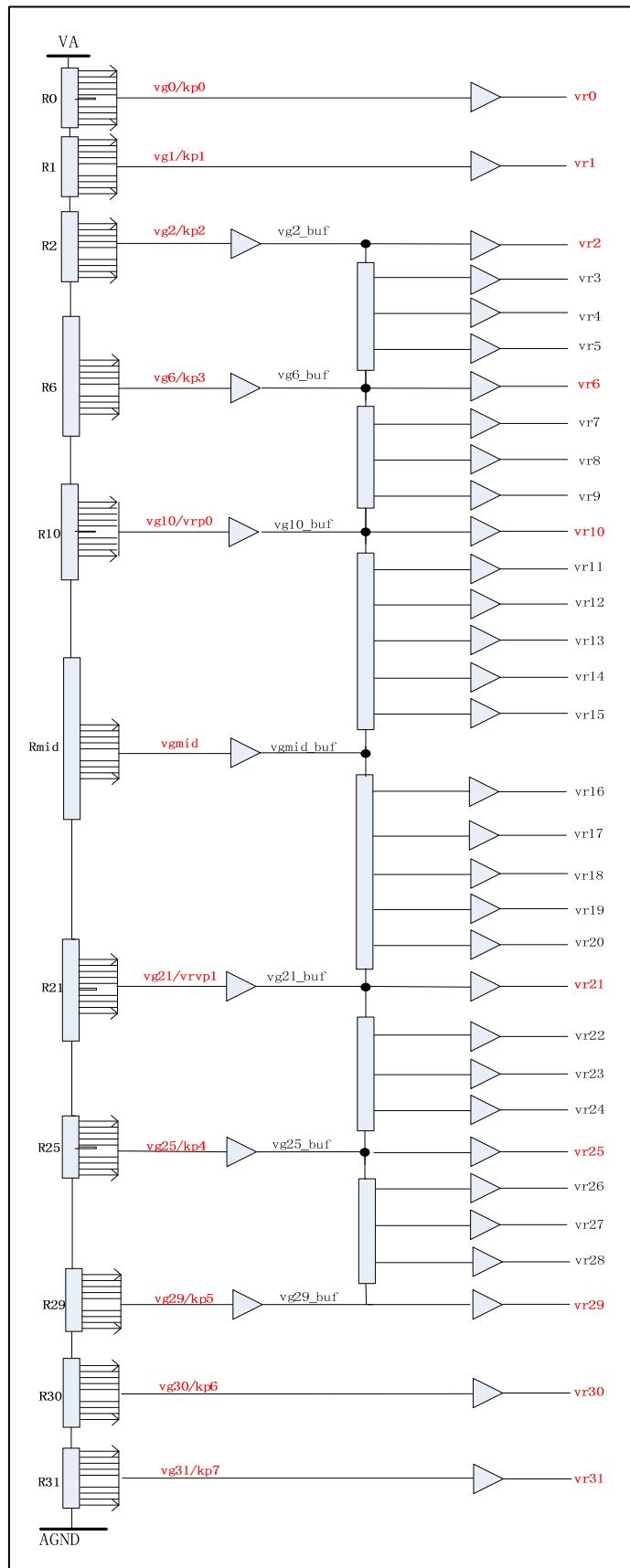
Note 3: It is recommended that it should be enter Sleep in before power off.

## 9. Gamma Curve

### 9.1. Gamma curve according to the Gamma 1.0/1.8/2.2/2.5



## 9.2. Gamma Structure



## 10. Reset Function

### 10.1. State of Register After Different Reset

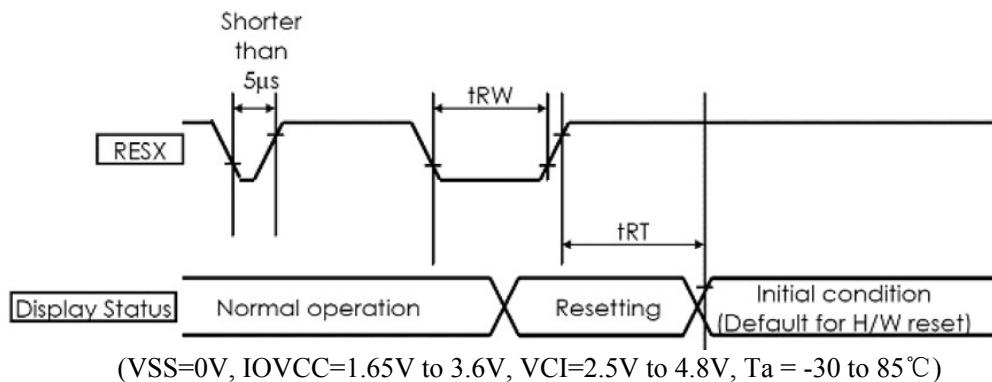
The registers for resolution 128(RGB) x160 are initialized are listed below:

Item	After Power On	After Hardware Reset	After
			Software Reset
Frame memory	Random	No Change	No Change
Sleep In/Out	In	In	In
Display On/Off	Off	Off	Off
Display mode(normal/partial)	Normal	Normal	Normal
Display Inversion On/Off	Off	Off	Off
Display Idle Mode On/Off	Off	Off	Off
Column:Start Address(XS)	0000h	0000h	0000h
Column:End Address(XE)	007Fh	007Fh	007Fh
Row:Start Address(YS)	0000h	0000h	0000h
Row:End Address(YE)	009Fh	009Fh	009Fh
Gamma Setting	GC0	GC0	GC0
Color Set	262K	262K	262K
Partial:Start Address(PSL)	0000h	0000h	0000h
Partial:End Address(PEL)	009Fh	009Fh	009Fh
Scroll:Vertical scrolling	Off	Off	Off
Scroll:Top Fixed Area(TFA)	0000h	0000h	0000h
Scroll:Scroll Area(VSA)	00A0h	00A0h	00A0h
Scroll:Bottom Fixed Area(BFA)	0000h	0000h	0000h
Scroll Start Address (SSA)	0000h	0000h	0000h
Tearing:On/Off	Off	Off	Off
Tearing Effect Mode*3	0(Mode1)	0(Mode1)	0(Mode1)
Memory Data Access Control (MY/MX/MV/ML/MH/RBG)	0/0/0/0/0/0	0/0/0/0/0/0	No change
Interface Pixel Color Format	6(18-Bit/Pixel)	6(18-Bit/Pixel)	No change
RDDPM	08h	08h	08h
RDDMADCTR	0	0	No change
RDDCOLMOD	6(18-Bit/Pixel)	6(18-Bit/Pixel)	No change
RDDIM	00h	00h	No change
RDDSM	00h	00h	00h
RDDSER	00h	00h	00h
ID1	33h	33h	33h
ID2	30h	30h	30h
ID3	25h	25h	25h

Notes:

1. There will be no abnormal visible effects on the display when S/W or H/W Reset are applied.
2. After Powered-On Reset finishes within 10μs after both VCI & IOVCC are applied.
3. Mode 1 means Tearing Effect Output Line consists of V-Blanking Information only.

## 10.2. Reset Timing



Symbol	Parameter	Related Pins	MIN	TYP	MAX	Note	Unit
tRW	Valid Reset low pulse width	RESX	10	-	-	-	us
tRT	Valid Reset Complete width	RESX	-	-	5	When reset applied during Sleep in mode	ms
		RESX	-	-	120	When reset applied during Sleep out mode	ms

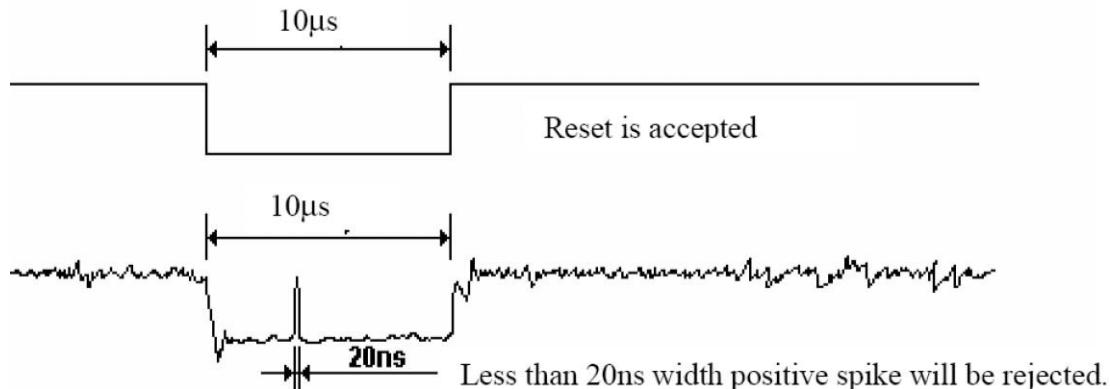
Note:

1> Spike due to an electrostatic discharge on RESX line does not cause system reset according to the table below.

RESX Pulse	Action
Shorten than 5us	Reset Rejected
Longer than 10us	Reset
Between 5us and 10us	Reset starts(It depends on voltage and temperature condition)

2> During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In mode) and then return to Default condition for Hardware Reset.

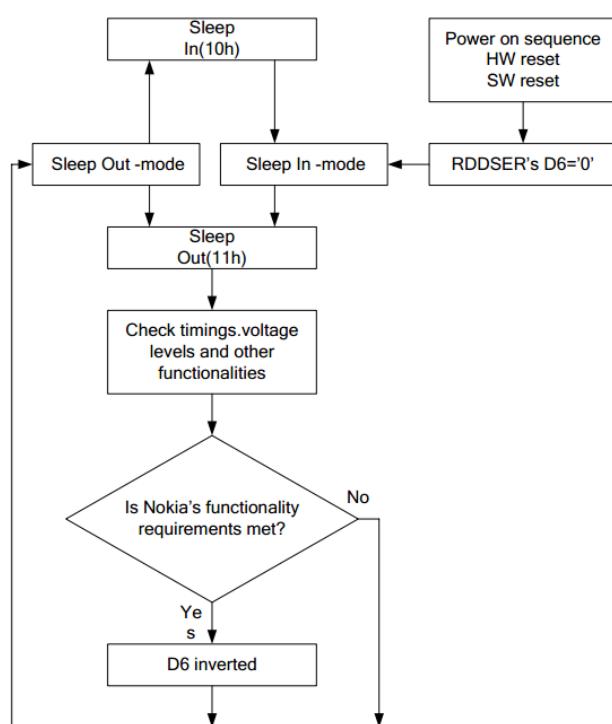
3> Spike Rejection also applies during a valid reset pulse as shown below:



4> It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

## 11. Sleep Out and Self-Diagnostic Functions of Display

Sleep Out-command (11h) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements. The internal function (= the display controller) is comparing, if the display module is still meeting functionality requirements (only Booster voltage level). If functionality requirement is met, there is inverted a bit, which defined in command (“0Fh”, The used bit of this command is D6). If functionality requirement is not same, this bit (D6) is not inverted. The flow chart for this internal function is following:



Note: There is needed 120msec after Sleep Out command, when there is changing from Sleep In mode to Sleep Out mode, before there is possible to check if Nokia's functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out command is sent in Sleep Out mode.

## 12. Command

### 12.1. System Function Command List and Description

Addr	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0x00	NOP	W	0	0	0	0	0	0	0	0
0x01	SWR ESET	W	0	0	0	0	0	0	0	0
0x04	RDDI D	R				sys_id1[7:0]				
						sys_id2[7:0]				
						sys_id3[7:0]				
0x09	RDD ST	R	boost_on	my	mx	mv	ml	rgb		
						pixel_fmt[3:0]	idle_on	ptl_on	slpout	norma1_on
			scroll_on	1'b0	invon	0	0	dispon	te_on	0
			0	0	telom			rgb_on		
0x0A	RDD PM	R	boost_on	idle_on	ptl_on	slpout	norma1_on	dispon	0	0
0x0B	RDD_MAD_CTR	R	my	mx	mv	ml	sbgr	0	0	0
0x0C	RDD_COL_MOD	R			vipf[3:0]		0		ifpf[2:0]	
0x0D	RDDI M	R	scroll_on	1'b0	invon	0	0	0	0	0
0x0E	RDD SM	R	te_on	telom	0	0	0	0	0	0
0x0F	RDD SDR	R			self_diag[4:0]		0	0	0	0
0x10	SLPI N	W								
0x11	SLPO UT	W								
0x12	PTLO N	W								
0x13	NOR ON	W								
0x20	INVO FF	W								
0x21	INVO N	W								
0x28	DISP OFF	W								
0x29	DISP ON	W								
0x2A	CASE T	W				0x00				
						col_st_set[7:0]				

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Addr	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0				
			0x00											
			col_ed_set[7:0]											
0x2B	RASET	W	0x00											
			row_st_set[7:0]											
			0x00											
			row_ed_set[7:0]											
0x2C	RAM WR	W												
0x2E	RAM RD	W												
0x30	PTLA R	W	ptl_st_set[7:0]											
			ptl_ed_set[7:0]											
0x33	SCRL AR	W	tfa[7:0]											
			vsd[7:0]											
0x34	TEOF F	W												
0x35	TEO N	W									TELO M			
0x36	MAD CTR	W	my	mx	mv	ml	rgb							
0x37	VSCS AD	W	ssa[7:0]											
0x38	IDM OFF	W												
0x39	IDM ON	W												
0x3A	COL MOD	W	vipf[3:0]					ifpf[2:0]						
0x3D	SPI2S ET	W					spi2li ne_en		spi2line_mode [1:0]					
0xDA	RDID 1	R	sys_id1[7:0]											
0xDB	RDID 2	R	sys_id2[7:0]											
0xDC	RDID 3	R	sys_id3[7:0]											

### 12.1.1. NOP (00h)

<b>00H</b>	<b>No Operation</b>																							
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	L	H	R	0	0	0	0	0	0	0	0	00H												
Parameter	No Parameter																							
Description	This command is an empty command. It does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands. X=Don't care.																							
Restriction	None																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode on,Idle Mode Off,Sleep Out	Yes																							
Normal Mode on,Idle Mode On,Sleep Out	Yes																							
Partial Mode on,Idle Mode Off,Sleep Out	Yes																							
Partial Mode on,Idle Mode On,Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>N/A</td> </tr> <tr> <td>SW Reset</td> <td>N/A</td> </tr> <tr> <td>HW Reset</td> <td>N/A</td> </tr> </tbody> </table>												Status	Default Value	Power On Sequence	N/A	SW Reset	N/A	HW Reset	N/A				
Status	Default Value																							
Power On Sequence	N/A																							
SW Reset	N/A																							
HW Reset	N/A																							

### 12.1.2. SWRESET (01h)

<b>01H</b>		Software Reset																						
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	L	H	R	0	0	0	0	0	0	0	1	01H												
Parameter	No Parameter																							
Description	When the Software Reset command is written, it causes software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are affected by this command. X=Don't care																							
Restriction	None																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode on,Idle Mode Off,Sleep Out	Yes																							
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Status	Default Value																							
Power On Sequence	N/A																							
SW Reset	N/A																							
HW Reset	N/A																							

### 12.1.3. RDDID (04h)

<b>04H</b>		Read Display ID																														
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																				
Command	L	R	H	0	0	0	0	0	1	0	0	04H																				
Parameter1	H	R	H	X	X	X	X	X	X	X	X	X																				
Parameter2	H	R	H	SYS_ID1[7:0]									33H																			
Parameter3	H	R	H	SYS_ID2[7:0]									30H																			
Parameter4	H	R	H	SYS_ID3[7:0]									25H																			
Description	This read byte returns 24-bit display identification. The 1st Parameter is dummy read. The 2st Parameter (SYS_ID1): LCD module's manufacture ID. The 3st Parameter (SYS_ID2): LCD module/driver version ID. The 4st Parameter (SYS_ID3): LCD module/driver version ID. Note: Commands RDDID1/2/3 (DAh, DBh, DCh) read data correspond to the parameters 1, 2, 3 of command 04h, respectively.																															
Restriction	None																															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes							
Status	Availability																															
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Partial Mode on,Idle Mode On,Sleep Out	Yes																															
Sleep In	Yes																															
Default	<table border="1"> <thead> <tr> <th rowspan="2">Status</th> <th colspan="3">Default Value</th> </tr> <tr> <th>ID1</th> <th>ID2</th> <th>ID3</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>33h</td> <td>30h</td> <td>25h</td> </tr> <tr> <td>SW Reset</td> <td>33h</td> <td>30h</td> <td>25h</td> </tr> <tr> <td>HW Reset</td> <td>33h</td> <td>30h</td> <td>25h</td> </tr> </tbody> </table>													Status	Default Value			ID1	ID2	ID3	Power On Sequence	33h	30h	25h	SW Reset	33h	30h	25h	HW Reset	33h	30h	25h
Status	Default Value																															
	ID1	ID2	ID3																													
Power On Sequence	33h	30h	25h																													
SW Reset	33h	30h	25h																													
HW Reset	33h	30h	25h																													

### 12.1.4. RDDST (09h)

09H		Read Display Status																																																																	
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																							
Command	L	R	H	0	0	0	0	1	0	0	1	09H																																																							
Parameter1	H	R	H	X	X	X	X	X	X	X	X	X																																																							
Parameter2	H	R	H	BOOS T_ON	MY	MX	MV	ML	RGB	0	0	-																																																							
Parameter3	H	R	H	PIXEL_FMT[3:0]				IDLE_ ON	PTL_O N	SLPOU T	NORMA L_ON	-																																																							
Parameter4	H	R	H	SCROL L_ON	0	INVON	0	0	DISPO N	TE_ON	0	-																																																							
Parameter5	H	R	H	0	0	TELO M	RGB_ON					-																																																							
Description	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>BOOST_ON</td> <td>Booster Voltage Status</td> <td>“1”=Booster on, “0”=Booster off</td> </tr> <tr> <td rowspan="2">MY</td> <td rowspan="2">Row Address Order(MY)</td> <td>“1”=Decrement. (Bottom to Top), when MADCTL (36h) D7=“1”</td> </tr> <tr> <td>“0”=Increment.(Bottom to Top),when MADCTL (36h) D7=“0”</td> </tr> <tr> <td rowspan="2">MX</td> <td rowspan="2">Column Adress Order(MX)</td> <td>“1”=Decrement.(Right to Left),when MADCTL(36h)D6=“1”</td> </tr> <tr> <td>“0”=Increment.(Left to Right),when MADCTL(36h)D6=“0”</td> </tr> <tr> <td rowspan="2">MV</td> <td rowspan="2">Row/Column Exchange(MV)</td> <td>“1”=Row/column exchange. when MADCTL (36h) D5=“1”</td> </tr> <tr> <td>“0”=Normal(MV=0).when MADCTL (36h) D5=“0”</td> </tr> <tr> <td rowspan="2">ML</td> <td rowspan="2">Vertical refresh Order(ML)</td> <td>“1”=Decrement.(LCD refresh Bottom to Top, when MADCTL (36h) D4=“1”)</td> </tr> <tr> <td>“0”=Increment.(LCD refresh Top to Bottom), when MADCTL(36h)D4=“0”</td> </tr> <tr> <td rowspan="2">RGB</td> <td rowspan="2">RGB/BGR Order(RGB)</td> <td>“1”=BGR.when MADCTL(36h)D3=“1”</td> </tr> <tr> <td>“0”=RGB.when MADCTL(36h)D3=“0”</td> </tr> <tr> <td rowspan="4">PIXEL_FMT[ 3:0]</td> <td rowspan="4">Interface Color Pixel Format Definition</td> <td>“0011”=12-bit/pixel</td> </tr> <tr> <td>“0101”=16-bit/pixel</td> </tr> <tr> <td>“0110”=18-bit/pixel</td> </tr> <tr> <td></td> </tr> <tr> <td>IDLE_ON</td> <td>Ldle Mode On/Off</td> <td>“1”=On, “0”=Off</td> </tr> <tr> <td>PTL_ON</td> <td>Partial Mode On/Off</td> <td>“1”=On, “0”=Off</td> </tr> <tr> <td>SLPOUT</td> <td>Sleep In/Out</td> <td>“1”=On, “0”=Off</td> </tr> <tr> <td>NORMAL_O N</td> <td>Display Normal Mode On/Off</td> <td>“1”=Normal Display, “0”=Normal Display Off</td> </tr> <tr> <td>SCROLL_ON</td> <td>Vertical Scrolling Status</td> <td>“1”=Scroll On, “0”=Scroll Off</td> </tr> <tr> <td>INVON</td> <td>Inversion Status</td> <td>“1”=On, “0”=Off</td> </tr> <tr> <td>DISPON</td> <td>Display On/Off</td> <td>“1”=On, “0”=Off</td> </tr> </tbody> </table>														Bit	Description	Value	BOOST_ON	Booster Voltage Status	“1”=Booster on, “0”=Booster off	MY	Row Address Order(MY)	“1”=Decrement. (Bottom to Top), when MADCTL (36h) D7=“1”	“0”=Increment.(Bottom to Top),when MADCTL (36h) D7=“0”	MX	Column Adress Order(MX)	“1”=Decrement.(Right to Left),when MADCTL(36h)D6=“1”	“0”=Increment.(Left to Right),when MADCTL(36h)D6=“0”	MV	Row/Column Exchange(MV)	“1”=Row/column exchange. when MADCTL (36h) D5=“1”	“0”=Normal(MV=0).when MADCTL (36h) D5=“0”	ML	Vertical refresh Order(ML)	“1”=Decrement.(LCD refresh Bottom to Top, when MADCTL (36h) D4=“1”)	“0”=Increment.(LCD refresh Top to Bottom), when MADCTL(36h)D4=“0”	RGB	RGB/BGR Order(RGB)	“1”=BGR.when MADCTL(36h)D3=“1”	“0”=RGB.when MADCTL(36h)D3=“0”	PIXEL_FMT[ 3:0]	Interface Color Pixel Format Definition	“0011”=12-bit/pixel	“0101”=16-bit/pixel	“0110”=18-bit/pixel		IDLE_ON	Ldle Mode On/Off	“1”=On, “0”=Off	PTL_ON	Partial Mode On/Off	“1”=On, “0”=Off	SLPOUT	Sleep In/Out	“1”=On, “0”=Off	NORMAL_O N	Display Normal Mode On/Off	“1”=Normal Display, “0”=Normal Display Off	SCROLL_ON	Vertical Scrolling Status	“1”=Scroll On, “0”=Scroll Off	INVON	Inversion Status	“1”=On, “0”=Off	DISPON	Display On/Off	“1”=On, “0”=Off
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MV	Row/Column Exchange(MV)	“1”=Row/column exchange. when MADCTL (36h) D5=“1”																																																																	
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	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">TE_ON</td><td style="padding: 2px;">Tearing effect line on/off</td><td style="padding: 2px;">“1”=On,“0”=Off</td></tr> <tr> <td style="padding: 2px;">TELOM</td><td style="padding: 2px;">Tearing effect line mode</td><td style="padding: 2px;">“0”=mode1,“1”=mode2,</td></tr> <tr> <td style="padding: 2px;">RGB_ON</td><td style="padding: 2px;">RGB interfacee flag</td><td style="padding: 2px;">“0x1A”=RGB ON,”0x00”=RGB OFF</td></tr> </table>	TE_ON	Tearing effect line on/off	“1”=On,“0”=Off	TELOM	Tearing effect line mode	“0”=mode1,“1”=mode2,	RGB_ON	RGB interfacee flag	“0x1A”=RGB ON,”0x00”=RGB OFF																
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Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th style="width: 60%;">Status</th> <th style="width: 40%;">Availability</th> </tr> </thead> <tbody> <tr> <td style="padding: 2px;">Normal Mode on,Idle Mode Off,Sleep Out</td><td style="padding: 2px;">Yes</td></tr> <tr> <td style="padding: 2px;">Normal Mode on,Idle Mode On,Sleep Out</td><td style="padding: 2px;">Yes</td></tr> <tr> <td style="padding: 2px;">Partial Mode on,Idle Mode Off,Sleep Out</td><td style="padding: 2px;">Yes</td></tr> <tr> <td style="padding: 2px;">Partial Mode on,Idle Mode On,Sleep Out</td><td style="padding: 2px;">Yes</td></tr> <tr> <td style="padding: 2px;">Sleep In</td><td style="padding: 2px;">Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes												
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Power on Sequence	0000-0100	0110-0001	0000-0000	0000-0000																						
SW Reset	0xxx-xxx0	0xxx-0001	0000-0000	0000-0000																						
HW Reset	0000-0000	0110-0001	0000-0000	0000-0000																						

### 12.1.5. RDDPM (0Ah)

<b>0AH</b>	<b>Read Display Power Mode</b>																																
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																					
Command	L	R	H	0	0	0	0	1	0	1	0	0AH																					
Parameter1	H	R	H	X	X	X	X	X	X	X	X	X																					
Parameter2	H	R	H	BOOS T_ON	IDLE_ ON	PTL_O N	SLPOU T	NORM AL_O N	DISPO N	0	0	-																					
Description	<table border="1"> <thead> <tr> <th><b>Bit</b></th><th><b>Description</b></th><th><b>Value</b></th></tr> </thead> <tbody> <tr> <td>BOOST_ON</td><td>Booster Voltage Status</td><td>“1”=Booster On “0”Booster Off</td></tr> <tr> <td>IDLE_ON</td><td>Idle mode On/Off</td><td>“1”=Idle mode On “0”=Idle mode Off</td></tr> <tr> <td>PTL_ON</td><td>Partial Mode On/Off</td><td>“1”=Partial Mode On “0”=Partial Mode Off</td></tr> <tr> <td>SLPOUT</td><td>Sleep In/Off</td><td>“1”=Sleep Out “0”=Sleep In</td></tr> <tr> <td>NORMAL_ON</td><td>Display Normal Mode On/Off</td><td>“1”=Normal Display “0”=Partial Display</td></tr> <tr> <td>DISPON</td><td>Display On/Off</td><td>“1”=Display On “0”=Display Off</td></tr> </tbody> </table>												<b>Bit</b>	<b>Description</b>	<b>Value</b>	BOOST_ON	Booster Voltage Status	“1”=Booster On “0”Booster Off	IDLE_ON	Idle mode On/Off	“1”=Idle mode On “0”=Idle mode Off	PTL_ON	Partial Mode On/Off	“1”=Partial Mode On “0”=Partial Mode Off	SLPOUT	Sleep In/Off	“1”=Sleep Out “0”=Sleep In	NORMAL_ON	Display Normal Mode On/Off	“1”=Normal Display “0”=Partial Display	DISPON	Display On/Off	“1”=Display On “0”=Display Off
<b>Bit</b>	<b>Description</b>	<b>Value</b>																															
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<b>Status</b>	<b>Availability</b>																																
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<b>Status</b>	<b>Default Value(D7 to D0)</b>																																
Power On Sequence	0000_1000(08h)																																
SW Reset	0000_1000(08h)																																
HW Reset	0000_1000(08h)																																

### 12.1.6. RDDMADCTL (0Bh)

<b>0BH</b>		Read Display MADCTL																													
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																			
Command	L	R	H	0	0	0	0	1	0	1	1	0BH																			
Parameter1	H	R	H	X	X	X	X	X	X	X	X	X																			
Parameter2	H	R	H	MY	MX	MV	ML	SBGR	0	0	0	-																			
Description	<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>MY</td><td>Page Address Order</td><td>“1”=Decrement, “0”=Increment</td></tr> <tr> <td>MX</td><td>Column Adress Order</td><td>“1”=Decrement, “0”=Increment</td></tr> <tr> <td>MV</td><td>Page/Column Order</td><td>“1”=Row/column exchange (MV=1) “0”=Normal(MV=0)</td></tr> <tr> <td>ML</td><td>Line Address Order</td><td>“1”=LCD Refresh Botton to top “0”=LCD Refresh top to Bottom</td></tr> <tr> <td>SBGR</td><td>RGB/BGR Order</td><td>“1”=BGR, “0”=RGB</td></tr> </tbody> </table>													Bit	Description	Value	MY	Page Address Order	“1”=Decrement, “0”=Increment	MX	Column Adress Order	“1”=Decrement, “0”=Increment	MV	Page/Column Order	“1”=Row/column exchange (MV=1) “0”=Normal(MV=0)	ML	Line Address Order	“1”=LCD Refresh Botton to top “0”=LCD Refresh top to Bottom	SBGR	RGB/BGR Order	“1”=BGR, “0”=RGB
Bit	Description	Value																													
MY	Page Address Order	“1”=Decrement, “0”=Increment																													
MX	Column Adress Order	“1”=Decrement, “0”=Increment																													
MV	Page/Column Order	“1”=Row/column exchange (MV=1) “0”=Normal(MV=0)																													
ML	Line Address Order	“1”=LCD Refresh Botton to top “0”=LCD Refresh top to Bottom																													
SBGR	RGB/BGR Order	“1”=BGR, “0”=RGB																													
Restriction	None																														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes						
Status	Availability																														
Normal Mode on,Idle Mode Off,Sleep Out	Yes																														
Normal Mode on,Idle Mode On,Sleep Out	Yes																														
Partial Mode on,Idle Mode Off,Sleep Out	Yes																														
Partial Mode on,Idle Mode On,Sleep Out	Yes																														
Sleep In	Yes																														
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>8'h08</td></tr> <tr> <td>SW Reset</td><td>8'h08</td></tr> <tr> <td>HW Reset</td><td>8'h08</td></tr> </tbody> </table>													Status	Default Value(D7 to D0)	Power On Sequence	8'h08	SW Reset	8'h08	HW Reset	8'h08										
Status	Default Value(D7 to D0)																														
Power On Sequence	8'h08																														
SW Reset	8'h08																														
HW Reset	8'h08																														

### 12.1.7. RDDCOLMOD (0Ch)

<b>0CH</b>	<b>Read Display Pixel Format</b>																								
	<b>D/CX</b>	<b>RDX</b>	<b>WRX</b>	<b>D7</b>	<b>D6</b>	<b>D5</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>	<b>HEX</b>													
Command	L	R	H	0	0	0	0	1	1	0	0	0	0CH												
Parameter1	H	R	H	X	X	X	X	X	X	X	X	X	X												
Parameter2	H	R	H	VIPF[3:0]				0	IFPF[2:0]			-													
	The 1st Parameter is dummy read.																								
Description	<b>Bit</b>	<b>Description</b>		<b>Value</b>																					
	D7	VIPF3		RGB Interface Color Fomat									0101=16 bit/pixel(1 time data transfer) 0110=18 bit/pixel(1 time data transfer)												
	D6	VIPF2											1110=18 bit/pixel(3 times data transfer)												
	D5	VIPF1											The other=not defined												
	D4	VIPF0											“0” (Not Used)												
	D3	D3																							
	D2	IFPF2											“011”=12 bit/pixel												
	D1	IFPF1											“101”=16 bit/pixel												
	D0	IFPF0											“110”=18 bit/pixel The other=not defined												
Restriction	None																								
Register Availability											<b>Status</b>	<b>Availability</b>													
											Normal Mode on,Idle Mode Off,Sleep Out	Yes													
											Normal Mode on,Idle Mode On,Sleep Out	Yes													
											Partial Mode on,Idle Mode Off,Sleep Out	Yes													
											Partial Mode on,Idle Mode On,Sleep Out	Yes													
											Sleep In	Yes													
Default											<b>Status</b>	<b>Default Value(D7 to D0)</b>													
											Power On Sequence	0110_0110(18bit/pixel)													
											SW Reset	No Change													
											HW Reset	0110_0110(18bit/pixel)													

### 12.1.8. RDDIM (0Dh)

<b>0DH</b>	<b>Read Display Image Mode</b>																								
	<b>D/CX</b>	<b>RDX</b>	<b>WRX</b>	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	L	R	H	0	0	0	0	1	1	0	1	0DH													
Parameter1	H	R	H	X	X	X	X	X	X	X	X	X													
Parameter2	H	R	H	SCROLL_ON	0	INVON	0	0	0	0	0	-													
	The 1st Parameter is dummy read.																								
Description	<table border="1"> <thead> <tr> <th><b>Bit</b></th><th><b>Description</b></th><th><b>Value</b></th></tr> </thead> <tbody> <tr> <td>D7</td><td>Scrolling On/Off</td><td>“1”=Scrolling is On “0”=Scrolling is Off</td></tr> <tr> <td>D5</td><td>Inversion On/Off</td><td>“1”=Inversion is On “0”=Inversion is Off</td></tr> </tbody> </table>													<b>Bit</b>	<b>Description</b>	<b>Value</b>	D7	Scrolling On/Off	“1”=Scrolling is On “0”=Scrolling is Off	D5	Inversion On/Off	“1”=Inversion is On “0”=Inversion is Off			
<b>Bit</b>	<b>Description</b>	<b>Value</b>																							
D7	Scrolling On/Off	“1”=Scrolling is On “0”=Scrolling is Off																							
D5	Inversion On/Off	“1”=Inversion is On “0”=Inversion is Off																							
Restriction	None																								
Register Availability	<table border="1"> <thead> <tr> <th><b>Status</b></th><th><b>Availability</b></th></tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>													<b>Status</b>	<b>Availability</b>	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
<b>Status</b>	<b>Availability</b>																								
Normal Mode on,Idle Mode Off,Sleep Out	Yes																								
Normal Mode on,Idle Mode On,Sleep Out	Yes																								
Partial Mode on,Idle Mode Off,Sleep Out	Yes																								
Partial Mode on,Idle Mode On,Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th><b>Status</b></th><th><b>Default Value(D7 to D0)</b></th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>8'h00</td></tr> <tr> <td>SW Reset</td><td>8'h00</td></tr> <tr> <td>HW Reset</td><td>8'h00</td></tr> </tbody> </table>													<b>Status</b>	<b>Default Value(D7 to D0)</b>	Power On Sequence	8'h00	SW Reset	8'h00	HW Reset	8'h00				
<b>Status</b>	<b>Default Value(D7 to D0)</b>																								
Power On Sequence	8'h00																								
SW Reset	8'h00																								
HW Reset	8'h00																								

### 12.1.9. RDDSM (0Eh)

<b>0EH</b>		Read Display Signal Mode																						
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	L	R	H	0	0	0	0	1	1	1	0	0EH												
Parameter1	H	R	H	X	X	X	X	X	X	X	X	X												
Parameter2	H	R	H	TE_ON	TELOM	0	0	0	0	0	0	-												
Description	The 1st Parameter is dummy read.																							
	<table border="1"> <thead> <tr> <th>Bit</th><th>Description</th><th>Value</th></tr> </thead> <tbody> <tr> <td>D7</td><td>Tearing Effect Line On/Off</td><td>“0”=Off, “1”= On</td></tr> <tr> <td>D6</td><td>Tearing Effect Line Mode</td><td>“0”=Mode1, “1”= Mode2</td></tr> </tbody> </table>												Bit	Description	Value	D7	Tearing Effect Line On/Off	“0”=Off, “1”= On	D6	Tearing Effect Line Mode	“0”=Mode1, “1”= Mode2			
Bit	Description	Value																						
D7	Tearing Effect Line On/Off	“0”=Off, “1”= On																						
D6	Tearing Effect Line Mode	“0”=Mode1, “1”= Mode2																						
Restriction	None																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>												Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode on,Idle Mode Off,Sleep Out	Yes																							
Normal Mode on,Idle Mode On,Sleep Out	Yes																							
Partial Mode on,Idle Mode Off,Sleep Out	Yes																							
Partial Mode on,Idle Mode On,Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th><th>Default Value(D7 to D0)</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>8'h00</td></tr> <tr> <td>SW Reset</td><td>8'h00</td></tr> <tr> <td>HW Reset</td><td>8'h00</td></tr> </tbody> </table>												Status	Default Value(D7 to D0)	Power On Sequence	8'h00	SW Reset	8'h00	HW Reset	8'h00				
Status	Default Value(D7 to D0)																							
Power On Sequence	8'h00																							
SW Reset	8'h00																							
HW Reset	8'h00																							

### 12.1.10. RDDSDR (0Fh)

<b>0FH</b>		Read Display Self-Diagnostic Result																							
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	L	R	H	0	0	0	0	1	1	1	1	0FH													
Parameter1	H	R	H	X	X	X	X	X	X	X	X	X													
Parameter2	H	R	H	SELF_DIAG[3:0]				0	0	0	0	-													
Description	The 1st Parameter is dummy read. If internal function work correctly, send this command will get an inverted result every time.																								
Restriction	None																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode on,Idle Mode Off,Sleep Out	Yes																								
Normal Mode on,Idle Mode On,Sleep Out	Yes																								
Partial Mode on,Idle Mode Off,Sleep Out	Yes																								
Partial Mode on,Idle Mode On,Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>SLPIN</td> </tr> <tr> <td>SW Reset</td> <td>8'h00</td> </tr> <tr> <td>HW Reset</td> <td>8'h00</td> </tr> </tbody> </table>													Status	Default Value(D7 to D0)	Power On Sequence	SLPIN	SW Reset	8'h00	HW Reset	8'h00				
Status	Default Value(D7 to D0)																								
Power On Sequence	SLPIN																								
SW Reset	8'h00																								
HW Reset	8'h00																								

### 12.1.11. SLPIN (10h)

<b>10H</b>		Sleep In																						
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	L	H	R	0	0	0	1	0	0	0	0	10H												
Parameter	No Parameter																							
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode e.g. the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped. MCU interface and memory are still working and the memory keeps it's contents.																							
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120 msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.																							
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes	
Status	Availability																							
Normal Mode on,Idle Mode Off,Sleep Out	Yes																							
Normal Mode on,Idle Mode On,Sleep Out	Yes																							
Partial Mode on,Idle Mode Off,Sleep Out	Yes																							
Partial Mode on,Idle Mode On,Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>SLPIN</td> </tr> <tr> <td>SW Reset</td> <td>SLPIN</td> </tr> <tr> <td>HW Reset</td> <td>SLPIN</td> </tr> </tbody> </table>											Status	Default Value(D7 to D0)	Power On Sequence	SLPIN	SW Reset	SLPIN	HW Reset	SLPIN					
Status	Default Value(D7 to D0)																							
Power On Sequence	SLPIN																							
SW Reset	SLPIN																							
HW Reset	SLPIN																							

### 12.1.12. SLPOUT(11h)

<b>11H</b>		Sleep Out																						
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	L	H	R	0	0	0	1	0	0	0	1	11H												
Parameter	No Parameter																							
Description	This command turns off sleep mode. In this mode e.g. the DC/DC converter is enabled. Internal oscillator is started, and panel scanning is started.																							
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command; this is to allow time for the clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 120 msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out-mode. The display module is doing self-diagnostic function during this 5msec. It will be necessary to wait 120msec after sending Sleep In command ( when in Sleep Out mode ) before Sleep Out command can be sent. This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by HW Reset, Software Reset (01h), Sleep In (10h), or a NMI event trigger.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode on,Idle Mode Off,Sleep Out	Yes																							
Normal Mode on,Idle Mode On,Sleep Out	Yes																							
Partial Mode on,Idle Mode Off,Sleep Out	Yes																							
Partial Mode on,Idle Mode On,Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>SLPOUT</td> </tr> <tr> <td>SW Reset</td> <td>SLPOUT</td> </tr> <tr> <td>HW Reset</td> <td>SLPOUT</td> </tr> </tbody> </table>												Status	Default Value(D7 to D0)	Power On Sequence	SLPOUT	SW Reset	SLPOUT	HW Reset	SLPOUT				
Status	Default Value(D7 to D0)																							
Power On Sequence	SLPOUT																							
SW Reset	SLPOUT																							
HW Reset	SLPOUT																							

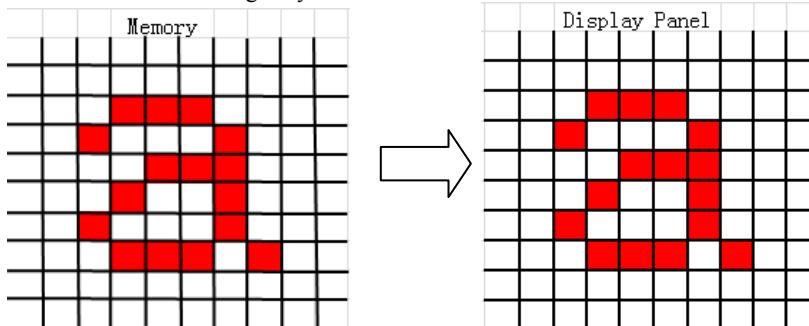
### 12.1.13. PTLON (12h)

12H		Partial Display Mode On																						
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	L	H	R	0	0	0	1	0	0	1	0	12H												
Parameter	No Parameter																							
Description	This command turns on partial mode. The partial mode is described by the Partial Area command (30h). To leave Partial mode, the Normal Display On command (13h) should be written. X=Don't care Note: If a command is written in a frame cycle, the command becomes effective from the next frame.																							
Restriction	This command has no effect during Partial mode is active.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes	
Status	Availability																							
Normal Mode on,Idle Mode Off,Sleep Out	Yes																							
Normal Mode on,Idle Mode On,Sleep Out	Yes																							
Partial Mode on,Idle Mode Off,Sleep Out	Yes																							
Partial Mode on,Idle Mode On,Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal Display On</td> </tr> <tr> <td>SW Reset</td> <td>Normal Display On</td> </tr> <tr> <td>HW Reset</td> <td>Normal Display On</td> </tr> </tbody> </table>											Status	Default Value(D7 to D0)	Power On Sequence	Normal Display On	SW Reset	Normal Display On	HW Reset	Normal Display On					
Status	Default Value(D7 to D0)																							
Power On Sequence	Normal Display On																							
SW Reset	Normal Display On																							
HW Reset	Normal Display On																							

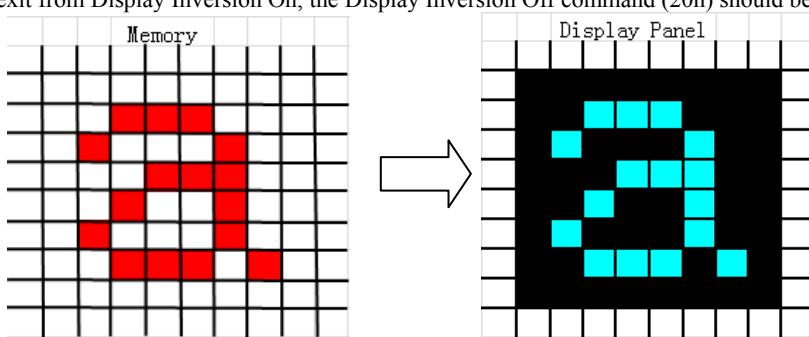
### 12.1.14. NORON (13h)

13H		Normal Display Mode On																						
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	L	H	R	0	0	0	1	0	0	1	1	13H												
Parameter	No Parameter																							
Description	This command returns the display to normal mode. Normal display mode on means Partial mode off and Scroll mode off. Exit from NORON by the Partial mode On command (12h) X=Don't care Note: If a command is written in a frame cycle, the command becomes effective from the next frame.																							
Restriction	This command has no effect when Normal Display mode is active.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes	
Status	Availability																							
Normal Mode on,Idle Mode Off,Sleep Out	Yes																							
Normal Mode on,Idle Mode On,Sleep Out	Yes																							
Partial Mode on,Idle Mode Off,Sleep Out	Yes																							
Partial Mode on,Idle Mode On,Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal Display On</td> </tr> <tr> <td>SW Reset</td> <td>Normal Display On</td> </tr> <tr> <td>HW Reset</td> <td>Normal Display On</td> </tr> </tbody> </table>											Status	Default Value(D7 to D0)	Power On Sequence	Normal Display On	SW Reset	Normal Display On	HW Reset	Normal Display On					
Status	Default Value(D7 to D0)																							
Power On Sequence	Normal Display On																							
SW Reset	Normal Display On																							
HW Reset	Normal Display On																							

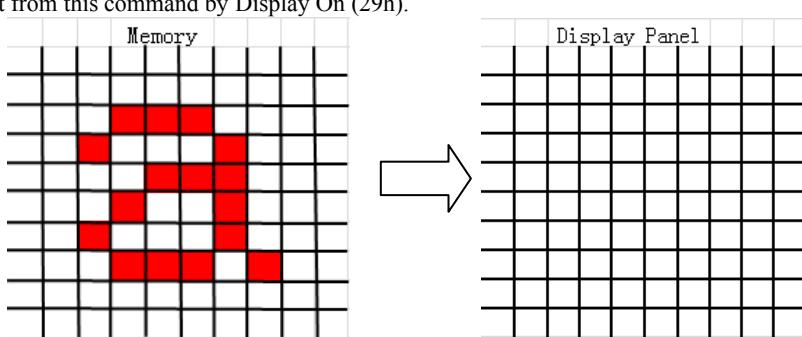
### 12.1.15. INVOFF (20h)

<b>20H</b>		Display Inversion Off																						
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	L	H	R	0	0	1	0	0	0	0	0	20H												
Parameter	No Parameter																							
Description	<p>This command is used to recover from display inversion mode.  This command makes no change of contents of frame memory.  This command does not change any other status.</p> 																							
Restriction	This command has no effect when module is already in inversion off mode.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode on,Idle Mode Off,Sleep Out	Yes																							
Normal Mode on,Idle Mode On,Sleep Out	Yes																							
Partial Mode on,Idle Mode Off,Sleep Out	Yes																							
Partial Mode on,Idle Mode On,Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal Display On</td> </tr> <tr> <td>SW Reset</td> <td>Normal Display On</td> </tr> <tr> <td>HW Reset</td> <td>Normal Display On</td> </tr> </tbody> </table>												Status	Default Value(D7 to D0)	Power On Sequence	Normal Display On	SW Reset	Normal Display On	HW Reset	Normal Display On				
Status	Default Value(D7 to D0)																							
Power On Sequence	Normal Display On																							
SW Reset	Normal Display On																							
HW Reset	Normal Display On																							

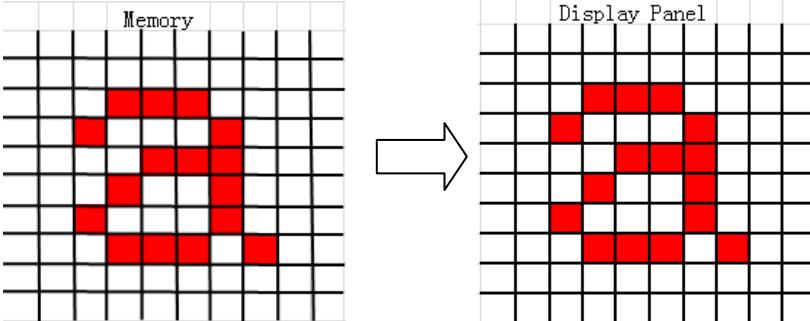
### 12.1.16. INVON (21h)

<b>21H</b>		Display Inversion On																						
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	L	H	R	0	0	1	0	0	0	0	1	21H												
Parameter	No Parameter																							
Description	<p>This command is used to enter into display inversion mode.  This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display.  This command does not change any other status.  To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.</p> 																							
Restriction	This command has no effect when module is already in inversion on mode.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode on,Idle Mode Off,Sleep Out	Yes																							
Normal Mode on,Idle Mode On,Sleep Out	Yes																							
Partial Mode on,Idle Mode Off,Sleep Out	Yes																							
Partial Mode on,Idle Mode On,Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Normal Display On</td> </tr> <tr> <td>SW Reset</td> <td>Normal Display On</td> </tr> <tr> <td>HW Reset</td> <td>Normal Display On</td> </tr> </tbody> </table>												Status	Default Value(D7 to D0)	Power On Sequence	Normal Display On	SW Reset	Normal Display On	HW Reset	Normal Display On				
Status	Default Value(D7 to D0)																							
Power On Sequence	Normal Display On																							
SW Reset	Normal Display On																							
HW Reset	Normal Display On																							

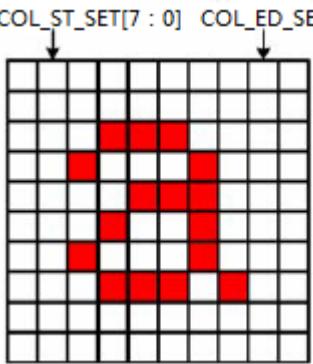
### 12.1.17. DISPOFF (28h)

<b>28H</b>		Display Off																						
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	L	H	R	0	0	1	0	1	0	0	0	28H												
Parameter	No Parameter																							
Description	<p>This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status.</p> <p>There will be no abnormal visible effect on the display.</p> <p>Exit from this command by Display On (29h).</p> 																							
Restriction	This command has no effect when module is already in display off mode.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode on,Idle Mode Off,Sleep Out	Yes																							
Normal Mode on,Idle Mode On,Sleep Out	Yes																							
Partial Mode on,Idle Mode Off,Sleep Out	Yes																							
Partial Mode on,Idle Mode On,Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display Off</td> </tr> <tr> <td>SW Reset</td> <td>Display Off</td> </tr> <tr> <td>HW Reset</td> <td>Display Off</td> </tr> </tbody> </table>												Status	Default Value(D7 to D0)	Power On Sequence	Display Off	SW Reset	Display Off	HW Reset	Display Off				
Status	Default Value(D7 to D0)																							
Power On Sequence	Display Off																							
SW Reset	Display Off																							
HW Reset	Display Off																							

### 12.1.18 DISPON (29h)

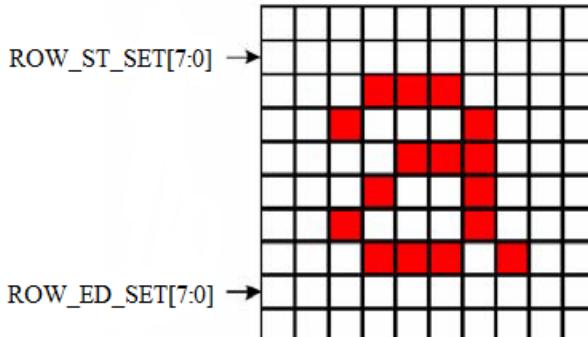
<b>29H</b>		Display On																						
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	L	H	R	0	0	1	0	1	0	0	1	29H												
Parameter	No Parameter																							
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status.																							
																								
Restriction	This command has no effect when module is already in display on mode.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability																							
Normal Mode on,Idle Mode Off,Sleep Out	Yes																							
Normal Mode on,Idle Mode On,Sleep Out	Yes																							
Partial Mode on,Idle Mode Off,Sleep Out	Yes																							
Partial Mode on,Idle Mode On,Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Display On</td> </tr> <tr> <td>SW Reset</td> <td>Display On</td> </tr> <tr> <td>HW Reset</td> <td>Display On</td> </tr> </tbody> </table>												Status	Default Value(D7 to D0)	Power On Sequence	Display On	SW Reset	Display On	HW Reset	Display On				
Status	Default Value(D7 to D0)																							
Power On Sequence	Display On																							
SW Reset	Display On																							
HW Reset	Display On																							

### 12.1.19 CASET (2Ah)

2AH		Column Address Set																					
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command	L	H	R	0	0	1	0	1	0	1	0	2AH											
Parameter1	H	H	R	COL_ST_SET[15:8]									00H										
Parameter2	H	H	R	COL_ST_SET[7:0]									00H										
Parameter3	H	H	R	COL_ED_SET[15:8]									00H										
Parameter4	H	H	R	COL_ED_SET[7:0]									83H										
Description	<p>This command is used to define area of frame memory where MCU can access.  This command makes no change on the other driver status.  The value of COL_ST_SET[7:0] and COL_ED_SET[7:0] are referred when RAMWR command comes.  Each value represents one column line in the Frame Memory.</p> 																						
Restriction	<p>XS[7:0] always must be equal to or less than XE[7:0].  When XS[7:0] or XE[7:0] is greater than maximum row address like below, data of out of range will be ignored.</p> <ol style="list-style-type: none"> <li>1. <b>132x132 memory base(GM='101')</b>  (Parameter range:0 ≤ XS[7:0] ≤ XE[7:0] ≤ 131(0083H)):MV="0"  (Parameter range:0 ≤ XS[7:0] ≤ XE[7:0] ≤ 131(0083H)):MV="1"</li> <li>2. <b>130x130 memory base(GM='100')</b>  (Parameter range:0 ≤ XS[7:0] ≤ XE[7:0] ≤ 129(0081H)):MV="0"  (Parameter range:0 ≤ XS[7:0] ≤ XE[7:0] ≤ 129(0081H)):MV="1"</li> <li>3. <b>128x160 memory base(GM='011')</b>  (Parameter range:0 ≤ XS[7:0] ≤ XE[7:0] ≤ 127(007FH)):MV="0"  (Parameter range:0 ≤ XS[7:0] ≤ XE[7:0] ≤ 159(009FH)):MV="1"</li> <li>4. <b>120x160 memory base(GM='010')</b>  (Parameter range:0 ≤ XS[7:0] ≤ XE[7:0] ≤ 119(0077H)):MV="0"  (Parameter range:0 ≤ XS[7:0] ≤ XE[7:0] ≤ 159(009FH)):MV="1"</li> <li>5. <b>128x128 memory base(GM='001')</b>  (Parameter range:0 ≤ XS[7:0] ≤ XE[7:0] ≤ 127(007FH)):MV="0"  (Parameter range:0 ≤ XS[7:0] ≤ XE[7:0] ≤ 127(007FH)):MV="1"</li> <li>6. <b>132x162 memory base(GM='000')</b>  (Parameter range:0 ≤ XS[7:0] ≤ XE[7:0] ≤ 131(0083H)):MV="0"  (Parameter range:0 ≤ XS[7:0] ≤ XE[7:0] ≤ 127(00A1H)):MV="1"</li> </ol>																						
Register Availability	<table border="1" data-bbox="463 1814 1257 2028"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes
Status	Availability																						
Normal Mode on,Idle Mode Off,Sleep Out	Yes																						
Normal Mode on,Idle Mode On,Sleep Out	Yes																						
Partial Mode on,Idle Mode Off,Sleep Out	Yes																						
Partial Mode on,Idle Mode On,Sleep Out	Yes																						

	Sleep In	Yes
<b>Default</b>		
	<b>Status</b>	<b>Default Value</b>
	(132x132 GM=”101”)	XS[7:0] XE[7:0] EX[7:0](MV=1)
	Power On Sequence	0000h 0083h(131)
	S/W Reset	0000h 0083h(131) 0083h(131)
	H/W Reset	0000h 0083h(131)
	<b>Status</b>	<b>Default Value</b>
	(130x130 GM=”100”)	XS[7:0] XE[7:0] EX[7:0](MV=1)
	Power On Sequence	0000h 0081h(129)
	S/W Reset	0000h 0081h(129) 0081h(129)
	H/W Reset	0000h 0081h(129)
	<b>Status</b>	<b>Default Value</b>
	(128x160 GM=”011”)	XS[7:0] XE[7:0] EX[7:0](MV=1)
	Power On Sequence	0000h 007Fh(127)
	S/W Reset	0000h 007Fh(127) 009Fh(159)
	H/W Reset	0000h 007Fh(127)
	<b>Status</b>	<b>Default Value</b>
	(120x160 GM=”010”)	XS[7:0] XE[7:0] EX[7:0](MV=1)
	Power On Sequence	0000h 0077h(119)
	S/W Reset	0000h 007Fh(119) 009Fh(159)
	H/W Reset	0000h 0077h(119)
	<b>Status</b>	<b>Default Value</b>
	(128x128 GM=”001”)	XS[7:0] XE[7:0] EX[7:0](MV=1)
	Power On Sequence	0000h 007Fh(127)
	S/W Reset	0000h 007Fh(127) 009Fh(127)
	H/W Reset	0000h 0077h(119)
	<b>Status</b>	<b>Default Value</b>
	(132x162 GM=”000”)	XS[7:0] XE[7:0] EX[7:0](MV=1)
	Power On Sequence	0000h 0083h(131)
	S/W Reset	0000h 0083h(131) 00A1h(161)
	HW Reset	0000h 0083H(131)

### 12.1.20 RASET (2Bh)

<b>2BH</b>	<b>Row Address Set</b>																					
	<b>D/CX</b>	<b>RDX</b>	<b>WRX</b>	<b>D7</b>	<b>D6</b>	<b>D5</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>	<b>HEX</b>										
Command	L	H	R	0	0	1	0	1	0	1	1	1	2BH									
Parameter1	H	H	R	ROW_ST_SET[15:8]									00H									
Parameter2	H	H	R	ROW_ST_SET[7:0]									00H									
Parameter3	H	H	R	ROW_ED_SET[15:8]									00H									
Parameter4	H	H	R	ROW_ED_SET[7:0]									A1H									
Description	<p>This command is used to define area of frame memory where MCU can access.  This command makes no change on the other driver status.  The value of ROW_ST_SET[7:0] and ROW_ED_SET[7:0] are referred when RAMWR command comes.  Each value represents one Page line in the Frame Memory.</p> 																					
Restriction	<p>YS[7:0] always must be equal to or less than EP[7:0].  When YS[7:0] or YE[7:0] is greater than maximum row address like below,data of out of range will be ignored.</p> <p><b>132x132 memory base(GM='101')</b>  (Parameter range:0 ≤ YS[7:0] ≤ YE[7:0] ≤ 131(0083H)):MV="0"  (Parameter range:0 ≤ YS[7:0] ≤ YE[7:0] ≤ 131(0083H)):MV="1"</p> <p><b>130x130 memory base(GM='100')</b>  (Parameter range:0 ≤ YS[7:0] ≤ YE[7:0] ≤ 129(0081H)):MV="0"  (Parameter range:0 ≤ YS[7:0] ≤ YE[7:0] ≤ 129(0081H)):MV="1"</p> <p><b>128x160 memory base(GM='011')</b>  (Parameter range:0 ≤ YS[7:0] ≤ YE[7:0] ≤ 159(009FH)):MV="0"  (Parameter range:0 ≤ YS[7:0] ≤ YE[7:0] ≤ 127(009FH)):MV="1"</p> <p><b>120x160 memory base(GM='010')</b>  (Parameter range:0 ≤ YS[7:0] ≤ YE[7:0] ≤ 159(009FH)):MV="0"  (Parameter range:0 ≤ YS[7:0] ≤ YE[7:0] ≤ 119(007FH)):MV="1"</p> <p><b>128x128 memory base(GM='001')</b>  (Parameter range:0 ≤ YS[7:0] ≤ YE[7:0] ≤ 127(007FH)):MV="0"  (Parameter range:0 ≤ YS[7:0] ≤ YE[7:0] ≤ 127(007FH)):MV="1"</p> <p><b>132x162 memory base(GM='000')</b>  (Parameter range:0 ≤ YS[7:0] ≤ YE[7:0] ≤ 161(00A1H)):MV="0"  (Parameter range:0 ≤ YS[7:0] ≤ YE[7:0] ≤ 131(0083H)):MV="1"</p>																					
Register Availability	<table border="1"> <thead> <tr> <th><b>Status</b></th> <th><b>Availability</b></th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> </tbody> </table>													<b>Status</b>	<b>Availability</b>	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	
<b>Status</b>	<b>Availability</b>																					
Normal Mode on,Idle Mode Off,Sleep Out	Yes																					
Normal Mode on,Idle Mode On,Sleep Out	Yes																					
Partial Mode on,Idle Mode Off,Sleep Out	Yes																					

		Partial Mode on,Idle Mode On,Sleep Out	Yes	
		Sleep In	Yes	
Default	<b>Status</b>	<b>Default Value</b>		
	(132x132 GM="101")	YS[7:0]	YE[7:0]	YX[7:0](MV=1)
	Power On Sequence	0000h	83h(131)	
	S/W Reset	0000h	83h(131)	83h(131)
	H/W Reset	0000h	83h(131)	
	<b>Status</b>	<b>Default Value</b>		
	(130x130 GM="100")	YS[7:0]	YE[7:0]	YX[7:0](MV=1)
	Power On Sequence	0000h	81h(129)	
	S/W Reset	0000h	81h(129)	81h(129)
	H/W Reset	0000h	81h(129)	
	<b>Status</b>	<b>Default Value</b>		
	(128x160 GM="011")	YS[7:0]	YE[7:0]	YX[7:0](MV=1)
	Power On Sequence	00h	9Fh(159)	
	S/W Reset	00h	9Fh(159)	7Fh(127)
	H/W Reset	00h	9Fh(159)	
	<b>Status</b>	<b>Default Value</b>		
(120x160 GM="010")	YS[7:0]	YE[7:0]	YX[7:0](MV=1)	
Power On Sequence	00h	9Fh(159)		
S/W Reset	00h	9Fh(159)	77h(119)	
H/W Reset	00h	9Fh(159)		
<b>Status</b>	<b>Default Value</b>			
(128x128 GM="001")	YS[7:0]	YE[7:0]	YX[7:0](MV=1)	
Power On Sequence	00h	7Fh(127)		
S/W Reset	00h	7Fh(127)	7Fh(127)	
H/W Reset	00h	7Fh(127)		
<b>Status</b>	<b>Default Value</b>			
(132x162 GM="000")	YS[7:0]	YE[7:0]	YX[7:0](MV=1)	
Power On Sequence	00h	A1h(161)		
S/W Reset	00h	A1h(161)	83h(131)	
HW Reset	00h	A1h(161)		

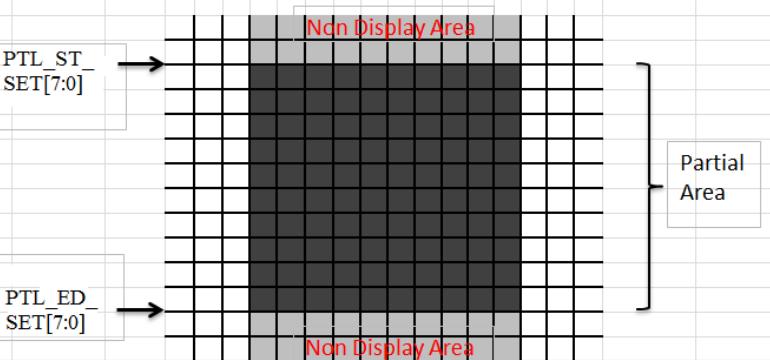
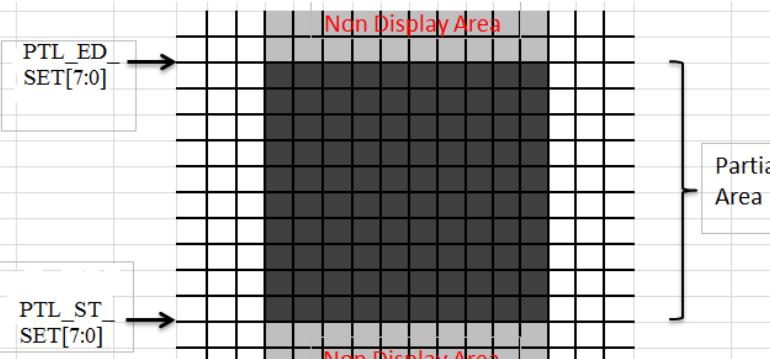
### 12.1.21 RAMWR (2Ch)

2CH		Memory Write																							
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	L	H	R	0	0	1	0	1	1	0	0	2CH													
1st Parameter	H	H	R	D[7:0]								-													
	H	H	R	D[7:0]								-													
Nth Parameter	H	H	R	D[7:0]								-													
Description	This command is used to transfer data from MCU to frame memory. This command makes no change to the other driver status. When this command is accepted, the column register and the page register are reset to the Start Column/Start Page positions. The Start Column /Start Page positions are different in accordance with MADCTL setting. Then D[7:0] is stored in frame memory and the column refister and the row register incremented. Sending any other command can stop frame Write.																								
Restriction	In all color modes, there is no restriction on length of parameters. <b>1. 132x132 memory base (GM="101")</b> 132x132x18-bit memory can be written by this command. Memory range(0000h,0000h)->(0083h,083h) <b>2. 130x130 memory base (GM="100")</b> 130x130x18-bit memory can be written by this command. Memory range(0000h,0000h)->(0081h,081h) <b>3. 128x160 memory base (GM="011")</b> 128x160x18-bit memory can be written by this command. Memory range(0000h,0000h)->(007Fh,09Fh) <b>4. 120x160 memory base (GM="010")</b> 120x160x18-bit memory can be written by this command. Memory range(0000h,0000h)->(0077h,09Fh) <b>5. 128x128 memory base (GM="001")</b> 128x128x18-bit memory can be written by this command. Memory range(0000h,0000h)->(007Fh,007Fh) <b>6. 132x162 memory base (GM="000")</b> 132x162x18-bit memory can be written by this command. Memory range(0000h,0000h)->(0083h,00A1h)																								
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Status	Default Value(D7 to D0)																								
Power On Sequence	Contents of memory is set randomly																								
SW Reset	Contents of memory is not cleared																								
HW Reset	Contents of memory is not cleared																								

### 12.1.22 RAMRD (2Eh)

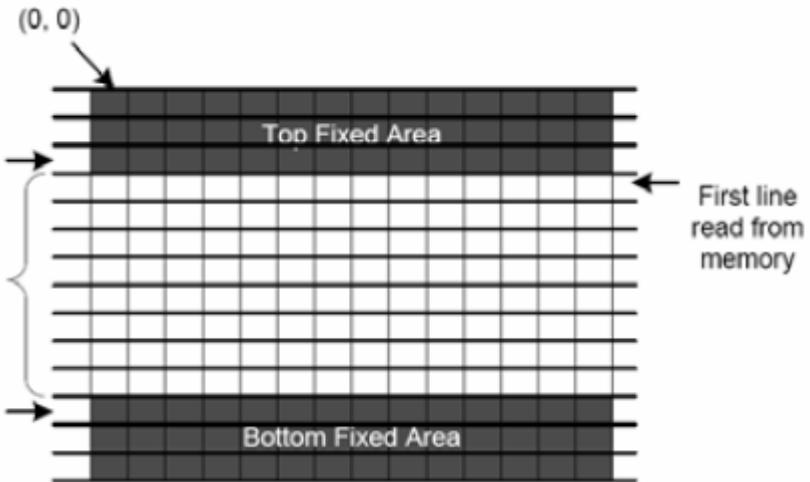
<b>2EH</b>		<b>Memory Read</b>																							
		D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	L	R	H	0	0	1	0	1	1	1	1	0	2EH												
1st Parameter	H	R	H										-												
	H	H	R										-												
Nth Parameter	H	H	R										-												
Description	This command is used to transfer data from frame memory to MCU. This command makes no change to other driver status. When this command is accepted, the column register and then row register are reset to the Start Column/Start Row positions. The Start Column/Start Row positions are different in accordance with MADCTL setting. Then D[7:0] is read back from the frame memory and the column register and the register incremented. Frame Read can be stopped by sending any other command. Display Data Format for color coding (18 bit cases), when there is used 8,9,16 or 18 data line for image data.																								
Restriction	In all color modes, the Frame Read is always 24 bit so there is no restriction on length of parameters. Note: Memory Read is only possible via the Parallel Interface.																								
Register Availability	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
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Status	Default Value(D7 to D0)																								
Power On Sequence	Contents of memory is set randomly																								
SW Reset	Contents of memory is not cleared																								
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### 12.1.23 PTLAR(30h)

<b>30H</b>		Partial Area											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	L	H	R	0	0	1	1	0	0	0	0	30H	
Parameter1	H	H	R	PTL_ST_SET[15:8]									00H
Parameter2	H	H	R	PTL_ST_SET[7:0]									00H
Parameter3	H	H	R	PTL_ED_SET[15:8]									00H
Parameter4	H	H	R	PTL_ED_SET[7:0]									a1H
Description	<p>This command defines the partial mode's display area. There are 4 parameters associated with this command, the first defines the Start Row(PSL) and the second the End Row(PEL), as illustrated in the figure below. PSL and PEL refer to the Frame Memory Line Pointer.</p> <p>If End Row&gt;Start Row when MADCTL B4=0:</p>  <p>If End Row&gt;Start Row when MADCTL ML=1:</p>  <p>If End Row&lt;Start Row when MADCTL ML=0:</p>												

	<p>If End Row&lt;Start Row when MADCTL ML=1:</p>																																															
	<p>If End Row=Start Row then the Partial Area will be one row deep.</p>																																															
Restriction	No Restriction																																															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes																																			
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HW Reset	00h	83h	81h	9Fh	9Fh	7Fh	A1h																																									

### 12.1.24 SCRLAR (33h)

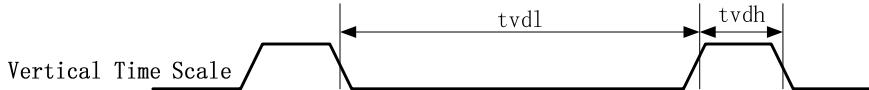
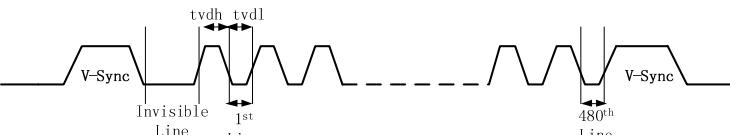
33H	Scroll Area											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	0	0	1	1	0	0	1	1	33H
Parameter1	H	H	R	00								
Parameter2	H	H	R	TFA[7:0]								
Parameter3	H	H	R	00								
Parameter4	H	H	R	VSA[7:0]								
Description	<p>This command defines the Vertical Scrolling Area of the display.  When MADCTL ML=0  The 1st &amp;2nd parameter TFA[7:0]describes the Top Fixed Area (in No.of lines from TOP of the Frame Memory and Display).  The 3rd &amp;4th parameter VSA[7:0]describes the height of the Vertical Scrolling Area(in No.of lines of the Frame Memory[ not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the bottom most line of the Top Fixed Area.</p> <p>TFA, VSA refer to the Frame Memory Line Point.</p>  <p>The diagram illustrates the frame memory structure. It shows a grid of horizontal lines representing memory lines. At the top, there is a dark grey horizontal bar labeled "Top Fixed Area". Below this is a white area with several horizontal lines. A bracket on the left indicates the height of this white area. An arrow points to the first line in this area with the label "First line read from memory". At the bottom, there is another dark grey horizontal bar labeled "Bottom Fixed Area". The space between the "Top Fixed Area" and the "Bottom Fixed Area" is the "Vertical Scrolling Area".</p> <p>When MADCTL ML=1  The 1st &amp;2nd parameter TFA[7:0] describes the Top Fixed Area (in No.of lines from Bottom of the Frame Memory and Display).  The 3rd &amp;4th parameter VSA[7:0] describes the height of the Vertical Sxrolling Area (in No.of lines of the Frame Memory [not the display] from the Vertical Scrolling Start Address). The first line read from Frame Memory appears immediately after the top most line of the Top Fixed Area.</p>											

Restriction	<p>The condition is <math>(TFA+VSA+BFA)=128</math> in 128RGBx128(GM="001")      The condition is <math>(TFA+VSA+BFA)=130</math> in 130RGBx130(GM="100")      The condition is <math>(TFA+VSA+BFA)=132</math> in 132RGBx132(GM="101")      The condition is <math>(TFA+VSA+BFA)=160</math> in 128RGBx160(GM="011") or 120 RGB x 160 (GM="010")      The condition is <math>(TFA+VSA+BFA)=162</math> in 132RGBx162(GM="000")      Otherwise Scrolling mode is undefined.      In Vertical Scrol Mode,MADCTL parameter MV should be set to "0"      this affects the Frame memory Write.</p>																																															
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes																																			
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HW Reset	00h	83h	81h	A0h	A0h	80h	A2h																																									

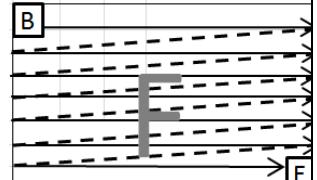
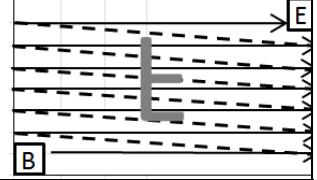
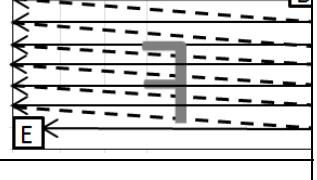
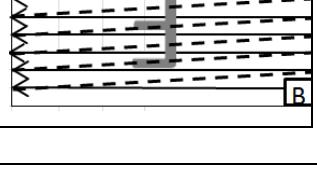
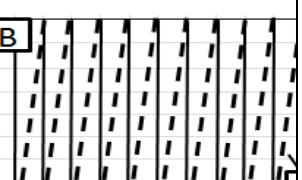
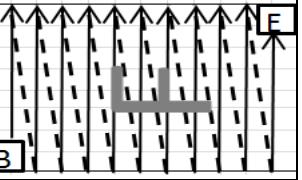
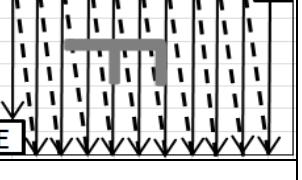
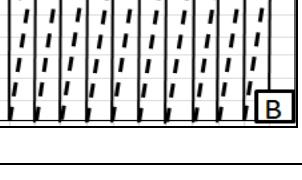
### 12.1.25 TEOFF (34h)

<b>34H</b>		Tearing Effect Line Off																						
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	L	H	R	0	0	1	1	0	1	0	0	34H												
Parameter	No Parameter																							
Description	This command is used to turn OFF (Active Low) the Tearing Effect output single from the TE signal line.																							
Restriction	This command has no effect when Tearing Effect output is already OFF.																							
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
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Partial Mode on,Idle Mode On,Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>OFF</td> </tr> <tr> <td>SW Reset</td> <td>OFF</td> </tr> <tr> <td>HW Reset</td> <td>OFF</td> </tr> </tbody> </table>												Status	Default Value(D7 to D0)	Power On Sequence	OFF	SW Reset	OFF	HW Reset	OFF				
Status	Default Value(D7 to D0)																							
Power On Sequence	OFF																							
SW Reset	OFF																							
HW Reset	OFF																							

### 12.1.26 TEON (35h)

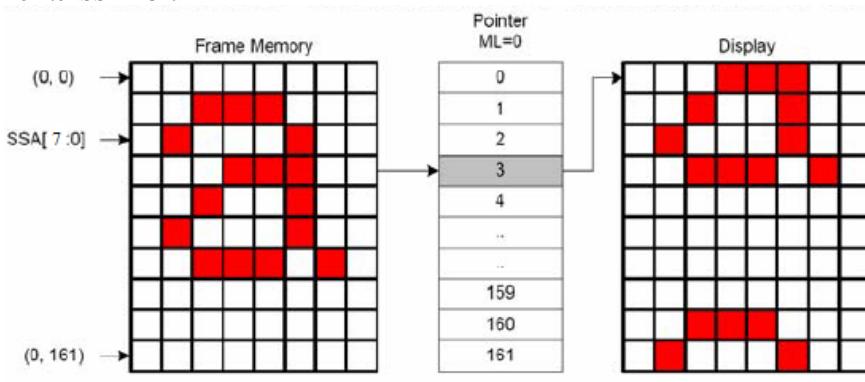
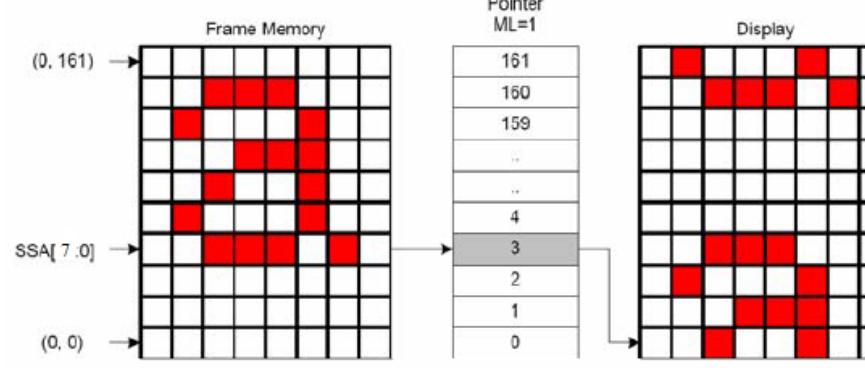
<b>35H</b>		Tearing Effect Line On																							
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	L	H	R	0	0	1	1	0	1	0	1	35H													
Parameter	H	H	R	0	0	0	0	0	0	0	TELOM	00H													
Description	<p>This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by charging MADCTL bit ML.</p> <p>The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care).</p> <p>When TELOM=0:</p> <p>The Tearing Effect Output line consists of V-Blanking information only:</p>  <p>When TELOM =1:</p> <p>The Tearing Effect Output line consists of both V-Blanking and H-Blanking information:</p>  <p>Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active LOW. Display Data Format for color coding (18 bit cases), when there is used 8,9,16 or 18 data line for image data.</p>																								
Restriction	This command has no effect when Tearing Effect output is already ON.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
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Partial Mode on,Idle Mode On,Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Tearing effect off &amp; M=0</td> </tr> <tr> <td>SW Reset</td> <td>Tearing effect off &amp; M=0</td> </tr> <tr> <td>HW Reset</td> <td>Tearing effect off &amp; M=0</td> </tr> </tbody> </table>													Status	Default Value(D7 to D0)	Power On Sequence	Tearing effect off & M=0	SW Reset	Tearing effect off & M=0	HW Reset	Tearing effect off & M=0				
Status	Default Value(D7 to D0)																								
Power On Sequence	Tearing effect off & M=0																								
SW Reset	Tearing effect off & M=0																								
HW Reset	Tearing effect off & M=0																								

### 12.1.27 MADCTR (36h)

<b>36H</b>	<b>Memory Data Access Control</b>																											
	<b>D/CX</b>	<b>RDX</b>	<b>WRX</b>	<b>D7</b>	<b>D6</b>	<b>D5</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>	<b>HEX</b>																
Command	L	H	R	0	0	1	1	0	1	1	0	36H																
Parameter	H	H	R	MY	MX	MV	ML	RGB	0	0	0	00H																
	This command defines read/write scanning direction of frame memory. This command makes no change on the other driver status. Bit Assignment																											
	<table border="1"> <thead> <tr> <th><b>Bit</b></th><th><b>Description</b></th><th><b>Value</b></th></tr> </thead> <tbody> <tr> <td>MY</td><td>Row Address Order</td><td rowspan="3">These 3 bits controls MPU to memory write/read direction.</td></tr> <tr> <td>MX</td><td>Column Address Order</td></tr> <tr> <td>MV</td><td>Page/Column Selection</td></tr> <tr> <td>ML</td><td>Vertical Order</td><td>LCD Vertical refresh direction control</td></tr> <tr> <td>RGB</td><td>RGB/BGR Order</td><td>Color selector switch control 0=RGB color filter panel 1=BGR color filter panel</td></tr> </tbody> </table>												<b>Bit</b>	<b>Description</b>	<b>Value</b>	MY	Row Address Order	These 3 bits controls MPU to memory write/read direction.	MX	Column Address Order	MV	Page/Column Selection	ML	Vertical Order	LCD Vertical refresh direction control	RGB	RGB/BGR Order	Color selector switch control 0=RGB color filter panel 1=BGR color filter panel
<b>Bit</b>	<b>Description</b>	<b>Value</b>																										
MY	Row Address Order	These 3 bits controls MPU to memory write/read direction.																										
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ML	Vertical Order	LCD Vertical refresh direction control																										
RGB	RGB/BGR Order	Color selector switch control 0=RGB color filter panel 1=BGR color filter panel																										
Description	<b>B</b> <b>5</b>	<b>B</b> <b>6</b>	<b>B</b> <b>7</b>	<b>Image in Frame Memory</b>																								
	0	0	0																									
	0	0	1																									
	0	1	0																									
	0	1	1																									
	<b>B</b> <b>5</b>	<b>B</b> <b>6</b>	<b>B</b> <b>7</b>	<b>Image in Frame Memory</b>																								
	1	0	0																									
	1	0	1																									
	1	1	0																									
	1	1	1																									

	<p style="text-align: center;">B3 = 0</p> <p style="text-align: center;">B3 = 1</p>												
Restriction													
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th style="text-align: center; padding: 2px;">Status</th> <th style="text-align: center; padding: 2px;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">Normal Mode on,Idle Mode Off,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Normal Mode on,Idle Mode On,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode on,Idle Mode Off,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode on,Idle Mode On,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Sleep In</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode on,Idle Mode Off,Sleep Out	Yes												
Normal Mode on,Idle Mode On,Sleep Out	Yes												
Partial Mode on,Idle Mode Off,Sleep Out	Yes												
Partial Mode on,Idle Mode On,Sleep Out	Yes												
Sleep In	Yes												
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th style="text-align: center; padding: 2px;">Status</th> <th style="text-align: center; padding: 2px;">Default Value</th> </tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">Power On Sequence</td> <td style="text-align: center; padding: 2px;">08H</td> </tr> <tr> <td style="text-align: center; padding: 2px;">SW Reset</td> <td style="text-align: center; padding: 2px;">08H</td> </tr> <tr> <td style="text-align: center; padding: 2px;">HW Reset</td> <td style="text-align: center; padding: 2px;">08H</td> </tr> </tbody> </table>	Status	Default Value	Power On Sequence	08H	SW Reset	08H	HW Reset	08H				
Status	Default Value												
Power On Sequence	08H												
SW Reset	08H												
HW Reset	08H												

### 12.1.28 VSCSAD (37h)

<b>37H</b>	<b>Vertical Scroll Start Address of RAM</b>																					
	<b>D/CX</b>	<b>RDX</b>	<b>WRX</b>	<b>D7</b>	<b>D6</b>	<b>D5</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>	<b>HEX</b>										
Command	L	H	R	0	0	1	1	0	1	1	1	37H										
Parameter1	H	H	R	00									00H									
Parameter2	H	H	R	SSA[7:0]									00H									
Description	<p>This command is used together with Vertical Scrolling Definition(33h). These two command describe the scrolling area and scrolling mode.</p> <p>The Vertical Scrolling Start Address command has one parameter which describes the address of the line in the Frame Memory that will be written as the first line after the last line of the Top Fixed Area on the display as illustrated below.</p> <p>This command Start the scrolling.</p> <p>When MADCTL ML=0  Example: GM=000,132RGBx162  When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=162 and Vertical Scrolling Pointer SSA="3".</p>  <p>When MADCTL ML=1  Example: GM=000,132RGBx162  When Top Fixed Area=Bottom Fixed Area=00, Vertical Scrolling Area=162 and SSA="3".</p>  <p>Note:  When new Pointer position and Picture Data are sent, the result on the display will happen at the next Panel Scan to avoid tearing effect. SSA refers to the Frame Memory scan address.  When new Pointer position and Picture Data, internal system works as 128x128 and maximum scan address becomes 127 internal of 161.</p>																					
Restriction																						
Register Availability	<table border="1" style="width: 100%; text-align: center;"> <tr> <td style="width: 50%;"></td> <td><b>Status</b></td> <td><b>Availability</b></td> </tr> </table>														<b>Status</b>	<b>Availability</b>						
	<b>Status</b>	<b>Availability</b>																				

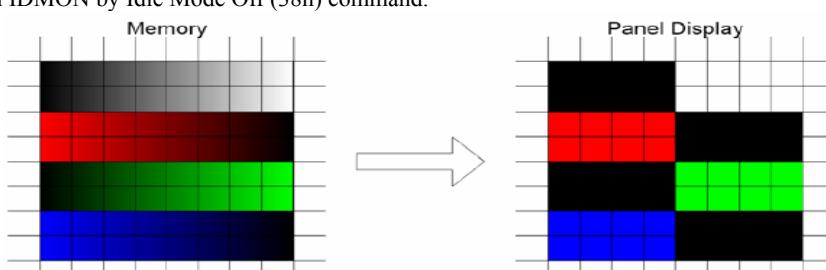
## NV3023A—132RGB x162 dot, 262k-color TFT LCD Single-Chip Driver

		Normal Mode on,Idle Mode Off,Sleep Out	Yes
		Normal Mode on,Idle Mode On,Sleep Out	Yes
		Partial Mode on,Idle Mode Off,Sleep Out	Yes
		Partial Mode on,Idle Mode On,Sleep Out	Yes
		Sleep In	Yes
Default		Status	Default Value
		Power On Sequence	8'h00
		SW Reset	8'h00
		HW Reset	8'h00

### 12.1.29 IDMOFF (38h)

<b>38H</b>		<b>Idle Mode Off</b>																						
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	L	H	R	0	0	1	1	1	0	0	0	38H												
Parameter	No Parameter																							
Description	This command is used to recover from Idle mode on. There will be no abnormal visible effect on the display mode change transition. In the Idle off mode 1, LCD can display maximum 4096, 65k, 262k colors. 2, Normal frame frequency is applied.																							
Restriction	This command has no effect when module is already in Idle off mode.																							
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;"><b>Status</b></th> <th style="text-align: center;"><b>Availability</b></th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td>Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>												<b>Status</b>	<b>Availability</b>	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
<b>Status</b>	<b>Availability</b>																							
Normal Mode on,Idle Mode Off,Sleep Out	Yes																							
Normal Mode on,Idle Mode On,Sleep Out	Yes																							
Partial Mode on,Idle Mode Off,Sleep Out	Yes																							
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Sleep In	Yes																							
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;"><b>Status</b></th> <th style="text-align: center;"><b>Default Value(D7 to D0)</b></th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td style="text-align: center;">Idle Mode Off</td> </tr> <tr> <td>SW Reset</td> <td style="text-align: center;">Idle Mode Off</td> </tr> <tr> <td>HW Reset</td> <td style="text-align: center;">Idle Mode Off</td> </tr> </tbody> </table>												<b>Status</b>	<b>Default Value(D7 to D0)</b>	Power On Sequence	Idle Mode Off	SW Reset	Idle Mode Off	HW Reset	Idle Mode Off				
<b>Status</b>	<b>Default Value(D7 to D0)</b>																							
Power On Sequence	Idle Mode Off																							
SW Reset	Idle Mode Off																							
HW Reset	Idle Mode Off																							

### 12.1.30 IDMON (39h)

<b>39H</b>		Idle Mode On																																															
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																					
Command	L	H	R	0	0	1	1	1	0	0	1	39H																																					
Parameter	No Parameter																																																
Description	<p>This command is used to enter into Idle mode on.          There will be no abnormal visible effect on the display mode change transition.          In the Idle mode.          Color expression is reduced. The primary and the secondary colors using MSB of each R,G and B in the Frame Memory, 8 color depth data is displayed.          8-Color mode frame frequency is applied.          Exit from IDMON by Idle Mode Off (38h) command.</p>  <table border="1"> <thead> <tr> <th>Reduced Color</th> <th>R[5:0]</th> <th>G[5:0]</th> <th>B[5:0]</th> </tr> </thead> <tbody> <tr> <td>Black</td> <td>0XXXX</td> <td>0XXXX</td> <td>0XXXX</td> </tr> <tr> <td>Blue</td> <td>0XXXX</td> <td>0XXXX</td> <td>1XXXX</td> </tr> <tr> <td>Red</td> <td>1XXXX</td> <td>0XXXX</td> <td>0XXXX</td> </tr> <tr> <td>Magenta</td> <td>1XXXX</td> <td>0XXXX</td> <td>1XXXX</td> </tr> <tr> <td>Green</td> <td>0XXXX</td> <td>1XXXX</td> <td>0XXXX</td> </tr> <tr> <td>Cyan</td> <td>0XXXX</td> <td>1XXXX</td> <td>1XXXX</td> </tr> <tr> <td>Yellow</td> <td>1XXXX</td> <td>1XXXX</td> <td>0XXXX</td> </tr> <tr> <td>White</td> <td>1XXXX</td> <td>1XXXX</td> <td>1XXXX</td> </tr> </tbody> </table>													Reduced Color	R[5:0]	G[5:0]	B[5:0]	Black	0XXXX	0XXXX	0XXXX	Blue	0XXXX	0XXXX	1XXXX	Red	1XXXX	0XXXX	0XXXX	Magenta	1XXXX	0XXXX	1XXXX	Green	0XXXX	1XXXX	0XXXX	Cyan	0XXXX	1XXXX	1XXXX	Yellow	1XXXX	1XXXX	0XXXX	White	1XXXX	1XXXX	1XXXX
Reduced Color	R[5:0]	G[5:0]	B[5:0]																																														
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Magenta	1XXXX	0XXXX	1XXXX																																														
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Cyan	0XXXX	1XXXX	1XXXX																																														
Yellow	1XXXX	1XXXX	0XXXX																																														
White	1XXXX	1XXXX	1XXXX																																														
Restriction	This command has no effect when module is already in idle on mode.																																																
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes																								
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Status	Default Value(D7 to D0)																																																
Power On Sequence	Idle Mode On																																																
SW Reset	Idle Mode On																																																
HW Reset	Idle Mode On																																																

### 12.1.31 COLMOD (3Ah)

<b>3AH</b>		Interface Color Mode Set																									
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	L	H	R	0	0	1	1	1	0	1	0	3AH															
Parameter	H	H	R	VIPF[3:0]				0	IFPF[2:0]			66H															
Description	This command is used to define the format of RGB picture data, which is to be transferred via the MCU interface. The formats are shown in the table:																										
	<b>Bit</b>	<b>Description</b>		<b>Value</b>																							
	VIPF3	RGB Interface Color Format		"0101"=16 bit/pixel(1 time data transfer) "0110"=18 bit/pixel(1 time data transfer) "1110"=18 bit/pixel(3 time data transfer) The others=not defined																							
	VIPF2																										
	VIPF1																										
	VIPF0																										
	D3			"0"(Not Used)																							
	IFPF2	Control Interface Color Format		"011"=12 bit/pixel "101"=16 bit/pixel "110"=18 bit/pixel The others=not defined																							
	IFPF1																										
	IFPF0																										
Note: 1. In 12-bits /Pixel, 16-bits/Pixel mode, the LUT is applied to transfer data into the Frame Memory. 2. When VIPF[3:0]=1110, 6-bits data width of 3-times transfer is used to transmin 1 pixel data with the 18-bits color depth information.																											
Restriction	This command has no effect when module is already in Idle off mode.																										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes		
Status	Availability																										
Normal Mode on,Idle Mode Off,Sleep Out	Yes																										
Normal Mode on,Idle Mode On,Sleep Out	Yes																										
Partial Mode on,Idle Mode Off,Sleep Out	Yes																										
Partial Mode on,Idle Mode On,Sleep Out	Yes																										
Sleep In	Yes																										
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h66</td> </tr> <tr> <td>SW Reset</td> <td>8'h66</td> </tr> <tr> <td>HW Reset</td> <td>8'h66</td> </tr> </tbody> </table>													Status	Default Value(D7 to D0)	Power On Sequence	8'h66	SW Reset	8'h66	HW Reset	8'h66						
Status	Default Value(D7 to D0)																										
Power On Sequence	8'h66																										
SW Reset	8'h66																										
HW Reset	8'h66																										

### 12.1.32 RDID1 (DAh)

DAH	Read ID1 Value																								
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	L	H	R	1	1	0	1	1	0	1	0	DAH													
Parameter1	H	R	H	X	X	X	X	X	X	X	X	X													
Parameter2	H	R	H	SYS_ID1[7:0]									33H												
Description	The 1st Parameter is dummy read. This read byte return 8-bit LCD module's ID. The parameter(SYS_ID7- SYS_ID0): LCD module manufacturer ID																								
Restriction	Should set “FF=A5” before configure this registers																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
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Partial Mode on,Idle Mode Off,Sleep Out	Yes																								
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Sleep In	Yes																								
<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h33</td> </tr> <tr> <td>SW Reset</td> <td>8'h33</td> </tr> <tr> <td>HW Reset</td> <td>8'h33</td> </tr> </tbody> </table>													Status	Default Value(D7 to D0)	Power On Sequence	8'h33	SW Reset	8'h33	HW Reset	8'h33					
Status	Default Value(D7 to D0)																								
Power On Sequence	8'h33																								
SW Reset	8'h33																								
HW Reset	8'h33																								

### 12.1.33 RDID2 (DBh)

DBH	Read ID2 Value																								
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	L	H	R	1	1	0	1	1	0	1	1	DBH													
Parameter1	H	R	H	X	X	X	X	X	X	X	X	X													
Parameter2	H	R	H	SYS_ID2[7:0]									30H												
Description	The 1st Parameter is dummy read. This read byte return 8-bit LCD module's ID.																								
Restriction	Should set "FF=A5" before configure this registers																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode on,Idle Mode Off,Sleep Out	Yes																								
Normal Mode on,Idle Mode On,Sleep Out	Yes																								
Partial Mode on,Idle Mode Off,Sleep Out	Yes																								
Partial Mode on,Idle Mode On,Sleep Out	Yes																								
Sleep In	Yes																								
<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h30</td> </tr> <tr> <td>SW Reset</td> <td>8'h30</td> </tr> <tr> <td>HW Reset</td> <td>8'h30</td> </tr> </tbody> </table>													Status	Default Value(D7 to D0)	Power On Sequence	8'h30	SW Reset	8'h30	HW Reset	8'h30					
Status	Default Value(D7 to D0)																								
Power On Sequence	8'h30																								
SW Reset	8'h30																								
HW Reset	8'h30																								

### 12.1.34 RDID3 (DCh)

DCH	Read ID3 Value																								
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	L	H	R	1	1	0	1	1	1	0	0	0	DCH												
Parameter1	H	R	H	X	X	X	X	X	X	X	X	X	X												
Parameter2	H	R	H	SYS_ID3[7:0]									25H												
Description	The 1st Parameter is dummy read. This read byte return 8-bit LCD module's ID.																								
Restriction	Should set “FF=A5” before configure this registers																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability																								
Normal Mode on,Idle Mode Off,Sleep Out	Yes																								
Normal Mode on,Idle Mode On,Sleep Out	Yes																								
Partial Mode on,Idle Mode Off,Sleep Out	Yes																								
Partial Mode on,Idle Mode On,Sleep Out	Yes																								
Sleep In	Yes																								
<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h23</td> </tr> <tr> <td>SW Reset</td> <td>8'h23</td> </tr> <tr> <td>HW Reset</td> <td>8'h23</td> </tr> </tbody> </table>													Status	Default Value(D7 to D0)	Power On Sequence	8'h23	SW Reset	8'h23	HW Reset	8'h23					
Status	Default Value(D7 to D0)																								
Power On Sequence	8'h23																								
SW Reset	8'h23																								
HW Reset	8'h23																								

## 12.2 Panel Function Command List and Description

Addr	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0x3D	SPI2S ET	W					spi2li ne_en		spi2line_mode[ 1:0]	
0x51	PWC TR 1	W				ddvdh _clp_ en			ddvdh_clamp[2:0]	
0x52	PWC TR 2	W				vgh_c lp_en			vgh_clamp[1:0]	
0x53	PWC TR 3	W				vgl_cl p_en			vgl_clamp[1:0]	
0x61	FRM CTR 1	W					hbp[7:0]			
0x62	FRM CTR 2	W					hfp[7:0]			
0x63	FRM CTR 3	W					vbp[6:0]			
0x64	FRM CTR 4	W					vfp[6:0]			
0x82	RGB CTR	W					dpi_d p	dpi_e p	dpi_h sp	dpi_v sp
0x84	GAT EST	W					gate_st[7:0]			
0x85	GAT EED	W					gate_ed[7:0]			
0x87	PWC TR 4	W					vrh[4:0]			
0x88	VMC TR 1	W					vcm[5:0]			
0x89	VMC TR 2	W					vcom_vdv[5:0]			
0x93	SRCS ET	W				ndl			src_en sel	polar_ sel
0x94	SRCS T	W					src_st[7:0]			
0x95	PCH GST	W					pchg_st[7:0]			
0xB1	PWC TR 5	W					bth[1:0]		btl[1:0]	
0xB2	PWC TR 6	W	ddvdh_clk_sel[ 1:0]		vgh_clk_sel[1: 0]		vgl_clk_sel[1:0]		vcl_clk_sel[1:0]	
0xB6	VMBI AS	W							vcom_bias_fix[ 1:0]	
0xC3	REV	W				src_ss				gate_gs
0xC4	VDD	W					regu_ad[2:0]			
0xD1	RDO TP 1	R					otp_rd_dat[7:0]			
0xD2	RDO TP 2	R					otp_rd_dat[15:8]			

Addr	Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0xD3	RDO TP 3	R					otp_rd_dat[23:16]			
0xD4	RDO TP 4	R					otp_rd_dat[31:24]			
0xE1	OTPC TR 1	W			otp_ptm[1:0]	otp_vp_pp_sel	otp_prog	otp_wr_en	otp_rd_en	
0xE2	OTPC TR 2	W				otp_addr[6:0]				
0xE3	OTPC TR 3	W			otp_wr_dat[7:0]					
0xE4	OTPC TR 4	W							otp_sd_en	otp_slpout_en

## 12.2.1 SPI2SET (3Dh)

3DH	SPI 2 Line Set
-----	----------------

	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX															
Command	L	H	R	0	0	1	1	1	1	0	1	3DH															
Parameter	H	H	R	0	0	0	0	SPI2LINE_EN	0	SPI2LINE_MOD E[1:0]		00H															
Description	SPI2LINE_EN: Enable SPI two data line function. “0” is ON, “1” is OFF; SPI2LINE_MODE[1:0]: Select different data combination on data lines.																										
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th>MODE[1:0]</th> <th>Pixel format</th> <th>Transmit method</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>5-6-5</td> <td>One transmit per pixel</td> </tr> <tr> <td>11</td> <td>6-6-6</td> <td>One transmit per pixel</td> </tr> <tr> <td>01</td> <td>6-6-6</td> <td>Three transmits each two pixels</td> </tr> <tr> <td>10</td> <td></td> <td></td> </tr> </tbody> </table>				MODE[1:0]	Pixel format	Transmit method	00	5-6-5	One transmit per pixel	11	6-6-6	One transmit per pixel	01	6-6-6	Three transmits each two pixels	10										
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Restriction	Should set “FF=A5” before configure this registers																										
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes			
Status	Availability																										
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Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h00</td> </tr> <tr> <td>SW Reset</td> <td>8'h00</td> </tr> <tr> <td>HW Reset</td> <td>8'h00</td> </tr> </tbody> </table>												Status	Default Value(D7 to D0)	Power On Sequence	8'h00	SW Reset	8'h00	HW Reset	8'h00							
Status	Default Value(D7 to D0)																										
Power On Sequence	8'h00																										
SW Reset	8'h00																										
HW Reset	8'h00																										

;

## 12.2.2 DDVDH\_CLAMP (51h)

51H	Power Control 1
-----	-----------------

	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
Command	L	H	R	0	1	0	1	0	0	0	1	51H																		
Parameter	H	H	R	0	0	0	DDVDH_CLP_EN	0	DDVDH_CLAMP[2:0]			14H																		
DDVDH_CLP_EN: This command is used to define DDVDH clamp enable.																														
<table border="1"> <thead> <tr> <th>DDVDH_CLP_EN</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Disable the clamp</td> </tr> <tr> <td>1</td> <td>Enable the clamp</td> </tr> </tbody> </table>												DDVDH_CLP_EN	Description	0	Disable the clamp	1	Enable the clamp													
DDVDH_CLP_EN	Description																													
0	Disable the clamp																													
1	Enable the clamp																													
DDVDH_CLAMP[2:0]: This command is used to define DDVDH clamp value																														
<table border="1"> <thead> <tr> <th>DDVDH_CLAMP[1:0]</th> <th>DDVDH (V)</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>4.5</td> </tr> <tr> <td>001</td> <td>4.6</td> </tr> <tr> <td>010</td> <td>4.7</td> </tr> <tr> <td>011</td> <td>4.8</td> </tr> <tr> <td>100</td> <td>4.9</td> </tr> <tr> <td><b>101</b></td> <td><b>5</b></td> </tr> <tr> <td>110</td> <td>5.1</td> </tr> <tr> <td>111</td> <td>5.2</td> </tr> </tbody> </table>												DDVDH_CLAMP[1:0]	DDVDH (V)	000	4.5	001	4.6	010	4.7	011	4.8	100	4.9	<b>101</b>	<b>5</b>	110	5.1	111	5.2	
DDVDH_CLAMP[1:0]	DDVDH (V)																													
000	4.5																													
001	4.6																													
010	4.7																													
011	4.8																													
100	4.9																													
<b>101</b>	<b>5</b>																													
110	5.1																													
111	5.2																													
Restriction	Should set “FF=A5” before configure this registers																													
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>												Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes						
Status	Availability																													
Normal Mode on,Idle Mode Off,Sleep Out	Yes																													
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Sleep In	Yes																													
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h13</td> </tr> <tr> <td>SW Reset</td> <td>8'h13</td> </tr> <tr> <td>HW Reset</td> <td>8'h13</td> </tr> </tbody> </table>												Status	Default Value(D7 to D0)	Power On Sequence	8'h13	SW Reset	8'h13	HW Reset	8'h13										
Status	Default Value(D7 to D0)																													
Power On Sequence	8'h13																													
SW Reset	8'h13																													
HW Reset	8'h13																													

### 12.2.3 VGH\_CLAMP (52h)

52H	VGH_CLAMP											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX

Command	L	H	R	0	1	0	1	0	0	1	0	52H												
Parameter	H	H	R	0	0	0	VGH_CLP_EN	0	0	VGH_CLAMP[1:0]		13H												
VGH_CLP_EN: This command is used to define VGH clamp enable.																								
<table border="1"> <thead> <tr> <th>VGH_CLP_EN</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Disable the clamp</td> </tr> <tr> <td>1</td> <td>Enable the clamp</td> </tr> </tbody> </table>												VGH_CLP_EN	Description	0	Disable the clamp	1	Enable the clamp							
VGH_CLP_EN	Description																							
0	Disable the clamp																							
1	Enable the clamp																							
VGH_CLAMP[1:0]: This command is used to define VGH clamp value.																								
<table border="1"> <thead> <tr> <th>VGH_CLAMP[1:0]</th> <th>VGH (unit:V)</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>10</td> </tr> <tr> <td>01</td> <td>12</td> </tr> <tr> <td>10</td> <td>13.5</td> </tr> <tr> <td>11</td> <td>15</td> </tr> </tbody> </table>												VGH_CLAMP[1:0]	VGH (unit:V)	00	10	01	12	10	13.5	11	15			
VGH_CLAMP[1:0]	VGH (unit:V)																							
00	10																							
01	12																							
10	13.5																							
11	15																							
Restriction	Should set “FF=A5” before configure this registers																							
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Status	Availability																							
Normal Mode on,Idle Mode Off,Sleep Out	Yes																							
Normal Mode on,Idle Mode On,Sleep Out	Yes																							
Partial Mode on,Idle Mode Off,Sleep Out	Yes																							
Partial Mode on,Idle Mode On,Sleep Out	Yes																							
Sleep In	Yes																							
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h13</td> </tr> <tr> <td>SW Reset</td> <td>8'h13</td> </tr> <tr> <td>HW Reset</td> <td>8'h13</td> </tr> </tbody> </table>												Status	Default Value(D7 to D0)	Power On Sequence	8'h13	SW Reset	8'h13	HW Reset	8'h13				
Status	Default Value(D7 to D0)																							
Power On Sequence	8'h13																							
SW Reset	8'h13																							
HW Reset	8'h13																							

## 12.2.4 VGL\_CLAMP (53h)

53H	VGL_CLAMP											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	0	1	0	1	0	0	1	1	53H

## NV3023A—132RGB x162 dot, 262k-color TFT LCD Single-Chip Driver

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Parameter	H	H	R	0	0	0	VGL_CLP_EN	0	0	VGL_CLAMP[1:0]	11H															
Description	This command is used to set the VGL clamp voltage.																									
	<table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th>VGL_CLAMP[1]</th> <th>VGL_CLAMP[0]</th> <th>VGL</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>-7.5</td> </tr> <tr> <td>0</td> <td>1</td> <td>-10</td> </tr> <tr> <td>1</td> <td>0</td> <td>-12.5</td> </tr> <tr> <td>1</td> <td>1</td> <td>-13</td> </tr> </tbody> </table>											VGL_CLAMP[1]	VGL_CLAMP[0]	VGL	0	0	-7.5	0	1	-10	1	0	-12.5	1	1	-13
VGL_CLAMP[1]	VGL_CLAMP[0]	VGL																								
0	0	-7.5																								
0	1	-10																								
1	0	-12.5																								
1	1	-13																								
Restriction	Should set “FF=A5” before configure this registers																									
Register Availability	<table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes			
Status	Availability																									
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Sleep In	Yes																									
Default	<table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h10</td> </tr> <tr> <td>SW Reset</td> <td>8'h10</td> </tr> <tr> <td>HW Reset</td> <td>8'h10</td> </tr> </tbody> </table>											Status	Default Value(D7 to D0)	Power On Sequence	8'h10	SW Reset	8'h10	HW Reset	8'h10							
Status	Default Value(D7 to D0)																									
Power On Sequence	8'h10																									
SW Reset	8'h10																									
HW Reset	8'h10																									

### 12.2.5 DISP\_HBP (61h)

<b>61H</b>		Frame Rate Control 1										
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	0	1	1	0	0	0	0	1	61H

## NV3023A—132RGB x162 dot, 262k-color TFT LCD Single-Chip Driver

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Parameter	H	H	R	HBP[7:0]						05H													
Description	Internal frame rate control register, used to enlarge horizontal scan cycle. Frame rate=fosc/2*(131+HBP+HFP)*(162+VBP+VFP) Fosc=6MHz																						
Restriction	Should set “FF=A5” before configure this registers																						
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th style="text-align: center; padding: 2px;">Status</th> <th style="text-align: center; padding: 2px;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">Normal Mode on,Idle Mode Off,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Normal Mode on,Idle Mode On,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode on,Idle Mode Off,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode on,Idle Mode On,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Sleep In</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability																						
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Status	Default Value(D7 to D0)																						
Power On Sequence	8'h05																						
SW Reset	8'h05																						
HW Reset	8'h05																						

### 12.2.6 DISP\_HFP (62h)

62H		Frame Rate Control 2										
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	0	1	1	0	0	0	1	0	62H

## NV3023A—132RGB x162 dot, 262k-color TFT LCD Single-Chip Driver

---

Parameter	H	H	R	HFP[7:0]					05H												
Description	Internal frame rate control register, used to enlarge horizontal scan cycle. Frame rate=fosc/2*(131+HBP+HFP)*(162+VBP+VFP) Fosc=6MHz																				
Restriction	Should set “FF=A5” before configure this registers																				
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th style="text-align: center; padding: 2px;">Status</th> <th style="text-align: center; padding: 2px;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">Normal Mode on,Idle Mode Off,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Normal Mode on,Idle Mode On,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode on,Idle Mode Off,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode on,Idle Mode On,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Sleep In</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> </tbody> </table>									Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability																				
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Sleep In	Yes																				
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th style="text-align: center; padding: 2px;">Status</th> <th style="text-align: center; padding: 2px;">Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">Power On Sequence</td> <td style="text-align: center; padding: 2px;">8'h05</td> </tr> <tr> <td style="text-align: center; padding: 2px;">SW Reset</td> <td style="text-align: center; padding: 2px;">8'h05</td> </tr> <tr> <td style="text-align: center; padding: 2px;">HW Reset</td> <td style="text-align: center; padding: 2px;">8'h05</td> </tr> </tbody> </table>									Status	Default Value(D7 to D0)	Power On Sequence	8'h05	SW Reset	8'h05	HW Reset	8'h05				
Status	Default Value(D7 to D0)																				
Power On Sequence	8'h05																				
SW Reset	8'h05																				
HW Reset	8'h05																				

### 12.2.7 DISP\_VBP (63h)

<b>63H</b>		Frame Rate Control 3										
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	0	1	1	0	0	0	1	1	63H

## NV3023A—132RGB x162 dot, 262k-color TFT LCD Single-Chip Driver

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Parameter	H	H	R	0	VBP[6:0]	02H												
Description	Internal frame rate control register, used to enlarge vertical scan cycle. Frame rate=fosc/2*(131+HBP+HFP)*(162+VBP+VFP) Fosc=6MHz																	
Restriction	Should set “FF=A5” before configure this registers																	
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th style="text-align: center; padding: 2px;">Status</th> <th style="text-align: center; padding: 2px;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">Normal Mode on,Idle Mode Off,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Normal Mode on,Idle Mode On,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode on,Idle Mode Off,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode on,Idle Mode On,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Sleep In</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> </tbody> </table>						Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability																	
Normal Mode on,Idle Mode Off,Sleep Out	Yes																	
Normal Mode on,Idle Mode On,Sleep Out	Yes																	
Partial Mode on,Idle Mode Off,Sleep Out	Yes																	
Partial Mode on,Idle Mode On,Sleep Out	Yes																	
Sleep In	Yes																	
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th style="text-align: center; padding: 2px;">Status</th> <th style="text-align: center; padding: 2px;">Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">Power On Sequence</td> <td style="text-align: center; padding: 2px;">8'h02</td> </tr> <tr> <td style="text-align: center; padding: 2px;">SW Reset</td> <td style="text-align: center; padding: 2px;">8'h02</td> </tr> <tr> <td style="text-align: center; padding: 2px;">HW Reset</td> <td style="text-align: center; padding: 2px;">8'h02</td> </tr> </tbody> </table>						Status	Default Value(D7 to D0)	Power On Sequence	8'h02	SW Reset	8'h02	HW Reset	8'h02				
Status	Default Value(D7 to D0)																	
Power On Sequence	8'h02																	
SW Reset	8'h02																	
HW Reset	8'h02																	

### 12.2.8 DISP\_VFP (64h)

Frame Rate Control 4												
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	0	1	1	0	0	1	0	0	64H

## NV3023A—132RGB x162 dot, 262k-color TFT LCD Single-Chip Driver

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Parameter	H	H	R	0	VFP[6:0]	02H												
Description	Internal frame rate control register, used to enlarge vertical scan cycle. Frame rate=fosc/2*(131+HBP+HFP)*(162+VBP+VFP) Fosc=6MHz																	
Restriction	Should set “FF=A5” before configure this registers																	
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th style="text-align: center; padding: 2px;">Status</th> <th style="text-align: center; padding: 2px;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">Normal Mode on,Idle Mode Off,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Normal Mode on,Idle Mode On,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode on,Idle Mode Off,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode on,Idle Mode On,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Sleep In</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> </tbody> </table>						Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability																	
Normal Mode on,Idle Mode Off,Sleep Out	Yes																	
Normal Mode on,Idle Mode On,Sleep Out	Yes																	
Partial Mode on,Idle Mode Off,Sleep Out	Yes																	
Partial Mode on,Idle Mode On,Sleep Out	Yes																	
Sleep In	Yes																	
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th style="text-align: center; padding: 2px;">Status</th> <th style="text-align: center; padding: 2px;">Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">Power On Sequence</td> <td style="text-align: center; padding: 2px;">8'h02</td> </tr> <tr> <td style="text-align: center; padding: 2px;">SW Reset</td> <td style="text-align: center; padding: 2px;">8'h02</td> </tr> <tr> <td style="text-align: center; padding: 2px;">HW Reset</td> <td style="text-align: center; padding: 2px;">8'h02</td> </tr> </tbody> </table>						Status	Default Value(D7 to D0)	Power On Sequence	8'h02	SW Reset	8'h02	HW Reset	8'h02				
Status	Default Value(D7 to D0)																	
Power On Sequence	8'h02																	
SW Reset	8'h02																	
HW Reset	8'h02																	

### 12.2.9. Positive Gamma Correction Setting (70h~7Fh)

A1H~ABH		GAMMA CORRECTION SETTING											
		D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
70H	H	H	R						gam_vrp0				0x03
71H	H	H	R				gam_vrp2				0x32		

72H	H	H	R							gam_vrp4	0x0b												
73H	H	H	R							gam_vrp6	0x0c												
74H	H	H	R							gam_vrp12	0x07												
75H	H	H	R							gam_vrp16	0x0d												
76H	H	H	R							gam_vrp20	0x34												
77H	H	H	R							gam_vrp28	0x0a												
78H	H	H	R							gam_vrp34	0x08												
79H	H	H	R							gam_vrp42	0x32												
7AH	H	H	R							gam_vrp46	0x07												
7BH	H	H	R							gam_vrp50	0x16												
7CH	H	H	R							gam_vrp56	0x10												
7DH	H	H	R							gam_vrp58	0x0c												
7EH	H	H	R							gam_vrp60	0x31												
7FH	H	H	R							gam_vrp62	0x08												
Description	This command is used to get different gamma curve through changing this 16 key points's voltage to get the ideal gamma curve. Note: 19mV/step.																						
Restriction	Should set “FF=A5” before configure this registers																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes																						
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Status	Default Value(D7 to D0)																						
Power On Sequence	8'h02																						
SW Reset	8'h02																						
HW Reset	8'h02																						

### 12.2.10. Negative Gamma Correction Setting (A0h~AFh)

GAMMA CORRECTION SETTING												
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
0xA0	H	H	R									gam_vrn0
0xA1	H	H	R									gam_vrn2

0xA2	H	H	R						gam_vrn4	0x09												
0xA3	H	H	R						gam_vrn6	0x0c												
0xA4	H	H	R						gam_vrn12	0x07												
0xA5	H	H	R						gam_vrn16	0x03												
0xA6	H	H	R						gam_vrn20	0x34												
0xA7	H	H	R						gam_vrn28	0x05												
0xA8	H	H	R						gam_vrn34	0x07												
0xA9	H	H	R						gam_vrn42	0x32												
0xAA	H	H	R						gam_vrn46	0x0b												
0xAB	H	H	R						gam_vrn50	0x16												
0xAC	H	H	R						gam_vrn56	0x10												
0xAD	H	H	R						gam_vrn58	0x0a												
0xAE	H	H	R						gam_vrn60	0x31												
0xAF	H	H	R						gam_vrn62	0x07												
Description	This command is used to get different gamma curve through changing this 16 key points's voltage to get the ideal gamma curve. Note: 19mV/step.																					
Restriction	Should set “FF=A5” before configure this registers																					
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
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Sleep In	Yes																					
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Status	Default Value(D7 to D0)																					
Power On Sequence	8'h02																					
SW Reset	8'h02																					
HW Reset	8'h02																					

### 12.2.9 RGBCTR (82h)

82H	RGB Interface Control											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	1	0	0	0	0	0	1	0	82H
Parameter	H	H	R	0	0	0	0	DPI_DP	DPI_EP	DPI_HSP	DPI_VSP	00H
Description	DPI_DP : PCLK polarity ( “1”= data fetched at falling time, “0”= data fetched at rising time);											

	DPI_EP : DE polarity (“1”= Low enable, “0”=High enable) DPI_HSP: HS polarity(“1”=Low level sync clock, “0”=High level sync clock) DPI_VSP: VS polarity(“1”=Low level sync clock, “0”=High level sync clock)												
Restriction	Should set “FF=A5” before configure this registers												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th style="text-align: center; padding: 2px;">Status</th> <th style="text-align: center; padding: 2px;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">Normal Mode on,Idle Mode Off,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Normal Mode on,Idle Mode On,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode on,Idle Mode Off,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode on,Idle Mode On,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Sleep In</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability												
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Normal Mode on,Idle Mode On,Sleep Out	Yes												
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Sleep In	Yes												
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Status	Default Value(D7 to D0)												
Power On Sequence	8'h00												
SW Reset	8'h00												
HW Reset	8'h00												

### 12.2.10 GATEST (84h)

84H	GATE START SETTING																				
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	L	H	R	1	0	0	0	0	1	0	0	84H									
Parameter	H	H	R	GATE_ST[7:0]																	
Description	Gate enables start position setting.																				
Restriction	Should set “FF=A5” before configure this registers																				

Register Availability	Status		Availability	
	Normal Mode on,Idle Mode Off,Sleep Out		Yes	
	Normal Mode on,Idle Mode On,Sleep Out		Yes	
	Partial Mode on,Idle Mode Off,Sleep Out		Yes	
	Partial Mode on,Idle Mode On,Sleep Out		Yes	
	Sleep In		Yes	
Default	Status		Default Value(D7 to D0)	
	Power On Sequence		8'h14	
	SW Reset		8'h14	
	HW Reset		8'h14	

## 12.2.11 GATE\_ED (85h)

85H	GATE END SETTING																				
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	L	H	R	1	0	0	0	0	1	0	1	85H									
Parameter	H	H	R	GATE_ED[7:0]																	
Description	Gate enables end position setting.																				
Restriction	Should set “FF=A5” before configure this registers																				

Register Availability	Status		Availability	
	Normal Mode on,Idle Mode Off,Sleep Out		Yes	
	Normal Mode on,Idle Mode On,Sleep Out		Yes	
	Partial Mode on,Idle Mode Off,Sleep Out		Yes	
	Partial Mode on,Idle Mode On,Sleep Out		Yes	
	Sleep In		Yes	
Default	Status		Default Value(D7 to D0)	
	Power On Sequence		8'h78	
	SW Reset		8'h78	
	HW Reset		8'h78	

## 12.2.12 VRH\_TEST (87h)

87H	Power Control 4											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	1	0	0	0	0	1	1	1	87H
Parameter	H	H	R	0	0	0	VRH[4:0]					16H
Description	VRH[4:0]: This command is used to define GVDD trimming value.											
	VRH[4:0]		GVDD		VRH[4:0]		GVDD					

	00000	3.60	10000	4.40													
	00001	3.65	10001	4.45													
	00010	3.70	10010	4.50													
	00011	3.75	10011	4.55													
	00100	3.80	10100	4.60													
	00101	3.85	10101	4.65													
	00110	3.90	<b>10110</b>	<b>4.70</b>													
	00111	3.95	10111	4.75													
	01000	4.00	11000	4.80													
	01001	4.05	11001	4.85													
	01010	4.10	11010	4.90													
	01011	4.15	11011	4.95													
	01100	4.20	11100	5.00													
	01101	4.25	11101	5.05													
	01110	4.30	11110	5.10													
	01111	4.35	11111	5.15													
Restriction	Should set “FF=A5” before configure this registers																
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>					Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability																
Normal Mode on,Idle Mode Off,Sleep Out	Yes																
Normal Mode on,Idle Mode On,Sleep Out	Yes																
Partial Mode on,Idle Mode Off,Sleep Out	Yes																
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Sleep In	Yes																
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h17</td> </tr> <tr> <td>SW Reset</td> <td>8'h17</td> </tr> <tr> <td>HW Reset</td> <td>8'h17</td> </tr> </tbody> </table>					Status	Default Value(D7 to D0)	Power On Sequence	8'h17	SW Reset	8'h17	HW Reset	8'h17				
Status	Default Value(D7 to D0)																
Power On Sequence	8'h17																
SW Reset	8'h17																
HW Reset	8'h17																

### 12.2.13 VCM\_TEST (88h)

88H	VCOM Control 1											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	1	0	0	0	1	0	0	0	88H
Parameter	H	H	R	0	0	VCM[6:0]						14H
Description	VCM[6:0]: This command is used to define VCOMH trimming value.											

VCM[6:0]	VCOMH	VCM[6:0]	VCOMH
0000000	3.198900	0101100	3.862800
0000001	3.214000	0101101	3.877900
0000010	3.229100	0101110	3.892900
0000011	3.244100	0101111	3.908000
0000100	3.259200	0110000	3.923100
0000101	3.274300	0110001	3.938100
0000110	3.289400	0110010	3.953300
0000111	3.304500	0110011	3.968400
0001000	3.319600	0110100	3.983400
0001001	3.334700	0110101	3.998500
0001010	3.349800	0110110	4.013600
0001011	3.364800	0110111	4.028700
0001100	3.379900	0111000	4.043800
0001101	3.395000	0111001	4.058900
0001110	3.410100	0111010	4.074000
0001111	3.425200	0111011	4.089000
0010000	3.440300	0111100	4.104100
0010001	3.455400	0111101	4.119200
0010010	3.470500	0111110	4.134400
0010011	3.485600	0111111	4.149500
<b>0010100</b>	<b>3.500700</b>	1000000	4.164600
0010101	3.515800	1000001	4.179600
0010110	3.530900	1000010	4.194700
0010111	3.546000	1000011	4.209900
0011000	3.561000	1000100	4.224900
0011001	3.576100	1000101	4.239900
0011010	3.591200	1000110	4.255000
0011011	3.606300	1000111	4.270200
0011100	3.621400	1001000	4.285200
0011101	3.636500	1001001	4.300300
0011110	3.651500	1001010	4.315400
0011111	3.666700	1001011	4.330400
0100000	3.681700	1001100	4.345600
0100001	3.696900	1001101	4.360600
0100010	3.711900	1001110	4.375700
0100011	3.727000	1001111	4.390800
0100100	3.742100	1010000	4.405900
0100101	3.757100	1010001	4.420900
0100110	3.772200	1010010	4.436000
0100111	3.787300	1010011	4.451100
0101000	3.802400	1010100	4.466400
0101001	3.817500	1010101	4.481500
0101010	3.832600	1010110	4.496400

## NV3023A—132RGB x162 dot, 262k-color TFT LCD Single-Chip Driver

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	0101011	3.847600													
Restriction	Should set “FF=A5” before configure this registers														
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th style="text-align: center; padding: 2px;">Status</th> <th style="text-align: center; padding: 2px;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">Normal Mode on,Idle Mode Off,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Normal Mode on,Idle Mode On,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode on,Idle Mode Off,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode on,Idle Mode On,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Sleep In</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> </tbody> </table>			Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability														
Normal Mode on,Idle Mode Off,Sleep Out	Yes														
Normal Mode on,Idle Mode On,Sleep Out	Yes														
Partial Mode on,Idle Mode Off,Sleep Out	Yes														
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Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th style="text-align: center; padding: 2px;">Status</th> <th style="text-align: center; padding: 2px;">Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">Power On Sequence</td> <td style="text-align: center; padding: 2px;">8'h13</td> </tr> <tr> <td style="text-align: center; padding: 2px;">SW Reset</td> <td style="text-align: center; padding: 2px;">8'h13</td> </tr> <tr> <td style="text-align: center; padding: 2px;">HW Reset</td> <td style="text-align: center; padding: 2px;">8'h13</td> </tr> </tbody> </table>			Status	Default Value(D7 to D0)	Power On Sequence	8'h13	SW Reset	8'h13	HW Reset	8'h13				
Status	Default Value(D7 to D0)														
Power On Sequence	8'h13														
SW Reset	8'h13														
HW Reset	8'h13														

### 12.2.14 VDV\_TEST (89h)

89H		VCOM Control 2											
		D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command		L	H	R	1	0	0	0	1	0	0	1	89H
Parameter		H	H	R	0	0	VCOM_VDV[6:0]						34H

Description	VCOM_VDV[6:0]: This command is used to define VCOML trimming value.			
	VCOM_VDV[6:0]	VCOML	VCOM_VDV[6:0]	VCOML
	0000000	-0.21116	0110110	-1.0256
	0000001	-0.22624	0110111	-1.0407
	0000010	-0.24132	0111000	-1.0558
	0000011	-0.25641	0111001	-1.0709
	0000100	-0.27149	0111010	-1.086
	0000101	-0.28658	0111011	-1.1011
	0000110	-0.30166	0111100	-1.1162
	0000111	-0.31674	0111101	-1.1312
	0001000	-0.33182	0111110	-1.1463
	0001001	-0.3469	0111111	-1.1614
	0001010	-0.36199	1000000	-1.1765
	0001011	-0.37708	1000001	-1.1916
	0001100	-0.39216	1000010	-1.2067
	0001101	-0.40725	1000011	-1.2217
	0001110	-0.42233	1000100	-1.2368
	0001111	-0.43742	1000101	-1.2519
	0010000	-0.45249	1000110	-1.267
	0010001	-0.46758	1000111	-1.2821
	0010010	-0.48266	1001000	-1.2972
	0010011	-0.49775	1001001	-1.3122
	0010100	-0.51283	1001010	-1.3273
	0010101	-0.52791	1001011	-1.3424
	0010110	-0.543	1001100	-1.3575
	0010111	-0.55808	1001101	-1.3726
	0011000	-0.57316	1001110	-1.3877
	0011001	-0.58824	1001111	-1.4028
	0011010	-0.60333	1010000	-1.4178
	0011011	-0.61842	1010001	-1.4329
	0011100	-0.6335	1010010	-1.448
	0011101	-0.64859	1010011	-1.4631
	0011110	-0.66367	1010100	-1.4782
	0011111	-0.67876	1010101	-1.4933
	0100000	-0.69383	1010110	-1.5084
	0100001	-0.70892	1010111	-1.5234
	0100010	-0.724	1011000	-1.5385
	0100011	-0.73909	1011001	-1.5536
	0100100	-0.75417	1011011	-1.5687
	0100101	-0.76925	1011100	-1.5838
	0100110	-0.78434	1011101	-1.5989
	0100111	-0.79942	1011110	-1.6139
	0101000	-0.81451	1011111	-1.629
	0101001	-0.8296	1100000	-1.6441
	0101010	-0.84467	1100001	-1.6592
	0101011	-0.85977	1100010	-1.6743
	0101100	-0.87485	1100011	-1.6894

	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr><td>0101101</td><td>-0.88994</td><td>1100100</td><td>-1.7045</td><td></td></tr> <tr><td>0101110</td><td>-0.90502</td><td>1100101</td><td>-1.7195</td><td></td></tr> <tr><td>0101111</td><td>-0.92011</td><td>1100110</td><td>-1.7346</td><td></td></tr> <tr><td>0110000</td><td>-0.93518</td><td>1100111</td><td>-1.7497</td><td></td></tr> <tr><td>0110001</td><td>-0.95027</td><td>1101000</td><td>-1.7648</td><td></td></tr> <tr><td>0110010</td><td>-0.96535</td><td>1101001</td><td>-1.7799</td><td></td></tr> <tr><td>0110011</td><td>-0.98045</td><td>1101010</td><td>-1.795</td><td></td></tr> <tr><td><b>0110100</b></td><td><b>-0.99552</b></td><td>1101011</td><td>-1.8101</td><td></td></tr> <tr><td>0110101</td><td>-1.0106</td><td></td><td></td><td></td></tr> </table>					0101101	-0.88994	1100100	-1.7045		0101110	-0.90502	1100101	-1.7195		0101111	-0.92011	1100110	-1.7346		0110000	-0.93518	1100111	-1.7497		0110001	-0.95027	1101000	-1.7648		0110010	-0.96535	1101001	-1.7799		0110011	-0.98045	1101010	-1.795		<b>0110100</b>	<b>-0.99552</b>	1101011	-1.8101		0110101	-1.0106			
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Restriction	Should set “FF=A5” before configure this registers																																																	
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Power On Sequence	8'h0F																																																	
SW Reset	8'h0F																																																	
HW Reset	8'h0F																																																	

## 12.2.15 SRC\_POL (93h)

93H	SOURCE SET											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	1	0	0	1	0	0	1	1	93H

Parameter	H	H	R	0	NDL	TE_SEL	SRC_EN_SEL	0	0	POLAR_SEL	60H												
Description	NDL: Select max or min voltage to clear screen. SRC_EN_SEL: Decide if the source enable is open during v-porch area. “1” is OPEN, “0” is CLOSE; POLAR_SEL[1:0]:“00” is line inverse; “01” is two lines inverse “10” is four lines inverse “11” is frame inverse																						
Restriction	Should set “FF=A5” before configure this registers																						
Register Availability	<table border="1" style="width: 100%; text-align: center;"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>											Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
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Status	Default Value(D7 to D0)																						
Power On Sequence	8'h10																						
SW Reset	8'h10																						
HW Reset	8'h10																						

### 12.2.16 SRC\_ST (94h)

94H	SOURCE START SETTING											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	1	0	0	1	0	1	0	0	94H
Parameter	H	H	R	SRC_ST[7:0]								0aH

Description	src_out_ctrl start position setting.											
Restriction	Should set “FF=A5” before configure this registers											
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th style="text-align: center; padding: 2px;">Status</th> <th style="text-align: center; padding: 2px;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">Normal Mode on,Idle Mode Off,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Normal Mode on,Idle Mode On,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode on,Idle Mode Off,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode on,Idle Mode On,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes
Status	Availability											
Normal Mode on,Idle Mode Off,Sleep Out	Yes											
Normal Mode on,Idle Mode On,Sleep Out	Yes											
Partial Mode on,Idle Mode Off,Sleep Out	Yes											
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Status	Default Value(D7 to D0)											
Power On Sequence	8'h0A											
SW Reset	8'h0A											
HW Reset	8'h0A											

## 12.2.17 PCHGST (95h)

<b>95H</b>	SOURCE PRECHARGE START SETTING											
	<b>D/CX</b>	<b>RDX</b>	<b>WRX</b>	<b>D7</b>	<b>D6</b>	<b>D5</b>	<b>D4</b>	<b>D3</b>	<b>D2</b>	<b>D1</b>	<b>D0</b>	HEX
Command	L	H	R	1	0	0	1	0	1	0	1	95H

## NV3023A—132RGB x162 dot, 262k-color TFT LCD Single-Chip Driver

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Parameter	H	H	R	PCHG_ST[7:0]					03H												
Description	Source pre-charge start position setting.																				
Restriction	Should set “FF=A5” before configure this registers																				
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th style="text-align: center; padding: 2px;">Status</th> <th style="text-align: center; padding: 2px;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center; padding: 2px;">Normal Mode on,Idle Mode Off,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Normal Mode on,Idle Mode On,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode on,Idle Mode Off,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Partial Mode on,Idle Mode On,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="text-align: center; padding: 2px;">Sleep In</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> </tbody> </table>									Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability																				
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Status	Default Value(D7 to D0)																				
Power On Sequence	8'h03																				
SW Reset	8'h03																				
HW Reset	8'h03																				

### 12.2.18 PWCTR 5 (B1h)

Power Control 5												
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	1	0	1	1	0	0	0	1	B1H

## NV3023A—132RGB x162 dot, 262k-color TFT LCD Single-Chip Driver

Parameter	H	H	R	0	0	0	0	BTH[1:0]	BTL[1:0]	0FH															
Description	BTH[1:0]: is used to define the ratio in VGH pump.																								
	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>BTH[1:0]</th> <th>BTH[1:0]</th> <th>VGH</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>4*VCI</td> </tr> <tr> <td>0</td> <td>1</td> <td>5*VCI</td> </tr> <tr> <td>1</td> <td>0</td> <td>6*VCI</td> </tr> <tr> <td><b>1</b></td> <td><b>1</b></td> <td><b>6*VCI</b></td> </tr> </tbody> </table>										BTH[1:0]	BTH[1:0]	VGH	0	0	4*VCI	0	1	5*VCI	1	0	6*VCI	<b>1</b>	<b>1</b>	<b>6*VCI</b>
BTH[1:0]	BTH[1:0]	VGH																							
0	0	4*VCI																							
0	1	5*VCI																							
1	0	6*VCI																							
<b>1</b>	<b>1</b>	<b>6*VCI</b>																							
Description	BTL[1:0]: is used to define the ratio in VGL pump.																								
	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>BTL[1:0]</th> <th>BTL[1:0]</th> <th>VGL</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>-3*VCI</td> </tr> <tr> <td>0</td> <td>1</td> <td>-4*VCI</td> </tr> <tr> <td>1</td> <td>0</td> <td>-5*VCI</td> </tr> <tr> <td><b>1</b></td> <td><b>1</b></td> <td><b>-5*VCI</b></td> </tr> </tbody> </table>										BTL[1:0]	BTL[1:0]	VGL	0	0	-3*VCI	0	1	-4*VCI	1	0	-5*VCI	<b>1</b>	<b>1</b>	<b>-5*VCI</b>
BTL[1:0]	BTL[1:0]	VGL																							
0	0	-3*VCI																							
0	1	-4*VCI																							
1	0	-5*VCI																							
<b>1</b>	<b>1</b>	<b>-5*VCI</b>																							
Restriction	Should set “FF=A5” before configure this registers																								
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Partial Mode on,Idle Mode On,Sleep Out	Yes																								
Sleep In	Yes																								
Default	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h0F</td> </tr> <tr> <td>SW Reset</td> <td>8'h0F</td> </tr> <tr> <td>HW Reset</td> <td>8'h0F</td> </tr> </tbody> </table>										Status	Default Value(D7 to D0)	Power On Sequence	8'h0F	SW Reset	8'h0F	HW Reset	8'h0F							
Status	Default Value(D7 to D0)																								
Power On Sequence	8'h0F																								
SW Reset	8'h0F																								
HW Reset	8'h0F																								

### 12.2.19 PWCTR 6 (B2h)

B2H	Power Control 6											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	1	0	1	1	0	0	1	0	B2H

Parameter	H	H	R	ddvdh_clk_sel[1:0]	vgh_clk_sel[1:0]	vgl_clk_sel[1:0]	vcl_clk_sel[1:0]	96H												
	ddvdh_clk_sel[1:0] is used to set the operation frequency of DDVDH pump.																			
				<b>ddvdh_clk_sel [1]</b>	<b>ddvdh_clk_sel [0]</b>	<b>Frequency</b>														
				0	0	1 * OSC														
				0	1	1/2 * OSC														
				<b>1</b>	<b>0</b>	<b>1/4 * OSC</b>														
				1	1	1/8 * OSC														
	vgh_clk_sel [1:0] is used to set the operation frequency of VGH pump.																			
				<b>vgh_clk_sel [1]</b>	<b>vgh_clk_sel [0]</b>	<b>Frequency</b>														
				0	0	1 * OSC														
				<b>0</b>	<b>1</b>	<b>1/2 * OSC</b>														
				1	0	1/4 * OSC														
				1	1	1/8 * OSC														
Description	vgl_clk_sel [1:0] is used to set the operation frequency of VGL pump.																			
				<b>vgl_clk_sel [1]</b>	<b>vgl_clk_sel [0]</b>	<b>Frequency</b>														
				0	0	1 * OSC														
				<b>0</b>	<b>1</b>	<b>1/2 * OSC</b>														
				1	0	1/4 * OSC														
				1	1	1/8 * OSC														
	vcl_clk_sel[1:0] is used to set the operation frequency of VCL pump.																			
				<b>vcl_clk_sel [1]</b>	<b>vcl_clk_sel [0]</b>	<b>Frequency</b>														
				0	0	1 * OSC														
				0	1	1/2 * OSC														
				<b>1</b>	<b>0</b>	<b>1/4 * OSC</b>														
				1	1	1/8 * OSC														
Restriction	Should set “FF=A5” before configure this registers																			
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>								Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability																			
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Sleep In	Yes																			
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value(D7 to D0)</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>8'h00</td> </tr> <tr> <td>SW Reset</td> <td>8'h00</td> </tr> <tr> <td>HW Reset</td> <td>8'h00</td> </tr> </tbody> </table>								Status	Default Value(D7 to D0)	Power On Sequence	8'h00	SW Reset	8'h00	HW Reset	8'h00				
Status	Default Value(D7 to D0)																			
Power On Sequence	8'h00																			
SW Reset	8'h00																			
HW Reset	8'h00																			

### 12.2.20 CHOP (B5h)

<b>B5H</b>	CHOP SET											
	<b>D/CX</b>	<b>RDX</b>	<b>WRX</b>	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	1	0	1	1	0	1	0	1	B5H
Parameter	H	H	R	0	0	CHOP_SEL[1:0]	GAM_FLW_FIX	0	GAM_BIAS_FIX[1:0]			30H
Description	CHOPPER_SEL: Gamma chopper function option.											

	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th>CHOP_SEL[1:0]</th><th>Description</th></tr> </thead> <tbody> <tr> <td>00</td><td>2 frame chopper</td></tr> <tr> <td>01</td><td>1 line chopper (1 frame chopper polarity change)</td></tr> <tr> <td>10</td><td>1 line chopper (2 frame chopper polarity change)</td></tr> <tr style="background-color: #f2e0d2;"> <td><b>11</b></td><td><b>NONE</b></td></tr> </tbody> </table>	CHOP_SEL[1:0]	Description	00	2 frame chopper	01	1 line chopper (1 frame chopper polarity change)	10	1 line chopper (2 frame chopper polarity change)	<b>11</b>	<b>NONE</b>		
CHOP_SEL[1:0]	Description												
00	2 frame chopper												
01	1 line chopper (1 frame chopper polarity change)												
10	1 line chopper (2 frame chopper polarity change)												
<b>11</b>	<b>NONE</b>												
	Gam_bias_fix[1:0] is used to adjust gamma op's bias current, default =00. Gam_flw_fix is used to change gamma op's driver capacity, default =0.												
Restriction	Should set “FF=A5” before configure this registers												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td><td>Yes</td></tr> <tr style="background-color: #f2e0d2;"> <td>Sleep In</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode on,Idle Mode Off,Sleep Out	Yes												
Normal Mode on,Idle Mode On,Sleep Out	Yes												
Partial Mode on,Idle Mode Off,Sleep Out	Yes												
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Sleep In	Yes												
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th>Status</th><th>Default Value(D7 to D0)</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td>8'h00</td></tr> <tr> <td>SW Reset</td><td>8'h00</td></tr> <tr> <td>HW Reset</td><td>8'h00</td></tr> </tbody> </table>	Status	Default Value(D7 to D0)	Power On Sequence	8'h00	SW Reset	8'h00	HW Reset	8'h00				
Status	Default Value(D7 to D0)												
Power On Sequence	8'h00												
SW Reset	8'h00												
HW Reset	8'h00												

## 12.2.21 REV (C3h)

C3H	REV											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	1	1	0	0	0	0	1	1	C3H
Parameter	H	H	R	0	0	0	SRC_SS	0	0	0	GATE_GS	10H
Description	SRC_SS: source reverse scan control. “1” is reverse, “0” is normal.											

## NV3023A—132RGB x162 dot, 262k-color TFT LCD Single-Chip Driver

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	GATE_GS: gate reverse scan control. “1” is reverse, “0” is normal.												
Restriction	Should set “FF=A5” before configure this registers												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th style="text-align: center; padding: 2px;">Status</th> <th style="text-align: center; padding: 2px;">Availability</th> </tr> </thead> <tbody> <tr> <td style="padding: 2px;">Normal Mode on,Idle Mode Off,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="padding: 2px;">Normal Mode on,Idle Mode On,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="padding: 2px;">Partial Mode on,Idle Mode Off,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="padding: 2px;">Partial Mode on,Idle Mode On,Sleep Out</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> <tr> <td style="padding: 2px;">Sleep In</td> <td style="text-align: center; padding: 2px;">Yes</td> </tr> </tbody> </table>	Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
Status	Availability												
Normal Mode on,Idle Mode Off,Sleep Out	Yes												
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Status	Default Value(D7 to D0)												
Power On Sequence	8'h10												
SW Reset	8'h10												
HW Reset	8'h10												

### 12.2.22 VDD (C4h)

C4H	VDD Set											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	1	1	0	0	0	1	0	0	C4H
Parameter	H	H	R	0	0	0	0	REGU_AD[2:0]		0	00H	

Description	<b>REGU_AD[2:0]: VDD trimming signal.</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #f2e0d2;">REGU_AD[2:0]</th><th style="background-color: #f2e0d2;">VDD</th></tr> </thead> <tbody> <tr><td>000</td><td style="color: red;">1.853</td></tr> <tr><td>001</td><td>1.904</td></tr> <tr><td>010</td><td>1.958</td></tr> <tr><td>011</td><td>2.106</td></tr> <tr><td style="color: red;"><b>100</b></td><td>1.597</td></tr> <tr><td>101</td><td>1.654</td></tr> <tr><td>110</td><td>1.737</td></tr> <tr><td>111</td><td>1.805</td></tr> </tbody> </table>		REGU_AD[2:0]	VDD	000	1.853	001	1.904	010	1.958	011	2.106	<b>100</b>	1.597	101	1.654	110	1.737	111	1.805
REGU_AD[2:0]	VDD																			
000	1.853																			
001	1.904																			
010	1.958																			
011	2.106																			
<b>100</b>	1.597																			
101	1.654																			
110	1.737																			
111	1.805																			
Restriction Should set “FF=A5” before configure this registers																				
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="background-color: #f2e0d2;">Status</th><th style="background-color: #f2e0d2;">Availability</th></tr> </thead> <tbody> <tr><td>Normal Mode on,Idle Mode Off,Sleep Out</td><td>Yes</td></tr> <tr><td>Normal Mode on,Idle Mode On,Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode on,Idle Mode Off,Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode on,Idle Mode On,Sleep Out</td><td>Yes</td></tr> <tr><td>Sleep In</td><td>Yes</td></tr> </tbody> </table>		Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes							
Status	Availability																			
Normal Mode on,Idle Mode Off,Sleep Out	Yes																			
Normal Mode on,Idle Mode On,Sleep Out	Yes																			
Partial Mode on,Idle Mode Off,Sleep Out	Yes																			
Partial Mode on,Idle Mode On,Sleep Out	Yes																			
Sleep In	Yes																			
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Status	Default Value(D7 to D0)																			
Power On Sequence	8'h08																			
SW Reset	8'h08																			
HW Reset	8'h08																			

## 12.2.23 VBG (C5h)

C4H	VDD Set											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	1	1	0	0	0	1	0	0	C5H

Parameter	H	H	R	0	0	0	0	VBG_AD[3:0]	0	00H												
<b>VBG_AD[3:0]: VDD trimming signal.</b>																						
Description	<b>VBG_AD[3:0]</b>	<b>VBG</b>	<b>VBG_AD[3:0]</b>	<b>VBG</b>																		
	<b>0000</b>	<b>1.201</b>			1000			1.120														
	0001	1.211			1001			1.131														
	0010	1.221			1010			1.141														
	0011	1.231			1011			1.151														
	0100	1.241			1100			1.161														
	0101	1.251			1101			1.171														
	0110	1.262			1110			1.181														
	0111	1.271			1111			1.191														
Restriction	Should set “FF=A5” before configure this registers																					
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
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Status	Default Value(D7 to D0)																					
Power On Sequence	8'h08																					
SW Reset	8'h08																					
HW Reset	8'h08																					

## 12.2.24 RDOTP 1 (D1h)

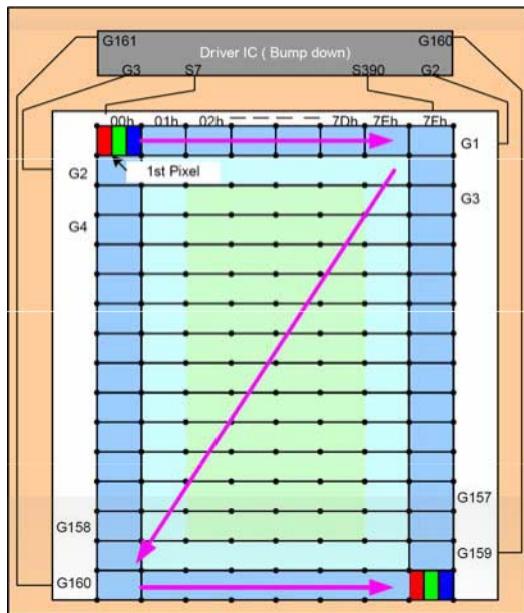
D1H	Read OTP Data 1											
	D/CX	RDX	WRX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	L	H	R	1	1	0	1	0	0	0	1	D1H
Parameter1	H	R	H	X	X	X	X	X	X	X	X	X

Parameter2	H	R	H	OTP_RD_DAT[7:0]	-												
Description	OTP read data[7:0]																
Restriction	The 1st Parameter is dummy read. Should set “FF=A5” before configure this registers																
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr style="background-color: #f2e0d2;"> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode Off,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode on,Idle Mode On,Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>					Status	Availability	Normal Mode on,Idle Mode Off,Sleep Out	Yes	Normal Mode on,Idle Mode On,Sleep Out	Yes	Partial Mode on,Idle Mode Off,Sleep Out	Yes	Partial Mode on,Idle Mode On,Sleep Out	Yes	Sleep In	Yes
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Status	Default Value(D7 to D0)																
Power On Sequence	8'h00																
SW Reset	8'h00																
HW Reset	8'h00																

## 13. Example Panel Connection (GM="011")

CASE 1: First pixel is at left\_top of the panel

RGB order is “R.G.B”



- Direction default setting(H/W)

SMX = 0

SMY = 0

SRGB = 0

S1 = Filter R

S2 = Filter G

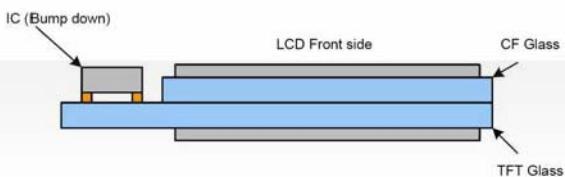
S3 = Filter B

- Display direction control (S/W)

- X- Mirror control by MX

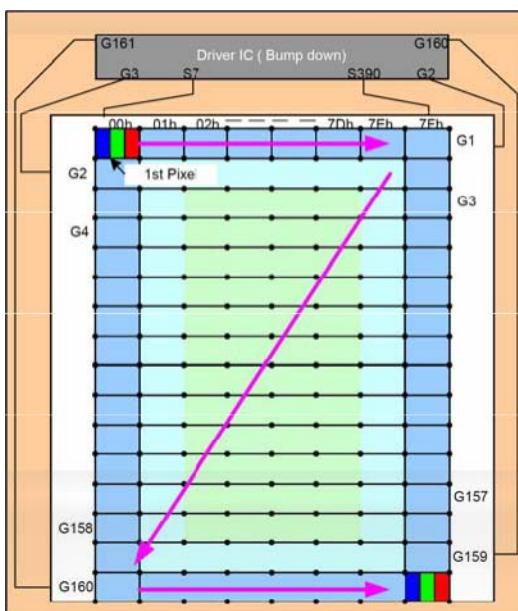
- Y- Mirror control by MY

-XY- Exchange control by MV



CASE 2: First pixel is at left\_top of the panel

RGB order is “B.G.R”



- Direction default setting(H/W)

SMX = 0

SMY = 0

SRGB = 1

S1 = Filter B

S2 = Filter G

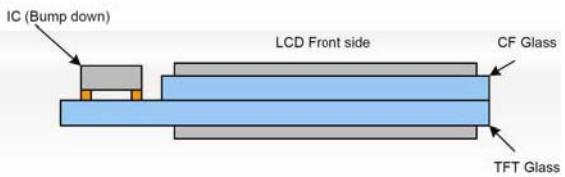
S3 = Filter R

- Display direction control (S/W)

- X- Mirror control by MX

- Y- Mirror control by MY

-XY- Exchange control by MV

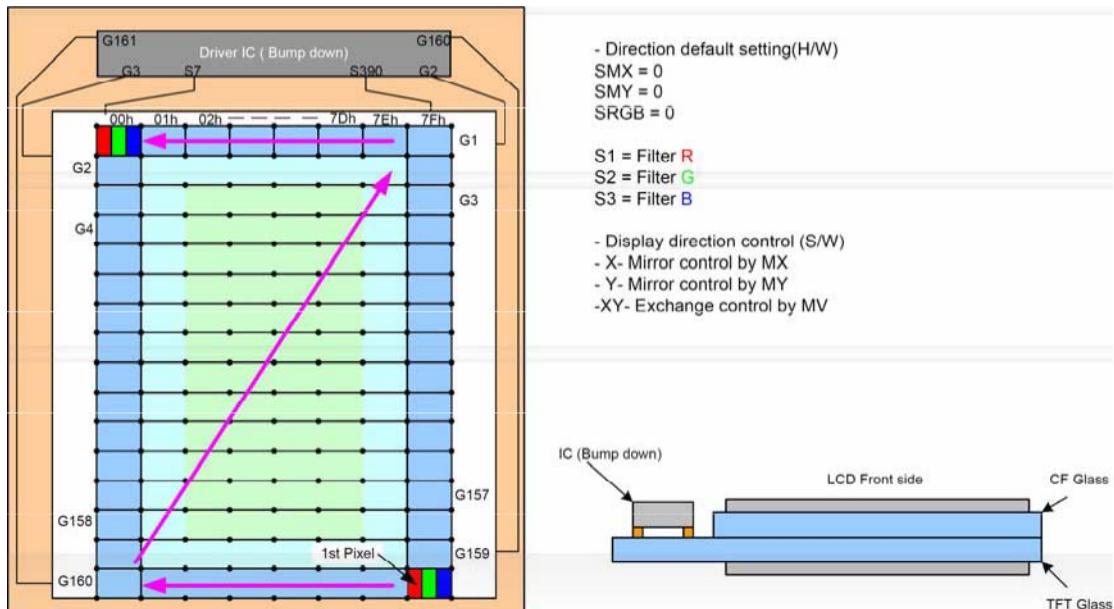


CASE 3: First pixel is at Right\_bottom of the panel

RGB order is “R.G.B”

CASE 3: First pixel is at Right\_bottom of the panel

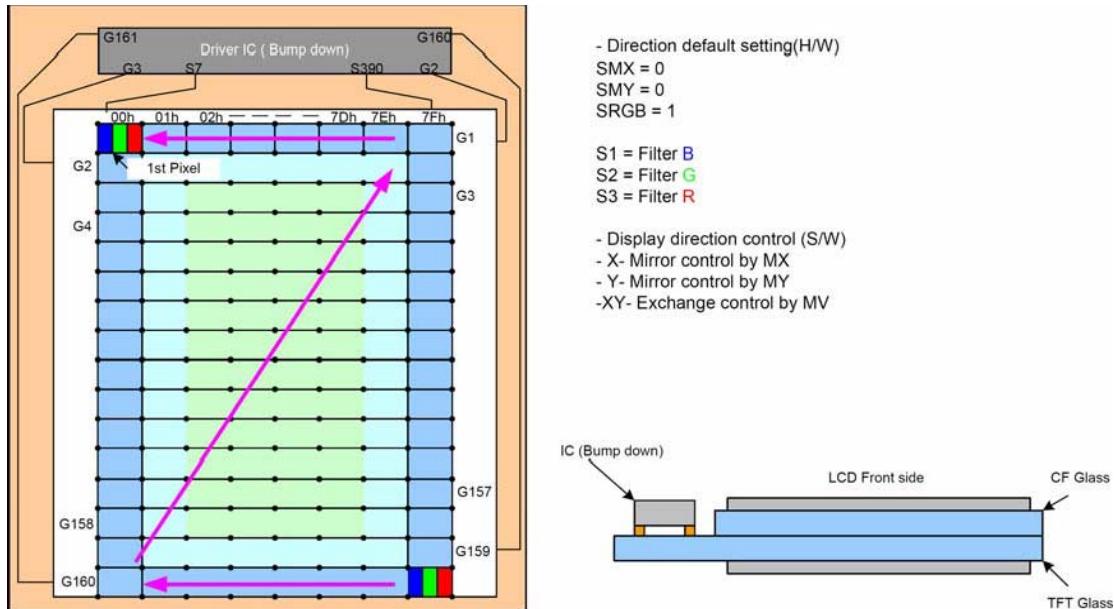
RGB order is “R.G.B”



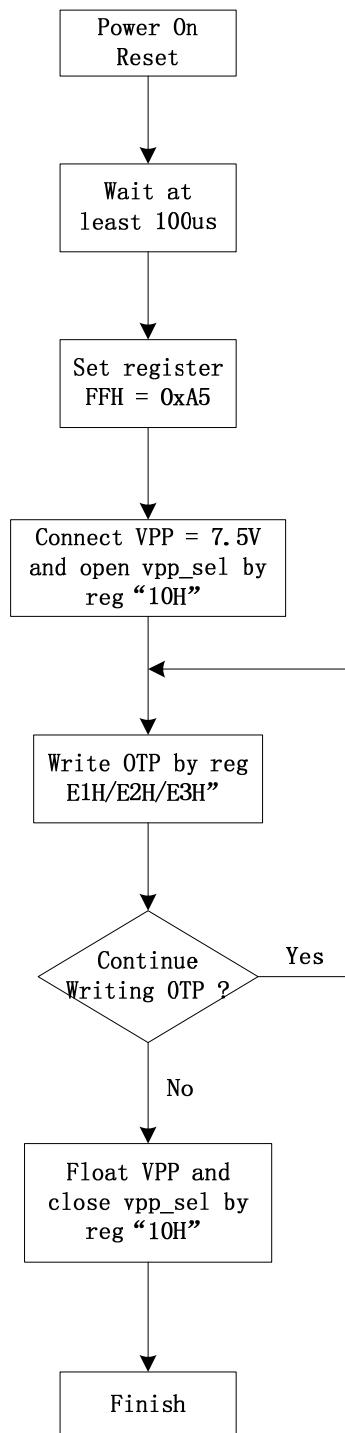
CASE 4: First pixel is at Right\_bottom of the panel

RGB order is “B.G.R”

CASE 3: First pixel is at Right\_bottom of the panel  
RGB order is “R.G.B”



## 14. OTP Flow



## 15. Electrical Characteristics

### 15.1. Absolute Maximum Ratings

The absolute maximum rating is listed on following table. When NV3023A is used out of the absolute maximum ratings, the NV3023A may be permanently damaged. So working within the following electrical characteristics limit is strongly recommended during normal operation.

Item	Symbol	Unit	Value Note
Supply voltage	VCI	V	-0.3~+4.8
Supply voltage(Logic)	IOVCC	V	-0.3~+3.6
Supply voltage(Digital)	VCC	V	-0.3~+2.4
Driver supply voltage	VGH-VGL	V	-0.3~+30.0
Logic input voltage range	VIN	V	-0.3~IOVCC+0.3
Logic output voltage range	VO	V	-0.3~IOVCC+0.3
Operation temperature	Topr	°C	-35~+85
Storage temperature	Tstg	°C	-55~+110

## 15.2. DC Characteristics

Item	Symbol	Unit	Condition	Min.	Typ.	Max.	Note
<b>Power &amp; Operation Voltage</b>							
Analog Operation Voltage	VCI	V	Operation Voltage	2.5	2.75	4.8	Note 2
Logic Operation Voltage	IOVCC	V	I/O Supply Voltage	1.65	1.8	3.6	Note 2
Digital Operation Voltage	VCC	V	Digital Supply Voltage		1.8		Note 2
Gate Driver High Voltage	VGH	V		10		16	Note 3
Gate Driver Low Voltage	VGL	V		-16		-7.5	Note 3
Driver Supply Voltage		V	VGH-VGL	19		32	Note 3
<b>Input/Output</b>							
Logic High Level Input Voltage	VIH	V		0.7IO VCC		IOVCC	Note 1,2,3
Logic Low Level Input Voltage	VIL	V		VSS		0.3IOVC C	Note 1,2,3
Logic High Level Output Voltage	VOH	V	IOH=-1.0mA	0.8IO VCC		IOVCC	Note 1,2,3
Logic Low Level Output Voltage	VOL	V	IOL=1.0mA	VSS		0.2IOVC C	Note 1,2,3
Logic Input Leakage Current	IIL	uA	VIN=IOVCC or VSS	-0.1		0.1	Note 1,2,3
<b>VCOM Operation</b>							
VCOM High Voltage	VCOM H	V	Ccom=12nF	2.5		5	Note 3
VCOM Low Voltage	VCOML	V	Ccom=12nF	-2.5		0	Note 3
VCOM Amplitude Voltage	VOMA	V	VCOMH-VCOML	4		5.5	Note 3
<b>Source Driver</b>							
Source Output Range	Vsout	V		0.5		AVDD-0.1	Note 4
Gama Reference Voltage	GVDD	V		3		4.9	Note 3

Note 1: IOVCC=1.65 to 3.3V, VCI=2.5 to 4.8V, VSSA=VSS=0V, Ta=-30 to 70 (to +85 °C °C no damage)

Note2: Please supply digital IOVCC voltage equal or less than analog VCI voltage. (IOVCC $\leq$ VCI)

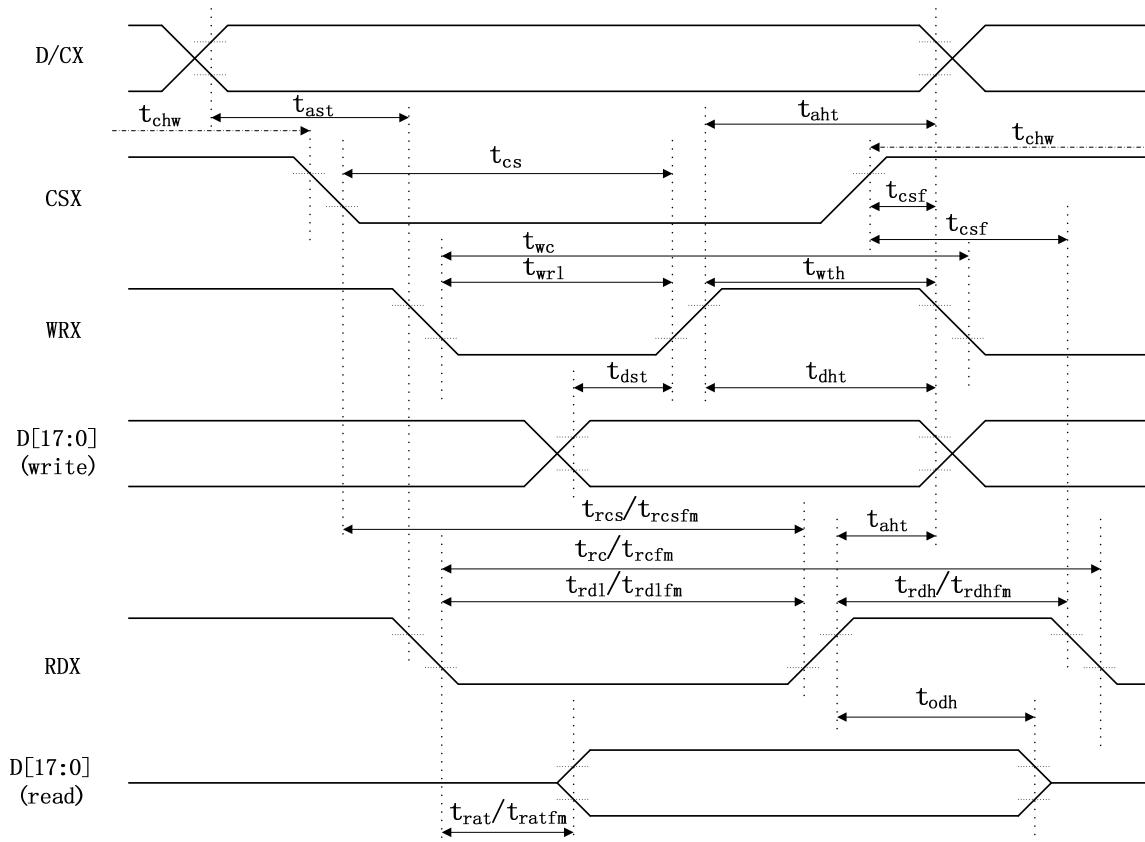
Note2, 3, 4: When the measurements are performed with LCD module. Measurement Points are like below.

Note3: CSX, RDX, WRX, D[23:0], D/CX, RESX, TE, PCLK, VS, HS, DE, SDA, SCL, GM2, GM1, GM0, RCM1, RCM0, P68, IM2, IM1, IM0, SRGB, REV, SMX, SMY, RL, TB, IDM, SHUT, PREG, GS and Test pins.

Note5: Source channel loading = 10pF/channel, Gate channel loading = 50pF/channel

### 15.3. AC Characteristics

#### 15.3.1 Parallel MCU 18/16/9/8-bit BUS



Note: Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

Table 15.3.1 AC characteristics of parallel MCU I/F in asynchronous mode

Signal	Symbol	Parameter	MIN	MAX	UNIT	Description
D/CX	TAST	Address Setup Time	0		ns	
	THAT	Address Hold Time (W/R)	10		ns	
CSX	TCHW	“S” “H” Pulse Width	0		ns	
	TCS	Chip Select Setup Time(W)	10		ns	
	TRCS	Chip Select Setup Time (Read ID)	45		ns	
	TRCSFM	Chip Select Setup Time (Read FM)	355		ns	
	TCSF	Chip Select Wait Time (W/R)	10		ns	
WRX	TWC	Write Cycle	66		ns	
	TWRH	Control Pulse H Duration	15		ns	
	TWRL	Control Pulse L Duration	15		ns	
RDX	TRC	Read Cycle(ID)	160		ns	When Read ID
	TRDH	Control Pulse H Duration(ID)	90		ns	
	TRDL	Control Pulse L	45		ns	

		Duration(ID)				
RDX	TRCFM	Read Cycle(FM)	450		ns	When Read From Frame Memory
	TRDHFM	Control Pulse H Duration(FM)	90		ns	
	TRDLFM	Control Pulse L Duration(FM)	355		ns	
D[17:0]	TDST	Data Setup Time	10		ns	CLmax=30pF Clmin=8pF
	TDHT	Data Hold Time	10		ns	
	TRAT	Read Access Time(ID)		40	ns	
	TRATFM	Read Access Time(FM)		340	ns	
	TODH	Output Disable Time	20	80	ns	

Note 1: IOVCC 1.65 to 3.3V, VCI=2.6 to 3.3V, VSSA=VSS=0V, Ta=-30 to 70 °C (to +85°C no damage)

Note 2: This input signal rise time and fall time ( $t_r$ ,  $t_f$ ) is specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of IOVCC for input signals

### 15.3.2 Display Serial Interface(SPI)

#### 15.3.2.1 SPI 3-Wire Interface

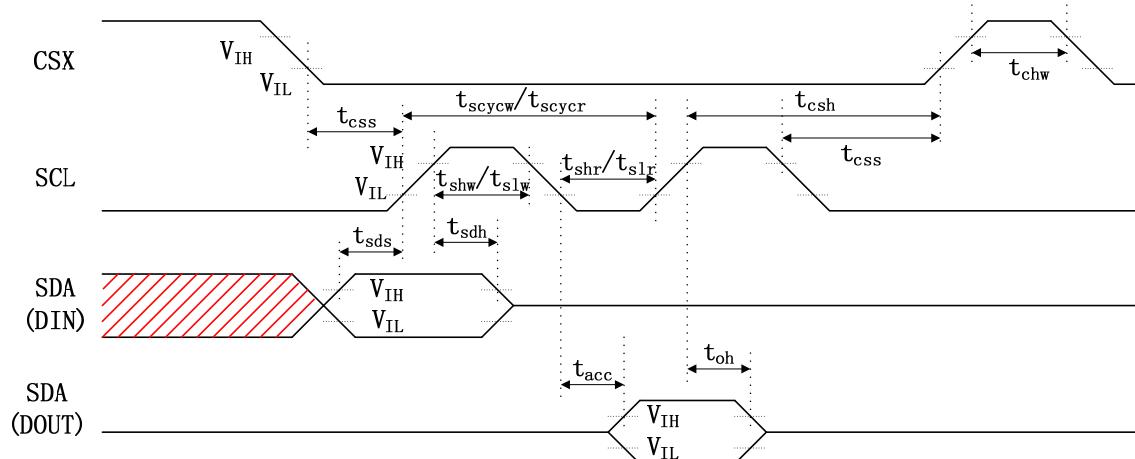


Table 15.3.2.1: 3-pin Serial Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	UNIT	Description
CSX	TCSS	Chip Select Setup Time	10		ns	
	TCSH	Chip Select Hold Time	30		ns	
	TCHW	Chip Select "H" Pulse Width	30		ns	
SCL	TSCYCW	Serial Clock Cycle(Write)	66		ns	
	TSHW	S" L " " H " Pulse Width(Write)	15		ns	
	TSLW	S" L " " L " Pulse Width(Write)	15		ns	
	TSCYCR	Serial Clock	150		ns	

<b>Signal</b>	<b>Symbol</b>	<b>Parameter</b>	<b>MIN</b>	<b>MAX</b>	<b>UNIT</b>	<b>Description</b>
		Cycle(Read)				
	TSHR	S”L””H” Pulse Width(Read)	60		ns	
	TSLR	S”L””L” Pulse Width(Read)	60		ns	
SDA(DIN) / (DOUT)	TSDS	Data Setup Time	15		ns	
	TSDH	Data Hold Time	5		ns	
	TACC	Access Time	5	50	ns	CLmax=30pF CLmin=8pF
	TOH	Output Disable Time	10		ns	

Note 1: IOVCC=1.65 to 3.3V, VCI=2.6 to 3.3V, VSSA=VSS=0V. Ta=-30 to 70°C (to +85°C no damage)

Note 2: The input signal rise time and fall time( $t_r$ ,  $t_f$ ) is specified at 15 ns or less. Logic high and low levels are specified as 10% and 90% of IOVCC for Input signals.

### 15.3.2.2 SPI 4-Wire Interface

Table 15.3.2.2: 4 pin Serial Interface Characteristics

<b>Signal</b>	<b>Symbol</b>	<b>Parameter</b>	<b>MIN</b>	<b>MAX</b>	<b>UNIT</b>	<b>Description</b>
CSX	TCSS	Chip Select Setup Time	10		ns	
	TCSH	Chip Select Hold Time	30		ns	
	TCHW	Chip Select “H” Pulse Width	30		ns	
SCL	TSCYCW	Serial Clock Cycle(Write)	66		ns	
	TSHW	S”L””H” Pulse Width(Write)	15		ns	
	TSLW	S”L””L” Pulse Width(Write)	15		ns	
	TSCYCR	Serial Clock Cycle(Read)	150		ns	
	TSHR	S”L””H” Pulse Width(Read)	60		ns	
	TSR	S”L””L” Pulse Width(Read)	60		ns	
D/CX	TDCS	D/CX Setup Time	5		ns	
	TDCH	D/CX Hold Time	5		ns	
SDA(DIN) (DOUT)	TSDS	Data Setup Time	15		ns	
	TSDH	Data Hold Time	5		ns	
	TACC	Access Time	5	50	ns	CLmax=30pF CLmin=8pF
	TOH	Output Disable Time	10		ns	

Note 1: IOVCC=1.65 to 3.3V, VCI=2.6 to 3.3V, VSSA=VSS=0V. Ta=-30 to 70°C (to +85°C no damage)

Note 2: The input signal rise time and fall time ( $t_r$ ,  $t_f$ ) is specified at 15 ns or less. Logic high and low levels are specified as 10% and 90% of IOVCC for Input signals.

### 15.3.3 Parallel RGB 18/16/6-bit BUS

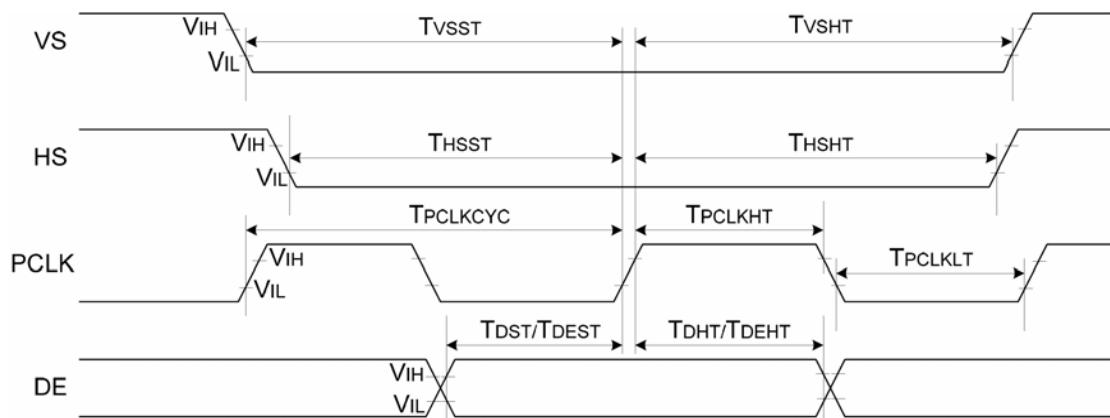


Table 15.3.3 RGB Interface Characteristics

Signal	Symbol	Parameter	MIN	MAX	UNIT	Description
PCLK	TPCLKCYC	TPCLK Cycle Time	66	-	ns	
	TPCLKLT	Pixel Low Pulse Width	15	-	ns	
	TPCLKHT	Pixel High Pulse Width	15	-	ns	
VS	TVSST	Vertical Sync.setup time	15	-	ns	
	TVSHT	Vertical Sync.hold time	15	-	ns	
HS	THSST	Horizontal Sync.setup time	15	-	ns	
	THSHT	Horizontal Sync.hold time	15	-	ns	
DE	TDEST	Data Enable Setup Time	15	-	ns	
	TDEHT	Data Enable Hold Time	15	-	ns	
D[17:0]	TDST	Data Setup Time	15	-	ns	
	TDHT	Data Hold Time	15	-	ns	

## 16. Revision History

Date	Revision	Page	Description
2019/10/12	V0.1	All	First Release by lvjj
2020/09/22	V0.2	4,5,6	Add some Pin Descriptions