MC68HC705J1A
MC68HRC705J1A
MC68HSC705J1A
MC68HSR705J1A

Technical Data

M68HC05
Microcontrollers

MC68HC705J1A/D
Rev. 4, 5/2002

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MC68HC705J1A
MC68HRC705J1A
MC68HSC705J1A
MC68HSR705J1A

Technical Data

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The following revision history table summarizes changes contained in this document. For your convenience, the page number designators have been linked to the appropriate location.

Revision History

Date	Revision Level	Description	Page Number(s)
May, 2002	4.0	**Figure 2-2. I/O Register Summary** — Corrected reset state for last entry (Mask Option Register)	37
		Figure 2-4. Mask Option Register (MOR) — Corrected reset state	41
		6.3.3 Pulldown Register A — Corrected note	91
		6.4.3 Pulldown Register B — Corrected note	94

List of Sections

Section 1. General Description 21

Section 2. Memory 33

Section 3. Central Processor Unit (CPU) 45

Section 4. Resets and Interrupts .69

Section 5. Low-Power Modes. 79

Section 6. Parallel Input/Output (I/O) Ports 87

Section 7. Computer Operating Properly (COP) Module 97

Section 8. External Interrupt Module (IRQ). 101

Section 9. Multifunction Timer Module 109

Section 10. Electrical Specifications. 117

Section 11. Mechanical Specifications 131

Section 12. Ordering Information 135

Appendix A. MC68HRC705J1A .137

Appendix B. MC68HSC705J1A .141

Appendix C. MC68HSR705J1A .145

Index. 151

List of Sections

Table of Contents

Section 1. General Description

1.1 Contents 21
1.2 Introduction 22
1.3 Features 24
1.4 Programmable Options 25
1.5 Pin Assignments 25
1.5.1 V_{DD} and V_{SS} 25
1.5.2 OSC1 and OSC2 27
1.5.2.1 Crystal Oscillator 27
1.5.2.2 Ceramic Resonator Oscillator 28
1.5.2.3 RC Oscillator 30
1.5.2.4 External Clock 30
1.6 $\overline{\text{RESET}}$ 30
1.7 $\overline{\text{IRQ}}/V_{PP}$ 31
1.8 PA0–PA7 31
1.9 PB0–PB5 31

Section 2. Memory

2.1 Contents 33
2.2 Introduction 33
2.3 Memory Map 34
2.4 Input/Output Register Summary 35
2.5 RAM 37

2.6 EPROM/OTPROM 38
2.6.1 EPROM/OTPROM Programming 38
2.6.2 EPROM Programming Register 39
2.6.3 EPROM Erasing 40

2.7 Mask Option Register 40

2.8 EPROM Programming Characteristics 43

Section 3. Central Processor Unit (CPU)

3.1 Contents 45

3.2 Introduction 46

3.3 CPU Control Unit 46

3.4 Arithmetic/Logic Unit 46

3.5 CPU Registers 48
3.5.1 Accumulator 48
3.5.2 Index Register 48
3.5.3 Stack Pointer 49
3.5.4 Program Counter 50
3.5.5 Condition Code Register 50

3.6 Instruction Set 52
3.6.1 Addressing Modes 52
3.6.1.1 Inherent 52
3.6.1.2 Immediate 52
3.6.1.3 Direct 53
3.6.1.4 Extended 53
3.6.1.5 Indexed, No Offset 53
3.6.1.6 Indexed, 8-Bit Offset 53
3.6.1.7 Indexed, 16-Bit Offset 54
3.6.1.8 Relative 54
3.6.2 Instruction Types 55
3.6.2.1 Register/Memory Instructions 55
3.6.2.2 Read-Modify-Write Instructions 56
3.6.2.3 Jump/Branch Instructions 57
3.6.2.4 Bit Manipulation Instructions 59
3.6.2.5 Control Instructions 60

3.7 Instruction Set Summary 61

3.8 Opcode Map 66

Section 4. Resets and Interrupts

4.1 Contents 69

4.2 Introduction 69

4.3 Resets. 70
4.3.1 Power-On Reset 71
4.3.2 External Reset 72
4.3.3 COP Watchdog Reset 72
4.3.4 Illegal Address Reset 72

4.4 Interrupts. 73
4.4.1 Software Interrupt. 73
4.4.2 External Interrupt 73
4.4.3 Timer Interrupts 76
4.4.3.1 Real-Time Interrupt 76
4.4.3.2 Timer Overflow Interrupt 76
4.4.4 Interrupt Processing 76

Section 5. Low-Power Modes

5.1 Contents 79

5.2 Introduction 79

5.3 Exiting Stop and Wait Modes 80

5.4 Effects of Stop and Wait Modes 81
5.4.1 Clock Generation 81
5.4.2 CPU 82
5.4.3 COP Watchdog 82
5.4.4 Timer 83
5.4.5 EPROM/OTPROM 84
5.4.6 Data-Retention Mode 84

5.5 Timing 85

Section 6. Parallel Input/Output (I/O) Ports

6.1 Contents 87

6.2 Introduction 87

6.3 Port A 89
6.3.1 Port A Data Register 89
6.3.2 Data Direction Register A 90
6.3.3 Pulldown Register A 91
6.3.4 Port A LED Drive Capability 92
6.3.5 Port A I/O Pin Interrupts 92

6.4 Port B 92
6.4.1 Port B Data Register 92
6.4.2 Data Direction Register B 93
6.4.3 Pulldown Register B 94

6.5 5.0-Volt I/O Port Electrical Characteristics 95

6.6 3.3-Volt I/O Port Electrical Characteristics 95

Section 7. Computer Operating Properly (COP) Module

7.1 Contents 97

7.2 Introduction 97

7.3 Operation 98
7.3.1 COP Watchdog Timeout 98
7.3.2 COP Watchdog Timeout Period 98
7.3.3 Clearing the COP Watchdog 98

7.4 Interrupts. 99

7.5 COP Register 99

7.6 Low-Power Modes 100
7.6.1 Stop Mode 100
7.6.2 Wait Mode 100

Section 8. External Interrupt Module (IRQ)

8.1 Contents 101

8.2 Introduction 101

8.3 Operation 102
8.3.1 $\overline{\text{IRQ}}/V_{PP}$ Pin 104
8.3.2 Optional External Interrupts 104

8.4 IRQ Status and Control Register 106

8.5 External Interrupt Timing 107
8.5.1 5.0-Volt External Interrupt Timing Characteristics 107
8.5.2 3.3-Volt External Interrupt Timing Characteristics 107

Section 9. Multifunction Timer Module

9.1 Contents 109

9.2 Introduction 109

9.3 Operation 111

9.4 Interrupts 112

9.5 I/O Registers 112
9.5.1 Timer Status and Control Register 112
9.5.2 Timer Counter Register 114

9.6 Low-Power Modes 115
9.6.1 Stop Mode 115
9.6.2 Wait Mode 115

Section 10. Electrical Specifications

10.1 Contents 117

10.2 Introduction 117

10.3 Maximum Ratings 118

10.4 Operating Temperature Range 119

10.5 Thermal Characteristics 119

10.6 Power Considerations. 120
10.7 5.0-Volt DC Electrical Characteristics. 121
10.8 3.3-Volt DC Electrical Characteristics 122
10.9 Driver Characteristics 123
10.10 Typical Supply Currents 125
10.11 EPROM Programming Characteristics 126
10.12 5.0-Volt Control Timing 126
10.13 3.3-Volt Control Timing 127

Section 11. Mechanical Specifications

11.1 Contents 131
11.2 Introduction. 131
11.3 Plastic Dual In-Line Package (Case 738). 132
11.4 Small Outline Integrated Circuit (Case 751) 132
11.5 Ceramic Dual In-Line Package (Case 732) 133

Section 12. Ordering Information

12.1 Contents 135
12.2 Introduction. 135
12.3 MCU Order Numbers 135

Appendix A. MC68HRC705J1A

A.1 Contents 137
A.2 Introduction. 137
A.3 RC Oscillator Connections 138
A.4 Typical Internal Operating Frequency for RC Oscillator Option. 139
A.5 Package Types and Order Numbers .140

Appendix B. MC68HSC705J1A

B.1 Contents 141

B.2 Introduction 141

B.3 5.0-Volt DC Electrical Characteristics 142

B.4 3.3-Volt DC Electrical Characteristics 142

B.5 Typical Supply Currents 142

B.6 Package Types and Order Numbers 144

Appendix C. MC68HSR705J1A

C.1 Contents 145

C.2 Introduction 145

C.3 RC Oscillator Connections (External Resistor) 145

C.4 Typical Internal Operating Frequency at 25°C
for High-Speed RC Oscillator Option 146

C.5 RC Oscillator Connections (No External Resistor) 147

C.6 Typical Internal Operating Frequency versus Temperature
(No External Resistor) 148

C.7 Package Types and Order Numbers 149

Index

Index 151

List of Figures

Figure	Title	Page
1-1	Block Diagram	23
1-2	Pin Assignments	26
1-3	Bypassing Layout Recommendation	26
1-4	Crystal Connections with Oscillator Internal Resistor Mask Option	28
1-5	Crystal Connections without Oscillator Internal Resistor Mask Option	28
1-6	Ceramic Resonator Connections with Oscillator Internal Resistor Mask Option	29
1-7	Ceramic Resonator Connections without Oscillator Internal Resistor Mask Option	29
1-8	External Clock Connections	30
2-1	Memory Map	34
2-2	I/O Register Summary	35
2-3	EPROM Programming Register (EPROG)	39
2-4	Mask Option Register (MOR)	41
3-1	Programming Model	47
3-2	Accumulator (A)	48
3-3	Index Register (X)	48
3-4	Stack Pointer (SP)	49
3-5	Program Counter (PC)	50
3-6	Condition Code Register (CCR)	50
4-1	Reset Sources	70
4-2	Power-On Reset Timing	71

List of Figures

Figure Title Page

4-3 External Reset Timing 72
4-4 External Interrupt Logic 74
4-5 External Interrupt Timing 75
4-6 Interrupt Stacking Order 77
4-7 Interrupt Flowchart 78

5-1 Stop Mode Recovery Timing 85
5-2 Stop/Halt/Wait Flowchart 86

6-1 Parallel I/O Port Register Summary .88
6-2 Port A Data Register (PORTA). 89
6-3 Data Direction Register A (DDRA) 90
6-4 Port A I/O Circuitry 90
6-5 Pulldown Register A (PDRA) 91
6-6 Port B Data Register (PORTB). 92
6-7 Data Direction Register B (DDRB) 93
6-8 Port B I/O Circuitry 93
6-9 Pulldown Register B (PDRB) 94

7-1 COP Register (COPR) 99

8-1 IRQ Module Block Diagram 102
8-2 Interrupt Flowchart 103
8-3 IRQ Status and Control Register (ISCR) 106
8-4 External Interrupt Timing 107

9-1 Multifunction Timer Block Diagram. 110
9-2 I/O Register Summary 111
9-3 Timer Status and Control Register (TSCR) 112
9-4 Timer Counter Register (TCR) 114

Figure	Title	Page
10-1	PA0–PA7, PB0–PB5 Typical High-Side Driver Characteristics	123
10-2	PA0–PA3, PB0–PB5 Typical Low-Side Driver Characteristics	123
10-3	PA4–PA7 Typical Low-Side Driver Characteristics	124
10-4	Typical Operating I_{DD} (25°C)	125
10-5	Typical Wait Mode I_{DD} (25°C)	125
10-6	External Interrupt Timing	128
10-7	Stop Mode Recovery Timing	128
10-8	Power-On Reset Timing	129
10-9	External Reset Timing	129
A-1	RC Oscillator Connections	138
A-2	Typical Internal Operating Frequency for Various V_{DD} at 25°C — RC Oscillator Option Only	139
B-1	Typical High-Speed Operating I_{DD} (25°C)	142
B-2	Typical High-Speed Wait Mode I_{DD} (25°C)	143
C-1	Typical Internal Operating Frequency at 25°C for High-Speed RC Oscillator Option	146
C-2	RC Oscillator Connections (No External Resistor)	147
C-3	Typical Internal Operating Frequency versus Temperature (OSCRES Bit = 1)	148

List of Figures

List of Tables

Table	Title	Page
1-1	Programmable Options	25
3-1	Register/Memory Instructions	55
3-2	Read-Modify-Write Instructions	56
3-3	Jump and Branch Instructions	58
3-4	Bit Manipulation Instructions	59
3-5	Control Instructions	60
3-6	Instruction Set Summary	61
3-7	Opcode Map	67
4-1	External Reset Timing	72
4-2	External Interrupt Timing (V_{DD} = 5.0 Vdc)	75
4-3	External Interrupt Timing (V_{DD} = 3.3 Vdc)	75
4-4	Reset/Interrupt Vector Addresses	77
6-1	Port A Pin Operation	91
6-2	Port B Pin Operation	94
9-1	Real-Time Interrupt Rate Selection	114
12-1	Order Numbers	135
A-1	MC68HRC705J1A (RC Oscillator Option) Order Numbers	140
B-1	MC68HSC705J1A (High Speed) Order Numbers	144
C-1	MC68HSR705J1A (High-Speed RC Oscillator Option) Order Numbers	149

List of Tables

Section 1. General Description

1.1 Contents

1.2 Introduction 22

1.3 Features 24

1.4 Programmable Options. 25

1.5 Pin Assignments 25
1.5.1 V_{DD} and V_{SS}. 25
1.5.2 OSC1 and OSC2 27
1.5.2.1 Crystal Oscillator 27
1.5.2.2 Ceramic Resonator Oscillator 28
1.5.2.3 RC Oscillator 30
1.5.2.4 External Clock 30

1.6 $\overline{\text{RESET}}$ 30

1.7 $\overline{\text{IRQ}}/V_{PP}$ 31

1.8 PA0–PA7 31

1.9 PB0–PB5 31

1.2 Introduction

The MC68HC705J1A is a member of Motorola's low-cost, high-performance M68HC05 Family of 8-bit microcontroller units (MCUs). The M68HC05 Family is based on the customer-specified integrated circuit (CSIC) design strategy. All MCUs in the family use the popular M68HC05 central processor unit (CPU) and are available with a variety of subsystems, memory sizes and types, and package types.

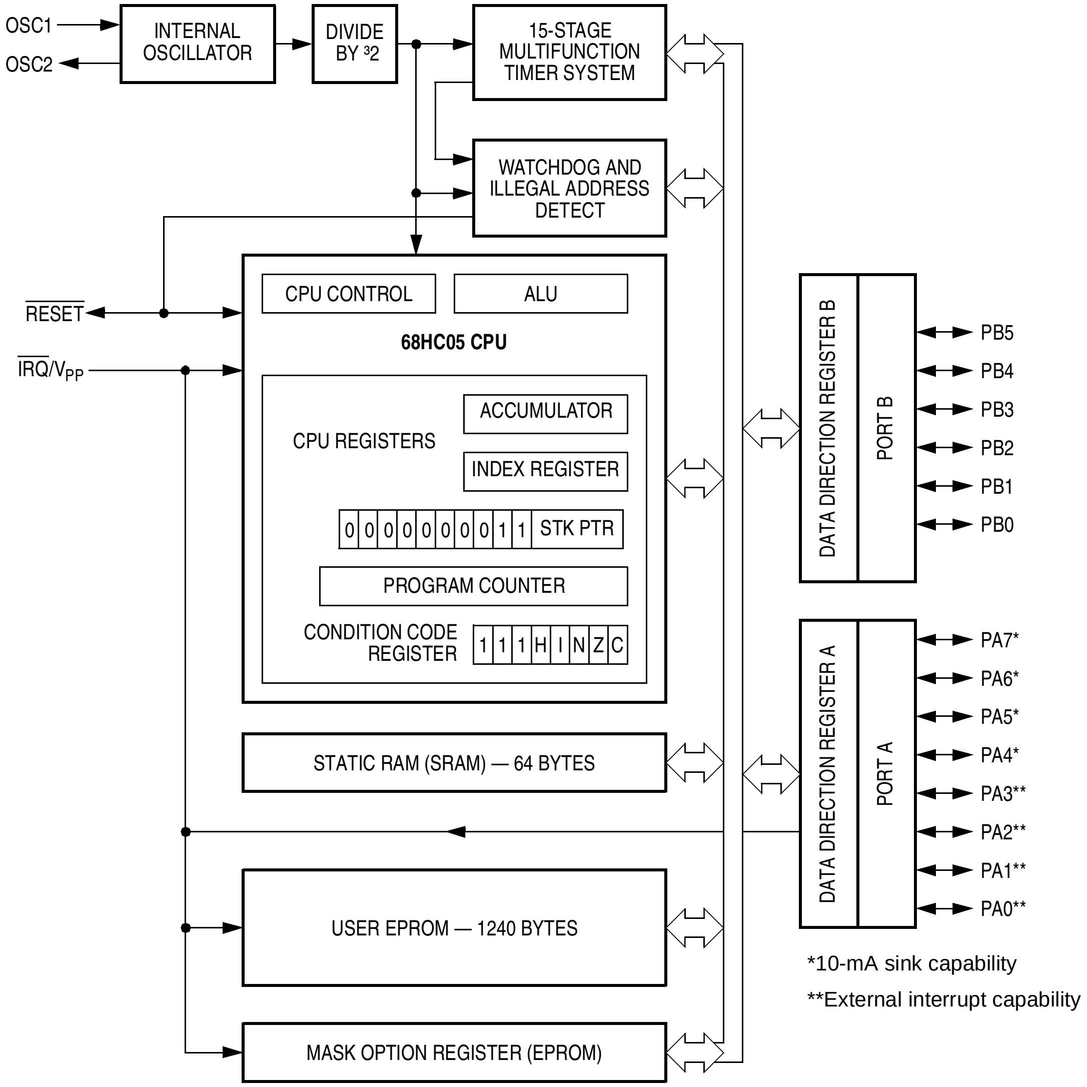
On-chip memory of the MC68HC705J1A includes 1240 bytes of erasable, programmable read-only memory (EPROM). In packages without the transparent window for EPROM erasure, the 1240 EPROM bytes serve as one-time programmable read-only memory (OTPROM).

The MC68HRC705J1A is a resistor-capacitor (RC) oscillator mask option version of the MC68HC705J1A and is discussed in **Appendix A. MC68HRC705J1A**.

A high-speed version of the MC68HC705J1A, the MC68HSC705J1A, is discussed in **Appendix B. MC68HSC705J1A**.

The MC68HSR705J1A, discussed in **Appendix C. MC68HSR705J1A**, is a high-speed version of the MC68HRC705J1A.

A functional block diagram of the MC68HC705J1A is shown in **Figure 1-1**.


OSC1
OSC2
INTERNAL OSCILLATOR
DIVIDE BY ³2
15-STAGE MULTIFUNCTION TIMER SYSTEM
WATCHDOG AND ILLEGAL ADDRESS DETECT
RESET
IRQ/VPP
CPU CONTROL
ALU
68HC05 CPU
CPU REGISTERS
ACCUMULATOR
INDEX REGISTER
0 0 0 0 0 0 0 0 1 1 STK PTR
PROGRAM COUNTER
CONDITION CODE REGISTER
1 1 1 H I N Z C
STATIC RAM (SRAM) — 64 BYTES
USER EPROM — 1240 BYTES
MASK OPTION REGISTER (EPROM)
DATA DIRECTION REGISTER B
PORT B
PB5
PB4
PB3
PB2
PB1
PB0
DATA DIRECTION REGISTER A
PORT A
PA7*
PA6*
PA5*
PA4*
PA3**
PA2**
PA1**
PA0**

*10-mA sink capability

**External interrupt capability

Figure 1-1. Block Diagram

1.3 Features

Features of the MC68HC705J1A include:

- Peripheral modules:
  - 15-stage multifunction timer
  - Computer operating properly (COP) watchdog
- 14 bidirectional input/output (I/O) lines, including:
  - 10-mA sink capability on four I/O pins
  - Mask option register (MOR) and software programmable pulldowns on all I/O pins
  - MOR selectable interrupt on four I/O pins, a keyboard scan feature
- MOR selectable sensitivity on external interrupt (edge- and level-sensitive or edge-sensitive only)
- On-chip oscillator with connections for:
  - Crystal
  - Ceramic resonator
  - Resistor-capacitor (RC) oscillator
  - External clock
- 1240 bytes of EPROM/OTPROM, including eight bytes for user vectors
- 64 bytes of user random-access memory (RAM)
- Memory-mapped I/O registers
- Fully static operation with no minimum clock speed
- Power-saving stop, halt, wait, and data-retention modes
- External interrupt mask bit and acknowledge bit
- Illegal address reset
- Internal steering diode and pullup resistor from $\overline{\text{RESET}}$ pin to V_{DD}

1.4 Programmable Options

The options in **Table 1-1** are programmable in the mask option register (MOR).

Table 1-1. Programmable Options

Feature	Option
COP watchdog timer	Enabled or disabled
External interrupt triggering	Edge-sensitive only or edge- and level-sensitive
Port A $\overline{\text{IRQ}}$ pin interrupts	Enabled or disabled
Port pulldown resistors	Enabled or disabled
STOP instruction mode	Stop mode or halt mode
Crystal oscillator internal resistor	Enabled or disabled
EPROM security	Enabled or disabled
Short oscillator delay counter	Enabled or disabled

1.5 Pin Assignments

Figure 1-2 shows the MC68HC705J1A pin assignments.

1.5.1 V_{DD} and V_{SS}

V_{DD} and V_{SS} are the power supply and ground pins. The MCU operates from a single power supply.

Very fast signal transitions occur on the MCU pins, placing high, short-duration current demands on the power supply. To prevent noise problems, take special care as **Figure 1-3** shows, by placing the bypass capacitors as close as possible to the MCU. C2 is an optional bulk current bypass capacitor for use in applications that require the port pins to source high current levels.

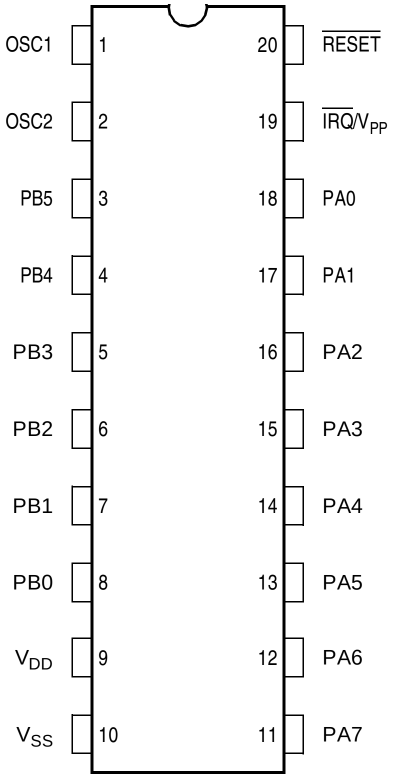

OSC1
1
OSC2
2
PB5
3
PB4
4
PB3
5
PB2
6
PB1
7
PB0
8
V_{DD}
9
V_{SS}
10
20
$\overline{RESET}$
19
$\overline{IRQ}/V_{PP}$
18
PA0
17
PA1
16
PA2
15
PA3
14
PA4
13
PA5
12
PA6
11
PA7

Figure 1-2. Pin Assignments

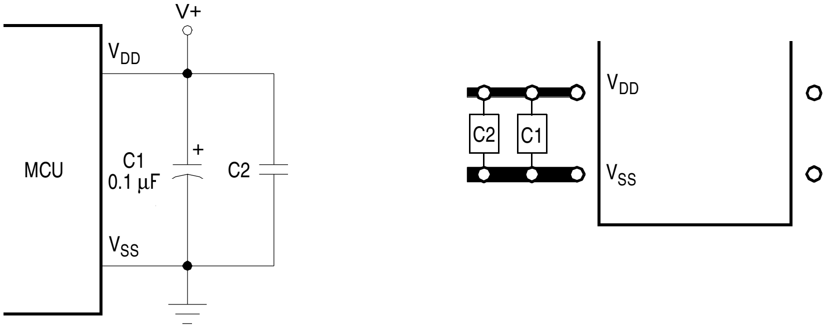

V+
V_{DD}
MCU
C1
0.1 µF
+
C2
V_{SS}
C2
C1
V_{DD}
V_{SS}

Figure 1-3. Bypassing Layout Recommendation

1.5.2 OSC1 and OSC2

The OSC1 and OSC2 pins are the connections for the on-chip oscillator. The oscillator can be driven by any of these:

1. Crystal (See **Figure 1-4** and **Figure 1-5**.)
2. Ceramic resonator (See **Figure 1-6** and **Figure 1-7**.)
3. Resistor/capacitor (RC) oscillator (Refer to **Appendix A. MC68HRC705J1A** and **Appendix C. MC68HSR705J1A**.)
4. External clock signal (See **Figure 1-8**.)

The frequency, f_{OSC}, of the oscillator or external clock source is divided by two to produce the internal operating frequency, f_{op}.

1.5.2.1 Crystal Oscillator

Figure 1-4 and **Figure 1-5** show a typical crystal oscillator circuit for an AT-cut, parallel resonant crystal. Follow the crystal supplier's recommendations, as the crystal parameters determine the external component values required to provide reliable startup and maximum stability. The load capacitance values used in the oscillator circuit design should include all stray layout capacitances.

To minimize output distortion, mount the crystal and capacitors as close as possible to the pins. An internal startup resistor of approximately 2 MΩ is provided between OSC1 and OSC2 for the crystal oscillator as a programmable mask option.

NOTE: *Use an AT-cut crystal and not an AT-strip crystal because the MCU can overdrive an AT-strip crystal.*

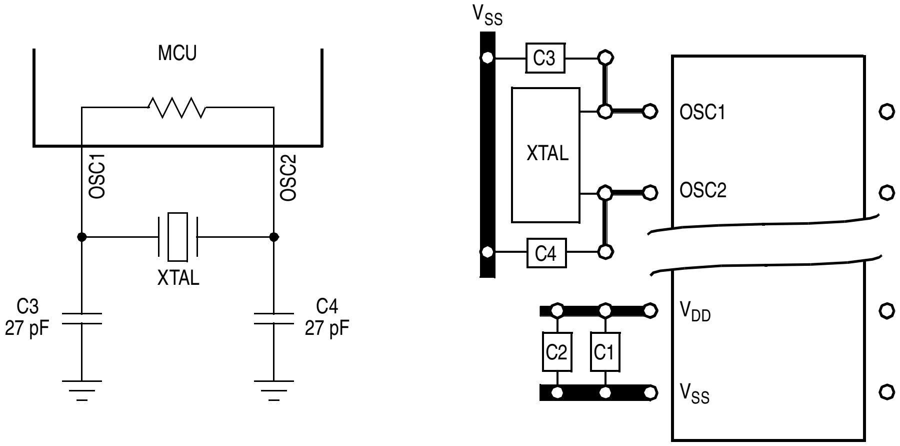

MCU
OSC1
OSC2
XTAL
C3
27 pF
C4
27 pF
V_SS
C3
XTAL
C4
OSC1
OSC2
V_DD
V_SS
C2
C1

Figure 1-4. Crystal Connections with Oscillator Internal Resistor Mask Option

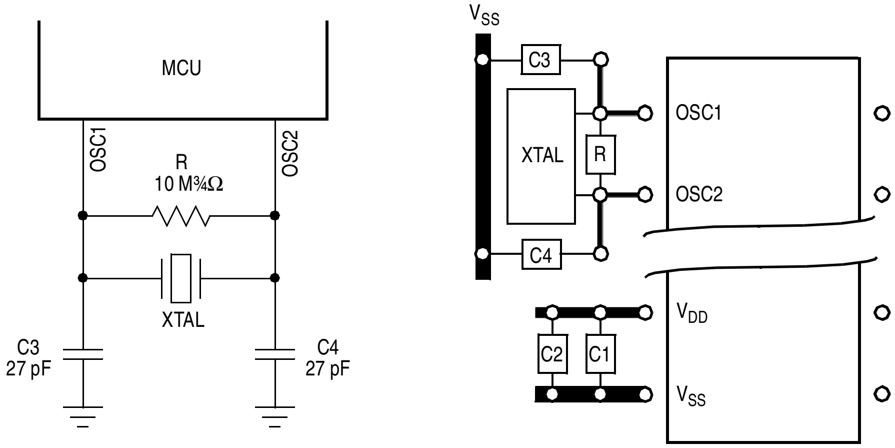

MCU
OSC1
OSC2
R
10 M¾Ω
XTAL
C3
27 pF
C4
27 pF
V_SS
C3
XTAL
R
C4
OSC1
OSC2
V_DD
V_SS
C2
C1

Figure 1-5. Crystal Connections without Oscillator Internal Resistor Mask Option

1.5.2.2 Ceramic Resonator Oscillator

To reduce cost, use a ceramic resonator instead of the crystal. The circuits shown in **Figure 1-6** and **Figure 1-7** show ceramic resonator circuits. Follow the resonator manufacturer's recommendations, as the resonator parameters determine the external component values required for maximum stability and reliable starting. The load capacitance values used in the oscillator circuit design should include all stray capacitances.

Mount the resonator and components as close as possible to the pins for startup stabilization and to minimize output distortion. An internal startup resistor of approximately 2 MΩ is provided between OSC1 and OSC2 as a programmable mask option.

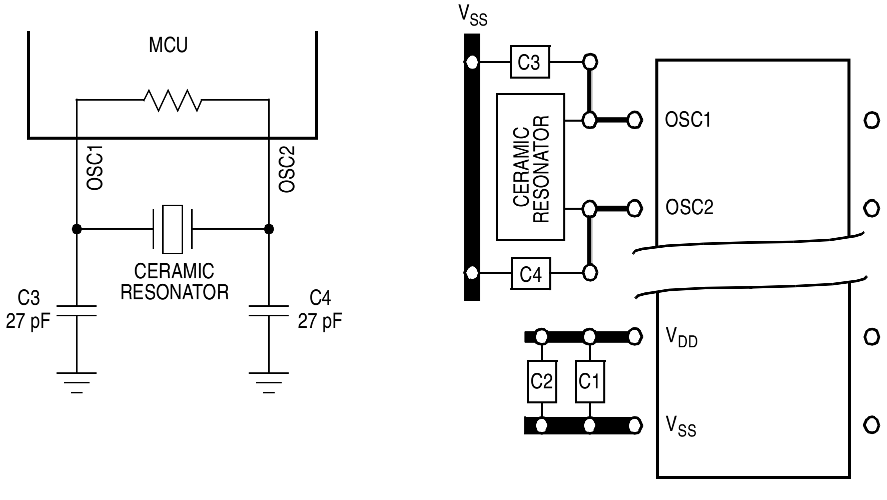

MCU
OSC1
OSC2
CERAMIC RESONATOR
C3
27 pF
C4
27 pF
V_{SS}
C3
CERAMIC RESONATOR
C4
OSC1
OSC2
V_{DD}
V_{SS}
C2
C1

Figure 1-6. Ceramic Resonator Connections with Oscillator Internal Resistor Mask Option

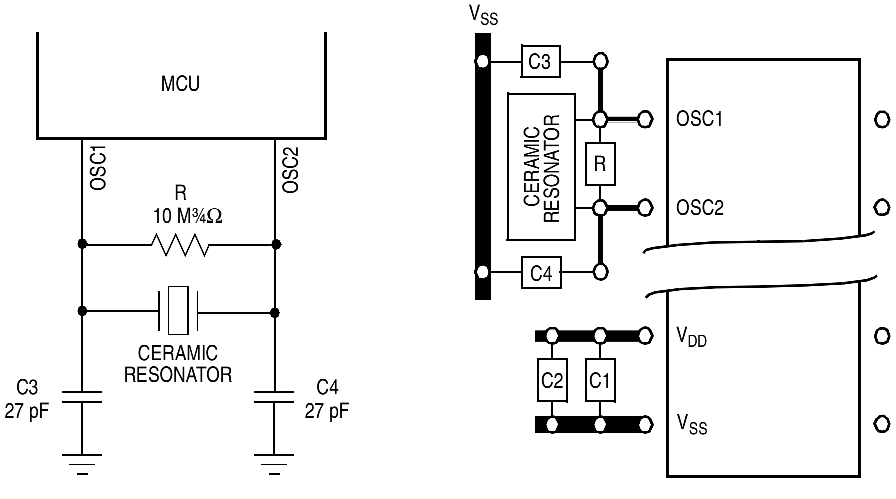

MCU
OSC1
OSC2
R
10 M¾Ω
CERAMIC RESONATOR
C3
27 pF
C4
27 pF
V_{SS}
C3
CERAMIC RESONATOR
R
C4
OSC1
OSC2
V_{DD}
V_{SS}
C2
C1

Figure 1-7. Ceramic Resonator Connections without Oscillator Internal Resistor Mask Option

1.5.2.3 RC Oscillator

Refer to **Appendix A. MC68HRC705J1A** and **Appendix C. MC68HSR705J1A**.

1.5.2.4 External Clock

An external clock from another complementary metal-oxide semiconductor (CMOS)-compatible device can be connected to the OSC1 input, with the OSC2 input not connected, as shown in **Figure 1-8**. This configuration is possible regardless of whether the crystal/ceramic resonator or the RC oscillator is enabled.

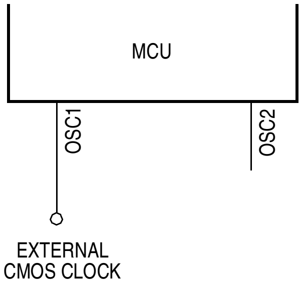


Figure 1-8. External Clock Connections

1.6 $\overline{\text{RESET}}$

Applying a logic 0 to the $\overline{\text{RESET}}$ pin forces the MCU to a known startup state. An internal reset also pulls the $\overline{\text{RESET}}$ pin low. An internal resistor to V_{DD} pulls the $\overline{\text{RESET}}$ pin high. A steering diode between the $\overline{\text{RESET}}$ and V_{DD} pins discharges any $\overline{\text{RESET}}$ pin voltage when power is removed from the MCU. The $\overline{\text{RESET}}$ pin contains an internal Schmitt trigger to improve its noise immunity as an input. Refer to **Section 4. Resets and Interrupts** for more information.

1.7 $\overline{\text{IRQ}}/V_{PP}$

The external interrupt/programming voltage pin ($\overline{\text{IRQ}}/V_{PP}$) drives the asynchronous IRQ interrupt function of the CPU. Additionally, it is used to program the user EPROM and mask option register. (See **Section 2. Memory** and **Section 8. External Interrupt Module (IRQ)**.)

The LEVEL bit in the mask option register provides negative edge-sensitive triggering or both negative edge-sensitive and low level-sensitive triggering for the interrupt function.

If level-sensitive triggering is selected, the $\overline{\text{IRQ}}/V_{PP}$ input requires an external resistor to V_{DD} for wired-OR operation. If the $\overline{\text{IRQ}}/V_{PP}$ pin is not used, it must be tied to the V_{DD} supply.

The $\overline{\text{IRQ}}/V_{PP}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity. The voltage on this pin should not exceed V_{DD} except when the pin is being used for programming the EPROM.

NOTE: *The mask option register can enable the PA0–PA3 pins to function as external interrupt pins.*

1.8 PA0–PA7

These eight input/output (I/O) lines comprise port A, a general-purpose, bidirectional I/O port. See **Section 8. External Interrupt Module (IRQ)** for information on PA0–PA3 external interrupts.

1.9 PB0–PB5

These six I/O lines comprise port B, a general-purpose, bidirectional I/O port.

Section 2. Memory

2.1 Contents

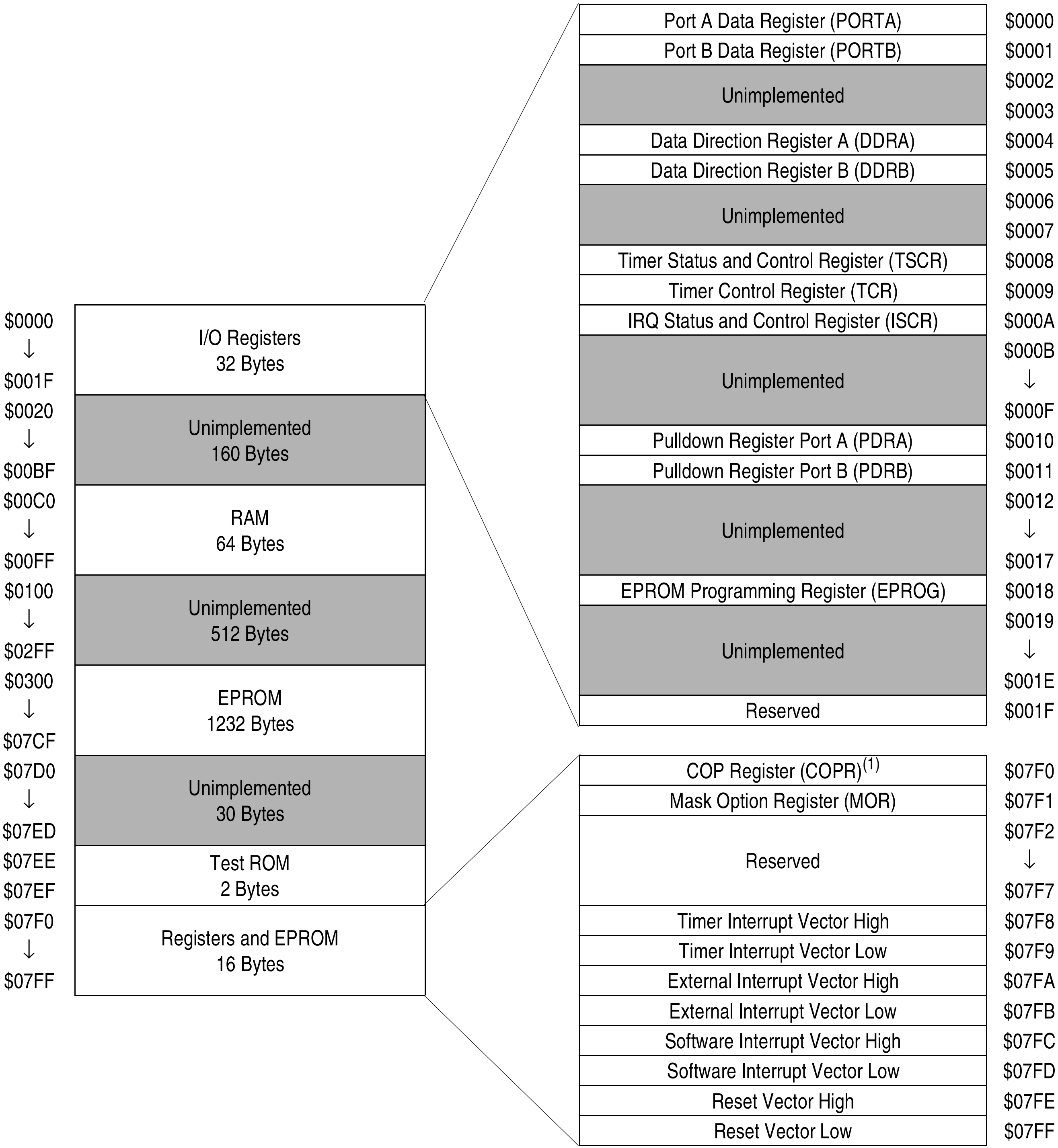
2.2 Introduction 33
2.3 Memory Map 34
2.4 Input/Output Register Summary 35
2.5 RAM 37
2.6 EPROM/OTPROM 38
2.6.1 EPROM/OTPROM Programming 38
2.6.2 EPROM Programming Register 39
2.6.3 EPROM Erasing 40
2.7 Mask Option Register 40
2.8 EPROM Programming Characteristics 43

2.2 Introduction

This section describes the organization of the on-chip memory consisting of:

- 1232 bytes of user erasable, programmable read-only memory (EPROM), plus eight bytes for user vectors
- 64 bytes of user random-access memory (RAM)

2.3 Memory Map



Address	Contents
\$0000 ↓ \$001F	I/O Registers 32 Bytes
\$0020 ↓ \$00BF	Unimplemented 160 Bytes
\$00C0 ↓ \$00FF	RAM 64 Bytes
\$0100 ↓ \$02FF	Unimplemented 512 Bytes
\$0300 ↓ \$07CF	EPROM 1232 Bytes
\$07D0 ↓ \$07ED	Unimplemented 30 Bytes
\$07EE \$07EF	Test ROM 2 Bytes
\$07F0 ↓ \$07FF	Registers and EPROM 16 Bytes

Register	Address
Port A Data Register (PORTA)	\$0000
Port B Data Register (PORTB)	\$0001
Unimplemented	\$0002 \$0003
Data Direction Register A (DDRA)	\$0004
Data Direction Register B (DDRB)	\$0005
Unimplemented	\$0006 \$0007
Timer Status and Control Register (TSCR)	\$0008
Timer Control Register (TCR)	\$0009
IRQ Status and Control Register (ISCR)	\$000A
Unimplemented	\$000B ↓ \$000F
Pulldown Register Port A (PDRA)	\$0010
Pulldown Register Port B (PDRB)	\$0011
Unimplemented	\$0012 ↓ \$0017
EPROM Programming Register (EPROG)	\$0018
Unimplemented	\$0019 ↓ \$001E
Reserved	\$001F

Register	Address
COP Register (COPR)(1)	\$07F0
Mask Option Register (MOR)	\$07F1
Reserved	\$07F2 ↓ \$07F7
Timer Interrupt Vector High	\$07F8
Timer Interrupt Vector Low	\$07F9
External Interrupt Vector High	\$07FA
External Interrupt Vector Low	\$07FB
Software Interrupt Vector High	\$07FC
Software Interrupt Vector Low	\$07FD
Reset Vector High	\$07FE
Reset Vector Low	\$07FF

(1) Writing to bit 0 of \$07F0 clears the computer operating properly (COP) watchdog.

Figure 2-1. Memory Map

2.4 Input/Output Register Summary

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PORTA) See page 89.	Read:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		Write:								
		Reset:	Unaffected by reset							
$0001	Port B Data Register (PORTB) See page 92.	Read:	0	0	PB5	PB4	PB3	PB2	PB1	PB0
		Write:	▨	▨						
		Reset:	Unaffected by reset							
$0002	Unimplemented		▨	▨	▨	▨	▨	▨	▨	▨
$0003	Unimplemented		▨	▨	▨	▨	▨	▨	▨	▨
$0004	Data Direction Register A (DDRA) See page 90.	Read:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0005	Data Direction Register B (DDRB) See page 93.	Read:	0	0	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		Write:	▨	▨						
		Reset:	0	0	0	0	0	0	0	0
$0006	Unimplemented		▨	▨	▨	▨	▨	▨	▨	▨
$0007	Unimplemented		▨	▨	▨	▨	▨	▨	▨	▨
$0008	Timer Status and Control Register (TSCR) See page 112.	Read:	TOF	RTIF	TOIE	RTIE	0	0	RT1	RT0
		Write:	▨	▨			TOFR	RTIFR		
		Reset:	0	0	0	0	0	0	1	1

▨ = Unimplemented R = Reserved

Figure 2-2. I/O Register Summary (Sheet 1 of 3)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0009	Timer Counter Register (TCR) See page 114.	Read:	TMR7	TMR6	TMR5	TMR4	TMR3	TMR2	TMR1	TMR0
		Write:	▨	▨	▨	▨	▨	▨	▨	▨
		Reset:	0	0	0	0	0	0	0	0
$000A	IRQ Status and Control Register (ISCR) See page 106.	Read:	IRQE	0	0	0	IRQF	0	0	0
		Write:		▨	▨	R	▨	▨	IRQR	▨
		Reset:	1	0	0	0	0	0	0	0
$000B	Unimplemented		▨	▨	▨	▨	▨	▨	▨	▨
↓										
$000F	Unimplemented		▨	▨	▨	▨	▨	▨	▨	▨
$0010	Pulldown Register A (PDRA) See page 91.	Read:	▨	▨	▨	▨	▨	▨	▨	▨
		Write:	PDIA7	PDIA6	PDIA5	PDIA4	PDIA3	PDIA2	PDIA1	PDIA0
		Reset:	0	0	0	0	0	0	0	0
$0011	Pulldown Register B (PDRB) See page 94.	Read:	▨	▨	▨	▨	▨	▨	▨	▨
		Write:	▨	▨	PDIB5	PDIB4	PDIB3	PDIB2	PDIB1	PDIB0
		Reset:	0	0	0	0	0	0	0	0
$0012	Unimplemented		▨	▨	▨	▨	▨	▨	▨	▨
↓										
$0017	Unimplemented		▨	▨	▨	▨	▨	▨	▨	▨
$0018	EPROM Programming Register (EPROG) See page 39.	Read:	0	0	0	0	0	ELAT	MPGM	EPGM
		Write:	▨	R	R	R	R			
		Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented R = Reserved

Figure 2-2. I/O Register Summary (Sheet 2 of 3)

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0019	Unimplemented		▨	▨	▨	▨	▨	▨	▨	▨
↓										
$001E	Unimplemented		▨	▨	▨	▨	▨	▨	▨	▨
$001F	Reserved		R	R	R	R	R	R	R	R
$07F0	COP Register (COPR) See page 99.	Read:	▨	▨	▨	▨	▨	▨	▨	▨
		Write:	▨	▨	▨	▨	▨	▨	▨	COPC
		Reset:								0
$07F1	Mask Option Register (MOR) See page 41.	Read:	SOSCD	EPMSEC	OSCRES	SWAIT	SWPDI	PIRQ	LEVEL	COPEN
		Write:								
		Reset:	Unaffected by reset							

▨ = Unimplemented R = Reserved

Figure 2-2. I/O Register Summary (Sheet 3 of 3)

2.5 RAM

The 64 addresses from $00C0 to $00FF serve as both the user RAM and the stack RAM. Before processing an interrupt, the central processor unit (CPU) uses five bytes of the stack to save the contents of the CPU registers. During a subroutine call, the CPU uses two bytes of the stack to store the return address. The stack pointer decrements when the CPU stores a byte on the stack and increments when the CPU retrieves a byte from the stack.

NOTE: *Be careful when using nested subroutines or multiple interrupt levels. The CPU may overwrite data in the RAM during a subroutine or during the interrupt stacking operation.*

2.6 EPROM/OTPROM

A microcontroller unit (MCU) with a quartz window has 1240 bytes of erasable, programmable ROM (EPROM). The quartz window allows EPROM erasure with ultraviolet light.

NOTE: *Keep the quartz window covered with an opaque material except when programming the MCU. Ambient light can affect MCU operation.*

In an MCU without the quartz window, the EPROM cannot be erased and serves as 1240 bytes of one-time programmable ROM (OTPROM).

These addresses are user EPROM/OTPROM locations:

- $0300–$07CF
- $07F8–$07FF, used for user-defined interrupt and reset vectors

The computer operating properly (COP) register (COPR) is an EPROM/OTPROM location at address $07F0.

The mask option register (MOR) is an EPROM/OTPROM location at address $07F1.

2.6.1 EPROM/OTPROM Programming

The two ways to program the EPROM/OTPROM are:

1. Manipulating the control bits in the EPROM programming register to program the EPROM/OTPROM on a byte-by-byte basis
2. Programming the EPROM/OTPROM with the M68HC705J in-circuit simulator (M68HC705JICS) available from Freescale

2.6.2 EPROM Programming Register

The EPROM programming register (EPROG) contains the control bits for programming the EPROM/OTPROM.

Address: $0018

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	ELAT	MPGM	EPGM
Write:	▨	R	R	R	R			
Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented R = Reserved

Figure 2-3. EPROM Programming Register (EPROG)

ELAT — EPROM Bus Latch Bit

This read/write bit latches the address and data buses for EPROM/OTPROM programming. Clearing the ELAT bit automatically clears the EPGM bit. EPROM/OTPROM data cannot be read while the ELAT bit is set. Reset clears the ELAT bit.

1 = Address and data buses configured for EPROM/OTPROM programming the EPROM
0 = Address and data buses configured for normal operation

MPGM — MOR Programming Bit

This read/write bit applies programming power from the $\overline{\text{IRQ}}/V_{PP}$ pin to the mask option register. Reset clears MPGM.

1 = Programming voltage applied to MOR
0 = Programming voltage not applied to MOR

EPGM — EPROM Programming Bit

This read/write bit applies the voltage from the $\overline{\text{IRQ}}/V_{PP}$ pin to the EPROM. To write the EPGM bit, the ELAT bit must be set already. Reset clears EPGM.

1 = Programming voltage ($\overline{\text{IRQ}}/V_{PP}$ pin) applied to EPROM
0 = Programming voltage ($\overline{\text{IRQ}}/V_{PP}$ pin) not applied to EPROM

NOTE: *Writing logic 1s to both the ELAT and EPGM bits with a single instruction sets ELAT and clears EPGM. ELAT must be set first by a separate instruction.*

Bits [7:3] — Reserved

Take these steps to program a byte of EPROM/OTPROM:

1. Apply the programming voltage, V_{PP}, to the $\overline{IRQ}/V_{PP}$ pin.
2. Set the ELAT bit.
3. Write to any EPROM/OTPROM address.
4. Set the EPGM bit and wait for a time, t_{EPGM}.
5. Clear the ELAT bit.

2.6.3 EPROM Erasing

The erased state of an EPROM bit is logic 0. Erase the EPROM by exposing it to 15 Ws/cm^2 of ultraviolet light with a wave length of 2537 angstroms. Position the ultraviolet light source one inch from the EPROM. Do not use a shortwave filter.

2.7 Mask Option Register

The mask option register (MOR) is an EPROM/OTPROM byte that controls these options:

- COP watchdog (enable or disable)
- External interrupt pin triggering (edge-sensitive only or edge- and level-sensitive)
- Port A external interrupts (enable or disable)
- Port pulldown resistors (enable or disable)
- STOP instruction (stop mode or halt mode)
- Crystal oscillator internal resistor (enable or disable)
- EPROM security (enable or disable)
- Short oscillator delay (enable or disable)

Take these steps to program the mask option register:

1. Apply the programming voltage, V_{PP}, to the $\overline{IRQ}/V_{PP}$ pin.
2. Write to the MOR.
3. Set the MPGM bit and wait for a time, t_{MPGM}.
4. Clear the MPGM bit.
5. Reset the MCU.

Address: $07F1

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SOSCD	EPMSEC	OSCRES	SWAIT	SWPDI	PIRQ	LEVEL	COPEN
Reset:	Unaffected by reset							

Figure 2-4. Mask Option Register (MOR)

SOSCD — Short Oscillator Delay Bit

The SOSCD bit controls the oscillator stabilization counter. The normal stabilization delay following reset or exit from stop mode is 4064 t_{cyc}. Setting SOSCD enables a short oscillator stabilization delay.

1 = Short oscillator delay enabled
0 = Short oscillator delay disabled

EPMSEC — EPROM Security Bit

The EPMSEC bit controls access to the EPROM/OTPROM.

1 = External access to EPROM/OTPROM denied
0 = External access to EPROM/OTPROM not denied

OSCRES — Oscillator Internal Resistor Bit

The OSCRES bit enables a 2-MΩ internal resistor in the oscillator circuit.

1 = Oscillator internal resistor enabled
0 = Oscillator internal resistor disabled

NOTE: *Program the OSCRES bit to logic 0 in devices using RC oscillators.*

SWAIT — Stop-to-Wait Conversion Bit

The SWAIT bit enables halt mode. When the SWAIT bit is set, the CPU interprets the STOP instruction as a WAIT instruction, and the MCU enters halt mode. Halt mode is the same as wait mode, except that an oscillator stabilization delay of 1 to 4064 t_{cyc} occurs after exiting halt mode.

1 = Halt mode enabled
0 = Halt mode not enabled

SWPDI — Software Pulldown Inhibit Bit

The SWPDI bit inhibits software control of the I/O port pulldown devices. The SWPDI bit overrides the pulldown inhibit bits in the port pulldown inhibit registers.

1 = Software pulldown control inhibited
0 = Software pulldown control not inhibited

PIRQ — Port A External Interrupt Bit

The PIRQ bit enables the PA0–PA3 pins to function as external interrupt pins.

1 = PA0–PA3 enabled as external interrupt pins
0 = PA0–PA3 not enabled as external interrupt pins

LEVEL —External Interrupt Sensitivity Bit

The LEVEL bit controls external interrupt triggering sensitivity.

1 = External interrupts triggered by active edges and active levels
0 = External interrupts triggered only by active edges

COPEN — COP Enable Bit

The COPEN bit enables the COP watchdog.

1 = COP watchdog enabled
0 = COP watchdog disabled

2.8 EPROM Programming Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Programming voltage $\overline{\text{IRQ}}/V_{PP}$	V_{PP}	16.0	16.5	17.0	V
Programming current $\overline{\text{IRQ}}/V_{PP}$	I_{PP}	—¦	3.0	10.0	mA
Programming time Per array byte MOR	 t_{EPGM} t_{MPGM}	 4 4	 — —	 — —	ms

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +105°C

Section 3. Central Processor Unit (CPU)

3.1 Contents

3.2 Introduction 46

3.3 CPU Control Unit 46

3.4 Arithmetic/Logic Unit. 46

3.5 CPU Registers 48
3.5.1 Accumulator 48
3.5.2 Index Register 48
3.5.3 Stack Pointer 49
3.5.4 Program Counter 50
3.5.5 Condition Code Register 50

3.6 Instruction Set. 52
3.6.1 Addressing Modes 52
3.6.1.1 Inherent 52
3.6.1.2 Immediate 52
3.6.1.3 Direct 53
3.6.1.4 Extended 53
3.6.1.5 Indexed, No Offset. 53
3.6.1.6 Indexed, 8-Bit Offset 53
3.6.1.7 Indexed, 16-Bit Offset 54
3.6.1.8 Relative 54
3.6.2 Instruction Types 55
3.6.2.1 Register/Memory Instructions .55
3.6.2.2 Read-Modify-Write Instructions 56
3.6.2.3 Jump/Branch Instructions 57
3.6.2.4 Bit Manipulation Instructions 59
3.6.2.5 Control Instructions 60

3.7 Instruction Set Summary 61

3.8 Opcode Map 66

3.2 Introduction

The central processor unit (CPU) consists of a CPU control unit, an arithmetic/logic unit (ALU), and five CPU registers. The CPU control unit fetches and decodes instructions. The ALU executes the instructions. The CPU registers contain data, addresses, and status bits that reflect the results of CPU operations. See **Figure 3-1**.

Features include:

- 2.1-MHz bus frequency
- 8-bit accumulator
- 8-bit index register
- 11-bit program counter
- 6-bit stack pointer
- Condition code register (CCR) with five status flags
- 62 instructions
- Eight addressing modes
- Power-saving stop, wait, halt, and data-retention modes

3.3 CPU Control Unit

The CPU control unit fetches and decodes instructions during program operation. The control unit selects the memory locations to read and write and coordinates the timing of all CPU operations.

3.4 Arithmetic/Logic Unit

The arithmetic/logic unit (ALU) performs the arithmetic, logic, and manipulation operations decoded from the instruction set by the CPU control unit. The ALU produces the results called for by the program and sets or clears status and control bits in the condition code register (CCR).

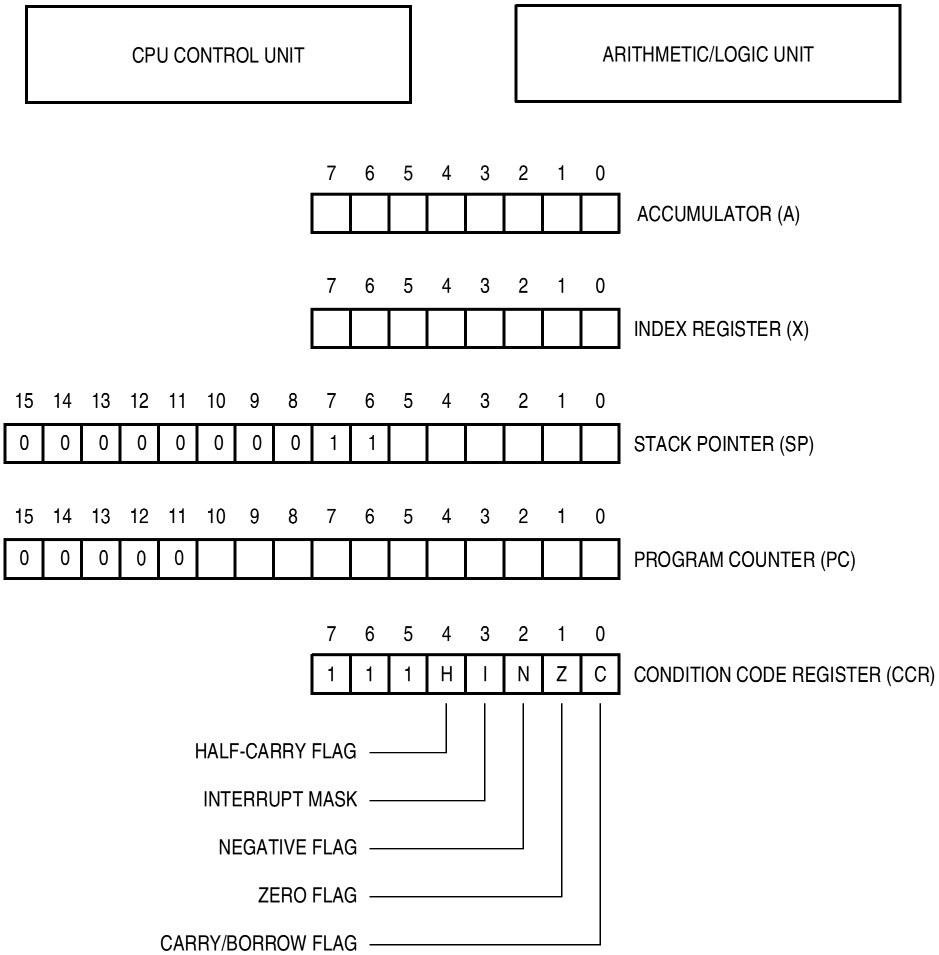

CPU CONTROL UNIT
ARITHMETIC/LOGIC UNIT
7 6 5 4 3 2 1 0
ACCUMULATOR (A)
7 6 5 4 3 2 1 0
INDEX REGISTER (X)
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0 0 0 0 0 0 0 0 1 1
STACK POINTER (SP)
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
0 0 0 0 0
PROGRAM COUNTER (PC)
7 6 5 4 3 2 1 0
1 1 1 H I N Z C
CONDITION CODE REGISTER (CCR)
HALF-CARRY FLAG
INTERRUPT MASK
NEGATIVE FLAG
ZERO FLAG
CARRY/BORROW FLAG

Figure 3-1. Programming Model

3.5 CPU Registers

The M68HC05 CPU contains five registers that control and monitor microcontroller unit (MCU) operation:

- Accumulator
- Index register
- Stack pointer
- Program counter
- Condition code register

CPU registers are not memory mapped.

3.5.1 Accumulator

The accumulator (A) is a general-purpose 8-bit register. The CPU uses the accumulator to hold operands and results of ALU operations.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:								
Write:								
Reset:	Unaffected by reset							

Figure 3-2. Accumulator (A)

3.5.2 Index Register

In the indexed addressing (X) modes, the CPU uses the byte in the index register to determine the conditional address of the operand. The index register also can serve as a temporary storage location or a counter.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:								
Write:								
Reset:	Unaffected by reset							

Figure 3-3. Index Register (X)

3.5.3 Stack Pointer

The stack pointer (SP) is a 16-bit register that contains the address of the next location on the stack. During a reset or after the reset stack pointer instruction (RSP), the stack pointer is preset to $00FF. The address in the stack pointer decrements after a byte is stacked and increments before a byte is unstacked.

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
Read:	0	0	0	0	0	0	0	0	1	1						
Write:	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨	▨
Reset:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

▨ = Unimplemented

Figure 3-4. Stack Pointer (SP)

The 10 most significant bits of the stack pointer are permanently fixed at 0000000011, so the stack pointer produces addresses from $00C0 to $00FF. If subroutines and interrupts use more than 64 stack locations, the stack pointer wraps around to address $00FF and begins writing over the previously stored data. A subroutine uses two stack locations; an interrupt uses five locations.

3.5.4 Program Counter

The program counter (PC) is a 16-bit register that contains the address of the next instruction or operand to be fetched. The five most significant bits of the program counter are ignored and appear as 00000.

Normally, the address in the program counter automatically increments to the next sequential memory location every time an instruction or operand is fetched. Jump, branch, and interrupt operations load the program counter with an address other than that of the next sequential location.

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
Read: Write:																
Reset:	0	0	0	0	0	Loaded with vector from $07FE and $07FF										

Figure 3-5. Program Counter (PC)

3.5.5 Condition Code Register

The condition code register (CCR) is an 8-bit register whose three most significant bits are permanently fixed at 111. The condition code register contains the interrupt mask and four flags that indicate the results of the instruction just executed.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	1	1	1	H	I	N	Z	C
Write:	▨	▨	▨					
Reset:	1	1	1	U	1	U	U	U

▨ = Unimplemented U = Unaffected

Figure 3-6. Condition Code Register (CCR)

H — Half-Carry Flag

The CPU sets the half-carry flag when a carry occurs between bits 3 and 4 of the accumulator during an ADD (add without carry) or ADC (add with carry) operation. The half-carry flag is required for binary-coded decimal (BCD) arithmetic operations.

I — Interrupt Mask Bit

Setting the interrupt mask disables interrupts. If an interrupt request occurs while the interrupt mask is logic 0, the CPU saves the CPU registers on the stack, sets the interrupt mask, and then fetches the interrupt vector. If an interrupt request occurs while the interrupt mask is logic 1, the interrupt request is latched. Normally, the CPU processes the latched interrupt request as soon as the interrupt mask is cleared again.

A return-from-interrupt instruction (RTI) unstacks the CPU registers, restoring the interrupt mask to its cleared state. After any reset, the interrupt mask is set and can be cleared only by a software instruction.

N — Negative Flag

The CPU sets the negative flag when an ALU operation produces a negative result.

Z — Zero Flag

The CPU sets the zero flag when an ALU operation produces a result of $00.

C — Carry/Borrow Flag

The CPU sets the carry/borrow flag when an addition operation produces a carry out of bit 7 of the accumulator or when a subtraction operation requires a borrow. Some logical operations and data manipulation instructions also clear or set the carry/borrow flag.

3.6 Instruction Set

The MCU instruction set has 62 instructions and uses eight addressing modes.

3.6.1 Addressing Modes

The CPU uses eight addressing modes for flexibility in accessing data. The addressing modes provide eight different ways for the CPU to find the data required to execute an instruction. The eight addressing modes are:

- Inherent
- Immediate
- Direct
- Extended
- Indexed, no offset
- Indexed, 8-bit offset
- Indexed, 16-bit offset
- Relative

3.6.1.1 Inherent

Inherent instructions are those that have no operand, such as return from interrupt (RTI) and stop (STOP). Some of the inherent instructions act on data in the CPU registers, such as set carry flag (SEC) and increment accumulator (INCA). Inherent instructions require no operand address and are one byte long.

3.6.1.2 Immediate

Immediate instructions are those that contain a value to be used in an operation with the value in the accumulator or index register. Immediate instructions require no operand address and are two bytes long. The opcode is the first byte, and the immediate data value is the second byte.

3.6.1.3 Direct

Direct instructions can access any of the first 256 memory locations with two bytes. The first byte is the opcode, and the second is the low byte of the operand address. In direct addressing, the CPU automatically uses $00 as the high byte of the operand address.

3.6.1.4 Extended

Extended instructions use three bytes and can access any address in memory. The first byte is the opcode; the second and third bytes are the high and low bytes of the operand address.

When using the Freescale assembler, the programmer does not need to specify whether an instruction is direct or extended. The assembler automatically selects the shortest form of the instruction.

3.6.1.5 Indexed, No Offset

Indexed instructions with no offset are 1-byte instructions that can access data with variable addresses within the first 256 memory locations. The index register contains the low byte of the effective address of the operand. The CPU automatically uses $00 as the high byte, so these instructions can address locations $0000–$00FF.

Indexed, no offset instructions are often used to move a pointer through a table or to hold the address of a frequently used RAM or input/output (I/O) location.

3.6.1.6 Indexed, 8-Bit Offset

Indexed, 8-bit offset instructions are 2-byte instructions that can access data with variable addresses within the first 511 memory locations. The CPU adds the unsigned byte in the index register to the unsigned byte following the opcode. The sum is the effective address of the operand. These instructions can access locations $0000–$01FE.

Indexed 8-bit offset instructions are useful for selecting the kth element in an n-element table. The table can begin anywhere within the first 256 memory locations and could extend as far as location 510 ($01FE).

The k value is typically in the index register, and the address of the beginning of the table is in the byte following the opcode.

3.6.1.7 Indexed, 16-Bit Offset

Indexed, 16-bit offset instructions are 3-byte instructions that can access data with variable addresses at any location in memory. The CPU adds the unsigned byte in the index register to the two unsigned bytes following the opcode. The sum is the effective address of the operand. The first byte after the opcode is the high byte of the 16-bit offset; the second byte is the low byte of the offset.

Indexed, 16-bit offset instructions are useful for selecting the kth element in an n-element table anywhere in memory.

As with direct and extended addressing, the Freescale assembler determines the shortest form of indexed addressing.

3.6.1.8 Relative

Relative addressing is only for branch instructions. If the branch condition is true, the CPU finds the effective branch destination by adding the signed byte following the opcode to the contents of the program counter. If the branch condition is not true, the CPU goes to the next instruction. The offset is a signed, two's complement byte that gives a branching range of –128 to +127 bytes from the address of the next location after the branch instruction.

When using the Freescale assembler, the programmer does not need to calculate the offset because the assembler determines the proper offset and verifies that it is within the span of the branch.

3.6.2 Instruction Types

The MCU instructions fall into these five categories:

- Register/memory instructions
- Read-modify-write instructions
- Jump/branch instructions
- Bit manipulation instructions
- Control instructions

3.6.2.1 Register/Memory Instructions

These instructions operate on CPU registers and memory locations. Most of them use two operands. One operand is in either the accumulator or the index register. The CPU finds the other operand in memory.

Table 3-1. Register/Memory Instructions

Instruction	Mnemonic
Add memory byte and carry bit to accumulator	ADC
Add memory byte to accumulator	ADD
AND memory byte with accumulator	AND
Bit test accumulator	BIT
Compare accumulator	CMP
Compare index register with memory byte	CPX
EXCLUSIVE OR accumulator with memory byte	EOR
Load accumulator with memory byte	LDA
Load index register with memory byte	LDX
Multiply	MUL
OR accumulator with memory byte	ORA
Subtract memory byte and carry bit from accumulator	SBC
Store accumulator in memory	STA
Store index register in memory	STX
Subtract memory byte from accumulator	SUB

3.6.2.2 Read-Modify-Write Instructions

These instructions read a memory location or a register, modify its contents, and write the modified value back to the memory location or to the register.

NOTE: *Do not use read-modify-write instructions on registers with write-only bits.*

Table 3-2. Read-Modify-Write Instructions

Instruction	Mnemonic
Arithmetic shift left (same as LSL)	ASL
Arithmetic shift right	ASR
Bit clear	BCLR(1)
Bit set	BSET(1)
Clear register	CLR
Complement (one's complement)	COM
Decrement	DEC
Increment	INC
Logical shift left (same as ASL)	LSL
Logical shift right	LSR
Negate (two's complement)	NEG
Rotate left through carry bit	ROL
Rotate right through carry bit	ROR
Test for negative or zero	TST(2)

1. Unlike other read-modify-write instructions, BCLR and BSET use only direct addressing.
2. TST is an exception to the read-modify-write sequence because it does not write a replacement value.

3.6.2.3 Jump/Branch Instructions

Jump instructions allow the CPU to interrupt the normal sequence of the program counter. The unconditional jump instruction (JMP) and the jump-to-subroutine instruction (JSR) have no register operand. Branch instructions allow the CPU to interrupt the normal sequence of the program counter when a test condition is met. If the test condition is not met, the branch is not performed.

The BRCLR and BRSET instructions cause a branch based on the state of any readable bit in the first 256 memory locations. These 3-byte instructions use a combination of direct addressing and relative addressing. The direct address of the byte to be tested is in the byte following the opcode. The third byte is the signed offset byte. The CPU finds the effective branch destination by adding the third byte to the program counter if the specified bit tests true. The bit to be tested and its condition (set or clear) is part of the opcode. The span of branching is from –128 to +127 from the address of the next location after the branch instruction. The CPU also transfers the tested bit to the carry/borrow bit of the condition code register.

NOTE: *Do not use BRCLR or BRSET instructions on registers with write-only bits.*

Table 3-3. Jump and Branch Instructions

Instruction	Mnemonic
Branch if carry bit clear	BCC
Branch if carry bit set	BCS
Branch if equal	BEQ
Branch if half-carry bit clear	BHCC
Branch if half-carry bit set	BHCS
Branch if higher	BHI
Branch if higher or same	BHS
Branch if $\overline{\text{IRQ}}$ pin high	BIH
Branch if $\overline{\text{IRQ}}$ pin low	BIL
Branch if lower	BLO
Branch if lower or same	BLS
Branch if interrupt mask clear	BMC
Branch if minus	BMI
Branch if interrupt mask set	BMS
Branch if not equal	BNE
Branch if plus	BPL
Branch always	BRA
Branch if bit clear	BRCLR
Branch never	BRN
Branch if bit set	BRSET
Branch to subroutine	BSR
Unconditional jump	JMP
Jump to subroutine	JSR

3.6.2.4 Bit Manipulation Instructions

The CPU can set or clear any writable bit in the first 256 bytes of memory, which includes I/O registers and on-chip RAM locations. The CPU can also test and branch based on the state of any bit in any of the first 256 memory locations.

Table 3-4. Bit Manipulation Instructions

Instruction	Mnemonic
Bit clear	BCLR
Branch if bit clear	BRCLR
Branch if bit set	BRSET
Bit set	BSET

NOTE: *Do not use bit manipulation instructions on registers with write-only bits.*

3.6.2.5 Control Instructions

These instructions act on CPU registers and control CPU operation during program execution.

Table 3-5. Control Instructions

Instruction	Mnemonic
Clear carry bit	CLC
Clear interrupt mask	CLI
No operation	NOP
Reset stack pointer	RSP
Return from interrupt	RTI
Return from subroutine	RTS
Set carry bit	SEC
Set interrupt mask	SEI
Stop oscillator and enable $\overline{\text{IRQ}}$ pin	STOP
Software interrupt	SWI
Transfer accumulator to index register	TAX
Transfer index register to accumulator	TXA
Stop CPU clock and enable interrupts	WAIT

3.7 Instruction Set Summary

Table 3-6. Instruction Set Summary (Sheet 1 of 6)

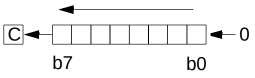
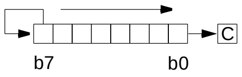
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
ADC #*opr* ADC *opr* ADC *opr* ADC *opr*,X ADC *opr*,X ADC ,X	Add with Carry	A ← (A) + (M) + (C)	↕	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A9 B9 C9 D9 E9 F9	ii dd hh ll ee ff ff	2 3 4 5 4 3
ADD #*opr* ADD *opr* ADD *opr* ADD *opr*,X ADD *opr*,X ADD ,X	Add without Carry	A ← (A) + (M)	↕	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	AB BB CB DB EB FB	ii dd hh ll ee ff ff	2 3 4 5 4 3
AND #*opr* AND *opr* AND *opr* AND *opr*,X AND *opr*,X AND ,X	Logical AND	A ← (A) ∧ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A4 B4 C4 D4 E4 F4	ii dd hh ll ee ff ff	2 3 4 5 4 3
ASL *opr* ASLA ASLX ASL *opr*,X ASL ,X	Arithmetic Shift Left (Same as LSL)		—	—	↕	↕	↕	DIR INH INH IX1 IX	38 48 58 68 78	dd ff 	5 3 3 6 5
ASR *opr* ASRA ASRX ASR *opr*,X ASR ,X	Arithmetic Shift Right		—	—	↕	↕	↕	DIR INH INH IX1 IX	37 47 57 67 77	dd ff 	5 3 3 6 5
BCC *rel*	Branch if Carry Bit Clear	PC ← (PC) + 2 + *rel* ? C = 0	—	—	—	—	—	REL	24	rr	3
BCLR *n opr*	Clear Bit n	Mn ← 0	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 13 15 17 19 1B 1D 1F	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5
BCS *rel*	Branch if Carry Bit Set (Same as BLO)	PC ← (PC) + 2 + *rel* ? C = 1	—	—	—	—	—	REL	25	rr	3
BEQ *rel*	Branch if Equal	PC ← (PC) + 2 + *rel* ? Z = 1	—	—	—	—	—	REL	27	rr	3
BHCC *rel*	Branch if Half-Carry Bit Clear	PC ← (PC) + 2 + *rel* ? H = 0	—	—	—	—	—	REL	28	rr	3
BHCS *rel*	Branch if Half-Carry Bit Set	PC ← (PC) + 2 + *rel* ? H = 1	—	—	—	—	—	REL	29	rr	3

Table 3-6. Instruction Set Summary (Sheet 2 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
BHI *rel*	Branch if Higher	PC ← (PC) + 2 + *rel* ? C ∨ Z = 0	—	—	—	—	—	REL	22	rr	3
BHS *rel*	Branch if Higher or Same	PC ← (PC) + 2 + *rel* ? C = 0	—	—	—	—	—	REL	24	rr	3
BIH *rel*	Branch if IRQ Pin High	PC ← (PC) + 2 + *rel* ? IRQ = 1	—	—	—	—	—	REL	2F	rr	3
BIL *rel*	Branch if IRQ Pin Low	PC ← (PC) + 2 + *rel* ? IRQ = 0	—	—	—	—	—	REL	2E	rr	3
BIT #*opr* BIT *opr* BIT *opr* BIT *opr*,X BIT *opr*,X BIT ,X	Bit Test Accumulator with Memory Byte	(A) ∧ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A5 B5 C5 D5 E5 F5	ii dd hh ll ee ff ff	2 3 4 5 4 3
BLO *rel*	Branch if Lower (Same as BCS)	PC ← (PC) + 2 + *rel* ? C = 1	—	—	—	—	—	REL	25	rr	3
BLS *rel*	Branch if Lower or Same	PC ← (PC) + 2 + *rel* ? C ∨ Z = 1	—	—	—	—	—	REL	23	rr	3
BMC *rel*	Branch if Interrupt Mask Clear	PC ← (PC) + 2 + *rel* ? I = 0	—	—	—	—	—	REL	2C	rr	3
BMI *rel*	Branch if Minus	PC ← (PC) + 2 + *rel* ? N = 1	—	—	—	—	—	REL	2B	rr	3
BMS *rel*	Branch if Interrupt Mask Set	PC ← (PC) + 2 + *rel* ? I = 1	—	—	—	—	—	REL	2D	rr	3
BNE *rel*	Branch if Not Equal	PC ← (PC) + 2 + *rel* ? Z = 0	—	—	—	—	—	REL	26	rr	3
BPL *rel*	Branch if Plus	PC ← (PC) + 2 + *rel* ? N = 0	—	—	—	—	—	REL	2A	rr	3
BRA *rel*	Branch Always	PC ← (PC) + 2 + *rel* ? 1 = 1	—	—	—	—	—	REL	20	rr	3
BRCLR *n opr rel*	Branch if Bit n Clear	PC ← (PC) + 2 + *rel* ? Mn = 0	—	—	—	—	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	01 03 05 07 09 0B 0D 0F	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BRN *rel*	Branch Never	PC ← (PC) + 2 + *rel* ? 1 = 0	—	—	—	—	—	REL	21	rr	3
BRSET *n opr rel*	Branch if Bit n Set	PC ← (PC) + 2 + *rel* ? Mn = 1	—	—	—	—	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	00 02 04 06 08 0A 0C 0E	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BSET *n opr*	Set Bit n	Mn ← 1	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	10 12 14 16 18 1A 1C 1E	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5

Table 3-6. Instruction Set Summary (Sheet 3 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
BSR *rel*	Branch to Subroutine	PC ← (PC) + 2; push (PCL) SP ← (SP) – 1; push (PCH) SP ← (SP) – 1 PC ← (PC) + *rel*	—	—	—	—	—	REL	AD	rr	6
CLC	Clear Carry Bit	C ← 0	—	—	—	—	0	INH	98		2
CLI	Clear Interrupt Mask	I ← 0	—	0	—	—	—	INH	9A		2
CLR *opr* CLRA CLRX CLR *opr*,X CLR ,X	Clear Byte	M ← $00 A ← $00 X ← $00 M ← $00 M ← $00	—	—	0	1	—	DIR INH INH IX1 IX	3F 4F 5F 6F 7F	dd ff 	5 3 3 6 5
CMP #*opr* CMP *opr* CMP *opr* CMP *opr*,X CMP *opr*,X CMP ,X	Compare Accumulator with Memory Byte	(A) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A1 B1 C1 D1 E1 F1	ii dd hh ll ee ff ff 	2 3 4 5 4 3
COM *opr* COMA COMX COM *opr*,X COM ,X	Complement Byte (One's Complement)	M ← ($\overline{M}$) = $FF – (M) A ← ($\overline{A}$) = $FF – (A) X ← ($\overline{X}$) = $FF – (X) M ← ($\overline{M}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M)	—	—	↕	↕	1	DIR INH INH IX1 IX	33 43 53 63 73	dd ff 	5 3 3 6 5
CPX #*opr* CPX *opr* CPX *opr* CPX *opr*,X CPX *opr*,X CPX ,X	Compare Index Register with Memory Byte	(X) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A3 B3 C3 D3 E3 F3	ii dd hh ll ee ff ff 	2 3 4 5 4 3
DEC *opr* DECA DECX DEC *opr*,X DEC ,X	Decrement Byte	M ← (M) – 1 A ← (A) – 1 X ← (X) – 1 M ← (M) – 1 M ← (M) – 1	—	—	↕	↕	—	DIR INH INH IX1 IX	3A 4A 5A 6A 7A	dd ff 	5 3 3 6 5
EOR #*opr* EOR *opr* EOR *opr* EOR *opr*,X EOR *opr*,X EOR ,X	EXCLUSIVE OR Accumulator with Memory Byte	A ← (A) ⊕ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A8 B8 C8 D8 E8 F8	ii dd hh ll ee ff ff 	2 3 4 5 4 3
INC *opr* INCA INCX INC *opr*,X INC ,X	Increment Byte	M ← (M) + 1 A ← (A) + 1 X ← (X) + 1 M ← (M) + 1 M ← (M) + 1	—	—	↕	↕	—	DIR INH INH IX1 IX	3C 4C 5C 6C 7C	dd ff 	5 3 3 6 5

Table 3-6. Instruction Set Summary (Sheet 4 of 6)

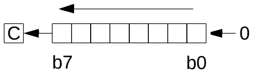
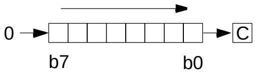
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
JMP *opr* JMP *opr* JMP *opr*,X JMP *opr*,X JMP ,X	Unconditional Jump	PC ← Jump Address	—	—	—	—	—	DIR EXT IX2 IX1 IX	BC CC DC EC FC	dd hh ll ee ff ff	2 3 4 3 2
JSR *opr* JSR *opr* JSR *opr*,X JSR *opr*,X JSR ,X	Jump to Subroutine	PC ← (PC) + n (n = 1, 2, or 3) Push (PCL); SP ← (SP) – 1 Push (PCH); SP ← (SP) – 1 PC ← Effective Address	—	—	—	—	—	DIR EXT IX2 IX1 IX	BD CD DD ED FD	dd hh ll ee ff ff	5 6 7 6 5
LDA #*opr* LDA *opr* LDA *opr* LDA *opr*,X LDA *opr*,X LDA ,X	Load Accumulator with Memory Byte	A ← (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A6 B6 C6 D6 E6 F6	ii dd hh ll ee ff ff	2 3 4 5 4 3
LDX #*opr* LDX *opr* LDX *opr* LDX *opr*,X LDX *opr*,X LDX ,X	Load Index Register with Memory Byte	X ← (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	AE BE CE DE EE FE	ii dd hh ll ee ff ff	2 3 4 5 4 3
LSL *opr* LSLA LSLX LSL *opr*,X LSL ,X	Logical Shift Left (Same as ASL)		—	—	↕	↕	↕	DIR INH INH IX1 IX	38 48 58 68 78	dd ff	5 3 3 6 5
LSR *opr* LSRA LSRX LSR *opr*,X LSR ,X	Logical Shift Right		—	—	0	↕	↕	DIR INH INH IX1 IX	34 44 54 64 74	dd ff	5 3 3 6 5
MUL	Unsigned Multiply	X : A ← (X) × (A)	0	—	—	—	0	INH	42		11
NEG *opr* NEGA NEGX NEG *opr*,X NEG ,X	Negate Byte (Two's Complement)	M ← –(M) = $00 – (M) A ← –(A) = $00 – (A) X ← –(X) = $00 – (X) M ← –(M) = $00 – (M) M ← –(M) = $00 – (M)	—	—	↕	↕	↕	DIR INH INH IX1 IX	30 40 50 60 70	dd ff	5 3 3 6 5
NOP	No Operation		—	—	—	—	—	INH	9D		2
ORA #*opr* ORA *opr* ORA *opr* ORA *opr*,X ORA *opr*,X ORA ,X	Logical OR Accumulator with Memory	A ← (A) ∨ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	AA BA CA DA EA FA	ii dd hh ll ee ff ff	2 3 4 5 4 3

Table 3-6. Instruction Set Summary (Sheet 5 of 6)

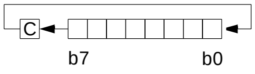
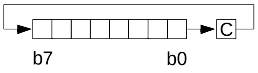
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
ROL *opr* ROLA ROLX ROL *opr*,X ROL ,X	Rotate Byte Left through Carry Bit		—	—	↕	↕	↕	DIR INH INH IX1 IX	39 49 59 69 79	dd ff 	5 3 3 6 5
ROR *opr* RORA RORX ROR *opr*,X ROR ,X	Rotate Byte Right through Carry Bit		—	—	↕	↕	↕	DIR INH INH IX1 IX	36 46 56 66 76	dd ff 	5 3 3 6 5
RSP	Reset Stack Pointer	SP ← $00FF	—	—	—	—	—	INH	9C		2
RTI	Return from Interrupt	SP ← (SP) + 1; Pull (CCR) SP ← (SP) + 1; Pull (A) SP ← (SP) + 1; Pull (X) SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	↕	↕	↕	↕	↕	INH	80		9
RTS	Return from Subroutine	SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	—	—	—	—	—	INH	81		6
SBC #*opr* SBC *opr* SBC *opr* SBC *opr*,X SBC *opr*,X SBC ,X	Subtract Memory Byte and Carry Bit from Accumulator	A ← (A) – (M) – (C)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A2 B2 C2 D2 E2 F2	ii dd hh ll ee ff ff 	2 3 4 5 4 3
SEC	Set Carry Bit	C ← 1	—	—	—	—	1	INH	99		2
SEI	Set Interrupt Mask	I ← 1	—	1	—	—	—	INH	9B		2
STA *opr* STA *opr* STA *opr*,X STA *opr*,X STA ,X	Store Accumulator in Memory	M ← (A)	—	—	↕	↕	—	DIR EXT IX2 IX1 IX	B7 C7 D7 E7 F7	dd hh ll ee ff ff 	4 5 6 5 4
STOP	Stop Oscillator and Enable IRQ Pin		—	0	—	—	—	INH	8E		2
STX *opr* STX *opr* STX *opr*,X STX *opr*,X STX ,X	Store Index Register In Memory	M ← (X)	—	—	↕	↕	—	DIR EXT IX2 IX1 IX	BF CF DF EF FF	dd hh ll ee ff ff 	4 5 6 5 4
SUB #*opr* SUB *opr* SUB *opr* SUB *opr*,X SUB *opr*,X SUB ,X	Subtract Memory Byte from Accumulator	A ← (A) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A0 B0 C0 D0 E0 F0	ii dd hh ll ee ff ff 	2 3 4 5 4 3

Table 3-6. Instruction Set Summary (Sheet 6 of 6)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
SWI	Software Interrupt	PC ← (PC) + 1; Push (PCL) SP ← (SP) – 1; Push (PCH) SP ← (SP) – 1; Push (X) SP ← (SP) – 1; Push (A) SP ← (SP) – 1; Push (CCR) SP ← (SP) – 1; I ← 1 PCH ← Interrupt Vector High Byte PCL ← Interrupt Vector Low Byte	—	1	—	—	—	INH	83		10
TAX	Transfer Accumulator to Index Register	X ← (A)	—	—	—	—	—	INH	97		2
TST *opr*	Test Memory Byte for Negative or Zero	(M) – $00	—	—	↕	↕	—	DIR	3D	dd	4
TSTA								INH	4D		3
TSTX								INH	5D		3
TST *opr*,X								IX1	6D	ff	5
TST ,X								IX	7D		4
TXA	Transfer Index Register to Accumulator	A ← (X)	—	—	—	—	—	INH	9F		2
WAIT	Stop CPU Clock and Enable Interrupts		—	↕	—	—	—	INH	8F		2

A	Accumulator
C	Carry/borrow flag
CCR	Condition code register
dd	Direct address of operand
dd rr	Direct address of operand and relative offset of branch instruction
DIR	Direct addressing mode
ee ff	High and low bytes of offset in indexed, 16-bit offset addressing
EXT	Extended addressing mode
ff	Offset byte in indexed, 8-bit offset addressing
H	Half-carry flag
hh ll	High and low bytes of operand address in extended addressing
I	Interrupt mask
ii	Immediate operand byte
IMM	Immediate addressing mode
INH	Inherent addressing mode
IX	Indexed, no offset addressing mode
IX1	Indexed, 8-bit offset addressing mode
IX2	Indexed, 16-bit offset addressing mode
M	Memory location
N	Negative flag
n	Any bit

opr	Operand (one or two bytes)
PC	Program counter
PCH	Program counter high byte
PCL	Program counter low byte
REL	Relative addressing mode
rel	Relative program counter offset byte
rr	Relative program counter offset byte
SP	Stack pointer
X	Index register
Z	Zero flag
#	Immediate value
∧	Logical AND
∨	Logical OR
⊕	Logical EXCLUSIVE OR
( )	Contents of
–( )	Negation (two's complement)
←	Loaded with
?	If
:	Concatenated with
↕	Set or cleared
—	Not affected

3.8 Opcode Map

See Table 3-7.

Table 3-7. Opcode Map

	Bit Manipulation		Branch	Read-Modify-Write					Control		Register/Memory						
	DIR	DIR	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	
MSB / LSB	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSB / LSB
0	5 BRSET0 3 DIR	5 BSET0 2 DIR	3 BRA 2 REL	5 NEG 2 DIR	3 NEGA 1 INH	3 NEGX 1 INH	6 NEG 2 IX1	5 NEG 1 IX	9 RTI 1 INH		2 SUB 2 IMM	3 SUB 2 DIR	4 SUB 3 EXT	5 SUB 3 IX2	4 SUB 2 IX1	3 SUB 1 IX	0
1	5 BRCLR0 3 DIR	5 BCLR0 2 DIR	3 BRN 2 REL						6 RTS 1 INH		2 CMP 2 IMM	3 CMP 2 DIR	4 CMP 3 EXT	5 CMP 3 IX2	4 CMP 2 IX1	3 CMP 1 IX	1
2	5 BRSET1 3 DIR	5 BSET1 2 DIR	3 BHI 2 REL		11 MUL 1 INH						2 SBC 2 IMM	3 SBC 2 DIR	4 SBC 3 EXT	5 SBC 3 IX2	4 SBC 2 IX1	3 SBC 1 IX	2
3	5 BRCLR1 3 DIR	5 BCLR1 2 DIR	3 BLS 2 REL	5 COM 2 DIR	3 COMA 1 INH	3 COMX 1 INH	6 COM 2 IX1	5 COM 1 IX	10 SWI 1 INH		2 CPX 2 IMM	3 CPX 2 DIR	4 CPX 3 EXT	5 CPX 3 IX2	4 CPX 2 IX1	3 CPX 1 IX	3
4	5 BRSET2 3 DIR	5 BSET2 2 DIR	3 BCC 2 REL	5 LSR 2 DIR	3 LSRA 1 INH	3 LSRX 1 INH	6 LSR 2 IX1	5 LSR 1 IX			2 AND 2 IMM	3 AND 2 DIR	4 AND 3 EXT	5 AND 3 IX2	4 AND 2 IX1	3 AND 1 IX	4
5	5 BRCLR2 3 DIR	5 BCLR2 2 DIR	3 BCS/BLO 2 REL								2 BIT 2 IMM	3 BIT 2 DIR	4 BIT 3 EXT	5 BIT 3 IX2	4 BIT 2 IX1	3 BIT 1 IX	5
6	5 BRSET3 3 DIR	5 BSET3 2 DIR	3 BNE 2 REL	5 ROR 2 DIR	3 RORA 1 INH	3 RORX 1 INH	6 ROR 2 IX1	5 ROR 1 IX			2 LDA 2 IMM	3 LDA 2 DIR	4 LDA 3 EXT	5 LDA 3 IX2	4 LDA 2 IX1	3 LDA 1 IX	6
7	5 BRCLR3 3 DIR	5 BCLR3 2 DIR	3 BEQ 2 REL	5 ASR 2 DIR	3 ASRA 1 INH	3 ASRX 1 INH	6 ASR 2 IX1	5 ASR 1 IX		2 TAX 1 INH		4 STA 2 DIR	5 STA 3 EXT	6 STA 3 IX2	5 STA 2 IX1	4 STA 1 IX	7
8	5 BRSET4 3 DIR	5 BSET4 2 DIR	3 BHCC 2 REL	5 ASL/LSL 2 DIR	3 ASLA/LSLA 1 INH	3 ASLX/LSLX 1 INH	6 ASL/LSL 2 IX1	5 ASL/LSL 1 IX		2 CLC 1 INH	2 EOR 2 IMM	3 EOR 2 DIR	4 EOR 3 EXT	5 EOR 3 IX2	4 EOR 2 IX1	3 EOR 1 IX	8
9	5 BRCLR4 3 DIR	5 BCLR4 2 DIR	3 BHCS 2 REL	5 ROL 2 DIR	3 ROLA 1 INH	3 ROLX 1 INH	6 ROL 2 IX1	5 ROL 1 IX		2 SEC 1 INH	2 ADC 2 IMM	3 ADC 2 DIR	4 ADC 3 EXT	5 ADC 3 IX2	4 ADC 2 IX1	3 ADC 1 IX	9
A	5 BRSET5 3 DIR	5 BSET5 2 DIR	3 BPL 2 REL	5 DEC 2 DIR	3 DECA 1 INH	3 DECX 1 INH	6 DEC 2 IX1	5 DEC 1 IX		2 CLI 1 INH	2 ORA 2 IMM	3 ORA 2 DIR	4 ORA 3 EXT	5 ORA 3 IX2	4 ORA 2 IX1	3 ORA 1 IX	A
B	5 BRCLR5 3 DIR	5 BCLR5 2 DIR	3 BMI 2 REL							2 SEI 1 INH	2 ADD 2 IMM	3 ADD 2 DIR	4 ADD 3 EXT	5 ADD 3 IX2	4 ADD 2 IX1	3 ADD 1 IX	B
C	5 BRSET6 3 DIR	5 BSET6 2 DIR	3 BMC 2 REL	5 INC 2 DIR	3 INCA 1 INH	3 INCX 1 INH	6 INC 2 IX1	5 INC 1 IX		2 RSP 1 INH		2 JMP 2 DIR	3 JMP 3 EXT	4 JMP 3 IX2	3 JMP 2 IX1	2 JMP 1 IX	C
D	5 BRCLR6 3 DIR	5 BCLR6 2 DIR	3 BMS 2 REL	4 TST 2 DIR	3 TSTA 1 INH	3 TSTX 1 INH	5 TST 2 IX1	4 TST 1 IX		2 NOP 1 INH	6 BSR 2 REL	5 JSR 2 DIR	6 JSR 3 EXT	7 JSR 3 IX2	6 JSR 2 IX1	5 JSR 1 IX	D
E	5 BRSET7 3 DIR	5 BSET7 2 DIR	3 BIL 2 REL						2 STOP 1 INH		2 LDX 2 IMM	3 LDX 2 DIR	4 LDX 3 EXT	5 LDX 3 IX2	4 LDX 2 IX1	3 LDX 1 IX	E
F	5 BRCLR7 3 DIR	5 BCLR7 2 DIR	3 BIH 2 REL	5 CLR 2 DIR	3 CLRA 1 INH	3 CLRX 1 INH	6 CLR 2 IX1	5 CLR 1 IX	2 WAIT 1 INH	2 TXA 1 INH		4 STX 2 DIR	5 STX 3 EXT	6 STX 3 IX2	5 STX 2 IX1	4 STX 1 IX	F

INH = Inherent
IMM = Immediate
DIR = Direct
EXT = Extended

REL = Relative
IX = Indexed, No Offset
IX1 = Indexed, 8-Bit Offset
IX2 = Indexed, 16-Bit Offset

	MSB of Opcode in Hexadecimal	
MSB / LSB	0	
LSB of Opcode in Hexadecimal 0	5 BRSET0 3 DIR	Number of Cycles Opcode Mnemonic Number of Bytes/Addressing Mode

Section 4. Resets and Interrupts

4.1 Contents

4.2 Introduction 69

4.3 Resets. 70
4.3.1 Power-On Reset. 71
4.3.2 External Reset 72
4.3.3 COP Watchdog Reset 72
4.3.4 Illegal Address Reset 72

4.4 Interrupts. 73
4.4.1 Software Interrupt. 73
4.4.2 External Interrupt 73
4.4.3 Timer Interrupts 76
4.4.3.1 Real-Time Interrupt 76
4.4.3.2 Timer Overflow Interrupt 76
4.4.4 Interrupt Processing 76

4.2 Introduction

Reset initializes the microcontroller unit (MCU) by returning the program counter to a known address and by forcing control and status bits to known states.

Interrupts temporarily change the sequence of program execution to respond to events that occur during processing.

4.3 Resets

A reset immediately stops the operation of the instruction being executed, initializes certain control and status bits, and loads the program counter with a user-defined reset vector address. These sources can generate a reset:

- Power-on reset (POR) circuit
- $\overline{\text{RESET}}$ pin
- Computer operating properly (COP) watchdog
- Illegal address

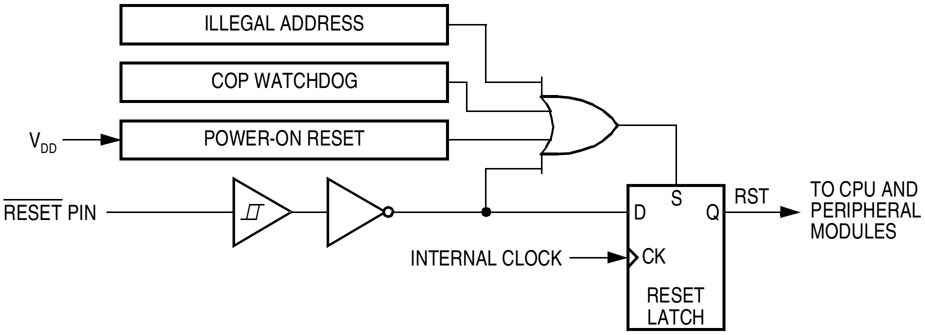

ILLEGAL ADDRESS
COP WATCHDOG
V_{DD}
POWER-ON RESET
$\overline{\text{RESET}}$ PIN
INTERNAL CLOCK
D
S
Q
CK
RESET LATCH
RST
TO CPU AND PERIPHERAL MODULES

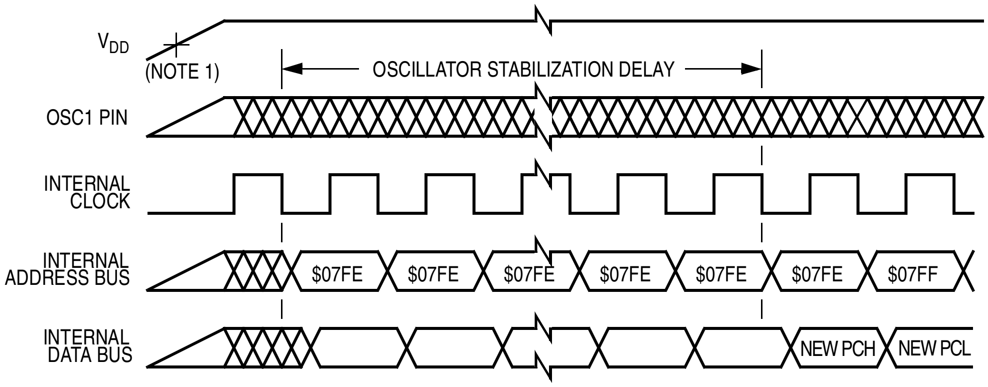
Figure 4-1. Reset Sources

4.3.1 Power-On Reset

A positive transition on the V_{DD} pin generates a power-on reset.

NOTE: *The power-on reset is strictly for power-up conditions and cannot be used to detect drops in power supply voltage.*

A 4064-t_{cyc} (internal clock cycle) delay after the oscillator becomes active allows the clock generator to stabilize. If any reset source is active at the end of this delay, the MCU remains in the reset condition until all reset sources are inactive.

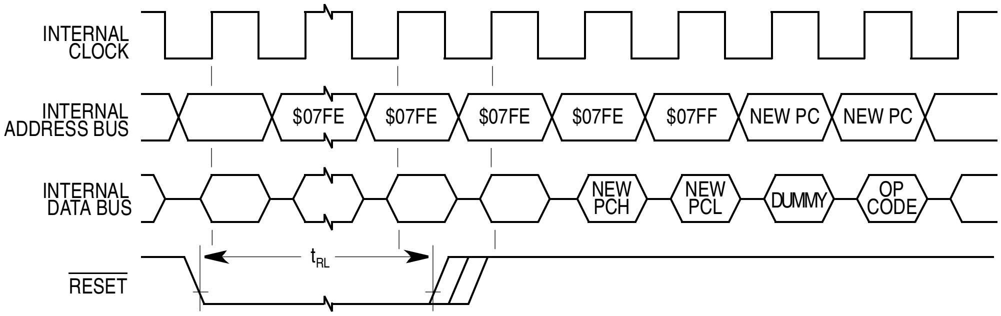

V_{DD}
(NOTE 1)
OSCILLATOR STABILIZATION DELAY
OSC1 PIN
INTERNAL CLOCK
INTERNAL ADDRESS BUS
$07FE
$07FE
$07FE
$07FE
$07FE
$07FE
$07FF
INTERNAL DATA BUS
NEW PCH
NEW PCL

Notes:
1. Power-on reset threshold is typically between 1 V and 2 V.
2. Internal clock, internal address bus, and internal data bus are not available externally.

Figure 4-2. Power-On Reset Timing

4.3.2 External Reset

A logic 0 applied to the $\overline{\text{RESET}}$ pin for 1 1/2 t_{cyc} generates an external reset. A Schmitt trigger senses the logic level at the $\overline{\text{RESET}}$ pin.


INTERNAL CLOCK
INTERNAL ADDRESS BUS
$07FE
$07FE
$07FE
$07FE
$07FF
NEW PC
NEW PC
INTERNAL DATA BUS
NEW PCH
NEW PCL
DUMMY
OP CODE
t_{RL}
$\overline{\text{RESET}}$

Notes:

1. Internal clock, internal address bus, and internal data bus are not available externally.
2. The next rising edge of the internal clock after the rising edge of $\overline{\text{RESET}}$ initiates the reset sequence.

Figure 4-3. External Reset Timing

Table 4-1. External Reset Timing

Characteristic	Symbol	Min	Max	Unit
$\overline{\text{RESET}}$ pulse width	t_{RL}	1.5	—	t_{cyc}

4.3.3 COP Watchdog Reset

A timeout of the COP watchdog generates a COP reset. The COP watchdog is part of a software error detection system and must be cleared periodically to start a new timeout period. To clear the COP watchdog and prevent a COP reset, write a logic 0 to bit 0 (COPC) of the COP register at location $07F0.

4.3.4 Illegal Address Reset

An opcode fetch from an address not in random-access memory (RAM) or erasable, programmable read-only memory (EPROM) generates a reset.

4.4 Interrupts

These sources can generate interrupts:

- Software interrupt (SWI) instruction
- External interrupt pins:
  - $\overline{\text{IRQ}}/V_{PP}$
  - PA0–PA3
- Timer:
  - Real-time interrupt flag (RTIF)
  - Timer overflow flag (TOF)

An interrupt temporarily stops the program sequence to process a particular event. An interrupt does not stop the operation of the instruction being executed, but takes effect when the current instruction completes its execution. Interrupt processing automatically saves the CPU registers on the stack and loads the program counter with a user-defined interrupt vector address.

4.4.1 Software Interrupt

The software interrupt (SWI) instruction causes a non-maskable interrupt.

4.4.2 External Interrupt

An interrupt signal on the $\overline{\text{IRQ}}/V_{PP}$ pin latches an external interrupt request. When the CPU completes its current instruction, it tests the IRQ latch. If the IRQ latch is set, the CPU then tests the I bit in the condition code register. If the I bit is clear, the CPU then begins the interrupt sequence.

The CPU clears the IRQ latch during interrupt processing, so that another interrupt signal on the $\overline{\text{IRQ}}/V_{PP}$ pin can latch another interrupt request during the interrupt service routine. As soon as the I bit is cleared during the return from interrupt, the CPU can recognize the new interrupt request. Figure 4-4 shows the $\overline{\text{IRQ}}/V_{PP}$ pin interrupt logic.

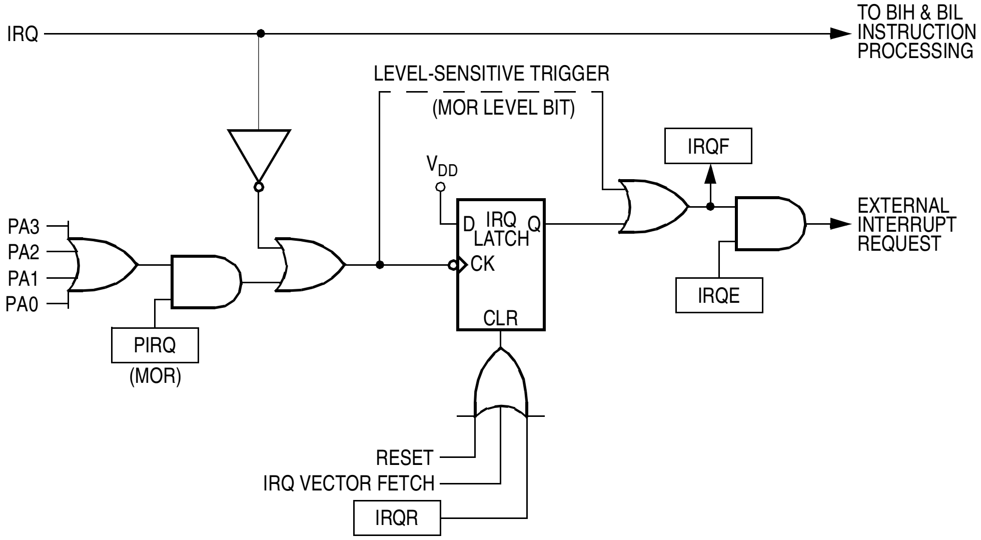

IRQ
TO BIH & BIL INSTRUCTION PROCESSING
LEVEL-SENSITIVE TRIGGER
(MOR LEVEL BIT)
V_{DD}
IRQF
D
IRQ LATCH
Q
CK
CLR
EXTERNAL INTERRUPT REQUEST
PA3
PA2
PA1
PA0
PIRQ
(MOR)
IRQE
RESET
IRQ VECTOR FETCH
IRQR

Figure 4-4. External Interrupt Logic

Setting the I bit in the condition code register disables external interrupts.

The port A external interrupt bit (PIRQ) in the mask option register enables pins PA0–PA3 to function as external interrupt pins.

The external interrupt sensitivity bit (LEVEL) in the mask option register controls interrupt triggering sensitivity of external interrupt pins. The $\overline{\text{IRQ}}/V_{PP}$ pin can be negative-edge triggered only or negative-edge and low-level triggered. Port A external interrupt pins can be positive-edge triggered only or both positive-edge and high-level triggered. The level-sensitive triggering option allows multiple external interrupt sources to be wire-ORed to an external interrupt pin. An external interrupt request, shown in Figure 4-5, is latched as long as any source is holding an external interrupt pin low.

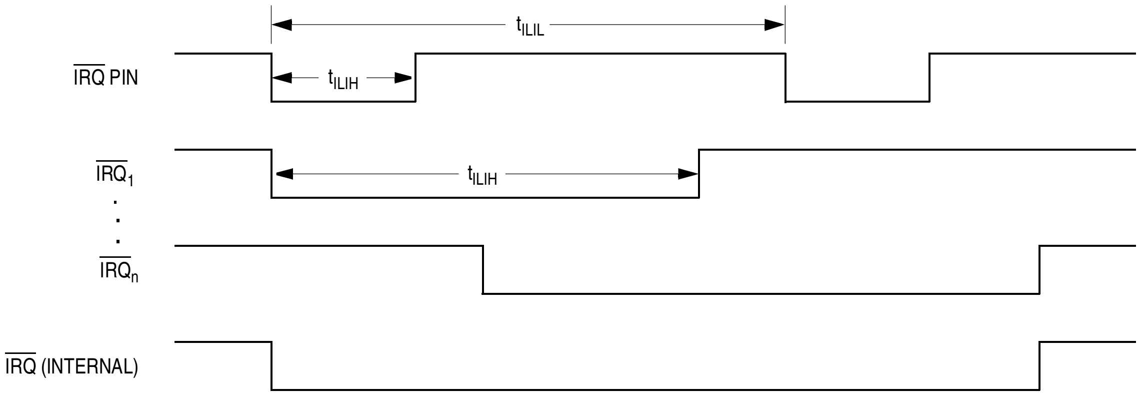


Figure 4-5. External Interrupt Timing

Table 4-2. External Interrupt Timing (V_{DD} = 5.0 Vdc)(1)

Characteristic	Symbol	Min	Max	Unit
Interrupt pulse width low (edge-triggered)	t_{ILIH}	125	—	ns
Interrupt pulse period	t_{ILIL}	Note(2)	—	t_{cyc}

1. V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, T_A = –40°C to +105°C, unless otherwise noted
2. The minimum, t_{ILIL}, should not be less than the number of interrupt service routine cycles plus 19 t_{cyc}.

Table 4-3. External Interrupt Timing (V_{DD} = 3.3 Vdc)(1)

Characteristic	Symbol	Min	Max	Unit
Interrupt pulse width low (edge-triggered)	t_{ILIH}	250	—	ns
Interrupt pulse period	t_{ILIL}	Note(2)	—	t_{cyc}

1. V_{DD} = 3.3 Vdc ±10%, V_{SS} = 0 Vdc, T_A = –40°C to +105°C, unless otherwise noted
2. The minimum, t_{ILIL}, should not be less than the number of interrupt service routine cycles plus 19 t_{cyc}.

4.4.3 Timer Interrupts

The timer can generate these interrupt requests:

- Real time
- Timer overflow

Setting the I bit in the condition code register disables timer interrupts.

4.4.3.1 Real-Time Interrupt

A real-time interrupt occurs if the real-time interrupt flag, RTIF, becomes set while the real-time interrupt enable bit, RTIE, is also set. RTIF and RTIE are in the timer status and control register.

4.4.3.2 Timer Overflow Interrupt

A timer overflow interrupt request occurs if the timer overflow flag, TOF, becomes set while the timer overflow interrupt enable bit, TOIE, is also set. TOF and TOIE are in the timer status and control register.

4.4.4 Interrupt Processing

The CPU takes these actions to begin servicing an interrupt:

- Stores the CPU registers on the stack in the order shown in **Figure 4-6**
- Sets the I bit in the condition code register to prevent further interrupts
- Loads the program counter with the contents of the appropriate interrupt vector locations:
  - $07FC and $07FD (software interrupt vector)
  - $07FA and $07FB (external interrupt vector)
  - $07F8 and $07F9 (timer interrupt vector)

The return-from-interrupt (RTI) instruction causes the CPU to recover the CPU registers from the stack as shown in **Figure 4-6**.

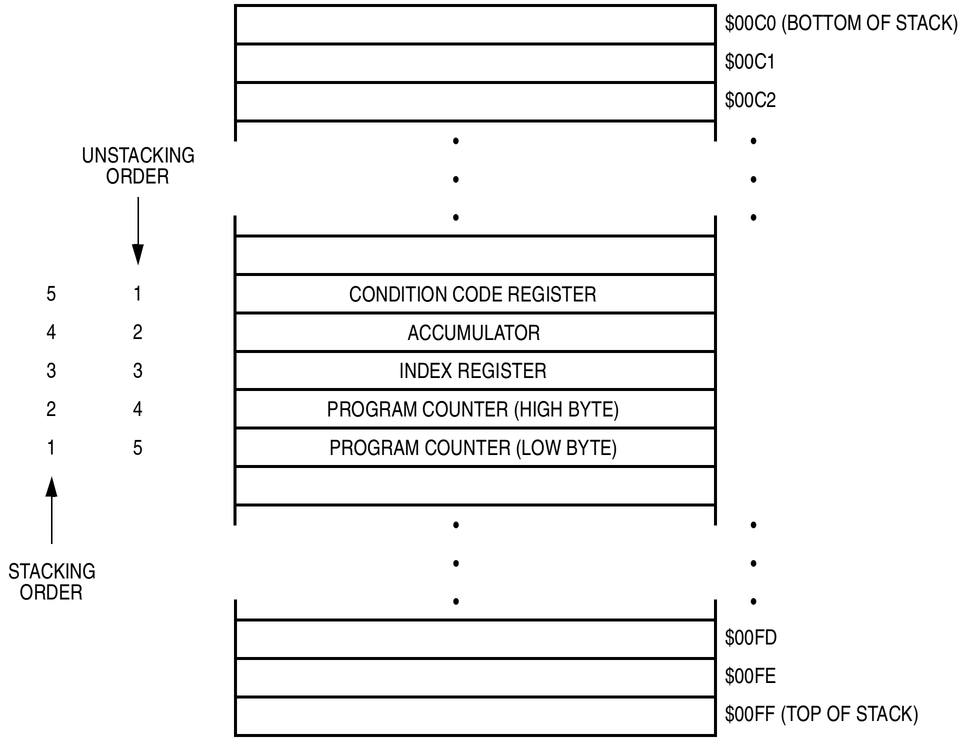

$00C0 (BOTTOM OF STACK)
$00C1
$00C2
UNSTACKING ORDER
5 1 CONDITION CODE REGISTER
4 2 ACCUMULATOR
3 3 INDEX REGISTER
2 4 PROGRAM COUNTER (HIGH BYTE)
1 5 PROGRAM COUNTER (LOW BYTE)
STACKING ORDER
$00FD
$00FE
$00FF (TOP OF STACK)

Figure 4-6. Interrupt Stacking Order

Table 4-4. Reset/Interrupt Vector Addresses

Function	Source	Local Mask	Global Mask	Priority (1 = Highest)	Vector Address
Reset	Power-on $\overline{\text{RESET}}$ pin COP watchdog[1] illegal address	None	None	1	\$07FE–\$07FF
Software interrupt (SWI)	User code	None	None	Same priority as instruction	\$07FC–\$07FD
External interrupt	$\overline{\text{IRQ}}/V_{PP}$ pin	IRQE	I bit	2	\$07FA–\$07FB
Timer interrupts	RTIF bit TOF bit	RTIE bit TOIE bit	I bit	3	\$07F8–\$07F9

1. The COP watchdog is programmable in the mask option register.

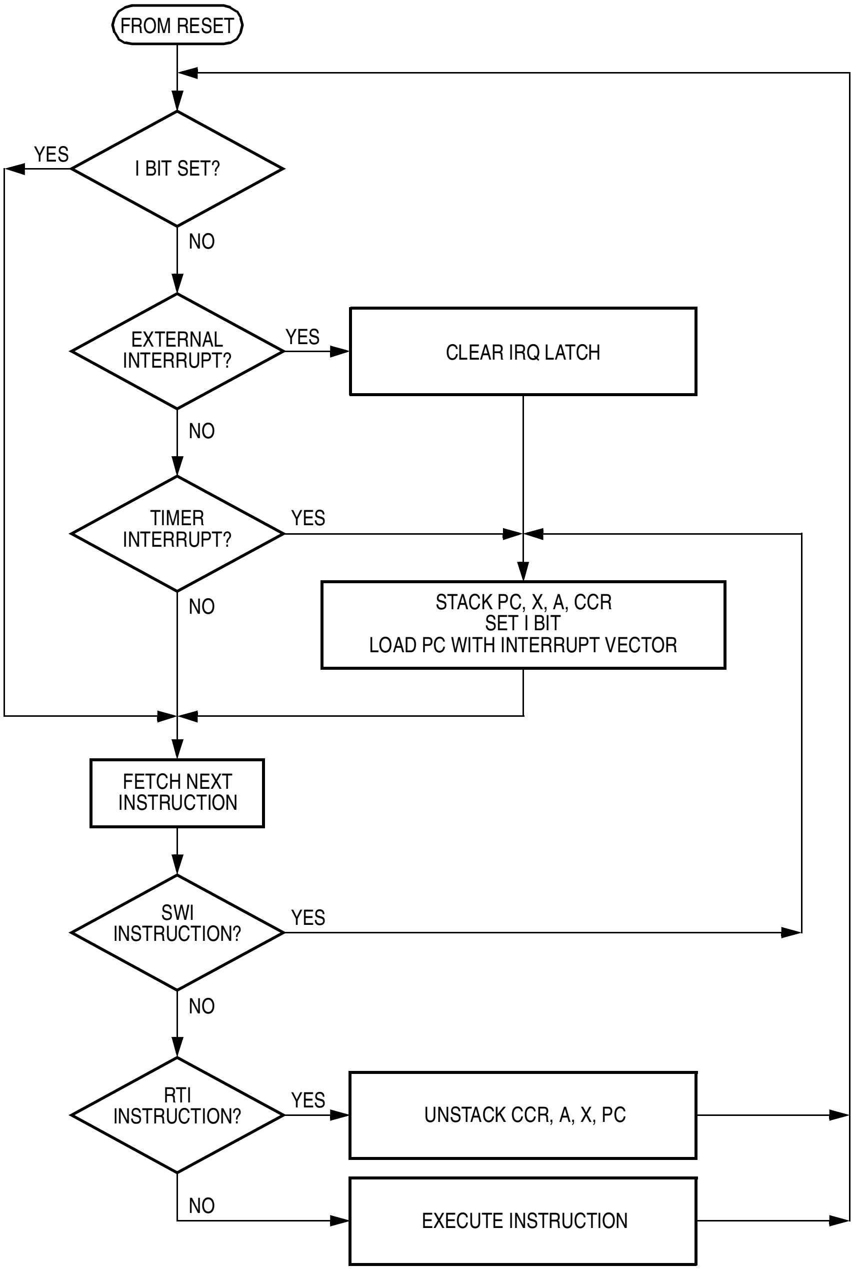

FROM RESET
I BIT SET?
YES
NO
EXTERNAL INTERRUPT?
YES
CLEAR IRQ LATCH
NO
TIMER INTERRUPT?
YES
STACK PC, X, A, CCR
SET I BIT
LOAD PC WITH INTERRUPT VECTOR
NO
FETCH NEXT INSTRUCTION
SWI INSTRUCTION?
YES
NO
RTI INSTRUCTION?
YES
UNSTACK CCR, A, X, PC
NO
EXECUTE INSTRUCTION

Figure 4-7. Interrupt Flowchart

Section 5. Low-Power Modes

5.1 Contents

5.2 Introduction 79

5.3 Exiting Stop and Wait Modes 80

5.4 Effects of Stop and Wait Modes 81
5.4.1 Clock Generation 81
5.4.2 CPU 82
5.4.3 COP Watchdog 82
5.4.4 Timer 83
5.4.5 EPROM/OTPROM 84
5.4.6 Data-Retention Mode 84

5.5 Timing 85

5.2 Introduction

The microcontroller unit (MCU) can enter these low-power standby modes:

- Stop mode — The STOP instruction puts the MCU in its lowest power-consumption mode.
- Wait mode — The WAIT instruction puts the MCU in an intermediate power-consumption mode.
- Halt mode — Halt mode is identical to wait mode, except that an oscillator stabilization delay of 1 to 4064 internal clock cycles occurs when the MCU exits halt mode. The stop-to-wait conversion bit, SWAIT, in the mask option register, enables halt mode.

Enabling halt mode prevents the computer operating properly (COP) watchdog from being inadvertently turned off by a STOP instruction.

- Data-retention mode — In data-retention mode, the MCU retains RAM contents and CPU register contents at V_{DD} voltages as low as 2.0 Vdc. The data-retention feature allows the MCU to remain in a low power-consumption state during which it retains data, but the CPU cannot execute instructions.

5.3 Exiting Stop and Wait Modes

The events described in this subsection bring the MCU out of stop mode and load the program counter with the reset vector or with an interrupt vector.

Exiting stop mode:

- External reset — A logic 0 on the $\overline{\text{RESET}}$ pin resets the MCU, starts the CPU clock, and loads the program counter with the contents of locations $07FE and $07FF.
- External interrupt — A high-to-low transition on the $\overline{\text{IRQ}}/V_{PP}$ pin or a low-to-high transition on an enabled port A external interrupt pin starts the CPU clock and loads the program counter with the contents of locations $07FA and $07FB.

Exiting wait mode:

- External reset — A logic 0 on the $\overline{\text{RESET}}$ pin resets the MCU, starts the CPU clock, and loads the program counter with the contents of locations $07FE and $07FF.
- External interrupt — A high-to-low transition on the $\overline{\text{IRQ}}/V_{PP}$ pin or a low-to-high transition on an enabled port A external interrupt pin starts the CPU clock and loads the program counter with the contents of locations $07FA and $07FB.

- COP watchdog reset — A timeout of the COP watchdog resets the MCU, starts the CPU clock, and loads the program counter with the contents of locations \$07FE and \$07FF. Software can enable timer interrupts so that the MCU periodically can exit wait mode to reset the COP watchdog.
- Timer interrupt — Real-time interrupt requests and timer overflow interrupt requests start the MCU clock and load the program counter with the contents of locations \$07F8 and \$07F9.

5.4 Effects of Stop and Wait Modes

The STOP and WAIT instructions have the effects described in this subsection on MCU modules.

5.4.1 Clock Generation

The STOP instruction:

The STOP instruction disables the internal oscillator, stopping the CPU clock and all peripheral clocks.

After exiting stop mode, the CPU clock and all enabled peripheral clocks begin running after the oscillator stabilization delay.

NOTE: *The oscillator stabilization delay holds the MCU in reset for the first 4064 internal clock cycles.*

The WAIT instruction:

The WAIT instruction disables the CPU clock.

After exiting wait mode, the CPU clock and all enabled peripheral clocks immediately begin running.

5.4.2 CPU

The STOP instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling external interrupts
- Disables the CPU clock

After exiting stop mode, the CPU clock begins running after the oscillator stabilization delay.

After exit from stop mode by external interrupt, the I bit remains clear.

After exit from stop mode by reset, the I bit is set.

The WAIT instruction:

- Clears the interrupt mask (I bit) in the condition code register, enabling interrupts
- Disables the CPU clock

After exit from wait mode by interrupt, the I bit remains clear.

After exit from wait mode by reset, the I bit is set.

5.4.3 COP Watchdog

The STOP instruction:

- Clears the COP watchdog counter
- Disables the COP watchdog clock

NOTE: *To prevent the STOP instruction from disabling the COP watchdog, program the stop-to-wait conversion bit (SWAIT) in the mask option register to logic 1.*

After exit from stop mode by external interrupt, the COP watchdog counter immediately begins counting from $0000 and continues counting throughout the oscillator stabilization delay.

NOTE: *Immediately after exiting stop mode by external interrupt, service the COP to ensure a full COP timeout period.*

After exit from stop mode by reset:

- The COP watchdog counter immediately begins counting from $0000.
- The COP watchdog counter is cleared at the end of the oscillator stabilization delay and begins counting from $0000 again.

The WAIT instruction:

The WAIT instruction has no effect on the COP watchdog.

NOTE: *To prevent a COP timeout during wait mode, exit wait mode periodically to service the COP.*

5.4.4 Timer

The STOP instruction:

- Clears the RTIE, TOFE, RTIF, and TOF bits in the timer status and control register, disabling timer interrupt requests and removing any pending timer interrupt requests
- Disables the clock to the timer

After exiting stop mode by external interrupt, the timer immediately resumes counting from the last value before the STOP instruction and continues counting throughout the oscillator stabilization delay.

After exiting stop mode by reset and after the oscillator stabilization delay, the timer resumes operation from its reset state.

The WAIT instruction:

The WAIT instruction has no effect on the timer.

5.4.5 EPROM/OTPROM

The STOP instruction:

> The STOP instruction during erasable, programmable read-only memory (EPROM) programming clears the EPGM bit in the EPROM programming register, removing the programming voltage from the EPROM.

The WAIT instruction:

> The WAIT instruction has no effect on EPROM/one-time programmable read-only memory (OTPROM) operation.

5.4.6 Data-Retention Mode

In data-retention mode, the MCU retains random-access memory (RAM) contents and CPU register contents at V_{DD} voltages as low as 2.0 Vdc. The data-retention feature allows the MCU to remain in a low power-consumption state during which it retains data, but the CPU cannot execute instructions.

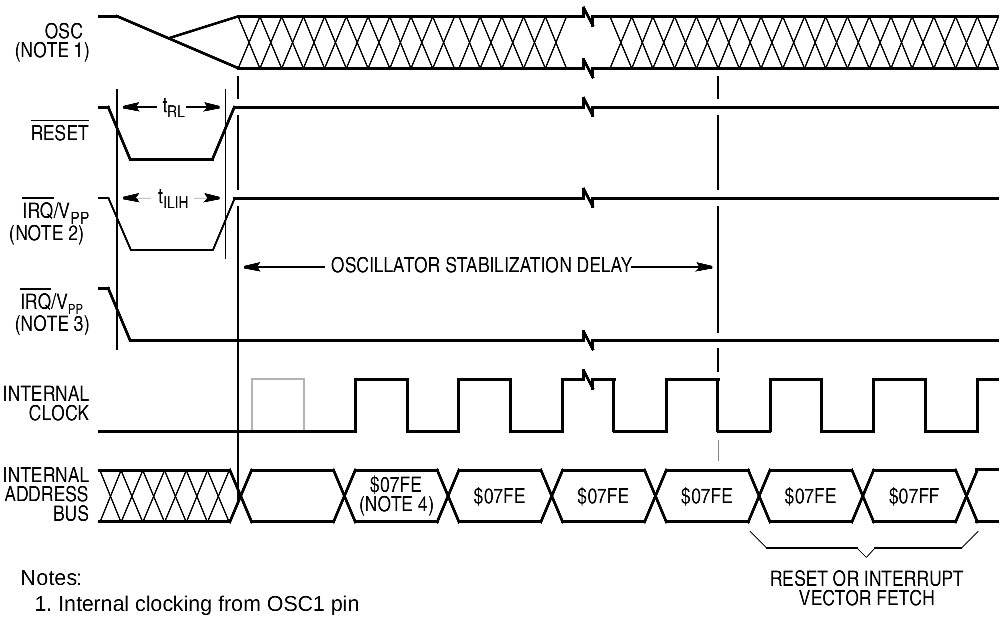
To put the MCU in data-retention mode:

1. Drive the $\overline{\text{RESET}}$ pin to logic 0.
2. Lower the V_{DD} voltage. The $\overline{\text{RESET}}$ pin must remain low continuously during data-retention mode.

To take the MCU out of data-retention mode:

1. Return V_{DD} to normal operating voltage.
2. Return the $\overline{\text{RESET}}$ pin to logic 1.

5.5 Timing


OSC
(NOTE 1)
RESET
t_{RL}
IRQ/V_{PP}
(NOTE 2)
t_{ILIH}
OSCILLATOR STABILIZATION DELAY
IRQ/V_{PP}
(NOTE 3)
INTERNAL
CLOCK
INTERNAL
ADDRESS
BUS
$07FE
(NOTE 4)
$07FE
$07FE
$07FE
$07FE
$07FF
RESET OR INTERRUPT
VECTOR FETCH

Notes:
1. Internal clocking from OSC1 pin
2. Edge-triggered external interrupt mask option
3. Edge- and level-triggered external interrupt mask option
4. Reset vector shown as example

Figure 5-1. Stop Mode Recovery Timing

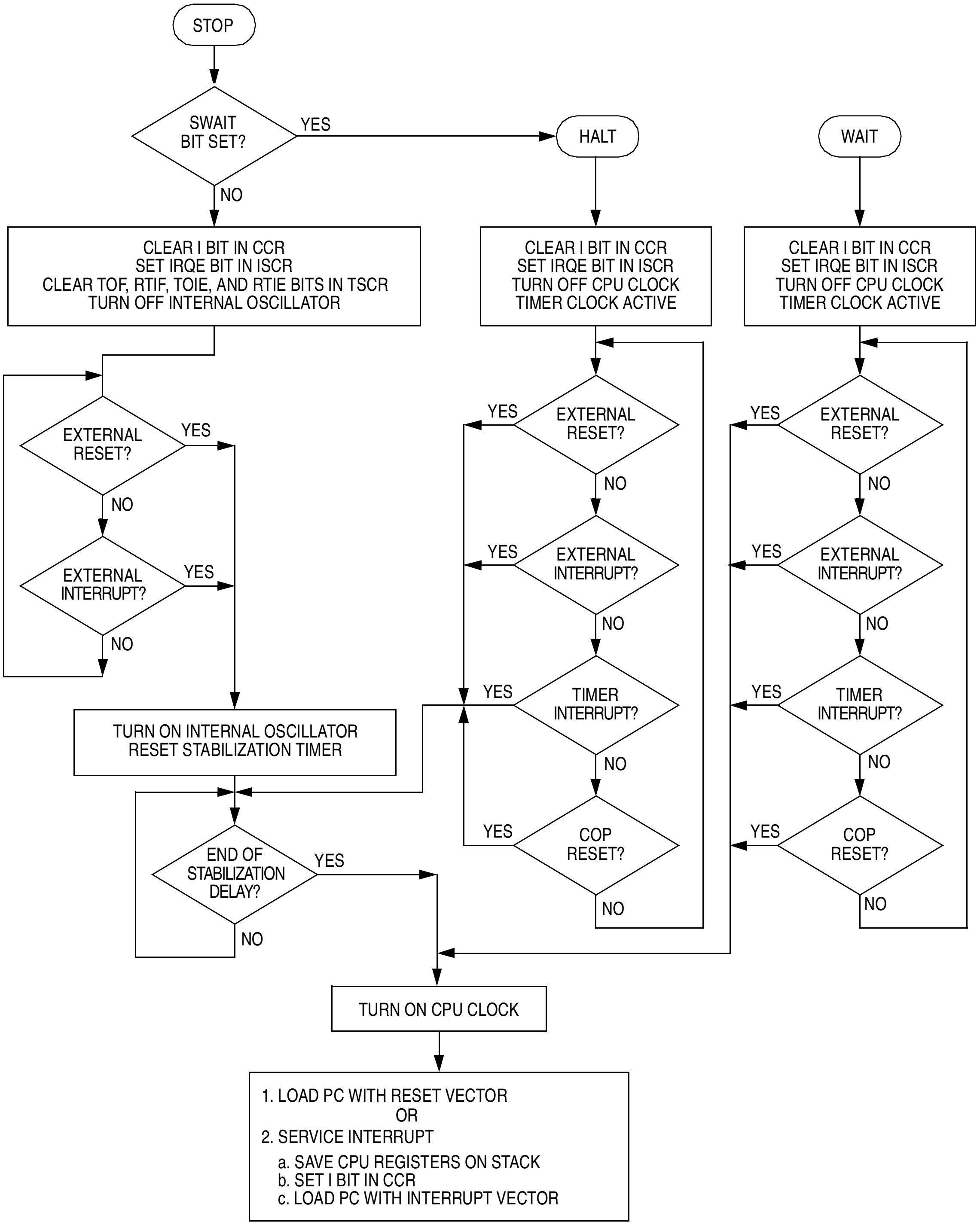

STOP
SWAIT BIT SET?
YES
NO
HALT
WAIT
CLEAR I BIT IN CCR
SET IRQE BIT IN ISCR
CLEAR TOF, RTIF, TOIE, AND RTIE BITS IN TSCR
TURN OFF INTERNAL OSCILLATOR
CLEAR I BIT IN CCR
SET IRQE BIT IN ISCR
TURN OFF CPU CLOCK
TIMER CLOCK ACTIVE
EXTERNAL RESET?
EXTERNAL INTERRUPT?
TIMER INTERRUPT?
COP RESET?
TURN ON INTERNAL OSCILLATOR
RESET STABILIZATION TIMER
END OF STABILIZATION DELAY?
TURN ON CPU CLOCK
1. LOAD PC WITH RESET VECTOR
OR
2. SERVICE INTERRUPT
a. SAVE CPU REGISTERS ON STACK
b. SET I BIT IN CCR
c. LOAD PC WITH INTERRUPT VECTOR

Figure 5-2. Stop/Halt/Wait Flowchart

Section 6. Parallel Input/Output (I/O) Ports

6.1 Contents

6.2 Introduction 87

6.3 Port A 89
6.3.1 Port A Data Register 89
6.3.2 Data Direction Register A. 90
6.3.3 Pulldown Register A 91
6.3.4 Port A LED Drive Capability 92
6.3.5 Port A I/O Pin Interrupts 92

6.4 Port B 92
6.4.1 Port B Data Register 92
6.4.2 Data Direction Register B. 93
6.4.3 Pulldown Register B 94

6.5 5.0-Volt I/O Port Electrical Characteristics 95

6.6 3.3-Volt I/O Port Electrical Characteristics 95

6.2 Introduction

Fourteen bidirectional pins form one 8-bit input/output (I/O) port and one 6-bit I/O port. All the bidirectional port pins are programmable as inputs or outputs.

NOTE: *Connect any unused I/O pins to an appropriate logic level, either* V_{DD} *or* $V_{SS.}$ *Although the I/O ports do not require termination for proper operation, termination reduces excess current consumption and the possibility of electrostatic damage.*

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PORTA) See page 89.	Read:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		Write:								
		Reset:	Unaffected by reset							
$0001	Port B Data Register (PORTB) See page 92.	Read:	0	0	PB5	PB4	PB3	PB2	PB1	PB0
		Write:	▨	▨						
		Reset:	Unaffected by reset							
$0004	Data Direction Register A (DDRA) See page 90.	Read:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0005	Data Direction Register B (DDRB) See page 93.	Read:	0	0	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
		Write:	▨	▨						
		Reset:	0	0	0	0	0	0	0	0
$0010	Pulldown Register A (PDRA) See page 91.	Read:	▨	▨	▨	▨	▨	▨	▨	▨
		Write:	PDIA7	PDIA6	PDIA5	PDIA4	PDIA3	PDIA2	PDIA1	PDIA0
		Reset:	0	0	0	0	0	0	0	0
$0011	Pulldown Register B (PDRB) See page 94.	Read:	▨	▨	▨	▨	▨	▨	▨	▨
		Write:			PDIB5	PDIB4	PDIB3	PDIB2	PDIB1	PDIB0
		Reset:			0	0	0	0	0	0

▨ = Unimplemented

Figure 6-1. Parallel I/O Port Register Summary

6.3 Port A

Port A is an 8-bit bidirectional port.

6.3.1 Port A Data Register

The port A data register (PORTA) contains a latch for each port A pin.

Address: $0000

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Reset:	Unaffected by reset							

Figure 6-2. Port A Data Register (PORTA)

PA[7:0] — Port A Data Bits

These read/write bits are software programmable. Data direction of each port A pin is under the control of the corresponding bit in data direction register A. Reset has no effect on port A data.

6.3.2 Data Direction Register A

Data direction register A (DDRA) determines whether each port A pin is an input or an output.

Address: $0004

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
Reset:	0	0	0	0	0	0	0	0

Figure 6-3. Data Direction Register A (DDRA)

DDRA[7:0] — Data Direction Register A Bits

These read/write bits control port A data direction. Reset clears DDRA[7:0], configuring all port A pins as inputs.

1 = Corresponding port A pin configured as output
0 = Corresponding port A pin configured as input

NOTE: *Avoid glitches on port A pins by writing to the port A data register before changing data direction register A bits from 0 to 1.*

Figure 6-4 shows the I/O logic of port A.

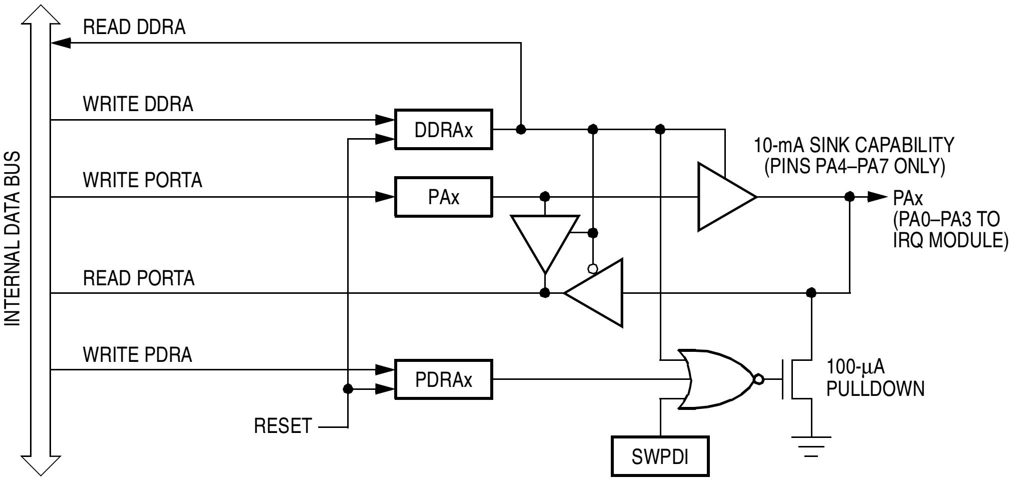

READ DDRA
WRITE DDRA
DDRAx
WRITE PORTA
PAx
READ PORTA
WRITE PDRA
PDRAx
RESET
INTERNAL DATA BUS
10-mA SINK CAPABILITY
(PINS PA4–PA7 ONLY)
PAx
(PA0–PA3 TO
IRQ MODULE)
100-µA
PULLDOWN
SWPDI

Figure 6-4. Port A I/O Circuitry

Writing a logic 1 to a DDRA bit enables the output buffer for the corresponding port A pin; a logic 0 disables the output buffer.

When bit DDRAx is a logic 1, reading address $0000 reads the PAx data latch. When bit DDRAx is a logic 0, reading address $0000 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit. **Table 6-1** summarizes the operation of the port A pins.

Table 6-1. Port A Pin Operation

Data Direction Bit	**I/O Pin Mode**	**Accesses to Data Bit**	
		Read	**Write**
0	Input, high-impedance	Pin	Latch(1)
1	Output	Latch	Latch

1. Writing affects the data register but does not affect input.

6.3.3 Pulldown Register A

Pulldown register A (PDRA) inhibits the pulldown devices on port A pins programmed as inputs.

NOTE: *If the SWPDI bit in the mask option register is programmed to logic 1, reset initializes all port A pins as inputs with disabled pulldown devices.*

Address: $0010

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	▨	▨	▨	▨	▨	▨	▨	▨
Write:	PDIA7	PDIA6	PDIA5	PDIA4	PDIA3	PDIA2	PDIA1	PDIA0
Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 6-5. Pulldown Register A (PDRA)

PDIA[7:0] — Pulldown Inhibit A Bits

PDIA[7:0] disable the port A pulldown devices. Reset clears PDIA[7:0].

1 = Corresponding port A pulldown device disabled
0 = Corresponding port A pulldown device not disabled

6.3.4 Port A LED Drive Capability

The outputs for the upper four bits of port A (PA4–PA7) can drive light-emitting diodes (LEDs). PA4–PA7 can sink approximately 10 mA of current to V_{SS}.

6.3.5 Port A I/O Pin Interrupts

If the PIRQ bit in the mask option register is programmed to logic 1, PA0–PA3 pins function as external interrupt pins. See **Section 8. External Interrupt Module (IRQ)**.

6.4 Port B

Port B is a 6-bit bidirectional port.

6.4.1 Port B Data Register

The port B data register (PORTB) contains a latch for each port B pin.

Address: $0001

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	PB5	PB4	PB3	PB2	PB1	PB0
Write:	▨	▨						
Reset:	Unaffected by reset							

▨ = Unimplemented

Figure 6-6. Port B Data Register (PORTB)

PB[5:0] — Port B Data Bits

These read/write bits are software programmable. Data direction of each port B pin is under the control of the corresponding bit in data direction register B. Reset has no effect on port B data.

6.4.2 Data Direction Register B

Data direction register B (DDRB) determines whether each port B pin is an input or an output.

Address: $0005

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	0	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
Write:	▨	▨						
Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 6-7. Data Direction Register B (DDRB)

DDRB[5:0] — Data Direction Register B Bits

These read/write bits control port B data direction. Reset clears DDRB[5:0], configuring all port B pins as inputs.

1 = Corresponding port B pin configured as output
0 = Corresponding port B pin configured as input

NOTE: *Avoid glitches on port B pins by writing to the port B data register before changing data direction register B bits from 0 to 1.*

Figure 6-8 shows the I/O logic of port B.

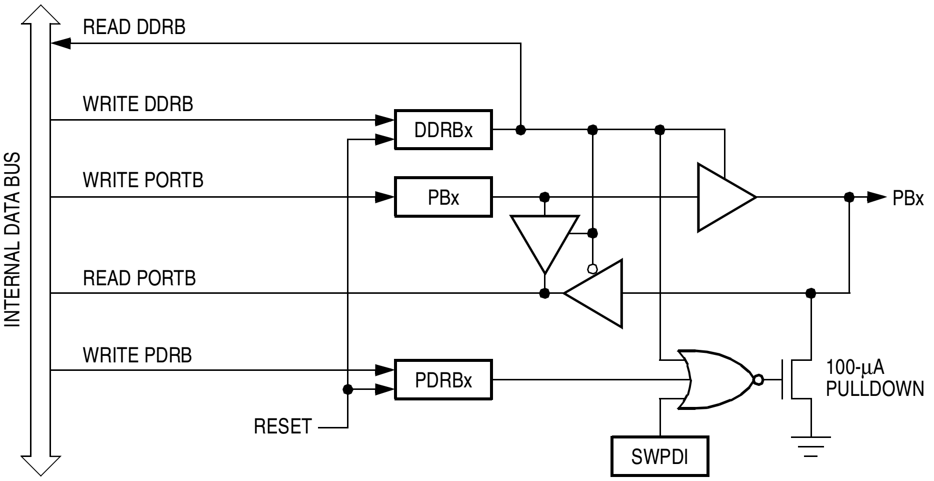

READ DDRB
WRITE DDRB
WRITE PORTB
READ PORTB
WRITE PDRB
INTERNAL DATA BUS
DDRBx
PBx
PDRBx
RESET
SWPDI
PBx
100-µA
PULLDOWN

Figure 6-8. Port B I/O Circuitry

Writing a logic 1 to a DDRB bit enables the output buffer for the corresponding port B pin; a logic 0 disables the output buffer.

When bit DDRBx is a logic 1, reading address $0001 reads the PBx data latch. When bit DDRBx is a logic 0, reading address $0001 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit. **Table 6-2** summarizes the operation of the port B pins.

Table 6-2. Port B Pin Operation

Data Direction Bit	I/O Pin Mode	Accesses to Data Bit	
		Read	**Write**
0	Input, high-impedance	Pin	Latch[1]
1	Output	Latch	Latch

[1] Writing affects the data register, but does not affect input.

6.4.3 Pulldown Register B

Pulldown register B (PDRB) inhibits the pulldown devices on port B pins programmed as inputs.

NOTE: *If the SWPDI bit in the mask option register is programmed to logic 1, reset initializes all port B pins as inputs with disabled pulldown devices.*

Address: $0011

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	▨	▨	▨	▨	▨	▨	▨	▨
Write:	▨	▨	PDIB5	PDIB4	PDIB3	PDIB2	PDIB1	PDIB0
Reset:			0	0	0	0	0	0

▨ = Unimplemented

Figure 6-9. Pulldown Register B (PDRB)

PDIB[7:0] — Pulldown Inhibit B Bits

PDIB[7:0] disable the port B pulldown devices. Reset clears PDIB[7:0].

1 = Corresponding port B pulldown device disabled
0 = Corresponding port B pulldown device not disabled

6.5 5.0-Volt I/O Port Electrical Characteristics

Characteristic(1)	Symbol	Min	Typ(2)	Max	Unit
Current drain per pin excluding PA4–PA7	I	—	25	—	mA
Output high voltage (I_{Load} = –0.8 mA) PA0–PA7, PB0–PB5	V_{OH}	V_{DD} –0.8	—	—	V
Output low voltage (I_{Load} = 1.6 mA) PA0–PA3, PB0–PB5 (I_{Load} = 10.0 mA) PA4–PA7	V_{OL}	— —	— —	0.4 0.4	V
Input high voltage PA0–PA7, PB0–PB5	V_{IH}	0.7 x V_{DD}	—	V_{DD}	V
Input low voltage PA0–PA7, PB0–PB5	V_{IL}	V_{SS}	—	0.2 x V_{DD}	V
I/O ports hi-z leakage current PA0–PA7, PB0–PB5 (without individual pulldown activated)	I_{IL}	—	0.2	±1	μA
Input pulldown current PA0–PA7, PB0–PB5 (with individual pulldown activated)	I_{IL}	35	80	200	μA

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +105°C, unless otherwise noted
2. Typical values reflect average measurements at midpoint of voltage range, 25°C.

6.6 3.3-Volt I/O Port Electrical Characteristics

Characteristic(1)	Symbol	Min	Typ(2)	Max	Unit
Current drain per pin excluding PA4–PA7	I	—	25	—	mA
Output high voltage (I_{Load} = –0.2 mA) PA0–PA7, PB0–PB5	V_{OH}	V_{DD} –0.3	—	—	V
Output low voltage (I_{Load} = 0.4 mA) PA0–PA3, PB0–PB5 (I_{Load} = 5.0 mA) PA4–PA7	V_{OL}	— —	— —	0.3 0.3	V
Input high voltage PA0–PA7, PB0–PB5	V_{IH}	0.7 x V_{DD}	—	V_{DD}	V
Input low voltage PA0–PA7, PB0–PB5	V_{IL}	V_{SS}	—	0.2 x V_{DD}	V
I/O ports hi-z leakage current PA0–PA7, PB0–PB5 (without individual pulldown activated)	I_{IL}	—	0.1	±1	μA
Input pulldown current PA0–PA7, PB0–PB5 (with individual pulldown activated)	I_{IL}	12	30	100	μA

1. V_{DD} = 3.3 Vdc ± 10%, V_{SS}= 0 Vdc, T_A = –40°C to +105°C, unless otherwise noted
2. Typical values reflect average measurements at midpoint of voltage range, 25°C.

Section 7. Computer Operating Properly (COP) Module

7.1 Contents

7.2 Introduction 97

7.3 Operation 98
7.3.1 COP Watchdog Timeout 98
7.3.2 COP Watchdog Timeout Period 98
7.3.3 Clearing the COP Watchdog 98

7.4 Interrupts. 99

7.5 COP Register 99

7.6 Low-Power Modes 100
7.6.1 Stop Mode 100
7.6.2 Wait Mode 100

7.2 Introduction

The computer operating properly (COP) watchdog resets the microcontroller (MCU) in case of software failure. Software that is operating properly periodically services the COP watchdog and prevents COP reset. The COP watchdog function is programmable by the COPEN bit in the mask option register.

Features include:

- Protection from runaway software
- Wait and halt mode operation

7.3 Operation

Operation of the COP is described in this subsection.

7.3.1 COP Watchdog Timeout

Four counter stages at the end of the timer make up the COP watchdog. The COP resets the MCU if the timeout period occurs before the COP watchdog timer is cleared by application software and the $\overline{\mathrm{IRQ}}/V_{PP}$ pin voltage is between V_{SS} and V_{DD}. Periodically clearing the counter starts a new timeout period and prevents COP reset. A COP watchdog timeout indicates that the software is not executing instructions in the correct sequence.

NOTE: *The internal clock drives the COP watchdog. Therefore, the COP watchdog cannot generate a reset for errors that cause the internal clock to stop.*

The COP watchdog depends on a power supply voltage at or above a minimum specification and is not guaranteed to protect against brownout.

7.3.2 COP Watchdog Timeout Period

The COP watchdog timer function is implemented by dividing the output of the real-time interrupt circuit (RTI) by eight. The RTI select bits in the timer status and control register control RTI output, and the selected output drives the COP watchdog. See timer status and control register in **Section 9. Multifunction Timer Module**.

NOTE: *The minimum COP timeout period is seven times the RTI period. The COP is cleared asynchronously with the value in the RTI divider; hence, the COP timeout period will vary between 7x and 8x the RTI period.*

7.3.3 Clearing the COP Watchdog

To clear the COP watchdog and prevent a COP reset, write a logic 0 to bit 0 (COPC) of the COP register at location $07F0 (see **Figure 7-1**).

Clearing the COP bit disables the COP watchdog timer regardless of the $\overline{\text{IRQ}}/V_{PP}$ pin voltage.

If the main program executes within the COP timeout period, the clearing routine should be executed only once. If the main program takes longer than the COP timeout period, the clearing routine must be executed more than once.

NOTE: *Place the clearing routine in the main program and not in an interrupt routine. Clearing the COP watchdog in an interrupt routine might prevent COP watchdog timeouts even though the main program is not operating properly.*

7.4 Interrupts

The COP watchdog does not generate interrupts.

7.5 COP Register

The COP register (COPR) is a write-only register that returns the contents of EPROM location $07F0 when read.

Address: $07F0

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	▨	▨	▨	▨	▨	▨	▨	▨
Write:	▨	▨	▨	▨	▨	▨	▨	COPC
Reset:								0

▨ = Unimplemented

Figure 7-1. COP Register (COPR)

COPC — COP Clear Bit

This write-only bit resets the COP watchdog. Reading address $07F0 returns undefined results.

7.6 Low-Power Modes

The STOP and WAIT instructions have these effects on the COP watchdog.

7.6.1 Stop Mode

The STOP instruction clears the COP watchdog counter and disables the clock to the COP watchdog.

NOTE: *To prevent the STOP instruction from disabling the COP watchdog, program the stop-to-wait conversion bit (SWAIT) in the mask option register to logic 1.*

Upon exit from stop mode by external reset:

- The counter begins counting from $0000.
- The counter is cleared again after the oscillator stabilization delay and begins counting from $0000 again.

Upon exit from stop mode by external interrupt:

- The counter begins counting from $0000.
- The counter is not cleared again after the oscillator stabilization delay and continues counting throughout the oscillator stabilization delay.

NOTE: *Immediately after exiting stop mode by external interrupt, service the COP to ensure a full COP timeout period.*

7.6.2 Wait Mode

The WAIT instruction has no effect on the COP watchdog.

NOTE: *To prevent a COP timeout during wait mode, exit wait mode periodically to service the COP.*

Section 8. External Interrupt Module (IRQ)

8.1 Contents

8.2 Introduction 101

8.3 Operation 102
8.3.1 $\overline{\text{IRQ}}/V_{PP}$ Pin 104
8.3.2 Optional External Interrupts 104

8.4 IRQ Status and Control Register 106

8.5 External Interrupt Timing 107
8.5.1 5.0-Volt External Interrupt Timing Characteristics 107
8.5.2 3.3-Volt External Interrupt Timing Characteristics 107

8.2 Introduction

The external interrupt (IRQ) module provides asynchronous external interrupts to the CPU. These sources can generate external interrupts:

- $\overline{\text{IRQ}}/V_{PP}$ pin
- PA0–PA3 pins

Features include:

- Dedicated external interrupt pin ($\overline{\text{IRQ}}/V_{PP}$)
- Selectable interrupt on four input/output (I/O) pins (PA0–PA3)
- Programmable edge-only or edge- and level-interrupt sensitivity

8.3 Operation

The interrupt request/programming voltage pin ($\overline{\text{IRQ}}/V_{PP}$) and port A pins 0–3 (PA0–PA3) provide external interrupts. The PIRQ bit in the mask option register (MOR) enables PA0–PA3 as IRQ interrupt sources, which are combined into a single ORing function to be latched by the IRQ latch. **Figure 8-1** shows the structure of the IRQ module.

After completing its current instruction, the CPU tests the IRQ latch. If the IRQ latch is set, the CPU then tests the I bit in the condition code register and the IRQE bit in the IRQ status and control register. If the I bit is clear and the IRQE bit is set, the CPU then begins the interrupt sequence. This interrupt is serviced by the interrupt service routine located at $07FA and $07FB.

The CPU clears the IRQ latch while it fetches the interrupt vector, so that another external interrupt request can be latched during the interrupt service routine. As soon as the I bit is cleared during the return from interrupt, the CPU can recognize the new interrupt request. **Figure 8-2** shows the sequence of events caused by an interrupt.

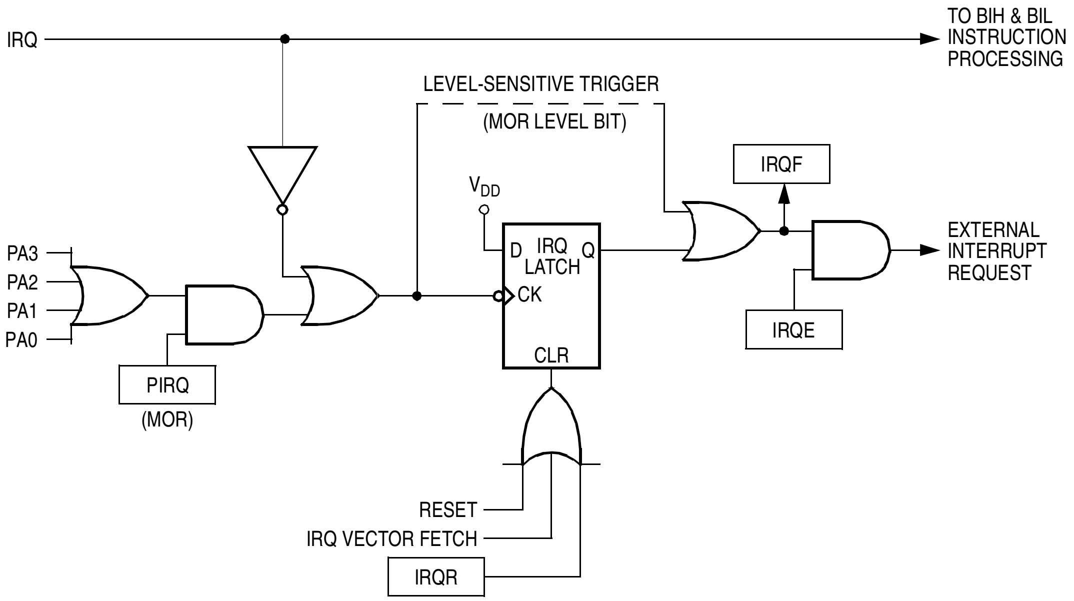

IRQ
TO BIH & BIL INSTRUCTION PROCESSING
LEVEL-SENSITIVE TRIGGER
(MOR LEVEL BIT)
IRQF
V_{DD}
D
IRQ LATCH
Q
CK
CLR
EXTERNAL INTERRUPT REQUEST
PA3
PA2
PA1
PA0
PIRQ
(MOR)
IRQE
RESET
IRQ VECTOR FETCH
IRQR

Figure 8-1. IRQ Module Block Diagram

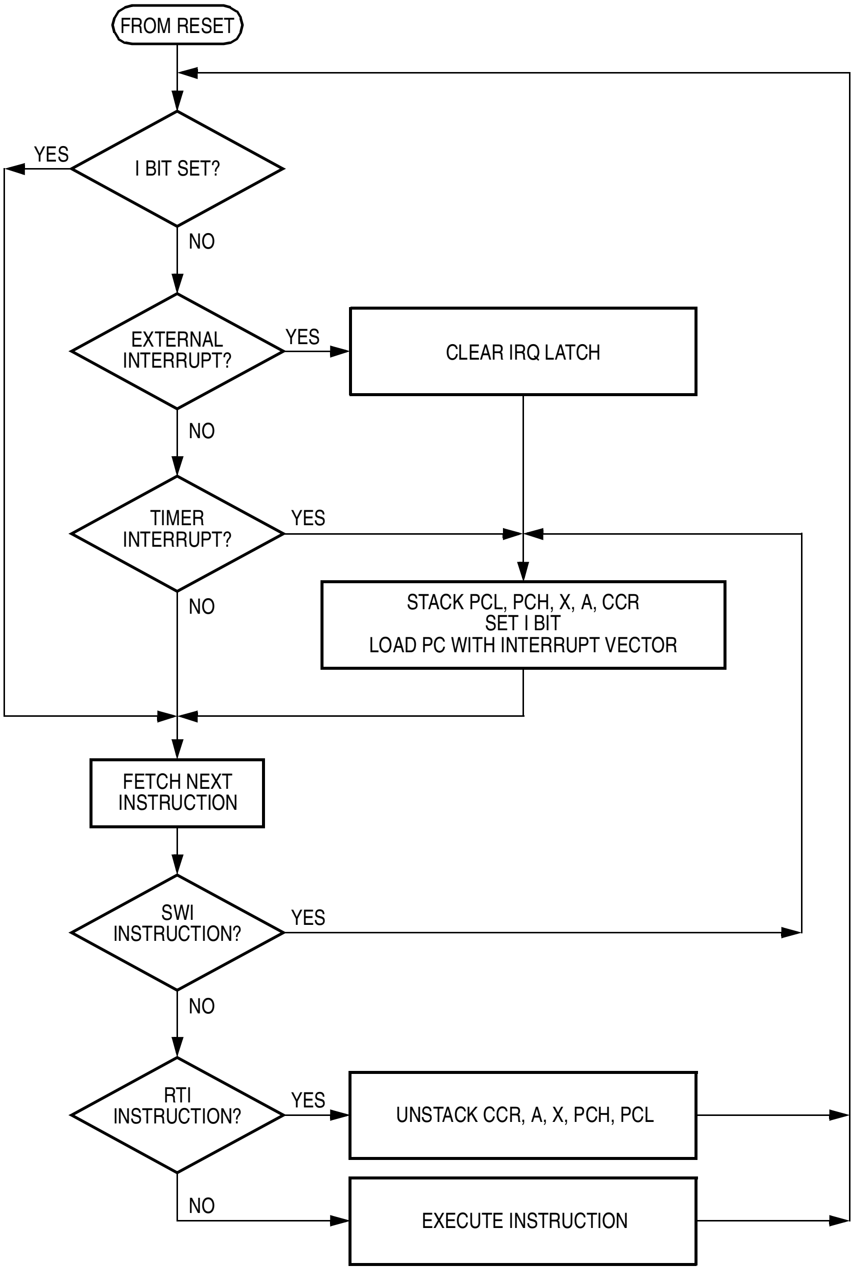

FROM RESET
I BIT SET?
YES
NO
EXTERNAL INTERRUPT?
YES
CLEAR IRQ LATCH
NO
TIMER INTERRUPT?
YES
NO
STACK PCL, PCH, X, A, CCR
SET I BIT
LOAD PC WITH INTERRUPT VECTOR
FETCH NEXT INSTRUCTION
SWI INSTRUCTION?
YES
NO
RTI INSTRUCTION?
YES
UNSTACK CCR, A, X, PCH, PCL
NO
EXECUTE INSTRUCTION

Figure 8-2. Interrupt Flowchart

8.3.1 $\overline{\text{IRQ}}/V_{PP}$ Pin

An interrupt signal on the $\overline{\text{IRQ}}/V_{PP}$ pin latches an external interrupt request. The LEVEL bit in the mask option register provides negative edge-sensitive triggering or both negative edge-sensitive and low level-sensitive triggering for the interrupt function.

If edge- and level-sensitive triggering is selected, a falling edge or a low level on the $\overline{\text{IRQ}}/V_{PP}$ pin latches an external interrupt request. Edge- and level-sensitive triggering allows the use of multiple wired-OR external interrupt sources. An external interrupt request is latched as long as any source is holding the $\overline{\text{IRQ}}/V_{PP}$ pin low.

If level-sensitive triggering is selected, the $\overline{\text{IRQ}}/V_{PP}$ input requires an external resistor to V_{DD} for wired-OR operation. If the $\overline{\text{IRQ}}/V_{PP}$ pin is not used, it must be tied to the V_{DD} supply.

If edge-sensitive-only triggering is selected, a falling edge on the $\overline{\text{IRQ}}/V_{PP}$ pin latches an external interrupt request. A subsequent external interrupt request can be latched only after the voltage level on the $\overline{\text{IRQ}}/V_{PP}$ pin returns to logic 1 and then falls again to logic 0.

The $\overline{\text{IRQ}}/V_{PP}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity. The voltage on this pin can affect the mode of operation and should not exceed V_{DD}.

8.3.2 Optional External Interrupts

The inputs for the lower four bits of port A (PA0–PA3) can be connected to the $\overline{\text{IRQ}}$ pin input of the CPU if enabled by the PIRQ bit in the mask option register. This capability allows keyboard scan applications where the transitions or levels on the I/O pins will behave the same as the $\overline{\text{IRQ}}/V_{PP}$ pin except for the inverted phase (logic 1, rising edge). The active state of the $\overline{\text{IRQ}}/V_{PP}$ pin is a logic 0 (falling edge).

The PA0–PA3 pins are selected as a group to function as IRQ interrupts and are enabled by the IRQE bit in the IRQ status and control register. The PA0–PA3 pins can be positive-edge triggered only or positive-edge and high-level triggered.

If edge- and level-sensitive triggering is selected, a rising edge or a high level on a PA0–PA3 pin latches an external interrupt request. Edge- and level-sensitive triggering allows the use of multiple wired-OR external interrupt sources. As long as any source is holding a PA0–PA3 pin high, an external interrupt request is latched, and the CPU continues to execute the interrupt service routine.

If edge-sensitive only triggering is selected, a rising edge on a PA0–PA3 pin latches an external interrupt request. A subsequent external interrupt request can be latched only after the voltage level of the previous interrupt signal returns to logic 0 and then rises again to logic 1.

NOTE: *The branch if interrupt pin is high (BIH) and branch if interrupt pin is low (BIL) instructions apply only to the level on the* $\overline{IRQ}/V_{PP}$ *pin itself and not to the output of the logic OR function with the PA0–PA3 pins. The state of the individual port A pins can be checked by reading the appropriate port A pins as inputs.*

Enabled PA0–PA3 pins cause an IRQ interrupt regardless of whether these pins are configured as inputs or outputs.

The $\overline{IRQ}$ *pin has an internal Schmitt trigger. The optional external interrupts (PA0–PA3) do not have internal Schmitt triggers.*

The interrupt mask bit (I) in the condition code register (CCR) disables all maskable interrupt requests, including external interrupt requests.

8.4 IRQ Status and Control Register

The IRQ status and control register (ISCR) controls and monitors operation of the IRQ module. All unused bits in the ISCR read as logic 0s. The IRQF bit is cleared and the IRQE bit is set by reset.

Address: $000A

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IRQE	0	0	0	IRQF	0	0	0
Write:		▨	▨	R	▨	▨	IRQR	▨
Reset:	1	0	0	0	0	0	0	0

▨ = Unimplemented R = Reserved

Figure 8-3. IRQ Status and Control Register (ISCR)

IRQR — Interrupt Request Reset Bit

This write-only bit clears the external interrupt request flag.

1 = Clears external interrupt and IRQF bit
0 = No effect on external interrupt and IRQF bit

IRQF — External Interrupt Request Flag

The external interrupt request flag is a clearable, read-only bit that is set when an external interrupt request is pending. Reset clears the IRQF bit.

1 = External interrupt request pending
0 = No external interrupt request pending

IRQE — External Interrupt Request Enable Bit

This read/write bit enables external interrupts. Reset sets the IRQE bit.

1 = External interrupt requests enabled
0 = External interrupt requests disabled

The STOP and WAIT instructions set the IRQE bit so that an external interrupt can bring the MCU out of these low-power modes. In addition, reset sets the I bit which masks all interrupt sources.

8.5 External Interrupt Timing

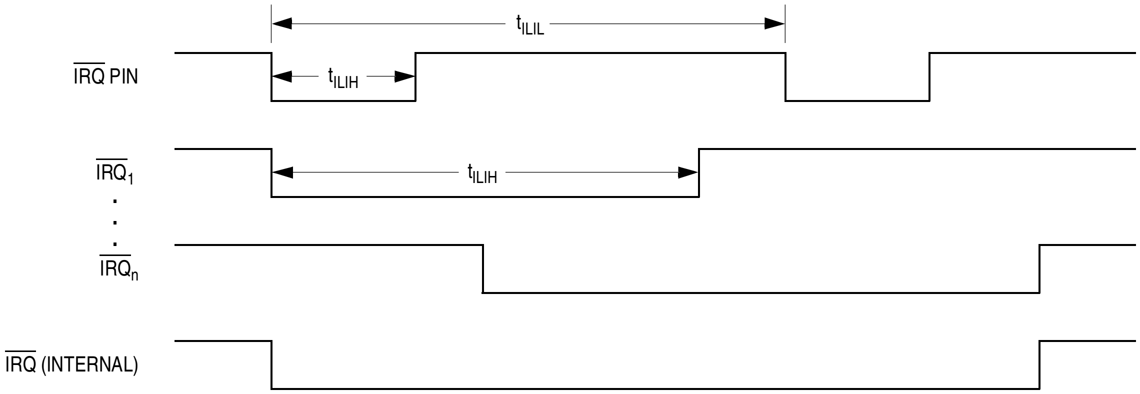


Figure 8-4. External Interrupt Timing

8.5.1 5.0-Volt External Interrupt Timing Characteristics

Characteristic[1]	Symbol	Min	Max	Unit
IRQ interrupt pulse width low (edge-triggered)	t_{ILIH}	1.5	—	t_{cyc}[2]
IRQ interrupt pulse width (edge- and level-triggered)	t_{ILIH}	1.5	Note(3)	t_{cyc}
PA0–PA3 interrupt pulse width high (edge-triggered)	t_{ILIL}	1.5	—	t_{cyc}
PA0–PA3 interrupt pulse width high (edge- and level-triggered)	t_{ILIH}	1.5	Note(3)	t_{cyc}

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +105°C, unless otherwise noted
2. $t_{cyc} = 1/f_{op}$; $f_{op} = f_{osc}/2$.
3. The minimum, t_{ILIL}, should not be less than the number of interrupt service routine cycles plus 19 t_{cyc}.

8.5.2 3.3-Volt External Interrupt Timing Characteristics

Characteristic[1]	Symbol	Min	Max	Unit
IRQ interrupt pulse width low (edge-triggered)	t_{ILIH}	1.5	—	t_{cyc}[2]
IRQ interrupt pulse width (edge- and level-triggered)	t_{ILIH}	1.5	Note(3)	t_{cyc}
PA0–PA3 interrupt pulse width high (edge-triggered)	t_{ILIL}	1.5	—	t_{cyc}
PA0–PA3 interrupt pulse width high (edge- and level-triggered)	t_{ILIH}	1.5	Note(3)	t_{cyc}

1. V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +105°C, unless otherwise noted
2. $t_{cyc} = 1/f_{op}$; $f_{op} = f_{osc}/2$.
3. The minimum, t_{ILIL}, should not be less than the number of interrupt service routine cycles plus 19 t_{cyc}.

Section 9. Multifunction Timer Module

9.1 Contents

9.2 Introduction 109

9.3 Operation 111

9.4 Interrupts. 112

9.5 I/O Registers. 112
9.5.1 Timer Status and Control Register 112
9.5.2 Timer Counter Register 114

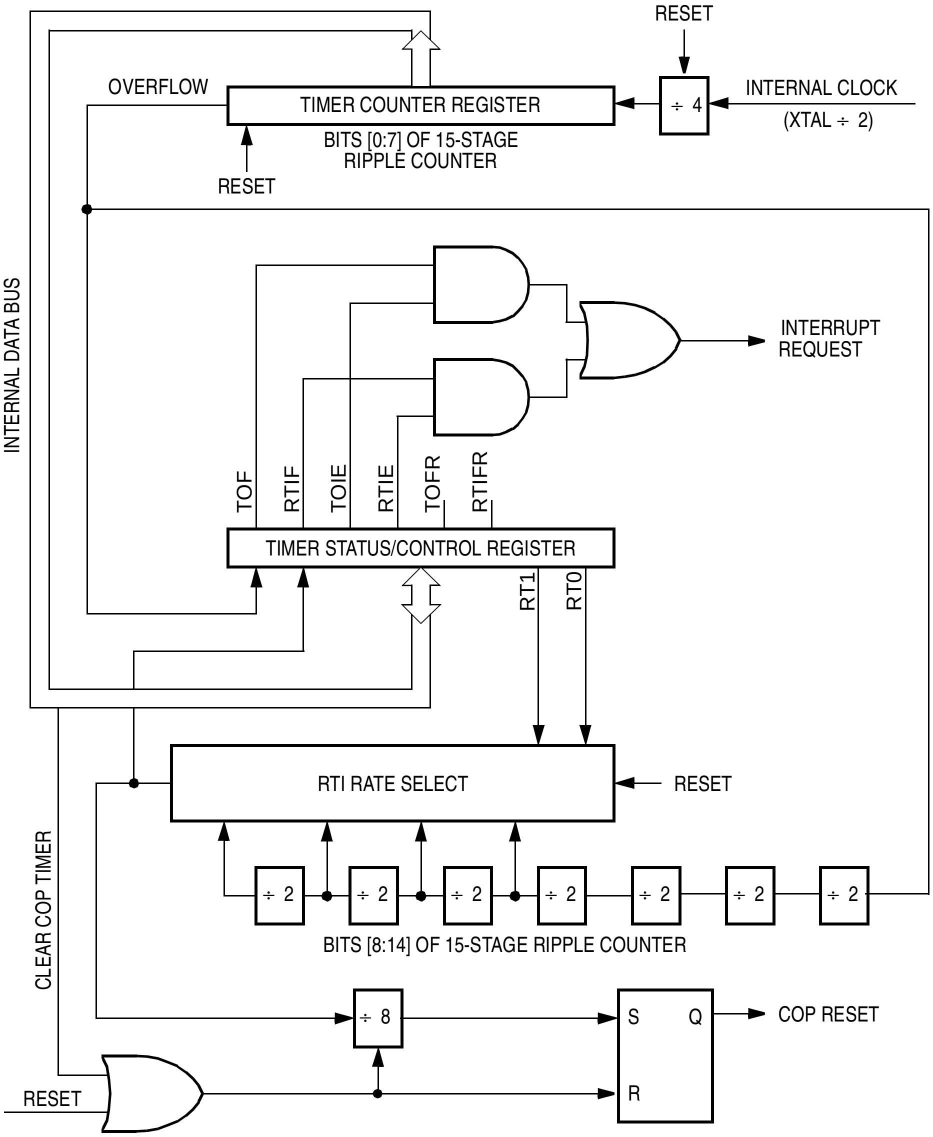
9.6 Low-Power Modes 115
9.6.1 Stop Mode 115
9.6.2 Wait Mode 115

9.2 Introduction

The multifunction timer provides a timing reference with programmable real-time interrupt (RTI) capability. **Figure 9-1** shows the timer organization.

Features include:

- Timer overflow
- Four selectable interrupt rates
- Computer operating properly (COP) watchdog timer



RESET
INTERNAL CLOCK
(XTAL ÷ 2)
÷ 4
OVERFLOW
TIMER COUNTER REGISTER
BITS [0:7] OF 15-STAGE
RIPPLE COUNTER
RESET
INTERNAL DATA BUS
INTERRUPT
REQUEST
TOF
RTIF
TOIE
RTIE
TOFR
RTIFR
TIMER STATUS/CONTROL REGISTER
RT1
RT0
RTI RATE SELECT
RESET
CLEAR COP TIMER
÷ 2
÷ 2
÷ 2
÷ 2
÷ 2
÷ 2
÷ 2
BITS [8:14] OF 15-STAGE RIPPLE COUNTER
÷ 8
S
Q
COP RESET
R
RESET

Figure 9-1. Multifunction Timer Block Diagram

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0008	Timer Status and Control Register (TSCR) See page 112.	Read:	TOF	RTIF	TOIE	RTIE	0	0	RT1	RT0
		Write:	▨	▨			TOFR	RTIFR		
		Reset:	0	0	0	0	0	0	1	1
$0009	Timer Counter Register (TCR) See page 114.	Read:	TMR7	TMR6	TMR5	TMR4	TMR3	TMR2	TMR1	TMR0
		Write:	▨	▨	▨	▨	▨	▨	▨	▨
		Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 9-2. I/O Register Summary

9.3 Operation

A 15-stage ripple counter, preceded by a prescaler that divides the internal clock signal by four, provides the timing reference for the timer functions. The value of the first eight timer stages can be read at any time by accessing the timer counter register at address $0009. A timer overflow function at the eighth stage allows a timer interrupt every 1024 internal clock cycles.

The next four stages lead to the real-time interrupt (RTI) circuit. The RT1 and RT0 bits in the timer status and control register at address $0008 allow a timer interrupt every 16,384, 32,768, 65,536, or 131,072 clock cycles. The last four stages drive the selectable COP system. For information on the COP, refer to the **Section 7. Computer Operating Properly (COP) Module**.

9.4 Interrupts

These timer sources can generate interrupts:

- Timer overflow flag (TOF) — The TOF bit is set when the first eight stages of the counter roll over from $FF to $00. The timer overflow interrupt enable bit, TOIE, enables TOF interrupt requests.
- Real-time interrupt flag (RTIF) — The RTIF bit is set when the selected RTI output becomes active. The real-time interrupt enable bit, RTIE, enables RTIF interrupt requests.

9.5 I/O Registers

These registers control and monitor the timer operation:

- Timer status and control register (TSCR)
- Timer counter register (TCR)

9.5.1 Timer Status and Control Register

The read/write timer status and control register (TSCR) performs these functions:

- Flags timer interrupts
- Enables timer interrupts
- Resets timer interrupt flags
- Selects real-time interrupt rates

Address: $0008

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TOF	RTIF	TOIE	RTIE	0	0	RT1	RT0
Write:	▨	▨			TOFR	RTIFR		
Reset:	0	0	0	0	0	0	1	1

▨ = Unimplemented

Figure 9-3. Timer Status and Control Register (TSCR)

TOF — Timer Overflow Flag

This read-only flag becomes set when the first eight stages of the counter roll over from $FF to $00. TOF generates a timer overflow interrupt request if TOIE is also set. Clear TOF by writing a logic 1 to the TOFR bit. Writing to TOF has no effect. Reset clears TOF.

RTIF — Real-Time Interrupt Flag

This read-only flag becomes set when the selected RTI output becomes active. RTIF generates a real-time interrupt request if RTIE is also set. Clear RTIF by writing a logic 1 to the RTIFR bit. Writing to RTIF has no effect. Reset clears RTIF.

TOIE — Timer Overflow Interrupt Enable Bit

This read/write bit enables timer overflow interrupts. Reset clears TOIE.

1 = Timer overflow interrupts enabled
0 = Timer overflow interrupts disabled

RTIE — Real-Time Interrupt Enable Bit

This read/write bit enables real-time interrupts. Reset clears RTIE.

1 = Real-time interrupts enabled
0 = Real-time interrupts disabled

TOFR — Timer Overflow Flag Reset Bit

Writing a logic 1 to this write-only bit clears the TOF bit. TOFR always reads as logic 0. Reset clears TOFR.

RTIFR — Real-Time Interrupt Flag Reset Bit

Writing a logic 1 to this write-only bit clears the RTIF bit. RTIFR always reads as logic 0. Reset clears RTIFR.

RT1 and RT0 — Real-Time Interrupt Select Bits

These read/write bits select one of four real-time interrupt rates, as shown in **Table 9-1**. Because the selected RTI output drives the COP watchdog, changing the real-time interrupt rate also changes the counting rate of the COP watchdog. Reset sets RT1 and RT0.

NOTE: *Changing RT1 and RT0 when a COP timeout is imminent can cause a real-time interrupt request to be missed or an additional real-time* *interrupt request to be generated. To prevent this occurrence, clear the COP timer before changing RT1 and RT0.*

Table 9-1. Real-Time Interrupt Rate Selection

RT1:RT0	Number of Cycles to RTI	RTI Period(1)	Number of Cycles to COP Reset	COP Timeout Period(1)
0 0	2^{14} = 16,384	8.2 ms	2^{17} = 131,072	65.5 ms
0 1	2^{15} = 32,768	16.4 ms	2^{18} = 262,144	131.1 ms
1 0	2^{16} = 65,536	32.8 ms	2^{19} = 524,288	262.1 ms
1 1	2^{17} = 131,072	65.5 ms	2^{20} = 1,048,576	524.3 ms

1. At 2-MHz bus, 4-MHz XTAL, 0.5 µs per cycle

9.5.2 Timer Counter Register

A 15-stage ripple counter is the core of the timer. The value of the first eight stages is readable at any time from the read-only timer counter register (TCR) shown in **Figure 9-4**.

Address: $0009

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TMR7	TMR6	TMR5	TMR4	TMR3	TMR2	TMR1	TMR0
Write:	▨	▨	▨	▨	▨	▨	▨	▨
Reset:	0	0	0	0	0	0	0	0

▨ = Unimplemented

Figure 9-4. Timer Counter Register (TCR)

Power-on clears the entire counter chain and the internal clock begins clocking the counter. After 4064 cycles (or 16 cycles if the SOSCD bit in the mask option register is set), the power-on reset circuit is released, clearing the counter again and allowing the MCU to come out of reset.

A timer overflow function at the eighth counter stage allows a timer interrupt every 1024 internal clock cycles.

9.6 Low-Power Modes

The STOP and WAIT instructions put the MCU in low power-consumption standby states.

9.6.1 Stop Mode

The STOP instruction has these effects on the timer:

- Clears the timer counter
- Clears interrupt flags (TOF and RTIF) and interrupt enable bits (TOFE and RTIE) in TSCR, removing any pending timer interrupt requests and disabling further timer interrupts.

9.6.2 Wait Mode

The timer remains active after a WAIT instruction. Any enabled timer interrupt request can bring the MCU out of wait mode.

Section 10. Electrical Specifications

10.1 Contents

10.2 Introduction 117
10.3 Maximum Ratings 118
10.4 Operating Temperature Range 119
10.5 Thermal Characteristics 119
10.6 Power Considerations 120
10.7 5.0-Volt DC Electrical Characteristics 121
10.8 3.3-Volt DC Electrical Characteristics 122
10.9 Driver Characteristics 123
10.10 Typical Supply Currents 125
10.11 EPROM Programming Characteristics 126
10.12 5.0-Volt Control Timing 126
10.13 3.3-Volt Control Timing 127

10.2 Introduction

This section contains electrical and timing specifications.

10.3 Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it.

The MCU contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in the table here. Keep V_{In} and V_{Out} within the range $V_{SS} \leq (V_{In}$ or $V_{Out}) \leq V_{DD}$. Connect unused inputs to the appropriate voltage level, either V_{SS} or V_{DD}.

Rating[1]	**Symbol**	**Value**	**Unit**
Supply voltage	V_{DD}	–0.3 to +7.0	V
Current drain per pin (excluding V_{DD}, V_{SS}, and PA4–PA7)	I	25	mA
Input voltage	V_{In}	V_{SS} – 0.3 to V_{DD} + 0.3	V
$\overline{IRQ}/V_{PP}$ pin	V_{PP}	V_{SS} – 0.3 to 2 x V_{DD} + 0.3	V
Storage temperature range	T_{STG}	–65 to +150	°C

[1] Voltages are referenced to V_{SS}.

NOTE: *This device is not guaranteed to operate properly at the maximum ratings. Refer to* ***10.7 5.0-Volt DC Electrical Characteristics*** *and* ***10.8 3.3-Volt DC Electrical Characteristics*** *for guaranteed operating conditions.*

10.4 Operating Temperature Range

Package Type	Symbol	Value (T_L to T_H)	Unit
MC68HC705J1AP(1), DW(2), S(3)	T_A	0 to 70	°C
MC68HC705J1AC(4)P, CDW, CS	T_A	–40 to +85	°C
MC68HC705J1AV(5)P, VDW, VS	T_A	–40 to +105	°C

1. P = plastic dual in-line package (PDIP)
2. DW = small outline integrated circuit (SOIC)
3. S = ceramic DIP (cerdip)
4. C = extended temperature range
5. V = automotive temperature range

10.5 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance MC68HC705J1AP(1) MC68HC705J1ADW(2) MC68HC705J1AS(3)	θ_{JA}	60	°C/W

1. P = plastic dual in-line package (PDIP)
2. DW = small outline integrated circuit (SOIC)
3. S = ceramic DIP (cerdip)

10.6 Power Considerations

The average chip junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \tag{1}$$

Where:

T_A = ambient temperature in °C
θ_{JA} = package thermal resistance, junction to ambient in °C/W
$P_D = P_{INT} + P_{I/O}$
$P_{INT} = I_{CC} \times V_{CC}$ = chip internal power dissipation
$P_{I/O}$ = power dissipation on input and output pins (user-determined)

For most applications, $P_{I/O} < P_{INT}$ and can be neglected.

Ignoring $P_{I/O}$, the relationship between P_D and T_J is approximately:

$$P_D = \frac{K}{T_J + 273°C} \tag{2}$$

Solving equations (1) and (2) for K gives:

$$= P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \tag{3}$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

10.7 5.0-Volt DC Electrical Characteristics

Characteristic(1)	Symbol	Min	Typ(2)	Max	Unit
Output voltage I_{Load} = 10.0 µA I_{Load} = –10.0 µA	V_{OL} V_{OH}	— V_{DD} – 0.1	— —	0.1 —	V
Output high voltage (I_{Load} = –0.8 mA) PA0–PA7, PB0–PB5	V_{OH}	V_{DD} – 0.8	—	—	V
Output low voltage (I_{Load} = 1.6 mA) PA0–PA3, PB0–PB5 (I_{Load} = 10.0 mA) PA4–PA7	V_{OL}	—	—	0.4 0.4	V
Input high voltage PA0–PA7, PB0–PB5, $\overline{\text{IRQ}}/V_{PP}$, $\overline{\text{RESET}}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input low voltage PA0–PA7, PB0–PB5, $\overline{\text{IRQ}}/V_{PP}$, $\overline{\text{RESET}}$, OSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
Supply current Run mode(3) Wait mode(4) Stop mode(5) 25°C –40 to 105°C	I_{DD}	— — — —	3.5 0.45 0.2 2.0	6.0 2.75 10 20	mA mA µA µA
I/O ports hi-z leakage current PA0–PA7, PB0–PB5 (without individual pulldown activated)	I_{IL}	—	0.2	±1	µA
Input pulldown current PA0–PA7, PB0–PB5 (with individual pulldown activated)	I_{IL}	35	80	200	µA
Input pullup current $\overline{\text{RESET}}$	I_{IL}	–15	–35	–85	µA
Input current(6) $\overline{\text{RESET}}$, $\overline{\text{IRQ}}/V_{PP}$, OSC1	I_{In}	—	0.2	±1	µA
Capacitance Ports (as inputs or outputs) $\overline{\text{RESET}}$, $\overline{\text{IRQ}}/V_{PP}$, OSC1, OSC2	C_{Out} C_{In}	— —	— —	12 8	pF
Crystal/ceramic resonator oscillator mode internal resistor OSC1 to OSC2(7)	R_{osc}	1.0	2.0	3.0	MΩ

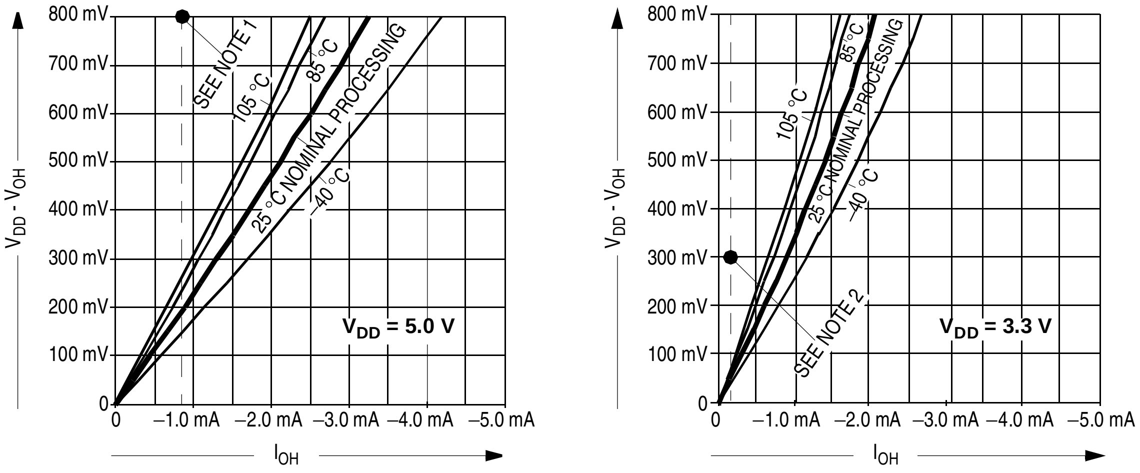
1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +105°C, unless otherwise noted
2. Typical values at midpoint of voltage range, 25°C only
3. Run mode I_{DD} is measured using external square wave clock source (f_{osc} = 4.2 MHz); all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2
4. Wait mode I_{DD}: only timer system active. Wait mode is affected linearly by OSC2 capacitance. Wait mode is measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V. Wait mode I_{DD} is measured using external square wave clock source (f_{osc} = 4.2 MHz); all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2.
5. Stop mode I_{DD} is measured with OSC1 = V_{SS}. Stop mode I_{DD} is measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V
6. Only input high current rated to +1 µA on $\overline{\text{RESET}}$.
7. The R_{osc} value selected for RC oscillator versions of this device is unspecified. See **Appendix C. MC68HSR705J1A** for additional information.

10.8 3.3-Volt DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output voltage I_{Load} = 10.0 µA I_{Load} = –10.0 µA	V_{OL} V_{OH}	— V_{DD}– 0.1	— —	0.1 —	V
Output high voltage (I_{Load} = –0.2 mA) PA0–PA7, PB0–PB5	V_{OH}	V_{DD} – 0.3	—	—	V
Output low voltage (I_{Load} = 0.4 mA) PA0–PA3, PB0–PB5 (I_{Load} = 5.0 mA) PA4–PA7	V_{OL}	—	—	0.3 0.3	V
Input high voltage PA0–PA7, PB0–PB5, $\overline{\text{IRQ}}/V_{PP}$, $\overline{\text{RESET}}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input low voltage PA0–PA7, PB0–PB5, $\overline{\text{IRQ}}/V_{PP}$, $\overline{\text{RESET}}$, OSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
Supply current Run Mode[3] Wait Mode[4] Stop Mode[5] 25°C –40 to 105°C	I_{DD}	— — — —	1.2 0.25 0.1 1.0	4.0 1.5 5 10	mA mA µA µA
I/O ports hi-z leakage current PA0–PA7, PB0–PB5 (without individual pulldown activated)	I_{IL}	—	0.1	±1	µA
Input pulldown current PA0–PA7, PB0–PB5 (with individual pulldown activated)	I_{IL}	12	30	100	µA
Input pullup current $\overline{\text{RESET}}$	I_{IL}	–10	–25	–45	µA
Input current[6] $\overline{\text{RESET}}$, $\overline{\text{IRQ}}/V_{PP}$, OSC1	I_{In}	—	0.1	±1	µA
Capacitance Ports (as inputs or outputs) $\overline{\text{RESET}}$, $\overline{\text{IRQ}}/V_{PP}$, OSC1, OSC2	C_{Out} C_{In}	— —	— —	12 8	pF
Crystal/ceramic resonator oscillator mode internal resistor OSC1 to OSC2[7]	R_{osc}	1.0	2.0	3.0	MΩ

1. V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +105°C, unless otherwise noted
2. Typical values at midpoint of voltage range, 25°C only
3. Run mode I_{DD} is measured using external square wave clock source (f_{osc} = 2.0 MHz); all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2
4. Wait mode I_{DD}: only timer system active. Wait mode is affected linearly by OSC2 capacitance. Wait mode is measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V. Wait mode I_{DD} is measured using external square wave clock source (f_{osc} = 2.0 MHz); all inputs 0.2 V from rail; no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2.
5. Stop mode I_{DD} is measured with OSC1 = V_{SS}. Stop mode I_{DD} is measured with all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} – 0.2 V
6. Only input high current rated to +1 µA on $\overline{\text{RESET}}$.
7. The R_{osc} value selected for RC oscillator versions of this device is unspecified. See **Appendix C. MC68HSR705J1A** for additional information.

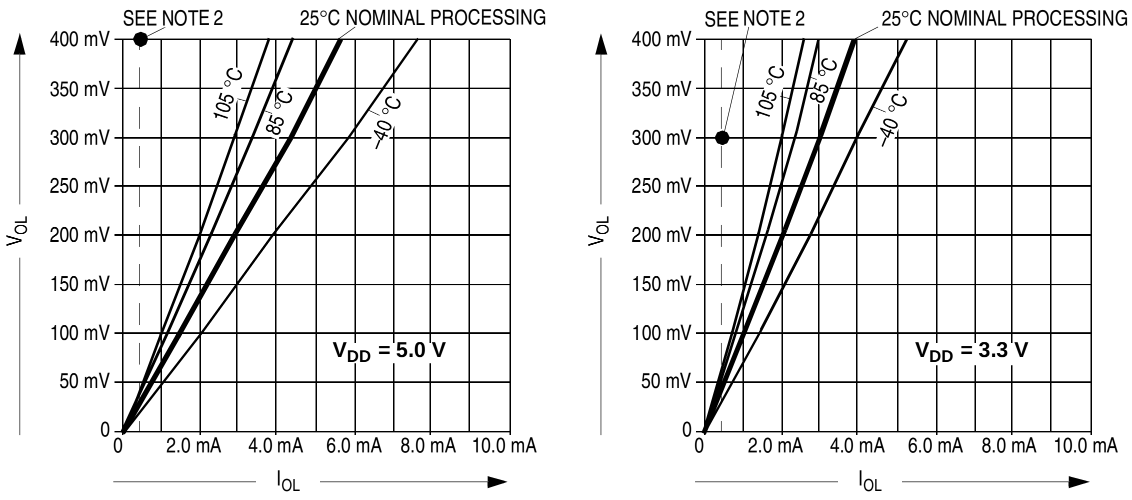
10.9 Driver Characteristics



Notes:

1. At V_{DD} = 5.0 V, devices are specified and tested for ($V_{DD} - V_{OH}$) ≤ 800 mV @ I_{OH} = –0.8 mA.
2. At V_{DD} = 3.3 V, devices are specified and tested for ($V_{DD} - V_{OH}$) ≤ 300 mV @ I_{OH} = –0.2 mA.

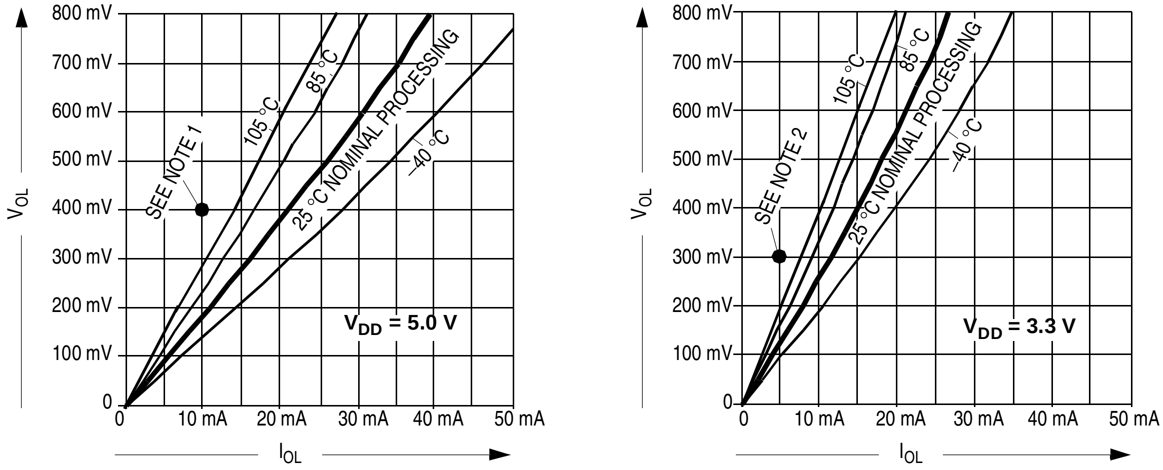
Figure 10-1. PA0–PA7, PB0–PB5 Typical High-Side Driver Characteristics



Notes:

1. At V_{DD} = 5.0 V, devices are specified and tested for V_{OL} ≤ 400 mV @ I_{OL} = 1.6 mA.
2. At V_{DD} = 3.3 V, devices are specified and tested for V_{OL} ≤ 300 mV @ I_{OL} = 0.4 mA.

Figure 10-2. PA0–PA3, PB0–PB5 Typical Low-Side Driver Characteristics

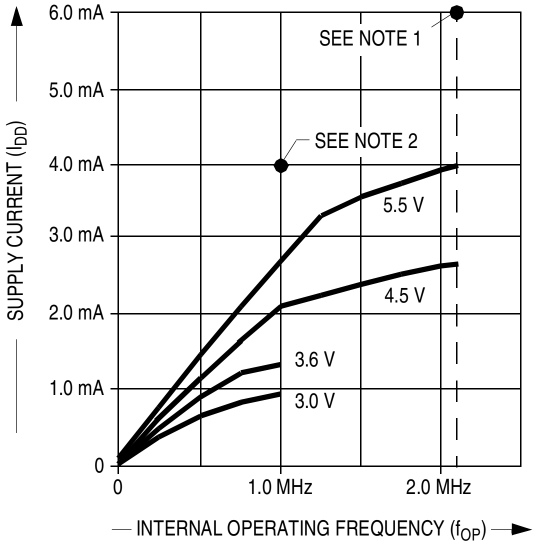


Notes:

1. At V_{DD} = 5.0 V, devices are specified and tested for $V_{OL} \leq 400$ mV @ I_{OL} = 10.0 mA.
2. At V_{DD} = 3.3 V, devices are specified and tested for $V_{OL} \leq 300$ mV @ I_{OL} = 5.0 mA.

Figure 10-3. PA4–PA7 Typical Low-Side Driver Characteristics

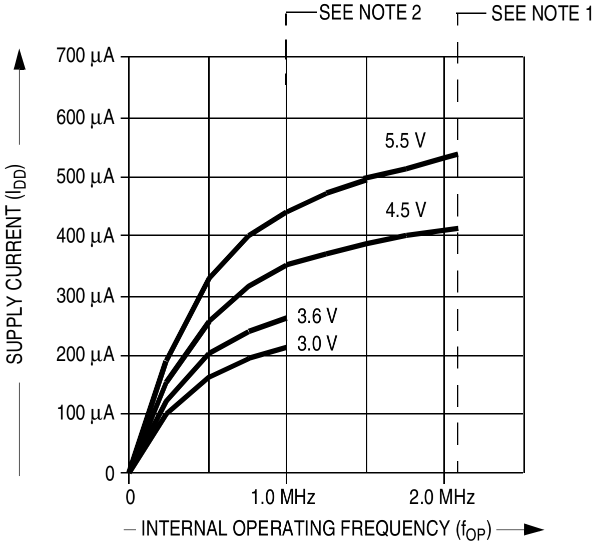
10.10 Typical Supply Currents



Notes:

1. At V_{DD} = 5.0 V, devices are specified and tested for $I_{DD} \leq 6.0$ mA @ f_{OP} = 2.1 MHz.
2. At V_{DD} = 3.3 V, devices are specified and tested for $I_{DD} \leq 4.0$ mA @ f_{OP} = 1.0 MHz.

Figure 10-4. Typical Operating I_{DD} (25°C)



Notes:

1. At V_{DD} = 5.0 V, devices are specified and tested for $I_{DD} \leq 2.75$ mA @ f_{OP} = 2.1 MHz.
2. At V_{DD} = 3.3 V, devices are specified and tested for $I_{DD} \leq 1.5$ mA @ f_{OP} = 1.0 MHz.

Figure 10-5. Typical Wait Mode I_{DD} (25°C)

10.11 EPROM Programming Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Programming voltage $\overline{\text{IRQ}}/V_{PP}$	V_{PP}	16.0	16.5	17.0	V
Programming current $\overline{\text{IRQ}}/V_{PP}$	I_{PP}	—	3.0	10.0	mA
Programming time Per array byte MOR	 t_{EPGM} t_{MPGM}	 4 4	 — —	 — —	ms

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +105°C, unless otherwise noted

10.12 5.0-Volt Control Timing

Characteristic[1]	Symbol	Min	Max	Unit
Oscillator frequency Crystal oscillator option External clock source	f_{osc}	 — dc	 4.2 4.2	MHz
Internal operating frequency (f_{osc} ÷ 2) Crystal oscillator External clock	f_{op}	 — dc	 2.1 2.1	MHz
Cycle time (1 ÷ f_{OP})	t_{cyc}	476	—	ns
$\overline{\text{RESET}}$ pulse width low	t_{RL}	1.5	—	t_{cyc}
$\overline{\text{IRQ}}$ interrupt pulse width low (edge-triggered)	t_{ILIH}	1.5	—	t_{cyc}
$\overline{\text{IRQ}}$ interrupt pulse width low (edge- and level-triggered)	t_{ILIL}	1.5	Note[2]	t_{cyc}
PA0–PA3 interrupt pulse width high (edge-triggered)	t_{IHIL}	1.5	—	t_{cyc}
PA0–PA3 interrupt pulse width (edge- and level-triggered)	t_{IHIH}	1.5	Note[2]	t_{cyc}
OSC1 pulse width	t_{OH}, t_{OL}	200	—	ns

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +105°C, unless otherwise noted
2. The maximum width, t_{ILIL} or t_{ILIH}, should not be more than the number of cycles it takes to execute the interrupt service routine plus 19 t_{cyc} or the interrupt service routine will be re-entered.

10.13 3.3-Volt Control Timing

Characteristic[1]	Symbol	Min	Max	Unit
Oscillator frequency Crystal oscillator option External clock source	f_{osc}	 — dc	 2.0 2.0	MHz
Internal operating frequency ($f_{osc} \div 2$) Crystal oscillator External clock	f_{op}	 — dc	 1.0 1.0	MHz
Cycle time ($1 \div f_{OP}$)	t_{cyc}	1000	—	ns
$\overline{\text{RESET}}$ pulse width low	t_{RL}	1.5	—	t_{cyc}
$\overline{\text{IRQ}}$ interrupt pulse width low (edge-triggered)	t_{ILIH}	1.5	—	t_{cyc}
$\overline{\text{IRQ}}$ interrupt pulse width low (edge- and level-triggered)	t_{ILIL}	1.5	Note[2]	t_{cyc}
PA0–PA3 interrupt pulse width high (edge-triggered)	t_{IHIL}	1.5	—	t_{cyc}
PA0–PA3 interrupt pulse width (edge- and level-triggered)	t_{IHIH}	1.5	Note[2]	t_{cyc}
OSC1 pulse width	t_{OH}, t_{OL}	400	—	ns

1. V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +105°C, unless otherwise noted
2. The maximum width, t_{ILIL} or t_{ILIH}, should not be more than the number of cycles it takes to execute the interrupt service routine plus 19 t_{cyc} or the interrupt service routine will be re-entered.

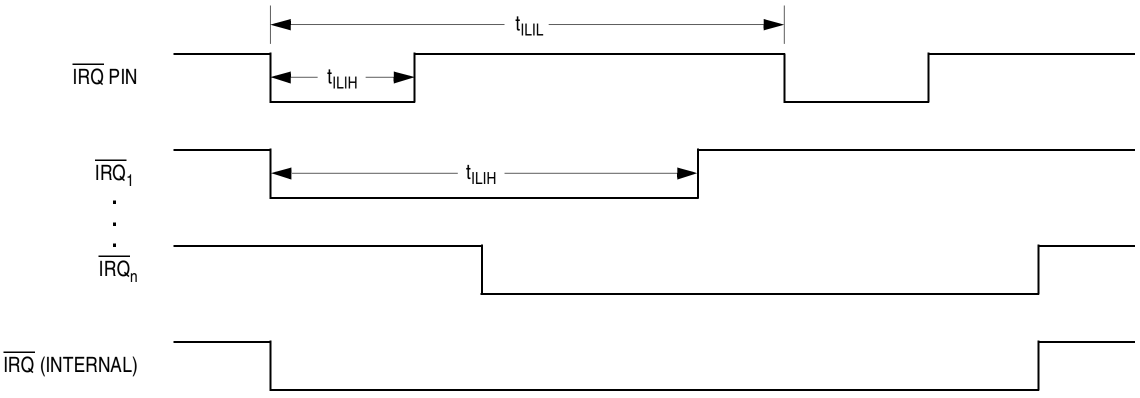
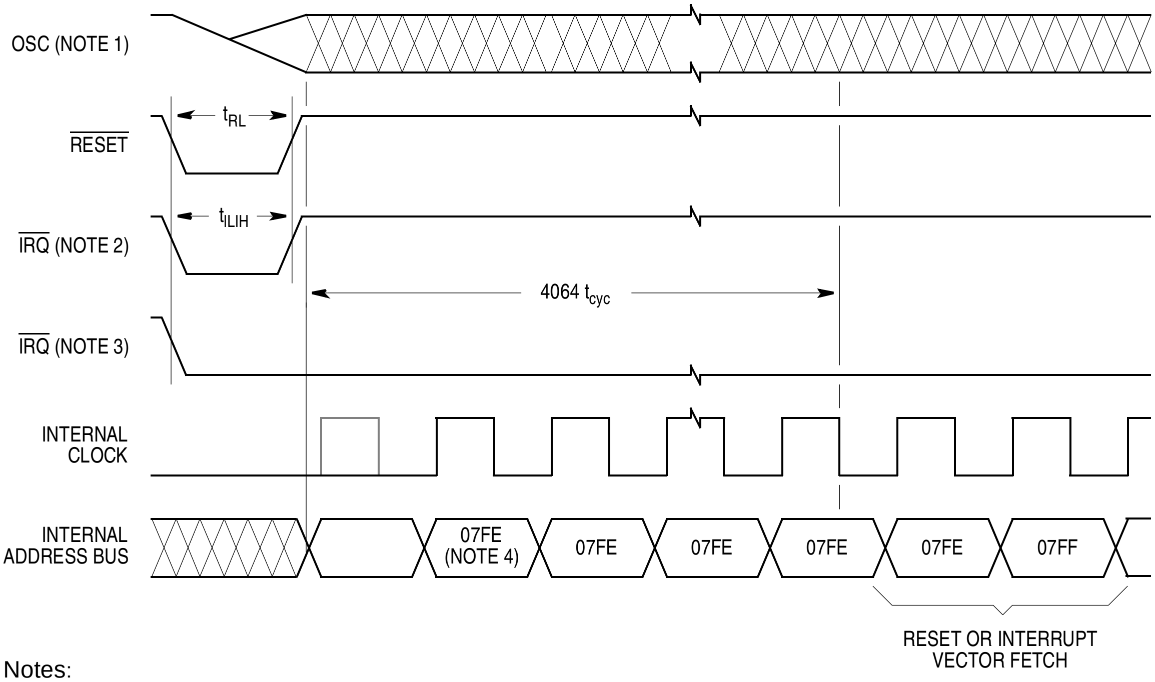

t_{ILIL}
$\overline{IRQ}$ PIN
t_{ILIH}
$\overline{IRQ}_1$
t_{ILIH}
$\overline{IRQ}_n$
$\overline{IRQ}$ (INTERNAL)

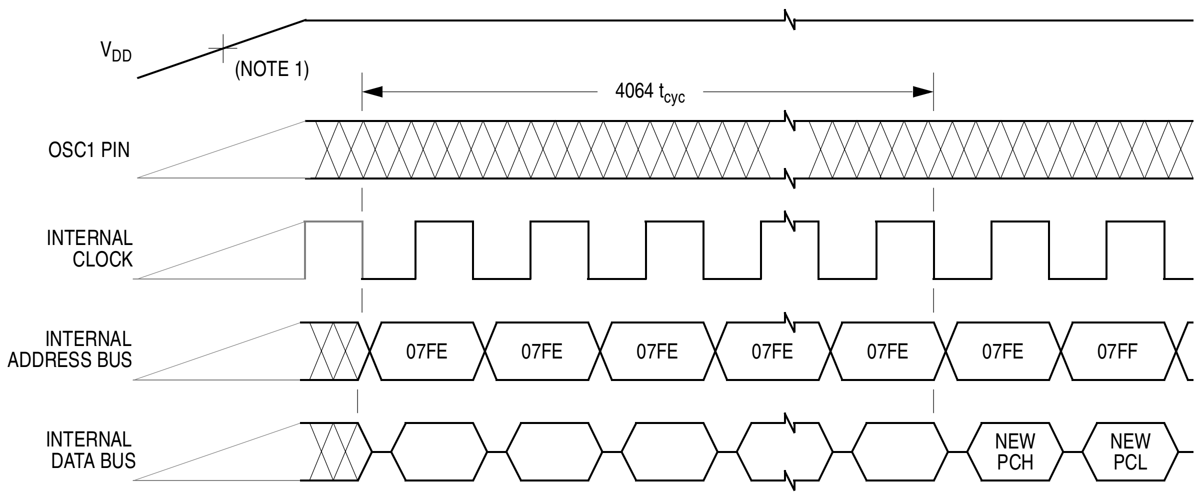
Figure 10-6. External Interrupt Timing


OSC (NOTE 1)
t_{RL}
$\overline{RESET}$
t_{ILIH}
$\overline{IRQ}$ (NOTE 2)
4064 t_{cyc}
$\overline{IRQ}$ (NOTE 3)
INTERNAL CLOCK
INTERNAL ADDRESS BUS
07FE (NOTE 4)
07FE
07FE
07FE
07FE
07FF
RESET OR INTERRUPT VECTOR FETCH

Notes:

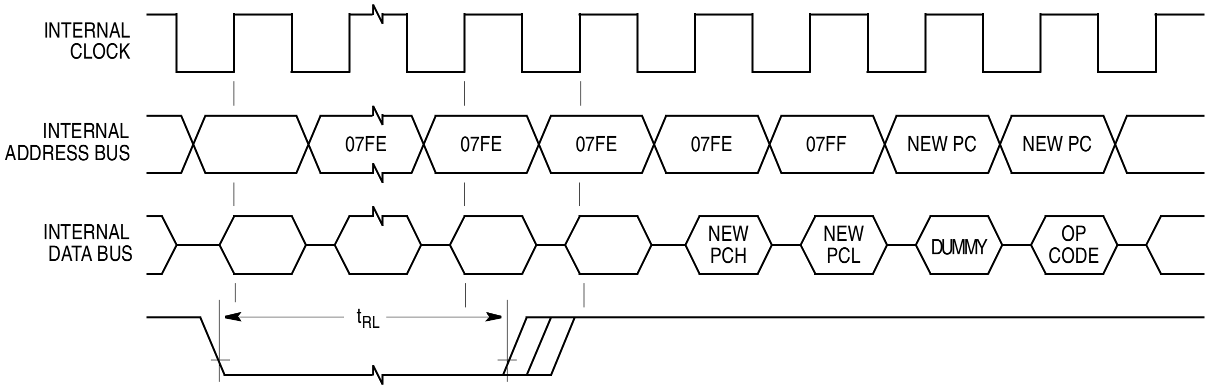
1. Internal clocking from OSC1 pin
2. Edge-triggered external interrupt mask option
3. Edge- and level-triggered external interrupt mask option
4. Reset vector shown as example

Figure 10-7. Stop Mode Recovery Timing


V_{DD}
(NOTE 1)
4064 t_{cyc}
OSC1 PIN
INTERNAL CLOCK
INTERNAL ADDRESS BUS
07FE
07FE
07FE
07FE
07FE
07FE
07FF
INTERNAL DATA BUS
NEW PCH
NEW PCL

Notes:
1. Power-on reset threshold is typically between 1 V and 2 V.
2. Internal clock, internal address bus, and internal data bus are not available externally.

Figure 10-8. Power-On Reset Timing


INTERNAL CLOCK
INTERNAL ADDRESS BUS
07FE
07FE
07FE
07FE
07FF
NEW PC
NEW PC
INTERNAL DATA BUS
NEW PCH
NEW PCL
DUMMY
OP CODE
t_{RL}

Notes:
1. Internal clock, internal address bus, and internal data bus are not available externally.
2. The next rising edge of the internal clock after the rising edge of $\overline{\text{RESET}}$ initiates the reset sequence.

Figure 10-9. External Reset Timing

Section 11. Mechanical Specifications

11.1 Contents

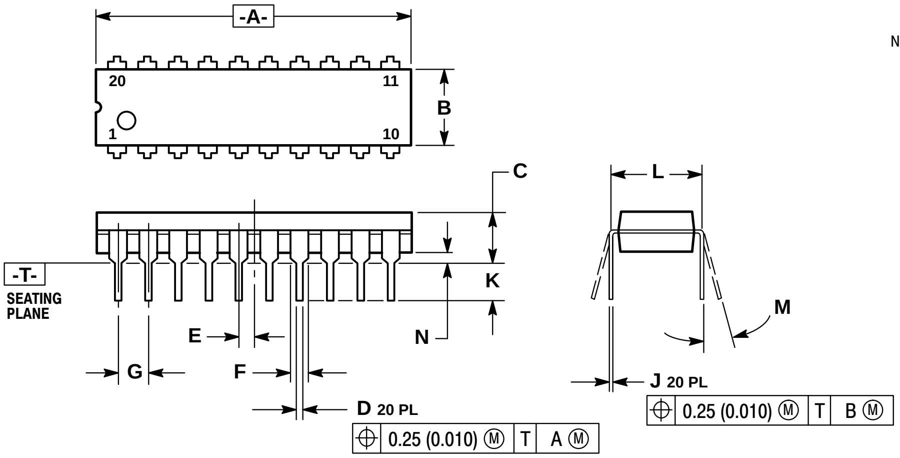
11.2 Introduction 131
11.3 Plastic Dual In-Line Package (Case 738). 132
11.4 Small Outline Integrated Circuit (Case 751) 132
11.5 Ceramic Dual In-Line Package (Case 732) 133

11.2 Introduction

The MC68HC705J1A, the resistor-capacitor (RC) oscillator, and high-speed option devices described in **Appendix A. MC68HRC705J1A**, **Appendix B. MC68HSC705J1A**, and **Appendix C. MC68HSR705J1A** are available in the following packages:

- 738-03 — plastic dual in-line package (PDIP)
- 751D-04 — small outline integrated circuit (SOIC)
- 732-03 — ceramic DIP (cerdip) (windowed)

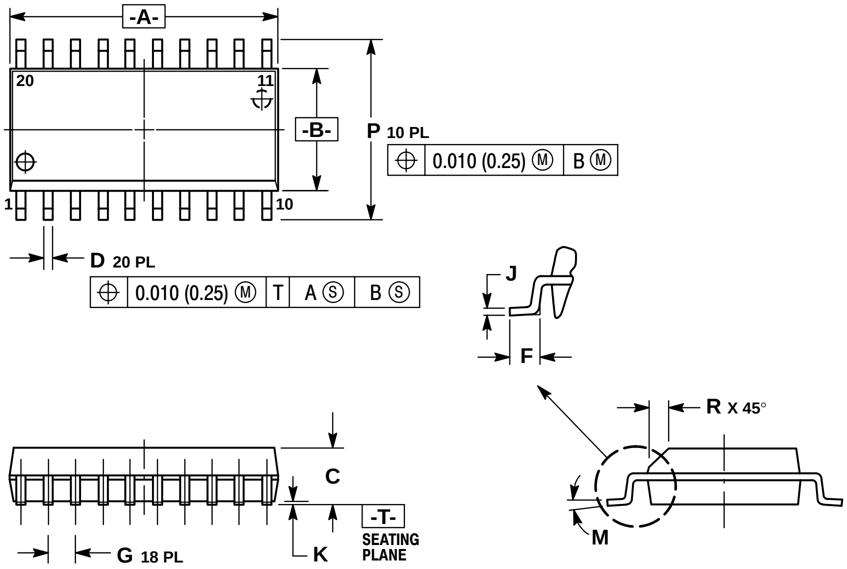
11.3 Plastic Dual In-Line Package (Case 738)


-A-
20
11
1
10
B
C
L
-T-
SEATING PLANE
K
M
E
N
G
F
J 20 PL
0.25 (0.010) Ⓜ T B Ⓜ
D 20 PL
0.25 (0.010) Ⓜ T A Ⓜ

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

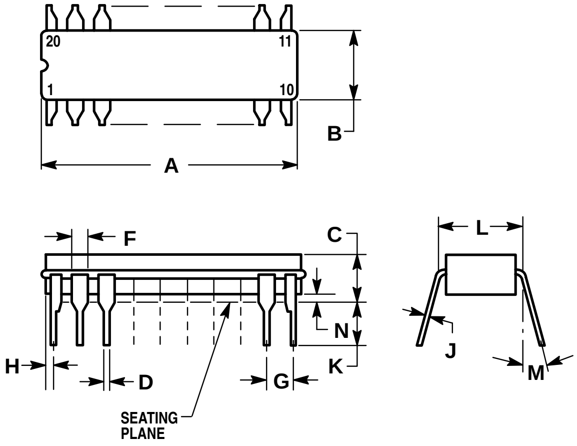
11.4 Small Outline Integrated Circuit (Case 751)


-A-
20
11
-B-
P 10 PL
0.010 (0.25) Ⓜ B Ⓜ
1
10
D 20 PL
0.010 (0.25) Ⓜ T A Ⓢ B Ⓢ
J
F
R X 45°
C
-T-
SEATING PLANE
M
G 18 PL
K

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

11.5 Ceramic Dual In-Line Package (Case 732)



NOTES:

1. LEADS WITHIN 0.010 DIAMETER, TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSIONS A AND B INCLUDE MENISCUS.

	INCHES	
DIM	**MIN**	**MAX**
A	0.940	0.990
B	0.260	0.295
C	0.150	0.200
D	0.015	0.022
F	0.055	0.065
G	0.100 BSC	
H	0.020	0.050
J	0.008	0.012
K	0.125	0.160
L	0.300 BSC	
M	0°	15°
N	0.010	0.040

Section 12. Ordering Information

12.1 Contents

12.2 Introduction 135
12.3 MCU Order Numbers 135

12.2 Introduction

This section contains ordering information for the available package types.

12.3 MCU Order Numbers

Table 12-1 lists the MC order numbers.

Table 12-1. Order Numbers

Package Type	Case Outline	Pin Count	Operating Temperature	Order Number[1]
PDIP	738-03	20	0 to 70°C –40 to +85°C –40 to +105°C	MC68HC705J1AP[2] MC68HC705J1AC[3]P MC68HC705J1AV[4]P
SOIC	751D-04	20	0 to 70°C –40 to +85°C –40 to +105°C	MC68HC705J1ADW[5] MC68HC705J1ACDW MC68HC705J1AVDW
Cerdip	732-03	20	0 to 70°C –40 to +85°C –40 to +105°C	MC68HC705J1AS[6] MC68HC705J1ACS MC68HC705J1AVS

1. Refer to **Appendix A. MC68HRC705J1A**, **Appendix B. MC68HSC705J1A**, and **Appendix C. MC68HSR705J1A** for ordering information on optional high-speed and resistor-capacitor oscillator devices.
2. P = Plastic dual in-line package (PDIP)
3. C = Extended temperature range
4. V = Automotive temperature range
5. DW = Small outline integrated circuit (SOIC)
6. S = Ceramic dual in-line package (cerdip)

Appendix A. MC68HRC705J1A

A.1 Contents

A.2 Introduction 137
A.3 RC Oscillator Connections 138
A.4 Typical Internal Operating Frequency for RC Oscillator Option 139
A.5 Package Types and Order Numbers 140

A.2 Introduction

This appendix introduces the MC68HRC705J1A, a resistor-capacitor (RC) oscillator mask option version of the MC68HC705J1A. All of the information in this document applies to the MC68HRC705J1A with the exceptions given in this appendix.

A.3 RC Oscillator Connections

For greater cost reduction, the RC oscillator mask option allows the configuration shown in **Figure A-1** to drive the on-chip oscillator. Mount the RC components as close as possible to the pins for startup stabilization and to minimize output distortion.

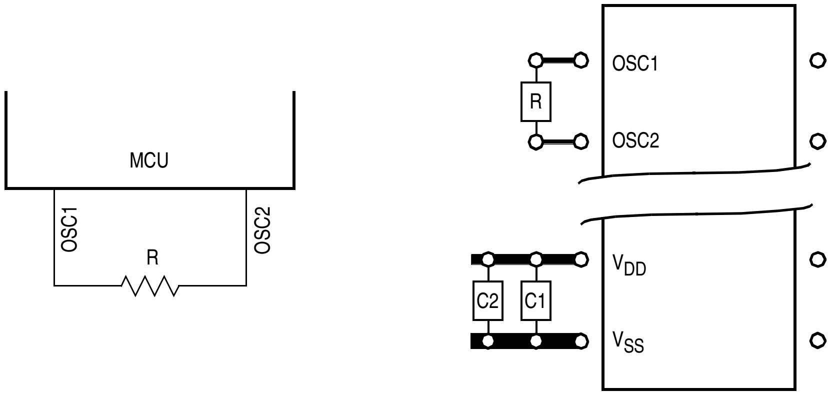


Figure A-1. RC Oscillator Connections

NOTE: *The optional internal resistor is **not** recommended for configurations that use the RC oscillator connections as shown in **Figure A-1**. For such configurations, the oscillator internal resistor (OSCRES) bit of the mask option register should be programmed to a logic 0.*

A.4 Typical Internal Operating Frequency for RC Oscillator Option

Figure A-2 shows typical internal operating frequencies at 25°C for the RC oscillator option.

NOTE: *Tolerance for resistance is ±50%. When selecting resistor size, consider the tolerance to ensure that the resulting oscillator frequency does not exceed the maximum operating frequency.*

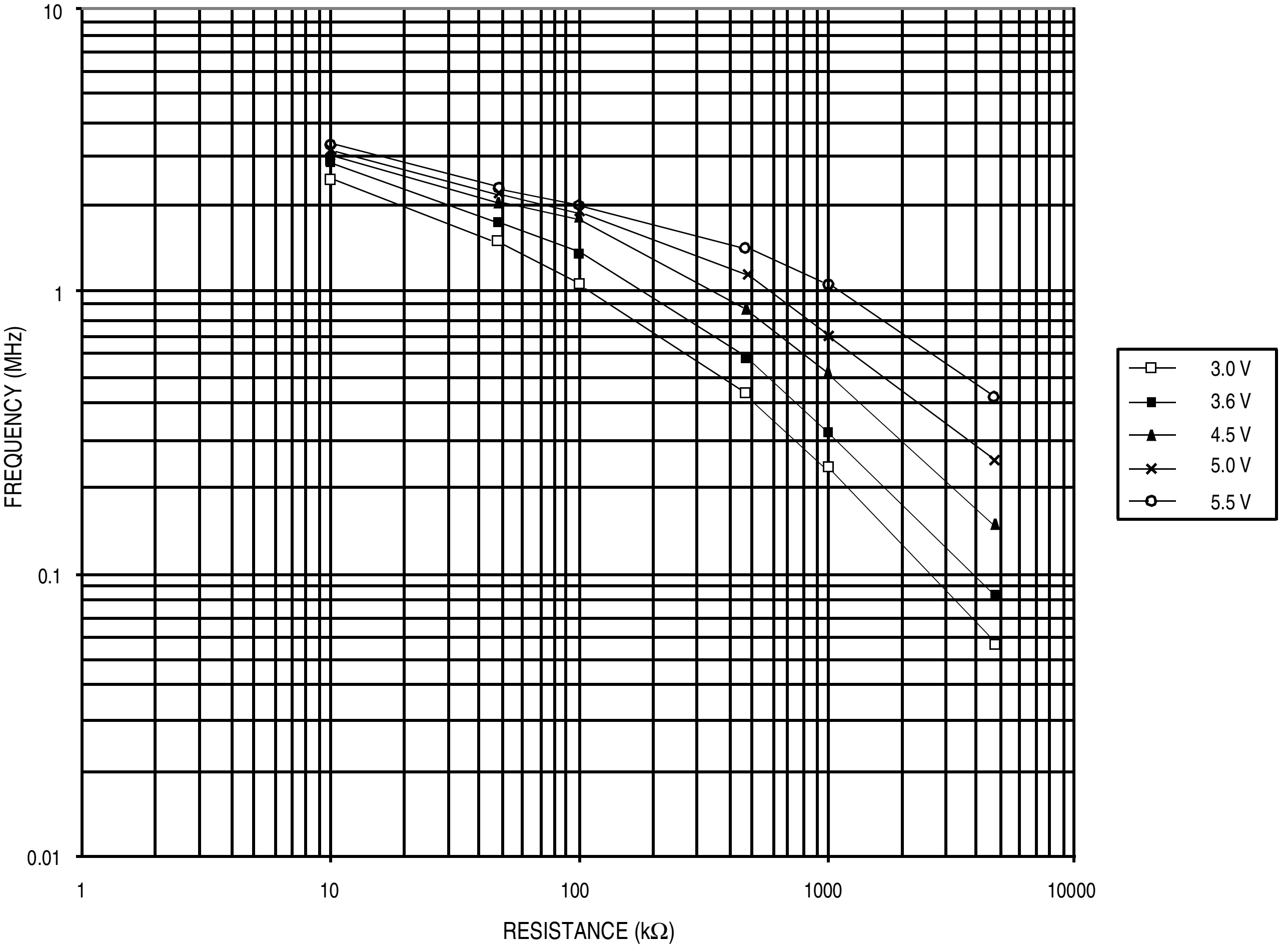


Figure A-2. Typical Internal Operating Frequency for Various V_{DD} at 25°C — RC Oscillator Option Only

A.5 Package Types and Order Numbers

Table A-1. MC68HRC705J1A (RC Oscillator Option) Order Numbers

Package Type	Case Outline	Pin Count	Operating Temperature	Order Number[1]
PDIP	738-03	20	0 to 70°C –40 to +85°C –40 to +105°C	MC68HRC705J1AP[2] MC68HRC705J1AC[3]P MC68HRC705J1AV[4]P
SOIC	751D-04	20	0 to 70°C –40 to +85°C –40 to +105°C	MC68HRC705J1ADW[5] MC68HRC705J1ACDW MC68HRC705J1AVDW
Cerdip	732-03	20	0 to 70°C –40 to +85°C –40 to +105°C	MC68HRC705J1AS[6] MC68HRC705J1ACS MC68HRC705J1AVS

1. Refer to **Section 12. Ordering Information** for standard part ordering information.
2. P = plastic dual in-line package (PDIP)
3. C = extended temperature range
4. V = automotive temperature range
5. DW = small outline integrated circuit (SOIC)
6. S = ceramic dual in-line package (cerdip)

Appendix B. MC68HSC705J1A

B.1 Contents

B.2 Introduction 141
B.3 5.0-Volt DC Electrical Characteristics. 142
B.4 3.3-Volt DC Electrical Characteristics. 142
B.5 Typical Supply Currents 142
B.6 Package Types and Order Numbers .144

B.2 Introduction

This appendix introduces the MC68HSC705J1A, a high-speed version of the MC68HC705J1A. All of the information in this document applies to the MC68HSC705J1A with the exceptions given in this appendix.

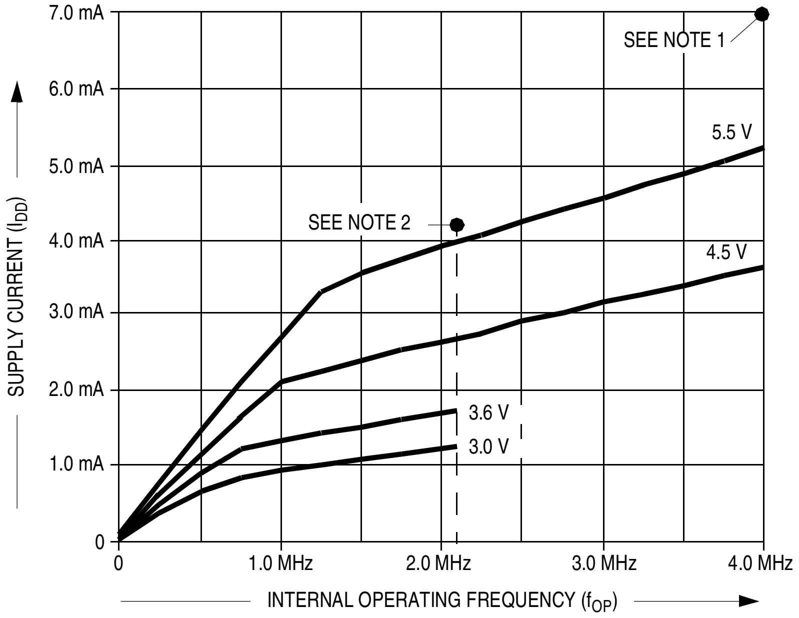
B.3 5.0-Volt DC Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Supply current (f_{OP} = 4.0 MHz) Run Wait	I_{DD}	—	4.25 0.57	7.0 3.25	mA

B.4 3.3-Volt DC Electrical Characteristics

Characteristic	Symbol	Min	Typ	Max	Unit
Supply current (f_{OP} = 2.1 MHz) Run Wait	I_{DD}	—	1.4 0.28	4.25 1.75	mA

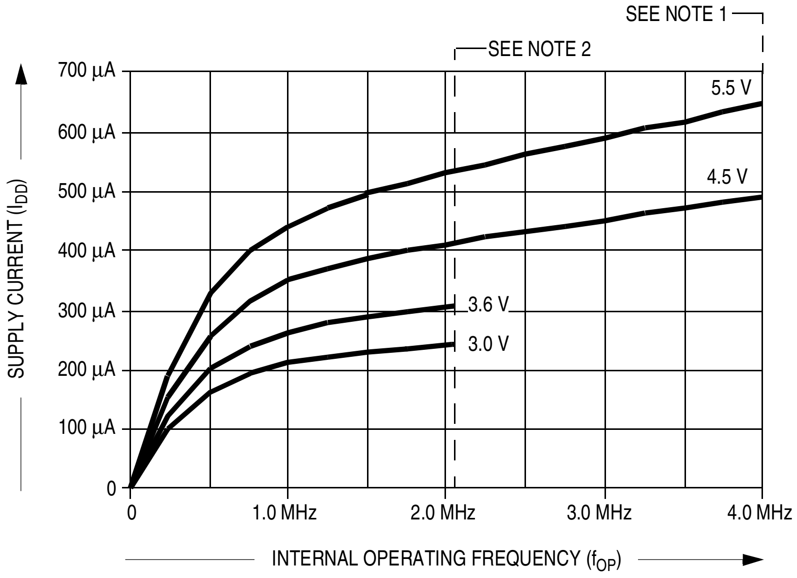
B.5 Typical Supply Currents



Notes:

1. At V_{DD} = 5.0 V, high-speed devices are specified and tested for $I_{DD} \leq 7.0$ mA @ f_{OP} = 4.0 MHz.
2. At V_{DD} = 3.3 V, high-speed devices are specified and tested for $I_{DD} \leq 4.25$ mA @ f_{OP} = 2.1 MHz.

Figure B-1. Typical High-Speed Operating I_{DD} (25°C)



Notes:

1. At V_{DD} = 5.0 V, high-speed devices are specified and tested for $I_{DD} \leq 3.25$ mA @ f_{OP} = 4.0 MHz.
2. At V_{DD} = 3.3 V, high-speed devices are specified and tested for $I_{DD} \leq 1.75$ mA @ f_{OP} = 2.1 MHz.

Figure B-2. Typical High-Speed Wait Mode I_{DD} (25°C)

B.6 Package Types and Order Numbers

Table B-1. MC68HSC705J1A (High Speed) Order Numbers

Package Type	Case Outline	Pin Count	Operating Temperature	Order Number[1]
PDIP	738-03	20	0 to 70°C –40 to +85°C	MC68HSC705J1AP[2] MC68HSC705J1AC[3]P
SOIC	751D-04	20	0 to 70°C –40 to +85°C	MC68HSC705J1ADW[4] MC68HSC705J1ACDW
Cerdip	732-03	20	0 to 70°C –40 to +85°C	MC68HSC705J1AS[5] MC68HSC705J1ACS

1. Refer to **Section 12. Ordering Information** for standard part ordering information.
2. P = plastic dual in-line package (PDIP)
3. C = extended temperature range
4. DW = small outline integrated circuit (SOIC)
5. S = ceramic dual in-line package (cerdip)

Appendix C. MC68HSR705J1A

C.1 Contents

C.2 Introduction 145
C.3 RC Oscillator Connections (External Resistor). 145
C.4 Typical Internal Operating Frequency at 25°C for High-Speed RC Oscillator Option. 146
C.5 RC Oscillator Connections (No External Resistor) 147
C.6 Typical Internal Operating Frequency versus Temperature (No External Resistor) 148
C.7 Package Types and Order Numbers 149

C.2 Introduction

This appendix introduces the MC68HSR705J1A, a high-speed version of the MC68HRC705J1A. All of the information in this document applies to the MC68HSR705J1A with the exceptions given in this appendix.

C.3 RC Oscillator Connections (External Resistor)

Refer to **Appendix A. MC68HRC705J1A** for a description of the resistor-capacitor (RC) oscillator connections with external resistor.

C.4 Typical Internal Operating Frequency at 25°C for High-Speed RC Oscillator Option

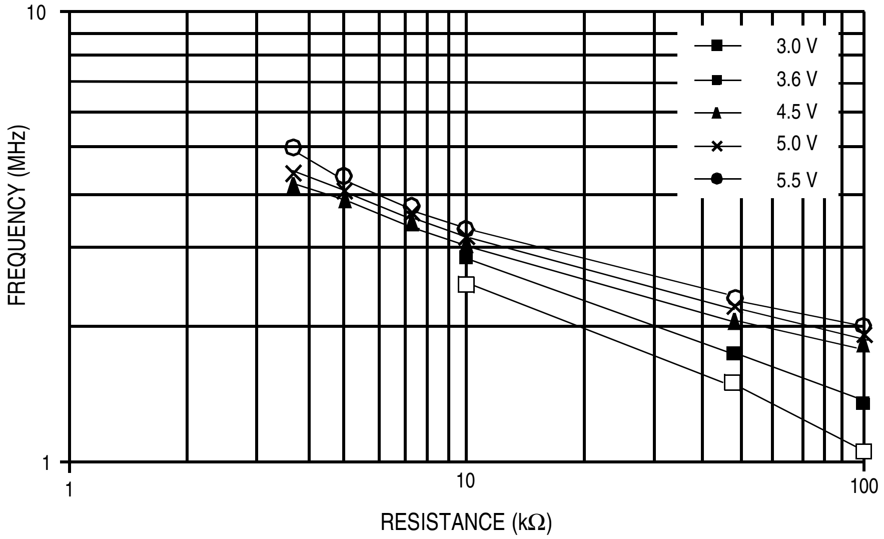


Figure C-1. Typical Internal Operating Frequency at 25°C for High-Speed RC Oscillator Option

For lower frequency operation characteristics, refer to **Appendix A. MC68HRC705J1A**.

NOTE: *Tolerance for resistance is ±50 percent. When selecting resistor size, consider the tolerance to ensure that resulting oscillator frequency does not exceed the maximum operating frequency.*

C.5 RC Oscillator Connections (No External Resistor)

For maximum cost reduction, the RC oscillator mask connections shown in **Figure C-2** allow the on-chip oscillator to be driven with **no** external components. This can be accomplished by programming the oscillator internal resistor (OSCRES) bit in the mask option register to a logic 1. When programming the OSCRES bit for the MC68HSR705J1A, an internal resistor is selected which yields typical internal oscillator frequencies as shown in **Figure C-3**. The internal resistance for this device is different than the resistance of the selectable internal resistor on the MC68HC705J1A and the MC68HSC705J1A devices.

NOTE: *This option is not available on the ROM version of this device (MC68HC05J1A).*

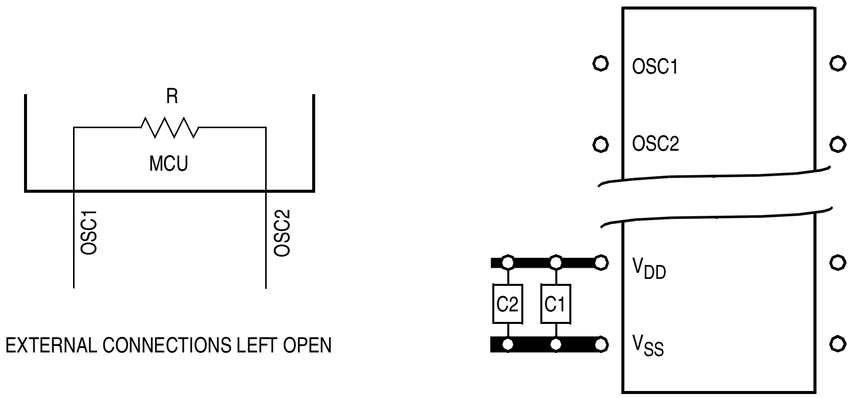


Figure C-2. RC Oscillator Connections (No External Resistor)

C.6 Typical Internal Operating Frequency versus Temperature (No External Resistor)

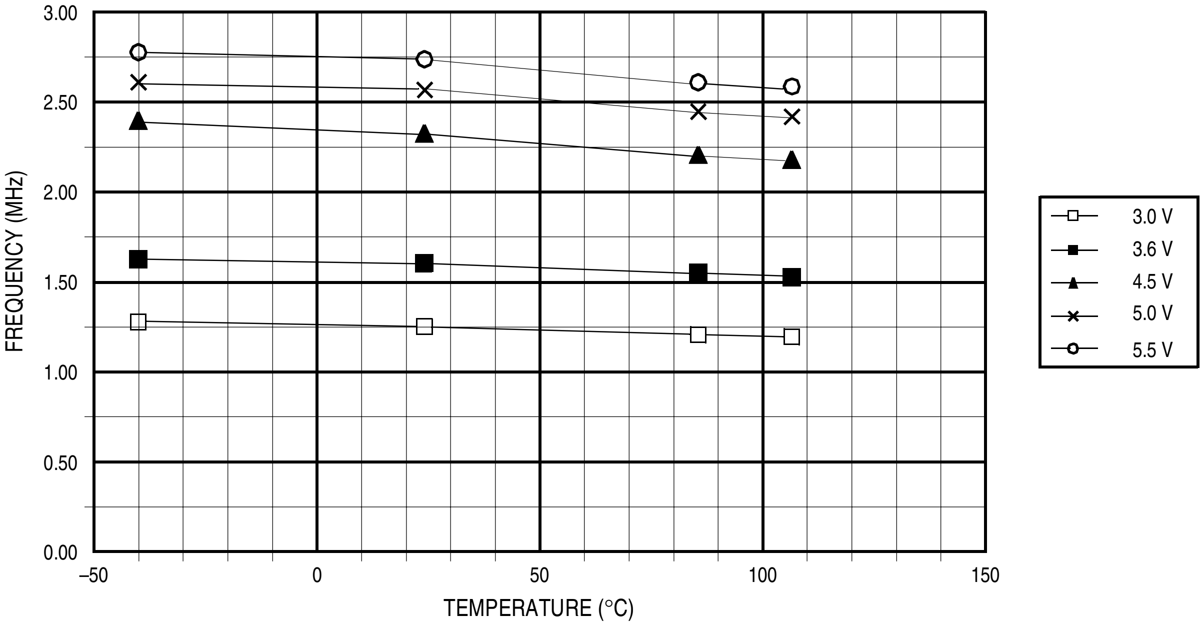


Figure C-3. Typical Internal Operating Frequency versus Temperature (OSCRES Bit = 1)

NOTE: *Due to process variations, operating voltages, and temperature requirements, the internal resistance and tolerance are unspecified. Typically for a given voltage and temperature, the frequency should not vary more than ±500 kHz. However, this data is not guaranteed. It is the user's responsibility to ensure that the resulting internal operating frequency meets the user's requirements.*

C.7 Package Types and Order Numbers

Table C-1. MC68HSR705J1A (High-Speed RC Oscillator Option) Order Numbers(1)

Package Type	Case Outline	Pin Count	Operating Temperature	Order Number
PDIP	738-03	20	0 to 70°C –40 to +85°C	MC68HSR705J1AP(2) MC68HSR705J1AC(3)P
SOIC	751D-04	20	0 to 70°C –40 to +85°C	MC68HSR705J1ADW(4) MC68HSR705J1ACDW
Cerdip	732-03	20	0 to 70°C –40 to +85°C	MC68HSR705J1AS(5) MC68HSR705J1ACS

1. Refer to **Section 12. Ordering Information** for standard part ordering information.
2. P = plastic dual in-line package (PDIP)
3. C = extended temperature range
4. DW = small outline integrated circuit (SOIC)
5. S = ceramic dual in-line package (cerdip)

Index

A

accumulator register (A) 48
addressing modes 52

B

block diagram 23
brownout 98

C

C bit 51
central processor unit (CPU) 45
computer operating properly (COP) module 97
condition code register (CCR) 50
COP watchdog 82
  COP in stop mode 100
  COP in wait mode 100
  COP register (COPR) 99
  COP reset 72
  features 97
  interrupts 99
  low-power modes 100
  operation 98
  programmable option 25
COPEN bit 42
CPU 46
  features 46
  instruction set 52
  instruction set summary 61
  instruction types 55
  opcode map 67
  programming model 47

CPU registers
  accumulator register (A). 48
  index register (X) 48
  program counter register (PC) 50
  stack pointer register (SP) 49

D

data direction registers
  data direction register A (DDRA) 90
  data direction register B (DDRB) 93
data-retention mode 84

E

ELAT bit. 39
electrical specifications 117
  control timing 126, 127
  DC electrical characteristics. 121, 122
  driver characteristics 123
  maximum ratings 118
  MC68HSC705J1A (high-speed option) 142
  MC68HSR705J1A (high-speed RC oscillator option) 145
  operating temperature range 119
  port A 95
  port B 95
  power considerations 120
  thermal resistance 119
  typical supply currents 125
electrostatic damage 87
EPGM bit 39
EPMSEC bit. 41
EPROM
  EPROM security programmable option 25
EPROM/OTPROM. 38
  erasing 40
  programming 38, 40
  programming characteristics 43
  programming register (EPROG). 39

external interrupt module (IRQ) 101
external interrupt pins 31
external reset. 72

G

general description 21

H

H bit 51

I

I bit. 51
index register (X) 48
instruction set 52
  addressing modes 52
  instruction set summary 61
  instruction types 55
  opcode map 67
instruction types. 55
interrupts
  external interrupt 73, 74
  external interrupt logic 74
  external interrupt module 101
  external interrupt timing 75, 107
  external interrupt vector 76
  features 101
  interrupt flowchart. 78, 103
  interrupt processing 76
  interrupt sources 73
  interrupt stacking order 77
  IRQ module block diagram. 102
  $\overline{\text{IRQ}}$ status and control register (ISCR) 106
  $\overline{\text{IRQ}}/V_{PP}$ pin 101, 104
  operation 102
  optional external interrupts. 104
  pin sensitivity selection. 104
  pin triggering option 25
  port A external interrupts programmable option. 25

- real-time interrupts . . . 76
- reset/interrupt vector addresses. . . . 77
- software interrupt . . . 73
- software interrupt vector. . . . 76
- sources. . . . 73
- timer interrupt vector . . . 76
- timer interrupts . . . 76, 112
- timer overflow. . . . 76

IRQ latch . . . 73

$\overline{\text{IRQ}}/V_{PP}$ pin . . . 31, 98, 104

IRQE bit . . . 106

IRQF bit . . . 106

IRQR bit . . . 106

J

junction temperature . . . 120

L

LEVEL bit. . . . 42

low-power modes . . . 79
- COP timeout period . . . 82
- data-retention mode . . . 80, 84
- effects on clock generation . . . 81
- effects on COP . . . 82
- effects on CPU . . . 82
- effects on EPROM/OTPROM. . . . 84
- effects on timer. . . . 83
- exiting stop mode . . . 80
- exiting wait mode . . . 80
- flowchart (STOP/HALT/WAIT) . . . 86
- halt mode . . . 79
- STOP instruction flowchart. . . . 86
- stop mode . . . 79, 82
- stop recovery timing . . . 85
- timer . . . 115
- timing of stop mode recovery . . . 85
- wait mode. . . . 79

M

mask option register (MOR) 40
    programming 41
MC68HC705J1A
    features 24
MC68HRC705J1A (RC oscillator option) 137
    operating frequency 139
    order numbers 140
    package types 140
    RC oscillator connections. 138
MC68HSC705J1A (high-speed option) 141
    DC electrical characteristics. 142
    order numbers 144
    package types 144
    typical operating current. 142
    typical wait mode current 143
MC68HSR705J1A (high-speed RC oscillator option) 145
    operating frequencies (with OSCRES bit set) 148
    operating frequency 146
    order numbers 149
    package types 149
    RC oscillator. 147
    RC oscillator connections. 147
mechanical specifications 131
memory 33
    EPROM/OTPROM 38
    EPROM/OTPROM programming 38
    features 33
    I/O register summary 35
    mask option register. 40
    memory map 34
    RAM 37
MPGM bit. 39
multifunction timer module. 109

N

N bit 51

O

opcode map 67

options (mask) 40

options (programmable) 25

ordering information 135
    MC68HRC705J1A (RC oscillator option) 140
    MC68HSC705J1A (high-speed option) 144
    MC68HSR705J1A (high-speed RC oscillator option) 149
    order numbers 135, 140, 144, 149

OSC1 pin 27

OSC2 pin 27

oscillator
    crystal oscillator internal resistor option 25
    delay counter programmable option 25
    on-chip oscillator stabilization delay 71
    pins 27

OSCRES bit 41

P

PA0–PA3 pins 101

package types 135

parallel input/output (I/O) ports 87

pin assignments 26

PIRQ bit 42

port A
    data direction register (DDRA) 90
    data register (PORTA) 89
    electrical characteristics 95
    I/O circuitry 90
    I/O pin interrupts (PA0–PA3) 92
    LED drive capability 92
    pin operation 91
    pins 31
    pulldown register (PDRA) 91

port B
    data direction register (DDRB) 93
    electrical characteristics 95

I/O circuitry 93
pin operation 94
pins. 31
port B data register (PORTB). 92
pulldown register (PDRB). 94

power dissipation. 120

power-on reset. 71

program counter (PC) 50

programmable options. 25

programming model (CPU) 47

pulldown register A (PDRA). 91

pulldown register B (PDRB). 94

pulldown resistors
programmable option 25

R

RAM. 37
stack RAM 76

registers
CPU 48
I/O register summary 35
parallel I/O port register summary 88

$\overline{\text{RESET}}$ pin. 30, 72

resets. 70
COP register (COPR). 72
COP watchdog reset 72
external reset 72
external reset timing. 72
illegal address 72
power-on reset (POR) 71
power-on reset timing. 71
reset sources 70
reset/interrupt vector addresses. 77

resistors (pulldown)
programmable option 25

RT1, RT0 bits 113

RTIE bit 113
RTIF bit 113
RTIFR bit 113

S

Schmitt trigger 31, 104, 105
SOSCD bit 41
stack pointer register (SP) 49
STOP instruction 81, 100, 106
stop mode 82, 100
    effect on COP watchdog 100
    effects on timer. 115
    STOP instruction flowchart. 86
    stop recovery timing 85
stop/halt mode programmable option 25
SWAIT bit 42
SWPDI bit 42

T

thermal resistance 120
timer
    block diagram. 110
    features 109
    I/O registers 112
    interrupts 76, 112
    low-power modes 115
    operation 111
    timer counter register 114
    timer interrupt vector 76
    timer status and control register (TSCR) 112
TOF bit. 113
TOFR bit 113
TOIE bit 113

V

V_{DD} pin 25

V_{SS} pin. 25

W

WAIT instruction 81, 100, 106

wait mode 100

  effects on timer. 115

Z

Z bit 51

Index

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