11

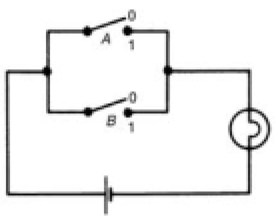
Boolean algebra and logic circuits

11.1 Boolean algebra and switching circuits

A **two-state device** is one whose basic elements can only have one of two conditions. Thus, two-way switches, which can either be on or off, and the binary numbering system, having the digits 0 and 1 only, are two-state devices. In Boolean algebra, if A represents one state, then $\overline{A}$, called 'not-A', represents the second state.

The or-function

In Boolean algebra, the **or**-function for two elements A and B is written as $A+B$, and is defined as 'A, or B, or both A and B'. The equivalent electrical circuit for a two-input **or**-function is given by two switches connected in parallel. With reference to Fig. 11.1(a), the lamp will be on when A is on, when B is on, or when both A and B are on. In the table shown in Fig. 11.1(b), all the possible switch combinations are shown in columns 1 and 2, in which a 0 represents a switch being off and a 1 represents the switch being on, these columns being called the inputs. Column 3 is called the output and a 0 represents the lamp being off and a 1 represents the lamp being on. Such a table is called a **truth table**.



(a) Switching circuit for or - function

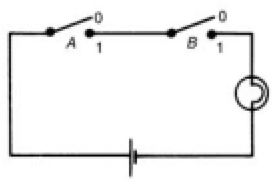
1	2	3
Input (switches)		Output (lamp)
A	B	$Z=A+B$
0	0	0
0	1	1
1	0	1
1	1	1

(b) Truth table for or - function

Figure 11.1

The and-function

In Boolean algebra, the **and**-function for two elements A and B is written as $A \cdot B$ and is defined as 'both A and B'. The equivalent electrical circuit for a two-input **and**-function is given by two switches connected in series. With reference to Fig. 11.2(a) the lamp will be on only when both A and B are on. The truth table for a two-input **and**-function is shown in Fig. 11.2(b).



(a) Switching circuit for and - function

Input (switches)		Output (lamp)
A	B	$Z=A.B$
0	0	0
0	1	0
1	0	0
1	1	1

(b) Truth table for and - function

Figure 11.2

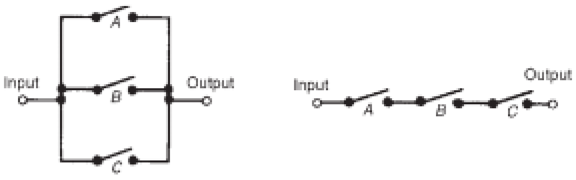
The not-function

In Boolean algebra, the **not**-function for element A is written as $\overline{A}$, and is defined as 'the opposite to A'. Thus if A means switch A is on, $\overline{A}$ means that switch A is off. The truth table for the **not**-function is shown in Table 11.1

Table 11.1

Input A	Output $Z=\overline{A}$
0	1
1	0

In the above, the Boolean expressions, equivalent switching circuits and truth tables for the three functions used in Boolean algebra are given for a two-input system. A system may have more than two inputs and the Boolean expression for a three-input **or**-function having elements A, B and C is $A+B+C$. Similarly, a three-input **and**-function is written as $A \cdot B \cdot C$. The equivalent electrical circuits and truth tables for three-input **or** and **and**-functions are shown in Figs 11.3(a) and (b) respectively.



Input A	Input B	Input C	Output $Z = A + B + C$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

(a) The or - function electrical circuit and truth table

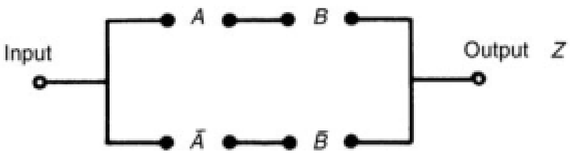
Input A	Input B	Input C	Output $Z = A.B.C$
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

(b) The and - function electrical circuit and truth table

Figure 11.3

1	2	3	4	5
A	B	$A.B$	$\overline{A}.\overline{B}$	$Z = AB + \overline{A}.\overline{B}$
0	0	0	1	1
0	1	0	0	0
1	0	0	0	0
1	1	1	0	1

(a) Truth table for $Z = A.B + \overline{A}.\overline{B}$



(b) Switching circuit for $Z = A.B + \overline{A}.\overline{B}$

Figure 11.4

To achieve a given output, it is often necessary to use combinations of switches connected both in series and in parallel. If the output from a switching circuit is given by the Boolean expression $Z = A \cdot B + \overline{A} \cdot \overline{B}$, the truth table is as shown in Fig. 11.4(a). In this table, columns 1 and 2 give all the possible combinations of A and B. Column 3 corresponds to $A \cdot B$ and column 4 to $\overline{A} \cdot \overline{B}$, i.e. a 1 output is obtained when $A = 0$ and when $B = 0$. Column 5 is the **or**-function applied to columns 3 and 4 giving an output of $Z = A \cdot B + \overline{A} \cdot \overline{B}$. The corresponding switching circuit is shown in Fig. 11.4(b) in which A and B are connected in series to give $A \cdot B$, $\overline{A}$ and $\overline{B}$ are connected in series to give $\overline{A} \cdot \overline{B}$, and $A \cdot B$ and $\overline{A} \cdot \overline{B}$ are connected in parallel to give $A \cdot B + \overline{A} \cdot \overline{B}$. The circuit symbols used are such that A means the switch is on when A is 1, $\overline{A}$ means the switch is on when A is 0, and so on.

Problem 1. Derive the Boolean expression and construct a truth table for the switching circuit shown in Fig. 11.5.

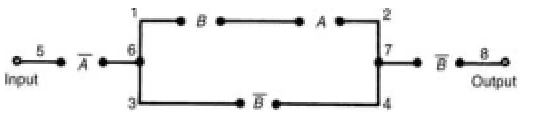


Figure 11.5

The switches between 1 and 2 in Fig. 11.5 are in series and have a Boolean expression of $B \cdot A$. The parallel circuit 1 to 2 and 3 to 4 have a Boolean expression of $(B \cdot A + \overline{B})$. The parallel circuit can be treated as a single switching unit, giving the equivalent of switches 5 to 6, 6 to 7 and 7 to 8 in series. Thus the output is given by:

$$Z = \overline{A} \cdot (B \cdot A + \overline{B}) \cdot \overline{B}$$

The truth table is as shown in Table 11.2. Columns 1 and 2 give all the possible combinations of switches A and B. Column 3 is the **and**-function applied to columns 1 and 2, giving $B \cdot A$. Column 4 is $\overline{B}$, i.e., the opposite to column 2. Column 5 is the **or**-function applied to columns 3 and 4. Column 6 is $\overline{A}$, i.e. the opposite to column 1. The output is column 7 and is obtained by applying the **and**-function to columns 4, 5 and 6.

Table 11.2

1	2	3	4	5	6	7
A	B	$B \cdot A$	$\overline{B}$	$B \cdot A + \overline{B}$	$\overline{A}$	$Z = \overline{A} \cdot (B \cdot A + \overline{B}) \cdot \overline{B}$
0	0	0	1	1	1	1
0	1	0	0	0	1	0
1	0	0	1	1	0	0
1	1	1	0	1	0	0

Problem 2. Derive the Boolean expression and construct a truth table for the switching circuit shown in Fig. 11.6.

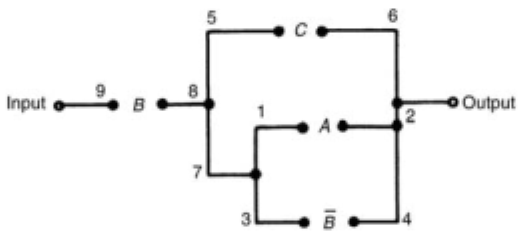


Figure 11.6

The parallel circuit 1 to 2 and 3 to 4 gives $(A+\overline{B})$ and this is equivalent to a single switching unit between 7 and 2. The parallel circuit 5 to 6 and 7 to 2 gives $C+(A+\overline{B})$ and this is equivalent to a single switching unit between 8 and 2. The series circuit 9 to 8 and 8 to 2 gives the output

$$\boldsymbol{Z = B\cdot[C+(A+\overline{B})]}$$

The truth table is shown in Table 11.3. Columns 1, 2 and 3 give all the possible combinations of A, B and C. Column 4 is $\overline{B}$ and is the opposite to column 2. Column 5 is the **or**-function applied to columns 1 and 4, giving $(A+\overline{B})$. Column 6 is the **or**-function applied to columns 3 and 5 giving $C+(A+\overline{B})$. The output is given in column 7 and is obtained by applying the **and**-function to columns 2 and 6, giving $Z = B\cdot[C+(A+\overline{B})]$.

Table 11.3

1	2	3	4	5	6	7
A	B	C	$\overline{B}$	$A+\overline{B}$	$C+(A+\overline{B})$	$Z=B\cdot[C+(A+\overline{B})]$
0	0	0	1	1	1	0
0	0	1	1	1	1	0
0	1	0	0	0	0	0
0	1	1	0	0	1	1
1	0	0	1	1	1	0
1	0	1	1	1	1	0
1	1	0	0	1	1	1
1	1	1	0	1	1	1

Problem 3. Construct a switching circuit to meet the requirements of the Boolean expression: $Z = A\cdot\overline{C}+\overline{A}\cdot B+\overline{A}\cdot B\cdot\overline{C}$ Construct the truth table for this circuit.

The three terms joined by **or**-functions, $(+)$, indicate three parallel branches,

having: branch 1 A **and** $\overline{C}$ in series

branch 2 $\overline{A}$ **and** B in series

and branch 3 $\overline{A}$ **and** B **and** $\overline{C}$ in series

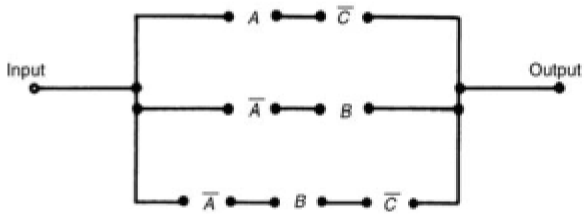


Figure 11.7

Hence the required switching circuit is as shown in Fig. 11.7. The corresponding truth table is shown in Table 11.4.

Table 11.4

1	2	3	4	5	6	7	8	9
A	B	C	$\overline{C}$	$A\cdot\overline{C}$	$\overline{A}$	$\overline{A}\cdot B$	$\overline{A}\cdot B\cdot\overline{C}$	$Z=A\cdot\overline{C}+\overline{A}\cdot B$ $+\overline{A}\cdot B\cdot\overline{C}$
0	0	0	1	0	1	0	0	0
0	0	1	0	0	1	0	0	0
0	1	0	1	0	1	1	1	1
0	1	1	0	0	1	1	0	1
1	0	0	1	1	0	0	0	1
1	0	1	0	0	0	0	0	0
1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	0	0	0

Column 4 is $\overline{C}$, i.e. the opposite to column 3

Column 5 is $A\cdot\overline{C}$, obtained by applying the **and**-function to columns 1 and 4

Column 6 is $\overline{A}$, the opposite to column 1

Column 7 is $\overline{A}\cdot B$, obtained by applying the **and**-function to columns 2 and 6

Column 8 is $\overline{A}\cdot B\cdot\overline{C}$, obtained by applying the **and**-function to columns 4 and 7

Column 9 is the output, obtained by applying the **or**-function to columns 5, 7 and 8

Problem 4. Derive the Boolean expression and construct the switching circuit for the truth table given in Table 11.5.

Table 11.5

	A	B	C	Z
1	0	0	0	1
2	0	0	1	0
3	0	1	0	1
4	0	1	1	1
5	1	0	0	0
6	1	0	1	1
7	1	1	0	0
8	1	1	1	0

Examination of the truth table shown in Table 11.5 shows that there is a 1 output in the Z-column in rows 1, 3, 4 and 6. Thus, the Boolean expression and switching circuit should be such that a 1 output is obtained for row 1 **or** row 3 **or** row 4 **or** row 6. In row 1, A is 0 **and** B is 0 **and** C is 0 and this corresponds to the Boolean expression $\overline{A} \cdot \overline{B} \cdot \overline{C}$. In row 3, A is 0 **and** B is 1 **and** C is 0, i.e. the Boolean expression in $\overline{A} \cdot B \cdot \overline{C}$. Similarly in rows 4 and 6, the Boolean expressions are $\overline{A} \cdot B \cdot C$ and $A \cdot \overline{B} \cdot C$ respectively. Hence the Boolean expression is:

$$\boldsymbol{Z = \overline{A} \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot B \cdot \overline{C} + \overline{A} \cdot B \cdot C + A \cdot \overline{B} \cdot C}$$

The corresponding switching circuit is shown in Fig. 11.8. The four terms are joined by **or**-functions, (+), and are represented by four parallel circuits. Each term has three elements joined by an **and**-function, and is represented by three elements connected in series.

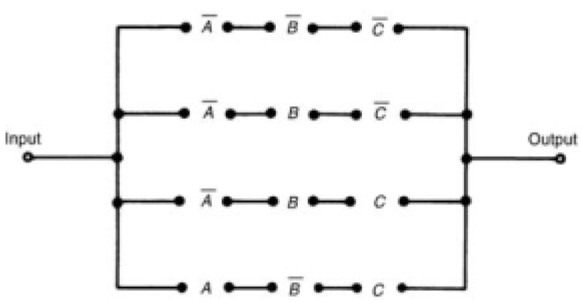


Figure 11.8

Now try the following exercise.

Exercise 46 Further problems on Boolean algebra and switching circuits

In Problems 1 to 4, determine the Boolean expressions and construct truth tables for the switching circuits given.

1. The circuit shown in Fig. 11.9
[$C \cdot (A \cdot B + \overline{A} \cdot B)$; see Table 11.6, col. 4]

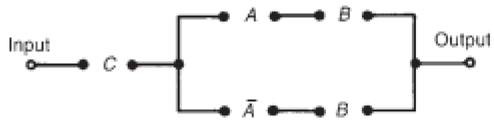


Figure 11.9

Table 11.6

1 A	2 B	3 C	4 $C \cdot (A \cdot B + \overline{A} \cdot B)$	5 $C \cdot (A \cdot \overline{B} + \overline{A})$
0	0	0	0	0
0	0	1	0	1
0	1	0	0	0
0	1	1	1	1
1	0	0	0	0
1	0	1	0	1
1	1	0	0	0
1	1	1	1	0

6 $A \cdot B(B \cdot \overline{C} + \overline{B} \cdot C + \overline{A} \cdot B)$	7 $C \cdot [B \cdot C \cdot \overline{A} + A \cdot (B + \overline{C})]$
0	0
0	0
0	0
0	1
0	0
0	0
1	0
0	1

2. The circuit shown in Fig. 11.10
[$C \cdot (A \cdot \overline{B} + \overline{A})$; see Table 11.6, col. 5]

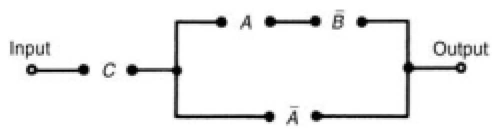


Figure 11.10

3. The circuit shown in Fig. 11.11

$$\left[\begin{array}{l} A \cdot B \cdot (B \cdot \overline{C} + \overline{B} \cdot C + \overline{A} \cdot B); \\ \text{see Table 11.6, col. 6} \end{array}\right]$$

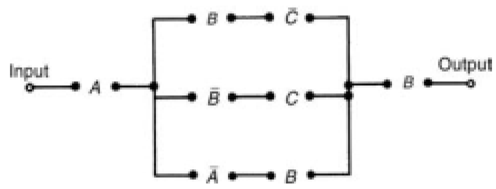


Figure 11.11

4. The circuit shown in Fig. 11.12

$$\left[\begin{array}{l} C \cdot [B \cdot C \cdot \overline{A} + A \cdot (B + \overline{C})], \\ \text{see Table 11.6, col. 7} \end{array}\right]$$

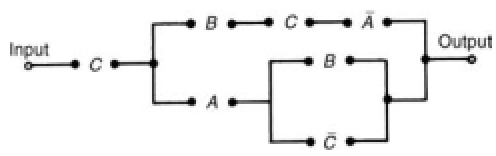


Figure 11.12

In Problems 5 to 7, construct switching circuits to meet the requirements of the Boolean expressions given.

5. $A \cdot C + A \cdot \overline{B} \cdot C + A \cdot B$

[See Fig. 11.13]

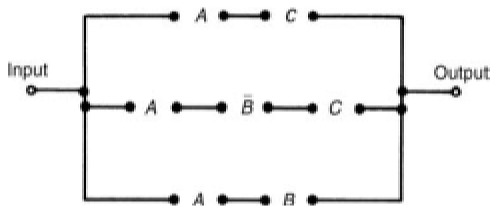


Figure 11.13

6. $A \cdot B \cdot C \cdot (A + B + C)$

[See Fig. 11.14]

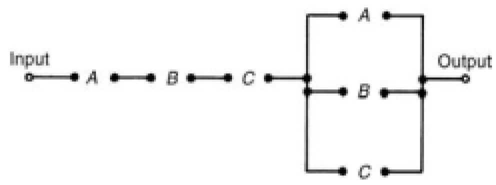


Figure 11.14

7. $A \cdot (A \cdot \overline{B} \cdot C + B \cdot (A + \overline{C}))$

[See Fig. 11.15]

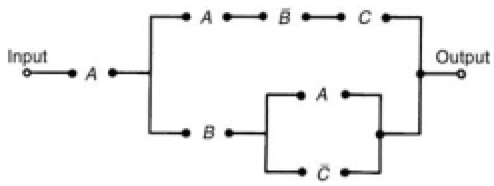


Figure 11.15

In Problems 8 to 10, derive the Boolean expressions and construct the switching circuits for the truth table stated.

8. Table 11.7, column 4

[$\overline{A} \cdot \overline{B} \cdot C + A \cdot B \cdot \overline{C}$; See Fig. 11.16]

Table 11.7

1 A	2 B	3 C	4	5	6
0	0	0	0	1	1
0	0	1	1	0	0
0	1	0	0	0	1
0	1	1	0	1	0
1	0	0	0	1	1
1	0	1	0	0	1
1	1	0	1	0	0
1	1	1	0	0	0

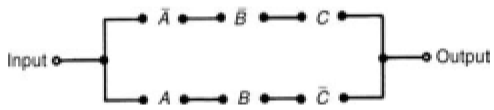


Figure 11.16

9. Table 11.7, column 5

$$\left[\begin{array}{l} \overline{A} \cdot \overline{B} \cdot \overline{C} + \overline{A} \cdot B \cdot C + A \cdot \overline{B} \cdot \overline{C}; \\ \text{see Fig. 11.17} \end{array}\right]$$

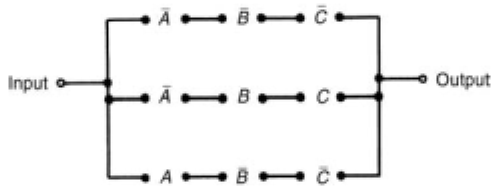


Figure 11.17

10. Table 11.7, column 6

$$\left[\begin{array}{l}\overline{A}\cdot\overline{B}\cdot\overline{C}+\overline{A}\cdot B\cdot\overline{C}+A\cdot\overline{B}\cdot\overline{C}\\ +A\cdot\overline{B}\cdot C;\text{ see Fig. 11.18}\end{array}\right]$$

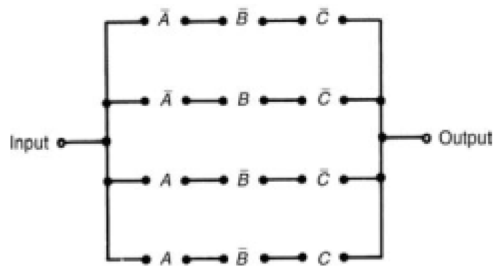


Figure 11.18

11.2 Simplifying Boolean expressions

A Boolean expression may be used to describe a complex switching circuit or logic system. If the Boolean expression can be simplified, then the number of switches or logic elements can be reduced resulting in a saving in cost. Three principal ways of simplifying Boolean expressions are:

(a) by using the laws and rules of Boolean algebra (see Section 11.3),
(b) by applying de Morgan's laws (see Section 11.4), and
(c) by using Karnaugh maps (see Section 11.5).

11.3 Laws and rules of Boolean algebra

A summary of the principal laws and rules of Boolean algebra are given in Table 11.8. The way in which these laws and rules may be used to simplify Boolean expressions is shown in Problems 5 to 10.

Table 11.8

Ref.	Name	Rule or law
1	Commutative laws	$A+B=B+A$
2		$A\cdot B=B\cdot A$
3	Associative laws	$(A+B)+C=A+(B+C)$
4		$(A\cdot B)\cdot C=A\cdot(B\cdot C)$
5	Distributive laws	$A\cdot(B+C)=A\cdot B+A\cdot C$
6		$A+(B\cdot C)=(A+B)\cdot(A+C)$
7	Sum rules	$A+0=A$
8		$A+1=1$
9		$A+A=A$
10		$A+\overline{A}=1$
11	Product rules	$A\cdot 0=0$
12		$A\cdot 1=A$
13		$A\cdot A=A$
14		$A\cdot\overline{A}=0$
15	Absorption rules	$A+A\cdot B=A$
16		$A\cdot(A+B)=A$
17		$A+\overline{A}\cdot B=A+B$

Problem 5. Simplify the Boolean expression: $\overline{P}\cdot\overline{Q}+\overline{P}\cdot Q+P\cdot\overline{Q}$

With reference to Table 11.8: *Reference*

$$\begin{array}{ll}\overline{P}\cdot\overline{Q}+\overline{P}\cdot Q+P\cdot\overline{Q} & \\ \quad=\overline{P}\cdot(\overline{Q}+Q)+P\cdot\overline{Q} & 5\\ \quad=\overline{P}\cdot 1+P\cdot\overline{Q} & 10\\ \quad=\boldsymbol{\overline{P}+P\cdot\overline{Q}} & 12\end{array}$$

Problem 6. Simplify $(P+\overline{P}\cdot Q)\cdot(Q+\overline{Q}\cdot P)$

With reference to Table 11.8: *Reference*

$$\begin{array}{ll}(P+\overline{P}\cdot Q)\cdot(Q+\overline{Q}\cdot P) & \\ \quad=P\cdot(Q+\overline{Q}\cdot P) & \\ \qquad+\overline{P}\cdot Q\cdot(Q+\overline{Q}\cdot P) & 5\\ \quad=P\cdot Q+P\cdot\overline{Q}\cdot P+\overline{P}\cdot Q\cdot Q & \\ \qquad+\overline{P}\cdot Q\cdot\overline{Q}\cdot P & 5\\ \quad=P\cdot Q+P\cdot\overline{Q}+\overline{P}\cdot Q & \\ \qquad+\overline{P}\cdot Q\cdot\overline{Q}\cdot P & 13\\ \quad=P\cdot Q+P\cdot\overline{Q}+\overline{P}\cdot Q+0 & 14\\ \quad=P\cdot Q+P\cdot\overline{Q}+\overline{P}\cdot Q & 7\\ \quad=P\cdot(Q+\overline{Q})+\overline{P}\cdot Q & 5\\ \quad=P\cdot 1+\overline{P}\cdot Q & 10\\ \quad=\boldsymbol{P+\overline{P}\cdot Q} & 12\end{array}$$

Problem 7. Simplify $F\cdot G\cdot\overline{H}+F\cdot G\cdot H+\overline{F}\cdot G\cdot H$

With reference to Table 11.8: *Reference*

$$\begin{aligned}
&F\cdot G\cdot\overline{H}+F\cdot G\cdot H+\overline{F}\cdot G\cdot H && \\
&\quad=F\cdot G\cdot(\overline{H}+H)+\overline{F}\cdot G\cdot H && 5\\
&\quad=F\cdot G\cdot 1+\overline{F}\cdot G\cdot H && 10\\
&\quad=F\cdot G+\overline{F}\cdot G\cdot H && 12\\
&\quad=\boldsymbol{G\cdot(F+\overline{F}\cdot H)} && 5
\end{aligned}$$

Problem 8. Simplify $\overline{F}\cdot\overline{G}\cdot H+\overline{F}\cdot G\cdot H+F\cdot\overline{G}\cdot H+F\cdot G\cdot H$

With reference to Table 11.8: *Reference*

$$\begin{aligned}
&\overline{F}\cdot\overline{G}\cdot H+\overline{F}\cdot G\cdot H+F\cdot\overline{G}\cdot H+F\cdot G\cdot H && \\
&\quad=\overline{G}\cdot H\cdot(\overline{F}+F)+G\cdot H\cdot(\overline{F}+F) && 5\\
&\quad=\overline{G}\cdot H\cdot 1+G\cdot H\cdot 1 && 10\\
&\quad=\overline{G}\cdot H+G\cdot H && 12\\
&\quad=H\cdot(\overline{G}+G) && 5\\
&\quad=H\cdot 1=\boldsymbol{H} && \text{10 and 12}
\end{aligned}$$

Problem 9. Simplify $A\cdot\overline{C}+\overline{A}\cdot(B+C)+A\cdot B\cdot(C+\overline{B})$ using the rules of Boolean algebra.

With reference to Table 11.8: *Reference*

$$\begin{aligned}
&A\cdot\overline{C}+\overline{A}\cdot(B+C)+A\cdot B\cdot(C+\overline{B}) && \\
&\quad=A\cdot\overline{C}+\overline{A}\cdot B+\overline{A}\cdot C+A\cdot B\cdot C && \\
&\qquad\qquad+A\cdot B\cdot\overline{B} && 5\\
&\quad=A\cdot\overline{C}+\overline{A}\cdot B+\overline{A}\cdot C+A\cdot B\cdot C && \\
&\qquad\qquad+A\cdot 0 && 14\\
&\quad=A\cdot\overline{C}+\overline{A}\cdot B+\overline{A}\cdot C+A\cdot B\cdot C && 11\\
&\quad=A\cdot(\overline{C}+B\cdot C)+\overline{A}\cdot B+\overline{A}\cdot C && 5\\
&\quad=A\cdot(\overline{C}+B)+\overline{A}\cdot B+\overline{A}\cdot C && 17\\
&\quad=A\cdot\overline{C}+A\cdot B+\overline{A}\cdot B+\overline{A}\cdot C && 5\\
&\quad=A\cdot\overline{C}+B\cdot(A+\overline{A})+\overline{A}\cdot C && 5\\
&\quad=A\cdot\overline{C}+B\cdot 1+\overline{A}\cdot C && 10\\
&\quad=\boldsymbol{A\cdot\overline{C}+B+\overline{A}\cdot C} && 12
\end{aligned}$$

Problem 10. Simplify the expression $P\cdot\overline{Q}\cdot R+P\cdot Q\cdot(\overline{P}+R)+Q\cdot R\cdot(\overline{Q}+P)$, using the rules of Boolean algebra.

With reference to Table 11.8: *Reference*

$$\begin{aligned}
&P\cdot\overline{Q}\cdot R+P\cdot Q\cdot(\overline{P}+R)+Q\cdot R\cdot(\overline{Q}+P) && \\
&\quad=P\cdot\overline{Q}\cdot R+P\cdot Q\cdot\overline{P}+P\cdot Q\cdot R && \\
&\qquad\qquad+Q\cdot R\cdot\overline{Q}+Q\cdot R\cdot P && 5\\
&\quad=P\cdot\overline{Q}\cdot R+0\cdot Q+P\cdot Q\cdot R+0\cdot R && \\
&\qquad\qquad+P\cdot Q\cdot R && 14\\
&\quad=P\cdot\overline{Q}\cdot R+P\cdot Q\cdot R+P\cdot Q\cdot R && \text{7 and 11}\\
&\quad=P\cdot\overline{Q}\cdot R+P\cdot Q\cdot R && 9\\
&\quad=P\cdot R\cdot(Q+\overline{Q}) && 5\\
&\quad=P\cdot R\cdot 1 && 10\\
&\quad=\boldsymbol{P\cdot R} && 12
\end{aligned}$$

Now try the following exercise.

Exercise 47 Further problems on the laws and the rules of Boolean algebra

Use the laws and rules of Boolean algebra given in Table 11.8 to simplify the following expressions:

1. $\overline{P}\cdot\overline{Q}+\overline{P}\cdot Q$ $[\overline{P}]$
2. $\overline{P}\cdot Q+P\cdot Q+\overline{P}\cdot\overline{Q}$ $[\overline{P}+P\cdot Q]$
3. $\overline{F}\cdot\overline{G}+F\cdot\overline{G}+\overline{G}\cdot(F+\overline{F})$ $[\overline{G}]$
4. $F\cdot\overline{G}+F\cdot(G+\overline{G})+F\cdot G$ $[F]$
5. $(P+P\cdot Q)\cdot(Q+Q\cdot P)$ $[P\cdot Q]$
6. $\overline{F}\cdot\overline{G}\cdot H+\overline{F}\cdot G\cdot H+F\cdot\overline{G}\cdot H$ $[H\cdot(\overline{F}+F\overline{G}]$
7. $F\cdot\overline{G}\cdot\overline{H}+F\cdot G\cdot H+\overline{F}\cdot G\cdot H$ $[F\cdot\overline{G}\cdot\overline{H}+G\cdot H]$
8. $\overline{P}\cdot\overline{Q}\cdot\overline{R}+\overline{P}\cdot Q\cdot R+P\cdot\overline{Q}\cdot\overline{R}$ $[\overline{Q}\cdot\overline{R}+\overline{P}\cdot Q\cdot R]$
9. $\overline{F}\cdot\overline{G}\cdot\overline{H}+\overline{F}\cdot\overline{G}\cdot H+F\cdot\overline{G}\cdot\overline{H}+F\cdot\overline{G}\cdot H$ $[\overline{G}]$
10. $F\cdot\overline{G}\cdot H+F\cdot G\cdot H+F\cdot G\cdot\overline{H}+\overline{F}\cdot G\cdot\overline{H}$ $[F\cdot H+G\cdot\overline{H}]$
11. $R\cdot(P\cdot Q+P\cdot\overline{Q})+\overline{R}\cdot(\overline{P}\cdot\overline{Q}+\overline{P}\cdot Q)$ $[P\cdot R+\overline{P}\cdot\overline{R}]$
12. $\overline{R}\cdot(\overline{P}\cdot\overline{Q}+P\cdot Q+P\cdot\overline{Q})+P\cdot(Q\cdot R+\overline{Q}\cdot R)$ $[P+\overline{Q}\cdot\overline{R}]$

11.4 De Morgan's laws

De Morgan's laws may be used to simplify **not**-functions having two or more elements. The laws state that:

$$\boxed{\overline{A+B}=\overline{A}\cdot\overline{B}} \quad \textbf{and} \quad \boxed{\overline{A\cdot B}=\overline{A}+\overline{B}}$$

and may be verified by using a truth table (see Problem 11). The application of de Morgan's laws in simplifying Boolean expressions is shown in Problems 12 and 13.

Problem 11. Verify that $\overline{A+B}=\overline{A}\cdot\overline{B}$

A Boolean expression may be verified by using a truth table. In Table 11.9, columns 1 and 2 give all the possible arrangements of the inputs A and B. Column 3 is the **or**-function applied to columns 1 and 2 and column 4 is the **not**-function applied to column 3. Columns 5 and 6 are the **not**-function applied to columns 1 and 2 respectively and column 7 is the **and**-function applied to columns 5 and 6.

Table 11.9

1	2	3	4	5	6	7
A	B	$A+B$	$\overline{A+B}$	$\overline{A}$	$\overline{B}$	$\overline{A}\cdot\overline{B}$
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

Since columns 4 and 7 have the same pattern of 0's and 1's this verifies that $\overline{A+B}=\overline{A}\cdot\overline{B}$.

Problem 12. Simplify the Boolean expression $(\overline{\overline{A}\cdot B})+(\overline{\overline{A}+B})$ by using de Morgan's laws and the rules of Boolean algebra.

Applying de Morgan's law to the first term gives:

$$\overline{\overline{A}\cdot B}=\overline{\overline{A}}+\overline{B}=A+\overline{B} \quad \text{since } \overline{\overline{A}}=A$$

Applying de Morgan's law to the second term gives:

$$\overline{\overline{A}+B}=\overline{\overline{A}}\cdot\overline{B}=A\cdot\overline{B}$$

Thus, $(\overline{\overline{A}\cdot B})+(\overline{\overline{A}+B})=(A+\overline{B})+A\cdot\overline{B}$

Removing the bracket and reordering gives: $A+A\cdot\overline{B}+\overline{B}$

But, by rule 15, Table 11.8, $A+A\cdot B=A$. It follows that: $A+A\cdot\overline{B}=A$

Thus: $\boldsymbol{(\overline{\overline{A}\cdot B})+(\overline{\overline{A}+B})=A+\overline{B}}$

Problem 13. Simplify the Boolean expression $(\overline{A\cdot\overline{B}+C})\cdot(\overline{A}+\overline{B\cdot\overline{C}})$ by using de Morgan's laws and the rules of Boolean algebra.

Applying de Morgan's laws to the first term gives:

$$\begin{aligned}\overline{A\cdot\overline{B}+C}&=\overline{A\cdot\overline{B}}\cdot\overline{C}=(\overline{A}+\overline{\overline{B}})\cdot\overline{C}\\&=(\overline{A}+B)\cdot\overline{C}=\overline{A}\cdot\overline{C}+B\cdot\overline{C}\end{aligned}$$

Applying de Morgan's law to the second term gives:

$$\overline{A}+\overline{B\cdot\overline{C}}=\overline{A}+(\overline{B}+\overline{\overline{C}})=\overline{A}+(\overline{B}+C)$$

Thus $(\overline{A\cdot\overline{B}+C})\cdot(\overline{A}+\overline{B\cdot\overline{C}})$

$$\begin{aligned}&=(\overline{A}\cdot\overline{C}+B\cdot\overline{C})\cdot(\overline{A}+\overline{B}+C)\\&=\overline{A}\cdot\overline{A}\cdot\overline{C}+\overline{A}\cdot\overline{B}\cdot\overline{C}+\overline{A}\cdot\overline{C}\cdot C\\&\quad+\overline{A}\cdot B\cdot\overline{C}+B\cdot\overline{B}\cdot\overline{C}+B\cdot\overline{C}\cdot C\end{aligned}$$

But from Table 11.8, $\overline{A}\cdot\overline{A}=\overline{A}$ and $\overline{C}\cdot C=B\cdot\overline{B}=0$

Hence the Boolean expression becomes:

$$\begin{aligned}&\overline{A}\cdot\overline{C}+\overline{A}\cdot\overline{B}\cdot\overline{C}+\overline{A}\cdot B\cdot\overline{C}\\&=\overline{A}\cdot\overline{C}(1+\overline{B}+B)\\&=\overline{A}\cdot\overline{C}(1+B)\\&=\overline{A}\cdot\overline{C}\end{aligned}$$

Thus: $\boldsymbol{(\overline{A\cdot\overline{B}+C})\cdot(\overline{A}+\overline{B\cdot\overline{C}})=\overline{A}\cdot\overline{C}}$

Now try the following exercise.

Exercise 48 Further problems on simplifying Boolean expressions using de Morgan's laws

Use de Morgan's laws and the rules of Boolean algebra given in Table 11.8 to simplify the following expressions.

1. $(\overline{A}\cdot\overline{B})\cdot(\overline{\overline{A}\cdot B})$ $[\overline{A}\cdot\overline{B}]$
2. $(\overline{A+\overline{B\cdot C}})+(\overline{A\cdot B}+C)$ $[\overline{A}+\overline{B}+C]$
3. $(\overline{\overline{A}\cdot B+B\cdot\overline{C}})\cdot\overline{A\cdot\overline{B}}$ $[\overline{A}\cdot\overline{B}+A\cdot B\cdot C]$
4. $(\overline{A\cdot\overline{B}}+\overline{B\cdot\overline{C}})+(\overline{\overline{A}\cdot B})$ $[1]$
5. $(\overline{P\cdot\overline{Q}}+\overline{\overline{P}\cdot R})\cdot(\overline{P}\cdot\overline{Q\cdot R})$ $[\overline{P}\cdot(\overline{Q}+\overline{R})]$

11.5 Karnaugh maps

(i) Two-variable Karnaugh maps

A truth table for a two-variable expression is shown in Table 11.10(a), the '1' in the third row output showing that $Z = A \cdot \overline{B}$. Each of the four possible Boolean expressions associated with a two-variable function can be depicted as shown in Table 11.10(b) in which one cell is allocated to each row of the truth table. A matrix similar to that shown in Table 11.10(b) can be used to depict $Z = A \cdot \overline{B}$, by putting a 1 in the cell corresponding to $A \cdot \overline{B}$ and 0's in the remaining cells. This method of depicting a Boolean expression is called a two-variable **Karnaugh map**, and is shown in Table 11.10(c).

Table 11.10

Inputs		Output	Boolean
A	B	Z	expression
0	0	0	$\overline{A} \cdot \overline{B}$
0	1	0	$\overline{A} \cdot B$
1	0	1	$A \cdot \overline{B}$
1	1	0	$A \cdot B$

(a)

B \ A	0 ($\overline{A}$)	1 (A)
0($\overline{B}$)	$\overline{A}.\overline{B}$	$A.\overline{B}$
1(B)	$\overline{A}.B$	A.B

(b)

B \ A	0	1
0	0	1
1	0	0

(c)

To simplify a two-variable Boolean expression, the Boolean expression is depicted on a Karnaugh map, as outlined above. Any cells on the map having either a common vertical side or a common horizontal side are grouped together to form a **couple**. (This is a coupling together of cells, not just combining two together). The simplified Boolean expression for a couple is given by those variables common to all cells in the couple. See Problem 14.

(ii) Three-variable Karnaugh maps

A truth table for a three-variable expression is shown in Table 11.11(a), the 1's in the output column showing that:

$$Z = \overline{A} \cdot \overline{B} \cdot C + \overline{A} \cdot B \cdot C + A \cdot B \cdot \overline{C}$$

Each of the eight possible Boolean expressions associated with a three-variable function can be depicted as shown in Table 11.11(b) in which one cell is allocated to each row of the truth table. A matrix similar to that shown in Table 11.11(b) can be used to depict: $Z = \overline{A} \cdot \overline{B} \cdot C + \overline{A} \cdot B \cdot C + A \cdot B \cdot \overline{C}$, by putting 1's in the cells corresponding to the Boolean terms on the right of the Boolean equation and 0's in the remaining cells. This method of depicting a three-variable Boolean expression is called a three-variable Karnaugh map, and is shown in Table 11.11(c).

Table 11.11

Inputs			Output	Boolean
A	B	C	Z	expression
0	0	0	0	$\overline{A} \cdot \overline{B} \cdot \overline{C}$
0	0	1	1	$\overline{A} \cdot \overline{B} \cdot C$
0	1	0	0	$\overline{A} \cdot B \cdot \overline{C}$
0	1	1	1	$\overline{A} \cdot B \cdot C$
1	0	0	0	$A \cdot \overline{B} \cdot \overline{C}$
1	0	1	0	$A \cdot \overline{B} \cdot C$
1	1	0	1	$A \cdot B \cdot \overline{C}$
1	1	1	0	$A \cdot B \cdot C$

(a)

C \ A.B	00 ($\overline{A}.\overline{B}$)	01 ($\overline{A}$.B)	11 (A.B)	10 (A.$\overline{B}$)
0($\overline{C}$)	$\overline{A}.\overline{B}.\overline{C}$	$\overline{A}.B.\overline{C}$	$A.B.\overline{C}$	$A.\overline{B}.\overline{C}$
1(C)	$\overline{A}.\overline{B}.C$	$\overline{A}.B.C$	A.B.C	$A.\overline{B}.C$

(b)

C \ A.B	00	01	11	10
0	0	0	1	0
1	1	1	0	0

(c)

To simplify a three-variable Boolean expression, the Boolean expression is depicted on a Karnaugh map as outlined above. Any cells on the map having common edges either vertically or horizontally are grouped together to form couples of four cells or two cells. During coupling the horizontal lines at the top and bottom of the cells are taken as a common edge, as are the vertical lines on the left and right of the cells. The simplified Boolean expression for a couple is given by those variables common to all cells in the couple. See Problems 15 to 17.

(iii) Four-variable Karnaugh maps

A truth table for a four-variable expression is shown in Table 11.12(a), the 1's in the output column showing that:

$$Z = \overline{A}\cdot\overline{B}\cdot C\cdot\overline{D}+\overline{A}\cdot B\cdot C\cdot\overline{D} \\ +A\cdot\overline{B}\cdot C\cdot\overline{D}+A\cdot B\cdot C\cdot\overline{D}$$

Each of the sixteen possible Boolean expressions associated with a four-variable function can be depicted as shown in Table 11.12(b), in which one cell is allocated to each row of the truth table. A matrix similar to that shown in Table 11.12(b) can be used to depict

$$Z = \overline{A}\cdot\overline{B}\cdot C\cdot\overline{D}+\overline{A}\cdot B\cdot C\cdot\overline{D} \\ +A\cdot\overline{B}\cdot C\cdot\overline{D}+A\cdot B\cdot C\cdot\overline{D}$$

by putting 1's in the cells corresponding to the Boolean terms on the right of the Boolean equation and 0's in the remaining cells. This method of depicting a four-variable expression is called a four-variable Karnaugh map, and is shown in Table 11.12(c).

To simplify a four-variable Boolean expression, the Boolean expression is depicted on a Karnaugh map as outlined above. Any cells on the map having common edges either vertically or horizontally are grouped together to form couples of eight cells, four cells or two cells. During coupling, the horizontal lines at the top and bottom of the cells may be considered to be common edges, as are the vertical lines on the left and the right of the cells. The simplified Boolean expression for a couple is given by those variables common to all cells in the couple. See Problems 18 and 19.

Table 11.12

Inputs				Output	Boolean
A	B	C	D	Z	expression
0	0	0	0	0	$\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}$
0	0	0	1	0	$\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot D$
0	0	1	0	1	$\overline{A}\cdot\overline{B}\cdot C\cdot\overline{D}$
0	0	1	1	0	$\overline{A}\cdot\overline{B}\cdot C\cdot D$
0	1	0	0	0	$\overline{A}\cdot B\cdot\overline{C}\cdot\overline{D}$
0	1	0	1	0	$\overline{A}\cdot B\cdot\overline{C}\cdot D$
0	1	1	0	1	$\overline{A}\cdot B\cdot C\cdot\overline{D}$
0	1	1	1	0	$\overline{A}\cdot B\cdot C\cdot D$
1	0	0	0	0	$A\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}$
1	0	0	1	0	$A\cdot\overline{B}\cdot\overline{C}\cdot D$
1	0	1	0	1	$A\cdot\overline{B}\cdot C\cdot\overline{D}$
1	0	1	1	0	$A\cdot\overline{B}\cdot C\cdot D$
1	1	0	0	0	$A\cdot B\cdot\overline{C}\cdot\overline{D}$
1	1	0	1	0	$A\cdot B\cdot\overline{C}\cdot D$
1	1	1	0	1	$A\cdot B\cdot C\cdot\overline{D}$
1	1	1	1	0	$A\cdot B\cdot C\cdot D$

(a)

C.D \ A.B	00 ($\overline{A}.\overline{B}$)	01 ($\overline{A}.B$)	11 ($A.B$)	10 ($A.\overline{B}$)
00 ($\overline{C}.\overline{D}$)	$\overline{A}.\overline{B}.\overline{C}.\overline{D}$	$\overline{A}.B.\overline{C}.\overline{D}$	$A.B.\overline{C}.\overline{D}$	$A.\overline{B}.\overline{C}.\overline{D}$
01 ($\overline{C}.D$)	$\overline{A}.\overline{B}.\overline{C}.D$	$\overline{A}.B.\overline{C}.D$	$A.B.\overline{C}.D$	$A.\overline{B}.\overline{C}.D$
11 ($C.D$)	$\overline{A}.\overline{B}.C.D$	$\overline{A}.B.C.D$	$A.B.C.D$	$A.\overline{B}.C.D$
10 ($C.\overline{D}$)	$\overline{A}.\overline{B}.C.\overline{D}$	$\overline{A}.B.C.\overline{D}$	$A.B.C.\overline{D}$	$A.\overline{B}.C.\overline{D}$

(b)

C.D \ A.B	0.0	0.1	1.1	1.0
0.0	0	0	0	0
0.1	0	0	0	0
1.1	0	0	0	0
1.0	1	1	1	1

(c)

Summary of procedure when simplifying a Boolean expression using a Karnaugh map

(a) Draw a four, eight or sixteen-cell matrix, depending on whether there are two, three or four variables.
(b) Mark in the Boolean expression by putting 1's in the appropriate cells.
(c) Form couples of 8, 4 or 2 cells having common edges, forming the largest groups of cells possible. (Note that a cell containing a 1 may be used more than once when forming a couple. Also note that each cell containing a 1 must be used at least once).
(d) The Boolean expression for the couple is given by the variables which are common to all cells in the couple.

Problem 14. Use the Karnaugh map techniques to simplify the expression $\overline{P}\cdot\overline{Q}+\overline{P}\cdot Q$

Using the above procedure:

(a) The two-variable matrix is drawn and is shown in Table 11.13.

Table 11.13

Q \ P	0	1
0	1	0
1	1	0

(b) The term $\overline{P}\cdot\overline{Q}$ is marked with a 1 in the top left-hand cell, corresponding to $P=0$ and $Q=0$; $\overline{P}\cdot Q$ is marked with a 1 in the bottom left-hand cell corresponding to $P=0$ and $Q=1$.

(c) The two cells containing 1's have a common horizontal edge and thus a vertical couple, can be formed.

(d) The variable common to both cells in the couple is $P=0$, i.e. $\overline{P}$ thus

$$\boldsymbol{\overline{P}\cdot\overline{Q}+\overline{P}\cdot Q=\overline{P}}$$

> Problem 15. Simplify the expression
> $\overline{X}\cdot Y\cdot\overline{Z}+\overline{X}\cdot\overline{Y}\cdot Z+X\cdot Y\cdot\overline{Z}+X\cdot\overline{Y}\cdot Z$
> by using Karnaugh map techniques.

Using the above procedure:

(a) A three-variable matrix is drawn and is shown in Table 11.14.

Table 11.14

Z \ X.Y	0.0	0.1	1.1	1.0
0	0	1	1	0
1	1	0	0	1

(b) The 1's on the matrix correspond to the expression given, i.e. for $\overline{X}\cdot Y\cdot\overline{Z}$, $X=0$, $Y=1$ and $Z=0$ and hence corresponds to the cell in the two row and second column, and so on.

(c) Two couples can be formed as shown. The couple in the bottom row may be formed since the vertical lines on the left and right of the cells are taken as a common edge.

(d) The variables common to the couple in the top row are $Y=1$ and $Z=0$, that is, $\boldsymbol{Y\cdot\overline{Z}}$ and the variables common to the couple in the bottom row are $Y=0$, $Z=1$, that is, $\boldsymbol{\overline{Y}\cdot Z}$. Hence:

$$\boldsymbol{\overline{X}\cdot Y\cdot\overline{Z}+\overline{X}\cdot\overline{Y}\cdot Z+X\cdot Y\cdot\overline{Z}+X\cdot\overline{Y}\cdot Z=Y\cdot\overline{Z}+\overline{Y}\cdot Z}$$

> Problem 16. Use a Karnaugh map technique to simplify the expression $(\overline{\overline{A}\cdot B})\cdot(\overline{\overline{A}+B})$.

Using the procedure, a two-variable matrix is drawn and is shown in Table 11.15.

Table 11.15

B \ A	0	1
0	1	1 2
1		1

$\overline{A}\cdot B$ corresponds to the bottom left-hand cell and $(\overline{\overline{A}\cdot B})$ must therefore be all cells except this one, marked with a 1 in Table 11.15. $(\overline{A}+B)$ corresponds to all the cells except the top right-hand cell marked with a 2 in Table 11.15. Hence $(\overline{\overline{A}+B})$ must correspond to the cell marked with a 2. The expression $(\overline{\overline{A}\cdot B})\cdot(\overline{\overline{A}+B})$ corresponds to the cell having both 1 and 2 in it, i.e.,

$$\boldsymbol{(\overline{\overline{A}\cdot B})\cdot(\overline{\overline{A}+B})=A\cdot\overline{B}}$$

> Problem 17. Simplify $(\overline{P+\overline{Q}\cdot R})+(\overline{P\cdot Q+\overline{R}})$ using a Karnaugh map technique.

The term $(P+\overline{Q}\cdot R)$ corresponds to the cells marked 1 on the matrix in Table 11.16(a), hence $(\overline{P+\overline{Q}\cdot R})$ corresponds to the cells marked 2. Similarly, $(P\cdot Q+\overline{R})$ corresponds to the cells marked 3 in Table 11.16(a), hence $(\overline{P\cdot Q+\overline{R}})$ corresponds to the cells marked 4. The expression $(\overline{P+\overline{Q}\cdot R})+(\overline{P\cdot Q+\overline{R}})$ corresponds to cells marked with either a 2 or with a 4 and is shown in Table 11.16(b) by X's. These cells may be coupled as shown. The variables common to the group of four cells is $P=0$, i.e., $\boldsymbol{\overline{P}}$, and those common to the group of two cells are $Q=0$, $R=1$, i.e. $\boldsymbol{\overline{Q}\cdot R}$

Thus: $(\overline{P+\overline{Q}\cdot R})+(\overline{P\cdot Q+\overline{R}})=\overline{P}+\overline{Q}\cdot R$

Table 11.16

(a)

R \ P.Q	0.0	0.1	1.1	1.0
0	3, 2	3, 2	3, 1	3, 1
1	4, 1	4, 2	3, 1	4, 1

(b)

R \ P.Q	0.0	0.1	1.1	1.0
0	X	X		
1	X	X		X

> Problem 18. Use Karnaugh map techniques to simplify the expression: $A\cdot B\cdot\overline{C}\cdot\overline{D}+A\cdot B\cdot C\cdot D+\overline{A}\cdot B\cdot C\cdot D+A\cdot B\cdot C\cdot\overline{D}+\overline{A}\cdot B\cdot C\cdot\overline{D}$.

Using the procedure, a four-variable matrix is drawn and is shown in Table 11.17. The 1's marked on the matrix correspond to the expression given. Two couples can be formed as shown. The four-cell couple has $B=1$, $C=1$, i.e. $\boldsymbol{B\cdot C}$ as the common variables to all four cells and the two-cell couple has $\boldsymbol{A\cdot B\cdot\overline{D}}$ as the common variables to both cells. Hence, the expression simplifies to:

$$\boldsymbol{B\cdot C+A\cdot B\cdot\overline{D}} \quad \text{i.e.} \quad \boldsymbol{B\cdot(C+A\cdot\overline{D})}$$

Table 11.17

C.D \ A.B	0.0	0.1	1.1	1.0
0.0			1	
0.1				
1.1		1	1	
1.0		1	1	

> Problem 19. Simplify the expression $\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}+A\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}+\overline{A}\cdot\overline{B}\cdot C\cdot\overline{D}+A\cdot\overline{B}\cdot C\cdot\overline{D}+A\cdot B\cdot C\cdot D$ by using Karnaugh map techniques.

The Karnaugh map for the expression is shown in Table 11.18. Since the top and bottom horizontal lines are common edges and the vertical lines on the left and right of the cells are common, then the four corner cells form a couple, $\overline{B}\cdot\overline{D}$ (the cells can be considered as if they are stretched to completely cover a sphere, as far as common edges are concerned). The cell $A\cdot B\cdot C\cdot D$ cannot be coupled with any other. Hence the expression simplifies to

$$\boldsymbol{\overline{B}\cdot\overline{D}+A\cdot B\cdot C\cdot D}$$

Table 11.18

C.D \ A.B	0.0	0.1	1.1	1.0
0.0	1			1
0.1				
1.1			1	
1.0	1			1

Now try the following exercise.

Exercise 49 Further problems on simplifying Boolean expressions using Karnaugh maps

In Problems 1 to 12 use Karnaugh map techniques to simplify the expressions given.

1. $\overline{X}\cdot Y+X\cdot Y$ $[Y]$
2. $\overline{X}\cdot\overline{Y}+\overline{X}\cdot Y+X\cdot Y$ $[\overline{X}+Y]$
3. $(\overline{P}\cdot\overline{Q})\cdot(\overline{\overline{P}\cdot Q})$ $[\overline{P}\cdot\overline{Q}]$
4. $A\cdot\overline{C}+\overline{A}\cdot(B+C)+A\cdot B\cdot(C+\overline{B})$ $[A\cdot\overline{C}+B+\overline{A}\cdot C]$
5. $\overline{P}\cdot\overline{Q}\cdot\overline{R}+\overline{P}\cdot Q\cdot\overline{R}+P\cdot Q\cdot\overline{R}$ $[\overline{R}\cdot(\overline{P}+Q)]$
6. $\overline{P}\cdot\overline{Q}\cdot\overline{R}+P\cdot Q\cdot\overline{R}+P\cdot Q\cdot R+P\cdot\overline{Q}\cdot R$ $[P\cdot(Q+R)+\overline{P}\cdot\overline{Q}\cdot\overline{R}]$
7. $\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}+\overline{A}\cdot B\cdot\overline{C}\cdot\overline{D}+\overline{A}\cdot B\cdot\overline{C}\cdot D$ $[\overline{A}\cdot\overline{C}\cdot(B+\overline{D})]$
8. $\overline{A}\cdot\overline{B}\cdot C\cdot D+\overline{A}\cdot\overline{B}\cdot C\cdot\overline{D}+A\cdot\overline{B}\cdot C\cdot\overline{D}$ $[\overline{B}\cdot C\cdot(\overline{A}+\overline{D})]$
9. $\overline{A}\cdot B\cdot\overline{C}\cdot D+A\cdot B\cdot\overline{C}\cdot D+A\cdot B\cdot C\cdot D+A\cdot\overline{B}\cdot\overline{C}\cdot D+A\cdot\overline{B}\cdot C\cdot D$ $[D\cdot(A+B\cdot\overline{C})]$

10. $\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot D+A\cdot B\cdot\overline{C}\cdot\overline{D}+A\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}+$
$A\cdot B\cdot C\cdot\overline{D}+A\cdot\overline{B}\cdot C\cdot\overline{D}$
$[A\cdot\overline{D}+\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot D]$

11. $A\cdot B\cdot\overline{C}\cdot\overline{D}+\overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}+\overline{A}\cdot B\cdot C\cdot D+$
$\overline{A}\cdot\overline{B}\cdot C\cdot D+A\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}+\overline{A}\cdot\overline{B}\cdot C\cdot\overline{D}+$
$\overline{A}\cdot B\cdot C\cdot\overline{D}$
$[\overline{A}\cdot C+A\cdot\overline{C}\cdot\overline{D}+\overline{B}\cdot\overline{D}\cdot(\overline{A}+\overline{C})]$

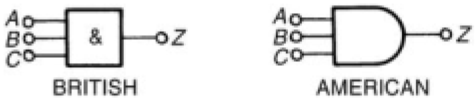
11.6 Logic circuits

In practice, logic gates are used to perform the **and, or** and **not**-functions introduced in Section 11.1. Logic gates can be made from switches, magnetic devices or fluidic devices, but most logic gates in use are electronic devices. Various logic gates are available. For example, the Boolean expression $(A\cdot B\cdot C)$ can be produced using a three-input, **and**-gate and $(C+D)$ by using a two-input **or**-gate. The principal gates in common use are introduced below. The term 'gate' is used in the same sense as a normal gate, the open state being indicated by a binary '1' and the closed state by a binary '0'. A gate will only open when the requirements of the gate are met and, for example, there will only be a '1' output on a two-input **and**-gate when both the inputs to the gate are at a '1' state.

The and-gate

The different symbols used for a three-input, **and**-gate are shown in Fig. 11.19(a) and the truth table is shown in Fig. 11.19(b). This shows that there will only be a '1' output when A is 1 and B is 1 and C is 1, written as:

$$Z=A\cdot B\cdot C$$



(a)

INPUTS A	B	C	OUTPUT $Z = A.B.C$
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

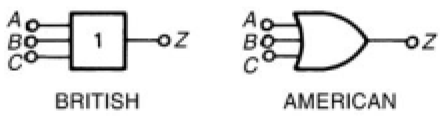
(b)

Figure 11.19

The or-gate

The different symbols used for a three-input **or**-gate are shown in Fig. 11.20(a) and the truth table is shown in Fig. 11.20(b). This shows that there will be a '1' output when A is 1, or B is 1, or C is 1, or any combination of A, B or C is 1, written as:

$$Z=A+B+C$$



(a)

INPUTS A	B	C	OUTPUT $Z=A+B+C$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

(b)

Figure 11.20

The invert-gate or not-gate

The different symbols used for an **invert**-gate are shown in Fig. 11.21(a) and the truth table is shown in Fig. 11.21(b). This shows that a '0' input gives a

'1' output and vice versa, i.e. it is an 'opposite to' function. The invert of A is written $\overline{A}$ and is called 'not-A'.

(a)

INPUT A	OUTPUT $Z=\overline{A}$
0	1
1	0

(b)

Figure 11.21

The nand-gate

The different symbols used for a **nand**-gate are shown in Fig. 11.22(a) and the truth table is shown in Fig. 11.22(b). This gate is equivalent to an **and**-gate and an **invert**-gate in series (not-and = nand) and the output is written as:

$$Z = \overline{A \cdot B \cdot C}$$

The nor-gate

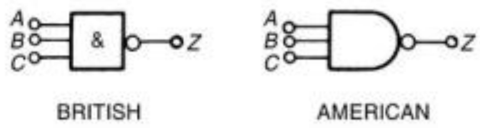
The different symbols used for a **nor**-gate are shown in Fig. 11.23(a) and the truth table is shown in Fig. 11.23(b). This gate is equivalent to an **or**-gate and an **invert**-gate in series, (not-or = nor), and the output is written as:

$$Z = \overline{A + B + C}$$

Combinational logic networks

In most logic circuits, more than one gate is needed to give the required output. Except for the **invert**-gate, logic gates generally have two, three or four inputs and are confined to one function only. Thus, for example, a two-input, **or**-gate or a four-input **and**-gate can be used when designing a logic circuit. The way in which logic gates are used to generate a given output is shown in Problems 20 to 23.

Problem 20. Devise a logic system to meet the requirements of: $Z = A \cdot \overline{B} + C$

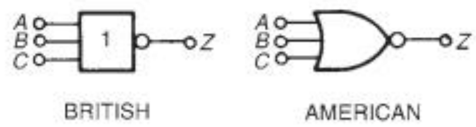


(a)

INPUTS A	B	C	$A.B.C.$	OUTPUT $Z=\overline{A.B.C.}$
0	0	0	0	1
0	0	1	0	1
0	1	0	0	1
0	1	1	0	1
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	0

(b)

Figure 11.22



(a)

INPUTS A	B	C	$A+B+C$	OUTPUT $Z=\overline{A+B+C}$
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	1	0
1	0	1	1	0
1	1	0	1	0
1	1	1	1	0

(b)

Figure 11.23

With reference to Fig. 11.24 an **invert**-gate, shown as (1), gives $\overline{B}$. The **and**-gate, shown as (2), has inputs of A and $\overline{B}$, giving $A \cdot \overline{B}$. The **or**-gate, shown as (3), has inputs of $A \cdot \overline{B}$ and C, giving:

$$\boldsymbol{Z = A \cdot \overline{B} + C}$$

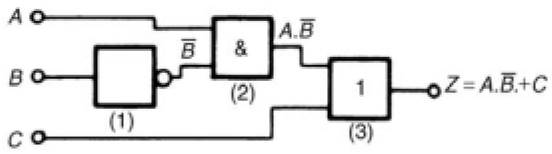


Figure 11.24

Problem 21. Devise a logic system to meet the requirements of $(P + \overline{Q}) \cdot (\overline{R} + S)$.

The logic system is shown in Fig. 11.25. The given expression shows that two **invert**-functions are needed to give $\overline{Q}$ and $\overline{R}$ and these are shown as gates (1) and (2). Two **or**-gates, shown as (3) and (4), give $(P + \overline{Q})$ and $(\overline{R} + S)$ respectively. Finally, an **and**-gate, shown as (5), gives the required output,

$$\boldsymbol{Z = (P + \overline{Q}) \cdot (\overline{R} + S)}$$

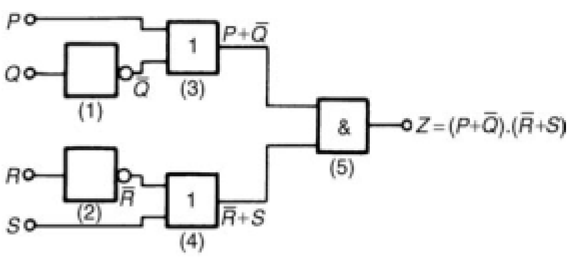


Figure 11.25

Problem 22. Devise a logic circuit to meet the requirements of the output given in Table 11.19, using as few gates as possible.

Table 11.19

Inputs			Output
A	B	C	Z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

The '1' outputs in rows 6, 7 and 8 of Table 11.19 show that the Boolean expression is:

$$Z = A \cdot \overline{B} \cdot C + A \cdot B \cdot \overline{C} + A \cdot B \cdot C$$

The logic circuit for this expression can be built using three, 3-input **and**-gates and one, 3-input **or**-gate, together with two **invert**-gates. However, the number of gates required can be reduced by using the techniques introduced in Sections 11.3 to 11.5, resulting in the cost of the circuit being reduced. Any of the techniques can be used, and in this case, the rules of Boolean algebra (see Table 11.8) are used.

$$\begin{aligned} Z &= A \cdot \overline{B} \cdot C + A \cdot B \cdot \overline{C} + A \cdot B \cdot C \\ &= A \cdot [\overline{B} \cdot C + B \cdot \overline{C} + B \cdot C] \\ &= A \cdot [\overline{B} \cdot C + B(\overline{C} + C)] = A \cdot [\overline{B} \cdot C + B] \\ &= A \cdot [B + \overline{B} \cdot C] = \boldsymbol{A \cdot [B + C]} \end{aligned}$$

The logic circuit to give this simplified expression is shown in Fig. 11.26.

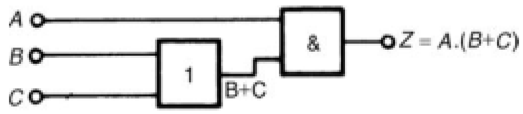


Figure 11.26

Problem 23. Simplify the expression:

$$Z = \overline{P} \cdot \overline{Q} \cdot \overline{R} \cdot \overline{S} + \overline{P} \cdot \overline{Q} \cdot \overline{R} \cdot S + \overline{P} \cdot Q \cdot \overline{R} \cdot \overline{S} + \overline{P} \cdot Q \cdot \overline{R} \cdot S + P \cdot \overline{Q} \cdot \overline{R} \cdot \overline{S}$$

and devise a logic circuit to give this output.

The given expression is simplified using the Karnaugh map techniques introduced in Section 11.5. Two couples are formed as shown in Fig. 11.27(a) and the simplified expression becomes:

$$Z = \overline{Q} \cdot \overline{R} \cdot \overline{S} + \overline{P} \cdot \overline{R}$$

i.e $\boldsymbol{Z = \overline{R} \cdot (\overline{P} + \overline{Q} \cdot \overline{S})}$

The logic circuit to produce this expression is shown in Fig. 11.27(b).

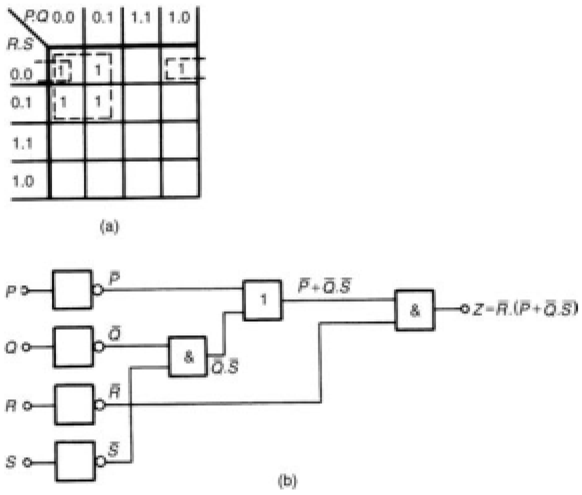


Figure 11.27

Now try the following exercise.

Exercise 50 Further problems on logic circuits

In Problems 1 to 4, devise logic systems to meet the requirements of the Boolean expressions given.

1. $Z=\overline{A}+B\cdot C$ [See Fig. 11.28(a)]
2. $Z=A\cdot\overline{B}+B\cdot\overline{C}$ [See Fig. 11.28(b)]
3. $Z=A\cdot B\cdot\overline{C}+\overline{A}\cdot\overline{B}\cdot C$ [See Fig. 11.28(c)]
4. $Z=(\overline{A}+B)\cdot(\overline{C}+D)$ [See Fig. 11.28(d)]

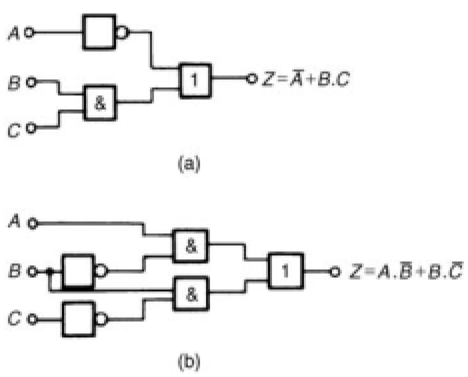


Figure 11.28

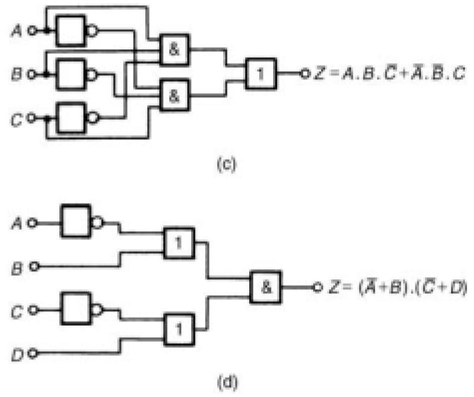


Figure 11.28 *Continued*

In Problems 5 to 7, simplify the expression given in the truth table and devise a logic circuit to meet the requirements stated.

5. Column 4 of Table 11.20 [$Z_1=A\cdot B+C$, see Fig. 11.29(a)]
6. Column 5 of Table 11.20 [$Z_2=A\cdot\overline{B}+B\cdot C$, see Fig. 11.29(b)]

Table 11.20

1	2	3	4	5	6
A	B	C	Z_1	Z_2	Z_3
0	0	0	0	0	0
0	0	1	1	0	0
0	1	0	0	0	1
0	1	1	1	1	1
1	0	0	0	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	1	1

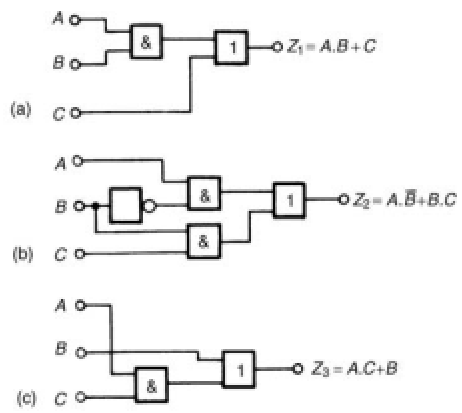


Figure 11.29

7. Column 6 of Table 11.20

[$Z_3 = A \cdot C + B$, see Fig. 11.29(c)]

In Problems 8 to 12, simplify the Boolean expressions given and devise logic circuits to give the requirements of the simplified expressions.

8. $\overline{P} \cdot \overline{Q} + \overline{P} \cdot Q + P \cdot Q$

[$\overline{P} + Q$, see Fig. 11.30(a)]

9. $\overline{P} \cdot \overline{Q} \cdot \overline{R} + P \cdot Q \cdot \overline{R} + P \cdot \overline{Q} \cdot \overline{R}$

[$\overline{R} \cdot (P + \overline{Q})$, see Fig. 11.30(b)]

10. $P \cdot \overline{Q} \cdot R + P \cdot \overline{Q} \cdot \overline{R} + \overline{P} \cdot \overline{Q} \cdot \overline{R}$

[$\overline{Q} \cdot (P + \overline{R})$, see Fig. 11.30(c)]

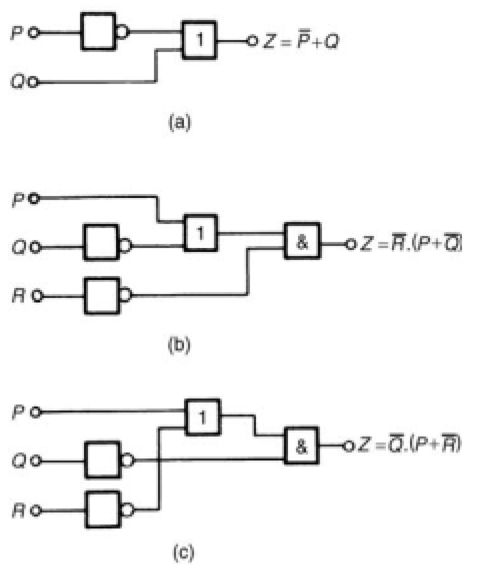


Figure 11.30

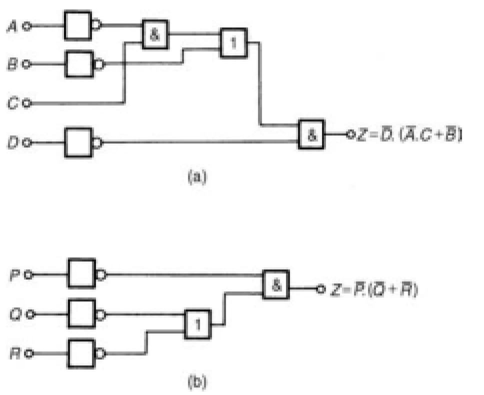


Figure 11.31

11. $\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} + A \cdot \overline{B} \cdot \overline{C} \cdot \overline{D} + \overline{A} \cdot \overline{B} \cdot C \cdot \overline{D} +$
$\overline{A} \cdot B \cdot C \cdot \overline{D} + A \cdot \overline{B} \cdot C \cdot \overline{D}$

[$\overline{D} \cdot (\overline{A} \cdot C + \overline{B})$, see Fig. 11.31(a)]

12. $\overline{(\overline{P} \cdot Q \cdot R)} \cdot \overline{(P + Q \cdot R)}$

[$\overline{P} \cdot (\overline{Q} + \overline{R})$ see Fig. 11.31(b)]

11.7 Universal logic gates

The function of any of the five logic gates in common use can be obtained by using either **nand**-gates or **nor**-gates and when used in this manner, the gate selected in called a **universal gate.** The way in which a universal **nand**-gate is used to produce the **invert, and, or** and **nor**-functions is shown in Problem 24. The way in which a universal **nor**-gate is used to produce the **invert, or, and** and **nand**-functions is shown in Problem 25.

Problem 24. Show how **invert, and, or** and **nor**-functions can be produced using nand-gates only.

A single input to a **nand**-gate gives the **invert**-function, as shown in Fig. 11.32(a). When two **nand**-gates are connected, as shown in Fig. 11.32(b), the output from the first gate is $\overline{A \cdot B \cdot C}$ and this is inverted by the second gate, giving $Z = \overline{\overline{A \cdot B \cdot C}} = A \cdot B \cdot C$ i.e. the **and**-function is produced. When $\overline{A}$, $\overline{B}$ and $\overline{C}$ are the inputs to a **nand**-gate, the output is $\overline{\overline{A} \cdot \overline{B} \cdot \overline{C}}$.

By de Morgan's law, $\overline{\overline{A} \cdot \overline{B} \cdot \overline{C}} = \overline{\overline{A}} + \overline{\overline{B}} + \overline{\overline{C}} = A + B + C$, i.e. a **nand**-gate is used to produce the **or**-function. The logic circuit is shown in Fig. 11.32(c). If the output from the logic circuit in Fig. 11.32(c) is inverted by adding an additional **nand**-gate, the output becomes the invert of an **or**-function, i.e. the **nor**-function, as shown in Fig. 11.32(d).

Problem 25. Show how **invert, or, and** and **nand**-functions can be produced by using **nor**-gates only.

A single input to a **nor**-gate gives the **invert**-function, as shown in Fig. 11.33(a). When two **nor**-gates are connected, as shown in Fig. 11.33(b), the output from the first gate is $\overline{A + B + C}$ and this is inverted by the second gate, giving $Z = \overline{\overline{A + B + C}} = A + B + C$, i.e. the **or**-function is

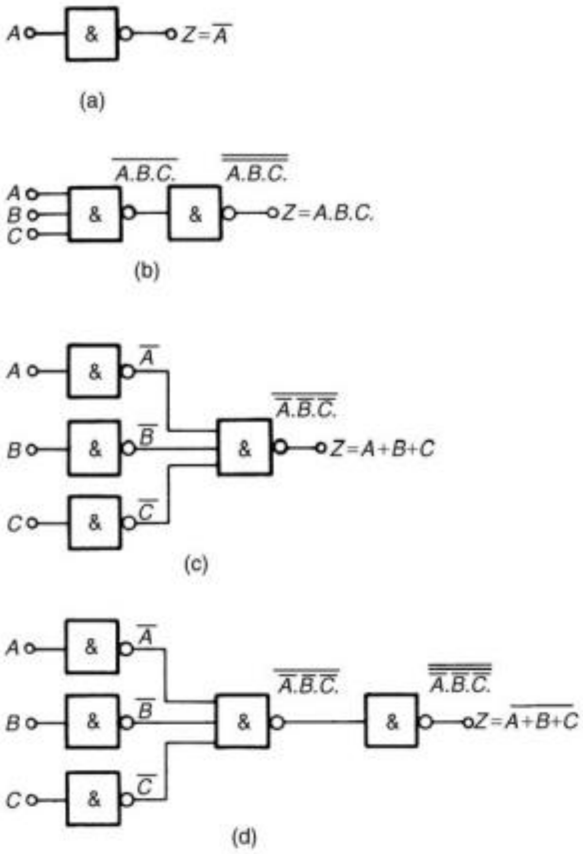


Figure 11.32

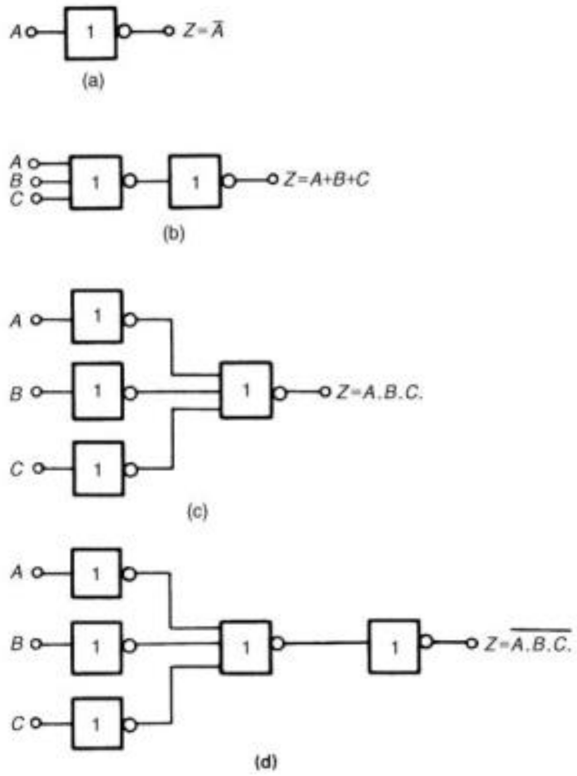


Figure 11.33

produced. Inputs of $\overline{A}$, $\overline{B}$, and $\overline{C}$ to a **nor**-gate give an output of $\overline{\overline{A}+\overline{B}+\overline{C}}$.

By de Morgan's law, $\overline{\overline{A}+\overline{B}+\overline{C}}=\overline{\overline{A}}\cdot\overline{\overline{B}}\cdot\overline{\overline{C}}=A\cdot B\cdot C$, i.e. the **nor**-gate can be used to produce the **and**-function. The logic circuit is shown in Fig. 11.33(c). When the output of the logic circuit, shown in Fig. 11.33(c), is inverted by adding an additional **nor**-gate, the output then becomes the invert of an **or**-function, i.e. the **nor**-function as shown in Fig. 11.33(d).

> Problem 26. Design a logic circuit, using **nand**-gates having not more than three inputs, to meet the requirements of the Boolean expression
>
> $$Z=\overline{A}+\overline{B}+C+\overline{D}$$

When designing logic circuits, it is often easier to start at the output of the circuit. The given expression shows there are four variables joined by **or**-functions. From the principles introduced in Problem 24, if a four-input **nand**-gate is used to give the expression given, the inputs are $\overline{\overline{A}}$, $\overline{\overline{B}}$, $\overline{C}$ and $\overline{\overline{D}}$ that is A, B, $\overline{C}$ and D. However, the problem states that three-inputs are not to be exceeded so two of the variables are joined, i.e. the inputs to the three-input **nand**-gate, shown as gate (1) in Fig. 11.34, is A, B, $\overline{C}$ and D. From Problem 24, the **and**-function is generated by using two **nand**-gates connected in series, as shown by gates (2) and (3) in Fig. 11.34. The logic circuit required to produce the given expression is as shown in Fig. 11.34.

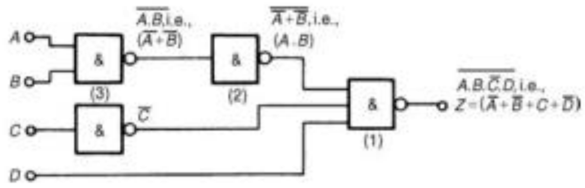


Figure 11.34

Problem 27. Use **nor**-gates only to design a logic circuit to meet the requirements of the expression: $Z = \overline{D} \cdot (\overline{A} + B + \overline{C})$

It is usual in logic circuit design to start the design at the output. From Problem 25, the **and**-function between $\overline{D}$ and the terms in the bracket can be produced by using inputs of $\overline{\overline{D}}$ and $\overline{\overline{A} + B + \overline{C}}$ to a **nor**-gate, i.e. by de Morgan's law, inputs of D and $A \cdot \overline{B} \cdot C$. Again, with reference to Problem 25, inputs of $\overline{A} \cdot B$ and $\overline{C}$ to a **nor**-gate give an output of $\overline{\overline{A} + B + \overline{C}}$, which by de Morgan's law is $A \cdot \overline{B} \cdot C$. The logic circuit to produce the required expression is as shown in Fig. 11.35.

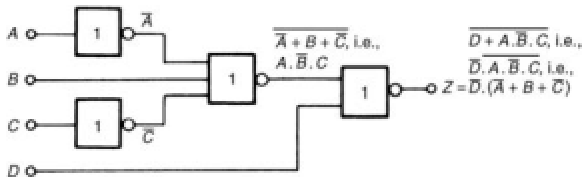


Figure 11.35

Problem 28. An alarm indicator in a grinding mill complex should be activated if (a) the power supply to all mills is off and (b) the hopper feeding the mills is less than 10% full, and (c) if less than two of the three grinding mills are in action. Devise a logic system to meet these requirements.

Let variable A represent the power supply on to all the mills, then $\overline{A}$ represents the power supply off. Let B represent the hopper feeding the mills being more than 10% full, then $\overline{B}$ represents the hopper being less than 10% full. Let C, D and E represent the three mills respectively being in action, then $\overline{C}, \overline{D}$ and $\overline{E}$ represent the three mills respectively not being in action. The required expression to activate the alarm is:

$$Z = \overline{A} \cdot \overline{B} \cdot (\overline{C} + \overline{D} + \overline{E})$$

There are three variables joined by **and**-functions in the output, indicating that a three-input **and**-gate is required, having inputs of $\overline{A}, \overline{B}$ and $(\overline{C} + \overline{D} + \overline{E})$. The term $(\overline{C} + \overline{D} + \overline{E})$ is produce by a three-input **nand**-gate. When variables C, D and E are the inputs to a **nand**-gate, the output is $\overline{C \cdot D \cdot E}$ which, by de Morgan's law is $\overline{C} + \overline{D} + \overline{E}$. Hence the required logic circuit is as shown in Fig. 11.36.

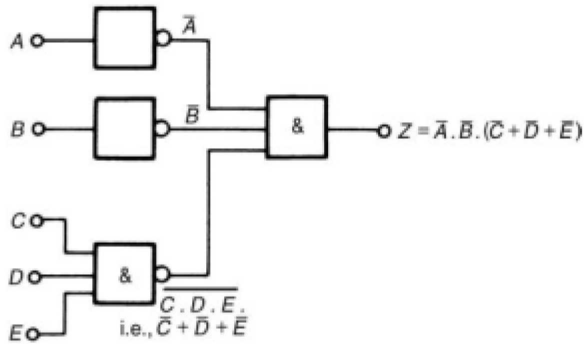


Figure 11.36

Now try the following exercise.

Exercise 51 Further problems on universal logic gates

In Problems 1 to 3, use **nand**-gates only to devise the logic systems stated.

1. $Z = A + B \cdot C$ [See Fig. 11.37(a)]

2. $Z = A \cdot \overline{B} + B \cdot \overline{C}$ [See Fig. 11.37(b)]

3. $Z = A \cdot B \cdot \overline{C} + \overline{A} \cdot \overline{B} \cdot C$ [See Fig. 11.37(c)]

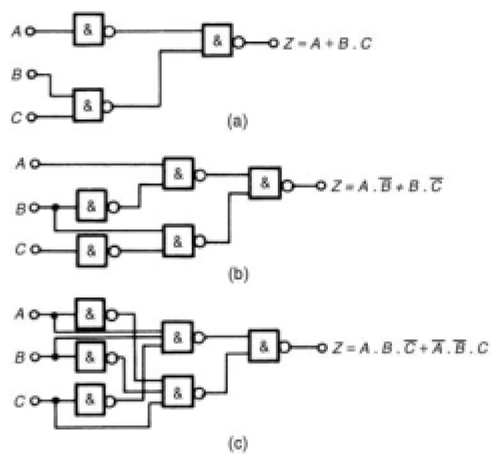


Figure 11.37

In Problems 4 to 6, use **nor**-gates only to devise the logic systems stated.

4. $Z=(\overline{A}+B)\cdot(\overline{C}+D)$

[see Fig. 11.38(a)]

5. $Z=A\cdot\overline{B}+B\cdot\overline{C}+C\cdot\overline{D}$

[see Fig. 11.38(b)]

6. $Z=\overline{P}\cdot Q+P\cdot(Q+R)$

[see Fig. 11.38(c)]

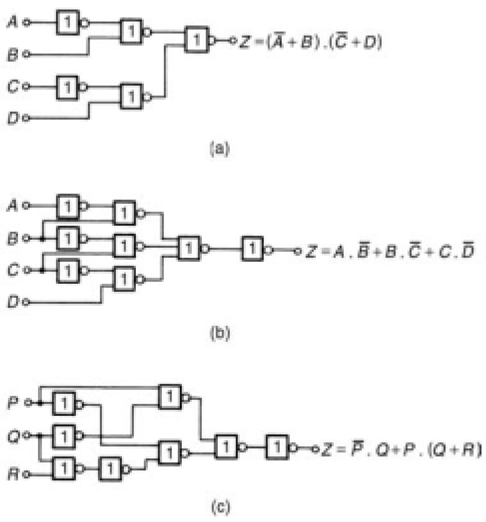


Figure 11.38

7. In a chemical process, three of the transducers used are P, Q and R, giving output signals of either 0 or 1. Devise a logic system to give a 1 output when:

   (a) P and Q and R all have 0 outputs, or when:

   (b) P is 0 and (Q is 1 or R is 0)

   [$\overline{P}\cdot(Q+\overline{R})$, see Fig. 11.39(a)]

8. Lift doors should close, (Z), if:

   (a) the master switch, (A), is on and either

   (b) a call, (B), is received from any other floor, or

   (c) the doors, (C), have been open for more than 10 seconds, or

   (d) the selector push within the lift (D), is pressed for another floor.

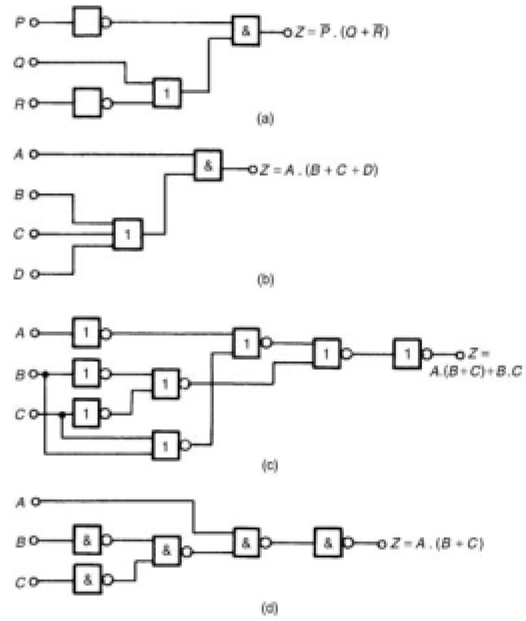


Figure 11.39

Devise a logic circuit to meet these requirements.

$$\begin{bmatrix} Z=A\cdot(B+C+D), \\ \text{see Fig. 11.39(b)} \end{bmatrix}$$

9. A water tank feeds three separate processes. When any two of the processes are in operation at the same time, a signal is required to start a pump to maintain the head of water in the tank. Devise a logic circuit using **nor**-gates only to give the required signal.

$$\begin{bmatrix} Z=A\cdot(B+C)+B\cdot C, \\ \text{see Fig. 11.39(c)} \end{bmatrix}$$

10. A logic signal is required to give an indication when:

   (a) the supply to an oven is on, and
   (b) the temperature of the oven exceeds 210°C, or
   (c) the temperature of the oven is less than 190°C

   Devise a logic circuit using **nand**-gates only to meet these requirements.

   [$Z=A\cdot(B+C)$, see Fig. 11.39(d)]