달력정보

달력
양음력변환

오늘 < 2025.03 .
전역일계산

>
음력 손없는날
기념일

오전 1시간

일
월
화
수
목
금
토

23
24
25
26
27
28
1

오늘

삼일절

2
3
4
5
6
7
8

대체 휴일

납세자의 날

따라기 .

교재 국제

국제 여성...

13.8 민주의...

ALU： Adder FND

9
10
11
12
13
14
음 2.151.5

16
17

23
24

국제 강아...

sTop_watch

31547454

315의거

18
19
20
21
22

상공의 날

UART. +FIFO. 레지스터

25

춘분) 국제 행복...

암예방의 날 세계 물의...

발표(mini). 각조 1명

bus Io Interface

26
27
28
29
음 3.1

서해수호...

센서제어 . UART- FIFO.

project.

30
31
2
3
4
5

발표 모두

1

┌

File
Edit Flow
Tools
Repo

PROJECT MANAGER - 250227_gates

Flow Navigator

PROJECT MANAGER

Settings

Add Sources

Language Templates

IP Catalog

v
IP INTEGRATOR

Create Block Design

Open Block Design

Generate Block Design
?

Sources

Q+

V Design Sources

Constraints

Simulation Sources

sim_1

Utility Sources

Verilog

SIMULATION

Run Simulation

RTL ANALYSIS

> Open Elaborated Design

v
SYNTHESIS

Run Synthesis

> Open Synthesized Design

IMPLEMENTATION

Run Implementation

> Open Implemented Design

PROGRAM AND DEBUG

Generate Bitstream

> Open Hardware Manager

Hierarchy

Libraries

Compile Order

Add Sources

VIVADO.

HLX Editions

Σ XILINX

?

? _ D E X

Add Sources

Add or Create Design Sources

Specify HDL, netlist, Block Design, and IP files, or and add it to your project.

Create Source File

+

↑

?
Scan and add RTL include files into project

Copy sources into project

Add sources from subdirectories

Add Sources
Create a new source file and add it to your project.

File type:
Verilog
<

File name:

File location:
<Local to Project>

?
OK
Cancel

Add Files
Add Directories
Create File
X Create a new source file on disk

< Back
Next >
Finish
Cancel

Add Sources

This guides you through the process of adding and creating sources for your project

Add or create constraints

Add or create design sources

Add or create simulation sources

Add or Create Design Sources

Specify HDL, netlist, Block Design, and IP files, or directories containing those file types to add to your project. Create a new source file on disk and add it to your project.

+

Index
Name

1
Library

gates.v xil_defaultlib
<Local to Project>
Location

< Back
Next >
Finish
Cancel
Scan and add RTL include files into project

Copy sources into project

Add sources from subdirectories
Add Files
Add Directories
Create File
X

< Back

Next >
Finish
Cancel
X

Top

Sources

Source 추가 .

Q+
=(+

Design Sources (1)

gates (gates.v)

› Constraints module

Simulation Sources (1)

sim_1 (1)

Utility Sources

0

Hierarchy Libraries Compile Order

? - □□ x

Top 21 3/23/

기준전

module

-동작시간 단위

2

->1 `timescale insp

해석단위

시작3 **module** gates(

10-9

lons/ps

10-2

77

+ng

4

5

_6 **endmodule**

-6

M

o

m

1

10-3

```
1 timescale 1ns/1ps
2
이름
3
module gates

5 endmodule
Que
맺음.
```

a

b

Top

module

AND

'Kill to

출력

AND

ŏ

10

?) 입력

6

"

OR

2127/

と

출력

3. module gates // top

module

input a

input b

1

output you

output y1,

입력

"

output y2,

출력

WAND

output y3,

Y2

EXOR

10

output y4,

list

11

output y5X

XOR NOT

12

-Y3

13

1

ว

1

14 **endmodule**

WOR

Y4

NOT.

Y5

Input

Tuputa

فا

& Ouput

wire

default

assign yoab

input wire a

연결

연결해라

NOT

항상

바트

Input a

!: 논리값 거짓.

변수 32bit

olll

Flow Navigator

PROJECT MANAGER
?
ELABORATED DESIGN - xc7a35tcpg236-1
? >

Source N x ?
Project Summary × **Schematic**
? □ G

K
+C 6 Cells
8 I/O Ports
8 Nets
IP INTEGRATOR

Create Block Design
R gates

> Nets (8)
Open Block Design

Generate Block Design

✓ SIMULATION

Run Simulation

RTL ANALYSIS

Open Elaborated Design

Report Methodology

Report DRC
> Leaf Cells (6)

Report Noise
Sourc
? - OG X
Schematic
gates.v

SYNTHESIS

Enabled

Run Synthesis
Location:
C:/Wol

› Open Synthesized Design
Type:
Verilog

Library:
xil_defi

✓ IMPLEMENTATION

Size:
0.4 KB

Run Implementation

› Open Implemented Design
General
Properties

L

O

10_yo_i
a
11
yo
O
y2_i
10
y2

RIL INV3
RTL AND

10 *y1*

|1

RTL OR
10 y3_i

○
|1
y3

RTL XOR

y1

y4_1

y4

RTL INV

y5_i
10
○
y5

RTL INV

1

14

+5V

UCC
&u
&

&
&

7400

SN 7400N

7645

The SN7400N chip contains

Q
GND

8

gates (Topmode

wire

Run Simulation

RTL ANALYSIS

✓ **Open Elaborated Design**

Report Methodology

Report DRC

Launch Runs

Launch the selected synthesis or implementation runs.

X

Launch directory: <Default Launch Directory>

Options

Report Noise

Sourc

? _ [EX

Schematic

gates.v

Launch runs on local host: Number of jobs: 16

Generate scripts only

SYNTHESIS
Enabled

‣ Run Synthesis
Don't show this dialog again
Location:
C:/Wol

> Open Synthesized Design
OK
Cancel
Type:
Veriloc

Library:
xil_def
• IMPLEMENTATION

cup 갯수

pe

10
yo

y2_i

y2

RTL_INV

10
y3_i

11

Dy3

동작중 .

Running synth_design Cancel

Default Layout

? X

? □ K

1
16
15

отна

14
13

IC1

2

ADIGILENT

w.digilentinc.com

3

UGA

FED

RGB motor

LOIS

1426

10031-17-6820

DOBEN 100TING

5536

5188

3009

8148

CLKIDOPHE

LINEAR BORED

8. 8:8.8.

LO13

CLAS

LOW

LOP

1231

77T4

22

11

10

9

CPLP)

C9101

9102

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24

& XILINX

UNIVERSI PROGRAM

8

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Bush

BTO

xilinx

RAM

FPGA) RANO.1

191

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bitstream

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0011

9-Seg

5

FOD

SW

Callout Component Description
BASYS 3

Figure 1. Easys3 board features
26
THO

CLT SO
6C191
6

Callout	Component Description
1	FPGA configuration reset button
2	Pmod connector(s)
3	Analog signal Pmod connector (XADC)
4	Four digit 7-segment display
6	LEDs (16)
9	Power good LED
10	Programming mode jumper
11	USB host connector
12	VGA connector
13	Shared UART/JTAG USB port
14	External power connector

Slide switches (16)

78

Pushbuttons (5)

15

`Power` Switch

FPGA programming done LED

16

`Power Select` Jumper

台

GND `to`

Yo

YK

Y5

Input/output

64

AB

열

しいいいい

2000000

300

دوست امیر آباد شد

in

wW19-U16 LDO

E19 LD1

w-T17 U19 LD2

2

3.3V

BTNL

BTNR

Buttons

w-T18

BTNU

Y4

w-U17

Y5

BTND

w-U18

BTNC

V19 LD3

LD4

LEDs

-W18. ww U15 LD5

LD6 U14 ww

V14 LD7 **WW** *V13* LD8

V3 LD9

w

W3 LD10 ww

Artix-7 U3 LD11

ww

2/22

a

b

Project Summary
X Schematic x

• XN

click

6 Cells
8 I/O Ports
8 Nets

rrrl

?
⊔ ⊔
>
C

Λ

Λ
>
F
F
F

Fixed
Bank I/O Std
Vcco

14 LVCMOS33
3.300

14 LVCMOS33*
3.300
>
14 LVCMOS33*
3.300

v
14 LVCMOS33*
3.300
>
>
14 LVCMOS33*
3.300

14 LVCMOS33*
3.300

14
LVCMOS33*
3.300
>
14 LVCMOS33*
3.300
3.3V

SW1

a

b

CPG 266

Constraints

SWOW V17

P3 LD12 w N3 LD13 P1 LD14 L1_LD15

10

11
yo_i
yo

y2_i

b
RTL AND
10
y2

RTL_INV

Tcl Console Messages
Messages Log **Reports Design Runs Find Results** x

C

Name Direction
Board Part Pin Board Part Interface Interface Neg Diff Pair Package Pin
Fixed Bank I/0 Std

wV16

IN
default (LVCMOS18)
Vcco

1.800
Vref Drive Strength
Slew Type
Pull Type

IN
default (LVCMOS18)
1.800
NONE

NONE

yo OUT
>
default (LVCMOS18)

y1 OUT
default (LVCMOS18)
1.800

1.800
12

12
NONE

NONE

ОЛЬ

y2 OUT

Tcl Console Messages
Log
Reports

y3 OUT

y4 OUT
^1
Direction
Board Part ...
y5 OUT
a
IN

b
IN
NN

yo
OUT

y1 OUT

y2 OUT

y3
OUT

y4
OUT

y5 OUT
Board Part Int... Interface Neg Diff Pair Package Pin

V17

V16

U16

E19

U19

V19

W18

U15
>
>
>
>
>
>
>

PROJECT MANAGER - 250227_gates

Sources

Km gates.xdc (C:\Working\FPGA_Harman_25_1\25...\250227_gates.srcs\constrs_1\new) - GVIM1 Q+ 파일(F) 편집(E) 도구(T) 문법(S) 버퍼(B) 창(W) 도움말(1)

Knaz

B

Design Sources (1)

gates (gates.)

Constraints (1)

constrs_1 (1)

gates.xdc (target)

Simulation Sources (1)

sim_1 (1)

Utility Sources

Hierarchy Libraries

Source File Properties

gates.xdc

1 2 3 5 5 8 2 1 **set** property PACKAGE_PIN_V17 [get_ports a 2 set_property PACKAGE_PIN V16 [get_ports b] 3 set_property PACKAGE_PIN U16 [get_ports y0] 4 set_property PACKAGE_PIN E19 [get_ports y1] 5 set_property PACKAGE_PIN U19 [get_ports y2] 6 set_property PACKAGE_PIN V19 [get_ports y3] 7 set_property PACKAGE_PIN W18 [get_ports y4] 8 set_property PACKAGE_PIN U15 [get_ports y5] 9 set_property IOSTANDARD LVCMOS 33 [get_ports a] 10 set_property

IOSTANDARD LVCMOS 33 [get_ports b] 11 set_property IOSTANDARD LVCMOS33 [get_ports y0] 12 set_property IOSTANDARD LVCMOS33 [get_ports y1] 13 set property IOSTANDARD LVCMOS33 [get_ports y2] Compi 14 set_property IOSTANDARD LVCMOS33 [get_ports y3] 15 set_property IOSTANDARD LVCMOS33 [get_ports y4] 16 set_property IOSTANDARD LVCMOS33 [get_ports y5] 17 set_property SLEW SLOW [get_ports yo]

JUL

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ЦИМ

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설계사양 결정/

ㅇㅎㅎㅎㅎㅎ 목표설정.

Spec 속도 ㅁㅁ

ó ó ó

6G Modem Stumdu.

및

상위수준 보델링 검증

알고리즘: 검증 없어

Nuthlab

염증

규격정 1.X.적용

1.x능

시뮬레이터

HDL 이용한 모델링

D

하면

전반부 설계

30

입력

35

사이즈

회로 합성 Netlistt

40

합성 후 검증 기능, 타이밍)

P&R

FFT

place & Routing

Wercto

bitt stream

레이아웃 설계(배치 및 배선)

X

후반부 설계 0x1700

레이아웃 후 검증(기능/타이밍)

PG 데이터 생성

20x170090

ALW

600M

dia 02112

1억

6

4개
x
비용

(JUM)
VI 검증 eng
GGG L

1만개

매스크 제작, 웨이퍼 가공

FPGA 디바이스 구현

칩 테스트 및 패키징

[그림 1-1] HDL 기반 시스템 반도체(디지털 시스템) 설계과정

SC

half Adder

Top, 현재까지,

HA

o

a

عن

자리수 1t

올림

nx a

*

o-s

7217

입력.

T

*

A и

b

힘으

10

ㅣ

b⇒

block

L

자리수

S=

올림

c

0 =

аль

946

코딩

⇒ tb_adder ← Top

T

فى

Fill

4 11

adver

Test (목적)

Z

S

C

adder Design

module

শুভ

সুপ্রভাত

a

b

S

C

Product family:

Project part:

Top module nan

Ctrl+E

Alt+O

Alt+Equals

adder u_half_adder (

);

aa .bb,

SSD, (CD

to cuola

reg a, b

wire s, **c;**

// **reg**, 저장하다 .

// **wire**.

연결용

"testbech

Sources

o

Design Sources (1)

Simulation.

?

+

?

ХЛО

Simulation Sources (2)

✓ sim_1 (2)

adder (adder.v)

tb_add
Source Node Properties...
Utility Sources
Open File

Hierarchy
Librari
adder (adder.v)
Replace File...

Add Sources
Copy File Into Project
Constraints
This guides you through the process of adding and creating sources **foource File Properti**
Copy All Files Into Project
Alt+1

constrs_1
tb_adder.v
X Remove File from Project...
Delete
Add or create constraints

Simulation Sources (1)
Enable File
Add or create design sources
✔Enabled

Disable File
Alt+Minus

sim_1 (1)

Add or create simulation sources
Location:
C:
Move to Simulation Sources

adder (adder.v)

Type:
Ve
Move to Design Sources

Library:
xil

Utility Sources

Hierarchy Update

Size:
0. C Refresh Hierarchy

Hierarchy Libraries

Compile Order

IP Hierarchy

Set as Top
General
Properti

难儿

누리

initial :

ㄴ

저장입

begin

#10:

end

delay = x/

시간

a = 0; b = **0**;

* timescale

initial :

begin

conse #10;

Gio

Lo use #10;

#10; **#10**;

10

a = 0;

a =

a =

1;

0;

b = 0;

b

a = 1; b

ro ro ro

ro

C

ے

6

half Adder

FA

لانا

a

S C

TOP, 현재까지

halfAdder

a b

oo

Sc

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Ha

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b

D

단위

3

a

عد

x.

10

o

b

block,

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FA

FA

=

b

b =

0; 2ons 1;30 n (

0 = 946

c

Сти

b =

1; 40use

end

poonsec

FA

S = a

Scope x Sources
Ox Pro ?G
Untitled 1

*
Q
Q
"QQ

Name

arther Justance 101

Design ʊ... BI
Name Value

b_adder tb adder Ve
la
1
Name
Value
,0,000 ns
,200,000 ns
,400,000 ns
,600,000 ns
,800,000 ns
1,000,000 ns

U_half_adde **adder**
1
Ma
1

glbl
gibl
VE
18 **s**

0

14b

14 **c**

1

1

0

18 c

1

? OK

oo

1,000,000 ns

Cin a bisc

Сти

3

-

o

b

o

half B

8 5729215

o

구조적 모델링

o

C

haltA

o

o

ง

1bit

FA

FA

b

C.

a

FA

S = a

Сти

s

halta

half B

b

Сти

구조적 모델링/

Cin a b

S

C

oo

0

Full-Adder-

U_HAI

ア

a ($

c

UHA

الى

5

```
input a,
```

```
6
input b
7
input cin,
8
output s
9
output c
10 );
S
11
12
wire w_s;
// wiring U_HA1 out s to U_HA2 in a
13
wire w_c1, w_c2;
14
15
assign c =
w_c1 || w_c2;
16
17
18
19
half_adder U_HA1 (
20
21
a (a), .b(b),
W_CI
OR
22
.s (w_s),
23
c (w_c1)
24
);
25
26
half_adder U_HA2 (
27
a (w_s),
// from U_HA1 of s
```

```
28
b(cin),
29
.s(s),
30
.c(w_c2)
//
31
);
32
33
34
35 endmodule
3 //1bit FA
4 module full_adder(
```

00

37 module half_adder(

3456

oo

10

38

input a

7

8
adder U_full_adder
39
input b
9
10
10
40
output s,
11
12
41
output c
13
3 module tb_adder();

reg a, b, cin; // reg.
wire s, c; // output wire.

.a (a), b(b), .cin(cin),

s(s),
.c(c)
// module instance

// input carry.

14
42);
15
);
16
43
17
initial

```
44
// half adder 1bit
18
begin
19
#10;
a =
0; b = 0;
cin = 0;
45
assign s = a ^ b;
20
#10;
a = 1; b = 0;
cin= 0;
21
#10;
a = 0; b = 1;
cin= 0;
46
assign c = a & b;
22
#10;
a = 1;
1: b = 1:
cin= 0;
23
#10;
a = 0: b
=
0;
cin = 1
47
24
#10;
a = 1; b = 0;
cin = 1;
25
#10;
a = =0; b = 1;
48 endmodule
```

```
26
#10;
a =
1;
b
=
1;
cin = 1; cin =
1;
27
$stop;
28
end
20
```

*4 bit FA

MRI Test

bench

าน

home work