



» **DATA SHEET**
(DOC No. HX8379-A-DS)

» **HX8379-A**
480RGB x 864 dot,
16.7M color,
TFT Mobile Single Chip Driver
Preliminary version 01 June, 2012

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1. General Description

This document describes Himax's HX8379-A supports WVGA (480RGBx864) resolution driving controller. The HX8379-A is designed to provide a single-chip solution that combines source driver control, gate in panel control and power supply circuit to drive a TFT dot matrix LCD with 480RGB x 1024 dots at maximum.

The HX8379-A can be operated in low-voltage condition for the interface and produced the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. In addition, The HX8379-A also supports various functions to reduce the power consumption of a LCD system via software control.

The HX8379-A supports several interface modes, including MIPI DPI and DBI Type C, I2C , SPI 16bits interface mode, MIPI DSI (Display Serial Interface) interface mode, . The interface mode is selected by the external hardware pins IM[3:0].

The HX8379-A is suitable for any small portable battery-driven and long-term driving products, such as small PDAs, digital cellular phones and bi-directional pagers.

2. Features

2.1 Display

- Single chip solution for a WVGA GIP (Gate In Panel) type TFT LCD display
- Resolution:
 - 480RGB x 320/360/640/720/800/854/864/1024
NL is internal register setting, and the maximum Gate number is 1024.
- Display color modes
 - Full color mode:
 - 16.7M colours (24-bit 8(R):8(G):8(B))
 - Reduce color mode:
 - 262k colours (18-bit 6(R):6(G):6(B))
 - 65k colours (16-bit 5(R):6(G):5(B))
 - 8 colors (Idle mode on): 8 colors (3-bit binary mode)

2.2 Display module

- Support 1440 source channel outputs
- Gate driver control signal for GIP
- Supports 1-dot / 2-dot / 4-dot/ 8-dot / Column / Zig-Zag inversion
- Output voltage level
 - VSP is 4.5V ~ 6.5V
 - VSN is -4.5V ~ -6.5V
 - Positive source output high voltage level: VSPR is 3.0V ~ 6.3V
 - Positive source output low voltage level: VGSP is 0V, 0.3V ~ 3.7V
 - Negative source output high voltage level: VSNR is -3.0V ~ -6.3V
 - Negative source output low voltage level: VGSN is 0V, -0.3V ~ -3.7V
 - Positive gate driver output voltage level: VGH is 7V ~ 18V
 - Positive gate driver output voltage level: VRGH is 3V ~ 12V
 - Negative gate driver output voltage level: VGL is -7V ~ -18V
 - Negative gate driver output voltage level: VGL_REG is -6.4V ~ -18V
 - Common electrode voltage level: VCOM is 0V, +1V ~ -3V, a step=15mV

2.3 Display / control interface

- Display interface types supported
 - MIPI-DBI mode
 - MIPI-DBI Type C (Serial data transfer interface) interface
 - MIPI-DPI mode
 - 16 bit/pixel R(5), G(6), B(5)
 - 18 bit/pixel R(6), G(6), B(6)
 - 24 bit/pixel R(8), G(8), B(8)
 - MIPI-DSI (Display Serial Interface) interface
 - Support DSI Version 1.02
 - Support D-PHY version 1.00
 - I2C (Inter-Integrated Circuit) interface
 - SPI 16bits interface

2.4 Input power

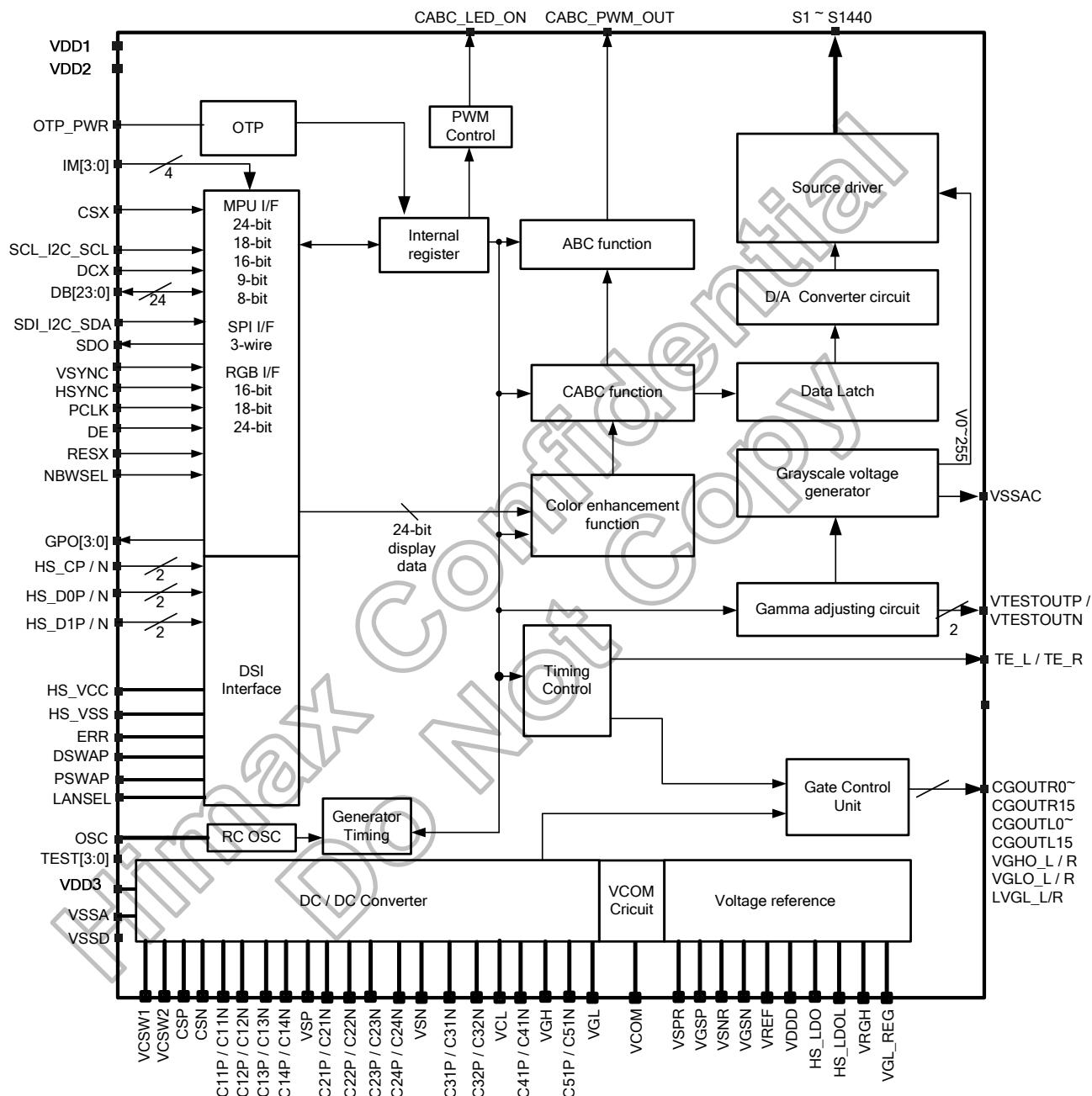
- I/O and interface power supply: VDD1 is 1.65V ~ 3.3V
- Analog power supply: VDD2 is 2.3V ~ 4.8V
- Logic power supply: VDD3 is 2.3V ~ 4.8V
- High speed interface power supply HS_VCC is 1.65V ~ 4.8V
- OTP programming voltage: OTP_PWR is 7.5V ± 0.2V.

2.5 Miscellaneous

- Software programmable color depth mode
- Oscillator for display clock generation
- Low power consumption, suitable for battery operated systems
- CMOS compatible inputs
- Proprietary multi phase driving for lower power consumption
- GAS function for preventing image sticking when abnormal power off
- Optimized layout for COG assembly
- Temperature range: -40 to +85 °C
- Support inversion mode
- DC/DC converter for source
- Support DC COM driving
- VCOM voltage generator
- On-chip OTP program voltage generator
- OTP memory to store initialization register settings
- 3 times MTP for VCOM setting ,ID setting
- Support Content Adaptive Brightness Control(CABC) function
- Support DGC (Digital Gamma Correction) function
- Support Image Enhancement function

3. Device Overview

3.1 Block diagram



3.2 Pin description

Host interface pins													
Signals	I/O	Pin no.	Connected with	Description									
IM [3 : 0]	I	4	VSSD / VDD1	Select the interface mode as listed below:									
				IM3	IM2	IM1	IM0	MPU interface mode	DB pins	Display mode			
				1	0	1	0	DPI/DBI TYPE-C Option 1	SDI/SDO, DB23-DB0	Type 1/3			
				1	0	0	1	DPI/DBI TYPE-C Option 3	SDI/SDO, DB23-DB0	Type 1/3			
				0	0	1	1	16bits SPI interface, rising trigger	SDI/SDO, DB23-DB0	Type 1/3			
				1	0	1	1	16bits SPI interface, falling trigger	SDI/SDO, DB23-DB0	Type 1/3			
				0	1	0	0	I2C interface	I2C_SDA / I2C_SCL, DB23-DB0	Type 1/3			
				0	1	0	1	MIPi DSI	HS_CLK_P/N, HS_D0P/N, HS_D1P/N,	-			
Other setting				Not used		-	-	-					
Must be connected to VSSD or VDD1													
CSX	I	1	MPU	Chip select signal. Low: chip can be accessed; High: chip cannot be accessed. If this pin is not used, connect it to VDD1.									
DCX	I	1	MPU	Data / Command Selection pin If this pin is not used, please connect it to VSSD or VDD1.									
RESX	I	1	MPU or reset circuit	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied (Must be connected to VSSD or VDD1)									
SCL_I2C_SCL	I	1	MPU	SPI:DBI Type-C Option 1/3: it servers as SCL (Serial Clock) I2C interface : serial clock input. If not use, let it open or connected to VDD1.									
SDI_I2C_SDA	I/O	1	MPU	SPI:Serial data input pin. I2C interface : serial data inout. If not used, let it to open.									
SDO	O	1	MPU	Serial data output pin. If not used, let it to open.									
DB23~0	I/O	24	MPU	DPI type interface, refer to section 4.1.2									
				Data bus									
				16-bit bus									
				18-bit bus									
				24-bit bus									
Let the unused pins open for each mode.													
NBWSEL	I	1	MPU	Select the voltage sequence of V0 ~ V255									
				NBWSEL		V0 ~ V255 voltage							
				0	V0 > V1 > ... > V254 > V255 (Normally White)								
I2C_SA0	I	1	MPU	I2C slave address select.									
				I2C_SA0		Slave Address							
				0	1001100								
GPO[3:0]	O	4	-	General purpose output pins to control the external circuits. Output level is VSSD to VDD1. If not used, let it open									
Clock input and RGB interface													
HS	I	1	MPU	Line synchronizing signal. If this pin is not used, connect it to VSSD or VDD1.									
DE	I	1	MPU	Data enable signal. If this pin is not used, connect it to VSSD or VDD1.									
VS	I	1	MPU	Frame synchronizing signal.									

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				If this pin is not used, connect it to VSSD or VDD1.
PCLK	I	1	MPU	Dot clock signal. If this pin is not used, connect it to VSSD or VDD1.
Source driver output pins				
S1 to S1440	O	1440	LCD	Output voltages applied to the liquid crystal.
SDUM[3:0]	O	4	LCD	Dummy Source. If not used, let it open
TE_L	O	1	MPU	Tearing Effect pin.
TE_R	O	1	MPU	Tearing Effect pin.
GIP control singal and bias voltage				
CGOUTL/R0~15	O	32/32	LCD	Gate control signals for GIP panel. Output level is VGLO to VGHO
VGHO_L/R	O	11/13	LCD	High voltage level for gate control signals and gate circuits on panel.
VGLO_L/R	O	17/17	LCD	Low voltage level for gate control signals and gate circuits on panel. Voltage source can be chosen from VGL or VGL_REG.
LVGL_L/R	O	3/3	LCD	Low voltage level for gate control signals and gate circuits on panel. Voltage source can be chosen from VGL or VGL_REG. If not used, let it open
Power supply pins				
VDD1	I	8	Power supply	A power supply for the I/O circuit. VDD1=1.65 ~ 3.3V
VDD2	I	4	Power supply	A power supply for the analog power. VDD2=2.3V to 4.8V VDD2 input level should be same as VDD3 input level to avoid the level-mismatching at internal level shifter circuit.
VDD3	I	15	Power supply	A power supply for the logic power, DC/DC converter VDD3=2.3V to 4.8V.
VDD3_P	I	11	Power supply	A power supply for charge-pump circuit. Please connect VDD3_P with VDD3 on FPC.
VSSA	P	25	Power supply	Analoge ground. VSSA=0V. When using the COG method, connect to VSSD on the FPC to prevent noise.
VSSAC	P	4	Power supply	Analoge ground. Must connect to VSSA on the FPC.
VSSD	P	17	Power supply	Ground for the internal logic. VSSD=0V. When using the COG method, connect to VSSA on the FPC to prevent noise.
VSSD_P	P	18	Power supply	Ground for charge-pump circuit. Please connect VSSD_P with VSSD on FPC.
OTP_PWR	I	5	Power supply	External high voltage pin used in OTP mode and operates at 7.5V. If not used, let it open.
Output pins of power and reference voltage				
VREF	O	4	Stabilizing capacitor	Reference voltage from internal band gap circuit. The tolerance of VREF voltage is $\pm 3\%$. (1.8V fixed) Connect to a stabilizing capacitor between VSSD and VREF.
VDDD	O	10	Stabilizing capacitor	Internal logic voltage output. (1.5V) Connect to a stabilizing capacitor between VSSD and VDDD.
VSP	I/O	8	Stabilizing capacitor	Voltage from the set-up circuit or external Power IC : HX5186-A/B (4.5V to 6.5V), it is generated from VDD3
VSN	I/O	11	Stabilizing capacitor	Voltage from the set-up circuit or external Power IC : HX5186-A/B (-4.5V to -6.5V). it is generated from VDD3.
VCL	O	17	Stabilizing capacitor	Voltage from the set-up circuit (-2.5V ~ -3.1V). it is generated from VDD3.
VSPR	O	1	-	Output regulated positive voltage for positive gamma high voltage. (3.0V to VSP – 0.5)
VGSP	O	1	-	Output regulated positive voltage for positive gamma low voltage. (0V, 0.3V to 3.7V)
VSNR	O	2	-	Output regulated negative voltage for negative gamma high voltage. (-3.0V to VSN + 0.5)
VGSN	O	2	-	Output regulated negative voltage for negative gamma low voltage. (0V, -0.3V to -3.7V)
VGH	O	2	Stabilizing capacitor	Output voltage from the step-up circuit, it is generated from VSP and VSN. Connect to a stabilizing capacitor between VSSA and VGH.
VRGH	O	12	Stabilizing capacitor	Output regulated voltage for panel voltage. It is generated from VGH. Connect to a stabilizing capacitor between VSSA and VRGH. If not used, let it open.
VGL	O	6	Stabilizing capacitor	Output voltage from the step-up circuit, it is generated from VSP and VSN. Connect to a stabilizing capacitor between VSSA and VGL. Place a schottkey barrier diode between VSSA and VGL.
VGL_REG	O	4	Stabilizing capacitor	Output regulated voltage for panel voltage. It is generated from VGL. Connect to a stabilizing capacitor between VSSA and VGL_REG.

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VCOM	O	10	Stabilizing capacitor	If not used, let it open. The power for common voltage in DC com driving. (0V, +1V to -3V) Connected a stabilizing capacitor 2.2u to VSSA.																																		
DC/DC pumping																																						
C11P, C11N C12P, C12N C13P, C13N C14P, C14N	I/O	24	Step-up Capacitor	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VSP voltage.																																		
C21P, C21N C22P, C22N C23P, C23N C24P, C24N	I/O	24	Step-up Capacitor	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VSN voltage.																																		
C31P, C31N C32P, C32N	I/O	12	Step-up Capacitor	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VCL voltage.																																		
C41P, C41N	I/O	4	Step-up Capacitor	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VGH voltage.																																		
C51P, C51N	I/O	4	Step-up Capacitor	Connect to the step-up capacitors according to the DC/DC pumping factor by pumping the VGL voltage.																																		
CSP	I	2	-	Current sensing input for PFM																																		
CSN	I	2	-	Current sensing input for PFM																																		
VCSW1, VCSW2	O	4	-	VCSW1 and VCSW2 connect with external power IC : HX5186-A/B or PFM circuit to generate VSP, VSN.																																		
CABC & ABC																																						
CABC_PWM_OUT	O	1	LED Driver	PWM output pin of Backlight control. If use CABC function, the pin can connect to external LED driver IC. If not used, let it open.																																		
CABC_LED_EN	O	1	LED Driver	Enable signal of Backlight LED driver(Active high). If not used, let it open.																																		
LED_BOOST	O	1	LED Driver	LED boost control signal at high brightness mode.(Active high) If not used, let it open.																																		
IDLE_ON	O	1	LED Driver	Digital LED control signal at IDLE mode. If not used, let it open.																																		
LED1, LED2	O	2	LED	Analog current output for LED control at IDLE mode. If not used, let it open.																																		
High speed interface parts																																						
DSWAP, PSWAP	I	2	MPU	MIPI DSI : DSWAP select the data output pin sequence. PSWAP select the signal polarity.																																		
				<table border="1"> <thead> <tr> <th>DSWAP</th><th>PSWAP</th><th>HS_D0P</th><th>HS_D0N</th><th>HS_CP</th><th>HS_CN</th><th>HS_D1P</th><th>HS_D1N</th></tr> </thead> <tbody> <tr> <td rowspan="2">0</td><td>0</td><td>Data Lane 0+</td><td>Data Lane 0-</td><td>Clock +</td><td>Clock -</td><td>Data Lane 1+</td><td>Data Lane 1-</td></tr> <tr> <td>1</td><td>Data Lane 0-</td><td>Data Lane 0+</td><td>Clock -</td><td>Clock +</td><td>Data Lane 1-</td><td>Data Lane 1+</td></tr> <tr> <td rowspan="5">1</td><td>0</td><td>Data Lane 1+</td><td>Data Lane 1-</td><td>Clock +</td><td>Clock -</td><td>Data Lane 0+</td><td>Data Lane 0-</td></tr> <tr> <td>1</td><td>Data Lane 1-</td><td>Data Lane 1+</td><td>Clock -</td><td>Clock +</td><td>Data Lane 0-</td><td>Data Lane 0+</td></tr> </tbody> </table>	DSWAP	PSWAP	HS_D0P	HS_D0N	HS_CP	HS_CN	HS_D1P	HS_D1N	0	0	Data Lane 0+	Data Lane 0-	Clock +	Clock -	Data Lane 1+	Data Lane 1-	1	Data Lane 0-	Data Lane 0+	Clock -	Clock +	Data Lane 1-	Data Lane 1+	1	0	Data Lane 1+	Data Lane 1-	Clock +	Clock -	Data Lane 0+	Data Lane 0-	1	Data Lane 1-	Data Lane 1+
DSWAP	PSWAP	HS_D0P	HS_D0N	HS_CP	HS_CN	HS_D1P	HS_D1N																															
0	0	Data Lane 0+	Data Lane 0-	Clock +	Clock -	Data Lane 1+	Data Lane 1-																															
	1	Data Lane 0-	Data Lane 0+	Clock -	Clock +	Data Lane 1-	Data Lane 1+																															
1	0	Data Lane 1+	Data Lane 1-	Clock +	Clock -	Data Lane 0+	Data Lane 0-																															
	1	Data Lane 1-	Data Lane 1+	Clock -	Clock +	Data Lane 0-	Data Lane 0+																															
	if not used , Please connected to VSSD																																					
	Select number of data lanes for MIPI DSI Low : 1 data lanes. (HS_D0P/N and HS_CP/N) High : 2 data lanes. (HS_D0P/N, HS_D1P/N and HS_CP/N) If not used , Please connected to VSSD																																					
HS_D0_P, HS_D0_N	I/O	8	High Speed Interface Host	MIPI DSI : Data differential signal input pins. (Data lane 0) if not used , Please connected to VSSD or open.																																		
HS_CLK_P, HS_CLK_N	I	8	High Speed Interface Host	MIPI DSI : CLOCK differential signal input pins. if not used , Please connected to VSSD or open.																																		
HS_D1_P,	I	8	High Speed	MIPI DSI : Data differential signal input pins. (Data lane 1)																																		

HS_D1_N			Interface Host	if not used , Please connected to VSSD or open.
ERR	O	1	-	CRC and ECC output pin for MIPI DSI. If not used , Please leave this pin open
HS_VCC	P	5	Power Supply	Power supply for the MIPI DSI analog power. MIPI DSI : HS_VCC=1.65V ~ 5.5V (Recommend to connect with VDD1)
HS_VSS	P	11	Ground	MIPI DSI analogy ground. HS_VSS=0V. When using the COG method, connect to VSSD on the FPC to prevent noise.
HS_LDO	O	3	Capacitor	MIPI DSI regulator output pin. (1.5V) Connect to a stabilizing capacitor between HS_VSS and HS_LDO If not used, please open these pins.
HS_LDOL	O	3	Capacitor	MIPI DSI regulator output pin. (1.2V) If not used, please open these pins.

Test Pins

DUMMY_DIOPWR	I	2	-	No function, let it open or connect to VSSD or VDD1
DUMMY_DSTB_SE_L	I	1	-	No function, let it open or connect to VSSD or VDD1
DUMMY_KBBC	I	1	-	No function, let it open or connect to VSSD or VDD1
DUMMY_RDX	I	1	-	No function, let it open or connect to VSSD or VDD1
DUMMY_RGBBP	I	1	-	No function, let it open or connect to VSSD or VDD1
OSC	I	1	Open	Oscillator input for test purpose. If not used, please let it open or connected to VSSD.(weak pull low)
TEST[3:0]	I	4	Open	A test pin. This pin is by internal logic function test.This pin can output on FPC. If not used, let it open or connected to VSSD.(weak pull low)
VTESTOUTP	O	1	Open	A test pin. Disconnect it. This pin will output Gamma voltage. This pin can output on FPC.
VTESTOUTN	O	1	Open	A test pin. Disconnect it. This pin will output Gamma voltage. This pin can output on FPC.
DUMMYR_1A, DUMMYR_1B, DUMMYR_2A, DUMMYR_2B	-	4	Open	DUMMY_1A and DUMMY_1B are short in driver IC. DUMMY_2A and DUMMY_2B are short in driver IC. These pins are for bonding resistance measurement. These pins are Hi-Z in driver IC.
VGSW[3:0]	-	4	Open	Not used. Let it open.
DUMMY1-109	-	109	Open	Not used. Let it open.

4. Interface

4.1 System interface

The HX8379-A supports MIPI interfaces: DBI (Display Bus Interface) serial interface Type-C, DPI (Display Pixel Interface), DSI (Display Serial Interface). Where. The interface mode can be selected by IM[3:0] pins setting as show in Table 4.1.

IM3	IM2	IM1	IM0	MPU interface mode	Display Data
1	0	1	0	DPI/DBI TYPE-C Option 1	DPI
1	0	0	1	DPI/DBI TYPE-C Option 3	DPI
0	0	1	1	16bits SPI interface, rising trigger	DPI
1	0	1	1	16bits SPI interface, falling trigger	DPI
0	1	0	0	I2C interface	DPI
0	1	0	1	MIPI DSI	DSI
Other setting				Not used	-

Table 4.1: Interface selection

Interface	RDX	SCL / I2C_SCL	DCX	D23–D0 or other input pin
DPI/DBI TYPE-C Option 1	Unused	SCL	Unused	DB23–DB0: 24-bit data bus SDI / SDO
DPI/DBI TYPE-C Option 3	Unused	SCL	DCX	DB23–DB0: 24-bit data bus SDI / SDO
16bits SPI interface, rising trigger	Unused	SCL	Unused	DB23–DB0: 24-bit data bus SDI / SDO
16bits SPI interface, falling trigger	Unused	SCL	Unused	DB23–DB0: 24-bit data bus SDI / SDO
I2C Interface	Unused	I2C_SCL	Unused	DB23–DB0: 24-bit data bus I2C_SDA, I2C_SCL
MIPI DSI	Unused	Unused	Unused	HS_CLK_P/N, HS_D0P/N, HS_D1P/N,

Table 4.2: Pin connection based on different interface

4.1.1 Serial data transfer interface (MIPI DBI TYPE-C)

The HX8379-A supports DBI Type C option 1 (3-wire) and option 3 (4-wire) serial data transfer interface, the interface selection by setting IM[3:0] pins, The IM[3:0] set "1010" is select option1 (3-wire) serial bus. The IM[3:0] set "1001" is select option 3 (4-wire) serial bus.

The 3 wire serial bus uses: chip select line (CSX), serial data input (SDI), serial data output (SDO) and the serial transfer clock line (SCL).

The 4 wire serial bus uses: chip select line (CSX), data/command select (DCX), serial data input (SDI), serial data output (SDO) and the serial transfer clock line (SCL).

4.1.1.1 Serial data write mode

The 3-pin serial data packet contains a control bit D/CX and a transmission byte and in 4-pin serial case, data packet contains just transmission byte and control signal D/CX is transferred by DCX pin. If DCX is low, the transmission byte is command byte. If DCX is high, the transmission byte is stored in to command register. The MSB is transmitted first. The serial interface is initialized when CSX is high. In this state, SCL clock pulse or serial input/output data (SDI and SDO) have no effect. A falling edge on CSX enables the serial interface and indicates the start of data transmission.

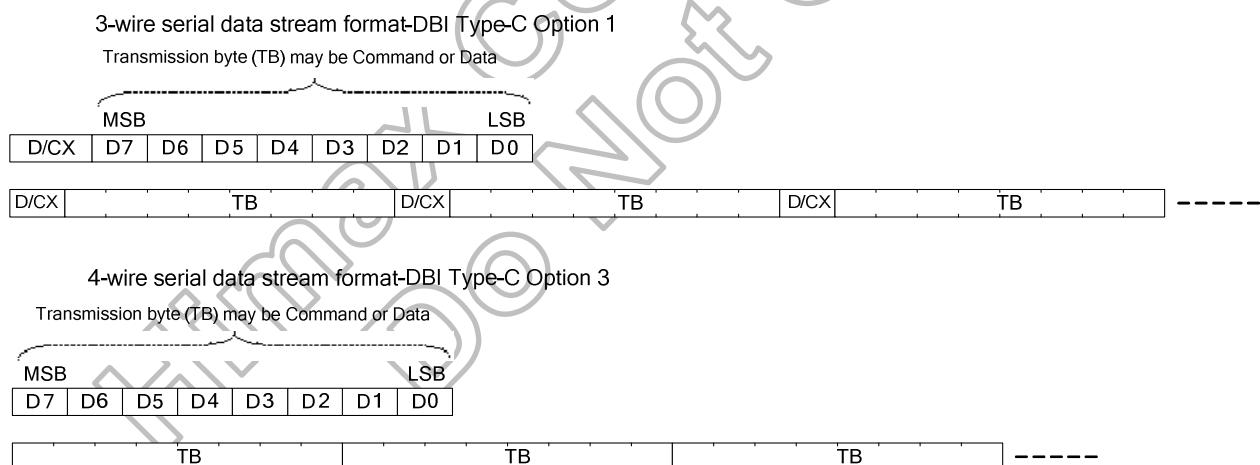
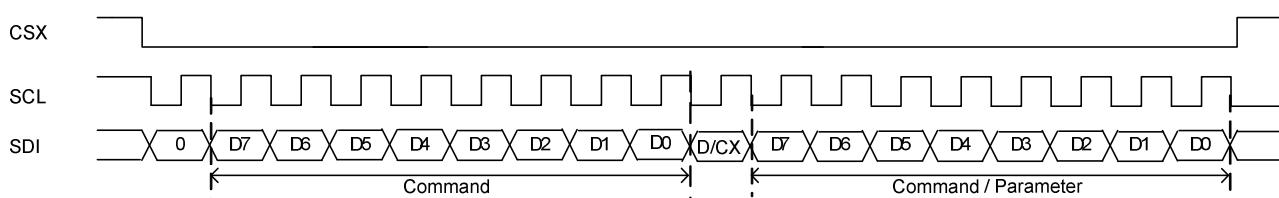
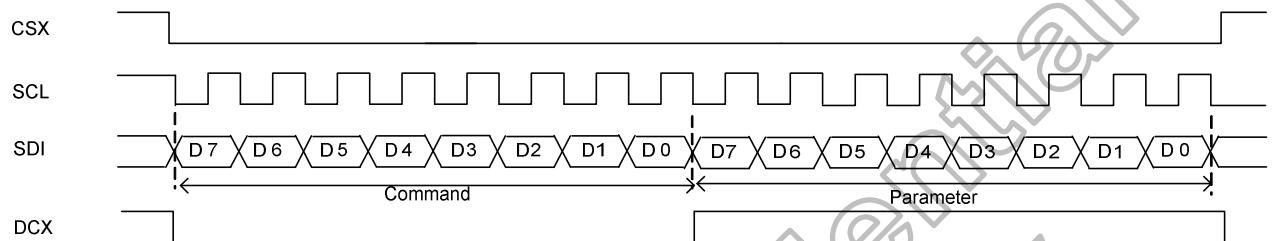
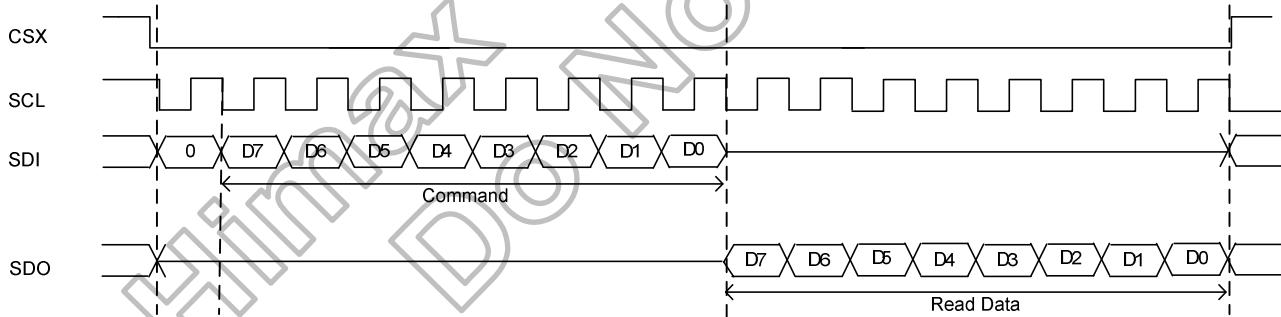
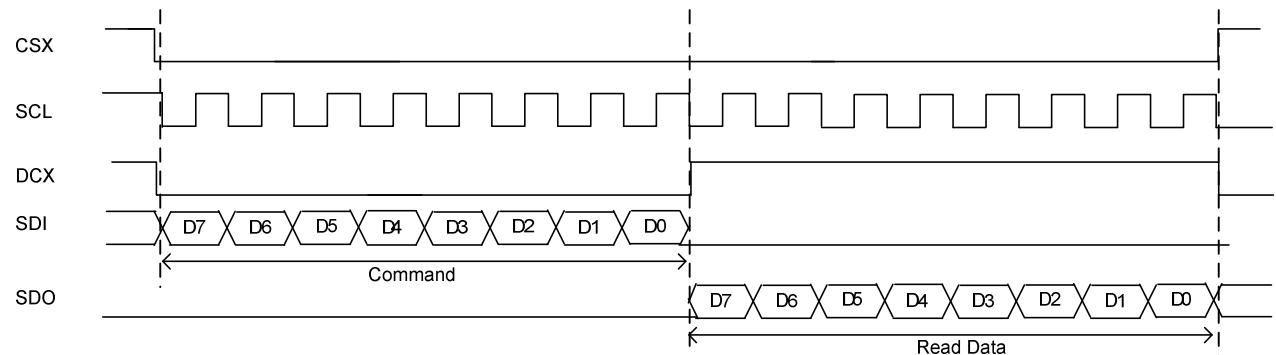


Figure 4.1: Serial data stream, write mode

DBI Type C: Interface protocol - Option 1 (3-wire)**DBI Type C: Interface protocol - Option 3 (4-wire)****Figure 4.2: DBI Type C: Serial interface protocol 3-wire/4-wire, write mode****4.1.1.2 Serial data read mode**

In serial peripheral interface read operation, the host controller first has to send a command and then the following byte is transmitted to host controller in the SDI.

DBI Type C: Interface protocol – Option 1 (3-wire)**DBI Type-C Interface Protocol – Option 3 (4 wire)****Figure 4.3: DBI Type C: Serial interface protocol 3-wire/4-wire read mode**

If there is a break on data transmission when transmit a command before a whole byte has been completed, then the display module will have reset the interface such that it will be ready to receive the same byte re-transmitted when the chip select line (CSX) is next activated. See the following figure.

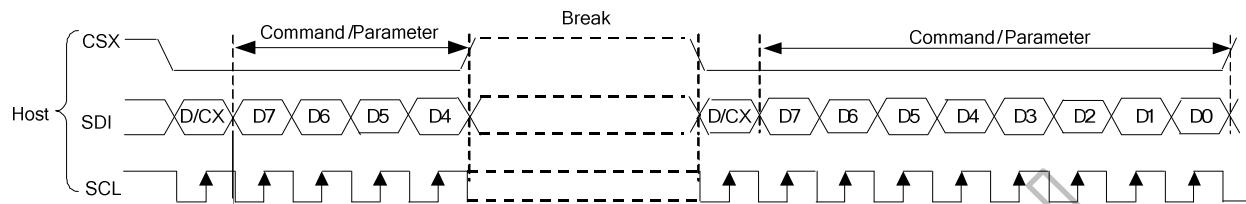


Figure 4.4: Display module data transfer recovery

If a one or more parameter command is being sent and a break occurs while sending any parameter before the last one and if the host then sends a new command rather than retransmitting the parameter that was interrupted, then the parameters that were successfully sent are stored and the parameter where the break occurred is rejected. The interface is ready to receive next byte as shown:

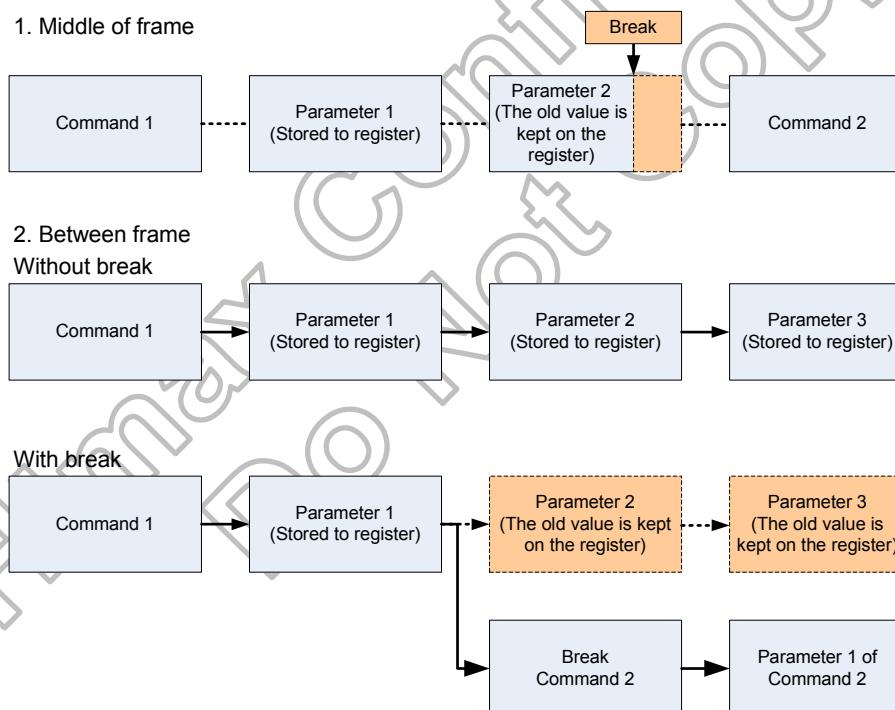


Figure 4.5: Break during parameter

The host processor can pause a write sequence by pulling the CSX signal high between command or data bytes. The display module shall wait for the host processor to drive CSX low before continuing the write sequence at the point where the sequence was paused.

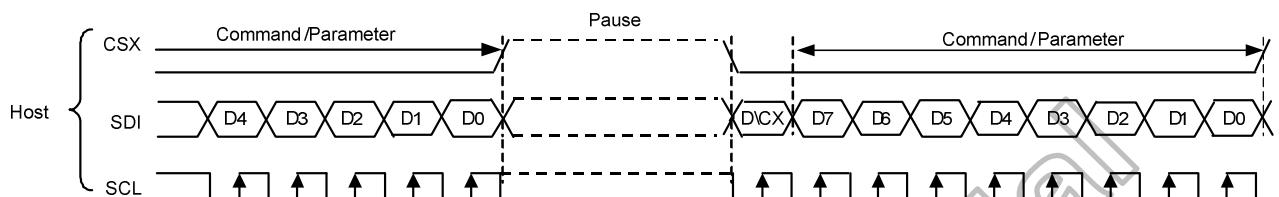


Figure 4.6: Display Module Data Transfer Pause

There are 4 cases where there is possible to see this kind of pause:

1. Command – Pause – Command
2. Command – Pause – Parameter
3. Parameter – Pause – Command
4. Parameter – Pause – Parameter

4.1.2 Serial data transfer interface (16bits data transfer)

The HX8379-A supports SPI 16bits dat transfer interface, the interface selection by setting IM[3:0] pins, The IM[3:0] set "0011" is select SPI 16bits, SCL rising trigger. The IM[3:0] set "1011" is select SPI 16bits, SCL rising trigger.

The SPI 16bits data transfer interface uses: chip select line (CSX), serial data input

4.1.2.1 Serial data 16bits write mode

The 3-pin serial data packet cont

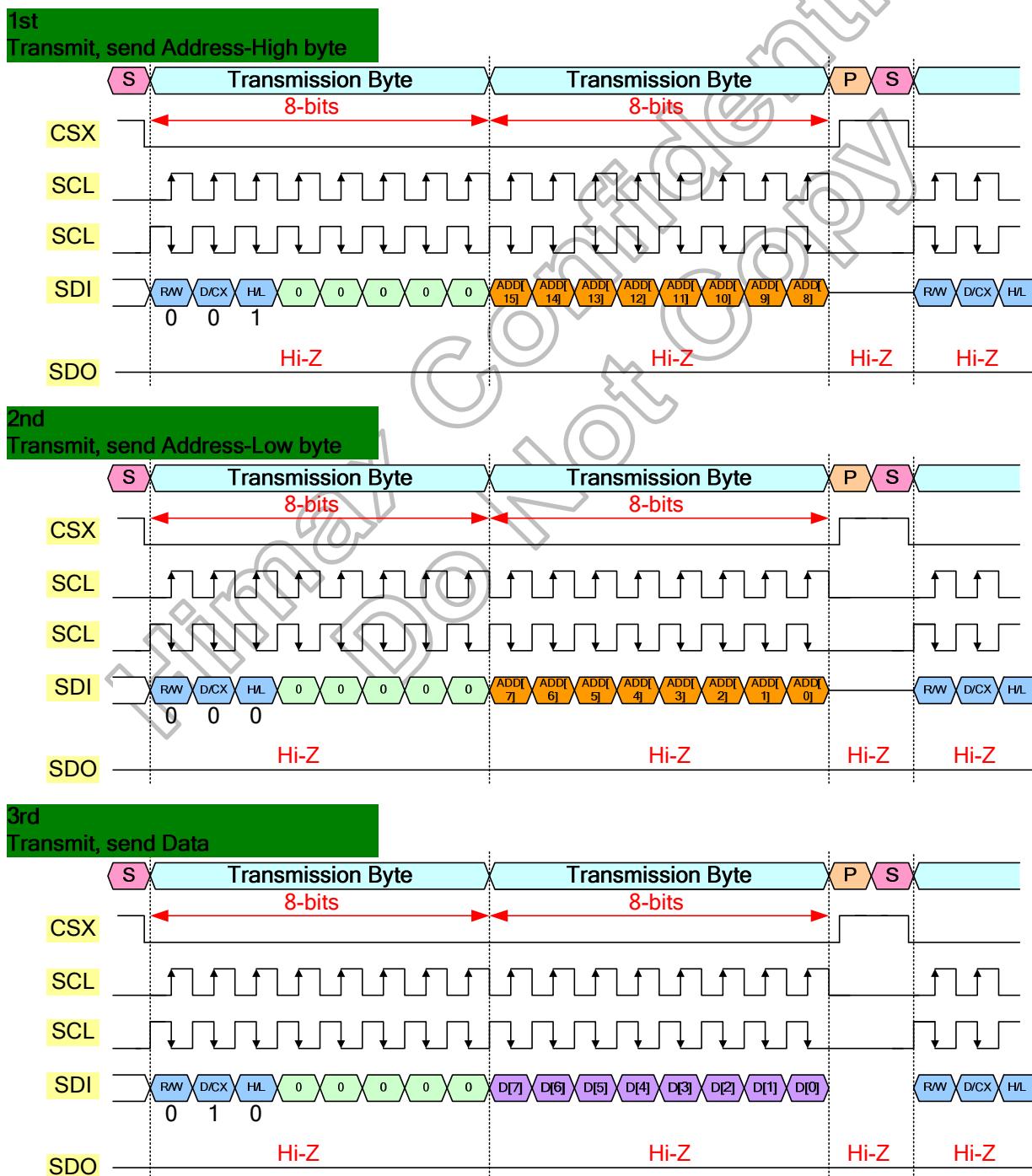


Figure 4.7: SPI 16bit mode, register write flow

4.1.2.2 Serial data 16bits read mode

The 3-pin serial data packet cont

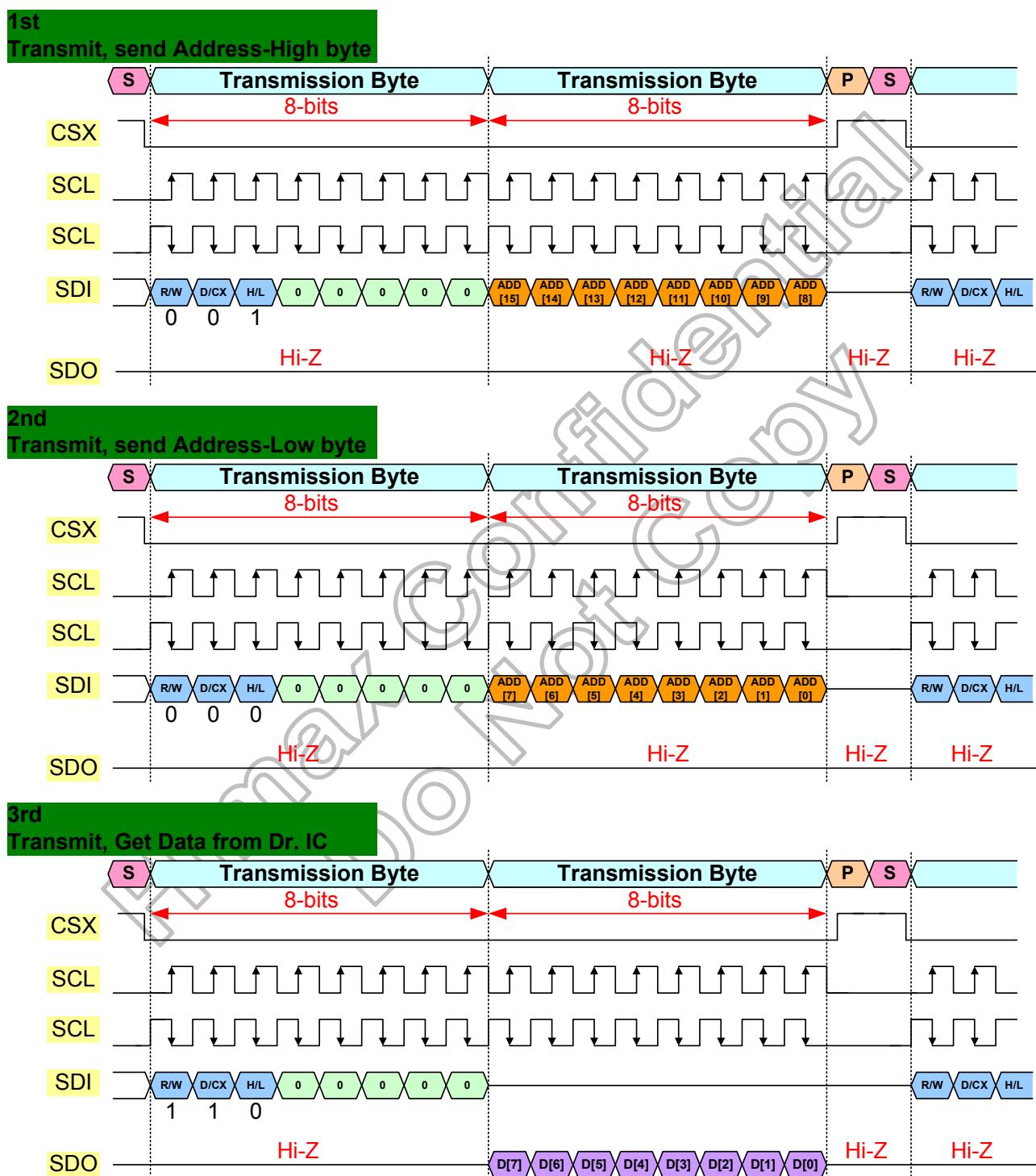


Figure 4.8: SPI 16bit mode, register read flow

4.1.3 I²C interface

The HX8379-A supports I²C interface, the interface selection by setting IM[3:0] pins, The IM[3:0] set “0100” is select I²C interface.

I²C interface 2 hardware pin – serial data (SDA) and serial clock (SCL), carry information between the devices connected to the bus. Each device is recognized by a unique address — whether it's a microcontroller, LCD driver, memory or keyboard interface — and can operate as either a transmitter or receiver, depending on the function of the device. Both SDA and SCL are needed connected to a positive supply voltage via a pull-up resistor. The pull-up resistor should connect to VDDI. When the bus is free, both lines are HIGH.

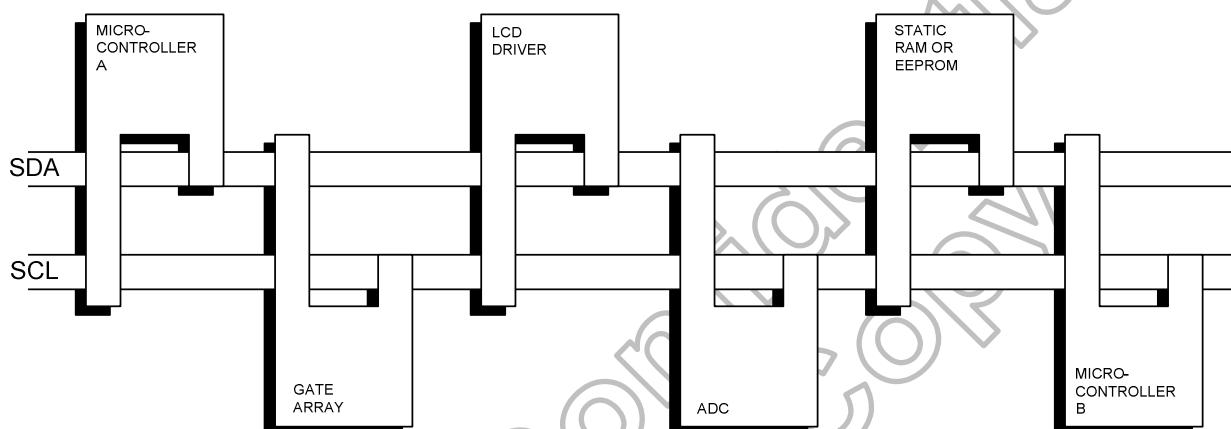


Figure 4.9 I²C connection diagram

4.1.3.1 I²C protocol

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

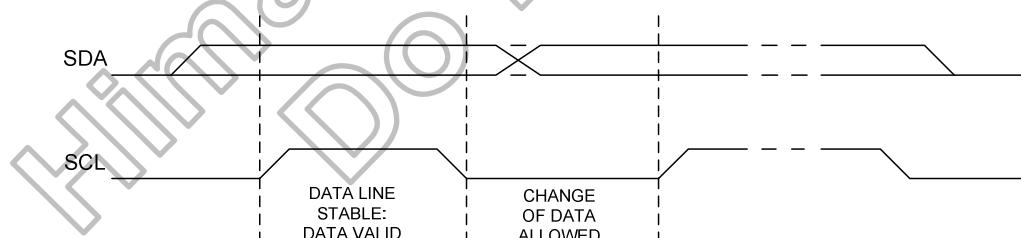
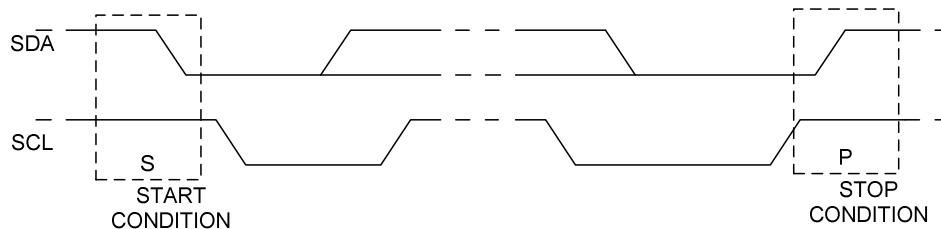
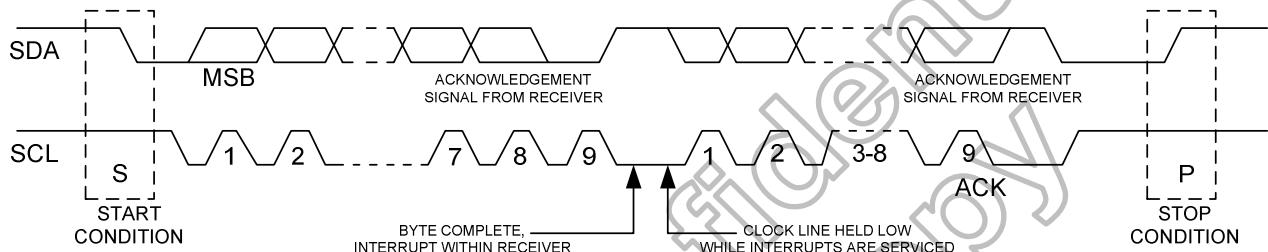


Figure 4.10: I²C Signal timing

Within the procedure of the I²C-bus, unique situations arise which are defined as START and STOP conditions. A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. START and STOP conditions are always generated by the master. The I²C bus is considered to be busy after the START condition. The I²C bus is considered to be free again a certain time after the STOP condition.

**Figure 4.11: I²C START/STOP**

Every byte put on the SDA line must be 8-bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first.

**Figure 4.12: I²C data transfer**

4.1.3.2 I²C slave address

HX8379-A has two slave address could be select by setting HW signal "I2C_SA0". The slave address of I²C selected by I2C_SA0 line is defined a follow table.

I2C_SA0	Slave address (A6-A0)
0	1001100
1	1001101

Table 4.3: I²C Slave Address table

4.1.3.3 I2C interface write mode

HX8379-A support I2C to write data to register. The write flow is described as below

- Send Start condition followed by I2C 6 bits slave address and 1 bit '0'(write flag)
- Send High byte of 16bits address, then IC feedback Ack.
- Send Low byte of 16bits address, then IC feedback Ack.
- Send 8bits register data, MSB first , ADD[7] send first, the IC feedback Ack
- Send Stop condition

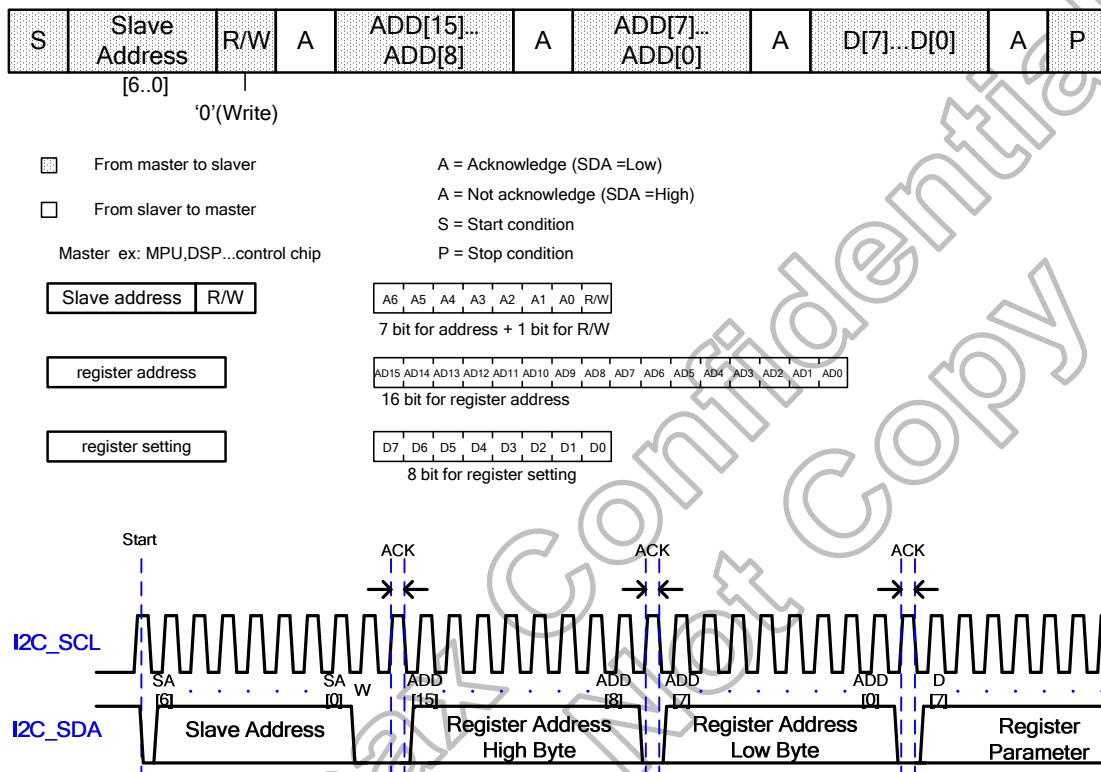


Figure 4.13: I2C interface register write flow

4.1.3.4 I2C interface read mode

HX8379-A also support I2C to read data from register. The write flow is described as below

- A. Send Start condition followed by I2C 6 bits slave address and 1 bit '0'(write flag)
- B. Sned High byte of 16bits address, then IC feedback Ack.
- C. Sned Low byte of 16bits address, then IC feedback Ack.
- D. Send restart condition followed by I2C 6 bits slave address and 1 bit '1'(read flag)
- E. IC send register data to baseband, and followed by an non-ack.
- F. Send Stop condition

S	Slave Address	0	A	ADD[15].. ADD[8]	A	ADD[7].. ADD[0]	A	Sr	Slave Address	1	A	Read Data	\bar{A}	P
---	---------------	---	---	---------------------	---	--------------------	---	----	---------------	---	---	-----------	-----------	---

From master to slaver

A = Acknowledge (SDA =Low)

From slaver to master

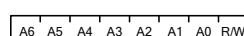
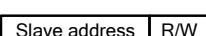
A = Not acknowledge (SDA =High)

Master ? ex: MPU,DSP...control chip

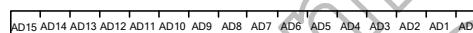
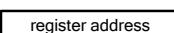
S = Start condition

Sr = ReStart

P = Stop condition



7 bit for address + 1 bit for R/W



16 bit for register address

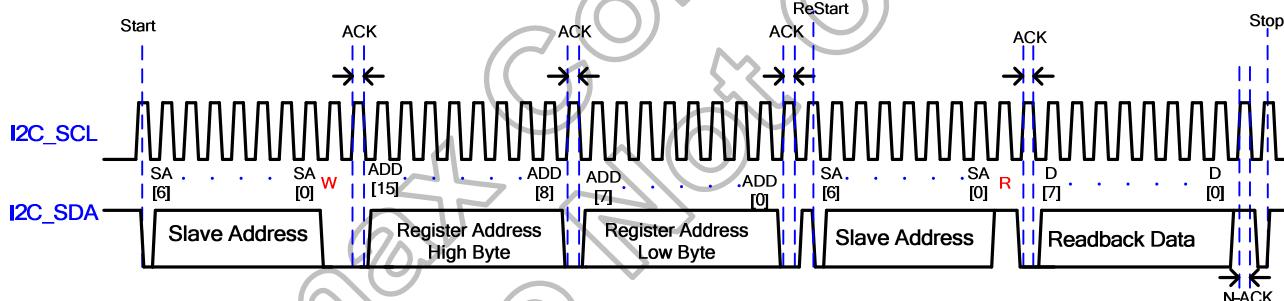
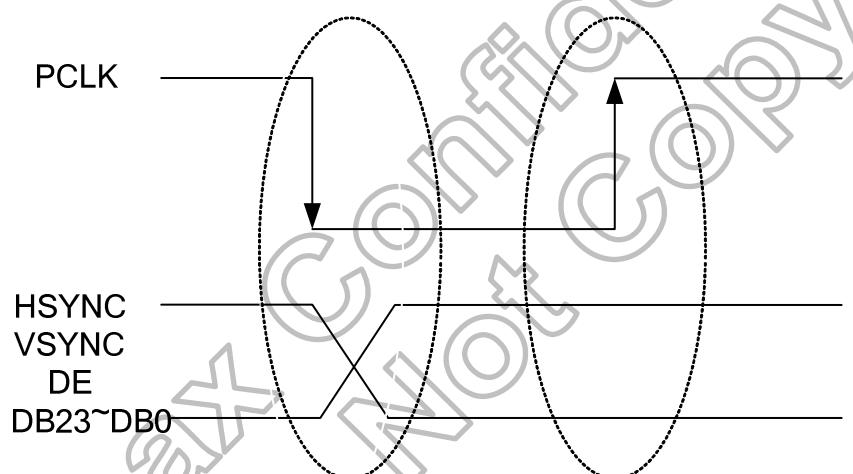


Figure 4.14: I2C interface register read flow

4.1.4 MIPI DPI interface (Display Pixel Interface)

The HX8379-A uses 16 or 18-bit or 24-bit parallel DPI interface which includes: HSYNC, VSYNC, DE, PCLK, DB23~DB0. The interface is active after Power On sequence. Pixel clock (PCLK) is running all the time without stopping and it is used to entering HSYNC, VSYNC, DE and DB23~DB0– lines states when there is a rising edge of the PCLK. The PCLK cannot be used as continue internal clock for other functions of the display module e.g. Sleep In– mode etc. Vertical synchronization (VSYNC) is used to tell when there is received a new frame of the display. This is negative (“-”, “0”, low) active and its state is read to the display module by a rising edge of the PCLK-line. Horizontal synchronization (HSYNC) is used to tell when there is received a new line of the frame. This is negative (“-”, “0”, low) active and its state is read to the display module by a rising edge of the PCLK- line. Data enable (DE) is used to tell when there is received RGB information that should be transferred on the display. This is positive (“+”, “1”, high) active and its state is read to the display module by a rising edge of the PCLK-line.

The pixel clock cycle is described in the following figure.



Note: PCLK is an unsynchronized signal (It can be stopped).

Figure 4.15: PCLK cycle

Register	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DPI Interface mode				
3Ah																													
50h	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	16-bit		
	x	x	x	R4	R3	R2	R1	R0						x	x	G5	G4	G3	G2	G1	G0	x	x	x	B4	B3	B2	B1	B0
	x	x	R4	R3	R2	R1	R0	x	x	x	x	x	x	G5	G4	G3	G2	G1	G0	x	x	B4	B3	B2	B1	B0			
60h	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	18-bit		
	x	x	R5	R4	R3	R2	R1	R0						x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0
70h	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	24-bit	-			

Table 4.4: DPI Color mapping

4.1.4.1 General timing diagram

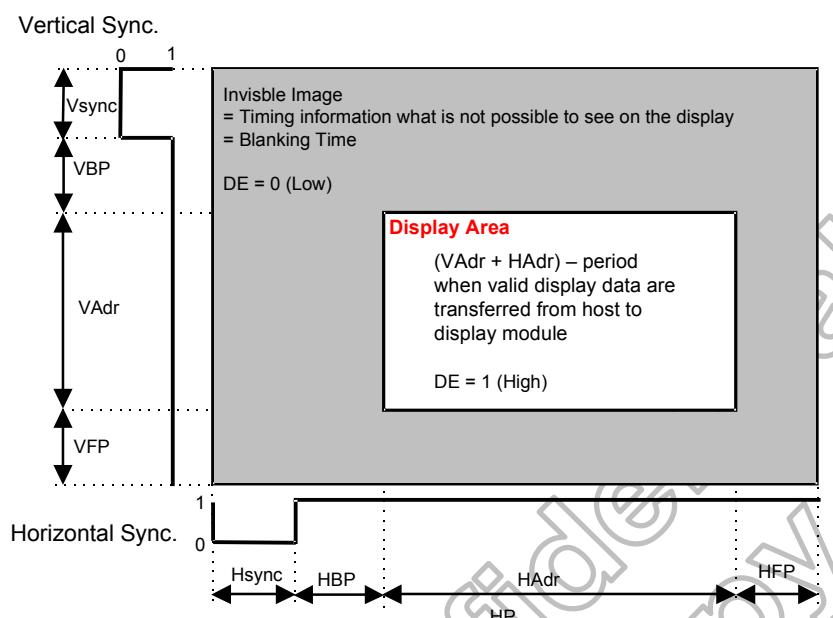


Figure 4.16: General timing diagram

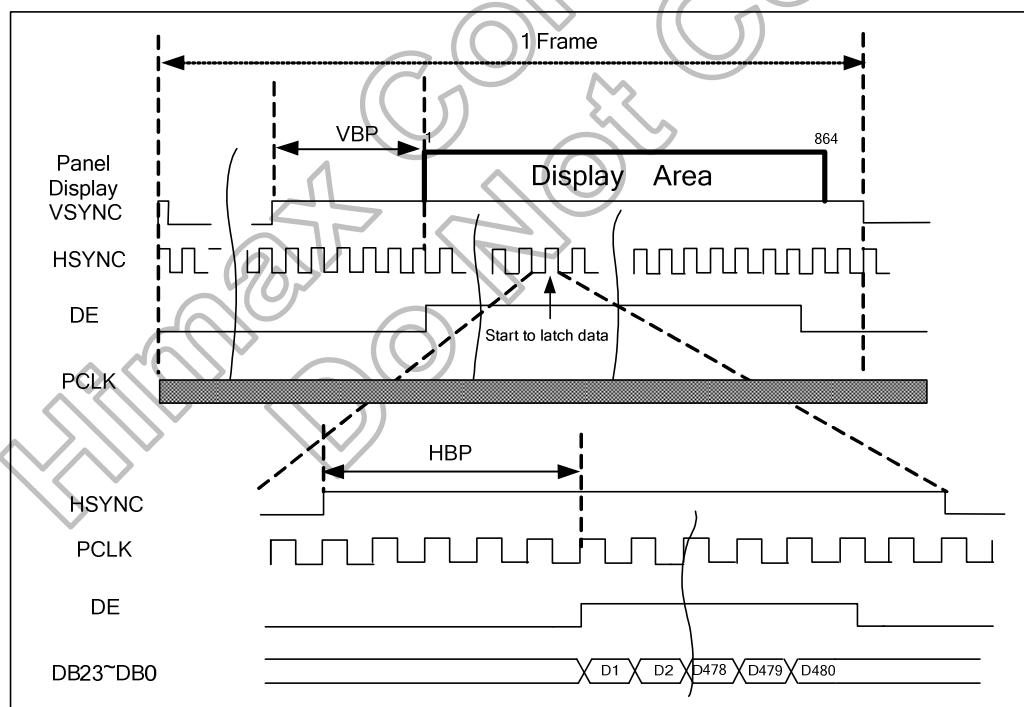
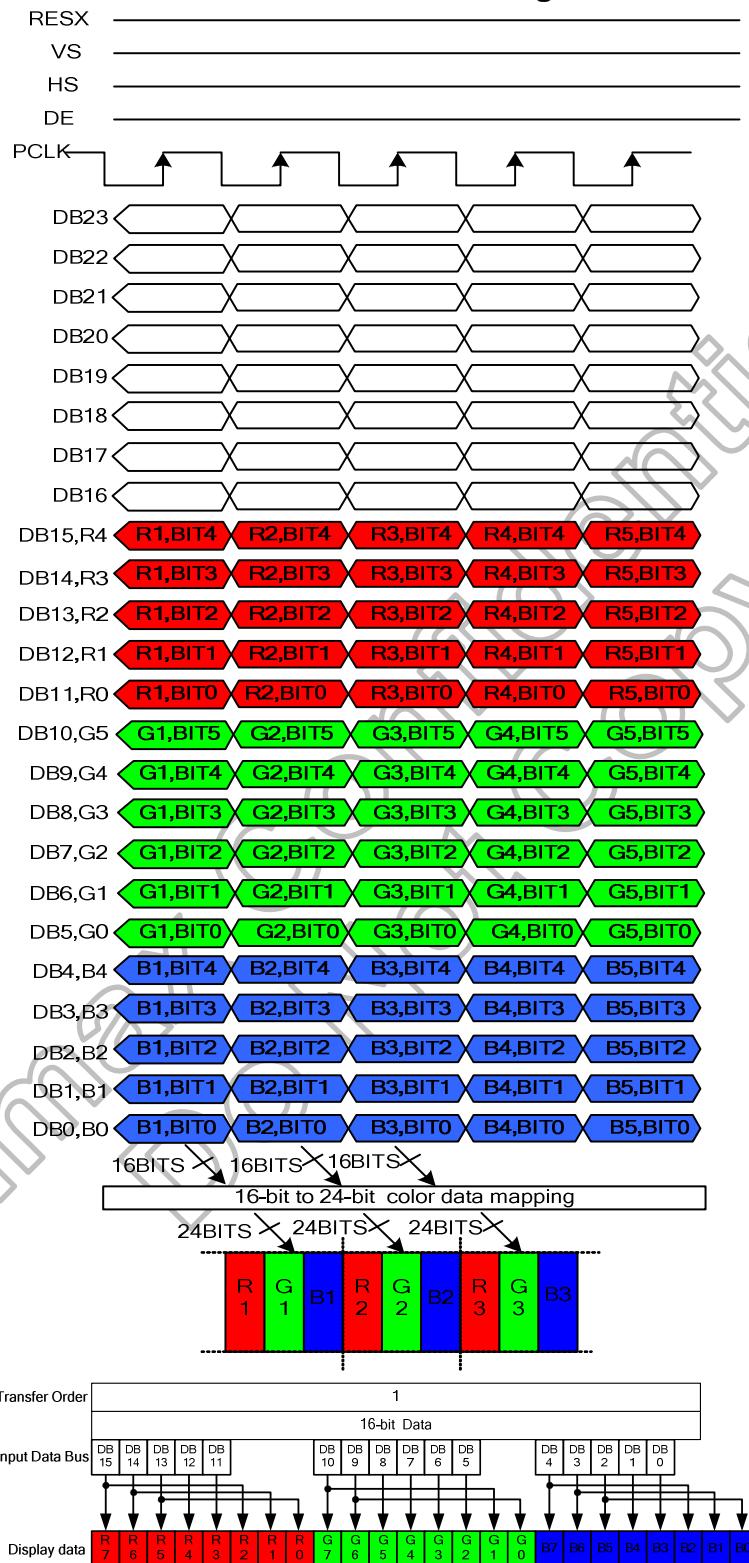


Figure 4.17: DPI (480RGB x 864) timing diagram

The image information must be correct on the display, when the timings are in range on the interface. However, the image information can be incorrect on the display, when timings are out of the range on the interface (Out of the range timings cannot cause any damage on the display module or it cannot cause any damage on the host side). The correct image information must be displayed automatically (by the display module) on the next frame (vertical sync.), when there is returned from out of the range to in range interface timings.

4.1.5 16-bit / pixel color order on the DPI I/F

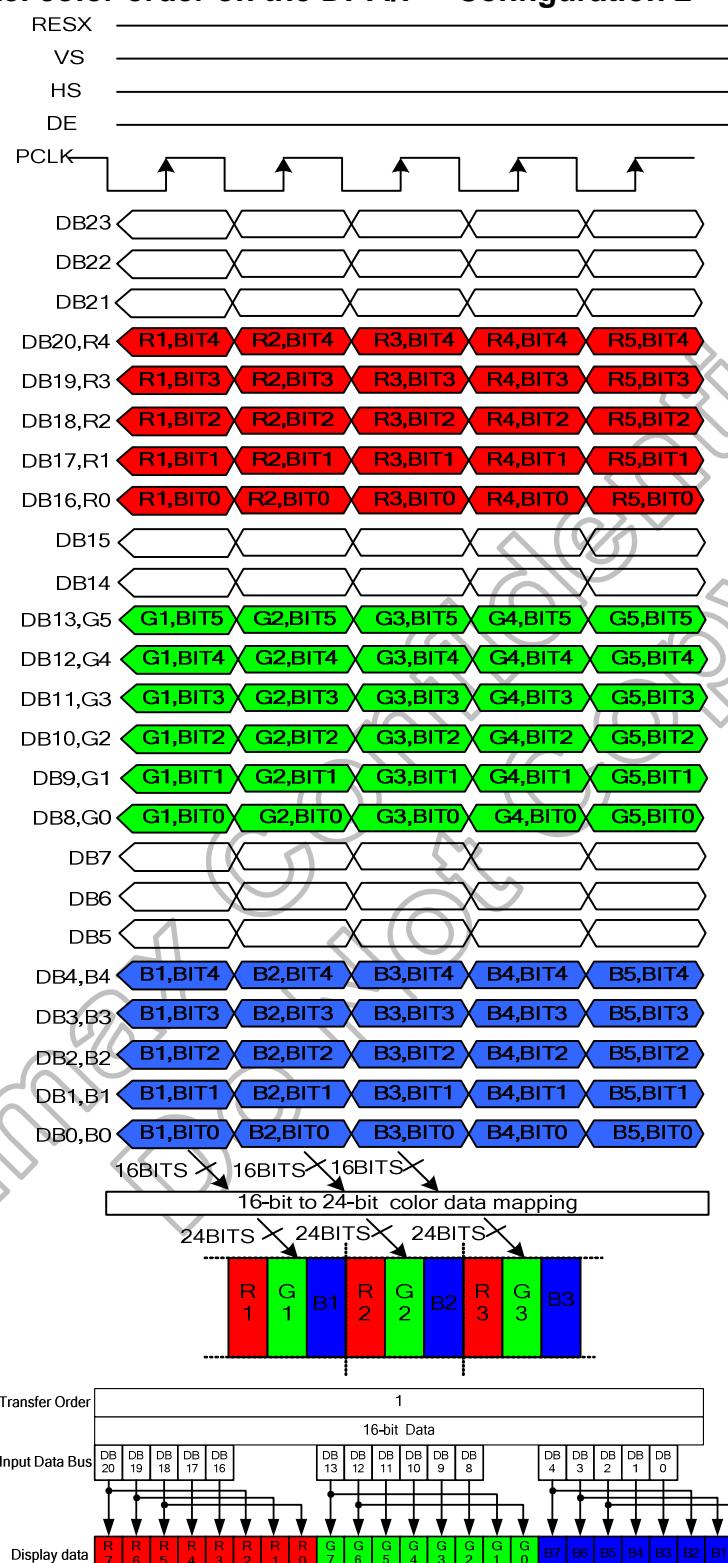
4.1.5.1 16-bit / pixel color order on the DPI I/F – Configuration 1



Note: MSB=DB23, LSB=DB0 and picture data is MSB=Bit5, LSB=Bit0 for Green data and MSB=Bit4, LSB=Bit0 for Red and Blue data.

Figure 4.18: 16-bit / pixel, 65K colours order on the DPI I/F– Configuration 1

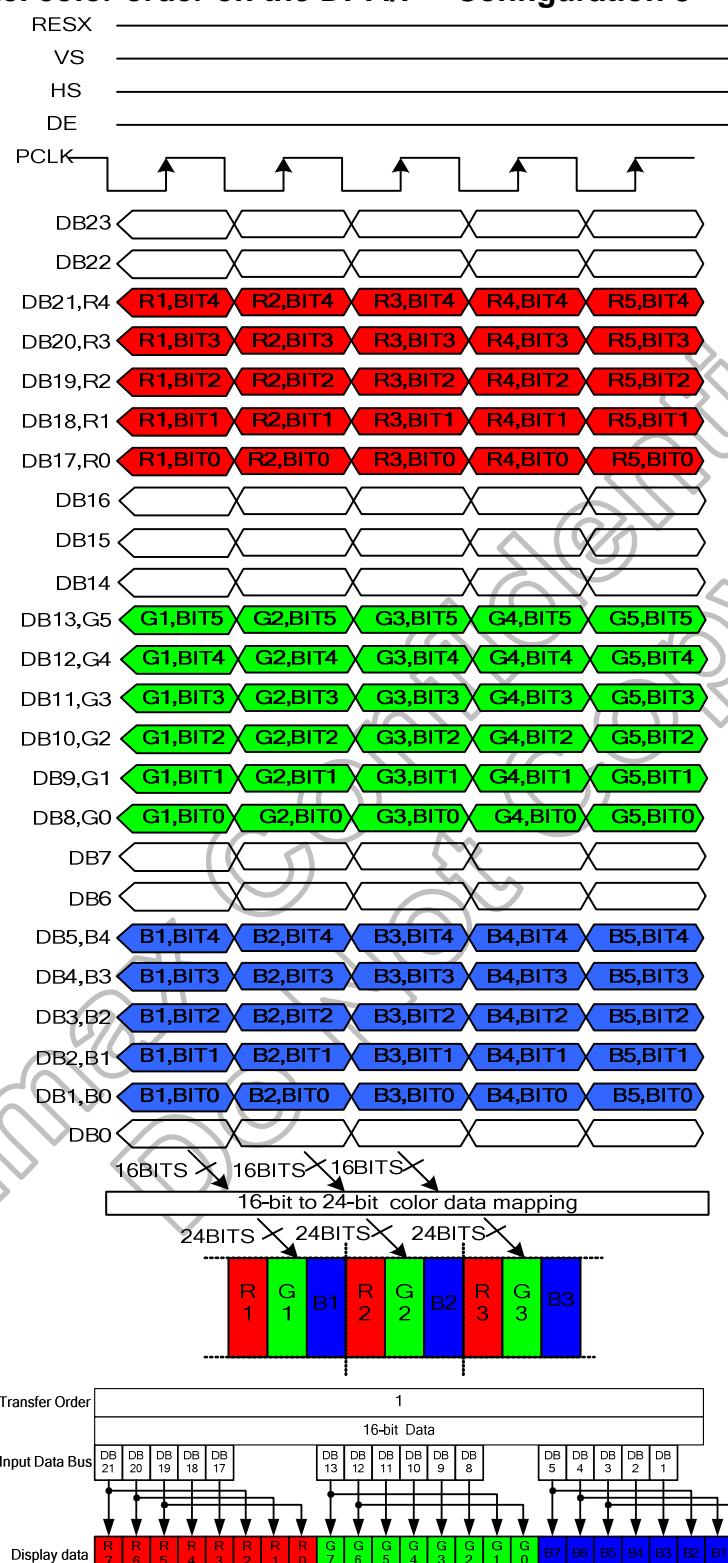
4.1.5.2 16-bit / pixel color order on the DPI I/F – Configuration 2



Note: MSB=DB23, LSB=DB0 and picture data is MSB=Bit5, LSB=Bit0 for Green data and MSB=Bit4, LSB=Bit0 for Red and Blue data.

Figure 4.19: 16-bit / pixel, 65K colours order on the DPI I/F– Configuration 2

4.1.5.3 16-bit / pixel color order on the DPI I/F – Configuration 3

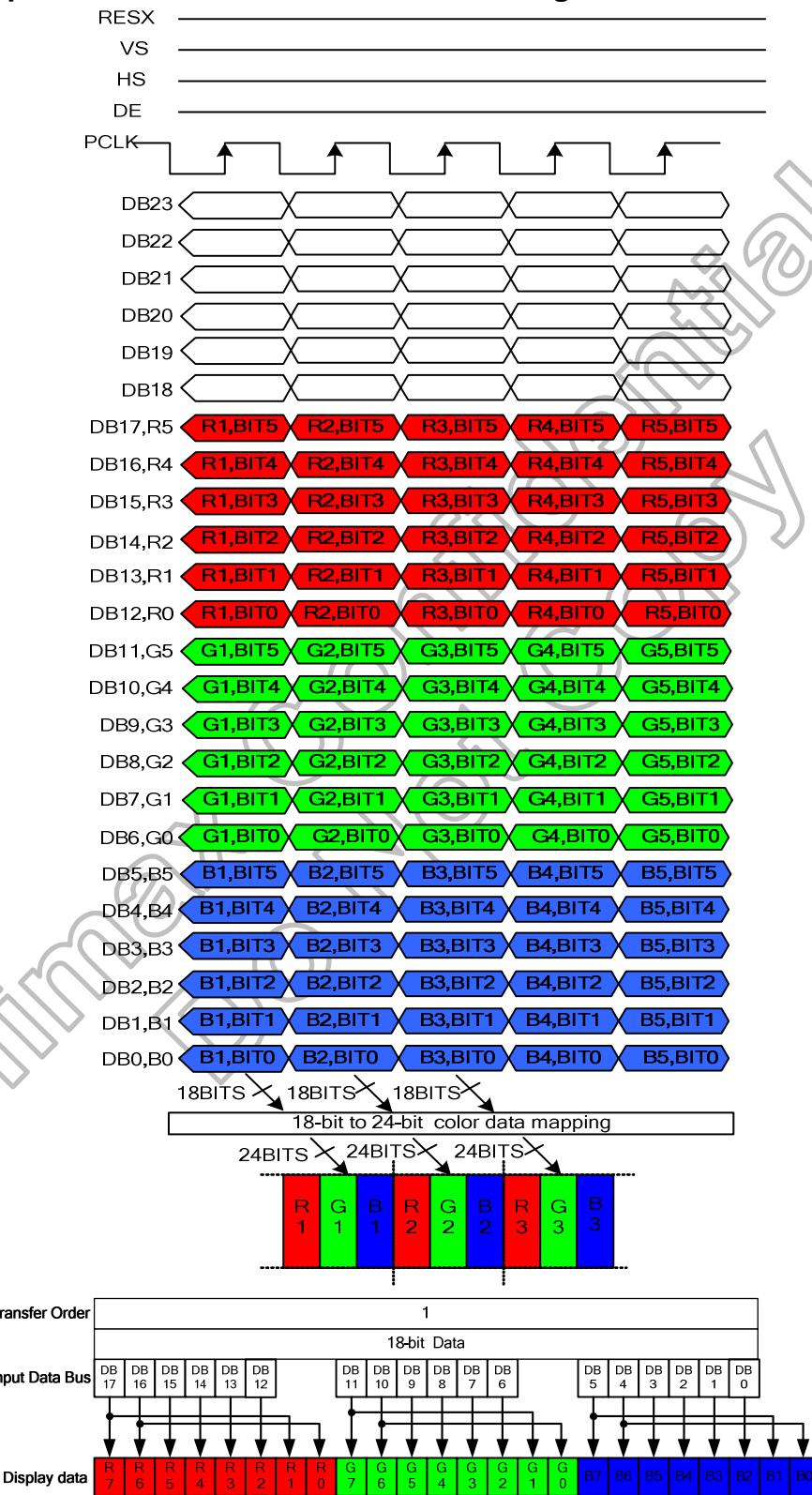


Note: MSB=DB23, LSB=DB0 and picture data is MSB=Bit5, LSB=Bit0 for Green data and MSB=Bit4, LSB=Bit0 for Red and Blue data.

Figure 4.20: 16-bit / pixel, 65K colours order on the DPI I/F– Configuration 3

4.1.6 18-bit / pixel color order on the DPI I/F

4.1.6.1 18-bit / pixel color order on the DPI I/F – Configuration 1



Note: MSB = DB23, LSB = DB0 and Picture Data is MSB = Bit5, LSB = Bit0 for Red, Green and Blue data.

Figure 4.21: 18-bit / pixel, 262k colours order on the DPI I/F– Configuration 1

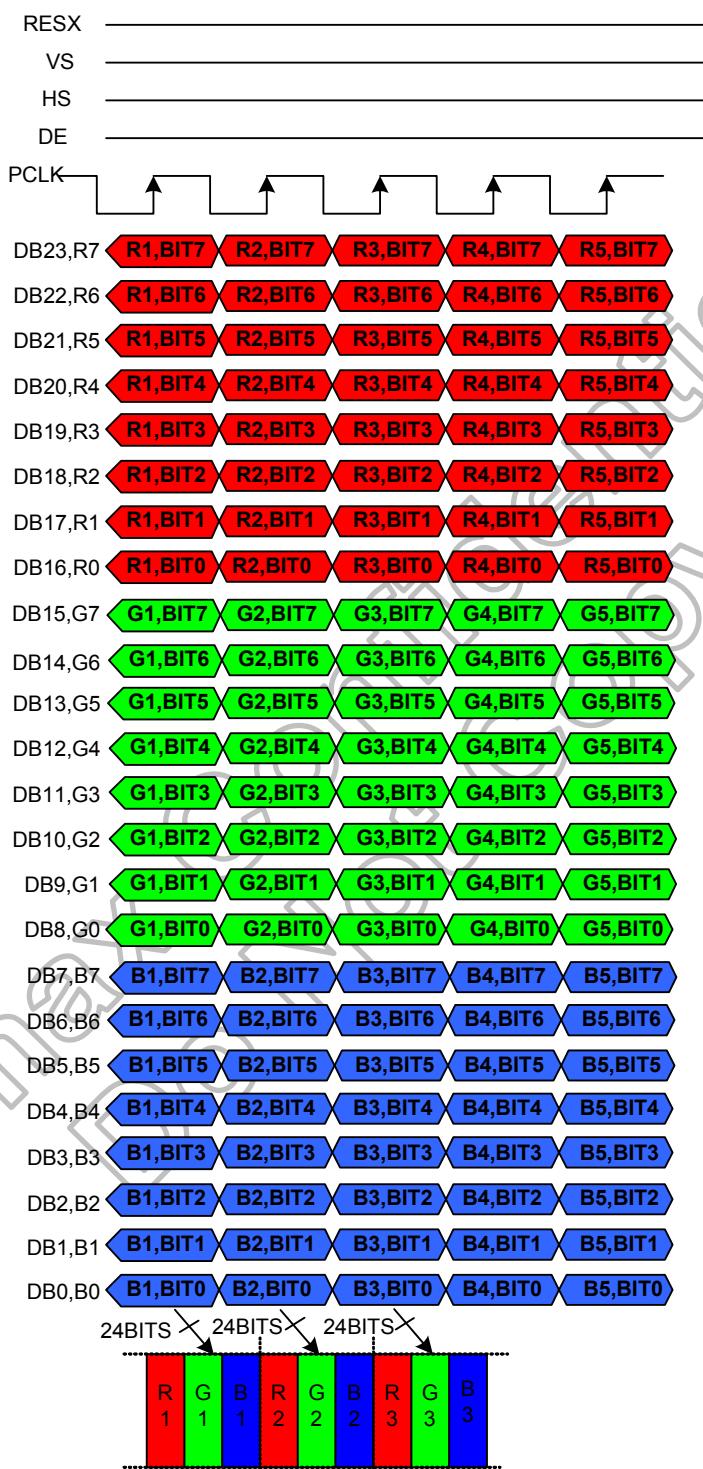
4.1.6.2 18-bit / pixel color order on the DPI I/F – Configuration 2



Note: MSB = DB23, LSB = DB0 and Picture Data is MSB = Bit5, LSB = Bit0 for Red, Green and Blue data.

Figure 4.22: 18-bit / pixel, 262k colours order on the DPI I/F– Configuration 2

4.1.7 24-bit / pixel color order on the DPI I/F



Note: MSB = DB23, LSB = DB0 and Picture Data is MSB = Bit7, LSB = Bit0 for Red, Green and Blue data.

Figure 4.23: 24-bit / pixel, 16.7M colours order on the RGB I/F

4.2 DSI system interface

The selection of interface is by IM[3:0] = "0101", the DSI specifies the interface between a host processor and a peripheral such as a display module. Figure 4.24 shows a simplified DSI interface. From a conceptual viewpoint, a DSI-compliant interface also sends pixels or commands to the peripheral, and can read back status or pixel information from the peripheral. The main difference is that DSI serializes all pixel data, commands, and events that. DSI-compliant peripherals support Command Mode. Which mode is used depends on the architecture and capabilities of the peripheral. The mode definitions reflect the primary intended use of DSI for display.

Command Mode refers to operation in which transactions primarily take the form of sending Commands and data to a peripheral, such as a display module, that incorporates a display controller. The display controller may include local registers and a frame buffer. Systems using Command Mode write to, and read from, the registers and frame buffer memory. The host processor indirectly controls activity at the peripheral by sending commands, parameters and data to the display controller. The host processor can also read display module status information or the contents of the frame memory. Command Mode operation requires a bidirectional interface.

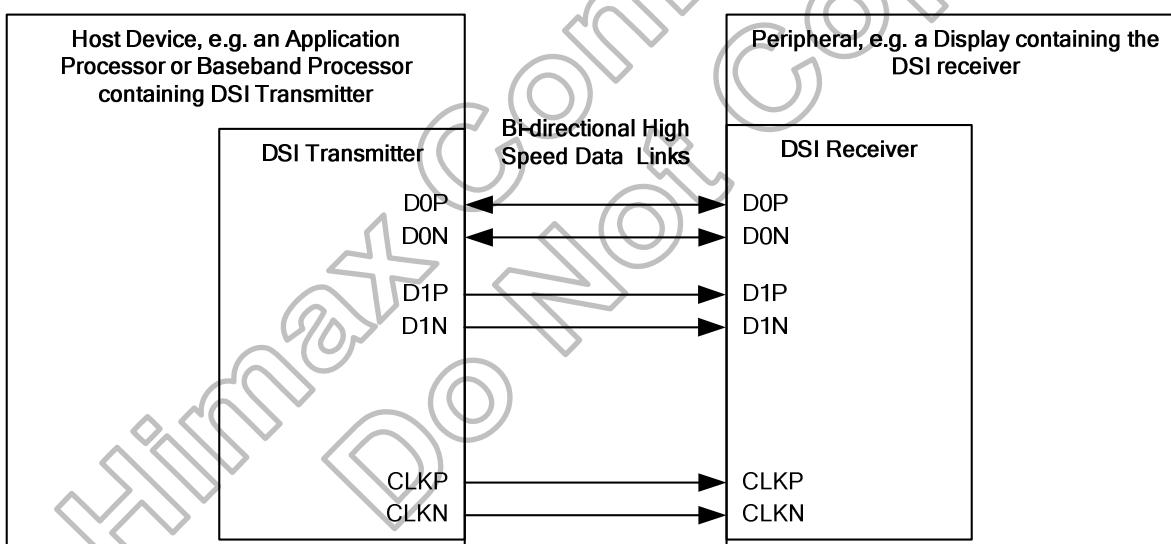


Figure 4.24: DSI transmitter and receiver interface

Please refer to “**DRAFT MIPI Alliance Standard for DSI**” for DSI detailed specifications. The data lane number is selected by HW pin: LANSEL.

4.2.1 DSI layer definitions

According Figure 4.25 DSI transmitter and Receiver interface to understand simple interface block diagram. Then under diagram is internal block for DSI which include four layers: PHY Layer, Lane Management Layer, Low level protocol and Application Layer.

The PHY Layer specifies the characteristics of transmission medium and electrical parameters for signaling the timing relationship between clock and Data Lanes.

The Lane Management Layer specifies DSI is Lane-scalable for increased performance. The data signals maybe transmission through one or more channel depending on the bandwidth requirements of the application.

The Protocol Layer specifies at the lowest level, DSI protocol specifies the sequence and value of bits and bytes traversing the interface. It specifies how bytes are organized into defined groups called packets.

The Application Layer describes higher-level encoding and interpretation of data contained in the data stream. The DSI specification describes the mapping of pixel values, commands and command's parameters to bytes in the packet assembly.

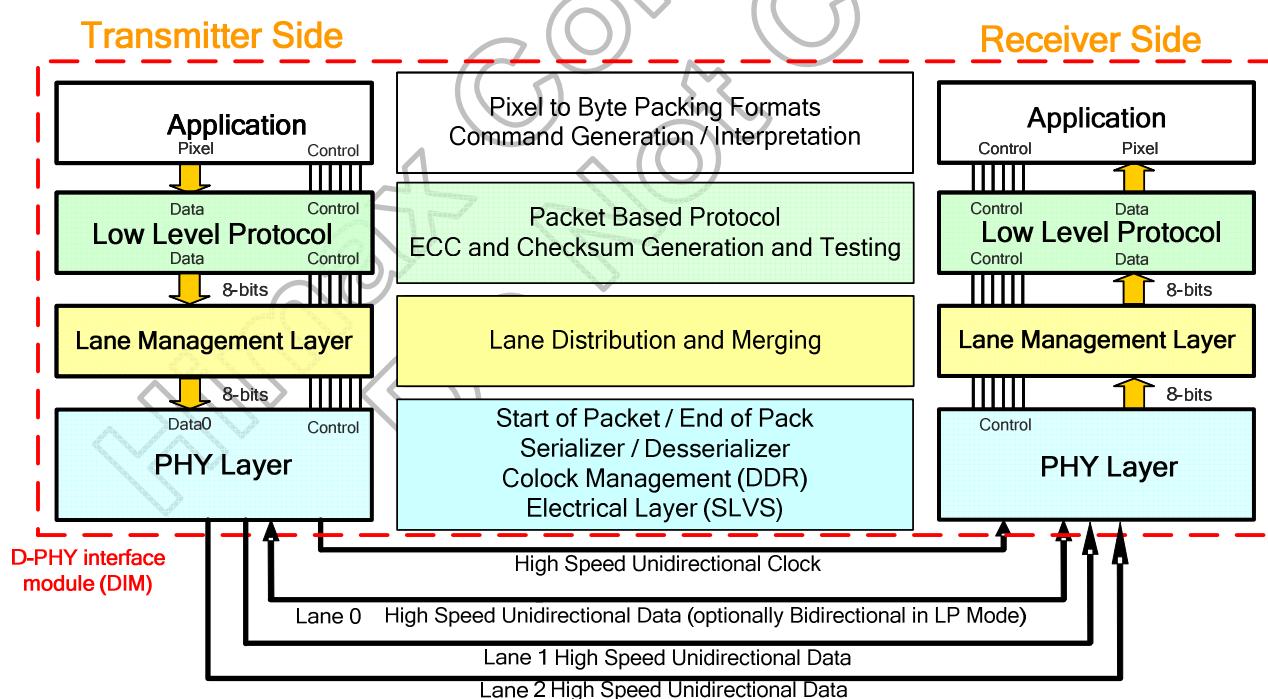


Figure 4.25: DSI transmitter and receiver interface

4.2.2 DSI protocol

The protocol layer appends packet-protocol information and headers. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands. The DSI protocol permits multiple packets which is useful for events such as peripheral initialization, where many registers may be loaded separate write commands at system startup. Figure 4.26 illustrates multiple HS Transmission packets.

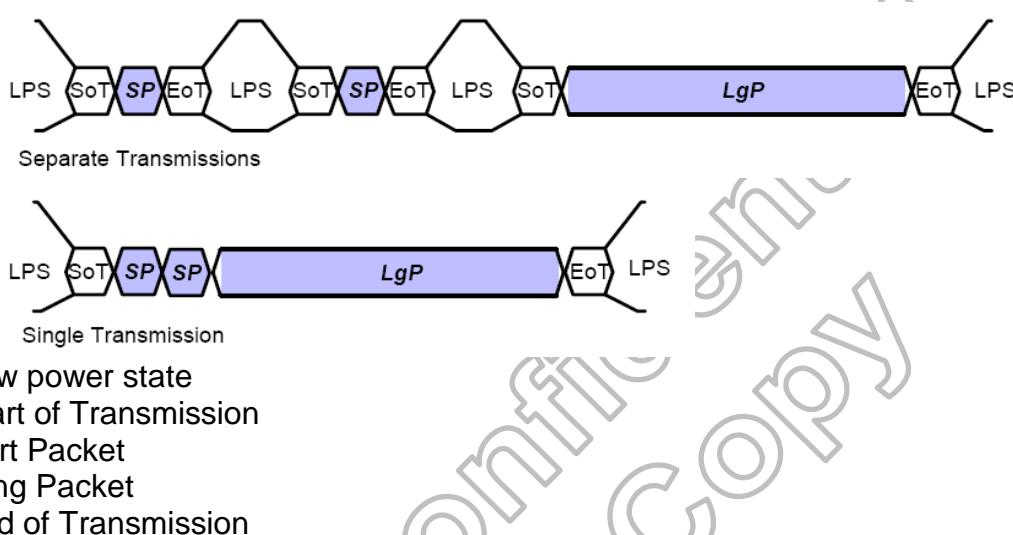
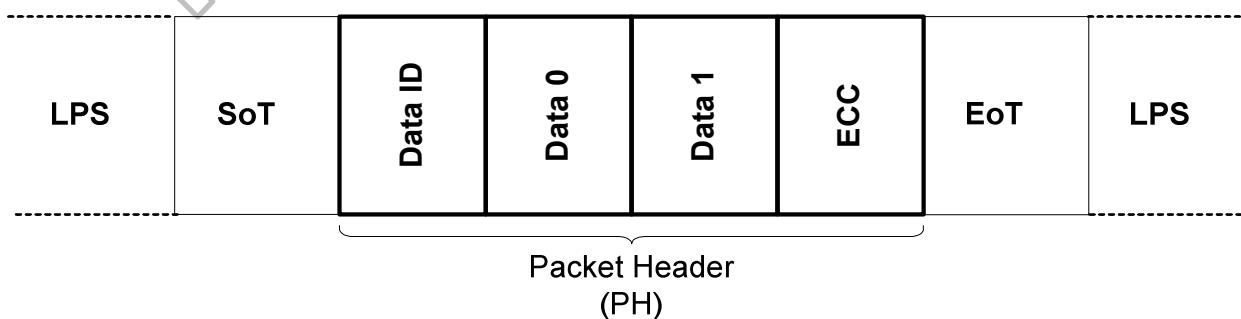


Figure 4.26: Multiple Packets Transmission

The packet includes two types which are Long packet and Short packet. The first byte of the packet, the Data Identifier (DI), includes information specifying the type of the packet. Command Mode systems send commands and an associated set of parameters, with the number of parameters depending on the command type.

Short packets are four bytes in length including the ECC. Short packet is used for most Command Mode commands and associated parameters. Where Short packets format include an 8-bit Data ID followed by two command or data and an 8-bit ECC. Figure 4.27 shows the structure of the Short packet.



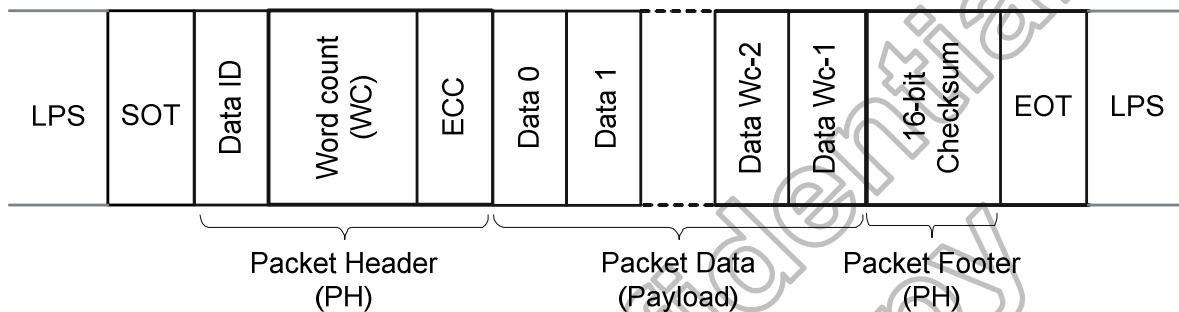
DI(Data ID) : Contain Virtual Channel Identifier and Data Type.

ECC(Error Correction Code) : The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Short packet.

Figure 4.27: Structure of the Short packet

Long packets specify the payload length using a two-byte Word Count field and then the payload maybe from 0 to 65,535 bytes in length. Long packets permit transmission of large blocks of pixel or other data. Figure 4.28 shows the structure of the Long packet. Long Packet Header composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. An application-specific Data Payload has Word Count * bytes following the Packet Header. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.

Where $65,541 \text{ bytes} = 4 \text{ bytes PH} + (2^{16}-1)\text{bytes Payload} + 2 \text{ bytes PF}$



DI (Data ID) : Contain Virtual Channel Identifier and Data Type.

WC (Word Count) : The receiver use WC to determine the packet end.

ECC (Error Correction Code) : The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.

PF(Packet Footer) : Mean 16-bit Checksum.

Figure 4.28: Structure of the long packet

According to packet form, basic elements include DI and ECC. Figure 4.29 the shows format of Data ID.

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
VC (Virtual Channel)	DT (Data Type)						

DI[7:6] → These two bits identify the data as directed to one of four virtual channels.
DI[5:0]: These six bits specify the Data Type.

Figure 4.29: The format of data ID

Due to Data Type (DT) mean format of transmission type, Figure 4.30 show Short- / Long-packet transmission command sequence.

Long packet write Command / Parameters / Pixel Data



DI -> Write suitable Data type.

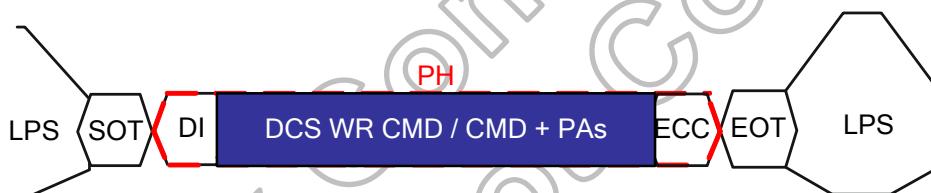
WC -> Write number of Payload Data.

Ex: One CMD write, WC setting as 1.

CMD + PAs write, WC setting as number of (CMD+PAs).

CMD + DATA write, WC setting as number of (CMD + Pixel DATA).

Short packet write Command / Parameters



DI è Write suitable Data type.

Ex: One CMD write, DI + DCS WR CMD

CMD + PAs write, DI + DCS WR CMD + PAs

Figure 4.30: Show short- / long-packet transmission command sequence

4.2.3 Processor to peripheral (forward direction) packets data types

The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown in Table 4.5 Data Types for Processor-sourced Packets.

Data type, hex	Data type, binary	Description packet	Size
01h	00 0001	Sync Event, V Sync Start	Short
11h	01 0001	Sync Event, V Sync End	Short
21h	10 0001	Sync Event, H Sync Start	Short
31h	11 0001	Sync Event, H Sync End	Short
08h	00 1000	End of Transmission packet(EoTp)	Short
05h	000101	DCS WRITE, no parameter	Short
15h	010101	DCS WRITE, 1 parameter	Short
06h	00 0110	DCS READ, no parameters	Short
37h	11 0111	Set Maximum Return Packet Size	Short
09h	00 1001	Null Packet, no data	Long
19h	01 1001	Blanking Packet, no data	Long
39h	11 1001	DCS Long Write/write_LUT Command Packet	Long
0Eh	00 1110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format	Long
1Eh	01 1110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
2Eh	10 1110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	Long
3Eh	11 1110	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	Long
X0h and XFh, unspecified	xx 0000 xx 1111	DO NOT USE All unspecified codes are reserved	-

Table 4.5: Data types for processor-sourced packets

Under tables list all detail function of all data types

Sync event (H start, H end, V start, V end), data type=xx 0001 (x1h)		
Data type, hex	Function description	Number of bytes
01h	V Sync start, Start of VSA pulse.	4 bytes (DI+00h+00h+ECC)
11h	V Sync End, End of VSA pulse.	
21h	H Sync Start, Start of HSA pulse.	
31h	H Sync End, End of HSA pulse.	
Note: V Sync Start and V Sync End event represents the start and end of the VSA, respectively. Similarly H Sync Start and H Sync End event represents the start and end of the HSA, respectively.		

Display status (shutdown command, turn-on command)		
Data type, hex	Function description	Number of bytes
22h	Shutdown Peripheral command that turns off the display in a Video Mode display for power saving.	4 bytes (DI+00h+00h+ECC)
32h	Turn On Peripheral command that turns on the display in Video Mode display for normal display.	
Note: When use shutdown command, interface shall remain powered in order to receive the turn-on, or wake-up, command.		

DCS command setting		
Data type, hex	Function description	Number of bytes
06h	DCS Read command, the returned data shall be Long packet format.	4 bytes (DI+Data0+Data1+ECC)
05h and 15h	DCS Short Write command, 0 or 1 parameter, Data Types = 00 0101(05h), 01 0101 (15h), Respectively.	4 bytes (DI+Data0+Data1+ECC)
39h	DCS Long Write/ Write _ LUT Command is used to send larger blocks of data to a display module that implements the Display Command Set.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)

Note: (1) For write part, If DCS Short Write command, followed by BTA, the peripheral shall respond with ACK when without error was detected in the transmission (Host → Slave). Unless an error was detected, the peripheral shall respond with Acknowledge with Error Report.

For example: 05h DCS WRITE for no parameter command set.

05h	CMD	0	ECC
-----	-----	---	-----

Ex. 05h, 29h, 00, 1Ch ↴ Display On(29h)

For example: 15h DCS WRITE for only one parameter command set.

15h	CMD	Par	ECC
-----	-----	-----	-----

Ex. 15h, 36h, 08h, 11h ↴ MADCTL(36h)-BGR bit=1

- (2) When use DCS Read Command, the Set Max Return Packet Size command will limit the size of returning packets.
- (3) The peripheral shall respond to DCS Read Command Request in one of the following ways:
 - ◆ If an error was detected by the peripheral, it shall send *Acknowledge with Error Report*. So the peripheral shall transmit the requested READ data packet with suitable ECC in the same transmission.
 - ◆ If no error was detected by the peripheral, it shall send the requested READ packet (Short or Long) with appropriate ECC and Checksum, if either or both features are enabled.
- (4) One byte <= Length of payload DATA <= $2^{16}-1$

Maximum Return packet size setting

Data type, hex	Function description	Number of bytes
37h	Set Maximum Return Packet Size that specifies the maximum size of the payload in a Long packet transmitted from peripheral back to the host processor.	4 bytes (DI + Maximum Return Packet Size + ECC)

Note: The two-byte value is transmitted with LS byte first. And during a power-on or Reset sequence, the Maximum Return Packet Size shall be set by the peripheral to a default value of one.

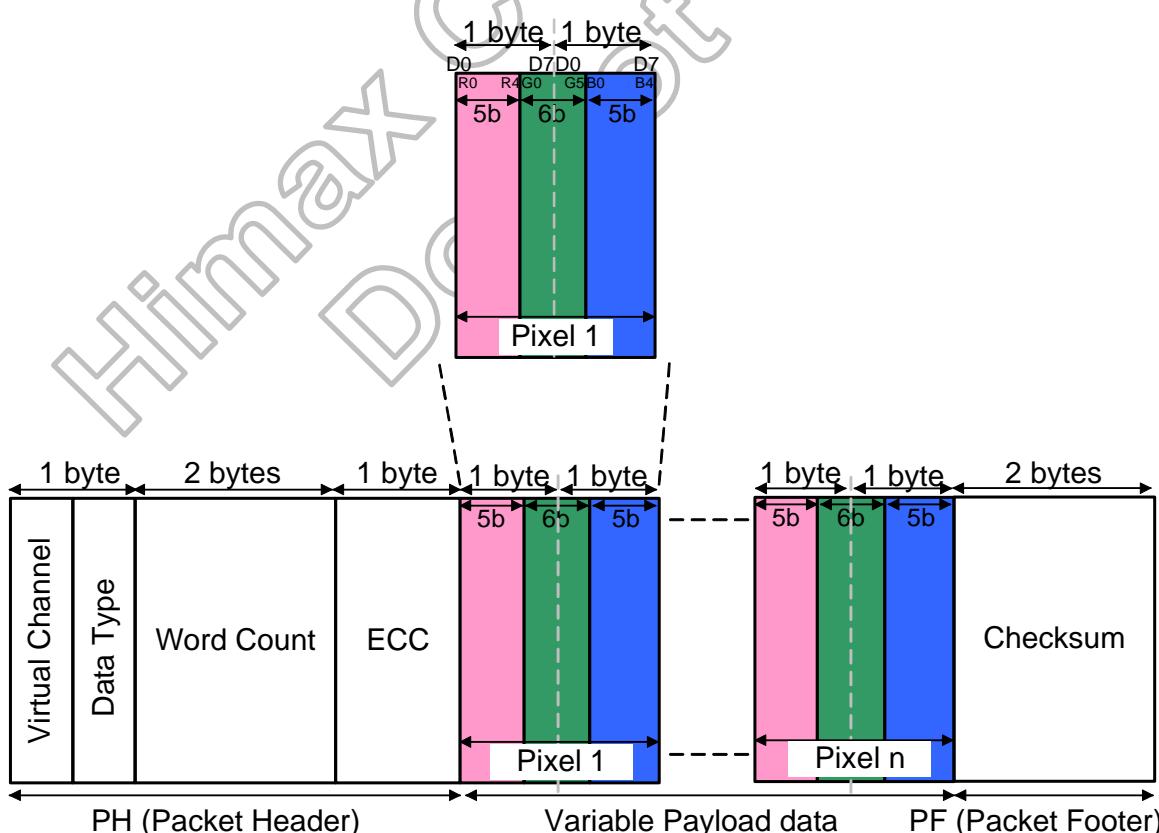
Variable data packet

Data type, hex	Function description	Number of bytes
09h	Null Packet is a mechanism for keeping the serial Data Lane(s) in High-Speed mode while sending dummy data.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)
19h	Blanking packet is used to convey blanking timing information in a Long packet.	

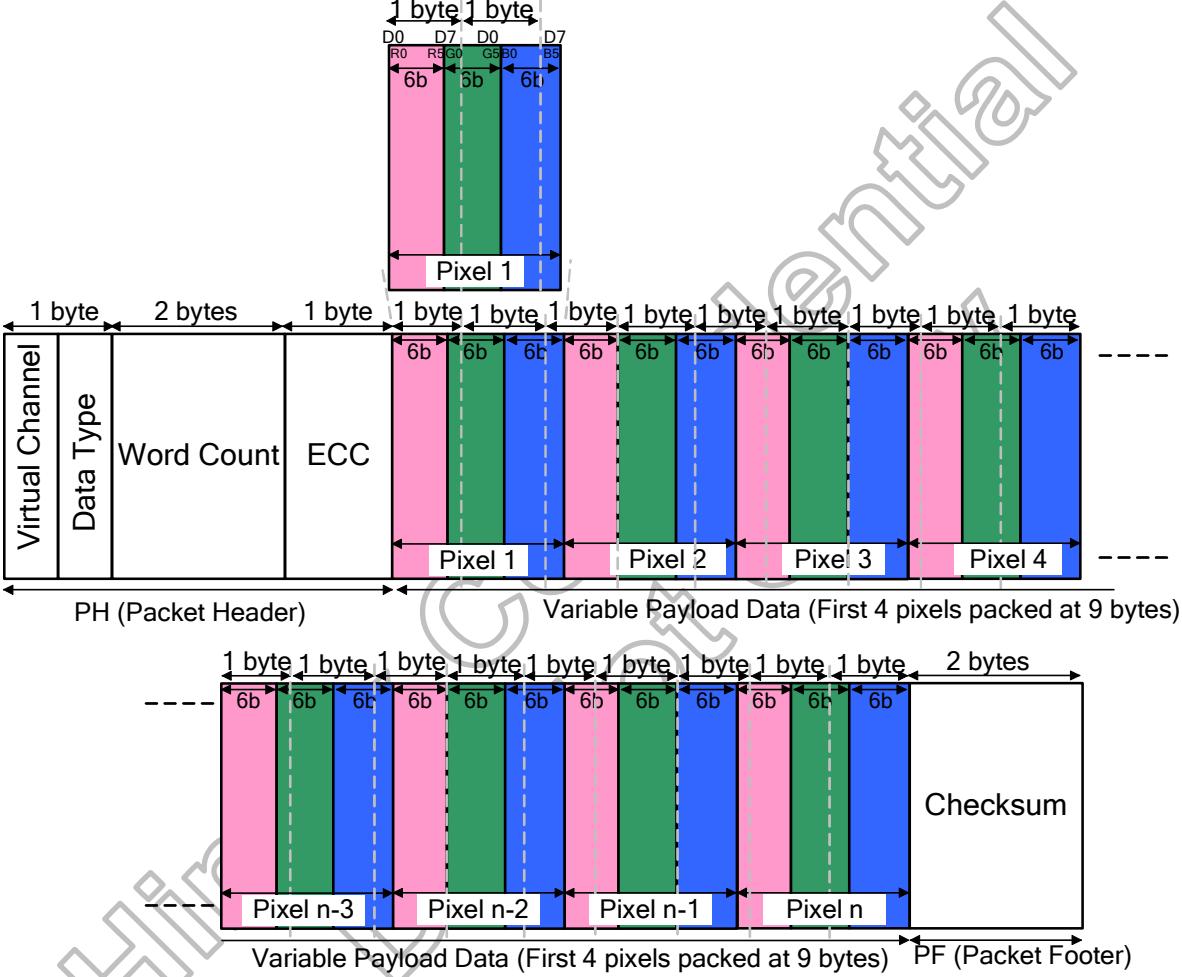
Note: (1) When Null Packet, the Payload Data belong "null" Data, actual data values sent are irrelevant because the peripheral does not capture or store the data.
(2) When Blanking packet, the packet represents a period between active scan lines of a Video Mode display,

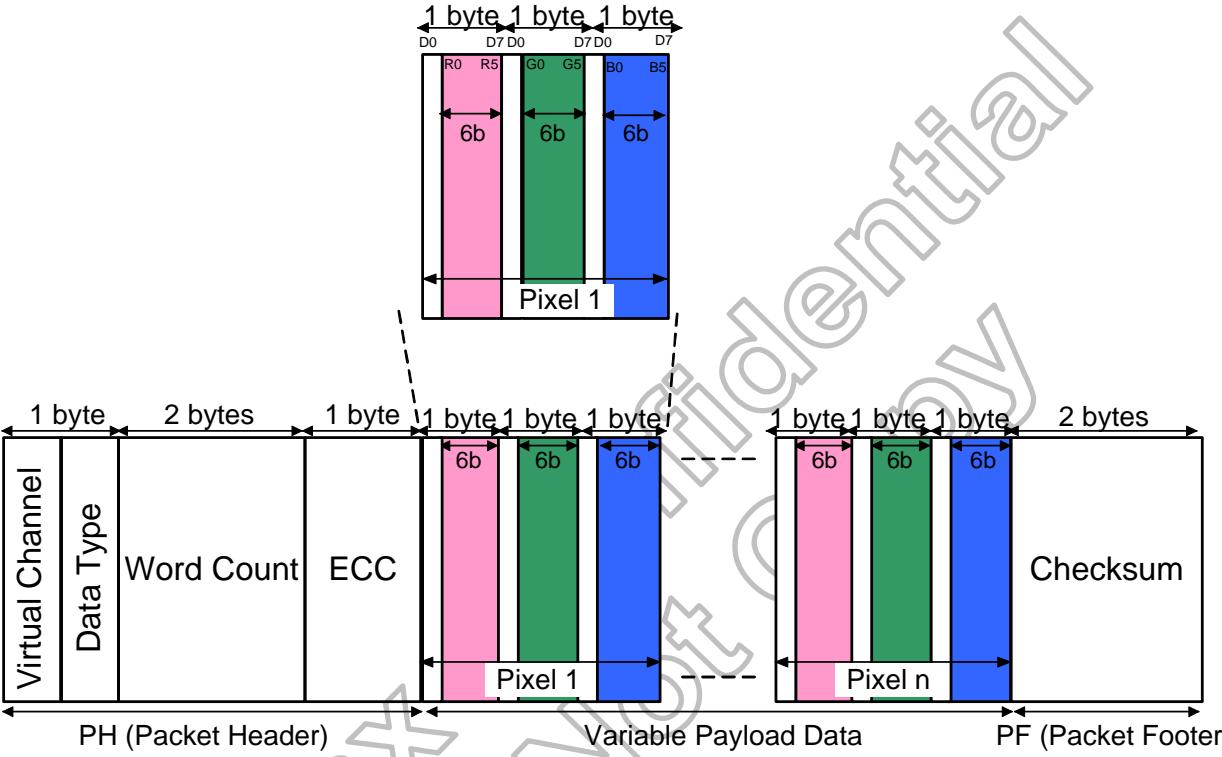
Data stream format

Data type, hex	Function description	Number of bytes
0Eh	Packed Pixel Stream 16-Bit Format is used to transmit image data formatted as 16-bit pixels to a Video Mode display module. Pixel format is "(5 bits) red, (6 bits) green and (5 bits) blue".	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)

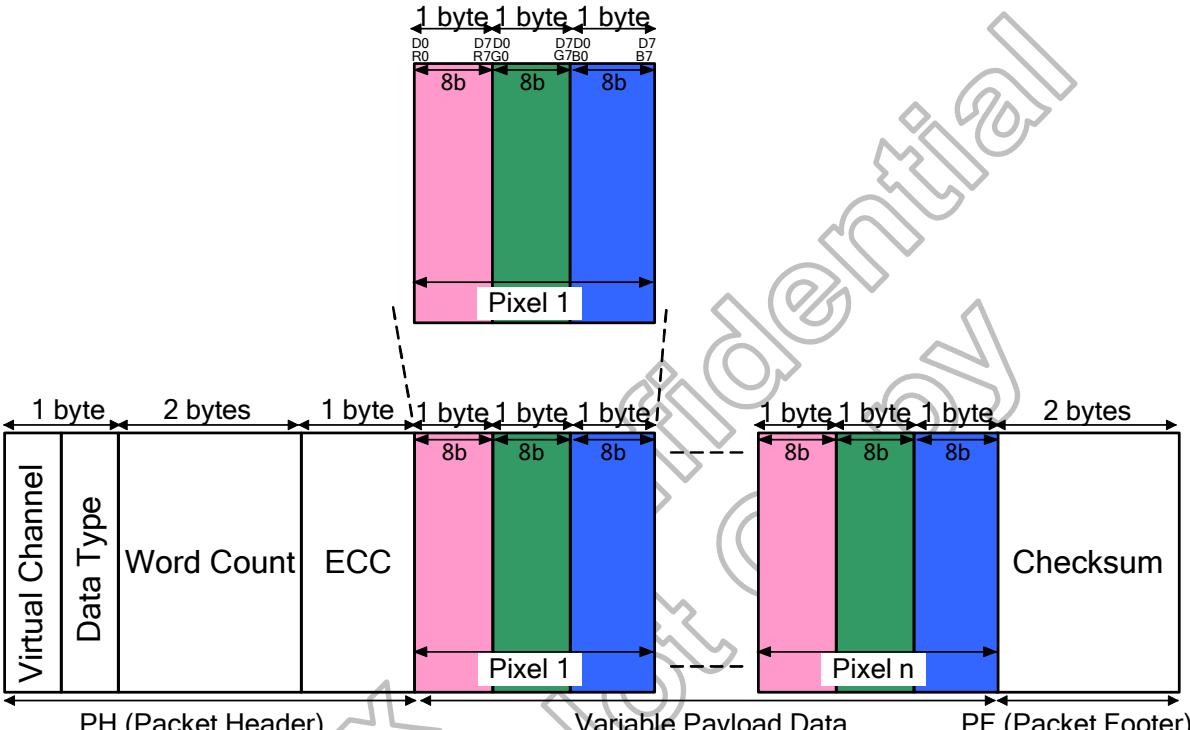


Note: Within a color component, the "LSB is sent first, the MSB last".

Data stream format		
Data type, hex	Function description	Number of bytes
1Eh	Packed Pixel Stream 18-Bit Format is used to transmit image data formatted as 18-bit pixels to a Video Mode display module. Pixel format is "(6 bits) red, (6 bits) green and (6 bits) blue".	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)
 <p>The diagram illustrates the data stream format. It starts with a PH (Packet Header) containing fields for Virtual Channel (1 byte), Data Type (2 bytes), and Word Count (1 byte). Following the header is the ECC (Error Correction Code). The main payload consists of Variable Payload Data, which is divided into two sections: 'First 4 pixels packed at 9 bytes' and 'Variable Payload Data (First 4 pixels packed at 9 bytes)'. Each pixel is represented by three 6-bit color components (Red, Green, Blue). A dashed line indicates the continuation of the payload. The final section is the PF (Packet Footer), which contains a 2-byte Checksum.</p>		
<p>Note: Within a color component, the LSB is sent first and the MSB last and pixel boundaries only line up with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. It is possible to send pixel data that represent a line width that is not a multiple of four pixels, but display logic on the receiver end shall dispose of the extra bits of the partial byte at the end of active display and ensure a "clean start" for the next line.</p>		

Data stream format		
Data type, hex	Function description	Number of bytes
2Eh	Packed Pixel Stream 18-Bit Format, each R, G, or B color component is one byte form, but the valid pixel bits occupy bits [7:2] and bits [1:0] of are ignored. Pixel format is "(6 bits) red, (6 bits) green and (6 bits) blue".	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)
 <p>The diagram illustrates the data stream format. At the top, a detailed view of a single pixel (Pixel 1) shows its 6-bit components (R0-R5, G0-G5, B0-B5) and their byte boundaries (D0-D7). Below this, the payload is shown as a sequence of pixels (Pixel 1 to Pixel n), each with its own 6-bit components and byte boundaries. The packet structure is divided into sections: PH (Packet Header) containing Virtual Channel, Data Type, Word Count, and ECC; Variable Payload Data containing the sequence of pixels; and PF (Packet Footer) containing a Checksum.</p>		

Note: Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

Packed pixel stream, 24-bit format		
Data type, hex	Function description	Number of bytes
3Eh	Packed Pixel Stream 24-Bit Format is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. Pixel format is (8 bits) red, (8 bits) green and (8 bits) blue.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)
 <p>The diagram illustrates the structure of a packed pixel stream packet. It is divided into three main sections: PH (Packet Header), Variable Payload Data, and PF (Packet Footer).</p> <ul style="list-style-type: none"> PH (Packet Header): Contains fields for Virtual Channel (1 byte), Data Type (2 bytes), Word Count (1 byte), and ECC (1 byte). Variable Payload Data: Contains multiple pixels. Each pixel is 24 bits wide, divided into 8 bits Red (R), 8 bits Green (G), and 8 bits Blue (B). The bytes are transmitted from D0 to D7. A specific pixel is labeled "Pixel 1". PF (Packet Footer): Contains a 2-byte Checksum field. <p>A note at the bottom states: "Note: Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes."</p>		

4.2.4 Peripheral to processor (reverse direction) packet data type

All Command Mode systems require bidirectional capability for returning READ data, ACK or error information to the host processor. Command Mode that use DCS shall have a bidirectional data path. Short packets and the header of Long packets shall use ECC and may use Checksum to provide a higher level of data integrity. The Checksum feature enables detection of errors in the payload of Long packets. The packet structure for peripheral-to-processor transactions is the same as for the processor-to-peripheral direction.

Peripheral-to-processor transactions are of four basic types:

- A. *Tearing Effect* is a Trigger message sent to convey display timing information to the host processor. Trigger messages are single byte packets sent by a peripheral's PHY layer in response to a signal from the DSI protocol layer.
- B. *Acknowledge* is a Trigger Message sent when the current transmission, as well as all preceding transmissions since the last peripheral to host communication is received by the peripheral with no errors.
- C. *Acknowledge and Error Report* is a Short packet sent if any errors were detected in preceding transmission from the host processor. Once reported, accumulated errors in the error register are cleared.
- D. *Response to Read Request* may be Short or Long packet that returns data requested by the preceding READ command from the processor.

In general, if the host processor completes a transmission to the peripheral with BTA asserted, the peripheral shall respond with one or more appropriate packet(s), and then return bus ownership to the host processor. If BTA is not asserted following a transmission from the host processor, the peripheral shall not communicate an Acknowledge or other error information back to the host processor.

The processor-to-peripheral transactions with BTA asserted, can contain under form.

- A. Following a non-Read command in which no error was detected, the peripheral shall respond with Acknowledge.
- B. Following a Read request in which no error was detected, the peripheral shall send the requested READ data.
- C. Following a Read request in which the ECC error was detected and corrected, the Peripheral shall send the requested READ data in a Long or Short packet, followed by a 4-byte (Acknowledge with Error Report) packet in the same LP transmission. The Error Report shall have the ECC Error flag set.
- D. Following a non-Read command in which the ECC error was detected and corrected, the peripheral shall proceed to execute the command, and shall respond to BTA by sending a 4-byte (Acknowledge with Error Report) packet, the Error Report shall have the ECC Error flag set.
- E. Following any command in which SoT Error, SoT Sync Error, EoT Sync Error, LP Transmit Sync Error, checksum error or DSI VC ID Invalid was detected, or the DSI command was not recognized, the peripheral shall send a 4-byte Acknowledge with Error Report response, with the appropriate error flags set in the two-byte error field. Only the ACK/Error Report packet shall be transmitted; no read or write accesses shall take place on the peripheral in response.

Which,

- A. "Acknowledge" is sent using a Trigger message which is one byte: 00100001
- B. "Acknowledge with Error Report" include 4 bytes which are DI, 2 bytes Error report and ECC.
- C. "Response to Read Request" are Long packet format.

An error report is comprised of two bytes following the DI byte, with an ECC byte following the error report bytes. Table 4.6 shows the Error Report Bit Definitions. And Table 4.7 lists complete set of peripheral-to-processor Data Types.

Bit	Description
0	SoT Error
1	SoT Sync Error
2	Reserved
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Peripheral Timeout Error
6	Reserved
7	Reserved
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (long packet only)
11	DSI Data Type Not Recognized
12	DSI VC ID Invalid
13	Reserved
14	Reserved
15	Reserved

Table 4.6: Shows the error report bit definitions

Data type, hex	Data type, binary	Description packet	Size
02h	00 0010	Acknowledge with Error Report	Short
1Ch	01 1100	DCS Long READ Response	Long
Others (00h→3Fh)		Reserved	-

Table 4.7: Complete set of peripheral-to-processor data types

Acknowledge types		
Data type, hex	Function description	Number of bytes
02	Get Acknowledge with Error report when Error occurs from processor transmission.	4 bytes

Note: When processor transmits complete Payload, following signal by BTA, peripheral must respond to processor.
With error → Acknowledge with error report (Short packet), Without error → request READ data or Acknowledge (trigger message).

DCS Read types		
Data type, hex	Function description	Number of bytes
1Ch	This is the Long-packet response to DCS Long Read Request.	Up to 65541 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)

Note: (1)If the peripheral is Checksum capable, it shall return a calculated two-byte Checksum appended to the N-byte payload data. If the peripheral does not support Checksum, it shall return 0000h.
If the DCS command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent after the Acknowledge with Error Report packet be sent.
(2)There is no dummy read byte in the read response packet.

5. Function Description

5.1 Tearing effect output line

The Tearing Effect output line supplies a panel synchronization signal to the MPU. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize frame memory writing when displaying video images.

5.1.1 Tearing effect line modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:

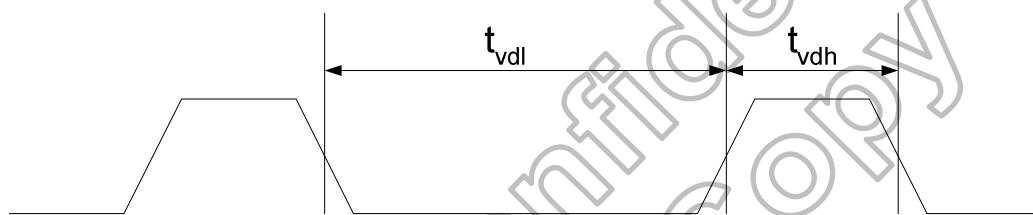


Figure 5.1: Tearing effect output signal mode 1

tvdh= The LCD display is not updated from the Frame Memory

tvdl= The LCD display is updated from the Frame Memory (except Invisible Line – see below)

Under Mode1, the TE output timing will be defined by TEP[9:0] setting.

Ex: 1. FB=BP=0x01h (3 line) .

TEP[9:0]=0, then TE signal will output after last Line finished.

TEP[9:0]=7, then TE signal will output at second Line start.

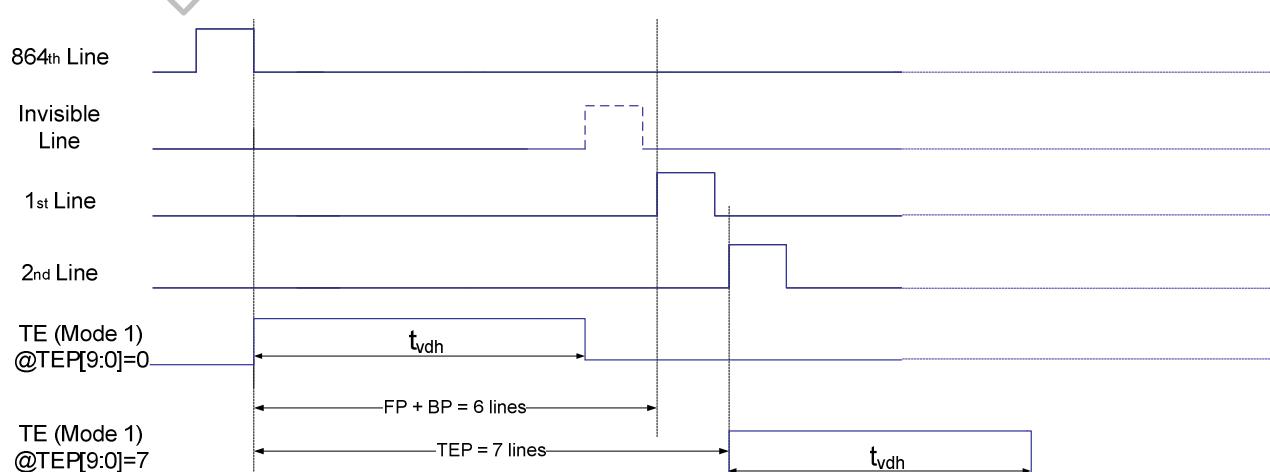


Figure 5.2: TE delay output

5.1.2 Tearing effect line timing

The tearing effect signal is described below :

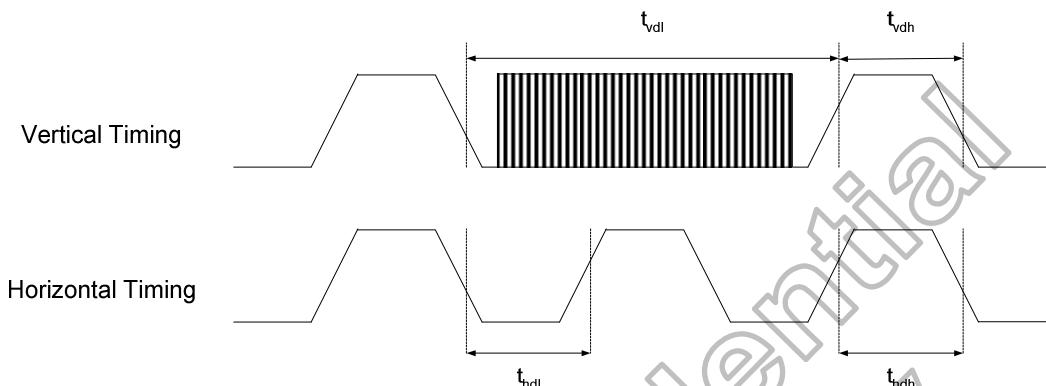


Figure 5.3: Tearing effect line timing

Idle mode off (Frame rate=60Hz)

Symbol	Parameter	Min.	Max.	Unit	description
tvdl	Vertical Timing Low Duration	15	-	ms	-
tvdh	Vertical Timing High Duration	VFP+VHP+VBP	-	us	-
thdl	Horizontal Timing Low Duration	-	15	us	-
thdh	Horizontal Timing High Duration	-	15	us	-

Note: The timings in Table 5.1 apply when MADCTL ML=0 and ML=1

Table 5.1: AC characteristics of tearing effect signal

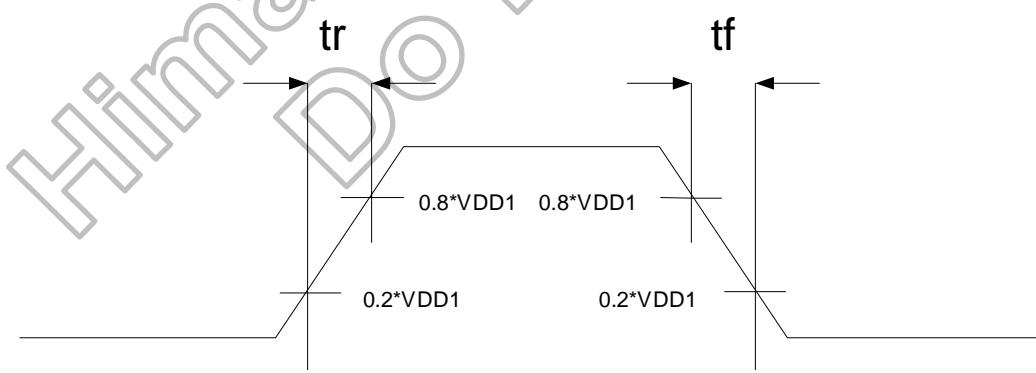


Figure 5.4: Rise and fall times of TE signal

The tearing effect output Line is fed back to the MPU and should be used as shown below to avoid tearing effect :

5.2 Oscillator

The HX8379-A can oscillate an internal R-C oscillator with an internal oscillation resistor (R_f). The oscillation frequency is changed according to the UADJ[3:0] internal register. Please refer to OSC control register (RB0h). The default frequency is 15MHz.

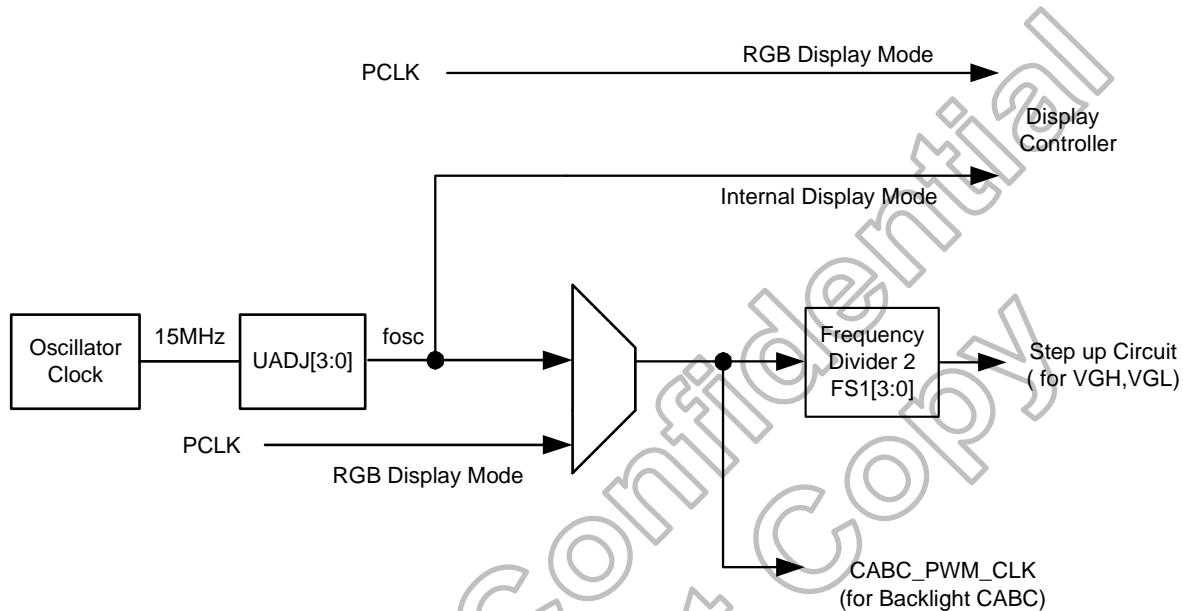


Figure 5.5: OSC architecture

5.3 Source driver

The HX8379-A contains a 1442 channels of source driver which is used for driving the source line of TFT LCD panel. The source driver converts the digital data into the analog voltage for 1442 channels and generates corresponding gray scale voltage output, which can realize a 16.7M colors display simultaneously. Since the output circuit of this source driver incorporates an operational amplifier, a positive and a negative voltage can be alternately outputted from each channel.

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5.3.1 Zig-Zag Inversion

The HX8379-A supports Zig-Zag inversion which can reduce power consumption. This inversion uses the same polarity as column inversion for data line and has almost the same display quality as 1-dot inversion. Using SDUM1 as S0, SDUM2 as S1441.



Figure 5.6: Normal type and Zig-Zag type panel

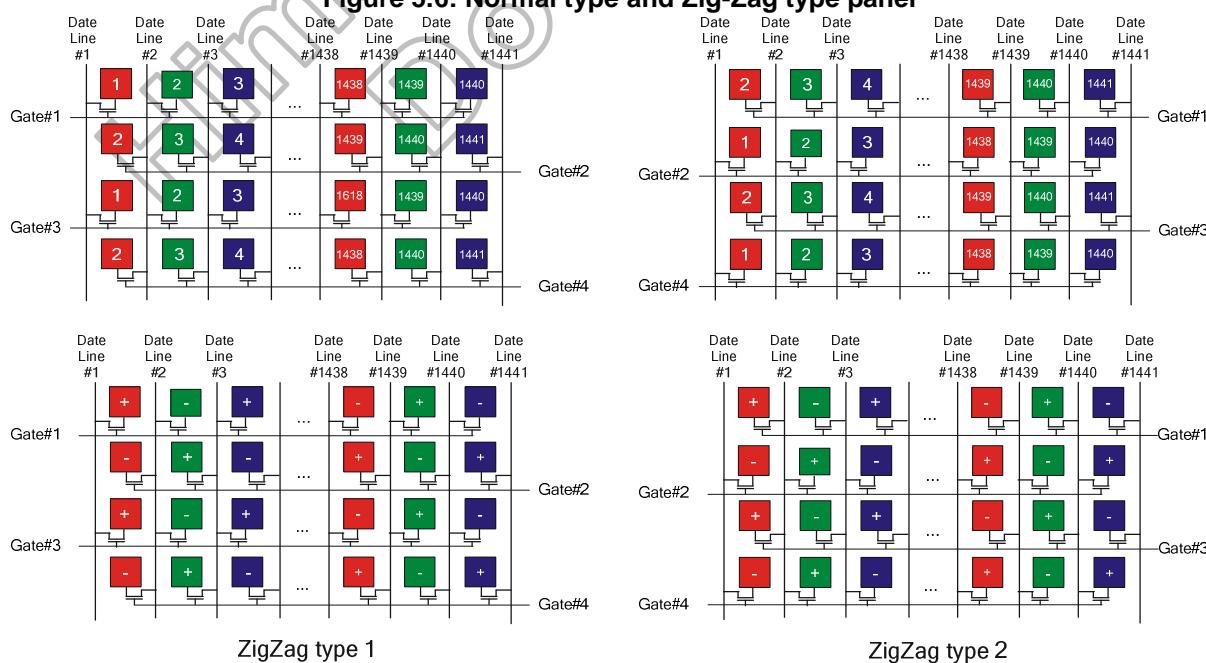


Figure 5.7: Different Zig-Zag type panel

5.3.2 Display red color by using Zig-Zag inversion

To display red color by using zig-zag inversion. The input date line 1/4/7...1435/1438 must send red color data for odd gates. And the input date line 2/5/8...1436/1439 must send red color data for even gates.

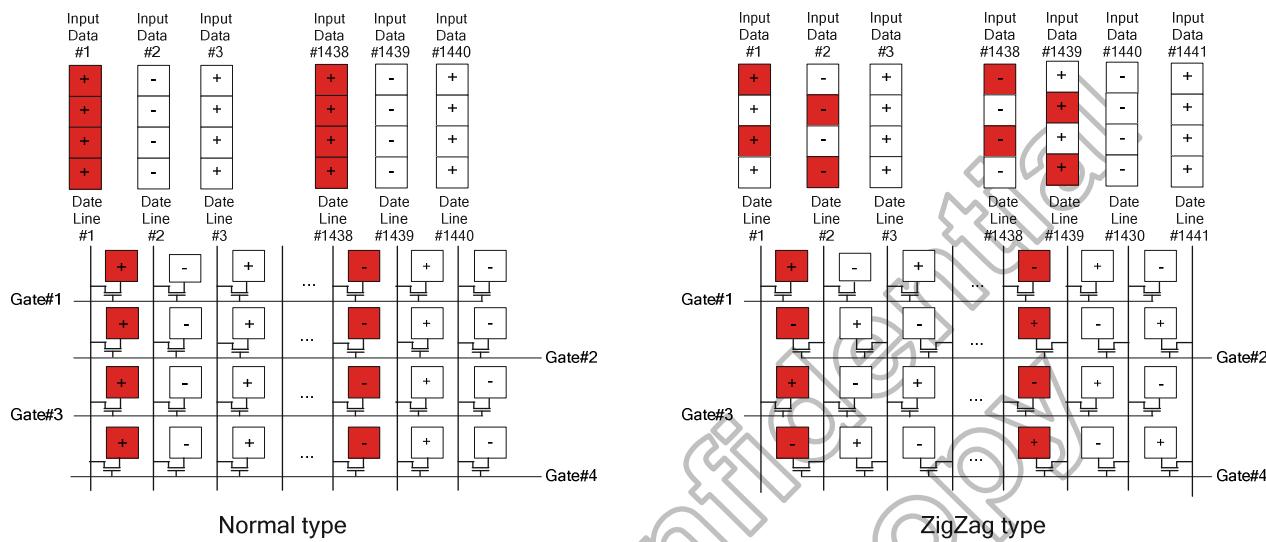


Figure 5.8: The method to display Red color(type 1)

5.3.3 Display green color by using Zig-Zag inversion

To display green color by using zig-zag inversion. The input date line 2/5/8...1436/1436 must send green color data for odd gates. And the input date line 3/6/9...1437/1440 must send green color data for even gates.



Figure 5.9: The method to display Green color(type 1)

5.3.4 Display blue color by using Zig-Zag inversion

To display blue color by using zig-zag inversion. The input date line 3/6/9...1437/1440 must send blue color data for odd gates. And the input date line 4/7/10...1438/1441 must send blue color data for even gates.

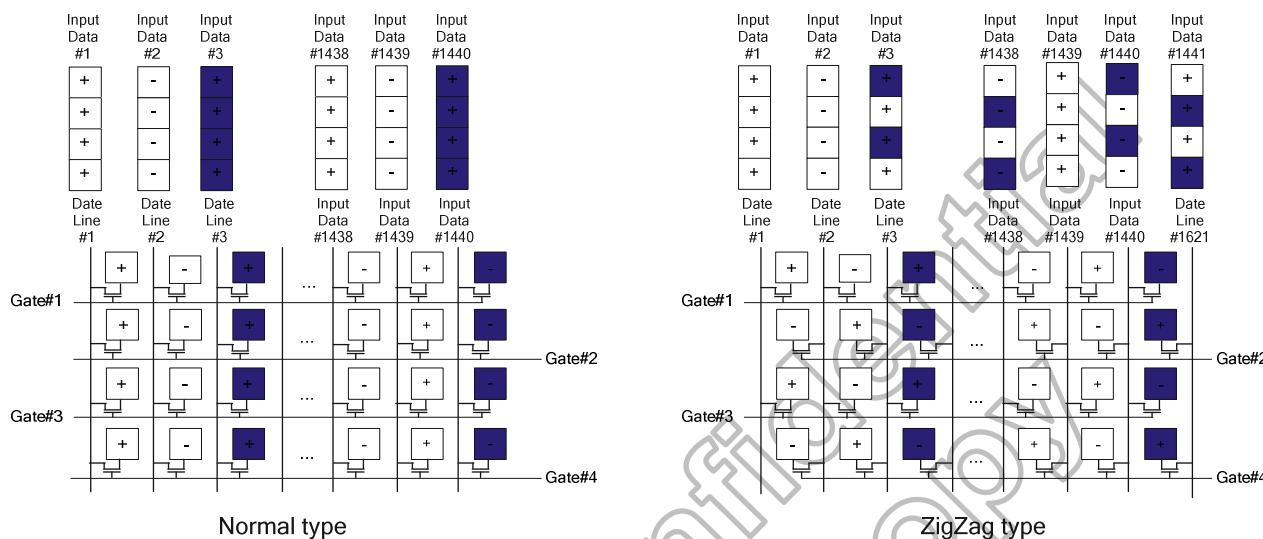


Figure 5.10: The method to display Blue color(type 1)

5.4 LCD power generation scheme

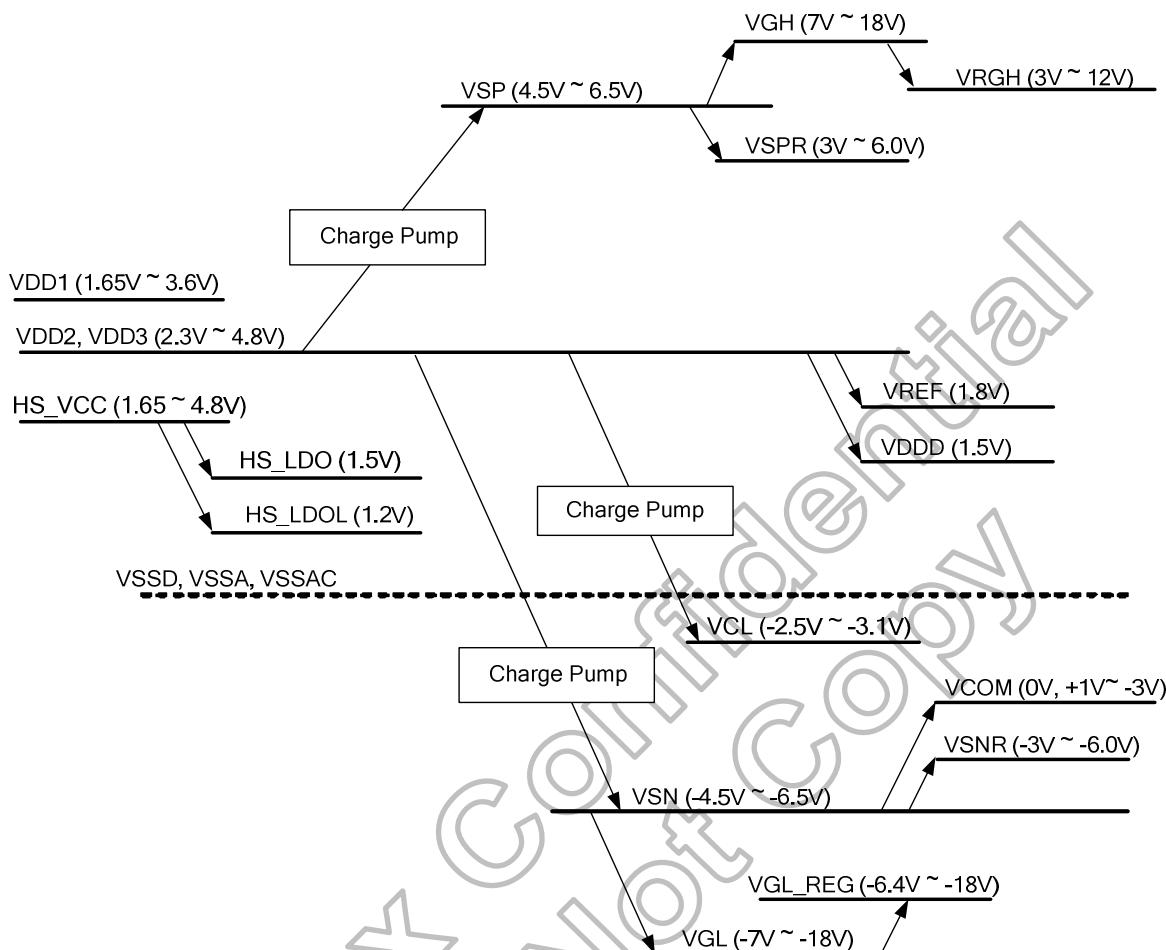


Figure 5.11: LCD power generation scheme

Voltage configuration

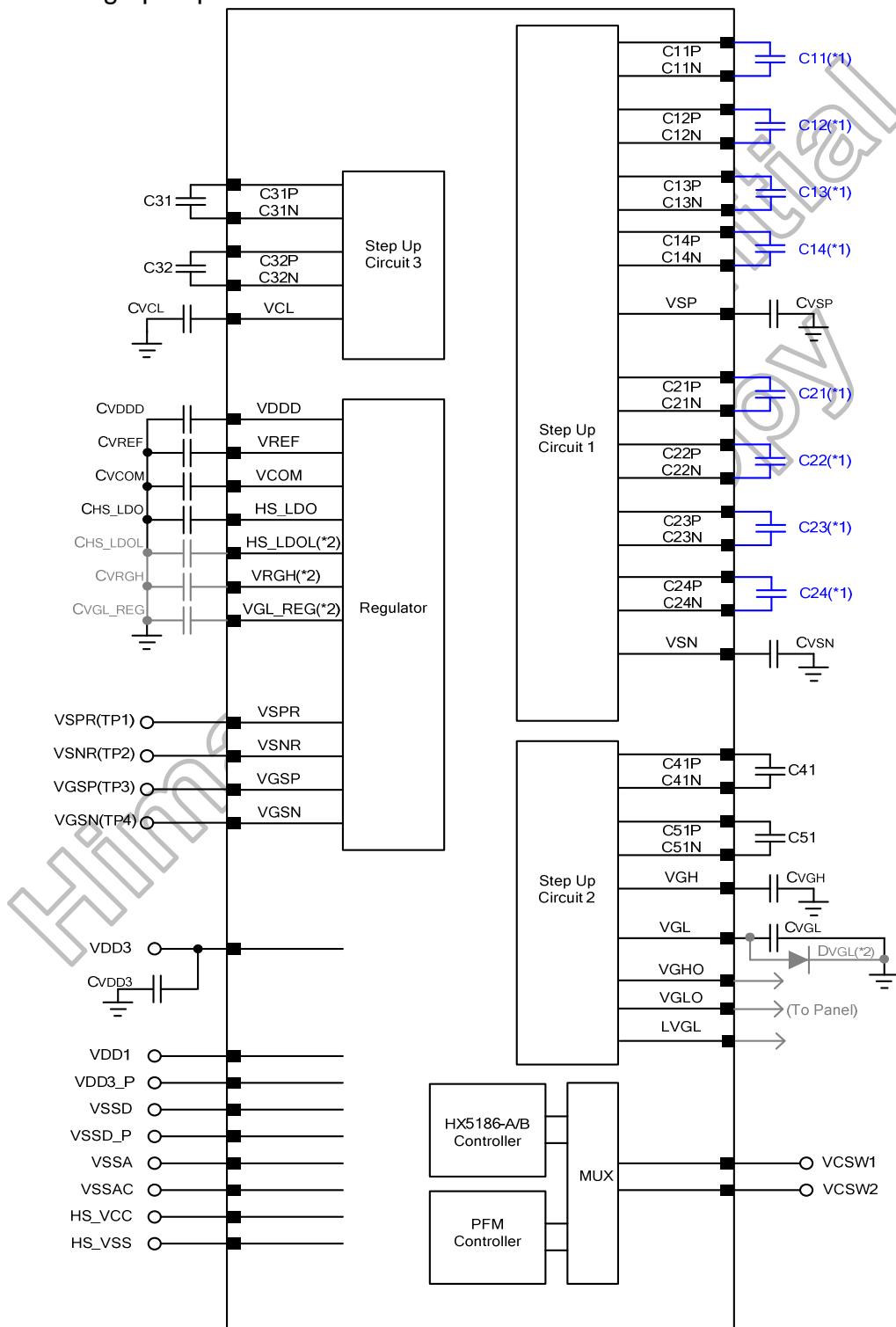
Please set up each voltage output according to the LCD panel.

Name	Function	Set up value	Note
VREF	Reference voltage from internal band gap circuit	1.8V	-
VSP	DC/DC converter circuit output	4.5V ~ 6.5V	Do not exceed 6.6V
VSN	DC/DC converter circuit output	-4.5V ~ -6.5V	Do not exceed -6.6V
VSPR	Regulated high positive voltage for gamma circuit	3.0V ~ 6.0V	Reference register
VSNR	Regulated high negative voltage for gamma circuit	-3.0V ~ -6.0V	Reference register
VGSP	Regulated low positive voltage for gamma circuit	0V, 0.3V ~ 3.7V	Reference register
VGSN	Regulated low negative voltage for gamma circuit	0V, -0.3V ~ -3.7V	Reference register
VDDD	Logic power supply	1.5V	-
VCL	Negative vltage for level shifter and VSN voltage.	-2.5V ~ -3.1V	-
VGH	Positive gate driver output voltage level	7.0V ~ 18.0V	Depend on VSP and VSN, VGH-VGL<30V
VGL	Negative gate driver output voltage level	-7.0V ~ -18.0V	
VRGH	Output regulated voltage for LCD panel	3.0V ~ 5.5V	Reference register
VGL_REG	Output regulated voltage for LCD panel	-6.4V ~ -18.0V	Reference register
VCOM	VCOM DC voltage	0V, +1V ~ -3.0V	Reference register
HS_LDO	Analog power for High speed interface circuit	1.5V	DSI I/F
HS_LDOL	Analog power for High speed interface circuit low power mode	1.2V	DSI I/F

5.5 DC/DC converter circuit

5.5.1 Use internal charge pump

HX8379-A generate supply voltage for LCD panel driving and backlight control with internal charge pump.



Note: (1) C11, C12, C13,C14 are for VSP and C21, C22, C23,C24 are for VSN internal charge pump.

(2) The capacitors of VRGH, VGL_REG, HS_LDOLand the diode of VGL are optional.

Figure 5.12: Internal charge pump

5.5.2 Use HX5186-A/B

The HX5186-A/B is highly efficient switching voltage generator circuits that generate the high voltage level VSP/VSN required for source drivers. HX8379-A contains Charge Pump Controller for HX5186-A/B, including a comparator for VSP/VSN feedback control. HX5186-A/B can provide maximum efficiency and use minimum number of external components. The output voltage of the boost converter can be set from 4.5 to 6.5 (VSP) and -4.5 to -6.5V (VSN)

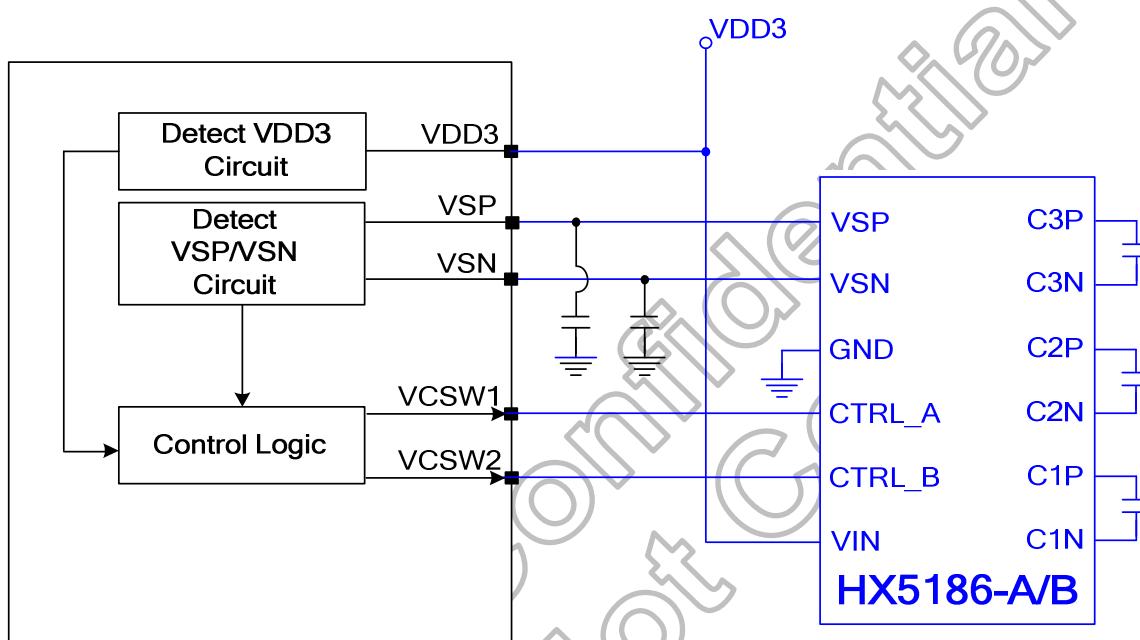


Figure 5.13: DC/DC converter circuit (HX5186-A/B)

5.5.3 Use PFM DC/DC converter

The PFM DC-DC converter generates the high voltage level VSP/VSN required for source drivers. HX8379-A contains sub-circuits of the PFM boost converter, including a precision 1.8V reference voltage, comparator, PFM controlling logic, and the output buffer. The boost converter uses a external power transistor to provide maximum efficiency and to minimize the number of external components. The output voltage of the boost converter can be set from 4.5 to 6.5 (VSP) and -4.5 to -6.5V (VSN)

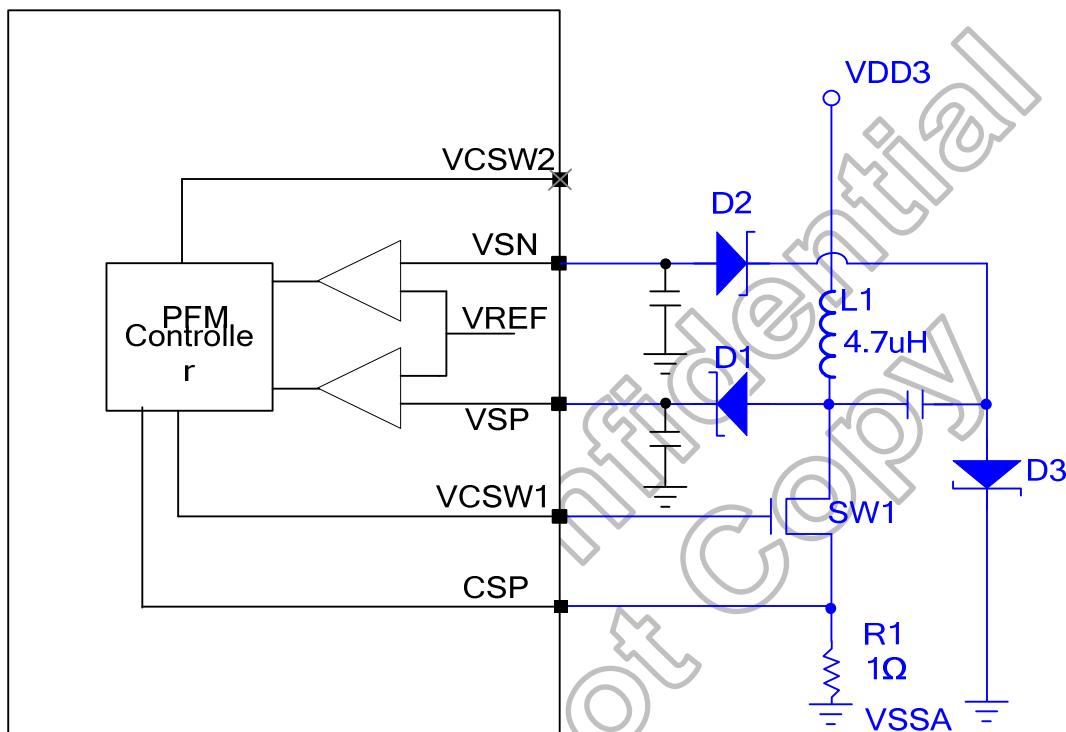


Figure 5.14: DC/DC converter circuit (PFM Type C)

5.5.4 VSN and VSP from external charge pump

The HX8379-A use external charge pump to provide VSN and VSP voltage.

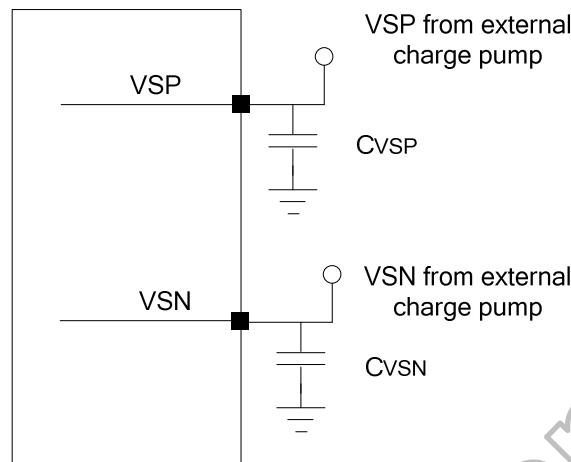


Figure 5.15: VSN and VSP by external charge pump

5.6 Idle display

The HX8379-A supports an idle display mode. The grayscale level to be used is V0 and V255 with R7, G7, B7 decoding, and the other levels (V1-V254) are halted to reduce power consumption. In idle display mode, the Gamma-micro-adjustment registers are invalid and only the upper bits of RGB are used for display.

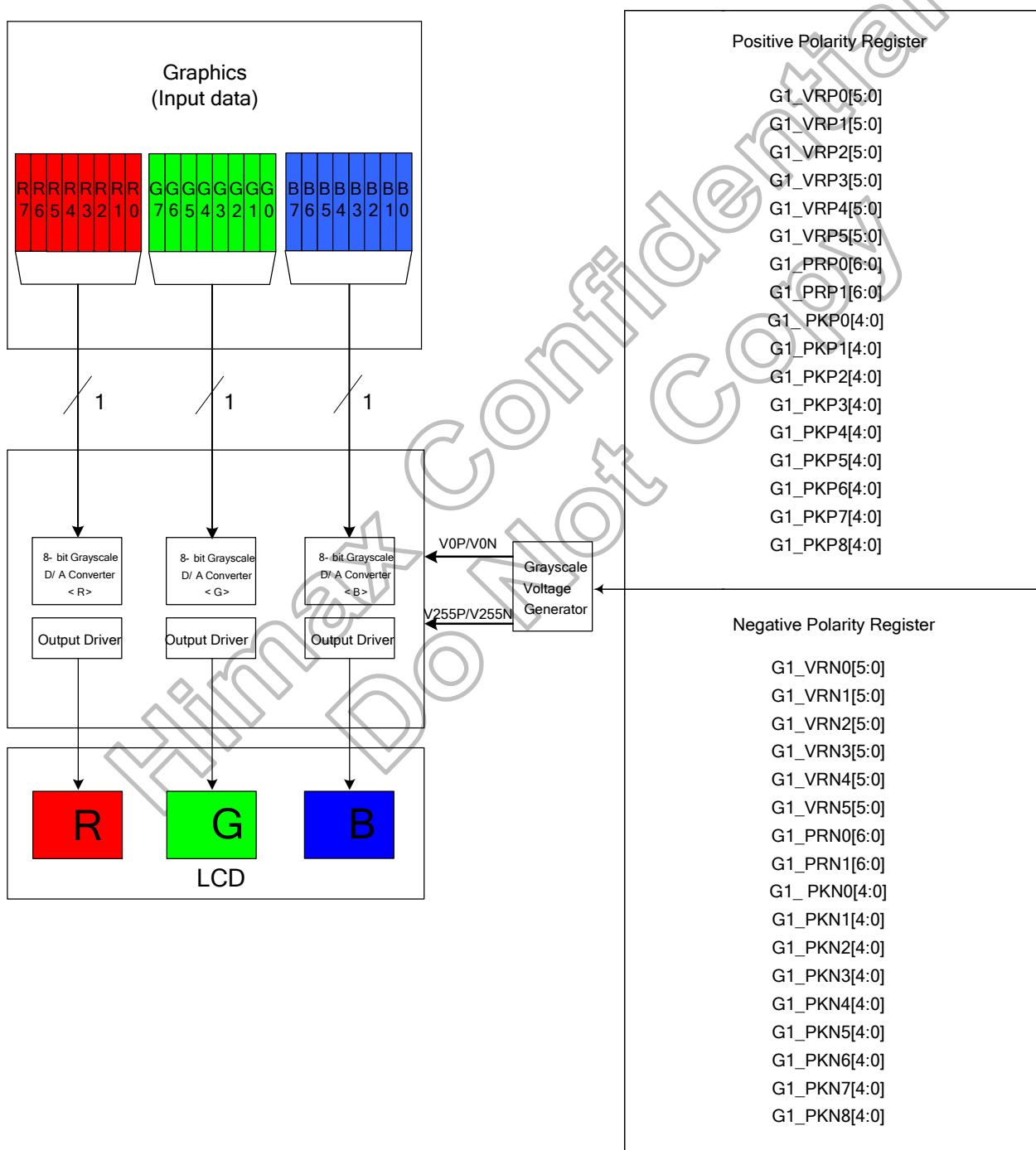


Figure 5.16: Idle mode grayscale control

5.7 Gamma characteristic correction function

The HX8379-A incorporates gamma adjustment function for the 16,777,216-color display (256 grayscale for each R, G, B color). Gamma adjustment operation is implemented by deciding the 16 grayscale levels firstly in gamma adjustment control registers to match the LCD panel. Then total 512 grayscale levels are generated in grayscale voltage generator. These registers are available for both polarities.

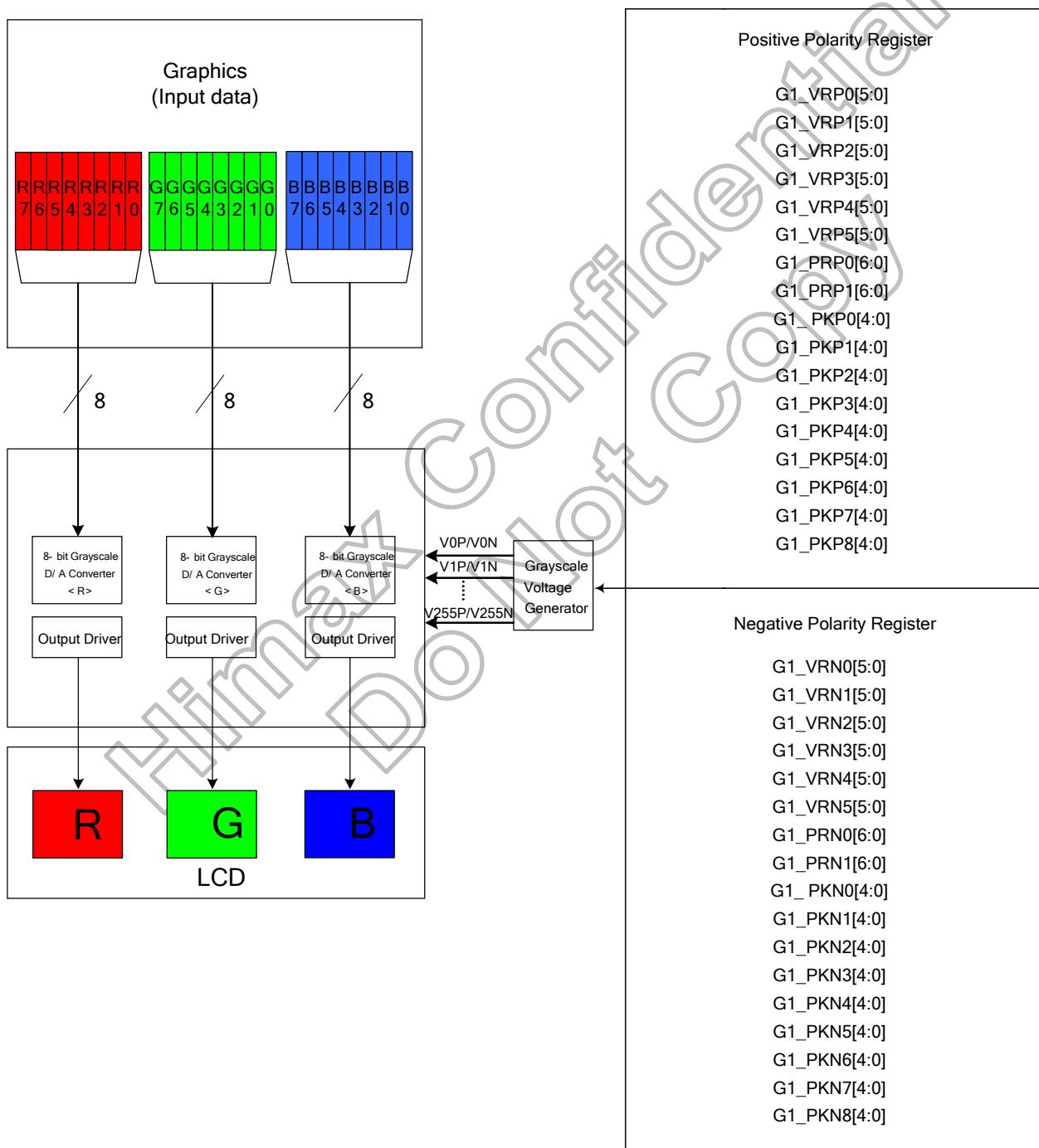


Figure 5.17: Grayscale control

Gamma-Characteristics adjustment register

This HX8379-A has register groups for specifying a series grayscale voltage that meets the Gamma-characteristics for the LCD panel used. These registers are divided into two groups, which correspond to the gradient, amplitude, and macro adjustment of the voltage for the grayscale characteristics. The polarity of each register can be specified independently.

(1) Offset adjustment registers

The offset adjustment variable registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling these variable resistors in the top and bottom of the gamma resistor stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

(2) Gamma center adjustment registers

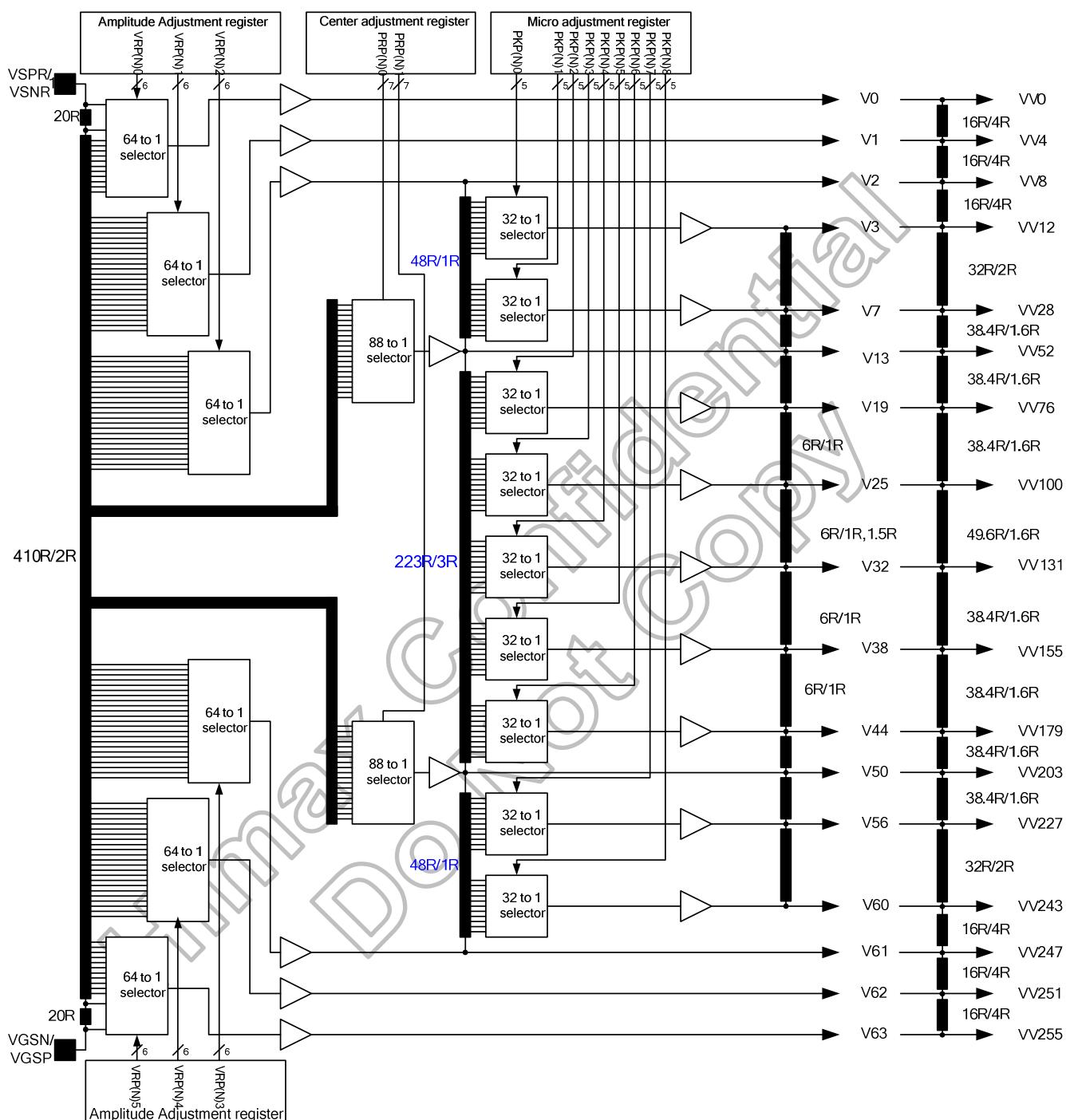
The gamma center adjustment registers are used to adjust the reference gamma voltage in the middle level of grayscale without changing the dynamic range. This function is implemented by choosing one input of 88 to 1 selector in the gamma resistor stream for reference gamma voltage generation. These registers are available for both positive and negative polarities.

(3) Gamma macro adjustment registers

The gamma macro adjustment registers can be used for fine adjustment of the reference gamma voltage. This function is implemented by controlling the 32-to-1 selectors (PKP/N0~5), each of which has 5 inputs and generates one reference voltage output ($V_g(P/N)3, 7, 19, 25, 32, 38, 44, 56, 60$).

Register Groups	Positive Polarity	Negative Polarity	Description
Center Adjustment	PRP0 6-0	PRN0 6-0	Variable resistor (PRP/N0) for center adjustment
	PRP1 6-0	PRN1 6-0	Variable resistor (PRP/N1) for center adjustment
Macro Adjustment	PKP0 4-0	PKN0 4-0	32-to-1 selector (voltage level of grayscale 3)
	PKP1 4-0	PKN1 4-0	32-to-1 selector (voltage level of grayscale 7)
	PKP2 4-0	PKN2 4-0	32-to-1 selector (voltage level of grayscale 19)
	PKP3 4-0	PKN3 4-0	32-to-1 selector (voltage level of grayscale 25)
	PKP4 4-0	PKN4 4-0	32-to-1 selector (voltage level of grayscale 32 for positive polarity and grayscale 31 for negative polarity)
	PKP5 4-0	PKN5 4-0	32-to-1 selector (voltage level of grayscale 38)
	PKP6 4-0	PKN6 4-0	32-to-1 selector (voltage level of grayscale 44)
	PKP7 4-0	PKN7 4-0	32-to-1 selector (voltage level of grayscale 56)
	PKP8 4-0	PKN8 4-0	32-to-1 selector (voltage level of grayscale 60)
	VRP0 5-0	VRN0 5-0	Variable resistor (VRP/N0) for offset adjustment
Offset Adjustment	VRP1 5-0	VRN1 5-0	Variable resistor (VRP/N1) for offset adjustment
	VRP2 5-0	VRN2 5-0	Variable resistor (VRP/N2) for offset adjustment
	VRP3 5-0	VRN3 5-0	Variable resistor (VRP/N3) for offset adjustment
	VRP4 5-0	VRN4 5-0	Variable resistor (VRP/N4) for offset adjustment
	VRP5 5-0	VRN5 5-0	Variable resistor (VRP/N5) for offset adjustment

Table 5.2: Gamma-Adjustment registers

Gamma register stream and 8 to 1 selector**Figure 5.18: Gamma register stream and gamma reference voltage**

Variable resistor

There are two types of variable resistors, one is for center adjustment and the other is for offset adjustment. The resistances are decided by setting values in the center adjustment, offset adjustment registers. Their relationships are shown below.

Value in Register VR(P/N)0 5-0	Resistance VR(P/N)0	Value in Register VR(P/N)1 5-0	Resistance VR(P/N)1	Value in Register VR(P/N)2 5-0	Resistance VR(P/N)2
000000	0R	000000	0R	000000	0R
000001	20R	000001	2R	000001	2R
000010	22R	000010	4R	000010	4R
000011	24R	000011	6R	000011	6R
•	•	•	•	•	•
•	•	•	•	•	•
011101	76R	011101	58R	011101	58R
011110	78R	011110	60R	011110	60R
011111	80R	011111	62R	011111	62R
100000	82R	100000	64R	100000	64R
100001	84R	100001	66R	100001	66R
100010	86R	100010	68R	100010	68R
•	•	•	•	•	•
•	•	•	•	•	•
111101	140R	111101	122R	111101	122R
111110	142R	111110	124R	111110	124R
111111	144R	111111	126R	111111	126R

Value in Register VR(P/N)3 5-0	Resistance VR(P/N)3	Value in Register VR(P/N)4 5-0	Resistance VR(P/N)4	Value in Register VR(P/N)5 5-0	Resistance VR(P/N)2
000000	0R	000000	0R	000000	0R
000001	2R	000001	2R	000001	2R
000010	4R	000010	4R	000010	4R
•	•	•	•	•	•
•	•	•	•	•	•
011101	58R	011101	58R	011101	58R
011110	60R	011110	60R	011110	60R
011111	62R	011111	62R	011111	62R
100000	64R	100000	64R	100000	64R
100001	66R	100001	66R	100001	66R
100010	68R	100010	68R	100010	68R
•	•	•	•	•	•
•	•	•	•	•	•
111100	120R	111100	120R	111100	120R
111101	122R	111101	122R	111101	122R
111110	124R	111110	124R	111110	124R
111111	126R	111111	126R	111111	144R

Table 5.3: Offset adjustment 0~5

Value in Register PR(P/N)0 6-0	Resistance PR(P/N)0	Value in Register PR(P/N)1 6-0	Resistance PR(P/N)1
0000000	0R	0000000	0R
0000001	2R	0000001	2R
0000010	4R	0000010	4R
•	•	•	•
•	•	•	•
1010101	170R	1010101	170R
1010110	172R	1010110	172R
1010111	174R	1010111	174R

Table 5.4: Center adjustment

The grayscale levels are determined by the following formulas:

Reference voltage	Macro adjustment value	VinP0 formula
VinP0	VRP0 5-0 = 000000	VSPR
	VRP0 5-0 = 000001	((450R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000010	((450R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000011	((450R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000100	((450R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000101	((450R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000110	((450R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 000111	((450R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001000	((450R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001001	((450R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001010	((450R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001011	((450R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001100	((450R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001101	((450R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001110	((450R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 001111	((450R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010000	((450R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010001	((450R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010010	((450R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010011	((450R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010100	((450R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010101	((450R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010110	((450R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 010111	((450R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011000	((450R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011001	((450R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011010	((450R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011011	((450R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011100	((450R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011101	((450R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011110	((450R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 011111	((450R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100000	((450R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100001	((450R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100010	((450R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100011	((450R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100100	((450R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100101	((450R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100110	((450R - 94R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 100111	((450R - 96R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101000	((450R - 98R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101001	((450R - 100R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101010	((450R - 102R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101011	((450R - 104R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101100	((450R - 106R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101101	((450R - 108R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101110	((450R - 110R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 101111	((450R - 112R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110000	((450R - 114R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110001	((450R - 116R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110010	((450R - 118R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110011	((450R - 120R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110100	((450R - 122R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110101	((450R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110110	((450R - 126R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 110111	((450R - 128R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111000	((450R - 130R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111001	((450R - 132R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111010	((450R - 134R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111011	((450R - 136R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111100	((450R - 138R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111101	((450R - 140R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111110	((450R - 142R) / 450R) * (VSPR - VGSP) + VGSP
	VRP0 5-0 = 111111	((450R - 144R) / 450R) * (VSPR - VGSP) + VGSP

Table 5.5: VinP0

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June, 2012

Reference voltage	Macro adjustment value	VinP1 formula
VinP1	VRP1 5-0 = 000000	((430R / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 000001	((430R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 000010	((430R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 000011	((430R - 6R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 000100	((430R - 8R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 000101	((430R - 10R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 000110	((430R - 12R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 000111	((430R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001000	((430R - 16R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001001	((430R - 18R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001010	((430R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001011	((430R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001100	((430R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001101	((430R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001110	((430R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 001111	((430R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010000	((430R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010001	((430R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010010	((430R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010011	((430R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010100	((430R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010101	((430R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010110	((430R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 010111	((430R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011000	((430R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011001	((430R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011010	((430R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011011	((430R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011100	((430R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011101	((430R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011110	((430R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 011111	((430R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100000	((430R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100001	((430R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100010	((430R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100011	((430R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100100	((430R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100101	((430R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100110	((430R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 100111	((430R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101000	((430R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101001	((430R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101010	((430R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101011	((430R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101100	((430R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101101	((430R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101110	((430R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 101111	((430R - 94R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110000	((430R - 96R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110001	((430R - 98R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110010	((430R - 100R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110011	((430R - 102R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110100	((430R - 104R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110101	((430R - 106R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110110	((430R - 108R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 110111	((430R - 110R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111000	((430R - 112R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111001	((430R - 114R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111010	((430R - 116R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111011	((430R - 118R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111100	((430R - 120R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111101	((430R - 122R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111110	((430R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	VRP1 5-0 = 111111	((430R - 126R) / 450R) * (VSPR - VGSP) + VGSP

Table 5.6: VinP1

Reference voltage	Macro adjustment value	VinP2 formula
VinP2	VRP2 5-0 = 000000	(420R / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000001	((420R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000010	((420R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000011	((420R - 6R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000100	((420R - 8R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000101	((420R - 10R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000110	((420R - 12R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 000111	((420R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001000	((420R - 16R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001001	((420R - 18R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001010	((420R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001011	((420R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001100	((420R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001101	((420R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001110	((420R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 001111	((420R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010000	((420R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010001	((420R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010010	((420R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010011	((420R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010100	((420R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010101	((420R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010110	((420R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 010111	((420R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011000	((420R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011001	((420R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011010	((420R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011011	((420R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011100	((420R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011101	((420R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011110	((420R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 011111	((420R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100000	((420R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100001	((420R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100010	((420R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100011	((420R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100100	((420R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100101	((420R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100110	((420R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 100111	((420R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101000	((420R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101001	((420R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101010	((420R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101011	((420R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101100	((420R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101101	((420R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101110	((420R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 101111	((420R - 94R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110000	((420R - 96R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110001	((420R - 98R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110010	((420R - 100R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110011	((420R - 102R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110100	((420R - 104R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110101	((420R - 106R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110110	((420R - 108R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 110111	((420R - 110R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111000	((420R - 112R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111001	((420R - 114R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111010	((420R - 116R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111011	((420R - 118R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111100	((420R - 120R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111101	((420R - 122R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111110	((420R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	VRP2 5-0 = 111111	((420R - 126R) / 450R) * (VSPR - VGSP) + VGSP

Table 5.7: VinP2

Reference voltage	Macro adjustment value	VinP14 formula
VinP14	VRP3 5-0 = 000000	$(156R / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 000001	$((156R - 2R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 000010	$((156R - 4R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 000011	$((156R - 6R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 000100	$((156R - 8R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 000101	$((156R - 10R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 000110	$((156R - 12R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 000111	$((156R - 14R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 001000	$((156R - 16R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 001001	$((156R - 18R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 001010	$((156R - 20R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 001011	$((156R - 22R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 001100	$((156R - 24R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 001101	$((156R - 26R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 001110	$((156R - 28R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 001111	$((156R - 30R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 010000	$((156R - 32R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 010001	$((156R - 34R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 010010	$((156R - 36R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 010011	$((156R - 38R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 010100	$((156R - 40R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 010101	$((156R - 42R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 010110	$((156R - 44R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 010111	$((156R - 46R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 011000	$((156R - 48R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 011001	$((156R - 50R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 011010	$((156R - 52R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 011011	$((156R - 54R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 011100	$((156R - 56R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 011101	$((156R - 58R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 011110	$((156R - 60R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 011111	$((156R - 62R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 100000	$((156R - 64R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 100001	$((156R - 66R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 100010	$((156R - 68R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 100011	$((156R - 70R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 100100	$((156R - 72R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 100101	$((156R - 74R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 100110	$((156R - 76R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 100111	$((156R - 78R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 101000	$((156R - 80R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 101001	$((156R - 82R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 101010	$((156R - 84R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 101011	$((156R - 86R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 101100	$((156R - 88R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 101101	$((156R - 90R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 101110	$((156R - 92R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 101111	$((156R - 94R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 110000	$((156R - 96R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 110001	$((156R - 98R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 110010	$((156R - 100R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 110011	$((156R - 102R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 110100	$((156R - 104R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 110101	$((156R - 106R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 110110	$((156R - 108R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 110111	$((156R - 110R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 111000	$((156R - 112R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 111001	$((156R - 114R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 111010	$((156R - 116R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 111011	$((156R - 118R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 111100	$((156R - 120R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 111101	$((156R - 122R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 111110	$((156R - 124R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP3 5-0 = 111111	$((156R - 126R) / 450R) * (VSPR - VGSP) + VGSP$

Table 5.8: VinP14

Reference voltage	Macro adjustment value	VinP15 formula
VinP15	VRP4 5-0 = 000000	(146R / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000001	((146R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000010	((146R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000011	((146R - 6R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000100	((146R - 8R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000101	((146R - 10R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000110	((146R - 12R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 000111	((146R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001000	((146R - 16R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001001	((146R - 18R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001010	((146R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001011	((146R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001100	((146R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001101	((146R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001110	((146R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 001111	((146R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010000	((146R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010001	((146R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010010	((146R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010011	((146R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010100	((146R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010101	((146R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010110	((146R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 010111	((146R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011000	((146R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011001	((146R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011010	((146R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011011	((146R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011100	((146R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011101	((146R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011110	((146R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 011111	((146R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100000	((146R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100001	((146R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100010	((146R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100011	((146R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100100	((146R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100101	((146R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100110	((146R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 100111	((146R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101000	((146R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101001	((146R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101010	((146R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101011	((146R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101100	((146R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101101	((146R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101110	((146R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 101111	((146R - 94R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110000	((146R - 96R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110001	((146R - 98R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110010	((146R - 100R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110011	((146R - 102R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110100	((146R - 104R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110101	((146R - 106R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110110	((146R - 108R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 110111	((146R - 110R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111000	((146R - 112R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111001	((146R - 114R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111010	((146R - 116R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111011	((146R - 118R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111100	((146R - 120R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111101	((146R - 122R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111110	((146R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	VRP4 5-0 = 111111	((146R - 126R) / 450R) * (VSPR - VGSP) + VGSP

Table 5.9: VinP15

Reference voltage	Macro adjustment value	VinP16 formula
VinP16	VRP5 5-0 = 000000	$((144R / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 000001	$((144R - 2R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 000010	$((144R - 4R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 000011	$((144R - 6R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 000100	$((144R - 8R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 000101	$((144R - 10R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 000110	$((144R - 12R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 000111	$((144R - 14R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 001000	$((144R - 16R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 001001	$((144R - 18R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 001010	$((144R - 20R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 001011	$((144R - 22R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 001100	$((144R - 24R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 001101	$((144R - 26R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 001110	$((144R - 28R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 001111	$((144R - 30R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 010000	$((144R - 32R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 010001	$((144R - 34R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 010010	$((144R - 36R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 010011	$((144R - 38R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 010100	$((144R - 40R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 010101	$((144R - 42R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 010110	$((144R - 44R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 010111	$((144R - 46R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 011000	$((144R - 48R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 011001	$((144R - 50R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 011010	$((144R - 52R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 011011	$((144R - 54R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 011100	$((144R - 56R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 011101	$((144R - 58R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 011110	$((144R - 60R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 011111	$((144R - 62R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 100000	$((144R - 64R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 100001	$((144R - 66R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 100010	$((144R - 68R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 100011	$((144R - 70R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 100100	$((144R - 72R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 100101	$((144R - 74R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 100110	$((144R - 76R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 100111	$((144R - 78R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 101000	$((144R - 80R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 101001	$((144R - 82R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 101010	$((144R - 84R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 101011	$((144R - 86R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 101100	$((144R - 88R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 101101	$((144R - 90R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 101110	$((144R - 92R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 101111	$((144R - 94R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 110000	$((144R - 96R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 110001	$((144R - 98R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 110010	$((144R - 100R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 110011	$((144R - 102R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 110100	$((144R - 104R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 110101	$((144R - 106R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 110110	$((144R - 108R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 110111	$((144R - 110R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 111000	$((144R - 112R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 111001	$((144R - 114R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 111010	$((144R - 116R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 111011	$((144R - 118R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 111100	$((144R - 120R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 111101	$((144R - 122R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 111110	$((144R - 124R) / 450R) * (VSPR - VGSP) + VGSP$
	VRP5 5-0 = 111111	VGSP

Table 5.10: VinP16

Reference voltage	Macro adjustment value	VinP5 formula
VinP5	PRP0 6-0 = 0000000	(350R / 450R) (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000001	((350R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000010	((350R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0000011	((350R - 6R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 00000100	((350R - 8R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 00000101	((350R - 10R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 00000110	((350R - 12R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 00000111	((350R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001000	((350R - 16R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001001	((350R - 18R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001010	((350R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001011	((350R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001100	((350R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001101	((350R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001110	((350R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0001111	((350R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010000	((350R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010001	((350R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 00100010	((350R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 00100011	((350R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010100	((350R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010101	((350R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010110	((350R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0010111	((350R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011000	((350R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011001	((350R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011010	((350R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011011	((350R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011100	((350R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011101	((350R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011110	((350R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0011111	((350R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100000	((350R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100001	((350R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100010	((350R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100011	((350R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100100	((350R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100101	((350R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100110	((350R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0100111	((350R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101000	((350R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101001	((350R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101010	((350R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101011	((350R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101100	((350R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101101	((350R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101110	((350R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	PRP0 6-0 = 0101111	((350R - 94R) / 450R) * (VSPR - VGSP) + VGSP
PRP0 6-0 = 0110000	((350R - 96R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0110001	((350R - 98R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0110010	((350R - 100R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0110011	((350R - 102R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0110100	((350R - 104R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0110101	((350R - 106R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0110110	((350R - 108R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0110111	((350R - 110R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0111000	((350R - 112R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0111001	((350R - 114R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0111010	((350R - 116R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0111011	((350R - 118R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0111100	((350R - 120R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0111101	((350R - 122R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0111110	((350R - 124R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 0111111	((350R - 126R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 1000000	((350R - 128R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 1000001	((350R - 130R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 1000010	((350R - 132R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 1000011	((350R - 134R) / 450R) * (VSPR - VGSP) + VGSP	
PRP0 6-0 = 1000100	((350R - 136R) / 450R) * (VSPR - VGSP) + VGSP	

Reference voltage	Macro adjustment value	VinP5 formula
	PRP0 6-0 = 1000101	$((350R - 138R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP0 6-0 = 1000110	$((350R - 140R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP0 6-0 = 1000111	$((350R - 142R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP0 6-0 = 1001000	$((350R - 144R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP0 6-0 = 1001001	$((350R - 146R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP0 6-0 = 1001010	$((350R - 148R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP0 6-0 = 1001011	$((350R - 150R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP0 6-0 = 1001100	$((350R - 152R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP0 6-0 = 1001101	$((350R - 154R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP0 6-0 = 1001110	$((350R - 156R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP0 6-0 = 1001111	$((350R - 158R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP0 6-0 = 1010000	$((350R - 160R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP0 6-0 = 1010001	$((350R - 162R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP0 6-0 = 1010010	$((350R - 164R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP0 6-0 = 1010011	$((350R - 166R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP0 6-0 = 1010100	$((350R - 168R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP0 6-0 = 1010101	$((350R - 170R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP0 6-0 = 1010110	$((350R - 172R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP0 6-0 = 1010111	$((350R - 174R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP0 6-0 = 1011000	inhibit
	PRP0 6-0 = 1011001	inhibit
	PRP0 6-0 = 1011010	inhibit
	PRP0 6-0 = 1011011	inhibit
	PRP0 6-0 = 1011100	inhibit
	PRP0 6-0 = 1011101	inhibit
	PRP0 6-0 = 1011110	inhibit
	PRP0 6-0 = 1011111	inhibit
	PRP0 6-0 = 1100000	inhibit
	PRP0 6-0 = 1100001	inhibit
	PRP0 6-0 = 1100010	inhibit
	PRP0 6-0 = 1100011	inhibit
	PRP0 6-0 = 1100100	inhibit
	PRP0 6-0 = 1100101	inhibit
	PRP0 6-0 = 1100110	inhibit
	PRP0 6-0 = 1100111	inhibit
	PRP0 6-0 = 1101000	inhibit
	PRP0 6-0 = 1101001	inhibit
	PRP0 6-0 = 1101010	inhibit
	PRP0 6-0 = 1101011	inhibit
	PRP0 6-0 = 1101100	inhibit
	PRP0 6-0 = 1101101	inhibit
	PRP0 6-0 = 1101110	inhibit
	PRP0 6-0 = 1101111	inhibit
	PRP0 6-0 = 1110000	inhibit
	PRP0 6-0 = 1110001	inhibit
	PRP0 6-0 = 1110010	inhibit
	PRP0 6-0 = 1110011	inhibit
	PRP0 6-0 = 1110100	inhibit
	PRP0 6-0 = 1110101	inhibit
	PRP0 6-0 = 1110110	inhibit
	PRP0 6-0 = 1110111	inhibit
	PRP0 6-0 = 1111000	inhibit
	PRP0 6-0 = 1111001	inhibit
	PRP0 6-0 = 1111010	inhibit
	PRP0 6-0 = 1111011	inhibit
	PRP0 6-0 = 1111100	inhibit
	PRP0 6-0 = 1111101	inhibit
	PRP0 6-0 = 1111110	inhibit
	PRP0 6-0 = 1111111	inhibit

Table 5.11: VinP5

Reference voltage	Macro adjustment value	VinP11 formula
VinP11	PRP1 6-0 = 0000000	(274R / 450R) (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000001	((274R - 2R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000010	((274R - 4R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000011	((274R - 6R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000100	((274R - 8R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000101	((274R - 10R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000110	((274R - 12R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0000111	((274R - 14R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001000	((274R - 16R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001001	((274R - 18R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001010	((274R - 20R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001011	((274R - 22R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001100	((274R - 24R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001101	((274R - 26R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001110	((274R - 28R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0001111	((274R - 30R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010000	((274R - 32R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010001	((274R - 34R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010002	((274R - 36R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010003	((274R - 38R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010100	((274R - 40R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010101	((274R - 42R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010110	((274R - 44R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0010111	((274R - 46R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011000	((274R - 48R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011001	((274R - 50R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011010	((274R - 52R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011011	((274R - 54R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011100	((274R - 56R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011101	((274R - 58R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011110	((274R - 60R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0011111	((274R - 62R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100000	((274R - 64R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100001	((274R - 66R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100010	((274R - 68R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100011	((274R - 70R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100100	((274R - 72R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100101	((274R - 74R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100110	((274R - 76R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0100111	((274R - 78R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101000	((274R - 80R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101001	((274R - 82R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101010	((274R - 84R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101011	((274R - 86R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101100	((274R - 88R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101101	((274R - 90R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101110	((274R - 92R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0101111	((274R - 94R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110000	((274R - 96R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110001	((274R - 98R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110010	((274R - 100R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110011	((274R - 102R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110100	((274R - 104R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110101	((274R - 106R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110110	((274R - 108R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0110111	((274R - 110R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111000	((274R - 112R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111001	((274R - 114R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111010	((274R - 116R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111011	((274R - 118R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111100	((274R - 120R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111101	((274R - 122R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111110	((274R - 124R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 0111111	((274R - 126R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000000	((274R - 128R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000001	((274R - 130R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000010	((274R - 132R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000011	((274R - 134R) / 450R) * (VSPR - VGSP) + VGSP
	PRP1 6-0 = 1000100	((274R - 136R) / 450R) * (VSPR - VGSP) + VGSP

Reference voltage	Macro adjustment value	VinP11 formula
	PRP1 6-0 = 1000101	$((274R - 138R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP1 6-0 = 1000110	$((274R - 140R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP1 6-0 = 1000111	$((274R - 142R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP1 6-0 = 1001000	$((274R - 144R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP1 6-0 = 1001001	$((274R - 146R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP1 6-0 = 1001010	$((274R - 148R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP1 6-0 = 1001011	$((274R - 150R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP1 6-0 = 1001100	$((274R - 152R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP1 6-0 = 1001101	$((274R - 154R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP1 6-0 = 1001110	$((274R - 156R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP1 6-0 = 1001111	$((274R - 158R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP1 6-0 = 1010000	$((274R - 160R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP1 6-0 = 1010001	$((274R - 162R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP1 6-0 = 1010010	$((274R - 164R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP1 6-0 = 1010011	$((274R - 166R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP1 6-0 = 1010100	$((274R - 168R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP1 6-0 = 1010101	$((274R - 170R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP1 6-0 = 1010110	$((274R - 172R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP1 6-0 = 1010111	$((274R - 174R) / 450R) * (VSPR - VGSP) + VGSP$
	PRP1 6-0 = 1011000	inhibit
	PRP1 6-0 = 1011001	inhibit
	PRP1 6-0 = 1011010	inhibit
	PRP1 6-0 = 1011011	inhibit
	PRP1 6-0 = 1011100	inhibit
	PRP1 6-0 = 1011101	inhibit
	PRP1 6-0 = 1011110	inhibit
	PRP1 6-0 = 1011111	inhibit
	PRP1 6-0 = 1100000	inhibit
	PRP1 6-0 = 1100001	inhibit
	PRP1 6-0 = 1100010	inhibit
	PRP1 6-0 = 1100011	inhibit
	PRP1 6-0 = 1100100	inhibit
	PRP1 6-0 = 1100101	inhibit
	PRP1 6-0 = 1100110	inhibit
	PRP1 6-0 = 1100111	inhibit
	PRP1 6-0 = 1101000	inhibit
	PRP1 6-0 = 1101001	inhibit
	PRP1 6-0 = 1101010	inhibit
	PRP1 6-0 = 1101011	inhibit
	PRP1 6-0 = 1101100	inhibit
	PRP1 6-0 = 1101101	inhibit
	PRP1 6-0 = 1101110	inhibit
	PRP1 6-0 = 1101111	inhibit
	PRP1 6-0 = 1110000	inhibit
	PRP1 6-0 = 1110001	inhibit
	PRP1 6-0 = 1110010	inhibit
	PRP1 6-0 = 1110011	inhibit
	PRP1 6-0 = 1110100	inhibit
	PRP1 6-0 = 1110101	inhibit
	PRP1 6-0 = 1110110	inhibit
	PRP1 6-0 = 1110111	inhibit
	PRP1 6-0 = 1111000	inhibit
	PRP1 6-0 = 1111001	inhibit
	PRP1 6-0 = 1111010	inhibit
	PRP1 6-0 = 1111011	inhibit
	PRP1 6-0 = 1111100	inhibit
	PRP1 6-0 = 1111101	inhibit
	PRP1 6-0 = 1111110	inhibit
	PRP1 6-0 = 1111111	inhibit

Table 5.12: VinP11

Reference voltage	Macro adjustment value	VinP3 formula
VinP3	PKP0 4-0 = 00000	$(47R / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 00001	$((47R - 1R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 00010	$((47R - 2R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 00011	$((47R - 3R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 00100	$((47R - 4R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 00101	$((47R - 5R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 00110	$((47R - 6R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 00111	$((47R - 7R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 01000	$((47R - 8R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 01001	$((47R - 9R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 01010	$((47R - 10R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 01011	$((47R - 11R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 01100	$((47R - 12R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 01101	$((47R - 13R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 01110	$((47R - 14R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 01111	$((47R - 15R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 10000	$((47R - 16R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 10001	$((47R - 17R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 10010	$((47R - 18R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 10011	$((47R - 19R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 10100	$((47R - 20R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 10101	$((47R - 21R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 10110	$((47R - 22R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 10111	$((47R - 23R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 11000	$((47R - 24R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 11001	$((47R - 25R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 11010	$((47R - 26R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 11011	$((47R - 27R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 11100	$((47R - 28R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 11101	$((47R - 29R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 11110	$((47R - 30R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP0 4-0 = 11111	$((47R - 31R) / 48R) * (VinP2 - VinP5) + VinP5$

Table 5.13: VinP3

Reference voltage	Macro adjustment value	VinP4 formula
VinP4	PKP1 4-0 = 00000	$(32R / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 00001	$((32R - 1R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 00010	$((32R - 2R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 00011	$((32R - 3R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 00100	$((32R - 4R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 00101	$((32R - 5R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 00110	$((32R - 6R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 00111	$((32R - 7R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 01000	$((32R - 8R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 01001	$((32R - 9R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 01010	$((32R - 10R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 01011	$((32R - 11R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 01100	$((32R - 12R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 01101	$((32R - 13R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 01110	$((32R - 14R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 01111	$((32R - 15R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 10000	$((32R - 16R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 10001	$((32R - 17R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 10010	$((32R - 18R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 10011	$((32R - 19R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 10100	$((32R - 20R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 10101	$((32R - 21R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 10110	$((32R - 22R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 10111	$((32R - 23R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 11000	$((32R - 24R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 11001	$((32R - 25R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 11010	$((32R - 26R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 11011	$((32R - 27R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 11100	$((32R - 28R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 11101	$((32R - 29R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 11110	$((32R - 30R) / 48R) * (VinP2 - VinP5) + VinP5$
	PKP1 4-0 = 11111	$((32R - 31R) / 48R) * (VinP2 - VinP5) + VinP5$

Table 5.14: VinP4

Reference voltage	Macro adjustment value	VinP6 formula
VinP6	PKP2 4-0 = 00000	$(220R / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 00001	$((220R - 3R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 00010	$((220R - 6R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 00011	$((220R - 9R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 00100	$((220R - 12R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 00101	$((220R - 15R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 00110	$((220R - 18R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 00111	$((220R - 21R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 01000	$((220R - 24R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 01001	$((220R - 27R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 01010	$((220R - 30R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 01011	$((220R - 33R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 01100	$((220R - 36R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 01101	$((220R - 39R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 01110	$((220R - 42R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 01111	$((220R - 45R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 10000	$((220R - 48R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 10001	$((220R - 51R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 10010	$((220R - 54R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 10011	$((220R - 57R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 10100	$((220R - 60R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 10101	$((220R - 63R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 10110	$((220R - 66R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 10111	$((220R - 69R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 11000	$((220R - 72R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 11001	$((220R - 75R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 11010	$((220R - 78R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 11011	$((220R - 81R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 11100	$((220R - 84R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 11101	$((220R - 87R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 11110	$((220R - 90R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP2 4-0 = 11111	$((220R - 93R) / 223R) * (VinP5 - VinP11) + VinP11$

Table 5.15: VinP6

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Reference voltage	Macro adjustment value	VinP7 formula
VinP7	PKP3 4-0 = 00000	$(193R / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 00001	$((193R - 3R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 00010	$((193R - 6R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 00011	$((193R - 9R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 00100	$((193R - 12R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 00101	$((193R - 15R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 00110	$((193R - 18R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 00111	$((193R - 21R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 01000	$((193R - 24R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 01001	$((193R - 27R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 01010	$((193R - 30R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 01011	$((193R - 33R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 01100	$((193R - 36R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 01101	$((193R - 39R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 01110	$((193R - 42R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 01111	$((193R - 45R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 10000	$((193R - 48R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 10001	$((193R - 51R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 10010	$((193R - 54R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 10011	$((193R - 57R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 10100	$((193R - 60R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 10101	$((193R - 63R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 10110	$((193R - 66R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 10111	$((193R - 69R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 11000	$((193R - 72R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 11001	$((193R - 75R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 11010	$((193R - 78R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 11011	$((193R - 81R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 11100	$((193R - 84R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 11101	$((193R - 87R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 11110	$((193R - 90R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP3 4-0 = 11111	$((193R - 93R) / 223R) * (VinP5 - VinP11) + VinP11$

Table 5.16: VinP7

Reference voltage	Macro adjustment value	VinP8 formula
VinP8	PKP4 4-0 = 00000	$(158R / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 00001	$((158R - 3R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 00010	$((158R - 6R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 00011	$((158R - 9R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 00100	$((158R - 12R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 00101	$((158R - 15R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 00110	$((158R - 18R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 00111	$((158R - 21R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 01000	$((158R - 24R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 01001	$((158R - 27R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 01010	$((158R - 30R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 01011	$((158R - 33R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 01100	$((158R - 36R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 01101	$((158R - 39R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 01110	$((158R - 42R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 01111	$((158R - 45R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 10000	$((158R - 48R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 10001	$((158R - 51R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 10010	$((158R - 54R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 10011	$((158R - 57R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 10100	$((158R - 60R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 10101	$((158R - 63R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 10110	$((158R - 66R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 10111	$((158R - 69R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 11000	$((158R - 72R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 11001	$((158R - 75R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 11010	$((158R - 78R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 11011	$((158R - 81R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 11100	$((158R - 84R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 11101	$((158R - 87R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 11110	$((158R - 90R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP4 4-0 = 11111	$((158R - 93R) / 223R) * (VinP5 - VinP11) + VinP11$

Table 5.17: VinP8

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Reference voltage	Macro adjustment value	VinP9 formula
VinP9	PKP5 4-0 = 00000	$(123R / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 00001	$((123R - 3R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 00010	$((123R - 6R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 00011	$((123R - 9R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 00100	$((123R - 12R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 00101	$((123R - 15R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 00110	$((123R - 18R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 00111	$((123R - 21R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 01000	$((123R - 24R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 01001	$((123R - 27R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 01010	$((123R - 30R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 01011	$((123R - 33R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 01100	$((123R - 36R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 01101	$((123R - 39R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 01110	$((123R - 42R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 01111	$((123R - 45R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 10000	$((123R - 48R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 10001	$((123R - 51R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 10010	$((123R - 54R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 10011	$((123R - 57R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 10100	$((123R - 60R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 10101	$((123R - 63R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 10110	$((123R - 66R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 10111	$((123R - 69R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 11000	$((123R - 72R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 11001	$((123R - 75R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 11010	$((123R - 78R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 11011	$((123R - 81R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 11100	$((123R - 84R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 11101	$((123R - 87R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 11110	$((123R - 90R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP5 4-0 = 11111	$((123R - 93R) / 223R) * (VinP5 - VinP11) + VinP11$

Table 5.18: VinP9

Reference voltage	Macro adjustment value	VinP10 formula
VinP10	PKP6 4-0 = 00000	$(96R / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 00001	$((96R - 3R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 00010	$((96R - 6R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 00011	$((96R - 9R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 00100	$((96R - 12R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 00101	$((96R - 15R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 00110	$((96R - 18R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 00111	$((96R - 21R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 01000	$((96R - 24R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 01001	$((96R - 27R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 01010	$((96R - 30R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 01011	$((96R - 33R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 01100	$((96R - 36R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 01101	$((96R - 39R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 01110	$((96R - 42R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 01111	$((96R - 45R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 10000	$((96R - 48R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 10001	$((96R - 51R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 10010	$((96R - 54R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 10011	$((96R - 57R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 10100	$((96R - 60R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 10101	$((96R - 63R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 10110	$((96R - 66R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 10111	$((96R - 69R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 11000	$((96R - 72R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 11001	$((96R - 75R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 11010	$((96R - 78R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 11011	$((96R - 81R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 11100	$((96R - 84R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 11101	$((96R - 87R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 11110	$((96R - 90R) / 223R) * (VinP5 - VinP11) + VinP11$
	PKP6 4-0 = 11111	$((96R - 93R) / 223R) * (VinP5 - VinP11) + VinP11$

Table 5.19: VinP10

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June, 2012

Reference voltage	Macro adjustment value	VinP12 formula
VinP12	PKP7 4-0 = 00000	$(47R / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 00001	$((47R - 1R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 00010	$((47R - 2R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 00011	$((47R - 3R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 00100	$((47R - 4R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 00101	$((47R - 5R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 00110	$((47R - 6R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 00111	$((47R - 7R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 01000	$((47R - 8R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 01001	$((47R - 9R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 01010	$((47R - 10R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 01011	$((47R - 11R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 01100	$((47R - 12R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 01101	$((47R - 13R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 01110	$((47R - 14R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 01111	$((47R - 15R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 10000	$((47R - 16R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 10001	$((47R - 17R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 10010	$((47R - 18R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 10011	$((47R - 19R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 10100	$((47R - 20R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 10101	$((47R - 21R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 10110	$((47R - 22R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 10111	$((47R - 23R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 11000	$((47R - 24R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 11001	$((47R - 25R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 11010	$((47R - 26R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 11011	$((47R - 27R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 11100	$((47R - 28R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 11101	$((47R - 29R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 11110	$((47R - 30R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP7 4-0 = 11111	$((47R - 31R) / 48R) * (VinP11 - VinP14) + VinP14$

Table 5.20: VinP12

Reference voltage	Macro adjustment value	VinP13 formula
VinP13	PKP8 4-0 = 00000	$(32R / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 00001	$((32R - 1R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 00010	$((32R - 2R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 00011	$((32R - 3R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 00100	$((32R - 4R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 00101	$((32R - 5R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 00110	$((32R - 6R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 00111	$((32R - 7R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 01000	$((32R - 8R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 01001	$((32R - 9R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 01010	$((32R - 10R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 01011	$((32R - 11R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 01100	$((32R - 12R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 01101	$((32R - 13R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 01110	$((32R - 14R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 01111	$((32R - 15R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 10000	$((32R - 16R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 10001	$((32R - 17R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 10010	$((32R - 18R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 10011	$((32R - 19R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 10100	$((32R - 20R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 10101	$((32R - 21R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 10110	$((32R - 22R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 10111	$((32R - 23R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 11000	$((32R - 24R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 11001	$((32R - 25R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 11010	$((32R - 26R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 11011	$((32R - 27R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 11100	$((32R - 28R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 11101	$((32R - 29R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 11110	$((32R - 30R) / 48R) * (VinP11 - VinP14) + VinP14$
	PKP8 4-0 = 11111	$((32R - 31R) / 48R) * (VinP11 - VinP14) + VinP14$

Table 5.21: VinP13

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Reference voltage	Macro adjustment value	VinN0 formula
VinN0	VRN0 5-0 = 000000	VSNR
	VRN0 5-0 = 000001	((450R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000010	((450R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000011	((450R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000100	((450R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000101	((450R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000110	((450R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 000111	((450R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001000	((450R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001001	((450R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001010	((450R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001011	((450R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001100	((450R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001101	((450R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001110	((450R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 001111	((450R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010000	((450R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010001	((450R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010010	((450R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010011	((450R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010100	((450R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010101	((450R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010110	((450R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 010111	((450R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011000	((450R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011001	((450R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011010	((450R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011011	((450R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011100	((450R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011101	((450R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011110	((450R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 011111	((450R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100000	((450R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100001	((450R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100010	((450R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100011	((450R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100100	((450R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100101	((450R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100110	((450R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 100111	((450R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101000	((450R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101001	((450R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101010	((450R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101011	((450R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101100	((450R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101101	((450R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101110	((450R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 101111	((450R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110000	((450R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110001	((450R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110010	((450R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110011	((450R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110100	((450R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110101	((450R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110110	((450R - 126R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 110111	((450R - 128R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111000	((450R - 130R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111001	((450R - 132R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111010	((450R - 134R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111011	((450R - 136R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111100	((450R - 138R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111101	((450R - 140R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111110	((450R - 142R) / 450R) * (VSNR - VGSN) + VGSN
	VRN0 5-0 = 111111	((450R - 144R) / 450R) * (VSNR - VGSN) + VGSN

Table 5.22: VinN0

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-P.84-

June, 2012

Reference voltage	Macro adjustment value	VinN1 formula
VinN1	VRN1 5-0 = 000000	(430R / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 000001	((430R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 000010	((430R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 000011	((430R - 6R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 000100	((430R - 8R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 000101	((430R - 10R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 000110	((430R - 12R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 000111	((430R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001000	((430R - 16R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001001	((430R - 18R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001010	((430R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001011	((430R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001100	((430R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001101	((430R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001110	((430R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 001111	((430R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010000	((430R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010001	((430R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010010	((430R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010011	((430R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010100	((430R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010101	((430R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010110	((430R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 010111	((430R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011000	((430R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011001	((430R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011010	((430R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011011	((430R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011100	((430R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011101	((430R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011110	((430R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 011111	((430R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100000	((430R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100001	((430R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100010	((430R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100011	((430R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100100	((430R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100101	((430R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100110	((430R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 100111	((430R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101000	((430R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101001	((430R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101010	((430R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101011	((430R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101100	((430R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101101	((430R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101110	((430R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 101111	((430R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110000	((430R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110001	((430R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110010	((430R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110011	((430R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110100	((430R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110101	((430R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110110	((430R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 110111	((430R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111000	((430R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111001	((430R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111010	((430R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111011	((430R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111100	((430R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111101	((430R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111110	((430R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	VRN1 5-0 = 111111	((430R - 126R) / 450R) * (VSNR - VGSN) + VGSN

Table 5.23: VinN1

Reference voltage	Macro adjustment value	VinN2 formula
VinN2	VRN2 5-0 = 000000	(420R / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000001	((420R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000010	((420R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000011	((420R - 6R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000100	((420R - 8R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000101	((420R - 10R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000110	((420R - 12R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 000111	((420R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001000	((420R - 16R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001001	((420R - 18R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001010	((420R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001011	((420R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001100	((420R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001101	((420R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001110	((420R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 001111	((420R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010000	((420R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010001	((420R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010010	((420R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010011	((420R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010100	((420R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010101	((420R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010110	((420R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 010111	((420R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011000	((420R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011001	((420R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011010	((420R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011011	((420R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011100	((420R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011101	((420R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011110	((420R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 011111	((420R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100000	((420R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100001	((420R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100010	((420R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100011	((420R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100100	((420R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100101	((420R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100110	((420R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 100111	((420R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101000	((420R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101001	((420R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101010	((420R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101011	((420R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101100	((420R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101101	((420R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101110	((420R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 101111	((420R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110000	((420R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110001	((420R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110010	((420R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110011	((420R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110100	((420R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110101	((420R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110110	((420R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 110111	((420R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111000	((420R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111001	((420R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111010	((420R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111011	((420R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111100	((420R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111101	((420R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111110	((420R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	VRN2 5-0 = 111111	((420R - 126R) / 450R) * (VSNR - VGSN) + VGSN

Table 5.24: VinN2

Reference voltage	Macro adjustment value	VinN14 formula
VinN14	VRN3 5-0 = 000000	((156R / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 000001	((156R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 000010	((156R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 000011	((156R - 6R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 000100	((156R - 8R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 000101	((156R - 10R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 000110	((156R - 12R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 000111	((156R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001000	((156R - 16R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001001	((156R - 18R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001010	((156R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001011	((156R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001100	((156R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001101	((156R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001110	((156R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 001111	((156R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010000	((156R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010001	((156R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010010	((156R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010011	((156R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010100	((156R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010101	((156R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010110	((156R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 010111	((156R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011000	((156R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011001	((156R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011010	((156R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011011	((156R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011100	((156R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011101	((156R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011110	((156R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 011111	((156R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100000	((156R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100001	((156R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100010	((156R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100011	((156R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100100	((156R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100101	((156R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100110	((156R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 100111	((156R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101000	((156R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101001	((156R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101010	((156R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101011	((156R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101100	((156R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101101	((156R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101110	((156R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 101111	((156R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110000	((156R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110001	((156R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110010	((156R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110011	((156R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110100	((156R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110101	((156R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110110	((156R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 110111	((156R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111000	((156R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111001	((156R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111010	((156R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111011	((156R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111100	((156R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111101	((156R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111110	((156R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	VRN3 5-0 = 111111	((156R - 126R) / 450R) * (VSNR - VGSN) + VGSN

Table 5.25: VinN14

Reference voltage	Macro adjustment value	VinN15 formula
VinN15	VRN4 5-0 = 000000	((146R / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000001	((146R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000010	((146R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000011	((146R - 6R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000100	((146R - 8R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000101	((146R - 10R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000110	((146R - 12R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 000111	((146R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001000	((146R - 16R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001001	((146R - 18R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001010	((146R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001011	((146R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001100	((146R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001101	((146R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001110	((146R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 001111	((146R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010000	((146R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010001	((146R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010010	((146R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010011	((146R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010100	((146R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010101	((146R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010110	((146R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 010111	((146R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011000	((146R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011001	((146R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011010	((146R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011011	((146R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011100	((146R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011101	((146R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011110	((146R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 011111	((146R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100000	((146R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100001	((146R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100010	((146R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100011	((146R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100100	((146R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100101	((146R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100110	((146R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 100111	((146R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101000	((146R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101001	((146R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101010	((146R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101011	((146R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101100	((146R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101101	((146R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101110	((146R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 101111	((146R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110000	((146R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110001	((146R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110010	((146R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110011	((146R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110100	((146R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110101	((146R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110110	((146R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 110111	((146R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111000	((146R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111001	((146R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111010	((146R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111011	((146R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111100	((146R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111101	((146R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111110	((146R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	VRN4 5-0 = 111111	((146R - 126R) / 450R) * (VSNR - VGSN) + VGSN

Table 5.26: VinN15

Reference voltage	Macro adjustment value	VinN16 formula
VinN16	VRN5 5-0 = 000000	$(144R / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 000001	$((144R - 2R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 000010	$((144R - 4R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 000011	$((144R - 6R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 000100	$((144R - 8R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 000101	$((144R - 10R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 000110	$((144R - 12R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 000111	$((144R - 14R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 001000	$((144R - 16R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 001001	$((144R - 18R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 001010	$((144R - 20R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 001011	$((144R - 22R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 001100	$((144R - 24R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 001101	$((144R - 26R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 001110	$((144R - 28R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 001111	$((144R - 30R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 010000	$((144R - 32R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 010001	$((144R - 34R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 010010	$((144R - 36R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 010011	$((144R - 38R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 010100	$((144R - 40R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 010101	$((144R - 42R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 010110	$((144R - 44R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 010111	$((144R - 46R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 011000	$((144R - 48R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 011001	$((144R - 50R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 011010	$((144R - 52R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 011011	$((144R - 54R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 011100	$((144R - 56R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 011101	$((144R - 58R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 011110	$((144R - 60R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 011111	$((144R - 62R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 100000	$((144R - 64R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 100001	$((144R - 66R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 100010	$((144R - 68R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 100011	$((144R - 70R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 100100	$((144R - 72R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 100101	$((144R - 74R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 100110	$((144R - 76R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 100111	$((144R - 78R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 101000	$((144R - 80R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 101001	$((144R - 82R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 101010	$((144R - 84R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 101011	$((144R - 86R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 101100	$((144R - 88R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 101101	$((144R - 90R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 101110	$((144R - 92R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 101111	$((144R - 94R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 110000	$((144R - 96R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 110001	$((144R - 98R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 110010	$((144R - 100R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 110011	$((144R - 102R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 110100	$((144R - 104R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 110101	$((144R - 106R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 110110	$((144R - 108R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 110111	$((144R - 110R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 111000	$((144R - 112R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 111001	$((144R - 114R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 111010	$((144R - 116R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 111011	$((144R - 118R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 111100	$((144R - 120R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 111101	$((144R - 122R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 111110	$((144R - 124R) / 450R) * (VSNR - VGSN) + VGSN$
	VRN5 5-0 = 111111	VGSN

Table 5.27: VinN16

Reference voltage	Macro adjustment value	VinN5 formula
VinN5	PRNO 6-0 = 0000000	(350R / 450R) (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0000001	((350R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0000010	((350R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0000011	((350R - 6R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0000100	((350R - 8R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0000101	((350R - 10R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0000110	((350R - 12R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0000111	((350R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0001000	((350R - 16R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0001001	((350R - 18R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0001010	((350R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0001011	((350R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0001100	((350R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0001101	((350R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0001110	((350R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0001111	((350R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0010000	((350R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0010001	((350R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0010010	((350R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0010011	((350R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0010100	((350R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0010101	((350R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0010110	((350R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0010111	((350R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0011000	((350R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0011001	((350R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0011010	((350R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0011011	((350R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0011100	((350R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0011101	((350R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0011110	((350R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0011111	((350R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0100000	((350R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0100001	((350R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0100010	((350R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0100011	((350R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0100100	((350R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0100101	((350R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0100110	((350R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0100111	((350R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0101000	((350R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0101001	((350R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0101010	((350R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0101011	((350R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0101100	((350R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0101101	((350R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0101110	((350R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0101111	((350R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0110000	((350R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0110001	((350R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0110010	((350R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0110011	((350R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0110100	((350R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0110101	((350R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0110110	((350R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0110111	((350R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0111000	((350R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0111001	((350R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0111010	((350R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0111011	((350R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0111100	((350R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0111101	((350R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0111110	((350R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 0111111	((350R - 126R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 1000000	((350R - 128R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 1000001	((350R - 130R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 1000010	((350R - 132R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 1000011	((350R - 134R) / 450R) * (VSNR - VGSN) + VGSN
	PRNO 6-0 = 1000100	((350R - 136R) / 450R) * (VSNR - VGSN) + VGSN

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Reference voltage	Macro adjustment value	VinN5 formula
	PRNO 6-0 = 1000101	$((350R - 138R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 1000110	$((350R - 140R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 1000111	$((350R - 142R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 1001000	$((350R - 144R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 1001001	$((350R - 146R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 1001010	$((350R - 148R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 1001011	$((350R - 150R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 1001100	$((350R - 152R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 1001101	$((350R - 154R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 1001110	$((350R - 156R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 1001111	$((350R - 158R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 1010000	$((350R - 160R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 1010001	$((350R - 162R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 1010010	$((350R - 164R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 1010011	$((350R - 166R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 1010100	$((350R - 168R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 1010101	$((350R - 170R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 1010110	$((350R - 172R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 1010111	$((350R - 174R) / 450R) * (VSNR - VGSN) + VGSN$
	PRNO 6-0 = 1011000	inhibit
	PRNO 6-0 = 1011001	inhibit
	PRNO 6-0 = 1011010	inhibit
	PRNO 6-0 = 1011011	inhibit
	PRNO 6-0 = 1011100	inhibit
	PRNO 6-0 = 1011101	inhibit
	PRNO 6-0 = 1011110	inhibit
	PRNO 6-0 = 1011111	inhibit
	PRNO 6-0 = 1100000	inhibit
	PRNO 6-0 = 1100001	inhibit
	PRNO 6-0 = 1100010	inhibit
	PRNO 6-0 = 1100011	inhibit
	PRNO 6-0 = 1100100	inhibit
	PRNO 6-0 = 1100101	inhibit
	PRNO 6-0 = 1100110	inhibit
	PRNO 6-0 = 1100111	inhibit
	PRNO 6-0 = 1101000	inhibit
	PRNO 6-0 = 1101001	inhibit
	PRNO 6-0 = 1101010	inhibit
	PRNO 6-0 = 1101011	inhibit
	PRNO 6-0 = 1101100	inhibit
	PRNO 6-0 = 1101101	inhibit
	PRNO 6-0 = 1101110	inhibit
	PRNO 6-0 = 1101111	inhibit
	PRNO 6-0 = 1110000	inhibit
	PRNO 6-0 = 1110001	inhibit
	PRNO 6-0 = 1110010	inhibit
	PRNO 6-0 = 1110011	inhibit
	PRNO 6-0 = 1110100	inhibit
	PRNO 6-0 = 1110101	inhibit
	PRNO 6-0 = 1110110	inhibit
	PRNO 6-0 = 1110111	inhibit
	PRNO 6-0 = 1111000	inhibit
	PRNO 6-0 = 1111001	inhibit
	PRNO 6-0 = 1111010	inhibit
	PRNO 6-0 = 1111011	inhibit
	PRNO 6-0 = 1111100	inhibit
	PRNO 6-0 = 1111101	inhibit
	PRNO 6-0 = 1111110	inhibit
	PRNO 6-0 = 1111111	inhibit

Table 5.28: VinN5

Reference voltage	Macro adjustment value	VinN11 formula
VinN11	PRN1 6-0 = 0000000	(274R / 450R) (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000001	((274R - 2R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000010	((274R - 4R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000011	((274R - 6R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000100	((274R - 8R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000101	((274R - 10R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000110	((274R - 12R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0000111	((274R - 14R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001000	((274R - 16R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001001	((274R - 18R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001010	((274R - 20R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001011	((274R - 22R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001100	((274R - 24R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001101	((274R - 26R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001110	((274R - 28R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0001111	((274R - 30R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010000	((274R - 32R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010001	((274R - 34R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010010	((274R - 36R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010011	((274R - 38R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010100	((274R - 40R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010101	((274R - 42R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010110	((274R - 44R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0010111	((274R - 46R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011000	((274R - 48R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011001	((274R - 50R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011010	((274R - 52R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011011	((274R - 54R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011100	((274R - 56R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011101	((274R - 58R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011110	((274R - 60R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0011111	((274R - 62R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100000	((274R - 64R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100001	((274R - 66R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100010	((274R - 68R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100011	((274R - 70R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100100	((274R - 72R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100101	((274R - 74R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100110	((274R - 76R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0100111	((274R - 78R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101000	((274R - 80R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101001	((274R - 82R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101010	((274R - 84R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101011	((274R - 86R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101100	((274R - 88R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101101	((274R - 90R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101110	((274R - 92R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0101111	((274R - 94R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110000	((274R - 96R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110001	((274R - 98R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110010	((274R - 100R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110011	((274R - 102R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110100	((274R - 104R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110101	((274R - 106R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110110	((274R - 108R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0110111	((274R - 110R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111000	((274R - 112R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111001	((274R - 114R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111010	((274R - 116R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111011	((274R - 118R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111100	((274R - 120R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111101	((274R - 122R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111110	((274R - 124R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 0111111	((274R - 126R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000000	((274R - 128R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000001	((274R - 130R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000010	((274R - 132R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000011	((274R - 134R) / 450R) * (VSNR - VGSN) + VGSN
	PRN1 6-0 = 1000100	((274R - 136R) / 450R) * (VSNR - VGSN) + VGSN

Reference voltage	Macro adjustment value	VinN11 formula
	PRN1 6-0 = 1000101	$((274R - 138R) / 450R) * (VSNR - VGSN) + VGSN$
	PRN1 6-0 = 1000110	$((274R - 140R) / 450R) * (VSNR - VGSN) + VGSN$
	PRN1 6-0 = 1000111	$((274R - 142R) / 450R) * (VSNR - VGSN) + VGSN$
	PRN1 6-0 = 1001000	$((274R - 144R) / 450R) * (VSNR - VGSN) + VGSN$
	PRN1 6-0 = 1001001	$((274R - 146R) / 450R) * (VSNR - VGSN) + VGSN$
	PRN1 6-0 = 1001010	$((274R - 148R) / 450R) * (VSNR - VGSN) + VGSN$
	PRN1 6-0 = 1001011	$((274R - 150R) / 450R) * (VSNR - VGSN) + VGSN$
	PRN1 6-0 = 1001100	$((274R - 152R) / 450R) * (VSNR - VGSN) + VGSN$
	PRN1 6-0 = 1001101	$((274R - 154R) / 450R) * (VSNR - VGSN) + VGSN$
	PRN1 6-0 = 1001110	$((274R - 156R) / 450R) * (VSNR - VGSN) + VGSN$
	PRN1 6-0 = 1001111	$((274R - 158R) / 450R) * (VSNR - VGSN) + VGSN$
	PRN1 6-0 = 1010000	$((274R - 160R) / 450R) * (VSNR - VGSN) + VGSN$
	PRN1 6-0 = 1010001	$((274R - 162R) / 450R) * (VSNR - VGSN) + VGSN$
	PRN1 6-0 = 1010010	$((274R - 164R) / 450R) * (VSNR - VGSN) + VGSN$
	PRN1 6-0 = 1010011	$((274R - 166R) / 450R) * (VSNR - VGSN) + VGSN$
	PRN1 6-0 = 1010100	$((274R - 168R) / 450R) * (VSNR - VGSN) + VGSN$
	PRN1 6-0 = 1010101	$((274R - 170R) / 450R) * (VSNR - VGSN) + VGSN$
	PRN1 6-0 = 1010110	$((274R - 172R) / 450R) * (VSNR - VGSN) + VGSN$
	PRN1 6-0 = 1010111	$((274R - 174R) / 450R) * (VSNR - VGSN) + VGSN$
	PRN1 6-0 = 1011000	inhibit
	PRN1 6-0 = 1011001	inhibit
	PRN1 6-0 = 1011010	inhibit
	PRN1 6-0 = 1011011	inhibit
	PRN1 6-0 = 1011100	inhibit
	PRN1 6-0 = 1011101	inhibit
	PRN1 6-0 = 1011110	inhibit
	PRN1 6-0 = 1011111	inhibit
	PRN1 6-0 = 1100000	inhibit
	PRN1 6-0 = 1100001	inhibit
	PRN1 6-0 = 1100010	inhibit
	PRN1 6-0 = 1100011	inhibit
	PRN1 6-0 = 1100100	inhibit
	PRN1 6-0 = 1100101	inhibit
	PRN1 6-0 = 1100110	inhibit
	PRN1 6-0 = 1100111	inhibit
	PRN1 6-0 = 1101000	inhibit
	PRN1 6-0 = 1101001	inhibit
	PRN1 6-0 = 1101010	inhibit
	PRN1 6-0 = 1101011	inhibit
	PRN1 6-0 = 1101100	inhibit
	PRN1 6-0 = 1101101	inhibit
	PRN1 6-0 = 1101110	inhibit
	PRN1 6-0 = 1101111	inhibit
	PRN1 6-0 = 1110000	inhibit
	PRN1 6-0 = 1110001	inhibit
	PRN1 6-0 = 1110010	inhibit
	PRN1 6-0 = 1110011	inhibit
	PRN1 6-0 = 1110100	inhibit
	PRN1 6-0 = 1110101	inhibit
	PRN1 6-0 = 1110110	inhibit
	PRN1 6-0 = 1110111	inhibit
	PRN1 6-0 = 1111000	inhibit
	PRN1 6-0 = 1111001	inhibit
	PRN1 6-0 = 1111010	inhibit
	PRN1 6-0 = 1111011	inhibit
	PRN1 6-0 = 1111100	inhibit
	PRN1 6-0 = 1111101	inhibit
	PRN1 6-0 = 1111110	inhibit
	PRN1 6-0 = 1111111	inhibit

Table 5.29: VinN11

Reference voltage	Macro adjustment value	VinN3 formula
VinN3	PKNO 4-0 = 00000	$(47R / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 00001	$((47R - 1R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 00010	$((47R - 2R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 00011	$((47R - 3R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 00100	$((47R - 4R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 00101	$((47R - 5R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 00110	$((47R - 6R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 00111	$((47R - 7R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 01000	$((47R - 8R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 01001	$((47R - 9R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 01010	$((47R - 10R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 01011	$((47R - 11R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 01100	$((47R - 12R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 01101	$((47R - 13R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 01110	$((47R - 14R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 01111	$((47R - 15R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 10000	$((47R - 16R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 10001	$((47R - 17R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 10010	$((47R - 18R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 10011	$((47R - 19R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 10100	$((47R - 20R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 10101	$((47R - 21R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 10110	$((47R - 22R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 10111	$((47R - 23R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 11000	$((47R - 24R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 11001	$((47R - 25R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 11010	$((47R - 26R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 11011	$((47R - 27R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 11100	$((47R - 28R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 11101	$((47R - 29R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 11110	$((47R - 30R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKNO 4-0 = 11111	$((47R - 31R) / 48R) * (VinN2 - VinN5) + VinN5$

Table 5.30: VinN3

Reference voltage	Macro adjustment value	VinN4 formula
VinN4	PKN1 4-0 = 00000	$(32R / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 00001	$((32R - 1R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 00010	$((32R - 2R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 00011	$((32R - 3R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 00100	$((32R - 4R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 00101	$((32R - 5R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 00110	$((32R - 6R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 00111	$((32R - 7R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 01000	$((32R - 8R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 01001	$((32R - 9R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 01010	$((32R - 10R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 01011	$((32R - 11R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 01100	$((32R - 12R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 01101	$((32R - 13R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 01110	$((32R - 14R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 01111	$((32R - 15R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 10000	$((32R - 16R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 10001	$((32R - 17R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 10010	$((32R - 18R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 10011	$((32R - 19R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 10100	$((32R - 20R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 10101	$((32R - 21R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 10110	$((32R - 22R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 10111	$((32R - 23R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 11000	$((32R - 24R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 11001	$((32R - 25R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 11010	$((32R - 26R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 11011	$((32R - 27R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 11100	$((32R - 28R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 11101	$((32R - 29R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 11110	$((32R - 30R) / 48R) * (VinN2 - VinN5) + VinN5$
	PKN1 4-0 = 11111	$((32R - 31R) / 48R) * (VinN2 - VinN5) + VinN5$

Table 5.31: VinN4

Reference voltage	Macro adjustment value	VinN6 formula
VinN6	PKN2 4-0 = 00000	$(220R / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 00001	$((220R - 3R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 00010	$((220R - 6R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 00011	$((220R - 9R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 00100	$((220R - 12R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 00101	$((220R - 15R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 00110	$((220R - 18R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 00111	$((220R - 21R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 01000	$((220R - 24R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 01001	$((220R - 27R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 01010	$((220R - 30R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 01011	$((220R - 33R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 01100	$((220R - 36R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 01101	$((220R - 39R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 01110	$((220R - 42R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 01111	$((220R - 45R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 10000	$((220R - 48R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 10001	$((220R - 51R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 10010	$((220R - 54R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 10011	$((220R - 57R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 10100	$((220R - 60R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 10101	$((220R - 63R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 10110	$((220R - 66R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 10111	$((220R - 69R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 11000	$((220R - 72R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 11001	$((220R - 75R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 11010	$((220R - 78R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 11011	$((220R - 81R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 11100	$((220R - 84R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 11101	$((220R - 87R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 11110	$((220R - 90R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN2 4-0 = 11111	$((220R - 93R) / 223R) * (VinN5 - VinN11) + VinN11$

Table 5.32: VinN6

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Reference voltage	Macro adjustment value	VinN7 formula
VinN7	PKN3 4-0 = 00000	$(193R / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 00001	$((193R - 3R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 00010	$((193R - 6R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 00011	$((193R - 9R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 00100	$((193R - 12R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 00101	$((193R - 15R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 00110	$((193R - 18R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 00111	$((193R - 21R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 01000	$((193R - 24R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 01001	$((193R - 27R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 01010	$((193R - 30R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 01011	$((193R - 33R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 01100	$((193R - 36R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 01101	$((193R - 39R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 01110	$((193R - 42R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 01111	$((193R - 45R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 10000	$((193R - 48R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 10001	$((193R - 51R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 10010	$((193R - 54R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 10011	$((193R - 57R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 10100	$((193R - 60R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 10101	$((193R - 63R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 10110	$((193R - 66R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 10111	$((193R - 69R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 11000	$((193R - 72R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 11001	$((193R - 75R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 11010	$((193R - 78R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 11011	$((193R - 81R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 11100	$((193R - 84R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 11101	$((193R - 87R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 11110	$((193R - 90R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN3 4-0 = 11111	$((193R - 93R) / 223R) * (VinN5 - VinN11) + VinN11$

Table 5.33: VinN7

Reference voltage	Macro adjustment value	VinN8 formula
VinN8	PKN4 4-0 = 00000	$(158R / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 00001	$((158R - 3R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 00010	$((158R - 6R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 00011	$((158R - 9R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 00100	$((158R - 12R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 00101	$((158R - 15R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 00110	$((158R - 18R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 00111	$((158R - 21R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 01000	$((158R - 24R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 01001	$((158R - 27R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 01010	$((158R - 30R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 01011	$((158R - 33R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 01100	$((158R - 36R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 01101	$((158R - 39R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 01110	$((158R - 42R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 01111	$((158R - 45R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 10000	$((158R - 48R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 10001	$((158R - 51R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 10010	$((158R - 54R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 10011	$((158R - 57R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 10100	$((158R - 60R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 10101	$((158R - 63R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 10110	$((158R - 66R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 10111	$((158R - 69R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 11000	$((158R - 72R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 11001	$((158R - 75R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 11010	$((158R - 78R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 11011	$((158R - 81R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 11100	$((158R - 84R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 11101	$((158R - 87R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 11110	$((158R - 90R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN4 4-0 = 11111	$((158R - 93R) / 223R) * (VinN5 - VinN11) + VinN11$

Table 5.34: VinN8

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Reference voltage	Macro adjustment value	VinN9 formula
VinN9	PKN5 4-0 = 00000	$(123R / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 00001	$((123R - 3R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 00010	$((123R - 6R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 00011	$((123R - 9R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 00100	$((123R - 12R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 00101	$((123R - 15R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 00110	$((123R - 18R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 00111	$((123R - 21R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 01000	$((123R - 24R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 01001	$((123R - 27R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 01010	$((123R - 30R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 01011	$((123R - 33R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 01100	$((123R - 36R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 01101	$((123R - 39R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 01110	$((123R - 42R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 01111	$((123R - 45R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 10000	$((123R - 48R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 10001	$((123R - 51R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 10010	$((123R - 54R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 10011	$((123R - 57R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 10100	$((123R - 60R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 10101	$((123R - 63R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 10110	$((123R - 66R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 10111	$((123R - 69R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 11000	$((123R - 72R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 11001	$((123R - 75R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 11010	$((123R - 78R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 11011	$((123R - 81R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 11100	$((123R - 84R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 11101	$((123R - 87R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 11110	$((123R - 90R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN5 4-0 = 11111	$((123R - 93R) / 223R) * (VinN5 - VinN11) + VinN11$

Table 5.35: VinN9

Reference voltage	Macro adjustment value	VinN10 formula
VinN10	PKN6 4-0 = 00000	$(96R / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 00001	$((96R - 3R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 00010	$((96R - 6R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 00011	$((96R - 9R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 00100	$((96R - 12R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 00101	$((96R - 15R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 00110	$((96R - 18R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 00111	$((96R - 21R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 01000	$((96R - 24R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 01001	$((96R - 27R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 01010	$((96R - 30R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 01011	$((96R - 33R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 01100	$((96R - 36R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 01101	$((96R - 39R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 01110	$((96R - 42R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 01111	$((96R - 45R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 10000	$((96R - 48R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 10001	$((96R - 51R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 10010	$((96R - 54R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 10011	$((96R - 57R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 10100	$((96R - 60R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 10101	$((96R - 63R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 10110	$((96R - 66R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 10111	$((96R - 69R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 11000	$((96R - 72R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 11001	$((96R - 75R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 11010	$((96R - 78R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 11011	$((96R - 81R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 11100	$((96R - 84R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 11101	$((96R - 87R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 11110	$((96R - 90R) / 223R) * (VinN5 - VinN11) + VinN11$
	PKN6 4-0 = 11111	$((96R - 93R) / 223R) * (VinN5 - VinN11) + VinN11$

Table 5.36: VinN10

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Reference voltage	Macro adjustment value	VinN12 formula
VinN12	PKN7 4-0 = 00000	$(47R / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 00001	$((47R - 1R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 00010	$((47R - 2R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 00011	$((47R - 3R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 00100	$((47R - 4R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 00101	$((47R - 5R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 00110	$((47R - 6R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 00111	$((47R - 7R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 01000	$((47R - 8R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 01001	$((47R - 9R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 01010	$((47R - 10R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 01011	$((47R - 11R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 01100	$((47R - 12R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 01101	$((47R - 13R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 01110	$((47R - 14R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 01111	$((47R - 15R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 10000	$((47R - 16R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 10001	$((47R - 17R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 10010	$((47R - 18R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 10011	$((47R - 19R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 10100	$((47R - 20R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 10101	$((47R - 21R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 10110	$((47R - 22R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 10111	$((47R - 23R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 11000	$((47R - 24R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 11001	$((47R - 25R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 11010	$((47R - 26R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 11011	$((47R - 27R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 11100	$((47R - 28R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 11101	$((47R - 29R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 11110	$((47R - 30R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN7 4-0 = 11111	$((47R - 31R) / 48R) * (VinN11 - VinN14) + VinN14$

Table 5.37: VinN12

Reference voltage	Macro adjustment value	VinN13 formula
VinN13	PKN8 4-0 = 00000	$(32R / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 00001	$((32R - 1R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 00010	$((32R - 2R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 00011	$((32R - 3R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 00100	$((32R - 4R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 00101	$((32R - 5R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 00110	$((32R - 6R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 00111	$((32R - 7R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 01000	$((32R - 8R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 01001	$((32R - 9R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 01010	$((32R - 10R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 01011	$((32R - 11R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 01100	$((32R - 12R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 01101	$((32R - 13R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 01110	$((32R - 14R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 01111	$((32R - 15R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 10000	$((32R - 16R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 10001	$((32R - 17R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 10010	$((32R - 18R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 10011	$((32R - 19R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 10100	$((32R - 20R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 10101	$((32R - 21R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 10110	$((32R - 22R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 10111	$((32R - 23R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 11000	$((32R - 24R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 11001	$((32R - 25R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 11010	$((32R - 26R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 11011	$((32R - 27R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 11100	$((32R - 28R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 11101	$((32R - 29R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 11110	$((32R - 30R) / 48R) * (VinN11 - VinN14) + VinN14$
	PKN8 4-0 = 11111	$((32R - 31R) / 48R) * (VinN11 - VinN14) + VinN14$

Table 5.38: VinN13

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Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VinP0	V32	VinP8
V1	VinP1	V33	VinP8 - (VinP8 - VinP9)*(1R/6R)
V2	VinP2	V34	VinP8 - (VinP8 - VinP9)*(2R/6R)
V3	VinP3	V35	VinP8 - (VinP8 - VinP9)*(3R/6R)
V4	VinP3 - (VinP3 - VinP4)*(1R/4R)	V36	VinP8 - (VinP8 - VinP9)*(4R/6R)
V5	VinP3 - (VinP3 - VinP4)*(2R/4R)	V37	VinP8 - (VinP8 - VinP9)*(5R/6R)
V6	VinP3 - (VinP3 - VinP4)*(3R/4R)	V38	VinP9
V7	VinP4	V39	VinP9 - (VinP9 - VinP10)*(1R/6R)
V8	VinP4 - (VinP4 - VinP5)*(1R/6R)	V40	VinP9 - (VinP9 - VinP10)*(2R/6R)
V9	VinP4 - (VinP4 - VinP5)*(2R/6R)	V41	VinP9 - (VinP9 - VinP10)*(3R/6R)
V10	VinP4 - (VinP4 - VinP5)*(3R/6R)	V42	VinP9 - (VinP9 - VinP10)*(4R/6R)
V11	VinP4 - (VinP4 - VinP5)*(4R/6R)	V43	VinP9 - (VinP9 - VinP10)*(5R/6R)
V12	VinP4 - (VinP4 - VinP5)*(5R/6R)	V44	VinP10
V13	VinP5	V45	VinP10 - (VinP10 - VinP11)*(1R/6R)
V14	VinP5 - (VinP5 - VinP6)*(1R/6R)	V46	VinP10 - (VinP10 - VinP11)*(2R/6R)
V15	VinP5 - (VinP5 - VinP6)*(2R/6R)	V47	VinP10 - (VinP10 - VinP11)*(3R/6R)
V16	VinP5 - (VinP5 - VinP6)*(3R/6R)	V48	VinP10 - (VinP10 - VinP11)*(4R/6R)
V17	VinP5 - (VinP5 - VinP6)*(4R/6R)	V49	VinP10 - (VinP10 - VinP11)*(5R/6R)
V18	VinP5 - (VinP5 - VinP6)*(5R/6R)	V50	VinP11
V19	VinP6	V51	VinP11 - (VinP11 - VinP12)*(1R/6R)
V20	VinP6 - (VinP6 - VinP7)*(1R/6R)	V52	VinP11 - (VinP11 - VinP12)*(2R/6R)
V21	VinP6 - (VinP6 - VinP7)*(2R/6R)	V53	VinP11 - (VinP11 - VinP12)*(3R/6R)
V22	VinP6 - (VinP6 - VinP7)*(3R/6R)	V54	VinP11 - (VinP11 - VinP12)*(4R/6R)
V23	VinP6 - (VinP6 - VinP7)*(4R/6R)	V55	VinP11 - (VinP11 - VinP12)*(5R/6R)
V24	VinP6 - (VinP6 - VinP7)*(5R/6R)	V56	VinP12
V25	VinP7	V57	VinP12 - (VinP12 - VinP13)*(1R/4R)
V26	VinP7 - (VinP7 - VinP8)*(1R/7.5R)	V58	VinP12 - (VinP12 - VinP13)*(2R/4R)
V27	VinP7 - (VinP7 - VinP8)*(2R/7.5R)	V59	VinP12 - (VinP12 - VinP13)*(3R/4R)
V28	VinP7 - (VinP7 - VinP8)*(3R/7.5R)	V60	VinP13
V29	VinP7 - (VinP7 - VinP8)*(4R/7.5R)	V61	VinP14
V30	VinP7 - (VinP7 - VinP8)*(5R/7.5R)	V62	VinP15
V31	VinP7 - (VinP7 - VinP8)*(6R/7.5R)	V63	VinP16

Table 5.39: Voltage calculation formula of 64-grayscale voltage (positive polarity)

Grayscale voltage	Formula
V0	VinN0
V1	VinN1
V2	VinN2
V3	VinN3
V4	VinN3 - (VinN3 - VinN4)*(1R/4R)
V5	VinN3 - (VinN3 - VinN4)*(2R/4R)
V6	VinN3 - (VinN3 - VinN4)*(3R/4R)
V7	VinN4
V8	VinN4 - (VinN4 - VinN5)*(1R/6R)
V9	VinN4 - (VinN4 - VinN5)*(2R/6R)
V10	VinN4 - (VinN4 - VinN5)*(3R/6R)
V11	VinN4 - (VinN4 - VinN5)*(4R/6R)
V12	VinN4 - (VinN4 - VinN5)*(5R/6R)
V13	VinN5
V14	VinN5 - (VinN5 - VinN6)*(1R/6R)
V15	VinN5 - (VinN5 - VinN6)*(2R/6R)
V16	VinN5 - (VinN5 - VinN6)*(3R/6R)
V17	VinN5 - (VinN5 - VinN6)*(4R/6R)
V18	VinN5 - (VinN5 - VinN6)*(5R/6R)
V19	VinN6
V20	VinN6 - (VinN6 - VinN7)*(1R/6R)
V21	VinN6 - (VinN6 - VinN7)*(2R/6R)
V22	VinN6 - (VinN6 - VinN7)*(3R/6R)
V23	VinN6 - (VinN6 - VinN7)*(4R/6R)
V24	VinN6 - (VinN6 - VinN7)*(5R/6R)
V25	VinP7
V26	VinP7 - (VinP7 - VinP8)*(1R/7.5R)
V27	VinP7 - (VinP7 - VinP8)*(2R/7.5R)
V28	VinP7 - (VinP7 - VinP8)*(3R/7.5R)
V29	VinP7 - (VinP7 - VinP8)*(4R/7.5R)
V30	VinP7 - (VinP7 - VinP8)*(5R/7.5R)
V31	VinP7 - (VinP7 - VinP8)*(6R/7.5R)

Grayscale voltage	Formula
V32	VinP8
V33	VinP8 - (VinP8 - VinP9)*(1R/6R)
V34	VinP8 - (VinP8 - VinP9)*(2R/6R)
V35	VinP8 - (VinP8 - VinP9)*(3R/6R)
V36	VinP8 - (VinP8 - VinP9)*(4R/6R)
V37	VinP8 - (VinP8 - VinP9)*(5R/6R)
V38	VinN9
V39	VinN9 - (VinN9 - VinN10)*(1R/6R)
V40	VinN9 - (VinN9 - VinN10)*(2R/6R)
V41	VinN9 - (VinN9 - VinN10)*(3R/6R)
V42	VinN9 - (VinN9 - VinN10)*(4R/6R)
V43	VinN9 - (VinN9 - VinN10)*(5R/6R)
V44	VinN10
V45	VinN10 - (VinN10 - VinN11)*(1R/6R)
V46	VinN10 - (VinN10 - VinN11)*(2R/6R)
V47	VinN10 - (VinN10 - VinN11)*(3R/6R)
V48	VinN10 - (VinN10 - VinN11)*(4R/6R)
V49	VinN10 - (VinN10 - VinN11)*(5R/6R)
V50	VinN11
V51	VinN11 - (VinN11 - VinN12)*(1R/6R)
V52	VinN11 - (VinN11 - VinN12)*(2R/6R)
V53	VinN11 - (VinN11 - VinN12)*(3R/6R)
V54	VinN11 - (VinN11 - VinN12)*(4R/6R)
V55	VinN11 - (VinN11 - VinN12)*(5R/6R)
V56	VinN12
V57	VinN12 - (VinN12 - VinN13)*(1R/4R)
V58	VinN12 - (VinN12 - VinN13)*(2R/4R)
V59	VinN12 - (VinN12 - VinN13)*(3R/4R)
V60	VinN13
V61	VinN14
V62	VinN15
V63	VinN16

Table 5.40: Voltage calculation formula of 64-grayscale voltage (negative polarity)

Grayscale voltage	Formula
VV0	V0
VV1	$V0 - (V0 - V1)*(4R/16R)$
VV2	$V0 - (V0 - V1)*(8R/16R)$
VV3	$V0 - (V0 - V1)*(12R/16R)$
VV4	V1
VV5	$V1 - (V1 - V2)*(4R/16R)$
VV6	$V1 - (V1 - V2)*(8R/16R)$
VV7	$V1 - (V1 - V2)*(12R/16R)$
VV8	V2
VV9	$V2 - (V2 - V3)*(4R/16R)$
VV10	$V2 - (V2 - V3)*(8R/16R)$
VV11	$V2 - (V2 - V3)*(12R/16R)$
VV12	V3
VV13	$V3 - (V3 - V4)*(2R/8R)$
VV14	$V3 - (V3 - V4)*(4R/8R)$
VV15	$V3 - (V3 - V4)*(6R/8R)$
VV16	V4
VV17	$V4 - (V4 - V5)*(2R/8R)$
VV18	$V4 - (V4 - V5)*(4R/8R)$
VV19	$V4 - (V4 - V5)*(6R/8R)$
VV20	V5
VV21	$V5 - (V5 - V6)*(2R/8R)$
VV22	$V5 - (V5 - V6)*(4R/8R)$
VV23	$V5 - (V5 - V6)*(6R/8R)$
VV24	V6
VV25	$V6 - (V6 - V7)*(2R/8R)$
VV26	$V6 - (V6 - V7)*(4R/8R)$
VV27	$V6 - (V6 - V7)*(6R/8R)$
VV28	V7
VV29	$V7 - (V7 - V8)*(1.6R/6.4R)$
VV30	$V7 - (V7 - V8)*(3.2R/6.4R)$
VV31	$V7 - (V7 - V8)*(4.8R/6.4R)$
VV32	V8
VV33	$V8 - (V8 - V9)*(1.6R/6.4R)$
VV34	$V8 - (V8 - V9)*(3.2R/6.4R)$
VV35	$V8 - (V8 - V9)*(4.8R/6.4R)$
VV36	V9
VV37	$V9 - (V9 - V10)*(1.6R/6.4R)$
VV38	$V9 - (V9 - V10)*(3.2R/6.4R)$
VV39	$V9 - (V9 - V10)*(4.8R/6.4R)$
VV40	V10
VV41	$V10 - (V10 - V11)*(1.6R/6.4R)$
VV42	$V10 - (V10 - V11)*(3.2R/6.4R)$
VV43	$V10 - (V10 - V11)*(4.8R/6.4R)$

Grayscale voltage	Formula
VV44	V11
VV45	$V11 - (V11 - V12)*(1.6R/6.4R)$
VV46	$V11 - (V11 - V12)*(3.2R/6.4R)$
VV47	$V11 - (V11 - V12)*(4.8R/6.4R)$
VV48	V12
VV49	$V12 - (V12 - V13)*(1.6R/6.4R)$
VV50	$V12 - (V12 - V13)*(3.2R/6.4R)$
VV51	$V12 - (V12 - V13)*(4.8R/6.4R)$
VV52	V13
VV53	$V13 - (V13 - V14)*(1.6R/6.4R)$
VV54	$V13 - (V13 - V14)*(3.2R/6.4R)$
VV55	$V13 - (V13 - V14)*(4.8R/6.4R)$
VV56	V14
VV57	$V14 - (V14 - V15)*(1.6R/6.4R)$
VV58	$V14 - (V14 - V15)*(3.2R/6.4R)$
VV59	$V14 - (V14 - V15)*(4.8R/6.4R)$
VV60	V15
VV61	$V15 - (V15 - V16)*(1.6R/6.4R)$
VV62	$V15 - (V15 - V16)*(3.2R/6.4R)$
VV63	$V15 - (V15 - V16)*(4.8R/6.4R)$
VV64	V16
VV65	$V16 - (V16 - V17)*(1.6R/6.4R)$
VV66	$V16 - (V16 - V17)*(3.2R/6.4R)$
VV67	$V16 - (V16 - V17)*(4.8R/6.4R)$
VV68	V17
VV69	$V17 - (V17 - V18)*(1.6R/6.4R)$
VV70	$V17 - (V17 - V18)*(3.2R/6.4R)$
VV71	$V17 - (V17 - V18)*(4.8R/6.4R)$
VV72	V18
VV73	$V18 - (V18 - V19)*(1.6R/6.4R)$
VV74	$V18 - (V18 - V19)*(3.2R/6.4R)$
VV75	$V18 - (V18 - V19)*(4.8R/6.4R)$
VV76	V19
VV77	$V19 - (V19 - V20)*(1.6R/6.4R)$
VV78	$V19 - (V19 - V20)*(3.2R/6.4R)$
VV79	$V19 - (V19 - V20)*(4.8R/6.4R)$
VV80	V20
VV81	$V20 - (V20 - V21)*(1.6R/6.4R)$
VV82	$V20 - (V20 - V21)*(3.2R/6.4R)$
VV83	$V20 - (V20 - V21)*(4.8R/6.4R)$
VV84	V21
VV85	$V21 - (V21 - V22)*(1.6R/6.4R)$
VV86	$V21 - (V21 - V22)*(3.2R/6.4R)$
VV87	$V21 - (V21 - V22)*(4.8R/6.4R)$

Grayscale voltage	Formula	Grayscale voltage	Formula
VV88	V22	VV132	V32 - (V32 - V33)*(1.6R/6.4R)
VV89	V22 - (V22 - V23)*(1.6R/6.4R)	VV133	V32 - (V32 - V33)*(3.2R/6.4R)
VV90	V22 - (V22 - V23)*(3.2R/6.4R)	VV134	V32 - (V32 - V33)*(4.8R/6.4R)
VV91	V22 - (V22 - V23)*(4.8R/6.4R)	VV135	V33
VV92	V23	VV136	V33 - (V33 - V34)*(1.6R/6.4R)
VV93	V23 - (V23 - V24)*(1.6R/6.4R)	VV137	V33 - (V33 - V34)*(3.2R/6.4R)
VV94	V23 - (V23 - V24)*(3.2R/6.4R)	VV138	V33 - (V33 - V34)*(4.8R/6.4R)
VV95	V23 - (V23 - V24)*(4.8R/6.4R)	VV139	V34
VV96	V24	VV140	V34 - (V34 - V35)*(1.6R/6.4R)
VV97	V24 - (V24 - V25)*(1.6R/6.4R)	VV141	V34 - (V34 - V35)*(3.2R/6.4R)
VV98	V24 - (V24 - V25)*(3.2R/6.4R)	VV142	V34 - (V34 - V35)*(4.8R/6.4R)
VV99	V24 - (V24 - V25)*(4.8R/6.4R)	VV143	V35
VV100	V25	VV144	V35 - (V35 - V36)*(1.6R/6.4R)
VV101	V25 - (V25 - V26)*(1.6R/6.4R)	VV145	V35 - (V35 - V36)*(3.2R/6.4R)
VV102	V25 - (V25 - V26)*(3.2R/6.4R)	VV146	V35 - (V35 - V36)*(4.8R/6.4R)
VV103	V25 - (V25 - V26)*(4.8R/6.4R)	VV147	V36
VV104	V26	VV148	V36 - (V36 - V37)*(1.6R/6.4R)
VV105	V26 - (V26 - V27)*(1.6R/6.4R)	VV149	V36 - (V36 - V37)*(3.2R/6.4R)
VV106	V26 - (V26 - V27)*(3.2R/6.4R)	VV150	V36 - (V36 - V37)*(4.8R/6.4R)
VV107	V26 - (V26 - V27)*(4.8R/6.4R)	VV151	V37
VV108	V27	VV152	V37 - (V37 - V38)*(1.6R/6.4R)
VV109	V27 - (V27 - V28)*(1.6R/6.4R)	VV153	V37 - (V37 - V38)*(3.2R/6.4R)
VV110	V27 - (V27 - V28)*(3.2R/6.4R)	VV154	V37 - (V37 - V38)*(4.8R/6.4R)
VV111	V27 - (V27 - V28)*(4.8R/6.4R)	VV155	V38
VV112	V28	VV156	V38 - (V38 - V39)*(1.6R/6.4R)
VV113	V28 - (V28 - V29)*(1.6R/6.4R)	VV157	V38 - (V38 - V39)*(3.2R/6.4R)
VV114	V28 - (V28 - V29)*(3.2R/6.4R)	VV158	V38 - (V38 - V39)*(4.8R/6.4R)
VV115	V28 - (V28 - V29)*(4.8R/6.4R)	VV159	V39
VV116	V29	VV160	V39 - (V39 - V40)*(1.6R/6.4R)
VV117	V29 - (V29 - V30)*(1.6R/6.4R)	VV161	V39 - (V39 - V40)*(3.2R/6.4R)
VV118	V29 - (V29 - V30)*(3.2R/6.4R)	VV162	V39 - (V39 - V40)*(4.8R/6.4R)
VV119	V29 - (V29 - V30)*(4.8R/6.4R)	VV163	V40
VV120	V30	VV164	V40 - (V40 - V41)*(1.6R/6.4R)
VV121	V30 - (V30 - V31)*(1.6R/6.4R)	VV165	V40 - (V40 - V41)*(3.2R/6.4R)
VV122	V30 - (V30 - V31)*(3.2R/6.4R)	VV166	V40 - (V40 - V41)*(4.8R/6.4R)
VV123	V30 - (V30 - V31)*(4.8R/6.4R)	VV167	V41
VV124	V31	VV168	V41 - (V41 - V42)*(1.6R/6.4R)
VV125	V31 - (V31 - V32)*(1.6R/11.2R)	VV169	V41 - (V41 - V42)*(3.2R/6.4R)
VV126	V31 - (V31 - V32)*(3.2R/11.2R)	VV170	V41 - (V41 - V42)*(4.8R/6.4R)
VV127	V31 - (V31 - V32)*(4.8R/11.2R)	VV171	V42
VV128	V31 - (V31 - V32)*(6.4R/11.2R)	VV172	V42 - (V42 - V43)*(1.6R/6.4R)
VV129	V31 - (V31 - V32)*(8R/11.2R)	VV173	V42 - (V42 - V43)*(3.2R/6.4R)
VV130	V31 - (V31 - V32)*(9.6R/11.2R)	VV174	V42 - (V42 - V43)*(4.8R/6.4R)
VV131	V32	VV175	V43

Grayscale voltage	Formula	Grayscale voltage	Formula
VV176	$V43 - (V43 - V44) * (1.6R/6.4R)$	VV216	$V53 - (V53 - V54) * (1.6R/6.4R)$
VV177	$V43 - (V43 - V44) * (3.2R/6.4R)$	VV217	$V53 - (V53 - V54) * (3.2R/6.4R)$
VV178	$V43 - (V43 - V44) * (4.8R/6.4R)$	VV218	$V53 - (V53 - V54) * (4.8R/6.4R)$
VV179	V44	VV219	V54
VV180	$V44 - (V44 - V45) * (1.6R/6.4R)$	VV220	$V54 - (V54 - V55) * (1.6R/6.4R)$
VV181	$V44 - (V44 - V45) * (3.2R/6.4R)$	VV221	$V54 - (V54 - V55) * (3.2R/6.4R)$
VV182	$V44 - (V44 - V45) * (4.8R/6.4R)$	VV222	$V54 - (V54 - V55) * (4.8R/6.4R)$
VV183	V45	VV223	V55
VV184	$V45 - (V45 - V46) * (1.6R/6.4R)$	VV224	$V55 - (V55 - V56) * (1.6R/6.4R)$
VV185	$V45 - (V45 - V46) * (3.2R/6.4R)$	VV225	$V55 - (V55 - V56) * (3.2R/6.4R)$
VV186	$V45 - (V45 - V46) * (4.8R/6.4R)$	VV226	$V55 - (V55 - V56) * (4.8R/6.4R)$
VV187	V46	VV227	V56
VV188	$V46 - (V46 - V47) * (1.6R/6.4R)$	VV228	$V56 - (V56 - V57) * (2R/8R)$
VV189	$V46 - (V46 - V47) * (3.2R/6.4R)$	VV229	$V56 - (V56 - V57) * (4R/8R)$
VV190	$V46 - (V46 - V47) * (4.8R/6.4R)$	VV230	$V56 - (V56 - V57) * (6R/8R)$
VV191	V47	VV231	V57
VV192	$V47 - (V47 - V48) * (1.6R/6.4R)$	VV232	$V57 - (V57 - V58) * (2R/8R)$
VV193	$V47 - (V47 - V48) * (3.2R/6.4R)$	VV233	$V57 - (V57 - V58) * (4R/8R)$
VV194	$V47 - (V47 - V48) * (4.8R/6.4R)$	VV234	$V57 - (V57 - V58) * (6R/8R)$
VV195	V48	VV235	V58
VV196	$V48 - (V48 - V49) * (1.6R/6.4R)$	VV236	$V58 - (V58 - V59) * (2R/8R)$
VV197	$V48 - (V48 - V49) * (3.2R/6.4R)$	VV237	$V58 - (V58 - V59) * (4R/8R)$
VV198	$V48 - (V48 - V49) * (4.8R/6.4R)$	VV238	$V58 - (V58 - V59) * (6R/8R)$
VV199	V49	VV239	V59
VV200	$V49 - (V49 - V50) * (1.6R/6.4R)$	VV240	$V59 - (V59 - V60) * (2R/8R)$
VV201	$V49 - (V49 - V50) * (3.2R/6.4R)$	VV241	$V59 - (V59 - V60) * (4R/8R)$
VV202	$V49 - (V49 - V50) * (4.8R/6.4R)$	VV242	$V59 - (V59 - V60) * (6R/8R)$
VV203	V50	VV243	V60
VV204	$V50 - (V50 - V51) * (1.6R/6.4R)$	VV244	$V60 - (V60 - V61) * (4R/16R)$
VV205	$V50 - (V50 - V51) * (3.2R/6.4R)$	VV245	$V60 - (V60 - V61) * (8R/16R)$
VV206	$V50 - (V50 - V51) * (4.8R/6.4R)$	VV246	$V60 - (V60 - V61) * (12R/16R)$
VV207	V51	VV247	V61
VV208	$V51 - (V51 - V52) * (1.6R/6.4R)$	VV248	$V61 - (V61 - V62) * (4R/16R)$
VV209	$V51 - (V51 - V52) * (3.2R/6.4R)$	VV249	$V61 - (V61 - V62) * (8R/16R)$
VV210	$V51 - (V51 - V52) * (4.8R/6.4R)$	VV250	$V61 - (V61 - V62) * (12R/16R)$
VV211	V52	VV251	V62
VV212	$V52 - (V52 - V53) * (1.6R/6.4R)$	VV252	$V62 - (V62 - V63) * (4R/16R)$
VV213	$V52 - (V52 - V53) * (3.2R/6.4R)$	VV253	$V62 - (V62 - V63) * (8R/16R)$
VV214	$V52 - (V52 - V53) * (4.8R/6.4R)$	VV254	$V62 - (V62 - V63) * (12R/16R)$
VV215	V53	VV255	V63

Table 5.41: Voltage calculation formula of 256-grayscale voltage (positive/negative polarity)

5.7.1 Gray voltage generator for digital gamma correction

The HX8379-A digital gamma correction can reach the independent gamma curve of RGB. HX8379-A utilizes DGC_LUT (Digital Gamma Correction Look Up Table) to change input data from 8-bit into 10-bit and sends 10-bit data to Dithering circuit, and then drive Source Driver via Dithering circuit. The following of the block diagram of the function.

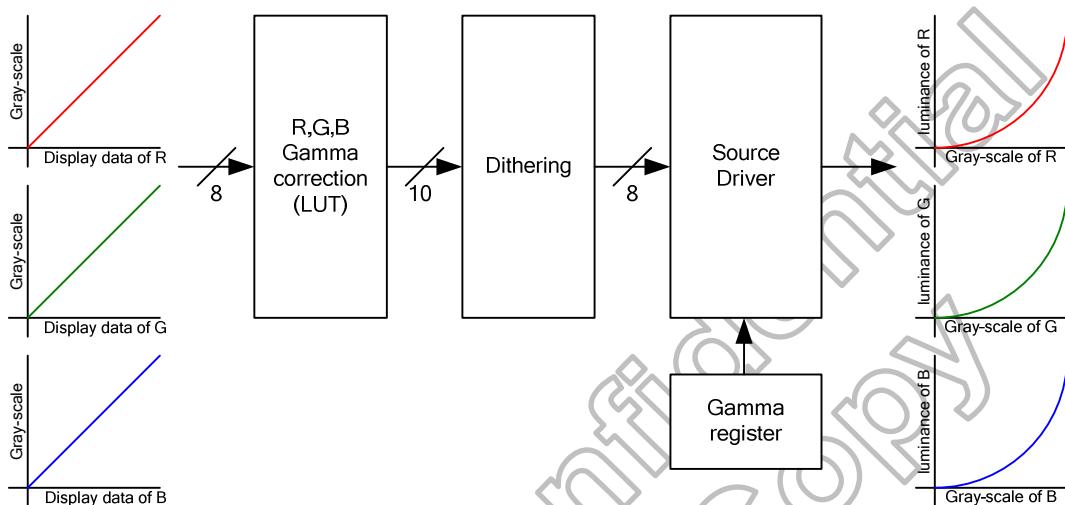


Figure 5.19: Block diagram of digital gamma correction

The HX8379-A builds one 126-bytes DGC_LUT (Digital Gamma Correction Look Up Table) to transfer every display data of Dithering circuit input and setting by DGC_LUT register in CMD RC1h.

By setting the independent R/G/B 33 sets of DGC_LUT[9:0], the corresponding source data can be extended to 1023 levels.

DGC_LUT[9:0] (10-bit)				Default Output GrayScale Voltage (8-bit)
DGC_LUT[9:2] (8-bit)	Default Value	DGC_LUT[1:0] (2-bit)	Default Value	
R00 / G00 / B00 [9:2]	00h	R00 / G00 / B00 [1:0]	0h	data_000
R01 / G01 / B01 [9:2]	08h	R01 / G01 / B01 [1:0]	0h	data_008
R02 / G02 / B02 [9:2]	10h	R02 / G02 / B02 [1:0]	0h	data_016
R03 / G03 / B03 [9:2]	18h	R03 / G03 / B03 [1:0]	0h	data_024
R04 / G04 / B04 [9:2]	20h	R04 / G04 / B04 [1:0]	0h	data_032
R05 / G05 / B05 [9:2]	28h	R05 / G05 / B05 [1:0]	0h	data_040
R06 / G06 / B06 [9:2]	30h	R06 / G06 / B06 [1:0]	0h	data_048
R07 / G07 / B07 [9:2]	38h	R07 / G07 / B07 [1:0]	0h	data_056
R08 / G08 / B08 [9:2]	40h	R08 / G08 / B08 [1:0]	0h	data_064
R09 / G09 / B09 [9:2]	48h	R09 / G09 / B09 [1:0]	0h	data_072
R10 / G10 / B10 [9:2]	50h	R10 / G10 / B10 [1:0]	0h	data_080
R11 / G11 / B11 [9:2]	58h	R11 / G11 / B11 [1:0]	0h	data_088
R12 / G12 / B12 [9:2]	60h	R12 / G12 / B12 [1:0]	0h	data_096
R13 / G13 / B13 [9:2]	68h	R13 / G13 / B13 [1:0]	0h	data_104
R14 / G14 / B14 [9:2]	70h	R14 / G14 / B14 [1:0]	0h	data_112
R15 / G15 / B15 [9:2]	78h	R15 / G15 / B15 [1:0]	0h	data_120
R16 / G16 / B16 [9:2]	80h	R16 / G16 / B16 [1:0]	0h	data_128
R17 / G17 / B17 [9:2]	88h	R17 / G17 / B17 [1:0]	0h	data_136
R18 / G18 / B18 [9:2]	90h	R18 / G18 / B18 [1:0]	0h	data_144
R19 / G19 / B19 [9:2]	98h	R19 / G19 / B19 [1:0]	0h	data_152
R20 / G20 / B20 [9:2]	A0h	R20 / G20 / B20 [1:0]	0h	data_160
R21 / G21 / B21 [9:2]	A8h	R21 / G21 / B21 [1:0]	0h	data_168
R22 / G22 / B22 [9:2]	B0h	R22 / G22 / B22 [1:0]	0h	data_176
R23 / G23 / B23 [9:2]	B8h	R23 / G23 / B23 [1:0]	0h	data_184
R24 / G24 / B24 [9:2]	C0h	R24 / G24 / B24 [1:0]	0h	data_192
R25 / G25 / B25 [9:2]	C8h	R25 / G25 / B25 [1:0]	0h	data_200
R26 / G26 / B26 [9:2]	D0h	R26 / G26 / B26 [1:0]	0h	data_208
R27 / G27 / B27 [9:2]	D8h	R27 / G27 / B27 [1:0]	0h	data_216
R28 / G28 / B28 [9:2]	E0h	R28 / G28 / B28 [1:0]	0h	data_224
R29 / G29 / B29 [9:2]	E8h	R29 / G29 / B29 [1:0]	0h	data_232
R30 / G30 / B30 [9:2]	F0h	R30 / G30 / B30 [1:0]	0h	data_240
R31 / G31 / B31 [9:2]	F8h	R31 / G31 / B31 [1:0]	0h	data_248
R32 / G32 / B32 [9:2]	FFh	R32 / G32 / B32 [1:0]	0h	data_255

Table 5.42: DGC-LUT

5.8 Characteristics of I/O

5.8.1 Output or bi-directional (I/O) pins

Output or bi-directional pins	After power on	After hardware reset	After software reset
TE_L/TE_R	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
SDO	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)
CABC_PWM_OUT	Low	Low	Low
CABC_LED_ON	Low	Low	Low
IDLE_ON	Low	Low	Low
LED1 / LED2	High-Z (Inactive)	High-Z (Inactive)	High-Z (Inactive)

Table 5.43: Characteristics of output or bi-directional (I/O) pins

5.8.2 Input pins

Input pins	During power on process	After power on	After hardware reset	After software reset	During power off process
RESX	Setion.5.18	Input valid	Input valid	Input valid	Setion.5.18
CSX	Input Invalid	Input valid	Input valid	Input valid	Input Invalid
DCX	Input Invalid	Input valid	Input valid	Input valid	Input Invalid
SCL_I2C_SCL	Input Invalid	Input valid	Input valid	Input valid	Input Invalid
DB[23:0]	Input Invalid	Input valid	Input valid	Input valid	Input Invalid
SDI_I2C_SDA	Input Invalid	Input valid	Input valid	Input valid	Input Invalid
HS	Input Invalid	Input valid	Input valid	Input valid	Input Invalid
VS	Input Invalid	Input valid	Input valid	Input valid	Input Invalid
PCLK	Input Invalid	Input valid	Input valid	Input valid	Input Invalid
DE	Input Invalid	Input valid	Input valid	Input valid	Input Invalid
OSC	Input Invalid	Input valid	Input valid	Input valid	Input Invalid
IM[3:0]	Input Invalid	Input valid	Input valid	Input valid	Input Invalid
TEST[3:0]	Low	Low	Low	Low	Low

Table 5.44: Characteristics of input pins

5.9 GIP control signal

HX8379-A is a single chip solution for a WVGA GIP (Gate In Panel) type TFT LCD display. There are many GIP/ASG type TFT panels that correspond to different GIP timing. Therefore, the GIP setting must be setup to the correct GIP/ASG timing for the normal display. The GIP timing adjustment is related to internal register.

The GIP control signals (CGOUT0_L/R ~ CGOUT15_L/R) are for panel used. The assignment of each panel type is specified on the application note. Regarding the GIP/ASG timing, please refer to HX8379-A application note.

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5.10 Sleep Out –command and self-diagnostic functions of the display module

5.10.1 Register loading detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP (or similar device) to registers of the display controller is working properly. There are compared factory values of the OTP and register values of the display controller by the display controller. If those both values (OTP and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (=increased by 1).

The flow chart for this internal function is following:

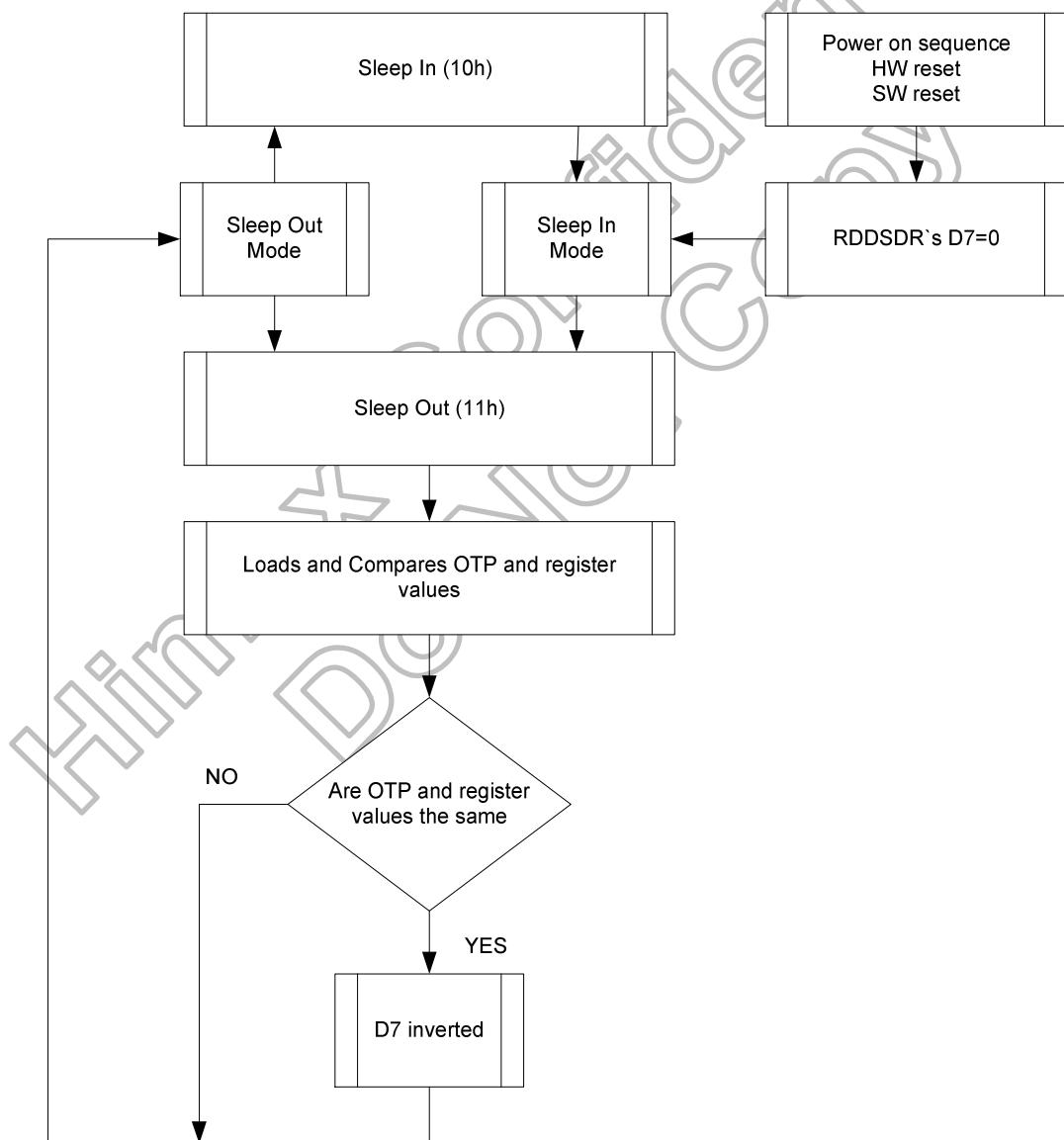
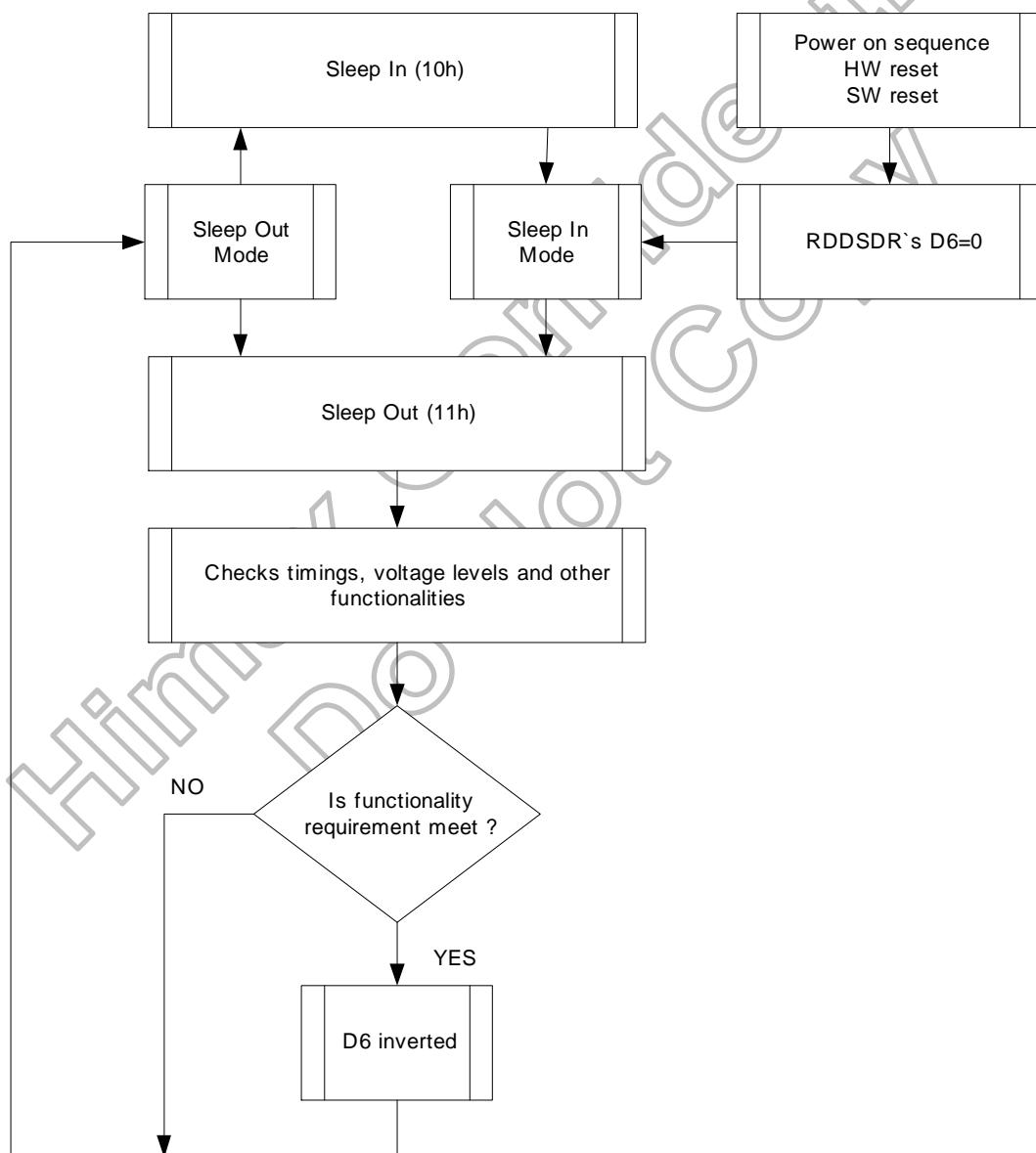


Figure 5.20: Sleep out flow chart–command and self-diagnostic functions

5.10.2 Functionality detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements.

The internal function (=the display controller) is comparing, if the display module still meets functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, 1 bit will be inverted (=increased by 1), which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D6). If functionality requirement is not the same, this bit (D6) is not inverted (=increased by 1). The flow chart for this internal function is shown as below.



Note: There is needed 120msec after Sleep Out -command, when there is changing from Sleep In-mode to Sleep Out -mode, before there is possible to check if Customer's functionality requirements are met and a value of RDDSDR's D6 is valid. Otherwise, there is 5msec delay for D6's value, when Sleep Out –command is sent in Sleep Out -mode.

Figure 5.21: Sleep out flow chart internal function detection

5.11 Power on/off sequence

VDD1, VDD2 and VDD3 can be applied in any order. VDD1, VDD2 and VDD3 can be powered down in any order. During power off, if LCD is in the Sleep Out mode, VDD1 and VDD2 must be powered down minimum 120msec after RESX has been released. During power off, if LCD is in the Sleep In mode, VDD1, VDD2 and VDD3 can be powered down minimum 0msec after RESX has been released. CSX can be applied at any timing or can be permanently grounded. RESX has priority over CSX. There will be no damage to the display module if the power sequences are not met. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence. If RESX line is not held stable by host during Power On Sequence as defined in Sections 5.11.1 and 5.11.2, then it will be necessary to apply a Hardware Reset (RESX) after Host Power On Sequence is complete to ensure correct operation. Otherwise function is not guaranteed. The power on/off sequence is illustrated below.

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5.11.1 Case 1: RESX line is held high or unstable by host at power on

If RESX line is held high or unstable by the host during power on, then a Hardware Reset must be applied after both VDD1, VDD2 and VDD3 have been applied-otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.

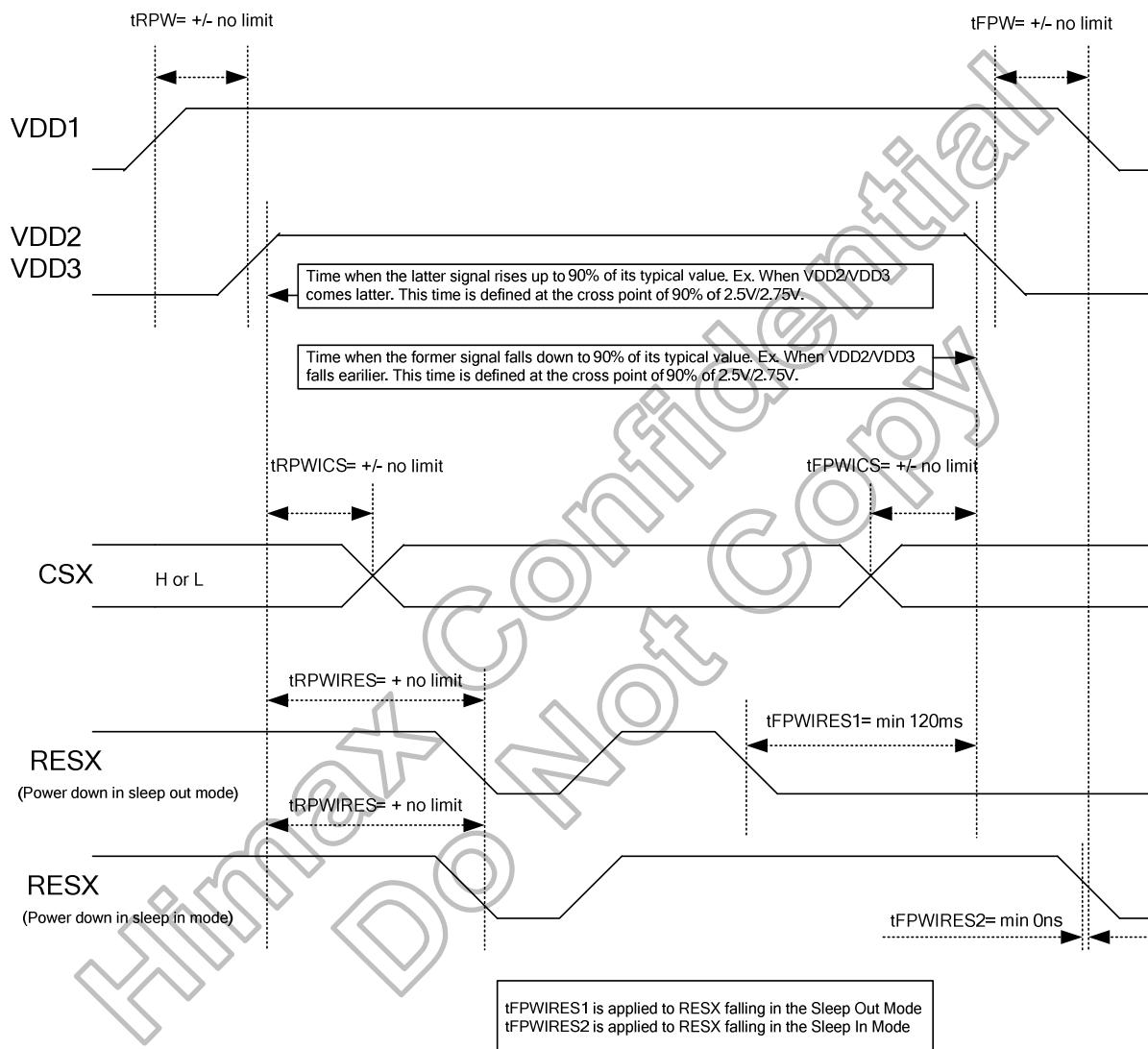


Figure 5.22: Case 1: RESX line is held high or unstable by host at power on

5.11.2 Case 2: RESX line is held low by host at power on

If RESX line is held low (and stable) by the host during power on, then the RESX must be held low for minimum 10 μ sec after both VDD1, VDD2 and VDD3 have been applied.

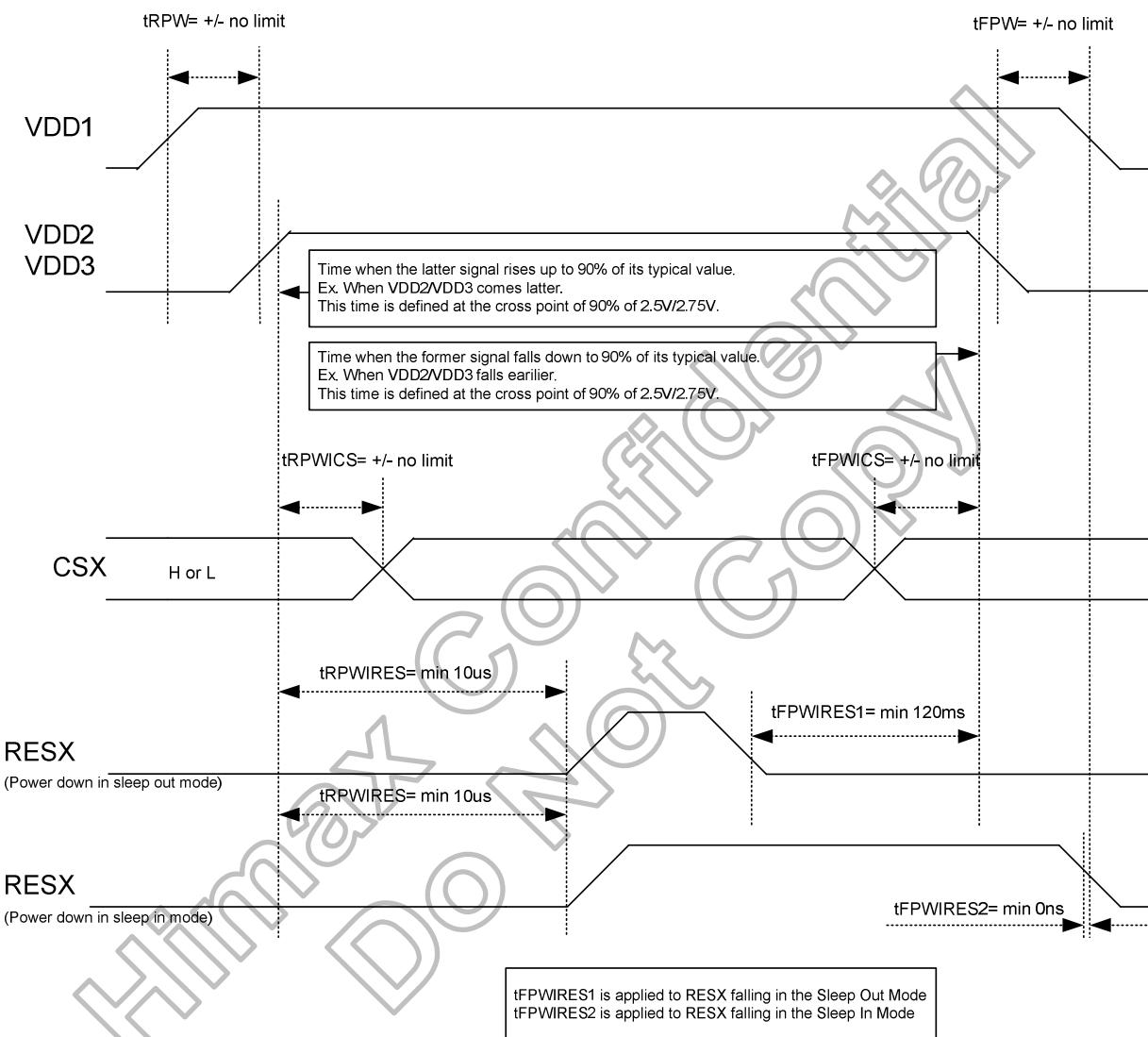


Figure 5.23: Case 2: RESX line is held low by host at power on

5.12 Uncontrolled power off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until "Power On Sequence" powers it up.

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5.13 Content adaptive brightness control (CABC) function

The general block diagram of the CABC and the brightness control is illustrated below:

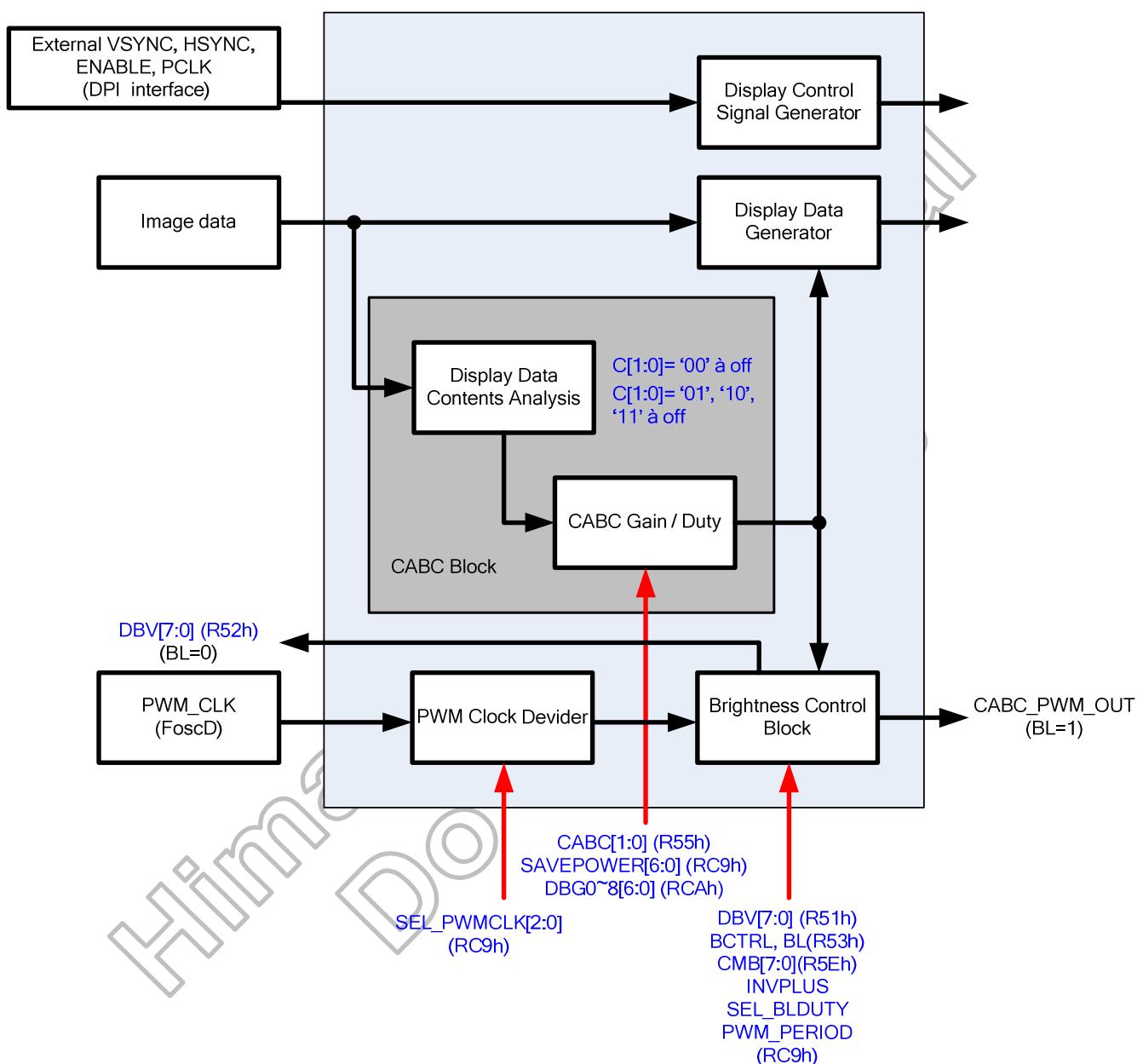
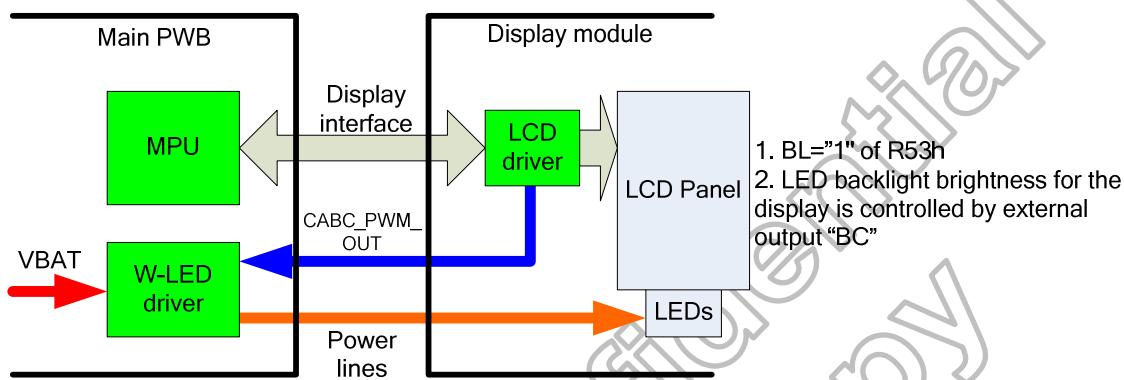


Figure 5.24: CABC block diagram

5.13.1 Module architectures

The HX8379-A can support two module architectures for CABC operation. The BL bit setting of R53h can be used to select used display module architecture. White LED driver circuit for display backlight is located on the main PWB, not in the display module both in architecture I and II.

- **Architecture I**



- **Architecture II**

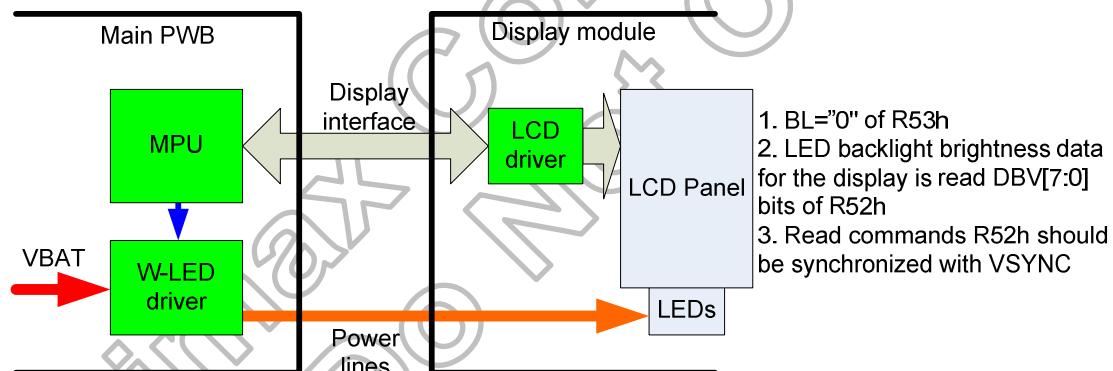


Figure 5.25: Module architecture

5.13.2 CABC block

There are DBG0~8[6:0] register bits in CABC block to define the “CABC gain”/ “CABC duty” table. Every DBGx[6:0] has 33 gain/duty value setting.

After one-frame display data content analysis, LSI will generate one CABC gain / CABC duty value calculated from DBG0~8[6:0] register bits setting (by using interpolated method) for display data generating and for backlight PWM pulse generating.

Please note that the CABC gain / CABC duty value calculated by the LSI is one of the 33 gain/duty value setting in DBGxx[6:0].

Please note that : Duty (valid level period (LED on) / one complete period)=1/ gain.

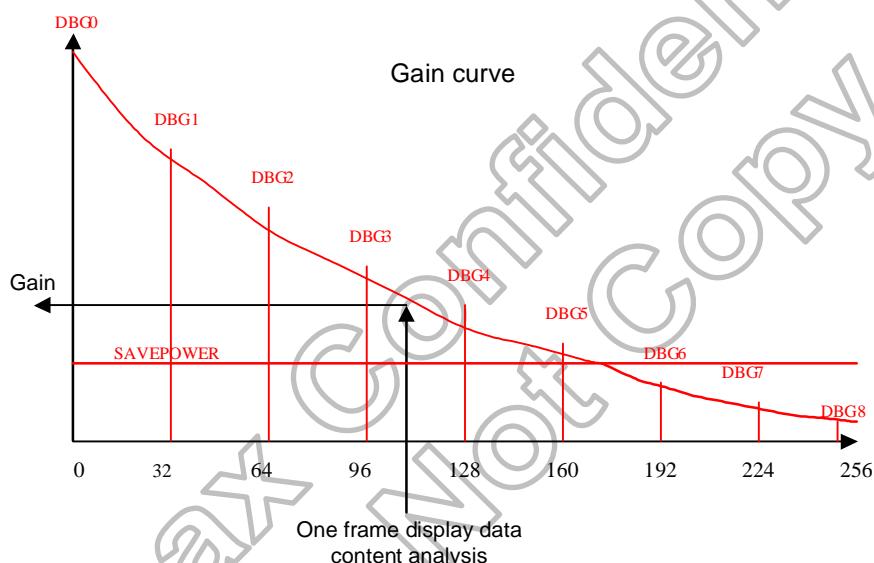


Figure 5.26: CABC gain / CABC duty generation

For power saving of backlight module, there are SAVEPOWER[6:0] bits to define the “minimum gain”/ “maximum duty” of CABC block output. If the CABC gain / duty after one-frame display data contents analysis is smaller(gain) / larger(duty) than SAVEPOWER[6:0] bits setting, the CABC block will output CABC gain / duty equal to SAVEPOWER[6:0] and ignore the result of display data contents analysis.

5.13.3 Brightness control block

There is an external output signal from brightness block, CABC_PWM_OUT, to control the LED driver IC in order to control display brightness.

There are register bits, DBV[7:0] of R51h, for display brightness of manual brightness setting. The CABC_PWM_OUT duty is calculated as $(DBV[7:0]) / 255 \times CABC\ duty$ (generated after one-frame display data content analysis).

For ex: CABC_PWM_OUT period = 2.95 ms, and DBV[7:0](R51h) = '228_{DEC}' and CABC duty is 74%. Then CABC_PWM_OUT duty = $(228) / 255 \times 74.42\% \equiv 66.54\%$. Correspond to the CABC_PWM_OUT period = 2.95 ms, the high-level of CABC_PWM_OUT (high effective) = 1.96ms, and the low-level of CABC_PWM_OUT = 0.99ms.

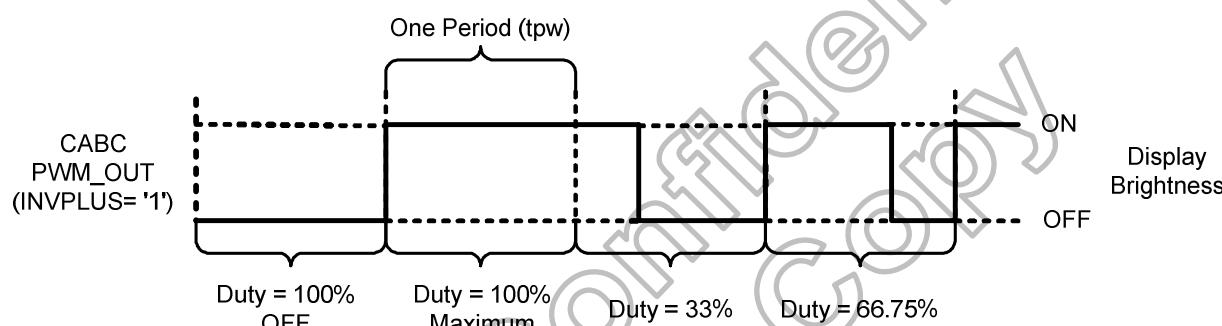


Figure 5.27: CABC_PWM_OUT output duty

Symbol	Parameter	Min.	Max.	Unit	Description
tpw	Pulse width	0.0333	8.33	ms	-

Table 5.45: CABC timing table

Note: (1) The signal rise and fall times (t_f, t_r) are stipulated to be equal to or less than 15ns.

(2) The pulse width range by setting CABC related registers is located between 0.0333ms to 8.33ms.

When Architecture II module is used ($BL='0'$) with the example below, the CABC_PWM_OUT is always output low and the DBV[7:0](R51h) will be read a value as 169_{DEC} ($(169) / 255 \equiv 66.27\%$).

5.13.4 Minimum brightness setting of CABC function

CABC function is automatically reduced backlight brightness based on image contents. In the case of the combination with the CABC or manual brightness setting, display brightness is too dark. It must affect to image quality degradation. CABC minimum brightness setting (CMB[7:0] bits of R5Eh) is to avoid too much brightness reduction.

When CABC is active, CABC can not reduce the display brightness to less than CABC minimum brightness setting. Image processing function is worked as normal, even if the brightness can not be changed.

This function does not affect to the other function, manual brightness setting. Manual brightness can be set the display brightness to less than CABC minimum brightness. Smooth transition and dimming function can be worked as normal.

When display brightness is turned off (BCTRL='0' of R53h), CABC minimum brightness setting is ignored. "CMB[7:0], Read CABC minimum brightness (R5Fh)" always read the setting value of "CMB[7:0], Write CABC minimum brightness (R5Eh)"

5.14 OTP programing

5.14.1 OTP table

OTP INDEX (HEX)	CMD/PA	B7	B6	B5	B4	B3	B2	B1	B0
009	B0_01	NVALID				AUTO_OPT[6:0]			
00F	NVALID	NVALID							
010	C4_01				DDB1[7:0]				
011	C4_02				DDB2[7:0]				
012	C4_03				DDB3[7:0]				
013	C4_04				DDB4[7:0]				
01C	NVALID	NVALID	-	-	-	-	-	-	-
01D	B4_01	ZZ_LR	ZZ_EO		NW_PE[2:0]			NW[2:0]	
01E	B4_02				USER_GIP_GATE[7:0]				
01F	B4_03	GIP_FR[1:0]	BLK_OSCSEL	-	STV_as_CK	-	-	GIP_FR_MODE	
020	B4_04		SHR0_3[3:0]			SHR0_2[3:0]			
021	B4_05		SHR0_1[3:0]			SHR0[11:8]			
022	B4_06				SHR0[7:0]				
023	B4_07		SHR1_3[3:0]			SHR1_2[3:0]			
024	B4_08		SHR1_1[3:0]			SHR1[11:8]			
025	B4_09				SHR1[7:0]				
026	B4_0A		SHR2_3[3:0]			SHR2_2[3:0]			
027	B4_0B		SHR2_1[3:0]			SHR2[11:8]			
028	B4_0C				SHR2[7:0]				
029	B4_0D		SHP[3:0]			SCP[3:0]			
02A	B4_0E				SPON[7:0]				
02B	B4_0F				SPOFF[7:0]				
02C	B4_10				CHR[7:0]				
02D	B4_11		CHP[3:0]			CCP[3:0]			
02E	B4_12				CON[7:0]				
02F	B4_13				COFF[7:0]				
030	B4_14				SON[7:0]				
031	B4_15				SOFF[7:0]				
032	B4_16				EQON2[7:0]				
033	B4_17				EQON1[7:0]				
034	B4_18				SPON_MPU[7:0]				
035	B4_19				SPOFF_MPU[7:0]				
036	B4_1A				CON_MPU[7:0]				
037	B4_1B				COFF_MPU[7:0]				
038	B4_1C				SON_MPU[7:0]				
039	B4_1D				SOFF_MPU[7:0]				
03A	B4_1E				EQON2_MPU[7:0]				
03B	B4_1F				EQON1_MPU[7:0]				
072	B3_01	NVALID	-	DPICC[1:0]	DPL	HSPL	VSPL	EPL	
075	CB_01	NVALID	-	-	-		UADJ[3:0]		
076	CB_02	-	-	-	-		UADJ_PE[3:0]		
077	B5_01	NVALID		RGB_VP[10:8]					Porch_Mode
078	B5_02				RGB_VP[7:0]				
079	B5_03				RGB_HP[7:0]				
07A	CC_01	NVALID	-	-	-	SS_PANE_L	GS_PANE_L	REV_PANE_L	BGR_PANEL
07B	NVALID	NVALID (SET1)	NVALID (SET2)	NVALID (SET3)	-	-	-	-	-
07C	C3_01				ID1[7:0] (SET1)				
07D	C3_02				ID2[7:0] (SET1)				
07E	C3_03				ID3[7:0] (SET1)				
07F	C3_04				ID4[7:0] (SET1)				
080	C3_01				ID1[7:0] (SET2)				
081	C3_02				ID2[7:0] (SET2)				
082	C3_03				ID3[7:0] (SET2)				

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083	C3_04	ID4[7:0] (SET2)													
084	C3_01	ID1[7:0] (SET3)													
085	C3_02	ID2[7:0] (SET3)													
086	C3_03	ID3[7:0] (SET3)													
087	C3_04	ID4[7:0] (SET3)													
088	B1_02	NVALID	DCLK_Reserved[2:0]			-	-	VGL_REG_EN							
089	B1_03	FS2[3:0]			VRGH_EN	AP[2:0]									
08A	B1_04	VGHS[7:0]													
08B	B1_05	VGLS[7:0]													
08C	B1_06	-	-	VGL_REGS[5:0]											
08D	B1_07	-	-	VRGH[5:0]											
08E	B1_08				BTP[4:0]										
08F	B1_09	VCL[2:0]			BTN[4:0]										
090	B1_0A	VRHP[7:0]													
091	B1_0B	VRHN[7:0]													
092	B1_0C	APF_EN	DD_TU	VRMP[5:0]											
093	B1_0D	-	-	VRMN[5:0]											
094	B1_0E	FS1[3:0]			PCCS[2:0]										
095	B1_0F	DT[1:0]		-	FS0[4:0]										
096	B1_10	-	XDK[2:0]		XDKN[2:0]		AUTO_XDK								
097	B1_11	CLK_OPT2	CLK_OPT1	DC_VPNL[1:0]	DCDIV[3:0]										
098	B1_12	DCS[1:0]		DTPS[2:0]			DTNS[2:0]								
099	B1_13	A_DC[1:0]		A_DTP[2:0]			A_DTN[2:0]								
09A	B1_14	B_DC[1:0]		B_DTP[2:0]			B_DTN[2:0]								
09B	B1_15	C_DC[1:0]		C_DTP[2:0]			C_DTN[2:0]								
09C	B1_16	D_DC[1:0]		D_DTP[2:0]			D_DTN[2:0]								
09D	B1_17	E_DC[1:0]		E_DTP[2:0]			E_DTN[2:0]								
09E	B1_18	Reserved													
09F	B1_19	FS0_LP[2:0]			BTP0[4:0]										
0A0	B1_1A	-	FS1_LP[1:0]	BTP1[4:0]											
0A1	B1_1B	-	DC_DIV_LP[1:0]	BTP2[4:0]											
0A2	B1_1C	-	DTP_LP[1:0]	BTP3[4:0]											
0A3	B1_1D	-	DTN_LP[1:0]	BTP4[4:0]											
0A4	B1_1E	-	FS2_LP[1:0]	BTP5[4:0]											
0A6	NVALID	NVALID	-	-	-	-	-	-							
0A7	B2_03	NL[7:0]													
0A8	B2_04	BP [7:0]													
0A9	B2_05	FP [7:0]													
0AA	B2_06	RTN[7:0]													
0AB	B2_07	SAP[3:0]			ABC_CLK_DIV[1:0]		vs_plus_bp_en	ABC_HS_BY_PASS							
0AC	B2_08	GEN_ON[7:0]													
0AD	B2_09	GEN_OFF[7:0]													
0AE	B2_0A	BP_PE [7:0]													
0AF	B2_0B	FP_PE [7:0]													
0B0	B2_0C	RTN_PE[7:0]													
0B1	B2_0D	SAP_PE[3:0]			-	-	-	-							
0CC	NVALID	NVALID (SET1)	NVALID (SET2)	NVALID (SET3)	-	-	-	-							
0CD	B6_01	-	-	-	-	-	VCMC_F8 (SET1)	VCMC_F8 (SET2)							
0CE	B6_03	-	-	-	-	-	VCMC_B8 (SET1)	VCMC_B8 (SET2)							
0CF	B6_02	VCMC_F[7:0] (SET1)													
0D0	B6_04	VCMC_B[7:0] (SET1)													
0D1	B6_02	VCMC_F[7:0] (SET2)													
0D2	B6_04	VCMC_B[7:0] (SET2)													
0D3	B6_02	VCMC_F[7:0] (SET3)													
0D4	B6_04	VCMC_B[7:0] (SET3)													
0D5	B7_01	NVALID	-	TE_SEL[1:0]	TEI[3:0]										
0D6	B7_02	TEL_SEL[1:0]		TER_SEL[1:0]	-	TEP[10:8]									
0D7	B7_03	TEP[7:0]													
0D8	E0_01	NVALID	-	G1_VRP0[5:0]											
0D9	E0_02	-	-	G1_VRP1[5:0]											

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0DA	E0_03	-	-		G1_VRP2[5:0]				
0DB	E0_04	-	-		G1_VRP3[5:0]				
0DC	E0_05	-	-		G1_VRP4[5:0]				
0DD	E0_06	-	-		G1_VRP5[5:0]				
0DE	E0_07	-			G1_PRP0[6:0]				
0DF	E0_08	-			G1_PRP1[6:0]				
0E0	E0_09	-	-	-	G1_PKP0[4:0]				
0E1	E0_0A	-	-	-	G1_PKP1[4:0]				
0E2	E0_0B	-	-	-	G1_PKP2[4:0]				
0E3	E0_0C	-	-	-	G1_PKP3[4:0]				
0E4	E0_0D	-	-	-	G1_PKP4[4:0]				
0E5	E0_0E	-	-	-	G1_PKP5[4:0]				
0E6	E0_0F	-	-	-	G1_PKP6[4:0]				
0E7	E0_10	-	-	-	G1_PKP7[4:0]				
0E8	E0_11	-	-	-	G1_PKP8[4:0]				
0E9	E0_12	-	-		G1_VRN0[5:0]				
0EA	E0_13	-	-		G1_VRN1[5:0]				
0EB	E0_14	-	-		G1_VRN2[5:0]				
0EC	E0_15	-	-		G1_VRN3[5:0]				
0ED	E0_16	-	-		G1_VRN4[5:0]				
0EE	E0_17	-	-		G1_VRN5[5:0]				
0EF	E0_18	-			G1_PRN0[6:0]				
0F0	E0_19	-			G1_PRN1[6:0]				
0F1	E0_1A	-	-	-	G1_PKN0[4:0]				
0F2	E0_1B	-	-	-	G1_PKN1[4:0]				
0F3	E0_1C	-	-	-	G1_PKN2[4:0]				
0F4	E0_1D	-	-	-	G1_PKN3[4:0]				
0F5	E0_1E	-	-	-	G1_PKN4[4:0]				
0F6	E0_1F	-	-	-	G1_PKN5[4:0]				
0F7	E0_20	-	-	-	G1_PKN6[4:0]				
0F8	E0_21	-	-	-	G1_PKN7[4:0]				
0F9	E0_22	-	-	-	G1_PKN8[4:0]				
0FA	C9_01	NVALID		SEL_PWMCLK[2:0]	SEL_GAIN[1:0]	INVPULS	SEL_BLDUTY		
0FB	C9_02			PWM_PERIOD[7:0]					
0FC	C9_03	CABC_FSYNC		DIM_FRAME[6:0]					
0FD	C9_04			CABC_STEP[7:0]					
0FE	C9_05			CABC_CLKEN[7:0]					
0FF	C9_06	-		SAVEPOWER[6:0]					
150	NVALID	NVALID	-	-	-	-	-	-	-
151	B8_01		GPO1SEL[3:0]		GPO0SEL[3:0]				
152	B8_02		GPO3SEL[3:0]		GPO2SEL[3:0]				
153	E4_02	NVALID	-	-	-	-	-	-	DYN_CEHEN
180	C1_01	NVALID	-	-	-	-	-	DITH_OPT	DGC_EN
181	C1_02			D1[7:0]					
...	C1_0n			Dn[7:0]					
1FE	C1_7F			D126[7:0]					

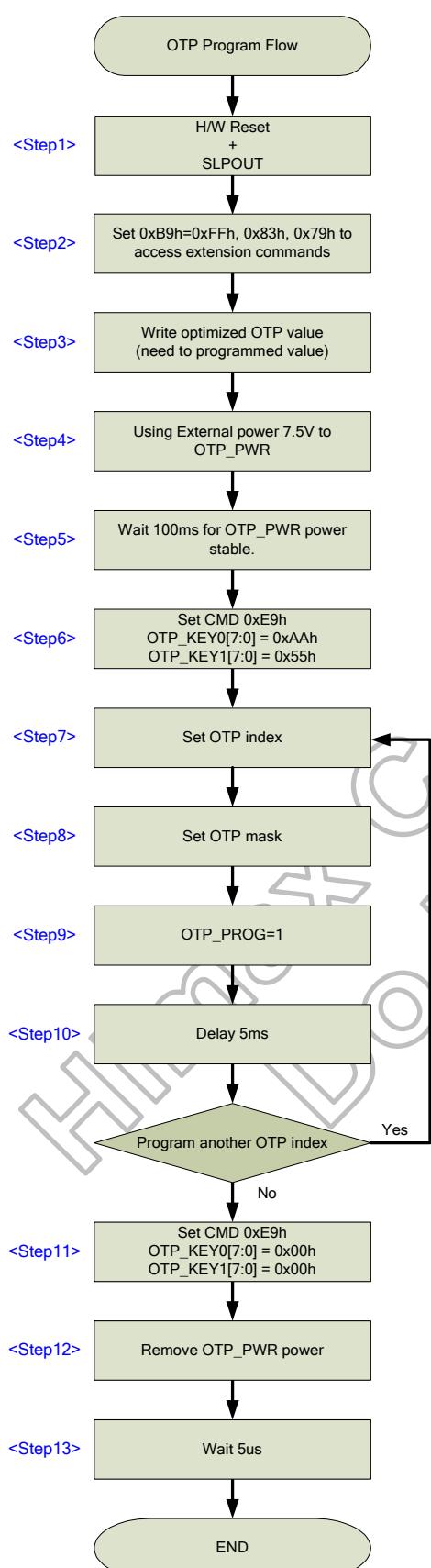
Note: (1) The default value of OTP memory bits are all "1".

(2) NVALID bit decide the OTP reload Enable/Disable, the default value is "1". If the own OTP area of NVALID bit had been programmed, the NVALID bit will be changed to "0" automatically and execute the OTP reload.

(3) There are some conditions that HX8379-A can reload OTP.

- a. Hardware reset.
- b. Software reset.
- c. SLPOUT command.

5.14.2 OTP programming flow



OTP_KEY0[7:0] OTP_KEY1[7:0]	Description	Note
OTP_KEY0[7:0] = 0xAAh OTP_KEY1[7:0] = 0x55h	Enter OTP program mode	
OTP_KEY0[7:0] = 0x00h OTP_KEY1[7:0] = 0x00h	Leave OTP program mode	
Other value	Invalid	1. If HX8379-A operate on OTP program mode, then keep on OTP program mode. 2. If HX8379-A operate on non-OTP program mode, then keep on non-OTP program mode.

Figure 5.28: OTP programming sequence

5.14.3 Programming sequence

Step	Operation
1	Power on and reset the module.
2	SLPOUT and set 0xB9h = 0xFFh, 0x83h, 0x79h to access the extension commands.
3	Write optimized values to related registers.
4	Set VGH power to 7.5V for OTP programming state for using internal power mode. Or using the external power 7.5V to OTP_PWR.
5	Wait 100ms for OTP_PWR power stable.
6	Set CMD RE9h: OTP_KEY0[7:0]=0xAAh and OTP_KEY1[7:0]=0x55h to enter OTP program mode.
7	Specify OTP_index, please refer to the OTP table.
8	Set OTP_Mask=0x00h, programming the entire bit of one parameter.
9	Set OTP_PROG=1, Internal register begin write to OTP according to OTP_index.
10	Wait 5 ms ⁽¹⁾
11	Complete programming one parameter to OTP. If continue to programming other parameter, return to step (7). Otherwise, Set CMD RE9h: OTP_KEY0[7:0]=0xAAh and OTP_KEY1[7:0]=0x55h to leave OTP program mode.
12	Remove the external power on OTP_PWR pin.
13	Wait 5us

- Note:** (1) During the OTP programming process, it must be added 5ms delay time after setting OTP_PROG=1.
 (2) During the OTP program on VCMC setting: VCMC(SET1), VCMC(SET2), VCMC(SET3), user just need to specify the OTP index CCh. All settings of SETVCOM will be programmed to VCMC(SET1), VCMC(SET2), VCMC(SET3) automatically.
 (3) During the OTP program on ID1~4 setting: ID1~4(SET1): 7Ch~7Fh, ID1~4(SET2): 80h~83h, and ID1~4(SET3): 84h~87h, user just need to specify the OTP index 7Bh. All settings of ID1~4 will be programmed to ID1~4(SET1), ID1~4(SET2) and ID1~4(SET3) automatically.
 (4) GAMMA OTP can program in group, and user just need to specify the first OTP_INDEX in the group. Then all settings of specify group will be programmed automatically. During the GAMMA OTP program, it must delay 100ms.

Reference Command	OTP Index for Program	OTP Group
SETGAMMA, RE0h	D8h	D8h~F9h

Table 5.46: OTP Programming sequence

5.14.4 OTP programming example of VCOM setting VCMC

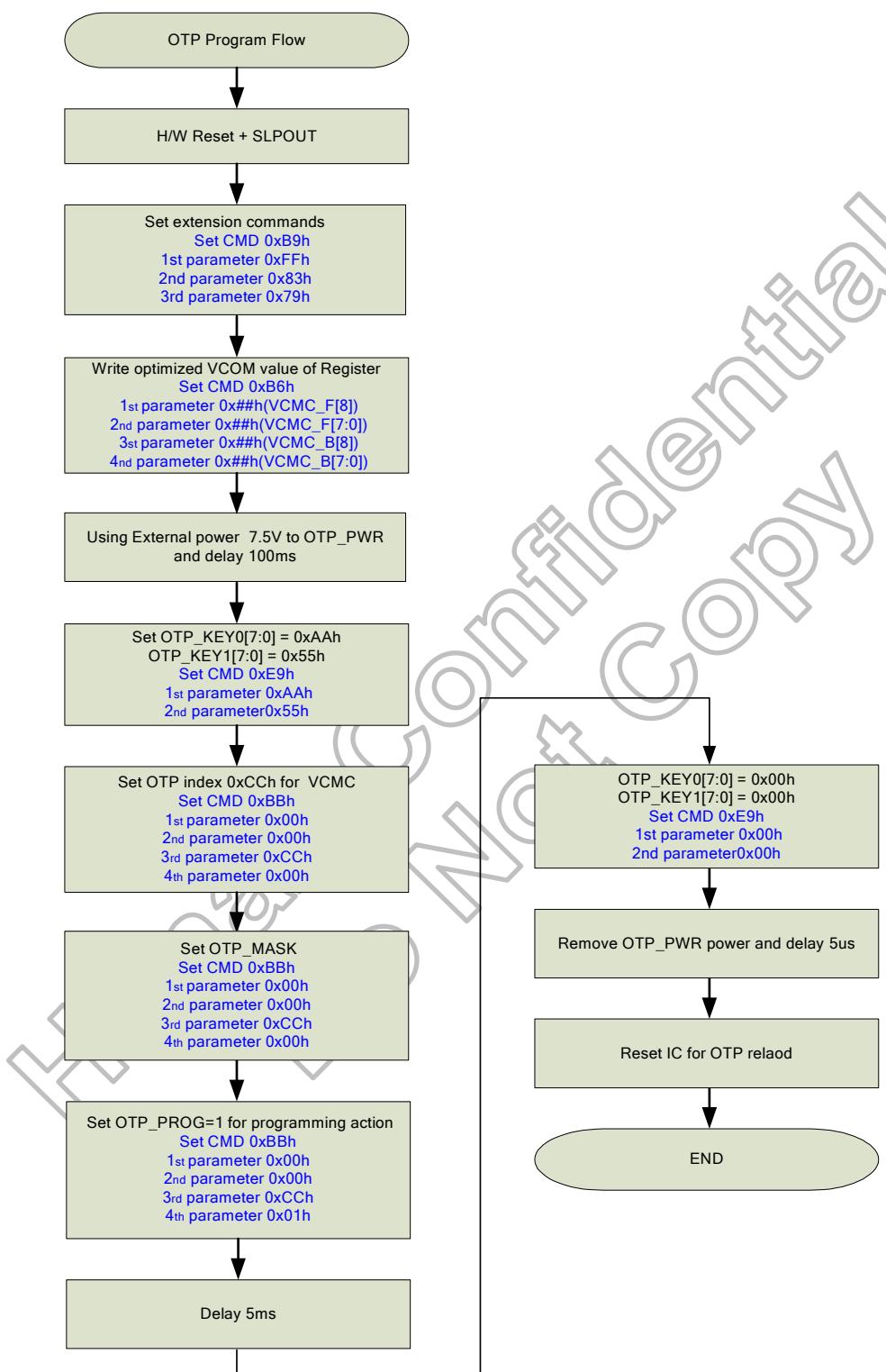


Figure 5.29: OTP programming sequence example 1

5.14.5 OTP programming example of ID1, ID2, ID3 and ID4

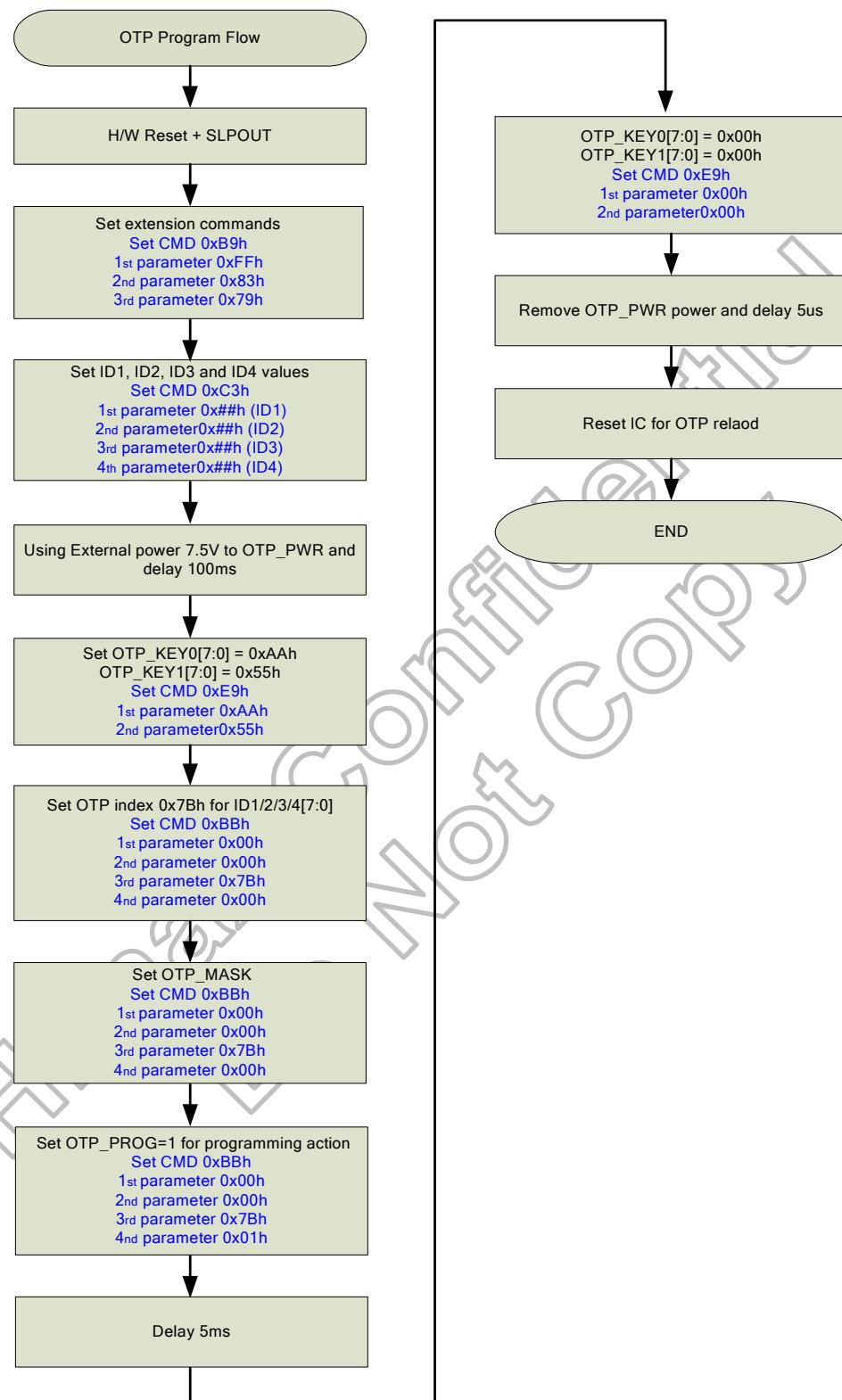


Figure 5.30: OTP programming sequence example 2

5.14.6 OTP read example of 0xCDh (VCMC)

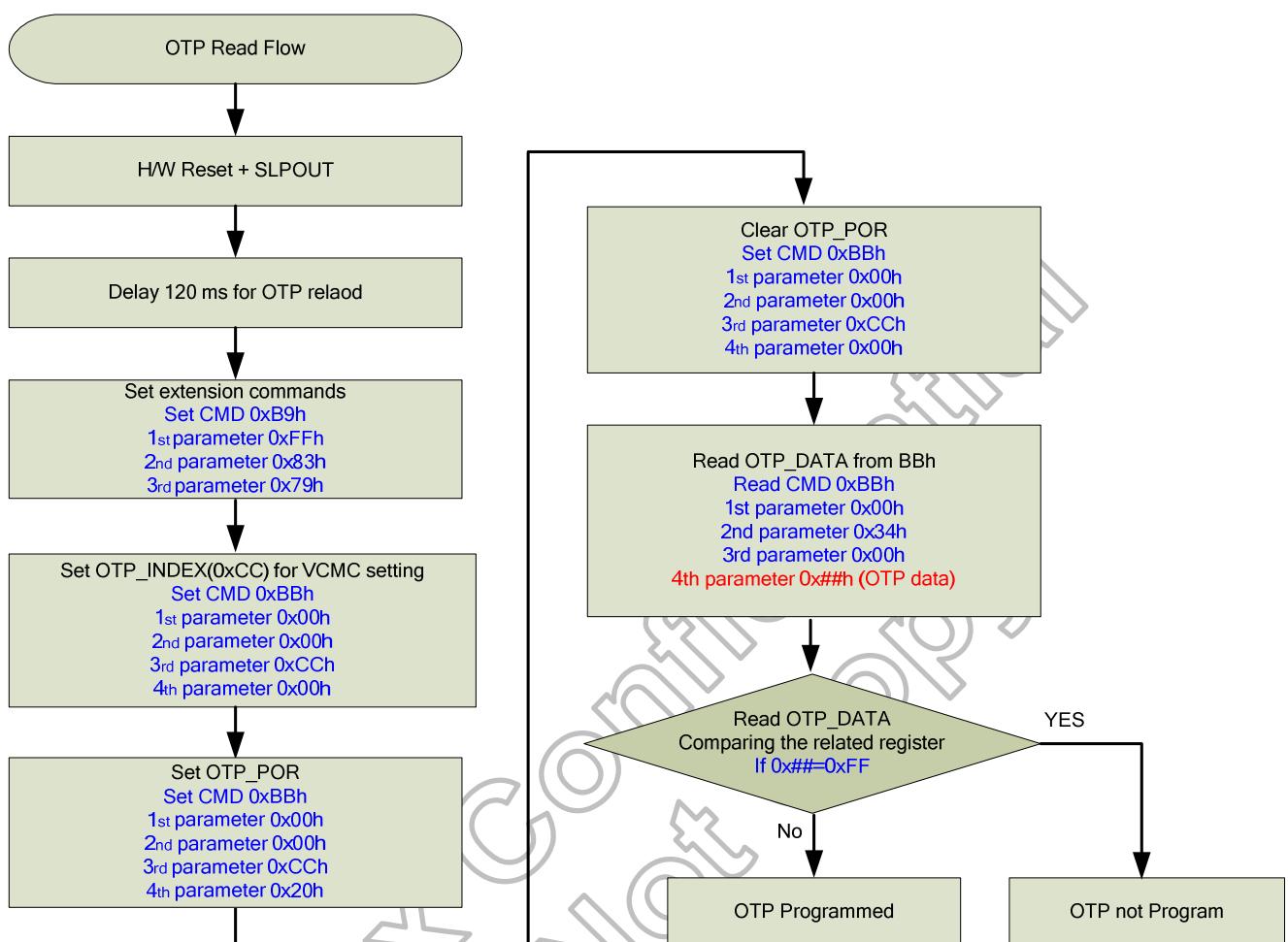


Figure 5.31: OTP read sequence flow of index 0xCCCh

6. Command

6.1 Command list

6.1.1 Standard command

(Hex)	Operation code	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)
00	NOP	0	0	0	0	0	0	0	0	0	No Operation	-
01	SWRESET	0	0	0	0	0	0	0	0	1	Software Reset	-
04	RDDIDIF	0	0	0	0	0	0	1	0	0	Read Display Identification Information	-
		1					ID1[7:0]					-
		1					ID2[7:0]					-
		1					ID3[7:0]					-
05	RDNUMPE	0	0	0	0	0	0	1	0	1	Read Number of DSI Parity Error	-
		1	x	x	x	x	x	x	x	x	Dummy read	-
		1				P[7:0]						-
06	RDRED	0	0	0	0	0	0	1	1	0	Read Red Colour	-
		1	x	x	x	x	x	x	x	x	Dummy read	-
		1	R7	R6	R5	R4	R3	R2	R1	R0		-
07	RDGREEN	0	0	0	0	0	0	1	1	1	Read Green Colour	-
		1	x	x	x	x	x	x	x	x	Dummy read	-
		1	G7	G6	G5	G4	G3	G2	G1	G0		-
08	RDBLUE	0	0	0	0	0	1	0	0	0	Read Blue Colour	-
		1	B7	B6	B5	B4	B3	B2	B1	B0		-
		0	0	0	0	0	1	0	0	1	Read display status	-
09	RDDST	0	0	0	0	0	1	0	0	0	D[31:24]	-
		1					D[23:16]					-
		1					D[15:8]					-
		1					D[7:0]					-
0A	RDDPM	0	0	0	0	0	1	0	1	0	Read display power mode	-
		1	x	x	x	x	x	x	x	x	Dummy read	-
		1	D7	D6	D5	D4	D3	D2	0	0		-
0B	RDDMADCTL	0	0	0	0	0	1	0	1	1	Read display MADCTL	-
		1	x	x	x	x	x	x	x	x	Dummy read	-
		1	D7	D6	D5	D4	D3	D2	D1	D0		-
0C	RDDCOLMOD	0	0	0	0	0	1	1	0	0	Read display pixel format	-
		1	x	x	x	x	x	x	x	x	Dummy read	-
		1	-	D6	D5	D4	-	D2	D1	D0		-
0D	RDDIM	0	0	0	0	0	1	1	0	1	Read display image mode	-
		1	x	x	x	x	x	x	x	x	Dummy read	-
		1	D7	-	D5	D4	D3	D2	D1	D0		-
0E	RDDSM	0	0	0	0	0	1	1	1	0	Read display signal mode	-
		1	x	x	x	x	x	x	x	x	Dummy read	-
		1	D7	D6	D5	D4	D3	D2	-	D0		-
0F	RDDSDR	0	0	0	0	0	1	1	1	1	Read display self-diagnostic result	-
		1	x	x	x	x	x	x	x	x	Dummy read	-
		1	D7	D6	D5	D4	-	-	-	-		-
10	SLPIN	0	0	0	0	1	0	0	0	0	Sleep In	-
11	SLPOUT	0	0	0	0	1	0	0	0	1	Sleep Out	-
13	NORON	0	0	0	0	1	0	0	1	1	Normal display mode on	-
20	INVOFF	0	0	0	1	0	0	0	0	0	Display inversion off	-
21	INVON	0	0	0	1	0	0	0	0	1	Display inversion on	-
22	ALLPOFF	0	0	0	1	0	0	0	0	1	All pixel off (Black)	-
23	ALLPON	0	0	0	1	0	0	0	1	1	All pixel on (White)	-
26	GAMSET	0	0	0	1	0	0	1	1	0	Gamma set	-
		1					GC[7:0]					-
28	DISPOFF	0	0	0	1	0	1	0	0	0	Display off	-
29	DISPON	0	0	0	1	0	1	0	0	1	Display on	-

(Hex)	Operation code	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)	
34	TEOFF	0	0	0	1	1	0	1	0	0	Tearing Effect Line OFF	-	
35	TEON	0	0	0	1	1	0	1	0	1	Tearing Effect Line ON	-	
		1	X	X	X	X	X	X	X	M		-	
36	MADCTL	0	0	0	1	1	0	1	1	0	Memory access Control	-	
		1	B7	B6	B5	B4	B3	B2	B1	B0		-	
38	IDMOFF	0	0	0	1	1	1	0	0	0	Idle mode off	-	
39	IDMON	0	0	0	1	1	1	0	0	1	Idle mode on	-	
3A	COLMOD	0	0	0	1	1	1	0	1	0	Set Color Mode	-	
		1	X	D6	D5	D4	X	D2	D1	D0		-	
44	TESL	0	0	1	0	0	0	1	0	0	Tearing Effect Scan Line number	-	
		1	TELIN[15:8](8'b0)									-	
		1	TELIN[7:0](8'b0)									-	
		0	0	1	0	0	0	1	0	1	Return the current scanline SLN[15:0]	-	
45	GETSCAN	1	SLN[15:8]									-	
		1	SLN[7:0]									-	
4F	DSTBON	0	0	1	0	0	1	1	1	1	Deep Standby Mode On	-	
51	WRDISBV	0	0	1	0	1	0	0	0	1	Write Display Brightness	-	
		1	DBV[7:0]									-	
52	RDDISBV	0	0	1	0	1	0	0	1	0	Read Display Brightness Value	-	
		1	x	x	x	x	x	x	x	x	Dummy read	-	
		1	DBV[7:0]								-	-	
53	WRCTRLD	0	0	1	0	1	0	0	1	1	Write CTRL Display	-	
		1	X	X	BCTRL	X	DD	BL	X	X		-	
54	RDCTRLD	0	0	1	0	1	0	0	1	1	Read Control Value Display	-	
		x	x	x	x	x	x	x	x	x	Dummy read	-	
		1	0	0	BCTRL	0	DD	BL	0	0	-	-	
55	WRCABC	0	0	1	0	1	0	1	0	1	Write Adaptive Brightness Control	-	
		1	IMAGE_Enhance[3:0]									-	
56	RDCABC	0	0	1	0	1	0	1	1	0	Read Adaptive Brightness Control Content	-	
		1	x	x	x	x	x	x	x	x	Dummy read	-	
		1	IMAGE_Enhance[3:0]								-	-	
5E	WRCABCMB	0	0	1	0	1	1	1	1	0	Write CABC minimum brightness	-	
		1	CMB[7:0]									-	
5F	RDCABCMB	0	0	1	0	1	1	1	1	1	Read CABC minimum brightness	-	
		1	x	x	x	x	x	x	x	x	Dummy read	-	
		1	CMB[7:0]								-	-	
68	RDABCSDR	0	0	1	1	0	1	0	0	0	Read Automatic Brightness Control Self-Diagnostic Result	-	
		1	x	x	x	x	x	x	x	x	Dummy read	-	
		1	D[7:6]	0	0	0	0	0	0	0	-	-	
DA	RDID1	0	1	1	0	1	1	0	1	0	Read ID1	-	
		1	x	x	x	x	x	x	x	x	Dummy read	-	
		1	module's manufacturer[7:0]								-	-	
DB	RDID2	0	1	1	0	1	1	0	1	1	Read ID2	-	
		1	x	x	x	x	x	x	x	x	Dummy read	-	
		1	LCD module/driver version [7:0]								-	-	
DC	RDID3	0	1	1	0	1	1	1	0	0	Read ID3	-	
		1	x	x	x	x	x	x	x	x	Dummy read	-	
		1	LCD module/driver ID[7:0]								-	-	
A1	Read_DDB_start	0	1	0	1	0	0	0	0	1	Read the DDB from the provided location.	-	
		1	x	x	x	x	x	x	x	x	Dummy read	-	
		1	xx	xx	xx	xx	xx	xx	xx	xx	-	-	
		1	xx	xx	xx	xx	xx	xx	xx	xx	-	-	
		1	xx	xx	xx	xx	xx	xx	xx	xx	-	-	
A8	Read_DDB_continue	0	1	0	1	0	1	0	0	0	Continue reading the DDB from the last read location.	-	
		1	x	x	x	x	x	x	x	x	Dummy read	-	
		1	xx	xx	xx	xx	xx	xx	xx	xx	-	-	
		1	xx	xx	xx	xx	xx	xx	xx	xx	-	-	
		1	xx	xx	xx	xx	xx	xx	xx	xx	-	-	

Note: (1) Undefined commands are treated as NOP (00h) command.

(2) B0h to FFh are for factory use of display supplier.

6.1.2 User define command list table

User define command list is available only set “SETEXTC” command.

(Hex)	Operation Code	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)
B0	SETSEQUENCE	0	1	0	1	1	0	0	0	0	Set Sequence	-
		1	-	-	-	-	-	-	-	AUTO_OPT[6:0]		00
		1	-	-	-	-	-	-	-	OSC_EN		00
		1	VSP_DI SC	VSN_EN	VSP_EN	VGL_EN	VGH_EN	VCL_EN	VDDDN_HZ	STB		81
		1	-	-	-	-	GON	DTE	D[1:0]			0C
B1	SETPOWER	0	1	0	1	1	0	0	0	1	Set power related setting	-
		1	-	-	-	-	-	-	-	DUMMY		00
		1	-	DCLK_Reserved[2:0]	-	-	-	-	VGL_RE G_EN	DSTB		50
		1	-	FS2[3:0]	-	VRGH_EN	-	-	AP[2:0]			44
		1	-	-	-	VGHS[7:0]	-	-	-			DE
		1	-	-	-	VGLS[7:0]	-	-	-			94
		1	-	-	-	VGL_REGS[5:0]	-	-	-			08
		1	-	-	-	VRGH[5:0]	-	-	-			11
		1	-	-	-	BTP[4:0]	-	-	-			B1
		1	-	VCL[2:0]	-	BTN[4:0]	-	-	-			11
		1	-	-	-	VRHP[7:0]	-	-	-			36
		1	-	-	-	VRHN[7:0]	-	-	-			3E
		1	APF_EN	DD_TU	-	VRMP[5:0]	-	-	-			9A
		1	-	-	-	VRMN[5:0]	-	-	-			1A
		1	-	FS1[3:0]	-	-	-	-	PCCS[2:0]			42
		1	DT[1:0]	-	-	-	-	-	FS0[4:0]			1B
		1	-	XDK[2:0]	-	XDKN[2:0]	-	-	AUTO_X DK			6E
		1	CLK_OP T2	CLK_OP T1	DC_VPNL[1:0]	-	-	-	DCDIV[3:0]			F1
		1	DCS[1:0]	-	DTPS[2:0]	-	-	-	DTNS[2:0]			C0
		1	A_DC[1:0]	-	A_DTP[2:0]	-	-	-	A_DTN[2:0]			E6
		1	B_DC[1:0]	-	B_DTP[2:0]	-	-	-	B_DTN[2:0]			E6
		1	C_DC[1:0]	-	C_DTP[2:0]	-	-	-	C_DTN[2:0]			E6
		1	D_DC[1:0]	-	D_DTP[2:0]	-	-	-	D_DTN[2:0]			E6
		1	E_DC[1:0]	-	E_DTP[2:0]	-	-	-	E_DTN[2:0]			E6
		1	-	-	-	-	-	-	DUMMY			00
		1	-	FS0_LP[2:0]	-	-	-	-	BTP0[4:0]			04
		1	-	FS1_LP[1:0]	-	-	-	-	BTP1[4:0]			05
		1	-	DC_DIV_LP[1:0]	-	-	-	-	BTP2[4:0]			0A
		1	-	DTP_LP[1:0]	-	-	-	-	BTP3[4:0]			0B
		1	-	DTN_LP[1:0]	-	-	-	-	BTP4[4:0]			04
		1	-	FS2_LP[1:0]	-	-	-	-	BTP5[4:0]			05
B2	SETDISP	0	1	0	1	1	0	0	1	0	Set display related register	-
		1	-	-	-	-	-	-	-	DUMMY		00
		1	-	-	-	-	-	-	-	DUMMY		00
		1	-	-	-	NL[7:0]	-	-	-			44
		1	-	-	-	BP [7:0]	-	-	-			OB
		1	-	-	-	FP [7:0]	-	-	-			11
		1	-	-	-	RTN[7:0]	-	-	-			19
		1	-	SAP[3:0]	-	ABC_CLK_DIV[1:0]	vs_plus_bp_en	ABC_HS_BYPASS	-			22
		1	-	-	GEN_ON[7:0]	-	-	-				00
		1	-	-	GEN_OFF[7:0]	-	-	-				FF
		1	-	-	BP_PE [7:0]	-	-	-				0B
		1	-	-	FP_PE [7:0]	-	-	-				11
		1	-	-	RTN_PE[7:0]	-	-	-				19
B3	SETRGBIF	0	1	0	1	1	0	0	1	1	Set DPI interface related register	-
		1	-	-	DPICC[1:0]	-	DPL	HSPL	VSPL	EPL		01
B4	SETCYC	0	1	0	1	1	0	1	0	0	Set Display waveform cycles	-
		1	ZZ_LR	ZZ_EO	-	NW_PE[2:0]	-	-	-	NW[2:0]		80
		1	-	-	-	USER_GIP_GATE[7:0]	-	-	-	-		04
		1	GIP_FR[1:0]	BLK_OS_CSEL	-	STV_as_CK	-	-	-	GIP_FR_MODE		00
		1	-	SHR0_3[3:0]	-	-	-	-	SHR0_2[3:0]	-		32
		1	-	SHR0_1[3:0]	-	-	-	-	SHR0[11:8]	-		10
		1	-	-	-	SHR0[7:0]	-	-	-	-		00

(Hex)	Operation Code	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)
		1		SHR1_3[3:0]				SHR1_2[3:0]				32
		1		SHR1_1[3:0]				SHR1[11:8]				13
		1			SHR1[7:0]							70
		1		SHR2_3[3:0]				SHR2_2[3:0]				32
		1		SHR2_1[3:0]				SHR2[11:8]				10
		1			SHR2[7:0]							08
		1		SHP[3:0]				SCP[3:0]				37
		1			SPON[7:0]							00
		1		SPOFF[7:0]								40
		1			CHR[7:0]							0A
		1		CHP[3:0]				CCP[3:0]				37
		1			CON[7:0]							08
		1		COFF[7:0]								28
		1		SON[7:0]								08
		1		SOFF[7:0]								30
		1		EQON2[7:0]								30
		1		EQON1[7:0]								04
		1		SPON_MPU[7:0]								00
		1		SPOFF_MPU[7:0]								40
		1		CON_MPU[7:0]								28
		1		COFF_MPU[7:0]								3A
		1		SON_MPU[7:0]								08
		1		SOFF_MPU[7:0]								30
		1		EQON2_MPU[7:0]								30
		1		EQON1_MPU[7:0]								04
B5	SET_Porch_Mode	0	1	0	1	1	0	1	0	1	SET Porch Mode	-
		1			RGB_VP[10:8]							00
		1				RGB_VP[7:0]						00
		1				RGB_HP[7:0]						00
B6	SETVCOM (OTPx3)	0	1	0	1	1	0	1	1	0	Set VCOM Voltage	-
		1	-	-	-	-	-	-	-	-		00
		1			VCMC_F[7:0]							86
		1	-	-	-	-	-	-	-	-		00
		1			VCMC_B[7:0]							86
		1		VCOM_TIMES[2:0]								E0
B7	SETTE	0	1	0	1	1	0	1	1	1	Set TE Function	-
		1	-	-	TE_SEL[1:0]			TEI[3:0]				00
		1	TEL_SEL[1:0]	TER_SEL[1:0]	-			TEP[10:8]				00
		1				TEP[7:0]						00
B8	SETGPO	0	1	0	1	1	1	0	0	0	Set GPIO	00
				GPO1SEL[3:0]				GPO0SEL[3:0]				00
				GPO3SEL[3:0]				GPO2SEL[3:0]				00
B9	SETEXTC	0	1	0	1	1	1	0	0	1	Set extended command set	-
		1			EXTC1[7:0]							00/FF
		1			EXTC2[7:0]							00/83
		1			EXTC3[7:0]							00/79
BB	SETOTP	0	1	0	1	1	1	0	1	1	Set OTP	-
		1			OTP_MASK[7:0]							00
		1										00
		1			OTP_INDEX[7:0]							FF
		1	OTP_LOAD_DISABLE	OTP_TE_ST	OTP_PO_R	OTP_P_W	OTP_PT	PTM[1:0]	VPP_SE_L	OTP_PR_OG		00
		1										xx
								OTP_DATA[7:0]				
C1	SETDGLUT	0	1	1	0	0	0	0	0	1	Set DGC LUT	-
		1	-	-	-	-	-	-	DITH_O_PT	DGC_EN		00
		1			D1[7:0]							
		1				:						
		1			Dn[7:0]							
		1			D126[7:0]							
C3	SETID (OTPx3)	0	1	1	0	0	0	0	1	1	Set ID	-
		1			ID1[7:0]							83
		1			ID2[7:0]							79
		1			ID3[7:0]							0A
		1			ID4[7:0]							00
		1		ID_TIMES[2:0]	-	-	-	-	-	-		E0

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June, 2012

(Hex)	Operation Code	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)
C4	SETDDB	0	1	1	0	0	0	1	0	0	Set DDB	-
		1					DDB1[7:0]					00
		1					DDB2[7:0]					00
		1					DDB3[7:0]					00
		1					DDB4[7:0]					00
C9	SETCABC	0	1	1	0	0	1	0	0	1	Set CABC Control	-
		1	-		SEL_PWMCLK[2:0]		SEL_GAIN[1:0]	INVPULS	SEL_BLD_UTY			0F
		1			PWM_PERIOD[7:0]							C5
		1	CABC_FSYNC				DIM_FRAME[6:0]					1E
		1			CABC_STEP[7:0]							1E
		1			CABC_CLKEN[7:0]							00
		1	CABC_DD		SAVEPOWER[6:0]							00
		1			MEAN_OFFSET[7:0]							00
		1	-	-	-	-	CABC_FLM[3:0]					01
		1	-	-	EN_DIM_MIX	EN_COS_T_MEAN	EN_COS_T	EN_NLN_GAIN	EN_JUDGE	EN_TEM_P		3E
CA	SETCABCGAIN	0	1	1	0	0	1	0	1	0	Set CABC Gain	--
		1	-				DBG0[6:0]					40
		1	-				DBG1[6:0]					3C
		1	-				DBG2[6:0]					38
		1	-				DBG3[6:0]					34
		1	-				DBG4[6:0]					33
		1	-				DBG5[6:0]					32
		1	-				DBG6[6:0]					2B
		1	-				DBG7[6:0]					24
		1	-				DBG8[6:0]					22
CB	SETCLOCK	0	1	1	0	0	1	0	1	1		--
		1	-	-	-	-		UADJ[3:0]				07
		1	-	-	-	-		UADJ_PE[3:0]				07
CC	SETPANEL	0	1	1	0	0	1	1	0	0	Set panel related register	-
		1	-	-	-	-	SS_PANEL	GS_PANEL	REV_PANEL	BGR_PANEL		00
E0	SETGAMMA	0	1	1	1	0	0	0	0	0	Set Gamma Curve Related Setting	-
		1					SETGAMMA_PASSWD[7:0]					
		1	-	-			G1_VRP0[5:0]					05
		1	-	-			G1_VRP1[5:0]					0C
		1	-	-			G1_VRP2[5:0]					13
		1	-	-			G1_VRP3[5:0]					20
		1	-	-			G1_VRP4[5:0]					39
		1	-	-			G1_VRP5[5:0]					3F
		1	-	-			G1_PRP0[6:0]					24
		1	-	-			G1_PRP1[6:0]					39
		1	G1_CGMP0[1:0]	-			G1_PKP0[4:0]					08
		1	G1_CGMP1[1:0]	-			G1_PKP1[4:0]					0C
		1	G1_CGMP2[1:0]	-			G1_PKP2[4:0]					10
		1	G1_CGMP3[1:0]	-			G1_PKP3[4:0]					16
		1	G1_CGMP5[1:0]	G1_CGM_P4	-		G1_PKP4[4:0]					1A
		1	-	-	-		G1_PKP5[4:0]					17
		1	-	-	-		G1_PKP6[4:0]					17
		1	-	-	-		G1_PKP7[4:0]					0D
		1	-	-	-		G1_PKP8[4:0]					12
		1	-	-			G1_VRN0[5:0]					05
		1	-	-			G1_VRN1[5:0]					0C
		1	-	-			G1_VRN2[5:0]					11
		1	-	-			G1_VRN3[5:0]					27
		1	-	-			G1_VRN4[5:0]					3B
		1	-	-			G1_VRN5[5:0]					3F
		1	-				G1_PRN0[6:0]					21
		1	-				G1_PRN1[6:0]					3A
		1	G1_CGMN0[1:0]	-			G1_PKN0[4:0]					04
		1	G1_CGMN1[1:0]	-			G1_PKN1[4:0]					0B
		1	G1_CGMN2[1:0]	-			G1_PKN2[4:0]					0F
		1	G1_CGMN3[1:0]	-			G1_PKN3[4:0]					15
		1	G1_CGMN5[1:0]	G1_CGM_N4	-		G1_PKN4[4:0]					17
		1	-	-	-		G1_PKN5[4:0]					15
		1	-	-	-		G1_PKN6[4:0]					16
		1	-	-	-		G1_PKN7[4:0]					0D

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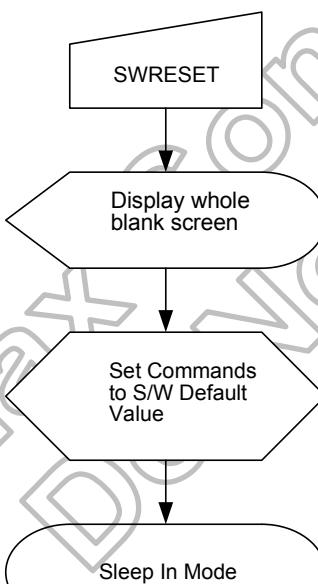
(Hex)	Operation Code	DCX	D7	D6	D5	D4	D3	D2	D1	D0	Function	Default (Hex)
		1	-	-	-			G1_PKN8[4:0]				17
E4	SETCHEMODE_DYN	0	1	1	1	0	0	1	0	0	Set color enhancement mode	--
		1	HUE_MODE[1:0]		SE_MODE[1:0]		BE_MODE[1:0]		CE_MODE[1:0]			00
		1	-	-	-	-	-	-	-	DYN_CE_H_EN		01
		0	1	1	1	0	1	1	0	0		-
E9	SETOTPKEY	1				OTP_KEY0[7:0]					Set OTP Key	00/AA
		1				OTP_KEY1[7:0]						00/55
		0	1	1	1	1	0	1	0	0		-
F4	GETHXID	1				Himax ID[7:0]					Get Himax ID	79
		0	1	1	1	1	1	1	0	1		-
FD	SETCNCD/GETCNCD	1				WR_CMD_CN[7:0]					Set/Get Continue Command	-
		0	1	1	1	1	1	1	1	0		-
FE	SET READ INDEX	0	1	1	1	1	1	1	1	0	SET READ Command Address	-
		1				CMD_ADD[7:0]						00
FF	GETSPIREAD	0	1	1	1	1	1	1	1	1	Read Command Data	-
		1				CMD_DATA1[7:0]						-
		1				:						-
		1				CMD_DATAN[7:0]						-

6.2 Standard Command Description

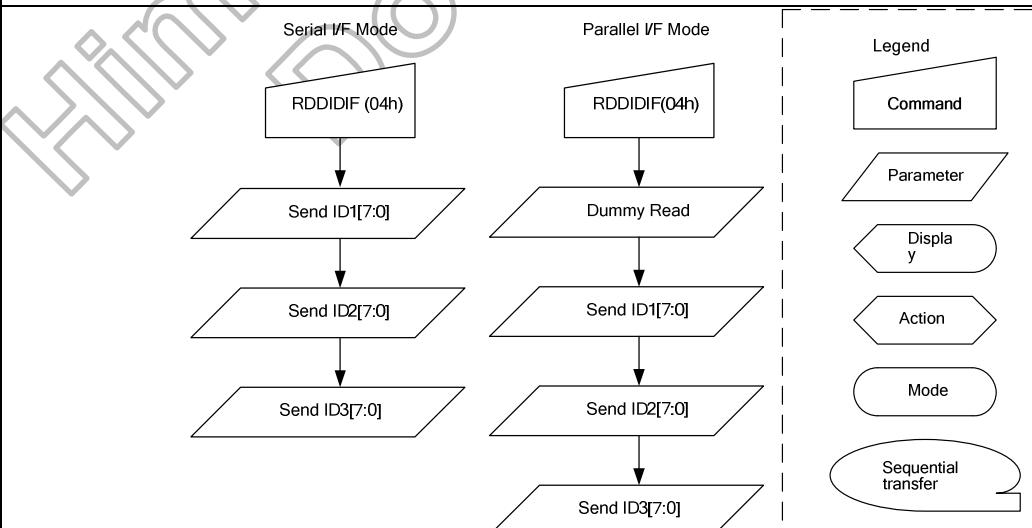
6.2.1 NOP (00h)

00H	NOP (No Operation)																		
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX						
Command	0	1	↑	-	0	0	0	0	0	0	0	0	00						
Parameter	NO PARAMETER																		
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write or Read as described in RAMWR (Memory Write) and RAMRD (Memory Read) Commands.																		
Restriction	-																		
Register Availability	Status							Availability											
	Normal Mode On, Idle Mode Off, Sleep Out							Yes											
	Normal Mode On, Idle Mode On, Sleep Out							Yes											
	Partial Mode On, Idle Mode Off, Sleep Out							Yes											
	Partial Mode On, Idle Mode On, Sleep Out							Yes											
Default		N/A																	
Flow Chart		-																	

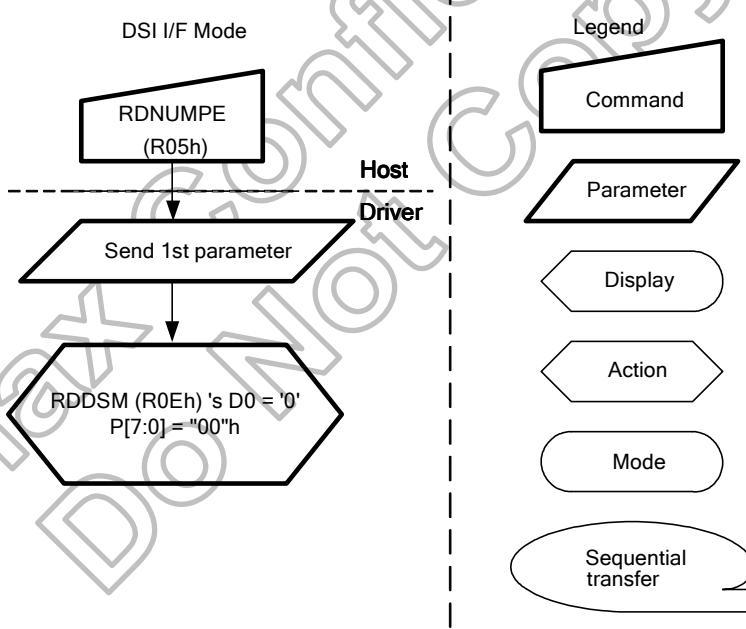
6.2.2 Software reset (01h)

01H	SWRESET (Software Reset)																									
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	1	0	0	0	0	0	0	0	1	01													
Parameter	NO PARAMETER																									
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.) Note: The Frame Memory contents are unaffected by this command. It will be necessary to wait 5msec before sending new command following software reset.																									
Restriction	The display module loads all display supplier's factory default values to the registers during this 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep out command. Software Reset Command cannot be sent during Sleep Out sequence.																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																									
Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In or Booster Off	Yes																									
Default	N/A																									
Flow Chart	 <p>Legend:</p> <ul style="list-style-type: none"> Red and Blue Parameter Display Action Mode Sequential transfer <pre> graph TD SWRESET[SWRESET] --> Display[Display whole blank screen] Display --> Set[Set Commands to S/W Default Value] Set --> SleepIn[Sleep In Mode] </pre>																									

6.2.3 Read Display Identification Information (04h)

04H		RDDIDIF (Read Display Identification Information)																																	
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																						
Command	0	1	↑	-	0	0	0	0	0	1	0	0	04																						
1 st parameter	1	↑	1	-	ID1[7:0]								xx																						
2 nd parameter	1	↑	1	-	ID2[7:0]								xx																						
3 rd parameter	1	↑	1	-	ID3[7:0]								xx																						
Description	This read byte returns 24-bit display identification information. The 1 st Parameter is dummy read. The 2 nd Parameter identifies the LCD module's manufacturer. It is specified by display supplier and for xx is defined as xxHEX. The 3 rd Parameter has 2 purposes. Bit7 (MSB) defines the type of panel. 0=Driver (STN B/W), 1=Module (Colour). Bits 6..0 are used to track the LCD module/driver version. It is defined by display supplier and it changes each time a revision is made to the display, material or construction specifications. See Table: <table border="1"> <thead> <tr> <th>ID Byte Value V[7:0]</th> <th>Version</th> <th>Changes</th> </tr> </thead> <tbody> <tr><td>80h</td><td>-</td><td>-</td></tr> <tr><td>81h</td><td>-</td><td>-</td></tr> <tr><td>82h</td><td>-</td><td>-</td></tr> <tr><td>83h</td><td>-</td><td>-</td></tr> <tr><td>84h</td><td>-</td><td>-</td></tr> <tr><td>85h</td><td>-</td><td>-</td></tr> </tbody> </table> The 4 th parameter identifies the LCD module/driver. It is specified by display supplier and for this LCD project module is defined as xxHEX.														ID Byte Value V[7:0]	Version	Changes	80h	-	-	81h	-	-	82h	-	-	83h	-	-	84h	-	-	85h	-	-
ID Byte Value V[7:0]	Version	Changes																																	
80h	-	-																																	
81h	-	-																																	
82h	-	-																																	
83h	-	-																																	
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Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr><td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr><td>Sleep In or Booster Off</td><td>Yes</td></tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes									
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Status	Default Value																																		
Power On Sequence	OTP Value																																		
S/W Reset	OTP Value																																		
H/W Reset	OTP Value																																		
Flow Chart	 <pre> graph TD Start((RDDIDIF (04h))) --> Send1[/Send ID1[7:0]/] Start --> Send2[/Send ID2[7:0]/] Start --> Send3[/Send ID3[7:0]/] subgraph "Serial I/F Mode" Send1 Send2 Send3 end subgraph "Parallel I/F Mode" Send1 DummyRead[/Dummy Read/] Send2 Send3 end Legend[Legend] Legend --- Command Legend --- Parameter Legend --- Display Legend --- Action Legend --- Mode Legend --- SequentialTransfer([Sequential transfer]) </pre>																																		

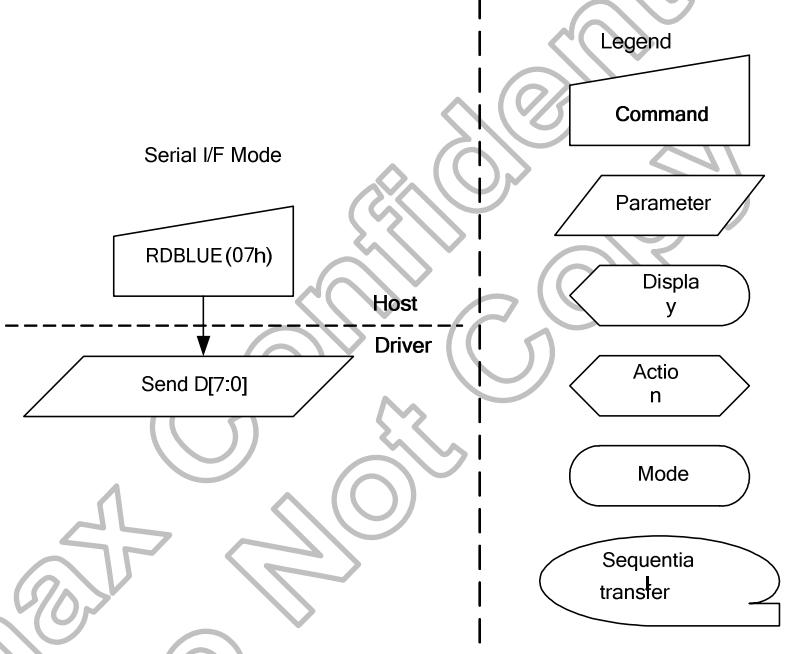
6.2.4 RDNUMPE: Read number of the parity errors (05h)

05H	RDNUMPE (Read Number of the Parity Errors)																								
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	-	0	0	0	0	0	1	0	1	05												
1 st parameter	1	↑	1	-	P7	P6	P5	P4	P3	P2	P1	P0	xx												
Description	<p>The first parameter is telling a number of the errors on DSI. The more detailed description of the bits is below.</p> <p>P[6..0] bits are telling a number of the errors.</p> <p>P[7] is set to '1' if there is overflow with P[6..0] bits.</p> <p>P[7..0] bits are set to '0's (as well as RDDSM(0Eh)'s D0 is set '0' at the same time) after there is sent the second parameter information (The read function is completed).</p>																								
Restriction	SETEXTC turn on to enable this command																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
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Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	P[7:0] = 0x00h																								
Flow Chart	 <pre> graph TD Start[DSI I/F Mode] --> RDNUMPE[RDNUMPE (R05h)] RDNUMPE --> Send1st[Send 1st parameter] Send1st --> RDDSM_Octagon{RDDSM (R0Eh) 's D0 = '0' P[7:0] = "00"h''} </pre>																								

6.2.5 Get_red_channel (06h)

06H	RDRED (Read Red Colour)																							
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command	0	1	↑	-	0	0	0	0	0	1	1	0	06											
1 st parameter	1	↑	1	-	R7	R6	R5	R4	R3	R2	R1	R0	xx											
Description	The first parameter is telling red colour value of the first pixel of the frame when there is used DPI I/F. 16 bit format: R5 is MSB and R1 is LSB. R7, R6 and R0 are set to '0'. 18 bit format: R5 is MSB and R0 is LSB. R7 and R6 are set to '0'.																							
Restriction	-																							
Register Availability	Status		Availability																					
	Sleep Out		Yes																					
	Sleep In		Yes																					
Default	R[7:0] = 0x00h																							
Flow Chart	<pre> graph TD RDBLUE[RDBLUE(06h)] --> Send[Send D[7:0]] subgraph HostDriver [Host Driver] Send end Legend[Legend] Legend --- Command Legend --- Parameter Legend --- Display Legend --- Action Legend --- Mode Legend --- Sequential[Sequential transfer] </pre>																							

6.2.6 Get_green_channel (07h)

07H	RDGREEN (Read Green Colour)																					
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	0	1	↑	-	0	0	0	0	0	1	1	1	07									
1 st parameter	1	↑	1	-	G7	G6	G5	G4	G3	G2	G1	G0	xx									
Description	The first parameter is telling green colour value of the first pixel of the frame when there is used DPI I/F. 16 and 18 bit formats: G5 is MSB and G0 is LSB. G7 and G6 are set to '0'.																					
Restriction	-																					
Register Availability	Status				Availability																	
	Sleep Out				Yes																	
	Sleep In				Yes																	
Default	G[7:0] = 0x00h																					
Flow Chart	 <pre> graph TD Host[Host] -- "RDBLUE(07h)" --> Driver[Driver] subgraph Legend [Legend] direction TB C[Command] --- P[Parameter] D[Display] --- A[Action] M[Mode] --- ST[Sequential transfer] end subgraph Host [Host] direction TB R[D[7:0]] --- S[Send D[7:0]] end subgraph Driver [Driver] direction TB RDBLUE[RDBLUE(07h)] end </pre>																					

6.2.7 Get_blue_channel (08h)

08H	RDBLUE (Read Blue Colour)																							
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command	0	1	↑	-	0	0	0	0	1	0	0	0	08											
1 st parameter	1	↑	1	-	B7	B6	B5	B4	B3	B2	B1	B0	xx											
Description	The first parameter is telling blue colour value of the first pixel of the frame when there is used DPI I/F. 16 bit format: B5 is MSB and B1 is LSB. B7, B6 and B0 are set to '0'. 18 bit format: B5 is MSB and B0 is LSB. B7 and B6 are set to '0'.																							
Restriction	-																							
Register Availability	Status		Availability																					
	Sleep Out		Yes																					
	Sleep In		Yes																					
Default	B[7:0] = 0x00h																							
Flow Chart	<pre> graph TD subgraph Host [Host] direction TB H_RDBLUE[RDBLUE(08h)] H_SendD[Send D[7:0]] end subgraph Driver [Driver] direction TB D_RDBLUE[RDBLUE(08h)] D_D[Display] D_A[Action] D_M[Mode] D_ST[Sequential transfer] end H_RDBLUE --> H_SendD H_SendD --> D_RDBLUE legend Command --- H_RDBLUE Parameter --- D_RDBLUE Display --- D_D Action --- D_A Mode --- D_M Sequential transfer --- D_ST </pre>																							

6.2.8 Read Display Status (09h)

09H	RDDST (Read Display Status)																																																																																																																
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																				
Command	0	1	↑	-	0	0	0	0	1	0	0	1	09																																																																																																				
1 st parameter	1	↑	1	-	D[31:24]								xx																																																																																																				
2 nd parameter	1	↑	1	-	D[23:16]								xx																																																																																																				
3 rd parameter	1	↑	1	-	D[15:8]								xx																																																																																																				
4 th parameter	1	↑	1	-	D[7:0]								xx																																																																																																				
Description	This command indicates the current status of the display as described in the table below: <table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Comment</th> </tr> </thead> <tbody> <tr><td>D31</td><td>Booster Voltage Status</td><td>-</td></tr> <tr><td>D30</td><td>Page Address Order</td><td>-</td></tr> <tr><td>D29</td><td>Column Address Order</td><td>-</td></tr> <tr><td>D28</td><td>Page/Column Order</td><td>-</td></tr> <tr><td>D27</td><td>Display Device Line Refresh Order</td><td>-</td></tr> <tr><td>D26</td><td>RGB/BGR Order</td><td>-</td></tr> <tr><td>D25</td><td>Display Data Latch Data Order</td><td>-</td></tr> <tr><td>D24</td><td>Source san sequence</td><td>-</td></tr> <tr><td>D23</td><td>Gate san sequence</td><td>-</td></tr> <tr><td>D22</td><td colspan="2" style="text-align:center;">Interface Colour Pixel Format Definition</td></tr> <tr><td>D21</td><td colspan="2" style="text-align:center;">-</td></tr> <tr><td>D20</td><td colspan="2" style="text-align:center;">-</td></tr> <tr><td>D19</td><td>Idle Mode On/Off</td><td>-</td></tr> <tr><td>D18</td><td>--</td><td>Set to '0'</td></tr> <tr><td>D17</td><td>Sleep In/Out</td><td>-</td></tr> <tr><td>D16</td><td>Display Normal Mode On/Off</td><td>-</td></tr> <tr><td>D15</td><td>--</td><td>Set to '0'</td></tr> <tr><td>D14</td><td>--</td><td>Set to '0'</td></tr> <tr><td>D13</td><td>Inversion Status</td><td>-</td></tr> <tr><td>D12</td><td>All Pixels On</td><td>-</td></tr> <tr><td>D11</td><td>All Pixels Off</td><td>-</td></tr> <tr><td>D10</td><td>Display On/Off</td><td>-</td></tr> <tr><td>D9</td><td>Tearing Effect Line On/Off</td><td>-</td></tr> <tr><td>D8</td><td colspan="2" style="text-align:center;">Gamma Curve Selection</td></tr> <tr><td>D7</td><td colspan="2" style="text-align:center;">-</td></tr> <tr><td>D6</td><td colspan="2" style="text-align:center;">-</td></tr> <tr><td>D5</td><td>Tearing Effect Output Line Mode</td><td>-</td></tr> <tr><td>D4</td><td>Horizontal Sync. (HSYNC, DPI I/F)</td><td>-</td></tr> <tr><td>D3</td><td>Vertical Sync. (VSYNC, DPI I/F)</td><td>-</td></tr> <tr><td>D2</td><td>Pixel Clock (DCK, DPI I/F)</td><td>-</td></tr> <tr><td>D1</td><td>Data Enable (ENABLE, DPI I/F)</td><td>-</td></tr> <tr><td>D0</td><td>Parity Error on DS1</td><td>-</td></tr> </tbody> </table> Bit Values are explained overleaf. Bit D31 – Booster Voltage Status '0' = Booster Off. '1' = Booster On. Bit D30 – Page Address Order '0' = Top to Bottom (When MADCTL B7='0'). '1' = Bottom to Top (When MADCTL B7='1'). Bit D29 – Column Address Order '0' = Left to Right (When MADCTL B6='0'). '1' = Right to Left (When MADCTL B6='1'). Bit D28 – Page/Column Order '0' = Normal (When MADCTL B5='0'). '1' = Rotation (When MADCTL B5='1'). Bit D27 – Line Address Order '0' = LCD Refresh Top to Bottom (When MADCTL B4='0'). '1' = LCD Refresh Bottom to Top (When MADCTL B4='1'). Bit D26 – RGB/BGR Order '0' = RGB (When MADCTL B3='0'). '1' = BGR (When MADCTL B3='1').														Bit	Description	Comment	D31	Booster Voltage Status	-	D30	Page Address Order	-	D29	Column Address Order	-	D28	Page/Column Order	-	D27	Display Device Line Refresh Order	-	D26	RGB/BGR Order	-	D25	Display Data Latch Data Order	-	D24	Source san sequence	-	D23	Gate san sequence	-	D22	Interface Colour Pixel Format Definition		D21	-		D20	-		D19	Idle Mode On/Off	-	D18	--	Set to '0'	D17	Sleep In/Out	-	D16	Display Normal Mode On/Off	-	D15	--	Set to '0'	D14	--	Set to '0'	D13	Inversion Status	-	D12	All Pixels On	-	D11	All Pixels Off	-	D10	Display On/Off	-	D9	Tearing Effect Line On/Off	-	D8	Gamma Curve Selection		D7	-		D6	-		D5	Tearing Effect Output Line Mode	-	D4	Horizontal Sync. (HSYNC, DPI I/F)	-	D3	Vertical Sync. (VSYNC, DPI I/F)	-	D2	Pixel Clock (DCK, DPI I/F)	-	D1	Data Enable (ENABLE, DPI I/F)	-	D0	Parity Error on DS1	-
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'0' = LCD Refresh Left to Right (When MADCTL B2='0').

'1' = LCD Refresh Right to Left (When MADCTL B2='1').

Bit D24 – Source scan sequence

'0' = Source output Left to Right (When MADCTL B1='0').

'1' = Source output Right to Left (When MADCTL B1='1').

Bit D23 – Gate scan sequence

'0' = Gate output Top to Bottom (When MADCTL B0='0').

'1' = Gate output Bottom to Top (When MADCTL B0='1').

Bits D22, D21, D20 – Interface Colour Pixel Format Definition

Interface Format	D22	D21	D20
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
Not Defined	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
24 Bit/Pixel	1	1	1

Bit D19 – Idle Mode On/Off

'0' = Idle Mode Off.

'1' = Idle Mode On.

Bit D17 – Sleep In/Out

'0' = Sleep In Mode.

'1' = Sleep Out Mode.

Bit D16 – Display Normal Mode On/Off

'0' = Partial or Scrolling Mode.

'1' = Normal Mode.

Bit D13 – Inversion On/Off

'0' = Inversion is Off.

'1' = Inversion is On.

Bit D12 – All Pixels On.

'0' = Normal mode.

'1' = All Pixels On.

Bit D11 – All Pixels Off.

'0' = Normal mode.

'1' = All Pixels Off.

Bit D10 – Display On/Off

'0' = Display is Off.

'1' = Display is On.

Bit D9 – Tearing Effect Line On/Off

'0' = Tearing Effect Line Off.

'1' = Tearing Effect On.

Bits D8, D7, D6 – Gamma Curve Selection

Gamma Curve Selected	B8	B7	B6	Gamma Set (26h) Parameter
Gamma Curve 1	0	0	0	Reserved
Gamma Curve 2	0	0	1	Reserved
Gamma Curve 3	0	1	0	Reserved
Gamma Curve 4	0	1	1	Reserved
Not Defined	1	0	0	Not Defined
Not Defined	1	0	1	Not Defined
Not Defined	1	1	0	Not Defined
Not Defined	1	1	1	Not Defined

Bit D5 – Tearing Effect Line Output Mode.

'0' = Mode 1, V-Blanking only.

'1' = Mode 2, both H-Blanking and V-Blanking.

Bit D4 – Horizontal Sync. (DPI I/F) On/Off, Note 1.

'0' = Horizontal Sync. line is Off ("Low").

'1' = Horizontal Sync. line is On ("High").

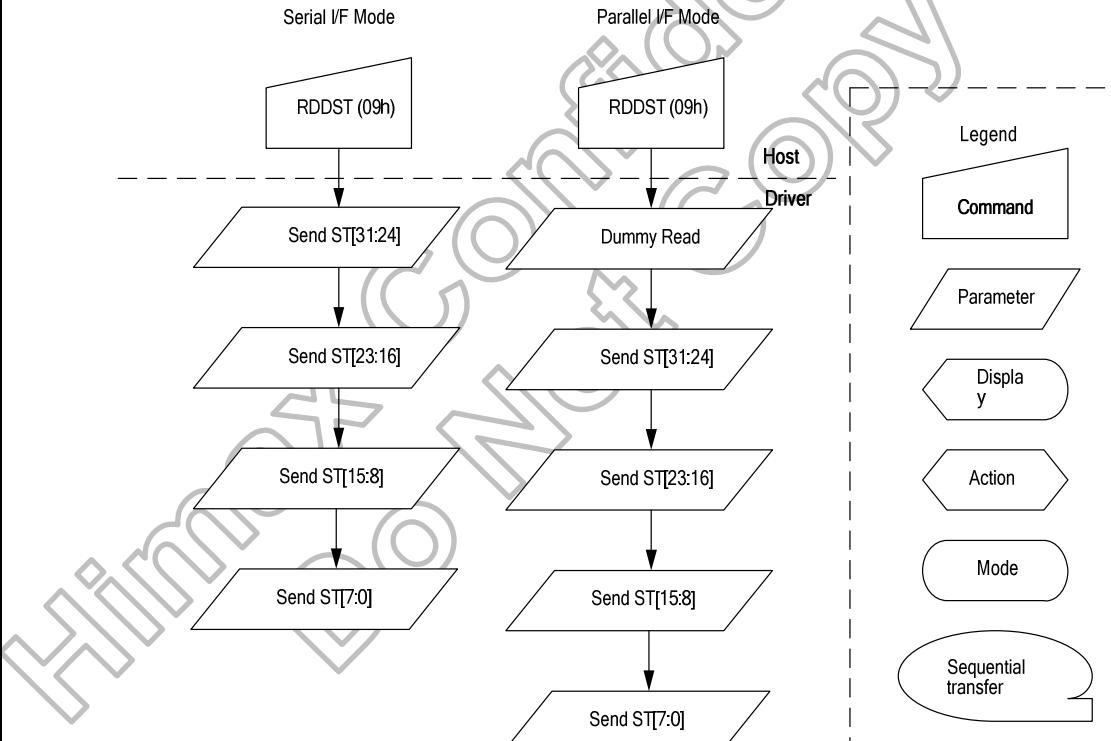
Bit D3 – Vertical Sync. (DPI I/F) On/Off, Note 1.

'0' = Vertical Sync. line is Off ("Low").

'1' = Vertical Sync. line is On ("High").

Bit D2 – Pixel Clock (PCLK, DPI I/F) On/Off, Note 1.

'0' = PCLK line is Off ("Low").

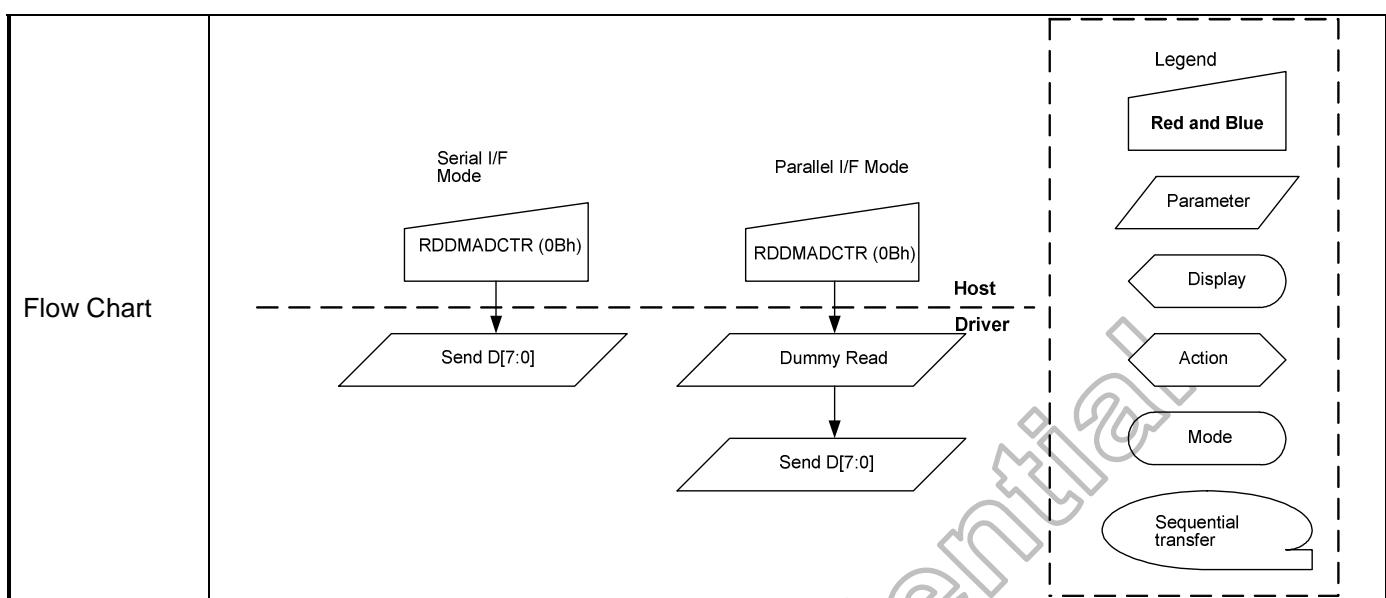
	<p>Bit D1 – Data Enable (DE, DPI I/F) On/Off, Note 1. '0' = DE line is Off ("Low"). '1' = DE line is On ("High"). Bit D0–Parity Error on DSI. '0'=No Parity Error. '1'=Parity Error.</p> <p>Note: This bit indicates current status of the line when this command has been sent.</p>												
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S/W Reset	See description												
H/W Reset	See description												
Flow Chart	 <pre> graph TD subgraph Serial_I_F [Serial I/F Mode] RDDST_S[RDDST (09h)] --> Send_ST_31_24[Send ST[31:24]] Send_ST_31_24 --> Send_ST_23_16[Send ST[23:16]] Send_ST_23_16 --> Send_ST_15_8[Send ST[15:8]] Send_ST_15_8 --> Send_ST_7_0[Send ST[7:0]] end subgraph Parallel_I_F [Parallel I/F Mode] RDDST_P[RDDST (09h)] --> DummyRead[Dummy Read] DummyRead --> Send_ST_31_24_P[Send ST[31:24]] Send_ST_31_24_P --> Send_ST_15_8_P[Send ST[15:8]] end </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

6.2.9 Get_power_mode (0Ah)

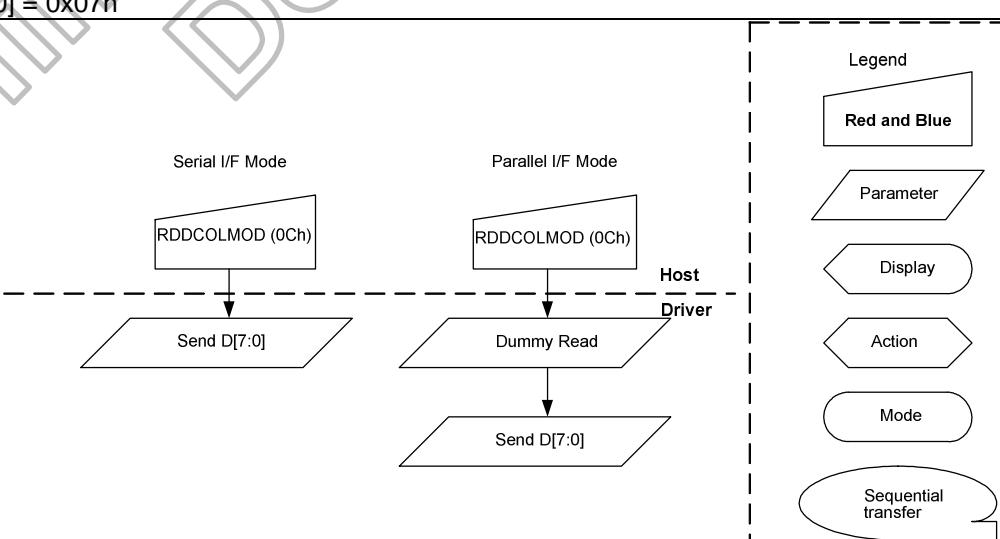
0AH		RDDPM (Read Display Power Mode)																																							
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																												
Command	0	1	↑	-	0	0	0	0	1	0	1	0	0A																												
1 st parameter	1	↑	1	-	D7	D6	D5	D4	D3	D2	0	0	xx																												
		This command indicates the current status of the display as described in the table below:																																							
		<table border="1"> <thead> <tr> <th>Bit</th><th>Description</th><th>Comment</th></tr> </thead> <tbody> <tr> <td>D7</td><td>--</td><td>Set to '0'</td></tr> <tr> <td>D6</td><td>Idle Mode On/Off</td><td>-</td></tr> <tr> <td>D5</td><td>--</td><td>-</td></tr> <tr> <td>D4</td><td>Sleep In/Out</td><td>Set to '0'</td></tr> <tr> <td>D3</td><td>Display Normal Mode On/Off</td><td>-</td></tr> <tr> <td>D2</td><td>Display On/Off</td><td>-</td></tr> <tr> <td>D1</td><td>--</td><td>Set to '0'</td></tr> <tr> <td>D0</td><td>--</td><td>Set to '0'</td></tr> </tbody> </table>													Bit	Description	Comment	D7	--	Set to '0'	D6	Idle Mode On/Off	-	D5	--	-	D4	Sleep In/Out	Set to '0'	D3	Display Normal Mode On/Off	-	D2	Display On/Off	-	D1	--	Set to '0'	D0	--	Set to '0'
Bit	Description	Comment																																							
D7	--	Set to '0'																																							
D6	Idle Mode On/Off	-																																							
D5	--	-																																							
D4	Sleep In/Out	Set to '0'																																							
D3	Display Normal Mode On/Off	-																																							
D2	Display On/Off	-																																							
D1	--	Set to '0'																																							
D0	--	Set to '0'																																							
Description	<p>Bits D7, D5, D1 and D0 for future use and are set to '0'.</p> <p>Bit D6 – Idle Mode On/Off</p> <p>'0' = Idle Mode Off.</p> <p>'1' = Idle Mode On.</p> <p>Bit D4 – Sleep In/Out</p> <p>'0' = Sleep In Mode.</p> <p>'1' = Sleep Out Mode.</p> <p>Bit D3 – Display Normal Mode On/Off</p> <p>'0' = Display Normal Mode Off.</p> <p>'1' = Display Normal Mode On.</p> <p>Bit D2 – Display On/Off</p> <p>'0' = Display is Off.</p>																																								
Restrictions	-																																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In or Booster Off</td><td>Yes</td></tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes															
Status	Availability																																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																																								
Sleep In or Booster Off	Yes																																								
Default	D[7:0] = 0x08h																																								

6.2.10 Read display MADCTL (0Bh)

0BH	RDDMADCTL (Read Display MADCTL)																													
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																	
Command	0	1	↑	-	0	0	0	0	1	0	1	1	0B																	
1 st parameter	1	↑	1	-	D7	D6	D5	D4	D3	D2	D1	D0	xx																	
This command indicates the current status of the display as described in the table below:																														
Description	Bit	Description								Comment																				
	D7	Page Address Order								-																				
	D6	Column Address Order								-																				
	D5	Page/Column Order								-																				
	D4	Line Address Order								-																				
	D3	RGB/BGR Order								-																				
	D2	Display Data Latch Order								-																				
	D1	Source scan sequence								-																				
	D0	Gate csan sequence								-																				
	Bit D7 – Page Address Order ‘0’ = Top to Bottom (When MADCTL B7=’0’). ‘1’ = Bottom to Top (When MADCTL B7=’1’).																													
	Bit D6 – Column Address Order ‘0’ = Left to Right (When MADCTL B6=’0’). ‘1’ = Right to Left (When MADCTL B6=’1’).																													
	Bit D5 – Page/Column Order ‘0’ = Normal (When MADCTL B5=’0’). ‘1’ = Roration (When MADCTL B5=’1’).																													
	Note: For Bits D7 to D5, also refer to Section 5.3 MCU to memory write/read direction.																													
	Bit D4 – Line Address Order ‘0’ = LCD Refresh Top to Bottom (When MADCTL B4=’0’). ‘1’ = LCD Refresh Bottom to Top (When MADCTL B4=’1’).																													
	Bit D3 – RGB/BGR Order ‘0’ = RGB (When MADCTL B3=’0’). ‘1’ = BGR (When MADCTL B3=’1’).																													
	Note: For Bits D4 and D3 also refer to Section 6.2.31 Set_address_mode (36h).																													
	Bit D2 – Display Data Latch Data Order ‘0’ = LCD Refresh Left to Right (When MADCTL B2=’0’). ‘1’ = LCD Refresh Right to Left (When MADCTL B2=’1’).																													
	Bit D1 – Source scan sequence ‘0’ = Source output Left to Right (When MADCTL B1=’0’). ‘1’ = Source output Right to Left (When MADCTL B1=’1’).																													
	Bit D0 – Gate scan sequence ‘0’ = Gate output Top to Bottom (When MADCTL B0=’0’).																													
Restrictions	-																													
Register Availability	Status		Availability																											
	Normal Mode On, Idle Mode Off, Sleep Out		Yes																											
	Normal Mode On, Idle Mode On, Sleep Out		Yes																											
	Partial Mode On, Idle Mode Off, Sleep Out		Yes																											
	Partial Mode On, Idle Mode On, Sleep Out		Yes																											
Sleep In or Booster Off		Yes																												
Default	D[7:0] = 0x00h																													



6.2.11 Get_pixel_format (0Ch)

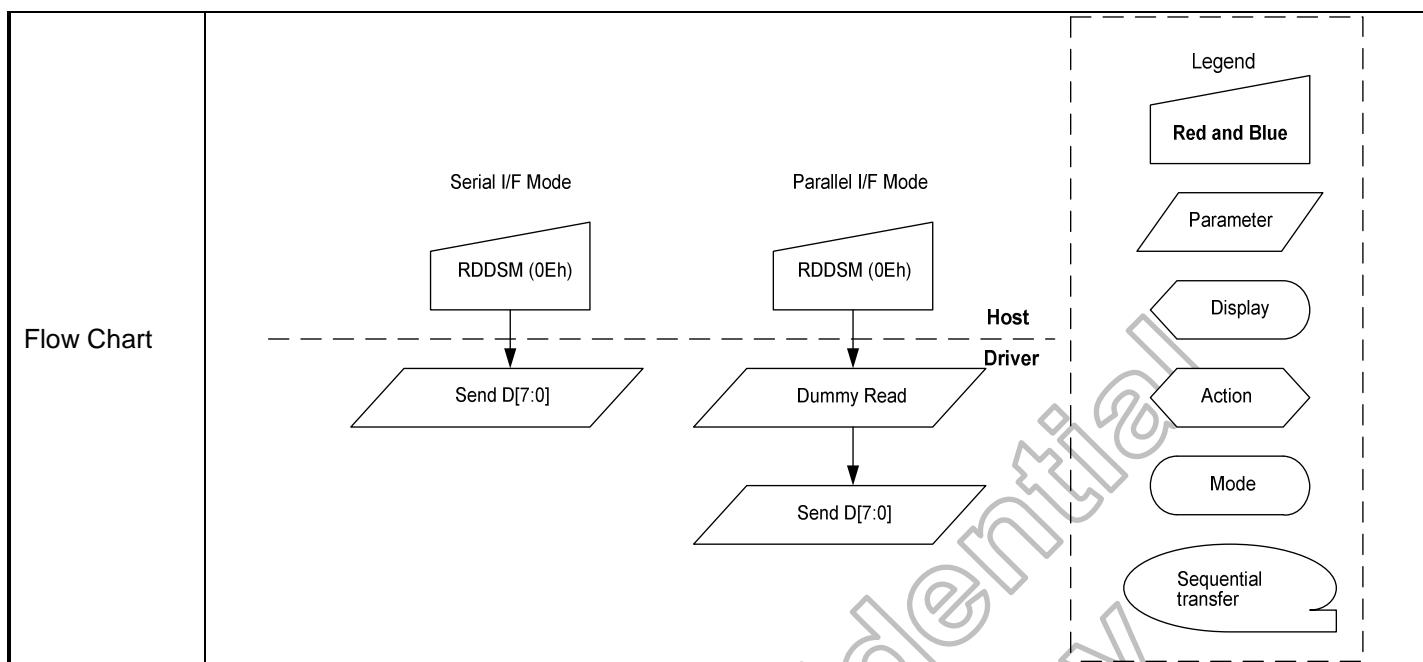
0CH	RDDCOLMOD (Read Display COLMOD)																																		
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																						
Command	0	1	↑	-	0	0	0	0	1	1	0	0	0C																						
1 st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read																						
2 nd parameter	1	↑	1	-	-	D6	D5	D4	-	D2	D1	D0	xx																						
Description	This command indicates the current status of the display as described in the table below: <table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Comment</th> </tr> </thead> <tbody> <tr> <td>D7</td> <td>Reserved</td> <td>Set to '0'</td> </tr> <tr> <td>D6</td> <td rowspan="4">DPI Interface Pixel format</td> <td>-</td> </tr> <tr> <td>D5</td> <td>-</td> </tr> <tr> <td>D4</td> <td>-</td> </tr> <tr> <td>D3</td> <td>Set to '0'</td> </tr> <tr> <td>D2</td> <td rowspan="3">Reserved</td> <td>Set to '0'</td> </tr> <tr> <td>D1</td> <td>Set to '0'</td> </tr> <tr> <td>D0</td> <td>Set to '0'</td> </tr> </tbody> </table> Bits D6, D5, D4 – DPI Interface Colour Pixel Format Definition For Setting pixel format, see section 6.2.30 Set_pixel_format (3Ah)".													Bit	Description	Comment	D7	Reserved	Set to '0'	D6	DPI Interface Pixel format	-	D5	-	D4	-	D3	Set to '0'	D2	Reserved	Set to '0'	D1	Set to '0'	D0	Set to '0'
Bit	Description	Comment																																	
D7	Reserved	Set to '0'																																	
D6	DPI Interface Pixel format	-																																	
D5		-																																	
D4		-																																	
D3		Set to '0'																																	
D2	Reserved	Set to '0'																																	
D1		Set to '0'																																	
D0		Set to '0'																																	
Restrictions	-																																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes										
Status	Availability																																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																																		
Partial Mode On, Idle Mode Off, Sleep Out	Yes																																		
Partial Mode On, Idle Mode On, Sleep Out	Yes																																		
Sleep In or Booster Off	Yes																																		
Default	D[7:0] = 0x07h																																		
Flow Chart	 <pre> graph TD Start((RDDCOLMOD (0Ch))) --> Send1[/Send D[7:0]/] Start --> Send2[/Send D[7:0]/] Send1 --> HostDriver[Host Driver] HostDriver --> Parallel[/Parallel I/F Mode/] HostDriver --> Serial[/Serial I/F Mode/] Parallel --> DummyRead[/Dummy Read/] Parallel --> Send2 Serial --> Send2 </pre> <p>Legend:</p> <ul style="list-style-type: none"> Red and Blue Parameter Display Action Mode Sequential transfer 																																		

6.2.12 Get_display_mode (0Dh)

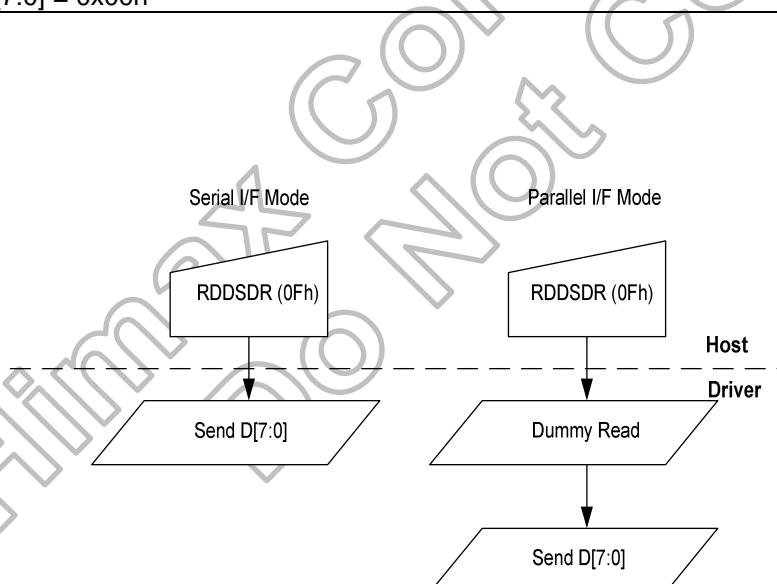
0DH	RDDIM (Read Display Image Mode)																																																								
	D/CX	RDX	WRX	D15-D8		D7	D6	D5	D4	D3	D2	D1	D0	HEX																																											
Command	0	1	↑	-		0	0	0	0	1	1	0	1	0D																																											
1 st parameter	1	↑	1	-		x	x	x	x	x	x	x	x	Dummy read																																											
2 nd parameter	1	↑	1	-		D7	D6	D5	D4	D3	D2	D1	D0	xx																																											
Description	This command indicates the current status of the display as described in the table below:																																																								
	Bit D5 – Inversion On/Off ‘0’ = Inversion is Off. ‘1’ = Inversion is On.																																																								
	Bit D4 – All Pixels On ‘0’ = Normal Display ‘1’ = White Display																																																								
	Bit D3 – All Pixels Off ‘0’ = Normal Display ‘1’ = Black Display																																																								
	Bits D2, D1, D0 – Gamma Curve Selection																																																								
	<table border="1"> <thead> <tr> <th>Gamma Curve Selected</th> <th>D2</th> <th>D1</th> <th>D0</th> <th>Gamma Set (26h) Parameter</th> </tr> </thead> <tbody> <tr> <td>Gamma Curve 1</td> <td>0</td> <td>0</td> <td>0</td> <td>GC0</td> </tr> <tr> <td>Gamma Curve 2</td> <td>0</td> <td>0</td> <td>1</td> <td>GC1</td> </tr> <tr> <td>Gamma Curve 3</td> <td>0</td> <td>1</td> <td>0</td> <td>GC2</td> </tr> <tr> <td>Gamma Curve 4</td> <td>0</td> <td>1</td> <td>1</td> <td>GC3</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>0</td> <td>0</td> <td>Not Defined</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>0</td> <td>1</td> <td>Not Defined</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>1</td> <td>0</td> <td>Not Defined</td> </tr> <tr> <td>Not Defined</td> <td>1</td> <td>1</td> <td>1</td> <td>Not Defined</td> </tr> </tbody> </table>													Gamma Curve Selected	D2	D1	D0	Gamma Set (26h) Parameter	Gamma Curve 1	0	0	0	GC0	Gamma Curve 2	0	0	1	GC1	Gamma Curve 3	0	1	0	GC2	Gamma Curve 4	0	1	1	GC3	Not Defined	1	0	0	Not Defined	Not Defined	1	0	1	Not Defined	Not Defined	1	1	0	Not Defined	Not Defined	1	1	1
Gamma Curve Selected	D2	D1	D0	Gamma Set (26h) Parameter																																																					
Gamma Curve 1	0	0	0	GC0																																																					
Gamma Curve 2	0	0	1	GC1																																																					
Gamma Curve 3	0	1	0	GC2																																																					
Gamma Curve 4	0	1	1	GC3																																																					
Not Defined	1	0	0	Not Defined																																																					
Not Defined	1	0	1	Not Defined																																																					
Not Defined	1	1	0	Not Defined																																																					
Not Defined	1	1	1	Not Defined																																																					
Restrictions																																																									
<table border="1"> <thead> <tr> <th></th> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td></td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td></td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td></td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td></td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td></td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out		Yes	Normal Mode On, Idle Mode On, Sleep Out		Yes	Partial Mode On, Idle Mode Off, Sleep Out		Yes	Partial Mode On, Idle Mode On, Sleep Out		Yes	Sleep In or Booster Off		Yes																											
	Status	Availability																																																							
Normal Mode On, Idle Mode Off, Sleep Out		Yes																																																							
Normal Mode On, Idle Mode On, Sleep Out		Yes																																																							
Partial Mode On, Idle Mode Off, Sleep Out		Yes																																																							
Partial Mode On, Idle Mode On, Sleep Out		Yes																																																							
Sleep In or Booster Off		Yes																																																							
Default																																																									
<pre> graph TD RDDIM[RDDIM (0Dh)] --> Serial SendD1[/Send D[7:0]/] RDDIM --> Parallel SendD2[/Send D[7:0]/] subgraph HostDriver [Host Driver] direction TB RD[Red and Blue] --- P[Parameter] RD --- D[Display] RD --- A[Action] RD --- M[Mode] RD --- ST[Sequential transfer] P --- D D --- A A --- M M --- ST end </pre>																																																									

6.2.13 Get_signal_mode (0Eh)

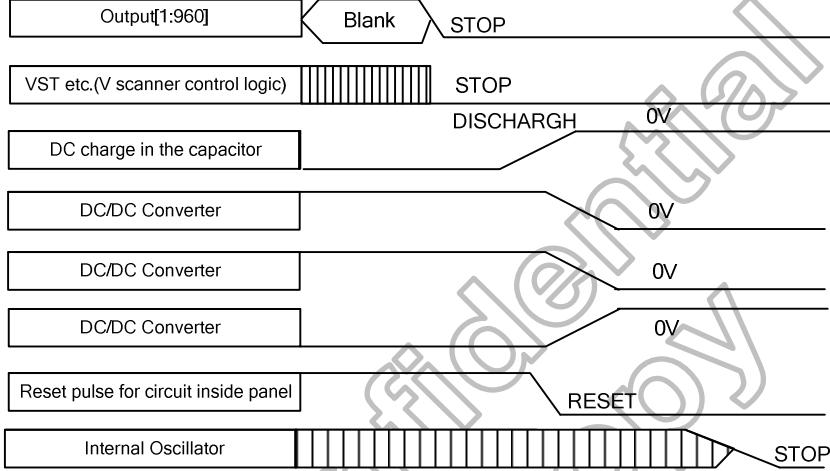
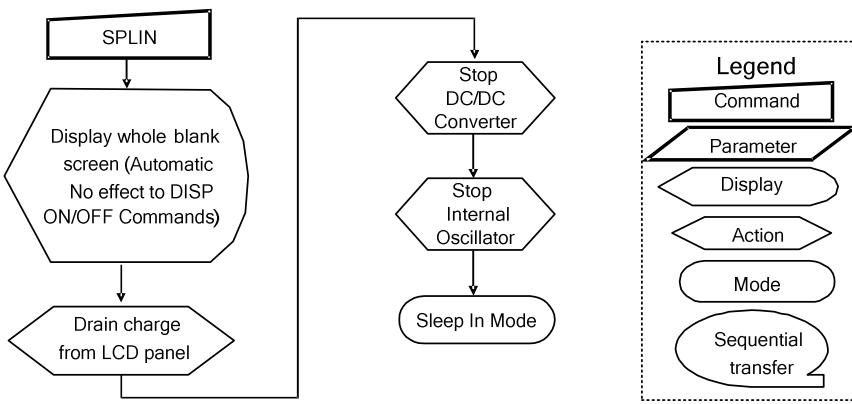
0EH	RDDSM (Read Display Signal Mode)																								
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	-	0	0	0	0	1	1	1	0	0E												
1 st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read												
2 nd parameter	1	↑	1	-	D7	D6	D5	D4	D3	D2	D1	D0	xx												
Description	T This command indicates the current status of the display as described in the table below: Bit D7 – Tearing Effect Line On/Off '0' = Tearing Effect Line Off. '1' = Tearing Effect On. Bit D6 – Tearing Effect Line Output Mode, see section 5.5.3 for mode definitions. '0' = Mode 1. '1' = Mode 2. Bit D5 – Horizontal Sync. (RGB I/F) On/Off. '0' = Horizontal Sync. Line is Off ("Low"). '1' = Horizontal Sync. Line is On ("High"). Bit D4 – Vertical Sync. (RGB I/F) On/Off. '0' = Vertical Sync. Line is Off ("Low"). '1' = Vertical Sync. Line is On ("High"). Bit D3 – Pixel Clock (PCLK, RGB I/F) On/Off. '0' = PCLK line is Off ("Low"). '1' = PCLK line is On ("High"). Bit D2 – Data Enable (DE, RGB I/F) On/Off. '0' = DE line is Off ("Low"). '1' = DE line is On ("High"). Bit D0 – Parity Error on DSI, see "Read number of the parity errors (05h)". '0'=No Parity Error. '1'=Parity Error. D1 is for future use and are set to '0'.																								
Restrictions	-																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	D[7:0] = 0x00h																								



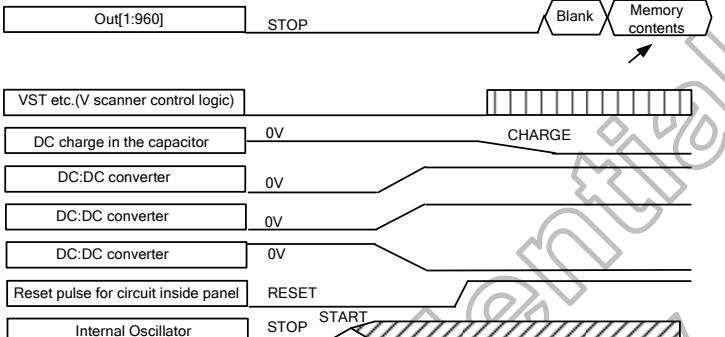
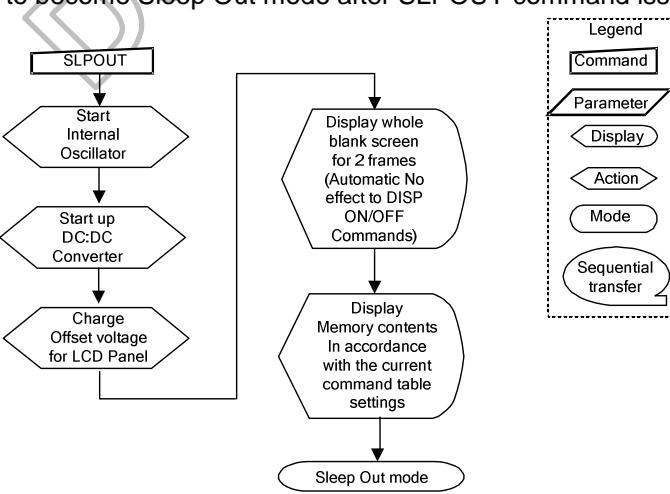
6.2.14 Get_diagnostic_result (0Fh)

0FH	RDDSDR (Read Display Self-Diagnostic Result)																								
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	-	0	0	0	0	1	1	1	1	0F												
1 st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read												
2 nd parameter	1	1	1	-	D7	D6	D5	D4	0	0	0	0	xx												
Description	The display module returns the self-diagnostic results following a Sleep Out command. See section 5.15 for a description of the status results. Bit D7 – Register Loading Detection Bit D6 – Functionality Detection Bit D5 – Chip Attachment Detection Set to '0' if feature unimplemented. Bit D4 – Display Glass Break Detection Set to '0' if feature unimplemented. Bits D[3:0] – Reserved Set to '0'.																								
Restrictions	-																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	D[7:0] = 0x00h																								
Flow Chart	 <pre> graph TD subgraph Host [Host] RDDSDR[RDDSDR (0Fh)] --> Send1[/Send D[7:0]/] Send1 --> DummyRead[/Dummy Read/] DummyRead --> Send2[/Send D[7:0]/] end subgraph Driver [Driver] RDDSDR Send1 DummyRead Send2 end RDDSDR --> Send1 RDDSDR --> DummyRead RDDSDR --> Send2 </pre> <p>Legend:</p> <ul style="list-style-type: none"> Red and Blue: Command Parameter: Parameter Display: Display Action: Action Mode: Mode Sequential transfer: Sequential transfer 																								

6.2.15 Enter_sleep_mode (10h)

10H		SLPIN (Sleep In)																								
		D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command		0	1	↑	-	0	0	0	1	0	0	0	0	10												
Parameter	NO PARAMETER																									
Description	<p>This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.</p>  <p>MCU interface and memory are still working and the memory keeps its contents.</p>																									
Restriction	<p>This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command (11h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.</p>																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes	
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																									
Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In or Booster Off	Yes																									
Default	N/A																									
Flow Chart																										

6.2.16 Exit_sleep_omde (11h)

11H		SLPOUT (Sleep Out)																							
Command	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Parameter	0	1	↑	-	0	0	0	1	0	0	0	1	11												
Description	<p>This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.</p> 																								
Restriction	<p>This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode.</p> <p>The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.</p>																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	N/A																								
Flow Chart	<p>It takes 120msec to become Sleep Out mode after SLPOUT command issued.</p> 																								

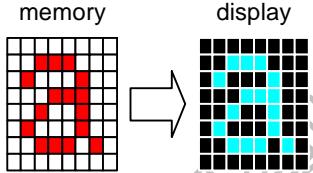
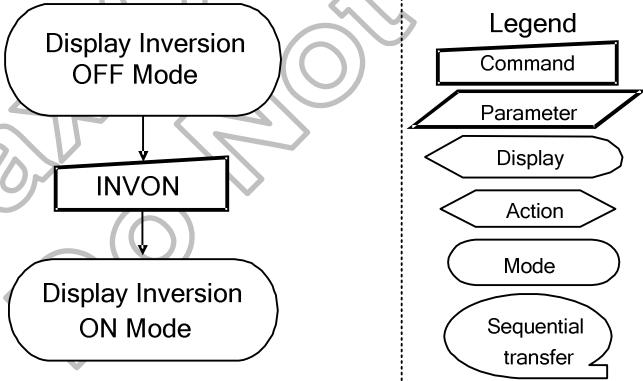
6.2.17 Enter_normal_mode (13h)

13H	NORON (Normal Display Mode On)																		
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX						
Command	0	1	↑	-	0	0	0	1	0	0	1	1	13						
Parameter	NO PARAMETER																		
Description	This command returns the display to normal mode. Normal display mode is means Partial mode off, Scroll mode Off.																		
Restriction	This command has no effect when Normal Display mode is active.																		
Register Availability	Status							Availability											
	Normal Mode On, Idle Mode Off, Sleep Out							Yes											
	Normal Mode On, Idle Mode On, Sleep Out							Yes											
	Partial Mode On, Idle Mode Off, Sleep Out							Yes											
	Partial Mode On, Idle Mode On, Sleep Out							Yes											
	Sleep In or Booster Off							Yes											
Default	N/A																		
Flow Chart	See Partial Area and Vertical Scrolling Definition Descriptions for details of when to use this command.																		

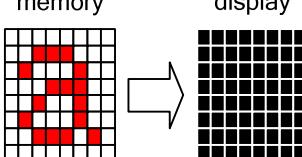
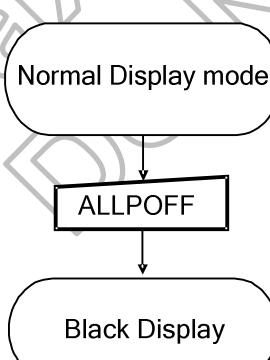
6.2.18 Exit_inversion_mode (20h)

20H	INVOFF (Display Inversion Off)																								
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	-	0	0	1	0	0	0	0	0	20												
Parameter	No parameter																								
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. (Example)																								
Restriction	This command has no effect when module is already in inversion off mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	N/A																								
Flow Chart	<p>The flowchart illustrates the sequence of operations for the INVOFF command. It begins with the state 'Display Inversion On Mode', followed by the execution of the command itself ('INVOFF'), which results in the final state 'Display Inversion OFF Mode'. The legend on the right defines the symbols used in the flowchart: a rectangle for 'Command', a rectangle for 'Parameter', an arrow pointing right for 'Display', an arrow pointing left for 'Action', a rectangle for 'Mode', and an oval for 'Sequential transfer'.</p>																								

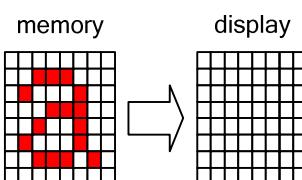
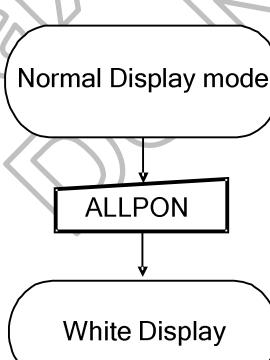
6.2.19 Enter_inversion_mode (21h)

21H	INVON (Display Inversion On)																									
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	-	0	0	1	0	0	0	0	1	21													
Parameter	NO PARAMETER																									
Description	<p>This command is used to enter into display inversion mode. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status.</p> <p style="text-align: center;">(Example)</p> 																									
Restriction	This command has no effect when module is already in inversion on mode.																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																									
Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In or Booster Off	Yes																									
Default	N/A																									
Flow Chart	 <pre> graph TD A([Display Inversion OFF Mode]) --> B[INVON] B --> C([Display Inversion ON Mode]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																									

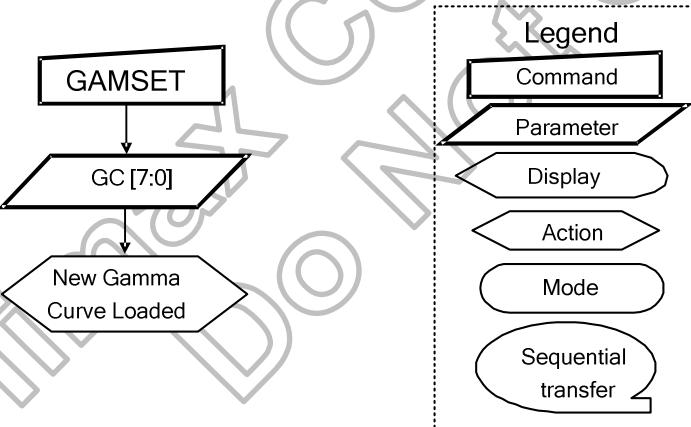
6.2.20 All_Pixel_Off (22h)

22H	ALLPOFF (All Pixel Off)																									
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	-	0	0	1	0	0	0	1	0	22													
Parameter	NO PARAMETER																									
Description	<p>This command turns the display panel black in 'Sleep Out' –mode and a status of the 'Display On/Off' –register can be 'on' or 'off'. This command makes no change of contents of frame memory. This command does not change any other status (Example)</p> <p style="text-align: center;">memory display</p>  <p>'All Pixels On', 'Normal Display Mode On' or 'Partial Mode On' – commands are used to leave this mode. The display panel is showing the content of the frame memory after 'Normal Display Mode On' and 'Partial Mode On' -commands.</p>																									
Restriction	This command has no effect when module is already in inversion on mode.																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																									
Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In or Booster Off	Yes																									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Off</td> </tr> <tr> <td>S/W Reset</td> <td>Off</td> </tr> <tr> <td>H/W Reset</td> <td>Off</td> </tr> </tbody> </table>														Status	Default Value	Power On Sequence	Off	S/W Reset	Off	H/W Reset	Off				
Status	Default Value																									
Power On Sequence	Off																									
S/W Reset	Off																									
H/W Reset	Off																									
Flow Chart	 <pre> graph TD A([Normal Display mode]) --> B[ALLPOFF] B --> C([Black Display]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																									

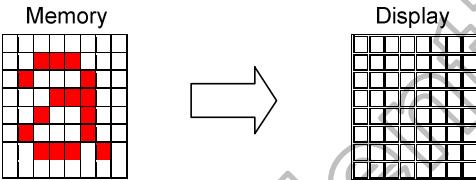
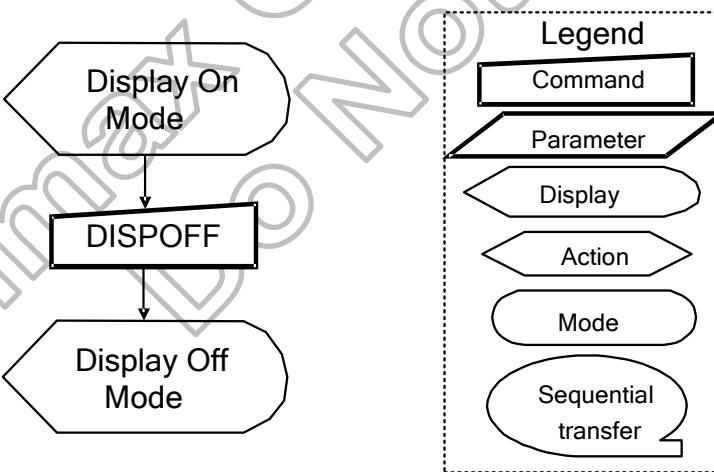
6.2.21 All_Pixel_On (23h)

23H	ALLPON(All Pixel On)																									
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	-	0	0	1	0	0	0	1	1	23													
Parameter	NO PARAMETER																									
Description	<p>This command turns the display panel white in 'Sleep out' –mode and a status of the 'Display On/Off' –register can be 'on' or 'off'. This command makes no change of contents of frame memory. This command does not change any other status.</p> <p>(Example)</p>  <p>'All Pixels Off', 'Normal Display Mode On' or 'Partial Mode On' – commands are used to leave this mode. The display is showing the content of the frame memory after 'Normal Display Mode On' and 'Partial Mode On' –commands.</p>																									
Restriction	This command has no effect when module is already in inversion on mode.																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																									
Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In or Booster Off	Yes																									
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default Value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>Off</td> </tr> <tr> <td>S/W Reset</td> <td>Off</td> </tr> <tr> <td>H/W Reset</td> <td>Off</td> </tr> </tbody> </table>														Status	Default Value	Power On Sequence	Off	S/W Reset	Off	H/W Reset	Off				
Status	Default Value																									
Power On Sequence	Off																									
S/W Reset	Off																									
H/W Reset	Off																									
Flow Chart	 <pre> graph TD A([Normal Display mode]) --> B[ALLPON] B --> C([White Display]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																									

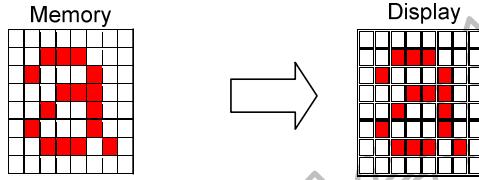
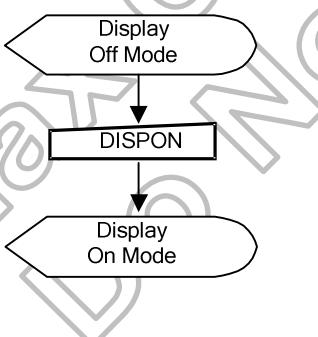
6.2.22 Set_gamma_curve (26h)

26H	GAMSET (Gamma Set)																									
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	-	0	0	1	0	0	1	1	0	26													
Parameter	1	1	↑	-	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0	1..08													
This command is used to select the desired Gamma curve for the current display. A maximum of 4 fixed gamma curves can be selected. The curves are defined in Curve Correction Power Supply Circuit. The curve is selected by setting the appropriate bit in the parameter as described in the Table:																										
Description	GC[7:0]	Parameter	Curve selected																							
	01h	GC0	Gamma Curve 1																							
	02h	GC1	Gamma Curve 2																							
	04h	GC2	Gamma Curve 3																							
	08h	GC3	Gamma Curve 4																							
	Note: All other values are undefined.																									
Restriction	Values of GC[7..0] not shown in table above are invalid and will not change the current selected Gamma curve until valid value is received.																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																									
Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In or Booster Off	Yes																									
Default	GC[7:0] = 0x01h																									
Flow Chart	 <pre> graph TD GAMSET[GAMSET] --> GC[7:0] GC[7:0] --> NewGamma[New Gamma Curve Loaded] </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																									

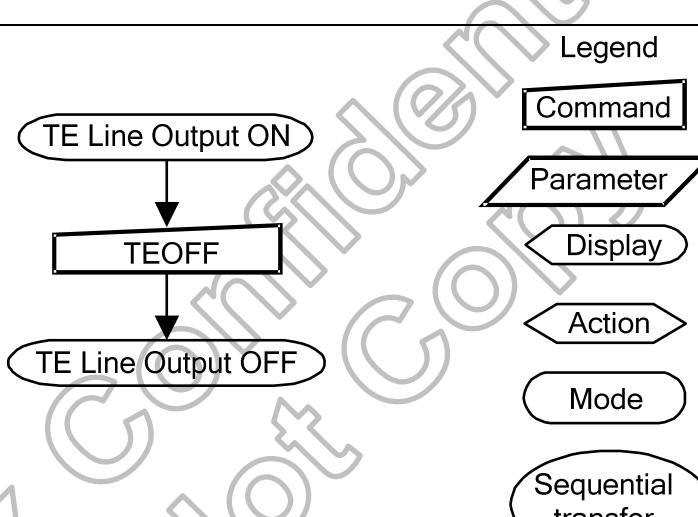
6.2.23 Set_display_off (28h)

28H	DISPOFF (Display Off)																								
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	-	0	0	1	0	1	0	0	0	28												
Parameter	NO PARAMETER																								
Description	<p>This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status.</p> <p>There will be no abnormal visible effect on the display.</p>																								
	Example 																								
Restriction	This command has no effect when module is already in display off mode.																								
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Partial Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In or Booster Off</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	N/A																								
Flow Chart	 <pre> graph TD A([Display On Mode]) --> B[DISPOFF] B --> C([Display Off Mode]) </pre>																								

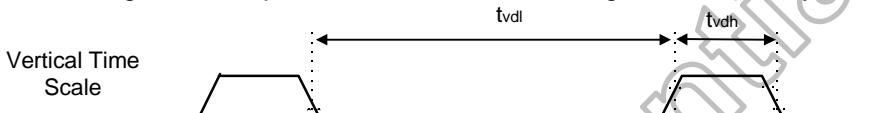
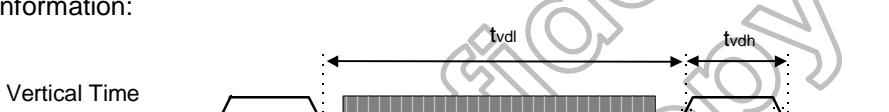
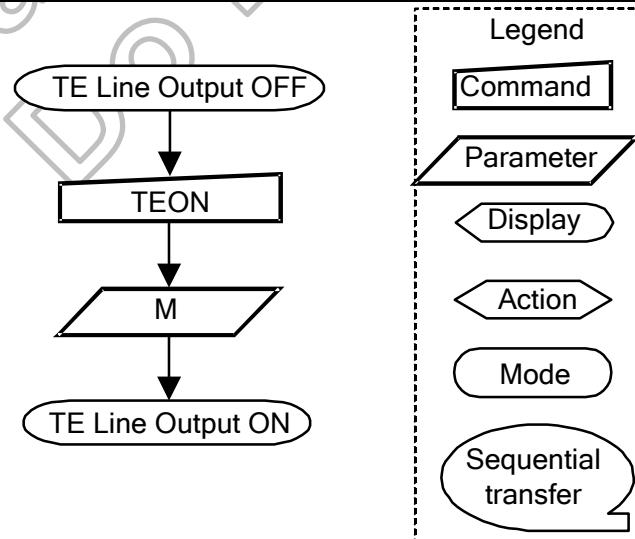
6.2.24 Set_display_on (29h)

29H	DISPON (Display On)																								
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	-	0	0	1	0	1	0	0	1	29												
Parameter	NO PARAMETER																								
Description	<p>This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled.</p> <p>This command makes no change of contents of frame memory.</p> <p>This command does not change any other status.</p> <p>(Example)</p> 																								
Restriction	This command has no effect when module is already in display on mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	N/A																								
Flow Chart	 <pre> graph TD A[Display Off Mode] --> B[DISPON] B --> C[Display On Mode] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

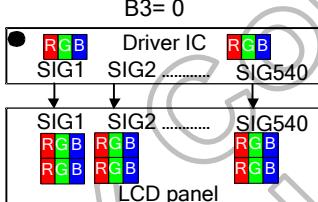
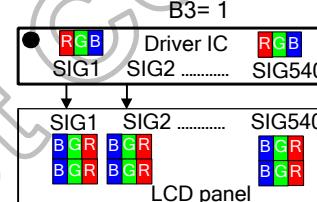
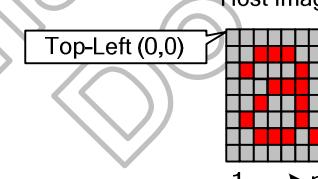
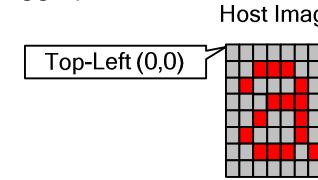
6.2.25 Tearing effect line off (34h)

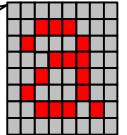
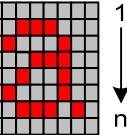
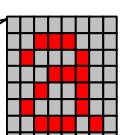
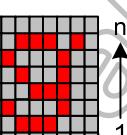
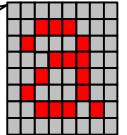
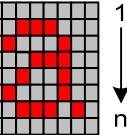
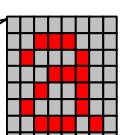
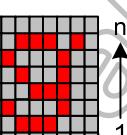
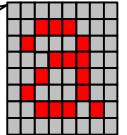
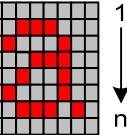
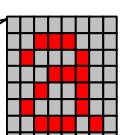
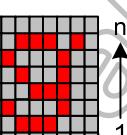
TEOFF (Tearing Effect Line OFF)																									
34H	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	-	0	0	1	1	0	1	0	0	34												
Parameter	NO PARAMETER																								
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.																								
Restriction	This command has no effect when Tearing Effect output is already OFF.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	OFF																								
Flow Chart	 <pre> graph TD A([TE Line Output ON]) --> B[TEOFF] B --> C([TE Line Output OFF]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

6.2.26 Set_tear_on (35h)

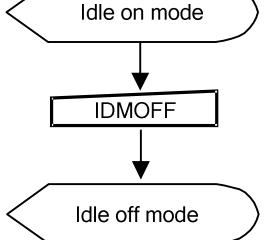
35H		TEON (Tearing Effect Line ON)																					
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX										
Command	0	1	↑	-	0	0	1	1	0	1	0	1	35										
Parameter	1	1	↑	-	X	X	X	X	X	X	X	M	xx										
Description	<p>This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit B4. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. (X=Don't Care).</p> <p>When M=0:</p> <p>The Tearing Effect Output line consists of V-Blanking information only:</p>  <p>When M=1:</p> <p>The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:</p>  <p>Note: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.</p>																						
Restriction	This command has no effect when Tearing Effect output is already ON.																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Default	OFF																						
Flow Chart	 <pre> graph TD A([TE Line Output OFF]) --> B[TEON] B --> C[M] C --> D([TE Line Output ON]) </pre> <p>Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																						

6.2.27 Set_address_mode (36h)

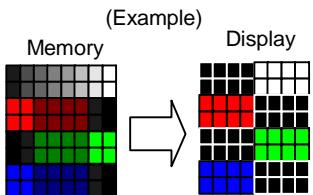
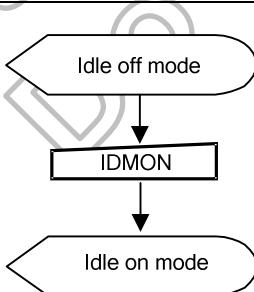
36H	MADCTL (Memory Access Control)																							
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX											
Command	0	1	↑	-	0	0	1	1	0	1	1	0	36											
1 st parameter	1	1	↑	-	B7	B6	B5	B4	B3	B2	B1	B0	XX											
This command defines read/write scanning direction of frame memory. This command makes no change on the other driver status.																								
Bit Assignment	BIT	NAME	DESCRIPTION																					
	B7	Not Defined	Set to "0".																					
	B6	Not Defined																						
	B5	Not Defined																						
	B4	Not Defined																						
	B3	RGB-BGR ORDER (BGR)	Colour selector switch control (0=RGB colour filter panel, 1=BGR colour filter panel)																					
	B2	Not Defined	Set to "0".																					
	B1	Flip Horizontal (SS)	Select the Source driver scan direction on panel module																					
	B0	Flip Vertical (GS)	Select the Gate driver scan direction on panel module																					
Description	RGB-BGR Order																							
	B3=0																							
																								
	B3=1																							
																								
	SS - Source scan sequence																							
	SS=0																							
																								
	SS=1																							
																								

	<p style="text-align: center;">GS - Gate scan sequence</p> <table border="0" style="width: 100%; text-align: center;"> <tr> <td style="width: 33%;">GS= 0</td><td>Host Image</td><td>Display Image</td></tr> <tr> <td></td><td> <div style="display: flex; align-items: center;"> Top-Left (0,0)  1 → m n </div> </td><td> <div style="display: flex; align-items: center;"> Top-Left (0,0)  1 → m n </div> </td></tr> <tr> <td style="width: 33%;">GS= 1</td><td>Host Image</td><td>Display Image</td></tr> <tr> <td></td><td> <div style="display: flex; align-items: center;"> Top-Left (0,0)  1 → m n </div> </td><td> <div style="display: flex; align-items: center;"> Top-Left (0,0)  n → 1 1 </div> </td></tr> </table>	GS= 0	Host Image	Display Image		<div style="display: flex; align-items: center;"> Top-Left (0,0)  1 → m n </div>	<div style="display: flex; align-items: center;"> Top-Left (0,0)  1 → m n </div>	GS= 1	Host Image	Display Image		<div style="display: flex; align-items: center;"> Top-Left (0,0)  1 → m n </div>	<div style="display: flex; align-items: center;"> Top-Left (0,0)  n → 1 1 </div>
GS= 0	Host Image	Display Image											
	<div style="display: flex; align-items: center;"> Top-Left (0,0)  1 → m n </div>	<div style="display: flex; align-items: center;"> Top-Left (0,0)  1 → m n </div>											
GS= 1	Host Image	Display Image											
	<div style="display: flex; align-items: center;"> Top-Left (0,0)  1 → m n </div>	<div style="display: flex; align-items: center;"> Top-Left (0,0)  n → 1 1 </div>											
Restriction	-												
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th><th style="text-align: center;">Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td style="text-align: center;">Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td style="text-align: center;">Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td><td style="text-align: center;">Yes</td></tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td><td style="text-align: center;">Yes</td></tr> <tr> <td>Sleep In or Booster Off</td><td style="text-align: center;">Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability												
Normal Mode On, Idle Mode Off, Sleep Out	Yes												
Normal Mode On, Idle Mode On, Sleep Out	Yes												
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Partial Mode On, Idle Mode On, Sleep Out	Yes												
Sleep In or Booster Off	Yes												
Default	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th><th style="text-align: center;">Default value</th></tr> </thead> <tbody> <tr> <td>Power On Sequence</td><td style="text-align: center;">B7=0,B6=0,B5=0,B4=0,B3=0,B2=0,B1=0,B0=0</td></tr> <tr> <td>S/W Reset</td><td style="text-align: center;">No Change</td></tr> </tbody> </table>	Status	Default value	Power On Sequence	B7=0,B6=0,B5=0,B4=0,B3=0,B2=0,B1=0,B0=0	S/W Reset	No Change						
Status	Default value												
Power On Sequence	B7=0,B6=0,B5=0,B4=0,B3=0,B2=0,B1=0,B0=0												
S/W Reset	No Change												
Flow Chart	<pre> graph TD MADCTL[MADCTL] --> B70[1st parameter B[7:0]] </pre> <p style="text-align: right;">Legend</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												

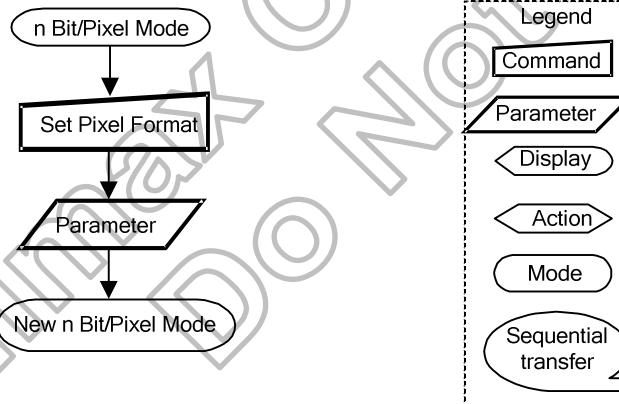
6.2.28 Idle mode off (38h)

38H	IDMOFF (Idle mode off)																								
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	-	0	0	1	1	1	0	0	0	38												
Parameter	NO PARAMETER																								
Description	This command is used to recover from Idle mode on. In the idle off mode, LCD can display maximum 16.7M colours.																								
Restriction	This command has no effect when module is already in idle off mode.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	Idle mode is OFF.																								
Flow Chart	 <pre> graph TD A([Idle on mode]) --> B[IDMOFF] B --> C([Idle off mode]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

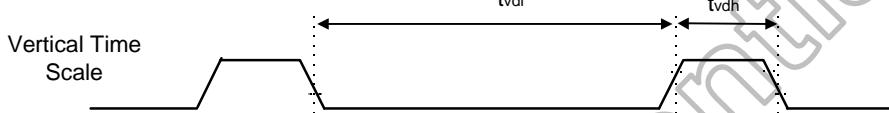
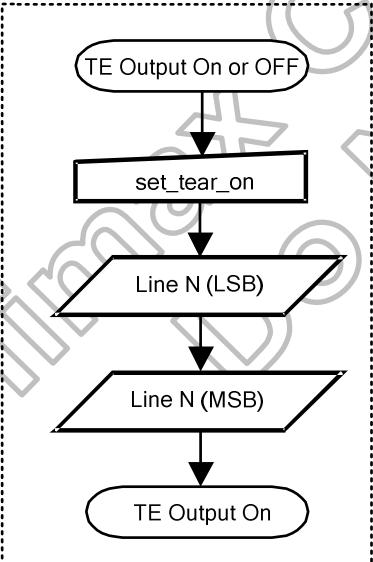
6.2.29 Enter_Idle_mode (39h)

39H	IDMON (Idle mode on)																																																	
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																					
Command	0	1	↑	-	0	0	1	1	1	0	0	1	39																																					
Parameter	NO PARAMETER																																																	
Description	<p>This command is used to enter into Idle mode on. In the idle on mode, colour expression is reduced. The primary and the secondary colours using MSB of each R, G and B in the Frame Memory, 8 colour depth data is displayed.</p> <p>(Example)</p> 																																																	
Display Colour	<table border="1"> <thead> <tr> <th></th> <th>R7 - R0</th> <th>G7 - G0</th> <th>B7 - B0</th> </tr> </thead> <tbody> <tr> <td>Black</td> <td>0x00h</td> <td>0x00h</td> <td>0x00h</td> </tr> <tr> <td>Blue</td> <td>0x00h</td> <td>0x00h</td> <td>0xFFh</td> </tr> <tr> <td>Red</td> <td>0xFFh</td> <td>0x00h</td> <td>0x00h</td> </tr> <tr> <td>Magenta</td> <td>0xFFh</td> <td>0x00h</td> <td>0xFFh</td> </tr> <tr> <td>Green</td> <td>0x00h</td> <td>0xFFh</td> <td>0x00h</td> </tr> <tr> <td>Cyan</td> <td>0x00h</td> <td>0xFFh</td> <td>0xFFh</td> </tr> <tr> <td>Yellow</td> <td>0xFFh</td> <td>0xFFh</td> <td>0x00h</td> </tr> <tr> <td>White</td> <td>0xFFh</td> <td>0xFFh</td> <td>0xFFh</td> </tr> </tbody> </table>															R7 - R0	G7 - G0	B7 - B0	Black	0x00h	0x00h	0x00h	Blue	0x00h	0x00h	0xFFh	Red	0xFFh	0x00h	0x00h	Magenta	0xFFh	0x00h	0xFFh	Green	0x00h	0xFFh	0x00h	Cyan	0x00h	0xFFh	0xFFh	Yellow	0xFFh	0xFFh	0x00h	White	0xFFh	0xFFh	0xFFh
	R7 - R0	G7 - G0	B7 - B0																																															
Black	0x00h	0x00h	0x00h																																															
Blue	0x00h	0x00h	0xFFh																																															
Red	0xFFh	0x00h	0x00h																																															
Magenta	0xFFh	0x00h	0xFFh																																															
Green	0x00h	0xFFh	0x00h																																															
Cyan	0x00h	0xFFh	0xFFh																																															
Yellow	0xFFh	0xFFh	0x00h																																															
White	0xFFh	0xFFh	0xFFh																																															
Restriction	This command has no effect when module is already in idle on mode.																																																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes																								
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Sleep In or Booster Off	Yes																																																	
Default	Idle mode is OFF.																																																	
Flow Chart	 <pre> graph TD A[Idle off mode] --> B[IDMON] B --> C[Idle on mode] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																																																	

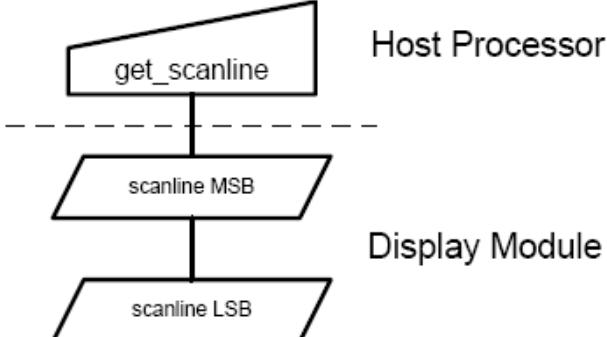
6.2.30 Set_pixel_format (3Ah)

3A H	COLMOD (Interface Pixel Format)																																
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																				
Command	0	1	↑	-	0	0	1	1	1	0	1	0	3A																				
1 st parameter	1	1	↑	-	X	D6	D5	D4	X	X	X	X	XX																				
This command is used to define the format of RGB picture data. D6~D4 : DPI Pixel format Definition. The formats are shown in the table:																																	
Description	<table border="1"> <thead> <tr> <th>Pixel Format</th> <th>D6</th> <th>D5</th> <th>D4</th> </tr> </thead> <tbody> <tr> <td>Not Defined</td> <td colspan="3">Others</td></tr> <tr> <td>16 Bit/Pixel</td> <td>1</td> <td>0</td> <td>1</td></tr> <tr> <td>18 Bit/Pixel</td> <td>1</td> <td>1</td> <td>0</td></tr> <tr> <td>24 Bit/Pixel</td> <td>1</td> <td>1</td> <td>1</td></tr> </tbody> </table> <p>If a particular interface is not used then the correspondind bits in the parameter returned from the display module undefined.</p>													Pixel Format	D6	D5	D4	Not Defined	Others			16 Bit/Pixel	1	0	1	18 Bit/Pixel	1	1	0	24 Bit/Pixel	1	1	1
Pixel Format	D6	D5	D4																														
Not Defined	Others																																
16 Bit/Pixel	1	0	1																														
18 Bit/Pixel	1	1	0																														
24 Bit/Pixel	1	1	1																														
Restriction	There is no visible effect until the Frame Memory is written to.																																
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes								
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Partial Mode On, Idle Mode On, Sleep Out	Yes																																
Sleep In or Booster Off	Yes																																
Default	<table border="1"> <thead> <tr> <th>Status</th> <th>Default value</th> </tr> </thead> <tbody> <tr> <td>Power On Sequence</td> <td>24 Bit/Pixel</td> </tr> <tr> <td>S/W Reset</td> <td>NO Change</td> </tr> </tbody> </table>													Status	Default value	Power On Sequence	24 Bit/Pixel	S/W Reset	NO Change														
Status	Default value																																
Power On Sequence	24 Bit/Pixel																																
S/W Reset	NO Change																																
Flow Chart	 <pre> graph TD A([n Bit/Pixel Mode]) --> B[Set Pixel Format] B --> C[/Parameter/] C --> D([New n Bit/Pixel Mode]) </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																																

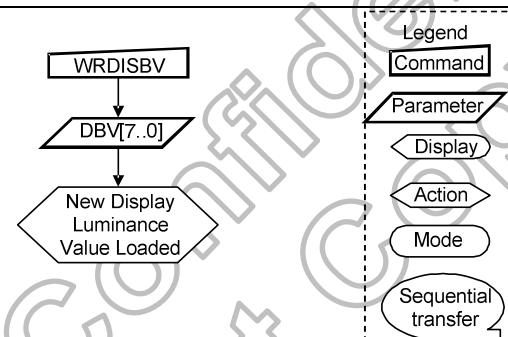
6.2.31 Set tear scan lines (44h)

44H	TESL (Tear Effect Scan Lines)																								
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	-	0	1	0	0	0	1	0	0	44												
1 st parameter	1	1	↑	-	TELIN[15:8](8'b0)								00..FF												
2 nd parameter	1	1	↑	-	TELIN[7:0](8'b0)								00..FF												
Description	<p>This command turns on the display module's Tearing Effect output signal on the TE signal Line when the display module reaches line TELIN. The TE signal is not affected by changing MADCTL bit B4.</p> <p>The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.</p> <p>The Tearing Effect Output line consists of V-Blanking information only:</p>  <p>Note: That TELIN=0 is equivalent to TEMODE=0. The Tearing Effect Output Line shall be active low when the display module is in Sleep mode.</p>																								
Restriction	The command has no effect when Tearing Effect output is already ON.																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	TELIN[15:0]=0x0000h																								
Flow Chart	 <pre> graph TD A([TE Output On or OFF]) --> B[set_tear_on] B --> C[/Line N (LSB)/] C --> D[/Line N (MSB)/] D --> E([TE Output On]) </pre>																								

6.2.32 Get the current scanline(45h)

45H	GETSCAN (Get the current scanline)																						
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX										
Command	0	1	↑	-	0	1	0	0	0	1	0	1	45										
1 st parameter	1	1	↑	-									00..FF										
2 nd parameter	1	1	↑	-									00..FF										
Description	The display module returns the current scanline, N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC + VBP + VACT + VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0. When in Sleep Mode, the value returned by get_scanline is undefined.																						
Restriction	-																						
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes
Status	Availability																						
Normal Mode On, Idle Mode Off, Sleep Out	Yes																						
Normal Mode On, Idle Mode On, Sleep Out	Yes																						
Partial Mode On, Idle Mode Off, Sleep Out	Yes																						
Partial Mode On, Idle Mode On, Sleep Out	Yes																						
Default	SLN[15:0]= 0x0000h																						
Flow Chart	 <pre> graph TD Host[Host Processor] -- "get_scanline" --> DM[Display Module] DM -- "scanline MSB" --> LS[scanline LSB] </pre>																						

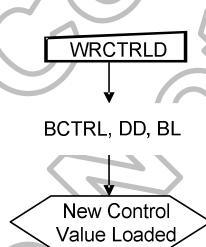
6.2.33 Write display brightness (51h)

51H	WRDISBV (Write Display Brightness)																		
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX						
Command	0	1	↑	-	0	1	0	1	0	0	0	1	51						
1 st parameter	1	1	↑	-									00 .. FF						
Description	This command is used to adjust the brightness value of the display. It should be checked what the relationship between this written value and output brightness of the display is. This relationship is defined on the display module specification. In principle relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapter "5.17.3 Brightness Control Block".																		
Restriction	-																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Sleep Out	Yes																		
Sleep In	Yes																		
Default	DBV[7:0]= 0x00h																		
Flow Chart	 <pre> graph TD A[WRDISBV] --> B{DBV[7..0]} B --> C[New Display Luminance Value Loaded] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																		

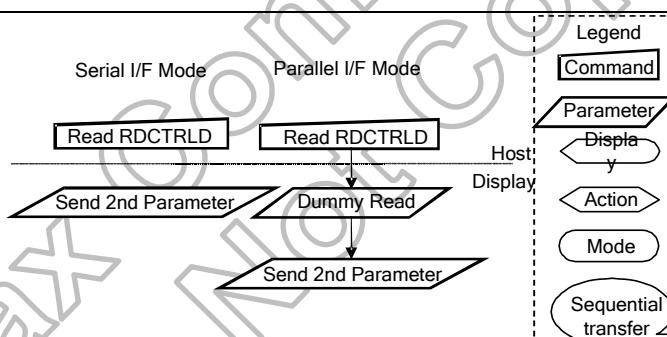
6.2.34 Read display brightness value (52h)

52H	RDDISBV (Read Display Brightness Value)																				
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	↑	-	0	1	0	1	0	0	1	0	52								
1 st parameter	1	↑	1	-	xx	xx	xx	xx	xx	xx	xx	xx	Dummy read								
2 nd parameter	1	↑	1	-	DBV[7:0]								xx								
Description	<p>This command returns the brightness value of the display. It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification is. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapters: "5.17.3 Brightness Control Block", and "6.2.43 Write Display Brightness (51h)" DBV[7:0] is reset when display is in sleep-in mode. DBV[7:0] is '0' when bit BCTRL of "6.2.45 Write CTRL Display (53h)" command is '0'. DBV[7:0] is manual set brightness specified with "6.2.45 Write CTRL Display (53h)" command when bit BCTRL is '1'. When bit BCTRL of "6.2.45 Write CTRL Display (53h)" command is '1' and bit C1/C0 of "6.2.47 Write Content Adaptive Brightness Control (55h)" are '0', DBV[7:0] output is the brightness value specified with "6.2.43 Write Display Brightness (51h)" command.</p>																				
Restriction	-																				
Register Availability	<table border="1"> <tr> <td>Status</td> <td>Availability</td> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </table>													Status	Availability	Sleep Out	Yes	Sleep In	Yes		
Status	Availability																				
Sleep Out	Yes																				
Sleep In	Yes																				
Default	DBV[7:0]= 0x00h																				
Flow Chart	<pre> graph TD Start(()) --> SIF[Serial I/F Mode] Start --> PIF[Parallel I/F Mode] SIF --> ReadS[Read RDDISBV] PIF --> ReadP[Read RDDISBV] ReadS --> SendS[Send 2nd Parameter] ReadP --> SendP[Send 2nd Parameter] SendS --> DummyP[Parallel I/F Mode] SendP --> DummyS[Serial I/F Mode] DummyP --> SendP Legend[Legend] Legend --- Command Legend --- Parameter Legend --- Display Legend --- Action Legend --- Mode Legend --- Sequential transfer </pre>																				

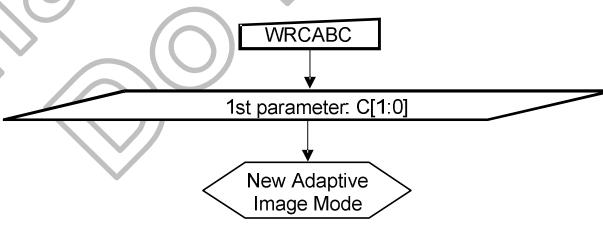
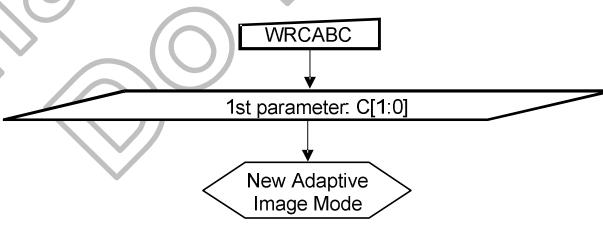
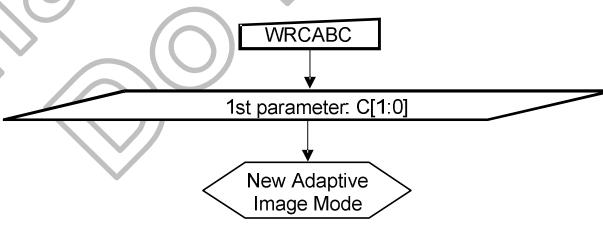
6.2.35 Write CTRL display (53h)

53H	WRCTRLD (Write Control Display)																		
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX						
Command	0	1	↑	-	0	1	0	1	0	0	1	1	53						
1 st parameter	1	1	↑	-	xx	xx	BCTRL	xx	DD	BL	xx	xx	00 .. FF						
Description	This command is used to control display brightness. BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off (Brightness registers are 00h, DBV[7..0]) 1 = On (Brightness registers are active, according to the other parameters.) Display Dimming (DD): (Only for manual brightness setting) DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (Completely turn off backlight circuit. Control lines must be low.) 1 = On Dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0. When BL bit change from "On" to "Off", backlight is turned off without gradual dimming, even if dimming-on (DD=1) are selected. X = Don't care.																		
Restriction	-																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Sleep Out	Yes																		
Sleep In	Yes																		
Default	D[7:0]= 0x00h																		
Flow Chart	 <pre> graph TD WRCTRLD[WRCTRLD] --> BCTRLD{BCTRL, DD, BL} BCTRLD --> NCVL{New Control Value Loaded} </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																		

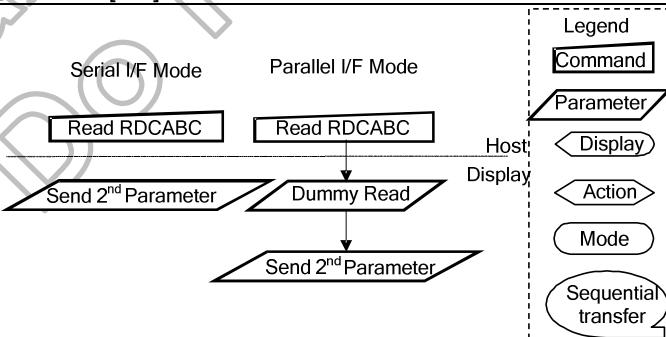
6.2.36 Read CTRL value display (54h)

54H	RDCTRLD (Read Control Value Display)																		
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX						
Command	0	1	↑	-	0	1	0	1	0	1	0	0	54						
1 st parameter	1	↑	1	-	xx	xx	xx	xx	xx	xx	xx	xx	xx						
2 nd parameter	1	↑	1	-	0	0	BCTRL	0	DD	BL	0	0	xx						
Description	This command returns ambient light and brightness control values, see chapter: "6.2.45 Write CTRL Display (53h)". BCTRL: Brightness Control Block On/Off, This bit is always used to switch brightness for display. 0 = Off 1 = On Display Dimming (DD): DD = 0: Display Dimming is off DD = 1: Display Dimming is on BL: Backlight Control On/Off 0 = Off (completely turn off backlight circuit) 1 = On																		
Restriction	-																		
Register Availability	<table border="1"> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </table>													Status	Availability	Sleep Out	Yes	Sleep In	Yes
Status	Availability																		
Sleep Out	Yes																		
Sleep In	Yes																		
Default	D[7:0]= 0x00h																		
Flow Chart	 <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																		

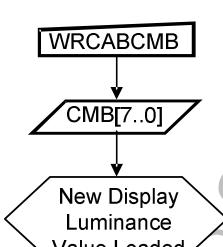
6.2.37 Write content adaptive brightness control (55h)

55 H	WRCABC (Write Content Adaptive Brightness Control)																																																																																																																																																																																																																																											
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																																																																																																																															
Command	0	1	↑	-	0	1	0	1	0	1	0	1	55																																																																																																																																																																																																																															
1 st parameter	1	1	↑	-	IMAGE_Enhance[3:0]			xx	xx	CABC[1:0]		xx																																																																																																																																																																																																																																
Description	<p>This command is used to set parameters for image content based adaptive brightness control functionality.</p> <p>There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. See chapter "5.17 Content Adaptive Brightness Control (CABC)".</p> <table border="1"> <thead> <tr> <th>C1</th> <th>C0</th> <th>Function</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Off</td> </tr> <tr> <td>0</td> <td>1</td> <td>User Interface Image</td> </tr> <tr> <td>1</td> <td>0</td> <td>Still Picture</td> </tr> <tr> <td>1</td> <td>1</td> <td>Moving Image</td> </tr> <tr> <td colspan="13">X = Don't care.</td></tr> <tr> <td colspan="3">IMAGE_Enhance[3:0]</td><td colspan="3">Function</td><td colspan="7">Note</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td colspan="3">IE and SRE off</td><td colspan="7"></td></tr> <tr> <td>1</td><td>0</td><td>0</td><td>0</td><td colspan="3">IE on, Low</td><td colspan="7">Low Enhancement of Image</td></tr> <tr> <td>1</td><td>0</td><td>0</td><td>1</td><td colspan="3">IE on, Medium</td><td colspan="7">Medium Enhancement of Image</td></tr> <tr> <td>1</td><td>0</td><td>1</td><td>1</td><td colspan="3">IE on, High</td><td colspan="7">High Enhancement of Image</td></tr> <tr> <td>0</td><td>1</td><td>0</td><td>0</td><td colspan="3">SRE on, Low</td><td colspan="7">Sunlight readability enhancement, low</td></tr> <tr> <td>0</td><td>1</td><td>0</td><td>1</td><td colspan="3">SRE on, Medium</td><td colspan="7">Sunlight readability enhancement, medium</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>0</td><td colspan="3">SRE on, High</td><td colspan="7">Sunlight readability enhancement, high</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>1</td><td colspan="3">SRE on, Auto</td><td colspan="7">Sunlight readability enhancement, auto</td></tr> <tr> <td colspan="3">Other</td><td colspan="3" rowspan="6">Reserved</td><td colspan="7" rowspan="2"></td></tr> <tr> <td>Restriction</td><td colspan="13">-</td></tr> <tr> <td rowspan="2">Register Availability</td><td colspan="6">Status</td><td colspan="7">Availability</td></tr> <tr> <td colspan="6">Sleep Out</td><td colspan="7" rowspan="3">Yes</td></tr> <tr> <td>Default</td><td colspan="13">CABC[1:0] = 00, IMAGE_Enhance[3:0]=0000</td></tr> <tr> <td>Flow Chart</td><td colspan="13">  <pre> graph TD WRCABC[WRCABC] --> C13[1st parameter: C[1:0]] C13 --> NAIM{New Adaptive Image Mode} </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer </td></tr> </tbody> </table>	C1	C0	Function	0	0	Off	0	1	User Interface Image	1	0	Still Picture	1	1	Moving Image	X = Don't care.													IMAGE_Enhance[3:0]			Function			Note							0	0	0	0	IE and SRE off										1	0	0	0	IE on, Low			Low Enhancement of Image							1	0	0	1	IE on, Medium			Medium Enhancement of Image							1	0	1	1	IE on, High			High Enhancement of Image							0	1	0	0	SRE on, Low			Sunlight readability enhancement, low							0	1	0	1	SRE on, Medium			Sunlight readability enhancement, medium							0	1	1	0	SRE on, High			Sunlight readability enhancement, high							0	1	1	1	SRE on, Auto			Sunlight readability enhancement, auto							Other			Reserved										Restriction	-													Register Availability	Status						Availability							Sleep Out						Yes							Default	CABC[1:0] = 00, IMAGE_Enhance[3:0]=0000													Flow Chart	 <pre> graph TD WRCABC[WRCABC] --> C13[1st parameter: C[1:0]] C13 --> NAIM{New Adaptive Image Mode} </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 												
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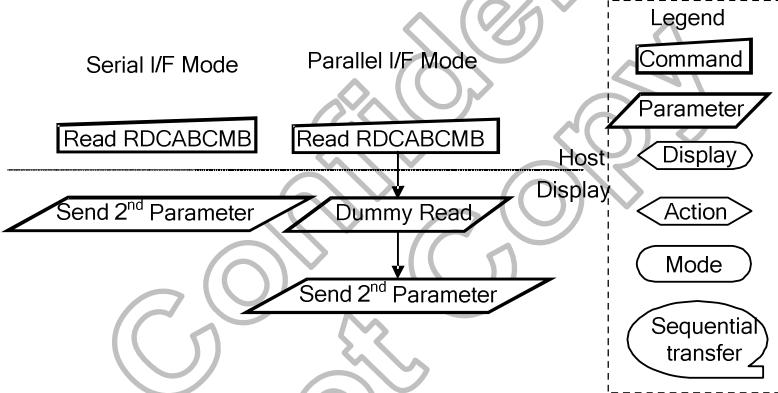
6.2.38 Read content adaptive brightness control (56h)

56H	RDCABC (Read Content Adaptive Brightness Control)																																																									
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																													
Command	0	1	↑	-	0	1	0	1	0	1	1	0	56																																													
1 st parameter	1	↑	1	-	XX	XX	XX	XX	XX	XX	XX	XX	Dummy read																																													
2 nd parameter	1	↑	1	-	IMAGE_Enhance[3:0]				0	0	C1	C0	xx																																													
Description	<p>This command is used to set parameters for image content based adaptive brightness control functionality.</p> <p>There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below. See chapter "5.17 Content Adaptive Brightness Control (CABC)".</p> <table border="1"> <tr> <th>C1</th> <th>C0</th> <th>Function</th> </tr> <tr> <td>0</td> <td>0</td> <td>Off</td> </tr> <tr> <td>0</td> <td>1</td> <td>User Interface Image</td> </tr> <tr> <td>1</td> <td>0</td> <td>Still Picture</td> </tr> <tr> <td>1</td> <td>1</td> <td>Moving Image</td> </tr> </table> <table border="1"> <tr> <th>IMAGE_Enhance[3:0]]</th> <th>Function</th> <th>Note</th> </tr> <tr> <td>0 0 0 0</td> <td>IE and SRE off</td> <td></td> </tr> <tr> <td>1 0 0 0</td> <td>IE on, Low</td> <td>Low Enhancement of Image</td> </tr> <tr> <td>1 0 0 1</td> <td>IE on, Medium</td> <td>Medium Enhancement of Image</td> </tr> <tr> <td>1 0 1 1</td> <td>IE on, High</td> <td>High Enhancement of Image</td> </tr> <tr> <td>0 1 0 0</td> <td>SRE on, Low</td> <td>Sunlight readability enhancement, low</td> </tr> <tr> <td>0 1 0 1</td> <td>SRE on, Medium</td> <td>Sunlight readability enhancement, medium</td> </tr> <tr> <td>0 1 1 0</td> <td>SRE on, High</td> <td>Sunlight readability enhancement, high</td> </tr> <tr> <td>0 1 1 1</td> <td>SRE on, Auto</td> <td>Sunlight readability enhancement, auto</td> </tr> <tr> <td>Other</td> <td>Reserved</td> <td></td> </tr> </table>													C1	C0	Function	0	0	Off	0	1	User Interface Image	1	0	Still Picture	1	1	Moving Image	IMAGE_Enhance[3:0]]	Function	Note	0 0 0 0	IE and SRE off		1 0 0 0	IE on, Low	Low Enhancement of Image	1 0 0 1	IE on, Medium	Medium Enhancement of Image	1 0 1 1	IE on, High	High Enhancement of Image	0 1 0 0	SRE on, Low	Sunlight readability enhancement, low	0 1 0 1	SRE on, Medium	Sunlight readability enhancement, medium	0 1 1 0	SRE on, High	Sunlight readability enhancement, high	0 1 1 1	SRE on, Auto	Sunlight readability enhancement, auto	Other	Reserved	
C1	C0	Function																																																								
0	0	Off																																																								
0	1	User Interface Image																																																								
1	0	Still Picture																																																								
1	1	Moving Image																																																								
IMAGE_Enhance[3:0]]	Function	Note																																																								
0 0 0 0	IE and SRE off																																																									
1 0 0 0	IE on, Low	Low Enhancement of Image																																																								
1 0 0 1	IE on, Medium	Medium Enhancement of Image																																																								
1 0 1 1	IE on, High	High Enhancement of Image																																																								
0 1 0 0	SRE on, Low	Sunlight readability enhancement, low																																																								
0 1 0 1	SRE on, Medium	Sunlight readability enhancement, medium																																																								
0 1 1 0	SRE on, High	Sunlight readability enhancement, high																																																								
0 1 1 1	SRE on, Auto	Sunlight readability enhancement, auto																																																								
Other	Reserved																																																									
Restriction																																																										
Register Availability	<table border="1"> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </table>													Status	Availability	Sleep Out	Yes	Sleep In	Yes																																							
Status	Availability																																																									
Sleep Out	Yes																																																									
Sleep In	Yes																																																									
Default	C[1:0] = 00, IMAGE_Enhance[3:0]=0000																																																									
Flow Chart	 <pre> graph TD Start(()) --> ReadS[Read RDCABC] Start(()) --> ReadP[Read RDCABC] ReadS --> SendS[Send 2nd Parameter] ReadP --> SendP[Send 2nd Parameter] SendS --> Dummy[Dummy Read] SendP --> Dummy[Dummy Read] </pre>																																																									

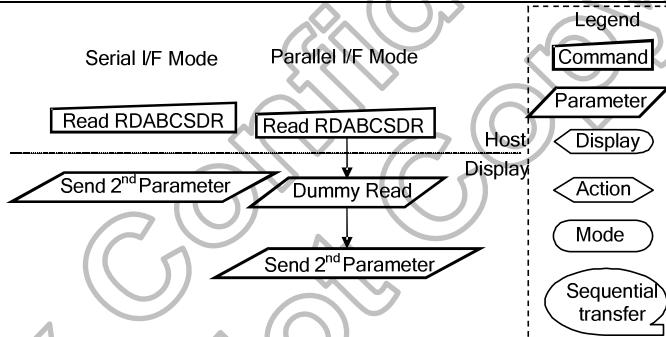
6.2.39 Write CABC minimum brightness (5Eh)

5E H	WRCABCMB (Write CABC minimum brightness)																					
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	0	1	↑	-	0	1	0	1	1	1	1	0	5E									
1 st parameter	1	1	1	-	CMB[7:0]																	
Description	This command is used to set the minimum brightness value of the display for CABC function. In principle relationship is that 00h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC. See chapter "5.17.4 Minimum brightness setting of CABC function".																					
Restriction	-																					
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>													Status	Availability	Sleep Out	Yes	Sleep In	Yes			
Status	Availability																					
Sleep Out	Yes																					
Sleep In	Yes																					
Default	CMB[7:0] = 0x00h																					
Flow Chart	 <div style="border: 1px dashed black; padding: 5px; margin-top: 10px;"> Legend Command Parameter Display Action Mode Sequential transfer </div>																					

6.2.40 Read CABC minimum brightness (5Fh)

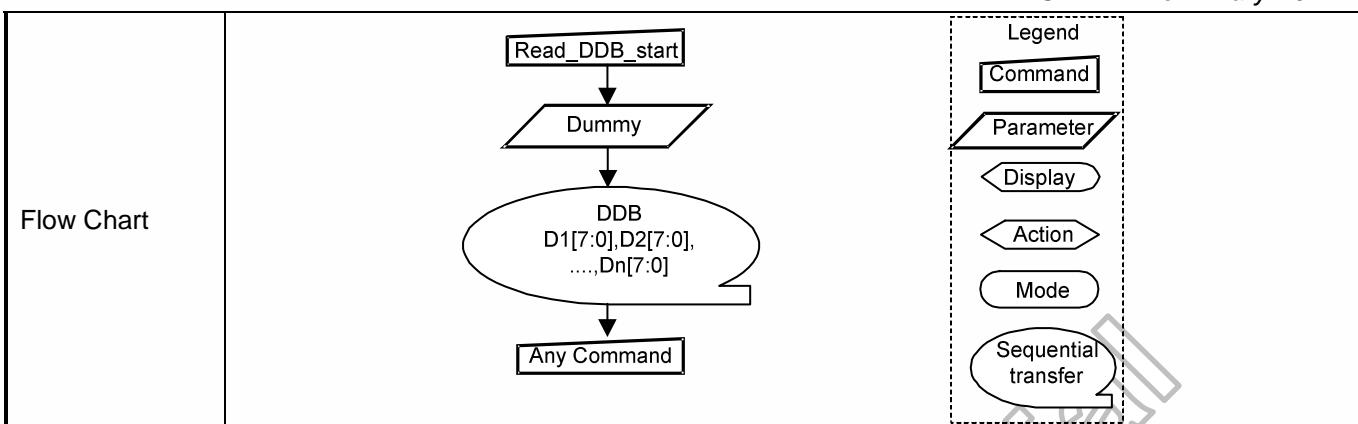
5FH	RDCABCMB (Read CABC minimum brightness)																				
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	↑	-	0	1	0	1	1	1	1	1	5F								
1 st parameter	1	↑	1	-	XX	XX	XX	XX	XX	XX	XX	XX	XX								
2 nd parameter	1	↑	1	-	CMB[7:0]								XX								
Description	This command returns the minimum brightness value of CABC function. In principle the relationship is that 00h value means the lowest brightness and FFh value means the highest brightness. See chapter "5.17.4 Minimum brightness setting of CABC function". CMB[7:0] is CABC minimum brightness specified with "6.2.49 Write CABC minimum brightness (5Eh)" command.																				
Restriction	-																				
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Sleep Out	Yes	Sleep In	Yes		
Status	Availability																				
Sleep Out	Yes																				
Sleep In	Yes																				
Default	CMB[7:0] = 0x00h																				
Flow Chart	 <pre> graph TD Start(()) --> SIF[Serial I/F Mode] Start --> PIF[Parallel I/F Mode] SIF --> ReadS[Read RDCABCMB] PIF --> ReadP[Read RDCABCMB] ReadS --> HostS(()) ReadP --> HostP(()) HostS --> SendS1[/Send 2nd Parameter/] HostS --> DummyS[/Dummy Read/] HostS --> SendS2[/Send 2nd Parameter/] HostP --> DispP(()) DispP --> ActionP[/Action/] ActionP --> ModeP[/Mode/] ModeP --> SeqP[/Sequential transfer/] </pre>																				

6.2.41 Read automatic brightness control self-diagnostic result (68h)

68H	RDABCSDR (Read Automatic Brightness Control Self-Diagnostic Result)																			
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX							
Command	0	1	↑	-	0	1	1	0	1	0	0	0	68							
1 st parameter	1	↑	1	-	xx	xx	xx	xx	xx	xx	xx	xx	xx							
2 nd parameter	1	↑	1	-	D[7:6]	0	0	0	0	0	0	0	xx							
Description	This command indicates the status of the display self-diagnostic results for automatic brightness control after Sleep Out -command as described in the table below:																			
	<ul style="list-style-type: none"> • Bit D7 – Register Loading Detection See section “5.15.1 Register loading Detection”. • Bit D6 – Functionality Detection See section “5.15.2 Functionality Detection ”. • Bits D5, D4, D3, D2, D1 and D0 are for future use and are set to ‘0’. 																			
Restriction	-																			
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Sleep Out	Yes	Sleep In	Yes
Status	Availability																			
Sleep Out	Yes																			
Sleep In	Yes																			
Default	D[7:0] = 0x00h																			
Flow Chart	 <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																			

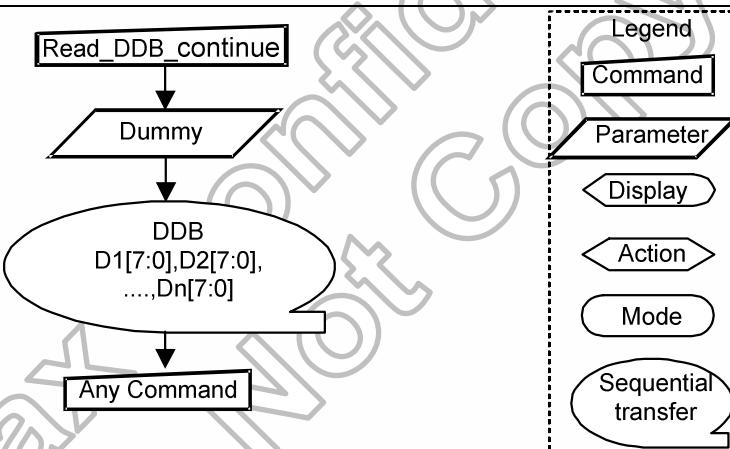
6.2.42 Read_DDB_start (A1h)

A1H	Read_DDB_start																								
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	-	1	0	1	0	0	0	0	1	A1												
1 st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read												
2 nd parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx												
:	1	↑	1	-	x	x	x	x	x	x	x	x	xx												
N th parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx												
Description	<p>This command reads identifying and descriptive information from the peripheral. This information is organized in the Device Descriptor Block (DDB) stored on the peripheral. The response to this command returns a sequence of bytes that may be any length up to 64K bytes. Note that the returned sequence of bytes does not necessarily correspond to the entire DDB; it may be a portion of a larger block of data.</p> <p>The format of returned data is as follows:</p> <ul style="list-style-type: none"> Parameter 2: LS (least significant) byte of Supplier ID. Supplier ID is a unique value assigned to each peripheral supplier by the MIPI organization. Parameter 3: MS (most significant) byte of Supplier ID. Parameter 4: LS (least significant) byte of Supplier Elective Data. This is a byte of information that is determined by the supplier. It could include model number or revision information, for example. Parameter 5: MS (most significant) byte of Supplier Elective Data Parameter 6: single-byte <i>Escape or Exit Code</i> (EEC). The code is interpreted as follows: <ul style="list-style-type: none"> - FFh - Exit code – there is no more data in the Descriptor Block - 00h - Escape code – there is supplier-proprietary data in the Descriptor Block (does not conform to any MIPI standard) - Any other value – there is DDB data in the Descriptor Block. The format and interpretation of this data is documented in <i>MIPI Alliance Standard for Device Descriptor Block (DDB)</i>. <p>DDBs may contain many more data fields providing information about the peripheral.</p> <p>In a DSI system, read activity takes the form of two separate transactions across the bus: first the read command read_DDB_start from host processor to peripheral, which includes the bus turn-around token.</p> <p>The peripheral then takes control of the bus and returns the requested data. The peripheral response to read_DDB_start is a Long Packet type, so its length may be up to 64K bytes unless limited by a previous set_max_return_size command.</p> <p>The response to a read_DDB_start command always starts at the beginning of the Device Descriptor Block. After receiving the first packet and processing the returned DDB data, the host processor may initiate a read_DDB_continue command to access the next portion of the DDB. A read_DDB_continue command begins the next read at the location following the last byte of the previous data read from the DDB.</p> <p>Subsequent read_DDB_continue commands can be used to read a DDB or supplier-proprietary block of arbitrary size. There is, however, no obligation to read the entire block. The host processor may choose to stop reading after completion of any read_DDB_xxx command.</p>																								
Restrictions	-																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	D[7:0] = 0x00h																								

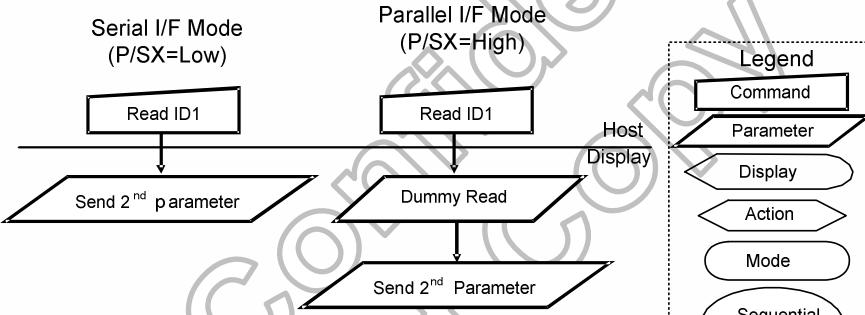


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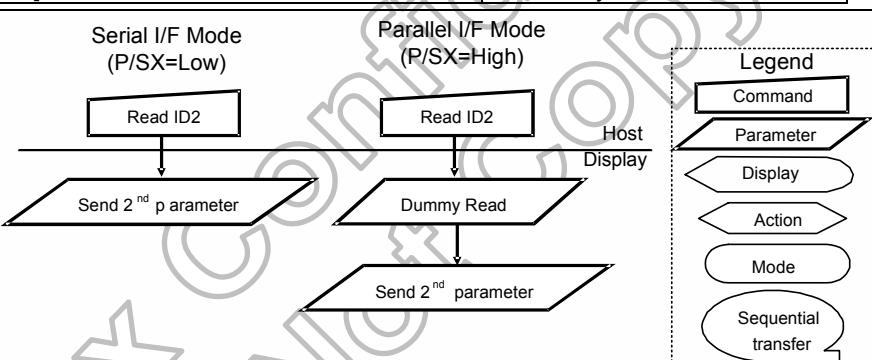
6.2.43 Read_DDB_continue (A8h)

A8H	Read_DDB_continue																								
	D/CX	RDX	WRX	D15-D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	-	1	0	1	0	1	0	0	0	A8												
1 st parameter	1	↑	1	-	x	x	x	x	x	x	x	x	Dummy read												
2 nd parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx												
:	1	↑	1	-	x	x	x	x	x	x	x	x	xx												
N th parameter	1	↑	1	-	x	x	x	x	x	x	x	x	xx												
Description	A read_DDB_start command should be executed at least once before a read_DDB_continue command to define the read location. Otherwise, data read with a read_DDB_continue command is undefined.																								
Restrictions	-																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	D[7:0] = 0x00h																								
Flow Chart	 <pre> graph TD A[Read_DDB_continue] --> B{Dummy} B --> C((DDB D1[7:0], D2[7:0], ..., Dn[7:0])) C --> D[Any Command] </pre> <p>Legend:</p> <ul style="list-style-type: none"> Command Parameter Display Action Mode Sequential transfer 																								

6.2.44 Read ID1 (DAh)

DAH	RDID1 (Read ID1)																								
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	↑	-	1	1	0	1	1	0	1	0	DA												
1 st parameter	1	↑	1	-	-	-	-	-	-	-	-	-	-												
2 nd parameter	1	↑	1	-	module's manufacturer[7:0]								xx												
Description	This read byte identifies the LCD module's manufacturer. It is specified by display supplier and for xx is defined as xxHEX.																								
Restriction	-																								
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>													Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																								
Normal Mode On, Idle Mode Off, Sleep Out	Yes																								
Normal Mode On, Idle Mode On, Sleep Out	Yes																								
Partial Mode On, Idle Mode Off, Sleep Out	Yes																								
Partial Mode On, Idle Mode On, Sleep Out	Yes																								
Sleep In or Booster Off	Yes																								
Default	<table border="1"> <thead> <tr> <th>Default value</th> <th>OTP value</th> </tr> </thead> <tbody> <tr> <td>ID1[7:0]=0x00h</td> <td>Define by customer</td> </tr> </tbody> </table>													Default value	OTP value	ID1[7:0]=0x00h	Define by customer								
Default value	OTP value																								
ID1[7:0]=0x00h	Define by customer																								
Flow Chart	 <pre> graph TD Start1[Read ID1] --> Send1[/Send 2nd parameter/] Start2[Read ID1] --> Host[Host Display] Host --> Dummy1[/Dummy Read/] Dummy1 --> Send2[/Send 2nd Parameter/] legend[Legend] legend -- Command --> rect[] legend -- Parameter --> para[] legend -- Display --> trap[] legend -- Action --> diam[] legend -- Mode --> oval[] legend -- Sequential transfer --> seq[] </pre>																								

6.2.45 Read ID2 (DBh)

DBH	RDID2 (Read ID2)																									
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX													
Command	0	1	↑	-	1	1	0	1	1	0	1	1	DB													
1 st parameter	1	↑	1	-	xx	xx	xx	xx	xx	xx	xx	xx	xx													
2 nd parameter	1	↑	1	-	LCD module/driver version [7:0]																					
Description	This read byte is used to track the LCD module/driver version. It is defined by display supplier and changes each time a revision is made to the display, material or construction specifications. See Table:																									
Restrictions	-																									
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Partial Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>														Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Partial Mode On, Idle Mode Off, Sleep Out	Yes	Partial Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																									
Normal Mode On, Idle Mode Off, Sleep Out	Yes																									
Normal Mode On, Idle Mode On, Sleep Out	Yes																									
Partial Mode On, Idle Mode Off, Sleep Out	Yes																									
Partial Mode On, Idle Mode On, Sleep Out	Yes																									
Sleep In or Booster Off	Yes																									
Default	<table border="1"> <thead> <tr> <th>Default value</th> <th>OTP value</th> </tr> </thead> <tbody> <tr> <td>ID2[7:0]=0x00h</td> <td>Define by customer</td> </tr> </tbody> </table>														Default value	OTP value	ID2[7:0]=0x00h	Define by customer								
Default value	OTP value																									
ID2[7:0]=0x00h	Define by customer																									
Flow Chart	 <pre> graph TD subgraph Host [Host] direction TB H1[Read ID2] --> S1[/Send 2nd parameter/] H2[Read ID2] --> P1[/Dummy Read/] P1 --> S2[/Send 2nd parameter/] end subgraph Display [Display] direction TB S1 P1 S2 end Legend[Legend] Legend --- C[Command] Legend --- P[Parameter] Legend --- D[Display] Legend --- A[Action] Legend --- M[Mode] Legend --- ST[Sequential transfer] </pre>																									

6.2.46 Read ID3 (DCh)

DCH	RDID3 (Read ID3)																				
	DNC	NRD	NWR	D15~D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	↑	-	1	1	0	1	1	1	0	0	DC								
1 st parameter	1	↑	1	-	xx	xx	xx	xx	xx	xx	xx	xx	xx								
2 nd parameter	1	↑	1	-	LCD module/driver ID[7:0]								xx								
Description	This read byte identifies the LCD module/driver. It is specified by display supplier and for this LCD project module is defined as xxHEX.																				
Restrictions	-																				
Register Availability	Status							Availability													
	Normal Mode On, Idle Mode Off, Sleep Out							Yes													
	Normal Mode On, Idle Mode On, Sleep Out							Yes													
	Partial Mode On, Idle Mode Off, Sleep Out							Yes													
	Partial Mode On, Idle Mode On, Sleep Out							Yes													
	Sleep In or Booster Off							Yes													
Default	Default value							OTP value													
	ID3[7:0]=0x00h							Define by customer													
Flow Chart	Serial I/F Mode (P/SX=Low)				Parallel I/F Mode (P/SX=High)				Host Display												
	<pre> graph TD A[Read ID3] --> B[/Send 2nd parameter/] B --> C[/Dummy Read/] </pre>				<pre> graph TD A[Read ID3] --> B[/Dummy Read/] B --> C[/Send 2nd parameter/] </pre>				<pre> graph LR subgraph Legend [Legend] direction TB L1[Command] --> C1[/] L2[Parameter] --> C2[/--/] L3[Display] --> C3[/-->] L4[Action] --> C4[/<-->] L5[Mode] --> C5[/<-->] L6[Sequential transfer] --> C6(()) end </pre>												

6.3 User Define Command Description

6.3.1 SETSEQUENCE: Set Sequence (B0h)

B0H	SETSEQUENCE(Set Sequence)																																							
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																														
Command	0	1	1	0	1	1	1	0	0	B0																														
1 st parameter	1	-								AUTO_OPT[6:0]																														
2 nd parameter	1	-	-	-	-	-	-	-	OSC_EN	-																														
3 rd parameter	1	VSP_DIS_C	VSN_EN	VSP_EN	VGL_EN	VGH_EN	VCL_EN	VDDDN_HZ	STB	-																														
4 th parameter	1	-	-	-	-	GON	DTE	D[1:0]		-																														
Description	<p>This command is used for DCS command auto sequence and manual mode debug use, please don't access this command in initial code.</p> <p>AUTO_OPT[6:0]: Internal option, not OPEN</p> <p>OSC_EN: Enable internal oscillator, High active.</p> <p>STB: When STB = "1", the HX8379-A enters the standby mode, where all display operation stops, suspend all the internal operations. But the internal R-C oscillator stop or not is determined by OSC_EN bit. To minimize the standby power, please set OSC_EN to 0. During the standby mode, only the following process can be executed.</p> <ul style="list-style-type: none"> a. Exit the Standby mode (STB = "0") b. Enable or disable the oscillation c. Software reset <p>VDDDN_HZ: Choose external or internal VDDDN power. VDDDN_HZ=0, VDDDN=-2.5V. VDDDN_HZ=1, VDDDN output High-Z. (For external VDDDN.)</p> <p>VCL_EN : ON/OFF the operation of VCL charge bump circuit.</p> <table border="1"> <tr> <td>VCL_EN</td> <td>Operation of VCL charge bump circuit</td> </tr> <tr> <td>0</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>ON</td> </tr> </table> <p>VGH_EN: ON/OFF the operation of VGH charge bump circuit.</p> <table border="1"> <tr> <td>VGH_EN</td> <td>Operation of VGH charge bump circuit</td> </tr> <tr> <td>0</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>ON</td> </tr> </table> <p>VGL_EN: ON/OFF the operation of VGL charge bump circuit.</p> <table border="1"> <tr> <td>VGL_EN</td> <td>Operation of VGL charge bump circuit</td> </tr> <tr> <td>0</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>ON</td> </tr> </table> <p>VSP_EN: ON/OFF the operation of VSP circuit.</p> <table border="1"> <tr> <td>VSP_EN</td> <td>Operation of VSP DC/DC circuit</td> </tr> <tr> <td>0</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>ON</td> </tr> </table> <p>VSN_EN: ON/OFF the operation of VSN circuit.</p> <table border="1"> <tr> <td>VSN_EN</td> <td>Operation of VSN DC/DC circuit</td> </tr> <tr> <td>0</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>ON</td> </tr> </table>										VCL_EN	Operation of VCL charge bump circuit	0	OFF	1	ON	VGH_EN	Operation of VGH charge bump circuit	0	OFF	1	ON	VGL_EN	Operation of VGL charge bump circuit	0	OFF	1	ON	VSP_EN	Operation of VSP DC/DC circuit	0	OFF	1	ON	VSN_EN	Operation of VSN DC/DC circuit	0	OFF	1	ON
VCL_EN	Operation of VCL charge bump circuit																																							
0	OFF																																							
1	ON																																							
VGH_EN	Operation of VGH charge bump circuit																																							
0	OFF																																							
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VGL_EN	Operation of VGL charge bump circuit																																							
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VSP_EN	Operation of VSP DC/DC circuit																																							
0	OFF																																							
1	ON																																							
VSN_EN	Operation of VSN DC/DC circuit																																							
0	OFF																																							
1	ON																																							

D[1:0]: Setting Source driver output

D1	D0	Source Output	HX8379-A Internal Display Operations
0	0	VSSD	Halt
0	1	Inhibit	Inhibit
1	0	V255	Operate
1	1	Display	Operate

GON: GIP control signal enable selection

GON	GIP Enable
0	GIP Off
1	GIP On

DTE: Source output enable selection

DTE	Source Output
0	Source output off
1	Source output on

Restrictions SETEXTC turn on to enable this command.

Register Availability	Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out		Yes
Normal Mode On, Idle Mode On, Sleep Out		Yes
Sleep In or Booster Off		Yes

6.3.2 SETPOWER: Set power (B1h)

B1H	SETPOWER(Set power related setting)																							
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
Command	0	1	0	1	1	0	0	0	1	B1														
1 st parameter	1					Dummy				-														
2 nd parameter	1	-		DCLK_Reserved[2:0]		-	-	VGL_REG_EN	DSTB	-														
3 rd parameter	1			FS2[3:0]		VRGH_EN		AP[2:0]		-														
4 th parameter	1					VGHS[7:0]				-														
5 th parameter	1					VGLS[7:0]				-														
6 th parameter	1	-	-			VGL_REGS[5:0]				-														
7 th parameter	1	-	-			VRGH[5:0]				-														
8 th parameter	1	-	-	-		BTP[4:0]				-														
9 th parameter	1			VCL[2:0]				BTN[4:0]		-														
10 th parameter	1					VRHP[7:0]				-														
11 th parameter	1					VRHN[7:0]				-														
12 th parameter	1	APF_EN	DD_TU			VRMP[5:0]				-														
13 th parameter	1	-	-			VRMN[5:0]				-														
14 th parameter	1			FS1[3:0]		-		PCCS[2:0]		-														
15 th parameter	1		DT[1:0]		-			FS0[4:0]		-														
16 th parameter	1	-		XDK[2:0]				XDKN[2:0]	AUTO_XDK	-														
17 th parameter	1	CLK_OPT2	CLK_OPT1	DC_VPNL[1:0]				DCDIV[3:0]		-														
18 th parameter	1		DCS[1:0]			DTPS[2:0]			DTNS[2:0]	-														
19 th parameter	1		A_DC[1:0]			A_DTP[2:0]			A_DTN[2:0]	-														
20 th parameter	1		B_DC[1:0]			B_DTP[2:0]			B_DTN[2:0]	-														
21 th parameter	1		C_DC[1:0]			C_DTP[2:0]			C_DTN[2:0]	-														
22 th parameter	1		D_DC[1:0]			D_DTP[2:0]			D_DTN[2:0]	-														
23 th parameter	1		E_DC[1:0]			E_DTP[2:0]			E_DTN[2:0]	-														
24 th parameter	1					DUMMY				-														
25 th parameter	1			FS0_LP[2:0]				BTP0[4:0]		-														
26 th parameter	1	-		FS1_LP[1:0]				BTP1[4:0]		-														
27 th parameter	1	-		DC_DIV_LP[1:0]				BTP2[4:0]		-														
28 th parameter	1	-		DTP_LP[1:0]				BTP3[4:0]		-														
29 th parameter	1	-		DTN_LP[1:0]				BTP4[4:0]		-														
30 th parameter	1	-		FS2_LP[1:0]				BTP5[4:0]		-														
Description	This command is used to set related setting of power.																							
	DSTB: Only active ac DSI mode. When DSTB=1, DSI will enter ULPS while IC into sleep in mode.																							
	VGL_REG_EN: ON/OFF the operation of VGL_REG circuit.																							
	<table border="1"> <tr> <th>VGL_REG_EN</th> <th>Operation of VGL charge bump circuit</th> </tr> <tr> <td>0</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>ON</td> </tr> </table>										VGL_REG_EN	Operation of VGL charge bump circuit	0	OFF	1	ON								
VGL_REG_EN	Operation of VGL charge bump circuit																							
0	OFF																							
1	ON																							
DCLK_Reserved[2:0]: Internal used, not open.																								
VRGH_EN: ON/OFF the operation of VRGH circuit.																								
<table border="1"> <tr> <th>VRGH_EN</th> <th>Operation of VRGH voltage circuit</th> </tr> <tr> <td>0</td> <td>OFF</td> </tr> <tr> <td>1</td> <td>ON</td> </tr> </table>										VRGH_EN	Operation of VRGH voltage circuit	0	OFF	1	ON									
VRGH_EN	Operation of VRGH voltage circuit																							
0	OFF																							
1	ON																							
FS2[3:0]: Adjust the charge pump frequency of internal VCL, VSN Fosc_pump=5MHz																								
<table border="1"> <tr> <th colspan="4">FS2[3:0]</th> <th>Charge pump frequency of VCL, VSN</th> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>Fosc_pump / 32</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>Fosc_pump / 64</td> </tr> </table>										FS2[3:0]				Charge pump frequency of VCL, VSN	0	0	0	0	Fosc_pump / 32	0	0	0	1	Fosc_pump / 64
FS2[3:0]				Charge pump frequency of VCL, VSN																				
0	0	0	0	Fosc_pump / 32																				
0	0	0	1	Fosc_pump / 64																				

0	0	1	1		Fosc_pump / 128
0	1	0	0		Fosc_pump / 160
0	1	0	1		Fosc_pump / 192
0	1	1	0		Fosc_pump / 224
0	1	1	1		Fosc_pump / 256
Others					Inhibited

AP[2:0]: Adjust the amount of fixed current from the fixed current source for the operational amplifier in the power supply circuit. When the amount of fixed current is increased, the LCD driving capacity and the display quality are high, but the current consumption is increased. This is a tradeoff, Adjust the fixed current by considering both the display quality and the current consumption. During no display operation, when AP[2:0] = 000, the current consumption can be reduced by stopping the operations of operational amplifier and step-up circuit.

AP2	AP1	AP0	Constant Current of Operational Amplifier
0	0	0	Stop
0	0	1	0.5μA
0	1	0	1.0μA
0	1	1	1.5μA
1	0	0	2.0μA
1	0	1	2.5μA
1	1	0	3.0μA
1	1	1	3.5μA

VGHS[5:0]: Switch the output factor for DC/DC circuit for VGH voltage generation. The LCD drive voltage level VGH can be selected according to the characteristic of liquid crystal which panel used.

VGHS5	VGHS4	VGHS3	VGHS2	VGHS1	VGHS0	VGH (V)
0	0	0	0	0	0	7.005
0	0	0	0	0	1	7.200
0	0	0	0	1	0	7.406
0	0	0	0	1	1	7.624
0	0	0	1	0	0	7.807
0	0	0	1	0	1	8.000
0	0	0	1	1	0	8.203
0	0	0	1	1	1	8.416
0	0	1	0	0	0	8.640
0	0	1	0	0	1	8.816
0	0	1	0	1	0	9.000
0	0	1	0	1	1	9.191
0	0	1	1	0	0	9.391
0	0	1	1	0	1	9.600
0	0	1	1	1	0	9.818
0	0	1	1	1	1	9.969
0	1	0	0	0	0	10.205
0	1	0	0	0	1	10.452
0	1	0	0	1	0	10.623
0	1	0	0	1	1	10.800
0	1	0	1	0	0	10.983
0	1	0	1	0	1	11.172
0	1	0	1	1	0	11.368
0	1	0	1	1	1	11.571
0	1	1	0	0	0	11.782
0	1	1	0	0	1	12.000
0	1	1	0	1	0	12.226
0	1	1	0	1	1	12.462
0	1	1	1	0	0	12.583
0	1	1	1	0	1	12.832
0	1	1	1	1	0	12.960
0	1	1	1	1	1	13.224
1	0	0	0	0	0	13.361
1	0	0	0	0	1	13.642

1	0	0	0	1	0	13.787
1	0	0	0	1	1	14.087
1	0	0	1	0	0	14.242
1	0	0	1	0	1	14.400
1	0	0	1	1	0	14.562
1	0	0	1	1	1	14.727
1	0	1	0	0	0	15.070
1	0	1	0	0	1	15.247
1	0	1	0	1	0	15.429
1	0	1	0	1	1	15.614
1	0	1	1	0	0	15.805
1	0	1	1	0	1	16.000
1	0	1	1	1	0	16.200
1	0	1	1	1	1	16.405
1	1	0	0	0	0	16.615
1	1	0	0	0	1	16.831
1	1	0	0	1	0	17.053
1	1	0	1	1	0	18.000
1	1	0	1	1	1	18.000
Others					Inhibited	

VGHS[7:6]: Specify the VGH voltage source.

VGHS7	VGHS6	VGH	VGH Fine Adjust Range
0	0	VSP+VDD3	VDD3 ~ VSP+VDD3
0	1	VSP*2	VSP ~ VSP*2
1	0	VSP-VSN+VDD3	-VSN+VDD3 ~ VSP-VSN+VDD3
1	1	VSP*2 -VSN	VSP-VSN ~ VSP*2-VSN

VGLS[5:0]: Switch the output factor for DC/DC circuit for VGL voltage generation. The LCD drive voltage level VGL can be selected according to the characteristic of liquid crystal which panel used.

VGLS5	VGLS4	VGLS3	VGLS2	VGLS1	VGLS0	VGL (V)
0	0	0	0	0	0	-7.005
0	0	0	0	0	1	-7.200
0	0	0	0	1	0	-7.406
0	0	0	0	1	1	-7.624
0	0	0	1	0	0	-7.807
0	0	0	1	0	1	-8.000
0	0	0	1	1	0	-8.203
0	0	0	1	1	1	-8.416
0	0	1	0	0	0	-8.640
0	0	1	0	0	1	-8.816
0	0	1	0	1	0	-9.000
0	0	1	0	1	1	-9.191
0	0	1	1	0	0	-9.391
0	0	1	1	0	1	-9.600
0	0	1	1	1	0	-9.818
0	0	1	1	1	1	-9.969
0	1	0	0	0	0	-10.205
0	1	0	0	0	1	-10.452
0	1	0	0	1	0	-10.623
0	1	0	0	1	1	-10.800
0	1	0	1	0	0	-10.983
0	1	0	1	0	1	-11.172
0	1	0	1	1	0	-11.368
0	1	0	1	1	1	-11.571
0	1	1	0	0	0	-11.782
0	1	1	0	0	1	-12.000
0	1	1	0	1	0	-12.226
0	1	1	0	1	1	-12.462
0	1	1	1	0	0	-12.583
0	1	1	1	0	1	-12.832
0	1	1	1	1	0	-12.960
0	1	1	1	1	1	-13.224

1	0	0	0	0	0	-13.361
1	0	0	0	0	1	-13.642
1	0	0	0	1	0	-13.787
1	0	0	0	1	1	-14.087
1	0	0	1	0	0	-14.242
1	0	0	1	0	1	-14.400
1	0	0	1	1	0	-14.562
1	0	0	1	1	1	-14.727
1	0	1	0	0	0	-15.070
1	0	1	0	0	1	-15.247
1	0	1	0	1	0	-15.429
1	0	1	0	1	1	-15.614
1	0	1	1	0	0	-15.805
1	0	1	1	0	1	-16.000
1	0	1	1	1	0	-16.200
1	0	1	1	1	1	-16.405
1	1	0	0	0	0	-16.615
1	1	0	0	0	1	-16.831
1	1	0	0	1	0	-17.053
1	1	0	0	1	1	-17.280
1	1	0	1	0	0	-17.514
1	1	0	1	0	1	-17.753
1	1	0	1	1	0	-18.000
1	1	0	1	1	1	-18.000
Others					Inhibited	

VGLS[7:6]: Specify the VGL voltage source.

VGLS7	VGLS6	VGL	VGL Fine Adjust Range
0	0	VSN+VCL	VCL ~ VSN+VCL
0	1	VSN-VSP	-VSP ~ VSN-VSP
1	0	VSN+VCL-VSP	VCL-VSP ~ VSN+VCL-VSP
1	1	VSN*2-VSP	VSN-VSP ~ VSN*2-VSP

VGL_REGS[5:0]: Set the VGL_REG voltage level.

VGL_REGS[5:0]						VGL_REG (V)
0	0	0	0	0	0	-6.400
0	0	0	0	0	1	-6.600
0	0	0	0	1	0	-6.800
0	0	0	0	1	1	-7.000
0	0	0	1	0	0	-7.200
0	0	0	1	0	1	-7.400
0	0	0	1	1	0	-7.600
0	0	0	1	1	1	-7.800
0	0	1	0	0	0	-8.000
0	0	1	0	0	1	-8.200
0	0	1	0	1	0	-8.400
0	0	1	0	1	1	-8.600
0	0	1	1	0	0	-8.800
0	0	1	1	0	1	-9.000
0	0	1	1	1	0	-9.200
0	0	1	1	1	1	-9.400
0	1	0	0	0	0	-9.600
0	1	0	0	0	1	-9.800
0	1	0	0	1	0	-10.000
0	1	0	0	1	1	-10.200
0	1	0	1	0	0	-10.400
0	1	0	1	0	1	-10.600
0	1	0	1	1	0	-10.800
0	1	0	1	1	1	-11.000
0	1	1	0	0	0	-11.200
0	1	1	0	0	1	-11.400
0	1	1	0	1	0	-11.600
0	1	1	0	1	1	-11.800
0	1	1	1	0	0	-12.000

0	1	1	1	0	1	-12.200
0	1	1	1	1	0	-12.400
0	1	1	1	1	1	-12.600
1	0	0	0	0	0	-12.800
1	0	0	0	0	1	-13.000
1	0	0	0	1	0	-13.200
1	0	0	0	1	1	-13.400
1	0	0	1	0	0	-13.600
1	0	0	1	0	1	-13.800
1	0	0	1	1	0	-14.000
1	0	0	1	1	1	-14.200
1	0	1	0	0	0	-14.400
1	0	1	0	0	1	-14.600
1	0	1	0	1	0	-14.800
1	0	1	0	1	1	-15.000
1	0	1	1	0	0	-15.200
1	0	1	1	0	1	-15.400
1	0	1	1	1	0	-15.600
1	0	1	1	1	1	-15.800
1	1	0	0	0	1	-16.200
1	1	0	0	1	0	-16.400
1	1	0	0	1	1	-16.600
1	1	0	1	0	0	-16.800
1	1	0	1	0	1	-17.000
1	1	0	1	1	0	-17.200
1	1	0	1	1	1	-17.400
1	1	1	0	0	0	-17.600
1	1	1	0	0	1	-17.800
1	1	1	0	1	0	-18.000
Others						Inhibited

VRGH[5:0]: Set the VRGH voltage level.

VRGH[5:0]						VRGH (V)
0	0	0	0	0	0	3.000
0	0	0	0	0	1	3.495
0	0	0	0	1	0	4.000
0	0	0	0	1	1	4.091
0	0	0	1	0	0	4.186
0	0	0	1	0	1	4.286
0	0	0	1	1	0	4.390
0	0	0	1	1	1	4.500
0	0	1	0	0	0	4.615
0	0	1	0	0	1	4.675
0	0	1	0	1	0	4.800
0	0	1	0	1	1	4.932
0	0	1	1	0	0	5.000
0	0	1	1	0	1	5.070
0	0	1	1	1	0	5.217
0	0	1	1	1	1	5.294
0	1	0	0	0	0	5.373
0	1	0	0	0	1	5.538
0	1	0	0	1	0	5.625
0	1	0	0	1	1	5.714
0	1	0	1	0	0	5.806
0	1	0	1	0	1	5.902
0	1	0	1	1	0	6.000
0	1	0	1	1	1	6.545
0	1	1	0	0	0	7.059
0	1	1	0	0	1	7.500
0	1	1	0	1	0	8.000
0	1	1	0	1	1	8.571
0	1	1	1	0	0	9.000
0	1	1	1	0	1	9.474
0	1	1	1	1	0	10.000
0	1	1	1	1	1	10.588

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1	0	0	0	0	0	10.909
1	0	0	0	0	1	11.613
1	0	0	0	1	0	12.000
1	0	0	0	1	1	12.414
1	0	0	1	0	0	12.857
Others					Inhibited	

BTP[4:0]: Switch the output factor for DC/DC circuit for VSP voltage generation. The LCD drive voltage level VSP can be selected according to the characteristic of liquid crystal which panel used.

BTP4	BTP3	BTP2	BTP1	BTP0	VSP (V)
0	0	0	0	0	3.000
0	0	0	0	1	3.150
0	0	0	1	0	3.300
0	0	0	1	1	3.450
0	0	1	0	0	3.600
0	0	1	0	1	3.750
0	0	1	1	0	3.900
0	0	1	1	1	4.050
0	1	0	0	0	4.200
0	1	0	0	1	4.350
0	1	0	1	0	4.500
0	1	0	1	1	4.650
0	1	1	0	0	4.800
0	1	1	0	1	4.950
0	1	1	1	0	5.100
0	1	1	1	1	5.250
1	0	0	0	0	5.400
1	0	0	0	1	5.550
1	0	0	1	0	5.700
1	0	0	1	1	5.850
1	0	1	0	0	6.000
1	0	1	0	1	6.150
1	0	1	1	0	6.300
1	0	1	1	1	6.450
1	1	0	0	0	6.600
Others					Inhibited

BTN[4:0]: For PCCS[2:0]=001 (PFM, Type-C) and PCCS[2:0]=010 (Internal Charge Pump) only. Switch the output factor of DC/DC circuit for VSN voltage generation. The LCD drive voltage level VSN can be selected according to the characteristic of liquid crystal which panel used.

BTN4	BTN3	BTN2	BTN1	BTN0	VSN (V)
0	0	0	0	0	-3.000
0	0	0	0	1	-3.150
0	0	0	1	0	-3.300
0	0	0	1	1	-3.450
0	0	1	0	0	-3.600
0	0	1	0	1	-3.750
0	0	1	1	0	-3.900
0	0	1	1	1	-4.050
0	1	0	0	0	-4.200
0	1	0	0	1	-4.350
0	1	0	1	0	-4.500
0	1	0	1	1	-4.650
0	1	1	0	0	-4.800
0	1	1	0	1	-4.950

0	1	1	1	0		-5.100
0	1	1	1	1		-5.250
1	0	0	0	0		-5.400
1	0	0	0	1		-5.550
1	0	0	1	0		-5.700
1	0	0	1	1		-5.850
1	0	1	0	0		-6.000
1	0	1	0	1		-6.150
1	0	1	1	0		-6.300
1	0	1	1	1		-6.450
1	1	0	0	0		-6.600
Others					Inhibited	

Note: For PCCS[2:0]=011 (HX5186-A/B Mode) and PCCS[2:0]=110 (VSN from internal charge pump, VSP from VPNL mode), VSN = -VSP.

VCL[2:0]: Set the power level of VCL voltage.

VCL2	VCL1	VCL0	VCL (V)
0	0	0	-2.5
0	0	1	-2.6
0	1	0	-2.7
0	1	1	-2.8
1	0	0	-2.9
1	0	1	-3
1	1	0	-3.1
1	1	1	-VDD3

VRHP[7:0]: VSPR regulator output control setting for source data output driving.

VRHP[7:0]								VSPR (V)
0	0	0	0	0	0	0	0	3.488
0	0	0	0	0	0	0	1	3.516
0	0	0	0	0	0	1	0	3.544
0	0	0	0	0	0	1	1	3.572
0	0	0	0	0	1	0	0	3.600
0	0	0	0	1	0	1	1	3.628
0	0	0	0	1	1	1	0	3.656
0	0	0	0	1	1	1	1	3.684
0	0	0	0	1	0	0	0	3.713
0	0	0	0	1	0	0	1	3.741
0	0	0	0	1	0	1	0	3.769
0	0	0	0	1	0	1	1	3.797
0	0	0	0	1	1	0	0	3.825
0	0	0	0	1	1	0	1	3.853
0	0	0	0	1	1	1	0	3.881
0	0	0	0	1	1	1	1	3.909
0	0	0	1	0	0	0	0	3.938
0	0	0	1	0	0	0	1	3.966
0	0	0	1	0	0	1	0	3.994
0	0	0	1	0	0	1	1	4.022
0	0	0	1	0	1	0	0	4.050
0	0	0	1	0	1	0	1	4.078
0	0	0	1	0	1	1	0	4.106
0	0	0	1	0	1	1	1	4.134
0	0	0	1	1	0	0	0	4.163
0	0	0	1	1	0	0	1	4.191
0	0	0	1	1	0	1	0	4.219
0	0	0	1	1	0	1	1	4.247
0	0	0	1	1	1	0	0	4.275
0	0	0	1	1	1	0	1	4.303
0	0	0	1	1	1	1	0	4.331
0	0	0	1	1	1	1	1	4.359
0	0	1	0	0	0	0	0	4.388
0	0	1	0	0	0	0	1	4.416

0	0	1	0	0	0	1	0	4.444
0	0	1	0	0	0	1	1	4.472
0	0	1	0	0	1	0	0	4.500
0	0	1	0	0	1	0	1	4.528
0	0	1	0	0	1	1	0	4.556
0	0	1	0	0	1	1	1	4.584
0	0	1	0	1	0	0	0	4.613
0	0	1	0	1	0	0	1	4.641
0	0	1	0	1	0	1	0	4.669
0	0	1	0	1	0	1	1	4.697
0	0	1	0	1	1	0	0	4.725
0	0	1	0	1	1	0	1	4.753
0	0	1	0	1	1	1	0	4.781
0	0	1	0	1	1	1	1	4.809
0	0	1	1	0	0	0	0	4.838
0	0	1	1	0	0	0	1	4.866
0	0	1	1	0	0	1	0	4.894
0	0	1	1	0	0	1	1	4.922
0	0	1	1	0	1	0	0	4.950
0	0	1	1	0	1	0	1	4.978
0	0	1	1	0	1	1	0	5.006
0	0	1	1	0	1	1	1	5.034
0	0	1	1	1	0	0	0	5.063
0	0	1	1	1	0	0	1	5.091
0	0	1	1	1	0	1	0	5.119
0	0	1	1	1	0	1	1	5.147
0	0	1	1	1	1	0	0	5.175
0	0	1	1	1	1	0	1	5.203
0	0	1	1	1	1	1	0	5.231
0	0	1	1	1	1	1	1	5.259
0	1	0	0	0	0	0	0	5.288
0	1	0	0	0	0	0	1	5.316
0	1	0	0	0	0	1	0	5.344
0	1	0	0	0	0	1	1	5.372
0	1	0	0	0	1	0	0	5.400
0	1	0	0	0	1	0	1	5.428
0	1	0	0	0	1	1	0	5.456
0	1	0	0	0	1	1	1	5.484
0	1	0	0	1	0	0	0	5.513
0	1	0	0	1	0	0	1	5.541
0	1	0	0	1	0	1	0	5.569
0	1	0	0	1	0	1	1	5.597
0	1	0	0	1	1	0	0	5.625
0	1	0	0	1	1	0	1	5.653
0	1	0	0	1	1	1	0	5.681
0	1	0	0	1	1	1	1	5.709
0	1	0	1	0	0	0	0	5.738
0	1	0	1	0	0	0	1	5.766
0	1	0	1	0	0	1	0	5.794
0	1	0	1	0	0	1	1	5.822
0	1	0	1	0	1	0	0	5.850
0	1	0	1	0	1	0	1	5.878
0	1	0	1	0	1	1	0	5.906
0	1	0	1	0	1	1	1	5.934
0	1	0	1	1	0	0	0	5.963
0	1	0	1	1	0	0	1	5.991
0	1	0	1	1	0	1	0	6.019
01011011 ~ 11111110								Inhibit
1	1	1	1	1	1	1	1	Hz

VRHN[7:0]: VSNR regulator output control setting for source data output driving.

VRHN[7:0]								VSNR (V)
0	0	0	0	0	0	0	0	-3.263
0	0	0	0	0	0	0	1	-3.291
0	0	0	0	0	0	1	0	-3.319

									-3.347
									-3.375
									-3.403
									-3.431
									-3.459
									-3.488
									-3.516
									-3.544
									-3.572
									-3.600
									-3.628
									-3.656
									-3.684
									-3.713
									-3.741
									-3.769
									-3.797
									-3.825
									-3.853
									-3.881
									-3.909
									-3.938
									-3.966
									-3.994
									-4.022
									-4.050
									-4.078
									-4.106
									-4.134
			1	0	0	0	0		-4.163
			1	0	0	0	0	1	-4.191
			1	0	0	0	1	0	-4.219
			1	0	0	0	1	1	-4.247
			1	0	0	1	0	0	-4.275
			1	0	0	1	0	1	-4.303
			1	0	0	1	1	0	-4.331
			1	0	0	1	1	1	-4.359
			1	0	1	0	0	0	-4.388
			1	0	1	0	0	1	-4.416
			1	0	1	0	1	0	-4.444
			1	0	1	0	1	1	-4.472
			1	0	1	1	0	0	-4.500
			1	0	1	1	0	1	-4.528
			1	0	1	1	1	0	-4.556
			1	0	1	1	1	1	-4.584
			1	1	0	0	0	0	-4.613
			1	1	0	0	0	1	-4.641
			1	1	0	0	1	0	-4.669
			1	1	0	0	1	1	-4.697
			1	1	0	1	0	0	-4.725
			1	1	0	1	0	1	-4.753
			1	1	0	1	1	0	-4.781
			1	1	0	1	1	1	-4.809
			1	1	1	0	0	0	-4.838
			1	1	1	0	0	1	-4.866
			1	1	1	1	0	0	-4.894
			1	1	1	1	0	1	-4.922
			1	1	1	1	1	0	-4.950
			1	1	1	1	1	0	-4.978
		1	1	1	1	1	1	0	-5.006
		1	1	1	1	1	1	1	-5.034
	1	0	0	0	0	0	0	0	-5.063
	1	0	0	0	0	0	0	1	-5.091
	1	0	0	0	0	0	1	0	-5.119
	1	0	0	0	0	0	1	1	-5.147

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0	1	0	0	0	1	0	0	-5.175
0	1	0	0	0	1	0	1	-5.203
0	1	0	0	0	1	1	0	-5.231
0	1	0	0	0	1	1	1	-5.259
0	1	0	0	1	0	0	0	-5.288
0	1	0	0	1	0	0	1	-5.316
0	1	0	0	1	0	1	0	-5.344
0	1	0	0	1	0	1	1	-5.372
0	1	0	0	1	1	0	0	-5.400
0	1	0	0	1	1	0	1	-5.428
0	1	0	0	1	1	1	0	-5.456
0	1	0	0	1	1	1	1	-5.484
0	1	0	1	0	0	0	0	-5.513
0	1	0	1	0	0	0	1	-5.541
0	1	0	1	0	0	1	0	-5.569
0	1	0	1	0	0	1	1	-5.597
0	1	0	1	0	1	0	0	-5.625
0	1	0	1	0	1	0	1	-5.653
0	1	0	1	0	1	1	0	-5.681
0	1	0	1	1	0	1	1	-5.709
0	1	0	1	1	0	0	0	-5.738
0	1	0	1	1	0	0	1	-5.766
0	1	0	1	1	0	1	0	-5.794
0	1	0	1	1	0	1	1	-5.822
0	1	0	1	1	1	0	0	-5.850
0	1	0	1	1	1	0	1	-5.878
0	1	0	1	1	1	1	0	-5.906
0	1	0	1	1	1	1	1	-5.934
0	1	1	0	0	0	0	0	-5.963
0	1	1	0	0	0	0	1	-5.991
0	1	1	0	0	0	1	0	-6.019
01100011 ~ 11111110								Inhibit
1	1	1	1	1	1	1	1	Hz

VRMP[5:0]: The positive polarity gamma amplitude voltage setting (VSPR-VGSP).

VRMP[5:0]						VSPR-VGSP (V)
0	0	0	0	0	0	2.588
0	0	0	0	0	1	2.644
0	0	0	0	1	0	2.700
0	0	0	0	1	1	2.756
0	0	0	1	0	0	2.813
0	0	0	1	0	1	2.869
0	0	0	1	1	0	2.925
0	0	0	1	1	1	2.981
0	0	1	0	0	0	3.038
0	0	1	0	0	1	3.094
0	0	1	0	1	0	3.150
0	0	1	0	1	1	3.206
0	0	1	1	0	0	3.263
0	0	1	1	0	1	3.319
0	0	1	1	1	0	3.375
0	0	1	1	1	1	3.431
0	1	0	0	0	0	3.488
0	1	0	0	0	1	3.544
0	1	0	0	1	0	3.600
0	1	0	0	1	1	3.656
0	1	0	1	0	0	3.713
0	1	0	1	0	1	3.769
0	1	0	1	1	0	3.825
0	1	0	1	1	1	3.881
0	1	1	0	0	0	3.938
0	1	1	0	0	1	3.994
0	1	1	0	1	0	4.050
0	1	1	0	1	1	4.106
0	1	1	1	0	0	4.163

0	1	1	1	0	1	4.219
0	1	1	1	1	0	4.275
0	1	1	1	1	1	4.331
1	0	0	0	0	0	4.388
1	0	0	0	0	1	4.444
1	0	0	0	1	0	4.500
1	0	0	0	1	1	4.556
1	0	0	1	0	0	4.613
1	0	0	1	0	1	4.669
1	0	0	1	1	0	4.725
1	0	0	1	1	1	4.781
1	0	1	0	0	0	4.838
1	0	1	0	0	1	4.894
1	0	1	0	1	0	4.950
1	0	1	0	1	1	5.006
1	0	1	1	0	0	5.063
1	0	1	1	0	1	5.119
1	0	1	1	1	0	5.175
1	0	1	1	1	1	5.231
1	1	0	0	0	0	5.288
1	1	0	0	0	1	5.344
1	1	0	0	1	0	5.400
1	1	0	0	1	1	5.456
1	1	0	1	0	0	5.513
1	1	0	1	0	1	5.569
1	1	0	1	1	0	5.625
1	1	0	1	1	1	5.681
1	1	1	0	0	0	5.738
1	1	1	0	0	1	5.794
1	1	1	0	1	0	5.850
1	1	1	0	1	1	5.906
1	1	1	1	0	0	5.963
1	1	1	1	0	1	6.019
Others						Inhibited
1	1	1	1	1	1	VSPR (VGSP=VSSA)

VRMN[5:0]: The negative polarity gamma amplitude voltage setting (VSNR-VGSN).

VRMN[5:0]						VSNR-VGSN (V)
0	0	0	0	0	0	-2.588
0	0	0	0	0	1	-2.644
0	0	0	0	1	0	-2.700
0	0	0	0	1	1	-2.756
0	0	0	1	0	0	-2.813
0	0	0	1	0	1	-2.869
0	0	0	1	1	0	-2.925
0	0	0	1	1	1	-2.981
0	0	1	0	0	0	-3.038
0	0	1	0	0	1	-3.094
0	0	1	0	1	0	-3.150
0	0	1	0	1	1	-3.206
0	0	1	1	0	0	-3.263
0	0	1	1	0	1	-3.319
0	0	1	1	1	0	-3.375
0	0	1	1	1	1	-3.431
0	1	0	0	0	0	-3.488
0	1	0	0	0	1	-3.544
0	1	0	0	1	0	-3.600
0	1	0	0	1	1	-3.656
0	1	0	1	0	0	-3.713
0	1	0	1	0	1	-3.769
0	1	0	1	1	0	-3.825
0	1	0	1	1	1	-3.881
0	1	1	0	0	0	-3.938
0	1	1	0	0	1	-3.994

0	1	1	0	1	0	-4.050
0	1	1	0	1	1	-4.106
0	1	1	1	0	0	-4.163
0	1	1	1	0	1	-4.219
0	1	1	1	1	0	-4.275
0	1	1	1	1	1	-4.331
1	0	0	0	0	0	-4.388
1	0	0	0	0	1	-4.444
1	0	0	0	1	0	-4.500
1	0	0	0	1	1	-4.556
1	0	0	1	0	0	-4.613
1	0	0	1	0	1	-4.669
1	0	0	1	1	0	-4.725
1	0	0	1	1	1	-4.781
1	0	1	0	0	0	-4.838
1	0	1	0	0	1	-4.894
1	0	1	0	1	0	-4.950
1	0	1	1	0	0	-5.006
1	0	1	1	0	1	-5.063
1	0	1	1	1	0	-5.119
1	0	1	1	1	0	-5.175
1	0	1	1	1	1	-5.231
1	1	0	0	0	0	-5.288
1	1	0	0	0	1	-5.344
1	1	0	0	1	0	-5.400
1	1	0	0	1	1	-5.456
1	1	0	1	0	0	-5.513
1	1	0	1	0	1	-5.569
1	1	0	1	1	0	-5.625
1	1	0	1	1	1	-5.681
1	1	1	0	0	0	-5.738
1	1	1	0	0	1	-5.794
1	1	1	0	1	0	-5.850
1	1	1	0	1	1	-5.906
1	1	1	1	0	0	-5.963
1	1	1	1	0	1	-6.019
Others					Inhibited	
1	1	1	1	1	1	VSNR (VGSN=VSSA)

FS1[3:0]: Set the operating frequency of the step-up circuit for VGH and VGL voltage generation. (Fosc_pump=5MHz)

FS1[3]	FS1[2]	FS1[1]	FS1[0]	Operation Frequency of Step-up Circuit for VGH/VGL
0	0	0	0	Fosc_pump /32
0	0	0	1	Fosc_pump /64
0	0	1	0	Fosc_pump /96
0	0	1	1	Fosc_pump /128
0	1	0	0	Fosc_pump /160
0	1	0	1	Fosc_pump /192
0	1	1	0	Fosc_pump /224
0	1	1	1	Fosc_pump /256
Others				Inhibited

PCCS[2:0]: Select the VSP/VSN bumping method as listed below

PCCS2	PCCS1	PCCS0	Driving Mode
0	0	1	PFM - Type C
0	1	0	Internal Charge Pump
0	1	1	HX5186-A/B
1	1	0	VSN and VSP from external
Others			Inhibited

DD_TU: DD_TU=1, VDDD will increase at sleep in mode.

APF_EN: Abnormal power-off detection enable.

DCDIV[3:0]: Set the normal operate frequency of DC/DC converter circuit during normal mode. (Fosc=15MHz)

DCDIV3	DCDIV2	DCDIV1	DCDIV0	Normal operate frequency of DC/DC converter(foscD)
0	0	0	0	Fosc / 1
0	0	0	1	Fosc / 2
0	0	1	0	Fosc / 3
0	0	1	1	Fosc / 4
0	1	0	0	Fosc / 5
0	1	0	1	Fosc / 6
0	1	1	0	Fosc / 7
0	1	1	1	Fosc / 8

DT[1:0]:Delay time of power on and power off sequence.

DT1	DT0	Delay time of power on and power off sequence on (ms)
0	0	5ms
0	1	10ms
1	0	15ms
1	1	20ms

FS0[4:0]: Frequency for VSP ciruit. (Fosc_pump=5MHz)

FS0[4]	FS0_[3:0]	Charge Pump Frequency for HX5186-A/B
0	0000	Fosc_pump / 2
	0001	Fosc_pump / 4
	0010	Fosc_pump / 8
	0011	Fosc_pump / 16
	0100	Fosc_pump / 32
	0101	Fosc_pump / 64
	0110	Fosc_pump / 128
	0111	Fosc_pump / 256
	1000	Fosc_pump / 512
	1001	Fosc_pump / 1024
	1010	Fosc_pump / 2048
	1011	Fosc_pump / 4096
	1100	Fosc_pump / 8192
	1101	Fosc_pump / 16384
	1110	Fosc_pump / 32768
	1111	Fosc_pump / 65536
10000-11111		Inhibited

AUTO_XDK: Auto XDK=1, charge pump mode is set automatically.

Auto XDK=0, charge pump mode depends on XDK[2:0], XDKN[2:0] setting.

Auto_XDK	VSPtarget	Charge pump mode
1	VDD3 x 1.5 > VSPtarget	X1.5
	VDD3 x 2 > VSPtarget > VDD3 x 1.5	X2
	VDD3 x 2.5 > VSPtarget > VDD3 x 2	X2.5
	VSPtarget > VDD3 x 3	X3
0	-	Depend on XDK[2:0]

Auto_XDK	VSNtarget	Charge pump mode
1	VSNtarget < VDD3 x 2	X2.5
	VSNtarget > VDD3 x 2	X3
0	-	Depend on XDKN[2:0]

XDKN[2:0]: Setting charge pump mode of VSN voltage

XDKN2	XDKN1	XDKN0	VSN	CAP.

0	0	0	Inhibit	-
0	0	1	X2.5 Pump	3
0	1	0	Inhibit	-
0	1	1	X3 Pump	4
1	0	0	Inhibit	-
1	0	1	X3 Pump	3
1	1	0	X2 Pump	4
1	1	1	X2.5 Pump	4

XDK[2:0]: Setting charge pump mode of VSP Voltage

XDK2	XDK1	XDK0	VSP	CAP.
0	0	0	X1.5 Pump	2
0	0	1	X2 Pump	4
0	1	0	X1.5 Pump	4
0	1	1	X2.5 Pump	3
1	0	0	X3 Pump	3
1	0	1	X2 Pump	3
1	1	0	X2.5 Pump	4
1	1	1	X3 Pump	4

DC_VPNL[1:0]: Internal used, not open.

CLK_OPT2: Internal used, not open.

CLK_OPT1: Internal used, not open.

DTNS[2:0]: Set the soft start operating duty cycle of DC/DC circuit. (PFM DC/DC circuit).

1 duty cycle = 1 foscD clock

DTNS2	DTNS1	DTNS0	Soft start operating duty cycle of DC/DC circuit
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

DTPS[2:0]: Set the soft start operating duty cycle of DC/DC circuit. (PFM DC/DC circuit).

1 duty cycle = 1 foscD clock

DTPS2	DTPS1	DTPS0	Soft start operating duty cycle of DC/DC circuit
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

DTN[2:0]:

For PFM circuit: Set the operating duty cycle of DC/DC clock for pumping phase.

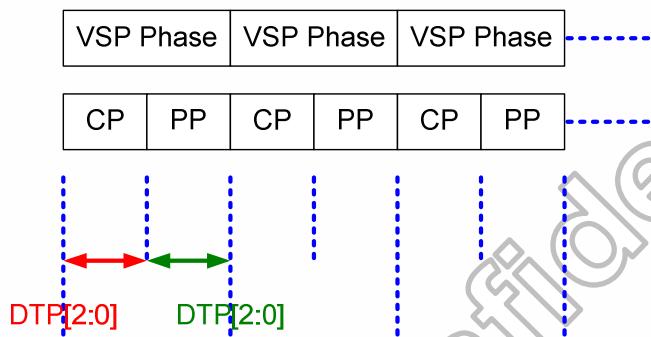
1 duty cycle = 1 foscD clock

DTN2	DTN1	DTN0	Operation Duty Cycle of DC/DC Clock for VSN Generation
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8

DTP[2:0]:
For PFM circuit: Set the operating duty cycle of DC/DC clock for charge phase.

1 duty cycle = 1 foscD clock

			Operation Duty Cycle of DC/DC Clock for VSP Generation
DTP2	DTP1	DTP0	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	8



Restriction SETEXTC turn on to enable this command.

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

6.3.3 SETDISP: Set display related register (B2h)

B2H	SETDISP(Set display related register)																																																																																																																																																					
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																																												
Command	0	1	0	1	1	0	0	1	0	B2																																																																																																																																												
1 st parameter	1					DUMMY				-																																																																																																																																												
2 nd parameter	1					DUMMY				-																																																																																																																																												
3 rd parameter	1					NL[7:0]				-																																																																																																																																												
4 th parameter	1					BP [7:0]				-																																																																																																																																												
5 th parameter	1					FP [7:0]				-																																																																																																																																												
6 th parameter	1					RTN[7:0]				-																																																																																																																																												
7 th parameter	1			SAP[3:0]			ABC_CLK_DIV[1:0]	vs_plus_bp_en	ABC_H_S_BYPASS	-																																																																																																																																												
8 th parameter	1					GEN_ON[7:0]				-																																																																																																																																												
9 th parameter	1					GEN_OFF[7:0]				-																																																																																																																																												
10 th parameter	1					BP_PE[7:0]				-																																																																																																																																												
11 th parameter	1					FP_PE[7:0]				-																																																																																																																																												
12 th parameter	1					RTN_PE[7:0]				-																																																																																																																																												
13 th parameter	1			SAP_PE[3:0]			-	-	-	-																																																																																																																																												
Description	<p>This command is used to set display related register NL[7:0]: Setting the number of lines to drive the LCD at an interval of 4 lines. The number of lines must be the same or more than the number of lines necessary for the size of the liquid crystal panel.</p> <table border="1"> <thead> <tr> <th colspan="8">NL[7:0]</th> <th>Line</th> </tr> </thead> <tbody> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td></td><td>320</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td></td><td>328</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td></td><td>336</td></tr> <tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td></td><td>344</td></tr> <tr><td colspan="8">...</td><td colspan="2">...</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td></td><td>864</td></tr> <tr><td colspan="8">...</td><td colspan="2">...</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td></td><td>1008</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td></td><td>1016</td></tr> <tr><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td></td><td>1024</td></tr> <tr><td colspan="8">Others</td><td colspan="2">Inhibited</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td></td><td>854</td></tr> <tr><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td></td><td>16(Internal used)</td></tr> </tbody> </table>											NL[7:0]								Line	0	0	0	0	0	0	0	0		320	0	0	0	0	0	0	0	1		328	0	0	0	0	0	0	1	0		336	0	0	0	0	0	0	1	1		344		0	1	0	0	0	1	0	0		864		0	1	0	1	0	1	1	0		1008	0	1	0	1	0	1	1	1		1016	0	1	0	1	1	0	0	0		1024	Others								Inhibited		1	1	1	1	1	1	1	0		854	1	1	1	1	1	1	1	1		16(Internal used)
NL[7:0]								Line																																																																																																																																														
0	0	0	0	0	0	0	0		320																																																																																																																																													
0	0	0	0	0	0	0	1		328																																																																																																																																													
0	0	0	0	0	0	1	0		336																																																																																																																																													
0	0	0	0	0	0	1	1		344																																																																																																																																													
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0	1	0	1	0	1	1	0		1008																																																																																																																																													
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0	1	0	1	1	0	0	0		1024																																																																																																																																													
Others								Inhibited																																																																																																																																														
1	1	1	1	1	1	1	0		854																																																																																																																																													
1	1	1	1	1	1	1	1		16(Internal used)																																																																																																																																													
<p>BP[7:0] : Specify the amount of scan line for back porch(BP).</p>																																																																																																																																																						
<p>FP[7:0]: Specify the amount of scan line for front porch (FP).</p>																																																																																																																																																						
<p>FP_PE[7:0]: Specify the amount of scan line for front porch (FP) on idle mode.</p>																																																																																																																																																						
<p>BP_PE[7:0] : Specify the amount of scan line for back porch(BP) on idle mode.</p> <table border="1"> <thead> <tr> <th>FP[7:0] / BP[7:0]</th> <th>Number of FP Line</th> <th>Number of BP Line</th> </tr> </thead> <tbody> <tr><td>FP_PE[7:0] / BP_PE[7:0]</td><td></td><td></td></tr> <tr><td>8h'00</td><td></td><td>2 lines</td></tr> <tr><td>8h'01</td><td></td><td>3 lines</td></tr> <tr><td>8h'02</td><td></td><td>4 lines</td></tr> <tr><td>8h'03</td><td></td><td>5 lines</td></tr> <tr><td>8h'04</td><td></td><td>6 lines</td></tr> <tr><td>8h'05</td><td></td><td>7 lines</td></tr> <tr><td>...</td><td></td><td>...</td></tr> <tr><td>8h'FB</td><td></td><td>253 lines</td></tr> <tr><td>8h'FC</td><td></td><td>254 lines</td></tr> <tr><td>8h'FD</td><td></td><td>255 lines</td></tr> </tbody> </table>										FP[7:0] / BP[7:0]	Number of FP Line	Number of BP Line	FP_PE[7:0] / BP_PE[7:0]			8h'00		2 lines	8h'01		3 lines	8h'02		4 lines	8h'03		5 lines	8h'04		6 lines	8h'05		7 lines	8h'FB		253 lines	8h'FC		254 lines	8h'FD		255 lines																																																																																																									
FP[7:0] / BP[7:0]	Number of FP Line	Number of BP Line																																																																																																																																																				
FP_PE[7:0] / BP_PE[7:0]																																																																																																																																																						
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8h'FC		254 lines																																																																																																																																																				
8h'FD		255 lines																																																																																																																																																				

8h'FF	257 lines
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Note: Set BP[7:0] = VS + VBP – 2, and FP[7:0] = VFP – 2.

RTN[7:0]: A cycle time of line width.

RTN_PE[7:0]: A cycle time of line width on idle mode.

RTN[7:0]/ RTN_PE[7:0]	Clock per Line
8h'00	200 clocks
8h'01	204 clocks
8h'02	208 clocks
8h'03	212 clocks
...	...
8'hFD	1216 clocks
8'hFE	1220 clocks
8'hFF	1224 clocks

ABC_CLK_DIV[1:0]: Select the ABC clock.

ABC_CLK_DIV1	ABC_CLK_DIV0	ABC clock division selection
0	0	OSC clock
0	1	OSC/2 clock
Others		Inhibited

VS_PLUS_BP_EN: When DSI blanking mode, internal osc will be clock.

0: No clock during DSI blanking period

1: Using internal osc as clock during blanking period.

ABC_HS_BYPASS: ABC Hsync bypass option.

0: Hsync path has latency(default)

1: Hsync path has no latency

SAP[3:0]: Set Current of Operational Amplifier

SAP_PE[3:0]: Set Current of Operational Amplifier on idle mode

SAP3	SAP2	SAP1	SAP0	Fixed Current of Operational Amplifier
SAP_PE3	SAP_PE2	SAP_PE1	SAP_PE0	
0	0	0	0	1 * Iref
0	0	0	1	2 * Iref
0	0	1	0	3 * Iref
0	0	1	1	4 * Iref
0	1	0	0	5 * Iref
0	1	0	1	6 * Iref
0	1	1	0	7 * Iref
0	1	1	1	8 * Iref
.....			
1	1	1	1	16 * Iref

GEN_ON[7:0]: Gamma OP turned on timing and in-house function not open.

GEN_OFF[7:0]: Gamma OP turned off timing and in-house function not open.

Restrictions	SETEXTC turn on to enable this command		
Register Availability	Status	Availability	
	Normal Mode On, Idle Mode Off, Sleep Out	Yes	
	Normal Mode On, Idle Mode On, Sleep Out	Yes	
	Sleep In or Booster Off	Yes	

6.3.4 SETRGBIF: Set RGB interface related register (B3h)

B3H	SETRGBIF(Set RGB interface related register)																																																																																																																																																																																																					
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																																																																																																																																												
Command	0	1	0	1	1	0	0	1	1	B3																																																																																																																																																																																												
1 st parameter	1	-	-	DPICC[1:0]	DPL	HSPL	VSPL	EPL	-																																																																																																																																																																																													
This command is used to set DPI interface related register.																																																																																																																																																																																																						
Description	EPL: Specify the polarity of DE pin in DPI interface mode.																																																																																																																																																																																																					
	<table border="1"> <thead> <tr> <th>EPL</th> <th>ENABLE pin</th> <th>Display</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Enable</td> </tr> <tr> <td>0</td> <td>1</td> <td>Disable</td> </tr> <tr> <td>1</td> <td>0</td> <td>Disable</td> </tr> <tr> <td>1</td> <td>1</td> <td>Enable</td> </tr> </tbody> </table>										EPL	ENABLE pin	Display	0	0	Enable	0	1	Disable	1	0	Disable	1	1	Enable																																																																																																																																																																													
EPL	ENABLE pin	Display																																																																																																																																																																																																				
0	0	Enable																																																																																																																																																																																																				
0	1	Disable																																																																																																																																																																																																				
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1	1	Enable																																																																																																																																																																																																				
VSPL: The polarity of VSYNC pin. When VSPL=0, the VSYNC pin is Low active. When VSPL=1, the VSYNC pin is High active.																																																																																																																																																																																																						
HSPL: The polarity of HSYNC pin. When HSPL=0, the HSYNC pin is Low active. When HSPL=1, the HSYNC pin is High active.																																																																																																																																																																																																						
DPL: The polarity of DCLK pin. When DPL=0, the data is read on the rising edge of DCLK signal. When DPL=1, the data is read on the falling edge of DCLK signal.																																																																																																																																																																																																						
DPICC: DPI Color mapping Configuration																																																																																																																																																																																																						
<table border="1"> <thead> <tr> <th>Register</th> <th>DB23</th><th>DB22</th><th>DB21</th><th>DB20</th><th>DB19</th><th>DB18</th><th>DB17</th><th>DB16</th><th>DB15</th><th>DB14</th><th>DB13</th><th>DB12</th><th>DB11</th><th>DB10</th><th>DB9</th><th>DB8</th><th>DB7</th><th>DB6</th><th>DB5</th><th>DB4</th><th>DB3</th><th>DB2</th><th>DB1</th><th>DB0</th> <th>DPICC</th> </tr> </thead> <tbody> <tr> <td>3Ah</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>R4</td><td>R3</td><td>R2</td><td>R1</td><td>R0</td><td>G5</td><td>G4</td><td>G3</td><td>G2</td><td>G1</td><td>G0</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td>2'b00</td></tr> <tr> <td rowspan="2">50h</td><td>x</td><td>x</td><td>x</td><td>R4</td><td>R3</td><td>R2</td><td>R1</td><td>R0</td><td>x</td><td>x</td><td>G5</td><td>G4</td><td>G3</td><td>G2</td><td>G1</td><td>G0</td><td>x</td><td>x</td><td>x</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td>2'b01</td></tr> <tr> <td>x</td><td>x</td><td>R4</td><td>R3</td><td>R2</td><td>R1</td><td>R0</td><td>x</td><td>x</td><td>x</td><td>G5</td><td>G4</td><td>G3</td><td>G2</td><td>G1</td><td>G0</td><td>x</td><td>x</td><td>x</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>x</td><td>2'b10</td></tr> <tr> <td rowspan="3">60h</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td><td>R5</td><td>R4</td><td>R3</td><td>R2</td><td>R1</td><td>R0</td><td>G5</td><td>G4</td><td>G3</td><td>G2</td><td>G1</td><td>G0</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td>2'b00</td></tr> <tr> <td>x</td><td>x</td><td>R5</td><td>R4</td><td>R3</td><td>R2</td><td>R1</td><td>R0</td><td>x</td><td>x</td><td>G5</td><td>G4</td><td>G3</td><td>G2</td><td>G1</td><td>G0</td><td>x</td><td>x</td><td>x</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td>2'b01</td></tr> <tr> <td colspan="10">70h</td><td>R7</td><td>R6</td><td>R5</td><td>R4</td><td>R3</td><td>R2</td><td>R1</td><td>R0</td><td>G7</td><td>G6</td><td>G5</td><td>G4</td><td>G3</td><td>G2</td><td>G1</td><td>G0</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td>2'b00</td></tr> </tbody> </table>											Register	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DPICC	3Ah	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	2'b00	50h	x	x	x	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	x	B4	B3	B2	B1	B0	2'b01	x	x	R4	R3	R2	R1	R0	x	x	x	G5	G4	G3	G2	G1	G0	x	x	x	B4	B3	B2	B1	x	2'b10	60h	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	2'b00	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	x	B5	B4	B3	B2	B1	B0	2'b01	70h										R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	2'b00
Register	DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DPICC																																																																																																																																																																													
3Ah	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0	2'b00																																																																																																																																																																														
50h	x	x	x	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	x	B4	B3	B2	B1	B0	2'b01																																																																																																																																																																													
	x	x	R4	R3	R2	R1	R0	x	x	x	G5	G4	G3	G2	G1	G0	x	x	x	B4	B3	B2	B1	x	2'b10																																																																																																																																																																													
60h	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0	2'b00																																																																																																																																																																														
	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	x	B5	B4	B3	B2	B1	B0	2'b01																																																																																																																																																																												
	70h										R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	2'b00																																																																																																																																																																			
Restrictions	SETEXTC turn on to enable this command.																																																																																																																																																																																																					
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Sleep In or Booster Off	Yes																																																																																																																																																																																																					

6.3.5 SETCYC: Set panel driving timing (B4h)

B4H	SETCYC(Set panel driving timing)																																													
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
Command	0	1	0	1	1	0	1	0	0	B4																																				
1 st parameter	1	ZZ_LR	ZZ_EO	NW_PE[2:0]			NW[2:0]			-																																				
2 nd parameter	1	USER_GIP_GATE[7:0]																																												
3 rd parameter	1	GIP_FR[1:0]		BLK_O SCSEL	-	STV_as _CK	-	-	GIP_FR _MODE	-																																				
4 th parameter	1	SHR0_3[3:0]					SHR0_2[3:0]			-																																				
5 th parameter	1	SHR0_1[3:0]					SHR0[11:8]			-																																				
6 th parameter	1	SHR0[7:0]																																												
7 th parameter	1	SHR1_3[3:0]					SHR1_2[3:0]			-																																				
8 th parameter	1	SHR1_1[3:0]					SHR1[11:8]			-																																				
9 th parameter	1	SHR1[7:0]																																												
10 th parameter	1	SHR2_3[3:0]					SHR2_2[3:0]			-																																				
11 th parameter	1	SHR2_1[3:0]					SHR2[11:8]			-																																				
12 th parameter	1	SHR2[7:0]																																												
13 th parameter	1	SHP[3:0]					SCP[3:0]			-																																				
14 th parameter	1	SPON[7:0]																																												
15 th parameter	1	SPOFF[7:0]																																												
16 th parameter	1	CHR[7:0]																																												
17 th parameter	1	CHP[3:0]					CCP[3:0]			-																																				
18 th parameter	1	CON[7:0]																																												
19 th parameter	1	COFF[7:0]																																												
20 th parameter	1	SON[7:0]																																												
21 th parameter	1	SOFF[7:0]																																												
22 th parameter	1	EQON2[7:0]																																												
23 th parameter	1	EQON1[7:0]																																												
24 th parameter	1	SPON_MPU[7:0]																																												
25 th parameter	1	SPOFF_MPU[7:0]																																												
26 th parameter	1	CON_MPU[7:0]																																												
27 th parameter	1	COFF_MPU[7:0]																																												
28 th parameter	1	SON_MPU[7:0]																																												
29 th parameter	1	SOFF_MPU[7:0]																																												
30 th parameter	1	EQON2_MPU[7:0]																																												
31 th parameter	1	EQON1_MPU[7:0]																																												
Description	This command is used to set display waveform cycles.																																													
	NW[2:0]: Inversion type setting. NW_PE[2:0]: Inversion type setting on idle mode.																																													
<table border="1"> <thead> <tr> <th>NW2</th> <th>NW1</th> <th>NW0</th> <th>Inversion type</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>Column inversion</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>1-dot inversion</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>2-dot inversion (1+2)</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>4-dot inversion</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>8-dot inversion</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> <td>Zig-zag inversion</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> <td>2-dot inversion (2+2)</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>Inhibited</td> </tr> </tbody> </table>											NW2	NW1	NW0	Inversion type	0	0	0	Column inversion	0	0	1	1-dot inversion	0	1	0	2-dot inversion (1+2)	0	1	1	4-dot inversion	1	0	0	8-dot inversion	1	0	1	Zig-zag inversion	1	1	0	2-dot inversion (2+2)	1	1	1	Inhibited
NW2	NW1	NW0	Inversion type																																											
0	0	0	Column inversion																																											
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0	1	0	2-dot inversion (1+2)																																											
0	1	1	4-dot inversion																																											
1	0	0	8-dot inversion																																											
1	0	1	Zig-zag inversion																																											
1	1	0	2-dot inversion (2+2)																																											
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Note 1: For details, please refer to chapter "5.3 Source driver".																																														
ZZ_EO: Zig-zag Odd / Even mode selection																																														
<table border="1"> <thead> <tr> <th>ZZ_EO</th> <th>Zig-zag Odd / Even mode selection</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>Odd-line shift</td> </tr> <tr> <td>1</td> <td>Even-line shift</td> </tr> </tbody> </table>											ZZ_EO	Zig-zag Odd / Even mode selection	0	Odd-line shift	1	Even-line shift																														
ZZ_EO	Zig-zag Odd / Even mode selection																																													
0	Odd-line shift																																													
1	Even-line shift																																													

ZZ_LR: Zig-zag Left / Right mode selection

ZZ_LR	Zig-zag Left / Right mode selection
1	S1~SDUM2
0	SDUM1~S1440

USER_GIP_Gate[7:0]: Set the GIP dummy clock numbers

GIP_FR[1:0]: GIP Frame (GIP signals only, no source data output) number control at mode D[1:0] = 01.

GIP_FR1	GIP_FR0	GIP frame number
0	0	1
0	1	2
1	0	3
1	1	4

STV_as_CK: Using STV[11:8] as CK output pins. Max CK output is 12.

STV_as_CK	STV[11:8]
0	Start / End pulse
1	Clock pulse

BLK_OSCSEL: Set clock source when blanking period

BLK_OSCSEL	Blanking Period clock source
0	Using internal clock
1	Using external clock

GIP_FR_MODE: GIP frame refresh mode. Set frame refresh period of GIP signal.

GIP_FR_MODE	GIP frame refresh mode
0	Each frame will refresh
1	Base on GIP_FR[1:0] setting

SHR0[11:0]: Set the Start signal delay from VSYNC falling edge.

SHR1[11:0]: Set the End signal delay from VSYNC falling edge.

SHR2[11:0]: Set the other group Start/End signal delay from VSYNC falling edge.

SHR0/SHR1/SHR2[11:0]	Start signal output delay
0x000h	1 x Hsync
0x001h	2 x Hsync
0x002h	3 x Hsync
0x003h	4 x Hsync
0x004h	5 x Hsync
0x005h	6 x Hsync
• • •	
0x3BFh	960 x Hsync
0x3C0h	961 x Hsync
0x3C1h	962 x Hsync
• • •	
0xFFEh	4095 x Hsync
0xFFFFh	4096 x Hsync

SHR0_1 / SHR1_1 / SHR2_1[3:0]: Set the 2nd Start / End signal delay from the 1st Start / End signal.

SHR0_2 / SHR1_2 / SHR2_2[3:0]: Set the 3rd Start / End signal delay from the 1st Start / End signal.

SHR0_3 / SHR1_3 / SHR2_3[3:0]: Set the 4th Start / End signal delay from the 1st Start / End signal.

SHR0_1 / SHR1_1 / SHR2_1[3:0]	2nd Start / End signal output delay
SHR0_2 / SHR1_2 / SHR2_2[3:0]	3th Start / End signal output delay
SHR0_3 / SHR1_3 / SHR2_3[3:0]	4th Start / End signal output delay
0000	1 x Hsync
0001	2 x Hsync
0010	3 x Hsync
.....
1110	15 x Hsync
1111	16 x Hsync

SCP[3:0]: Numbers of output Start and End signal.

SCP3	SCP2	SCP1	SCP0	Start and End numbers
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
.....
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

SHP[3:0]: Width of Start and End signal high pulse.

SHP3	SHP2	SHP1	SHP0	Start Pulse Width
0	0	0	0	1 x Hsync
0	0	0	1	2 x Hsync
0	0	1	0	3 x Hsync
.....
1	1	1	0	15 x Hsync
1	1	1	1	16 x Hsync

SPON[7:0]: Fine tune the Start and End signal delay from original starting point.

SPON[7:0]	Start / ENDsignal output start delay
0x00h	0 x OSC CLK
0x01h	4 x OSC CLK
0x02h	8 x OSC CLK
0x03h	12 x OSC CLK
.....
0xFEh	1016 OSC CLK
0xFFh	1020 OSC CLK

Note. When output Start / End signal width is 1- Hsync only, set SPON[7:0] < SPOFF[7:0]

SPOFF[7:0]: Fine tune the Start and End signal ending point.

SPON[7:0]	Start / END signal output end delay
0x00h	0 x OSC CLK
0x01h	4 x OSC CLK
0x02h	8 x OSC CLK
0x03h	12 x OSC CLK
0x04h	16 x OSC CLK
0x05h	20 x OSC CLK
.....
0xFEh	1016 x OSC CLK
0xFFh	1020 x OSC CLK

CHR[7:0]: Set the Clock signal delay from VSYNC falling edge.

CHR[7:0]	Clock signal output delay
0x00h	1 x HSYNC
0x01h	2 x HSYNC
0x02h	3 x HSYNC
0x03h	4 x HSYNC

0x04h	5 x HSYNC
0x05h	6 x HSYNC
• • •	
0xFEh	255 x HSYNC
0xFFh	256 x HSYNC

CCP[3:0]: Numbers of Output Clock signal.

CCP3	CCP2	CCP1	CCP0	Clock numbers
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
• • •				
1	1	1	0	15
1	1	1	1	16

CHP[3:0]: Width of Clock signal high pulse.

CHP3	CHP2	CHP1	CHP0	Clock signal width
0	0	0	0	1 x Hsync
0	0	0	1	2 x Hsync
0	0	1	0	3 x Hsync
0	0	1	1	4 x Hsync
• • •				
1	1	1	0	15 x Hsync
1	1	1	1	16 x Hsync

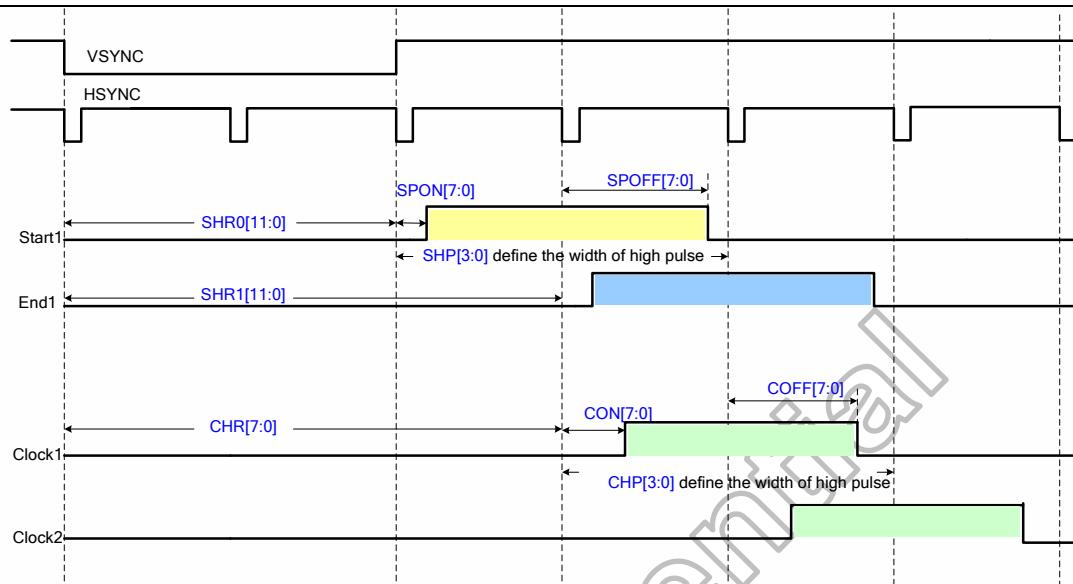
CON[7:0]: Fine tune the Clock signal delay from original starting point.

CON[7:0]	Clock signal output start delay
0x00h	0 x OSC CLK
0x01h	4 x OSC CLK
0x02h	8 x OSC CLK
0x03h	12 x OSC CLK
• • •	
0xFEh	1016 OSC CLK
0xFFh	1020 OSC CLK

Note. When output Clock signal width is 1- Hsync only, set COFF[7:0] \geq CON[7:0] + 2

COFF[7:0]: Fine tune the Start and End signal ending point.

COFF[7:0]	Clock signal output end delay
0x00h	0 x OSC CLK
0x01h	4 x OSC CLK
0x02h	8 x OSC CLK
0x03h	12 x OSC CLK
• • •	
0xFEh	1016 OSC CLK
0xFFh	1020 OSC CLK



SON[7:0]: Specify the valid source output start time.

(Please note that the EQON1[7:0] < SON[7:0] < SOFF[7:0] < EQON2[7:0])

SON[7:0]								Source output start time
0	0	0	0	0	0	0	0	0 OSC clock cycle
0	0	0	0	0	0	0	1	4 OSC clock cycle
0	0	0	0	0	0	1	0	8 OSC clock cycle
0	0	0	0	0	0	1	1	12 OSC clock cycle
0	0	0	0	0	1	0	0	16 OSC clock cycle
.....							
1	1	1	1	1	1	0	0	1008 OSC clock cycle
1	1	1	1	1	1	0	1	1012 OSC clock cycle
1	1	1	1	1	1	1	0	1016 OSC clock cycle
1	1	1	1	1	1	1	1	1020 OSC clock cycle

SOFF[7:0]: Specify the valid source output end time.

(Please note that the EQON1[7:0] < SON[7:0] < SOFF[7:0] < EQON2[7:0])

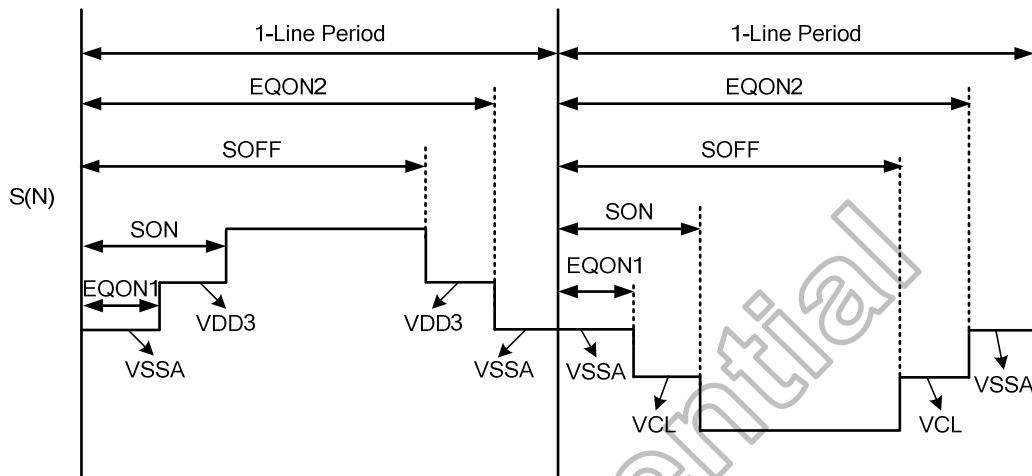
SOFF[7:0]								Source output end time
0	0	0	0	0	0	0	0	0 OSC clock cycle
0	0	0	0	0	0	0	1	4 OSC clock cycle
0	0	0	0	0	0	1	0	8 OSC clock cycle
0	0	0	0	0	0	1	1	12 OSC clock cycle
0	0	0	0	0	1	0	0	16 OSC clock cycle
.....							
1	1	1	1	1	1	0	0	1008 OSC clock cycle
1	1	1	1	1	1	0	1	1012 OSC clock cycle
1	1	1	1	1	1	1	0	1016 OSC clock cycle
1	1	1	1	1	1	1	1	1020 OSC clock cycle

EQON1/EQON2[7:0]: Specify the source EQ period.

(Please note that the EQON1[7:0] < SON[7:0] < SOFF[7:0] < EQON2[7:0])

EQON1/EQON2[7:0]								Source EQ Period
0	0	0	0	0	0	0	0	0 OSC clock cycle
0	0	0	0	0	0	0	1	4 OSC clock cycle
0	0	0	0	0	0	1	0	8 OSC clock cycle
0	0	0	0	0	0	1	1	12 OSC clock cycle
0	0	0	0	0	1	0	0	16 OSC clock cycle
.....							
1	1	1	1	1	1	0	0	1008 OSC clock cycle
1	1	1	1	1	1	0	1	1012 OSC clock cycle

1	1	1	1	1	1	1	0	1016 OSC clock cycle
1	1	1	1	1	1	1	1	1020 OSC clock cycle



SPON_MPU[7:0]: Specify MPU I/F timing
 SPOFF_MPU[7:0]: Specify MPU I/F timing
 CON_MPU[7:0]: Specify MPU I/F timing
 COFF_MPU[7:0]: Specify MPU I/F timing
 SON_MPU[7:0]: Specify MPU I/F timing
 SOFF_MPU[7:0]: Specify MPU I/F timing
 EQON2_MPU[7:0]: Specify MPU I/F timing
 EQON1_MPU[7:0]: Specify MPU I/F timing

Restrictions

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out		Yes
Sleep In or Booster Off		Yes

6.3.6 SET_Porch_Mode: Set Porch Mode (B5h)

B5 H	SETVPORCHMODE (Set Porch Mode)																					
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX												
Command	0	1	0	1	1	0	1	0	1	B6												
1 st parameter	1	-	RGB_VP[10:8]			-	-	-	Porch_Mode	-												
2 nd parameter	1	RGB_VP[7:0]							-													
3 rd parameter	1	RGB_HP[7:0]							-													
Description	This command is used to set Porch Mode. Porch_Mode: Set Porch mode at RGB I/F 0: DE mode, RGB interface will refer external DE signal to latch display data 1: Sync mode, RGB interface will use internal register setting to latch display data RGB_VP[10:0]: Define display data vertical latch point after VS falling edge. (VS+VBP) RGB_HP[7:0]: Define display data horizontal latch point after HS falling edge.(HS+HPB)																					
Restrictions	SETEXTC turn on to enable this command.																					
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes				
Status	Availability																					
Normal Mode On, Idle Mode Off, Sleep Out	Yes																					
Normal Mode On, Idle Mode On, Sleep Out	Yes																					
Sleep In or Booster Off	Yes																					

6.3.7 SETVCOM: Set VCOM voltage (B6h)

B6 H	SETVCOM (Set VCOM Voltage)											
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	0	1	0	1	1	0	1	1	0	B6		
1 st parameter	1	-	-	-	-	-	-	-	VCMC_F[8]	-		
2 nd parameter	1	VCMC_F[7:0]								-		
3 rd parameter	1	-	-	-	-	-	-	-	VCMC_B[8]	-		
4 th parameter	1	VCMC_B[7:0]								-		
5 th parameter	1	VCOM_TIMES[2:0]		-	-	-	-	-	-	-		
Description	This command is used to set VCOM Voltage. VCMC_F: VCOM voltage at forward scan VCMC_B: VCOM voltage at backward scan VCMC_F / VCMC_B[8:0]: Set DC VCOM voltage level.											
VCMC_F / VCMC_B[8:0]									VCOM (V)			
D8	D7	D6	D5	D4	D3	D2	D1	D0				
0	0	0	0	0	0	0	0	0	1.005			
0	0	0	0	0	0	0	0	1	0.990			
0	0	0	0	0	0	0	1	0	0.975			
0	0	0	0	0	0	0	1	1	0.960			
0	0	0	0	0	0	1	0	0	0.945			
0	0	0	0	0	0	1	0	1	0.930			
0	0	0	0	0	0	1	1	0	0.915			
0	0	0	0	0	0	1	1	1	0.900			
0	0	0	0	0	1	0	0	0	0.885			
0	0	0	0	0	1	0	0	1	0.870			
0	0	0	0	0	1	0	1	0	0.855			
0	0	0	0	0	1	0	1	1	0.840			
0	0	0	0	0	1	1	0	0	0.825			
0	0	0	0	0	1	1	0	1	0.810			
0	0	0	0	0	1	1	1	0	0.795			
0	0	0	0	0	1	1	1	1	0.780			
0	0	0	0	1	0	0	0	0	0.765			
0	0	0	0	1	0	1	0	1	0.750			
0	0	0	0	1	0	0	1	0	0.735			
0	0	0	0	1	0	0	1	1	0.720			
0	0	0	0	1	0	1	0	0	0.705			
0	0	0	0	1	0	1	0	1	0.690			
0	0	0	0	1	0	1	1	0	0.675			
0	0	0	0	1	0	1	1	1	0.660			
0	0	0	0	1	1	0	0	0	0.645			
0	0	0	0	1	1	1	0	0	0.630			
0	0	0	0	1	1	1	0	1	0.615			
0	0	0	0	1	1	1	0	1	0.600			
0	0	0	0	1	1	1	1	0	0.585			
0	0	0	0	1	1	1	0	1	0.570			
0	0	0	0	1	1	1	1	0	0.555			
0	0	0	0	1	1	1	1	1	0.540			
0	0	0	1	0	0	0	0	0	0.525			
0	0	0	1	0	0	0	0	1	0.510			
0	0	0	1	0	0	0	1	0	0.495			
0	0	0	1	0	0	0	1	1	0.480			
0	0	0	1	0	0	1	0	0	0.465			
0	0	0	1	0	0	1	0	1	0.450			
0	0	0	1	0	0	1	1	0	0.435			
0	0	0	1	0	0	1	1	1	0.420			
0	0	0	1	0	1	0	0	0	0.405			
0	0	0	1	0	1	0	0	0	0.390			
0	0	0	1	0	1	0	1	0	0.375			
0	0	0	1	0	1	0	1	1	0.360			
0	0	0	1	0	1	1	0	0	0.345			

0	0	0	1	0	1	1	0	1	0.330
0	0	0	1	0	1	1	1	0	0.315
0	0	0	1	0	1	1	1	1	0.300
0	0	0	1	1	0	0	0	0	0.285
0	0	0	1	1	0	0	0	1	0.270
0	0	0	1	1	0	0	1	0	0.255
0	0	0	1	1	0	0	1	1	0.240
0	0	0	1	1	0	1	0	0	0.225
0	0	0	1	1	0	1	0	1	0.210
0	0	0	1	1	0	1	1	0	0.195
0	0	0	1	1	0	1	1	1	0.180
0	0	0	1	1	1	0	0	0	0.165
0	0	0	1	1	1	0	0	1	0.150
0	0	0	1	1	1	0	1	0	0.135
0	0	0	1	1	1	0	1	1	0.120
0	0	0	1	1	1	1	0	0	0.105
0	0	0	1	1	1	1	0	1	0.090
0	0	0	1	1	1	1	1	0	0.075
0	0	0	1	1	1	1	1	1	0.060
0	0	1	0	0	0	0	0	0	0.045
0	0	1	0	0	0	0	0	1	0.030
0	0	1	0	0	0	0	1	0	0.015
0	0	1	0	0	0	0	1	1	0.000
0	0	1	0	0	0	1	0	0	-0.015
0	0	1	0	0	0	1	0	1	-0.030
0	0	1	0	0	0	1	1	0	-0.045
0	0	1	0	0	0	1	1	1	-0.060
0	0	1	0	0	1	0	0	0	-0.075
0	0	1	0	0	1	0	0	1	-0.090
0	0	1	0	0	1	0	1	0	-0.105
0	0	1	0	0	1	0	1	1	-0.120
0	0	1	0	0	1	1	0	0	-0.135
0	0	1	0	0	1	1	0	1	-0.150
0	0	1	0	0	1	1	1	0	-0.165
0	0	1	0	0	1	1	1	1	-0.180
0	0	1	0	1	0	0	0	0	-0.195
0	0	1	0	1	0	0	0	1	-0.210
0	0	1	0	1	0	0	1	0	-0.225
0	0	1	0	1	0	0	1	1	-0.240
0	0	1	0	1	0	1	0	0	-0.255
0	0	1	0	1	0	1	0	1	-0.270
0	0	1	0	1	0	1	1	0	-0.285
0	0	1	0	1	0	1	1	1	-0.300
0	0	1	0	1	1	0	0	0	-0.315
0	0	1	0	1	1	0	0	1	-0.330
0	0	1	0	1	1	0	1	0	-0.345
0	0	1	0	1	1	0	1	1	-0.360
0	0	1	0	1	1	1	0	0	-0.375
0	0	1	0	1	1	1	0	1	-0.390
0	0	1	0	1	1	1	1	0	-0.405
0	0	1	0	1	1	1	1	1	-0.420
0	0	1	1	0	0	0	0	0	-0.435
0	0	1	1	0	0	0	0	1	-0.450
0	0	1	1	0	0	0	1	0	-0.465
0	0	1	1	0	0	0	1	1	-0.480
0	0	1	1	0	0	1	0	0	-0.495
0	0	1	1	0	0	1	0	1	-0.510
0	0	1	1	0	0	1	1	0	-0.525
0	0	1	1	0	0	1	1	1	-0.540
0	0	1	1	0	1	0	0	0	-0.555
0	0	1	1	0	1	0	0	1	-0.570
0	0	1	1	0	1	0	1	0	-0.585
0	0	1	1	0	1	0	1	1	-0.600
0	0	1	1	0	1	1	0	0	-0.615
0	0	1	1	0	1	1	0	1	-0.630

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0	0	1	1	0	1	1	1	0	-0.645
0	0	1	1	0	1	1	1	1	-0.660
0	0	1	1	1	0	0	0	0	-0.675
0	0	1	1	1	0	0	0	1	-0.690
0	0	1	1	1	0	0	1	0	-0.705
0	0	1	1	1	0	0	1	1	-0.720
0	0	1	1	1	0	1	0	0	-0.735
0	0	1	1	1	0	1	0	1	-0.750
0	0	1	1	1	0	1	1	0	-0.765
0	0	1	1	1	0	1	1	1	-0.780
0	0	1	1	1	1	0	0	0	-0.795
0	0	1	1	1	1	0	0	1	-0.810
0	0	1	1	1	1	0	1	0	-0.825
0	0	1	1	1	1	0	1	1	-0.840
0	0	1	1	1	1	1	0	0	-0.855
0	0	1	1	1	1	1	0	1	-0.870
0	0	1	1	1	1	1	1	0	-0.885
0	0	1	1	1	1	1	1	1	-0.900
0	1	0	0	0	0	0	0	0	-0.915
0	1	0	0	0	0	0	0	1	-0.930
0	1	0	0	0	0	0	1	0	-0.945
0	1	0	0	0	0	0	1	1	-0.960
0	1	0	0	0	0	1	0	0	-0.975
0	1	0	0	0	0	1	0	1	-0.990
0	1	0	0	0	0	1	1	0	-1.005
0	1	0	0	0	0	1	1	1	-1.020
0	1	0	0	0	1	0	0	0	-1.035
0	1	0	0	0	1	0	0	1	-1.050
0	1	0	0	0	1	0	1	0	-1.065
0	1	0	0	0	1	0	1	1	-1.080
0	1	0	0	0	1	1	0	0	-1.095
0	1	0	0	0	1	1	0	1	-1.110
0	1	0	0	0	1	1	1	0	-1.125
0	1	0	0	0	1	1	1	1	-1.140
0	1	0	0	1	0	0	0	0	-1.155
0	1	0	0	1	0	0	0	1	-1.170
0	1	0	0	1	0	0	0	1	-1.185
0	1	0	0	1	0	0	1	1	-1.200
0	1	0	0	1	0	1	0	0	-1.215
0	1	0	0	1	0	1	0	1	-1.230
0	1	0	0	1	0	1	1	0	-1.245
0	1	0	0	1	0	1	1	1	-1.260
0	1	0	0	1	1	0	0	0	-1.275
0	1	0	0	1	1	0	0	1	-1.290
0	1	0	0	1	1	0	1	0	-1.305
0	1	0	0	1	1	0	1	1	-1.320
0	1	0	0	1	1	1	0	0	-1.335
0	1	0	0	1	1	1	0	1	-1.350
0	1	0	0	1	1	1	1	0	-1.365
0	1	0	0	1	1	1	1	1	-1.380
0	1	0	1	0	0	0	0	0	-1.395
0	1	0	1	0	0	0	0	1	-1.410
0	1	0	1	0	0	0	1	0	-1.425
0	1	0	1	0	0	0	1	1	-1.440
0	1	0	1	0	0	1	0	0	-1.455
0	1	0	1	0	0	1	0	1	-1.470
0	1	0	1	0	0	1	1	0	-1.485
0	1	0	1	0	0	1	1	1	-1.500
0	1	0	1	0	1	0	0	0	-1.515
0	1	0	1	0	1	0	0	1	-1.530
0	1	0	1	0	1	0	1	0	-1.545
0	1	0	1	0	1	0	1	1	-1.560
0	1	0	1	0	1	1	0	0	-1.575
0	1	0	1	0	1	1	1	0	-1.590
0	1	0	1	0	1	1	1	0	-1.605

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0	1	0	1	0	1	1	1	1	-1.620
0	1	0	1	1	0	0	0	0	-1.635
0	1	0	1	1	0	0	0	1	-1.650
0	1	0	1	1	0	0	1	0	-1.665
0	1	0	1	1	0	0	1	1	-1.680
0	1	0	1	1	0	1	0	0	-1.695
0	1	0	1	1	0	1	0	1	-1.710
0	1	0	1	1	0	1	1	0	-1.725
0	1	0	1	1	0	1	1	1	-1.740
0	1	0	1	1	1	0	0	0	-1.755
0	1	0	1	1	1	0	0	1	-1.770
0	1	0	1	1	1	0	1	0	-1.785
0	1	0	1	1	1	0	1	1	-1.800
0	1	0	1	1	1	1	0	0	-1.815
0	1	0	1	1	1	1	0	1	-1.830
0	1	0	1	1	1	1	1	0	-1.845
0	1	0	1	1	1	1	1	1	-1.860
0	1	1	0	0	0	0	0	0	-1.875
0	1	1	0	0	0	0	0	1	-1.890
0	1	1	0	0	0	0	1	0	-1.905
0	1	1	0	0	0	0	1	1	-1.920
0	1	1	0	0	0	1	0	0	-1.935
0	1	1	0	0	0	1	0	1	-1.950
0	1	1	0	0	0	1	1	0	-1.965
0	1	1	0	0	0	1	1	1	-1.980
0	1	1	0	0	1	0	0	0	-1.995
0	1	1	0	0	1	0	0	1	-2.010
0	1	1	0	0	1	0	1	0	-2.025
0	1	1	0	0	1	0	1	1	-2.040
0	1	1	0	0	1	1	0	0	-2.055
0	1	1	0	0	1	1	0	1	-2.070
0	1	1	0	0	1	1	1	0	-2.085
0	1	1	0	0	1	1	1	1	-2.100
0	1	1	0	1	0	0	0	0	-2.115
0	1	1	0	1	0	0	0	1	-2.130
0	1	1	0	1	0	1	0	1	-2.145
0	1	1	0	1	0	0	1	0	-2.160
0	1	1	0	1	0	1	0	0	-2.175
0	1	1	0	1	0	1	0	1	-2.190
0	1	1	0	1	0	1	1	0	-2.205
0	1	1	0	1	0	1	1	1	-2.220
0	1	1	0	1	1	0	0	0	-2.235
0	1	1	0	1	1	0	0	1	-2.250
0	1	1	0	1	1	0	1	0	-2.265
0	1	1	0	1	1	0	1	1	-2.280
0	1	1	0	1	1	1	0	0	-2.295
0	1	1	0	1	1	1	0	1	-2.310
0	1	1	0	1	1	1	1	0	-2.325
0	1	1	0	1	1	1	1	1	-2.340
0	1	1	1	0	0	0	0	0	-2.355
0	1	1	1	0	0	0	0	1	-2.370
0	1	1	1	0	0	0	1	0	-2.385
0	1	1	1	0	0	0	1	1	-2.400
0	1	1	1	0	0	1	0	0	-2.415
0	1	1	1	0	0	1	0	1	-2.430
0	1	1	1	0	0	1	1	0	-2.445
0	1	1	1	0	0	1	1	1	-2.460
0	1	1	1	0	1	0	0	0	-2.475
0	1	1	1	0	1	0	0	1	-2.490
0	1	1	1	0	1	0	1	0	-2.505
0	1	1	1	0	1	0	1	1	-2.520
0	1	1	1	0	1	1	0	0	-2.535
0	1	1	1	0	1	1	0	1	-2.550
0	1	1	1	0	1	1	1	0	-2.565
0	1	1	1	0	1	1	1	1	-2.580

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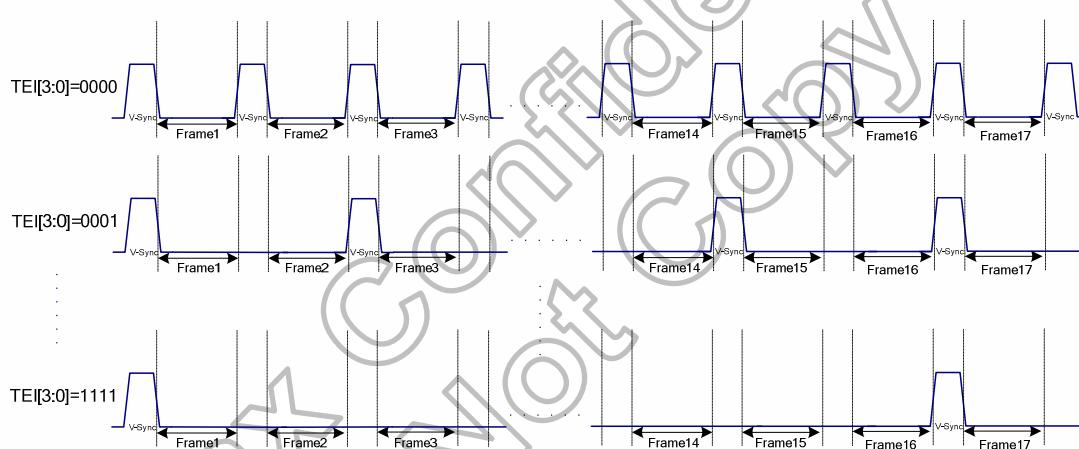
June, 2012

0	1	1	1	1	0	0	0	0	-2.595
0	1	1	1	1	0	0	0	1	-2.610
0	1	1	1	1	0	0	1	0	-2.625
0	1	1	1	1	0	0	1	1	-2.640
0	1	1	1	1	0	1	0	0	-2.655
0	1	1	1	1	0	1	0	1	-2.670
0	1	1	1	1	0	1	1	0	-2.685
0	1	1	1	1	0	1	1	1	-2.700
0	1	1	1	1	1	0	0	0	-2.715
0	1	1	1	1	1	0	0	1	-2.730
0	1	1	1	1	1	0	1	0	-2.745
0	1	1	1	1	1	0	1	1	-2.760
0	1	1	1	1	1	1	0	0	-2.775
0	1	1	1	1	1	1	0	1	-2.790
0	1	1	1	1	1	1	1	0	-2.805
0	1	1	1	1	1	1	1	1	-2.820
1	0	0	0	0	0	0	0	0	-2.835
1	0	0	0	0	0	0	0	1	-2.850
1	0	0	0	0	0	0	1	0	-2.865
1	0	0	0	0	0	0	1	1	-2.880
1	0	0	0	0	0	1	0	0	-2.895
1	0	0	0	0	0	1	0	1	-2.910
1	0	0	0	0	0	1	1	0	-2.925
1	0	0	0	0	0	1	1	1	-2.940
1	0	0	0	0	1	0	0	0	-2.955
1	0	0	0	0	1	0	0	1	-2.970
1	0	0	0	0	1	0	1	0	-2.985
1	0	0	0	0	1	0	1	1	-3.000
1	0	0	0	0	1	1	0	0	-3.015
1	0	0	0	0	1	1	0	1	-3.030
1	0	0	0	0	1	1	1	0	-3.045
1	0	0	0	0	1	1	1	1	-3.060
1	0	0	0	0	1	0	0	0	-3.075
1	0	0	0	0	1	0	0	1	-3.090
1	0	0	0	0	1	0	0	1	-3.105
1	0	0	0	0	1	0	0	1	-3.120
1	0	0	0	0	1	0	1	0	-3.135
1	0	0	0	0	1	0	1	0	-3.150
1	0	0	0	0	1	0	1	1	-3.165
1	0	0	0	0	1	0	1	1	-3.180
1	0	0	0	0	1	1	0	0	-3.195
1	0	0	0	0	1	1	0	0	-3.210
1	0	0	0	0	1	1	0	1	-3.225
1	0	0	0	0	1	1	0	1	-3.240
1	0	0	0	0	1	1	1	0	-3.255
1	0	0	0	0	1	1	1	0	-3.270
1	0	0	0	0	1	1	1	1	-3.285
1	0	0	0	0	1	1	1	1	-3.300
1	0	0	0	1	0	0	0	0	-3.315
1	0	0	1	0	0	0	0	1	-3.330
1	0	0	1	0	0	0	1	0	-3.345
1	0	0	1	0	0	0	1	1	-3.360
1	0	0	1	0	0	1	0	0	-3.375
1	0	0	1	0	0	1	0	1	-3.390
1	0	0	1	0	0	1	1	0	-3.405
1	0	0	1	0	0	1	1	1	-3.420
1	0	0	1	0	1	0	0	0	-3.435
1	0	0	1	0	1	0	0	1	-3.450
1	0	0	1	0	1	0	1	0	-3.465
1	0	0	1	0	1	0	1	1	-3.480
1	0	0	1	0	1	1	1	0	-3.495
1	0	0	1	0	1	1	1	0	-3.510
1_0010_1110 ~ 1_1111_1110									Inhibited
1_1111_1111									Hi-Z

	VCOM_TIMES[2:0]: Read the VCOM OTP programmed times.										
	<table border="1"> <thead> <tr> <th>VCOM_TIMES[2:0]</th><th>VCOM OTP Programmed Times</th></tr> </thead> <tbody> <tr> <td>111</td><td>No programmed</td></tr> <tr> <td>011</td><td>VCOM has been programmed 1 time</td></tr> <tr> <td>001</td><td>VCOM has been programmed 2 times</td></tr> <tr> <td>000</td><td>VCOM has been programmed 3 times</td></tr> </tbody> </table>	VCOM_TIMES[2:0]	VCOM OTP Programmed Times	111	No programmed	011	VCOM has been programmed 1 time	001	VCOM has been programmed 2 times	000	VCOM has been programmed 3 times
VCOM_TIMES[2:0]	VCOM OTP Programmed Times										
111	No programmed										
011	VCOM has been programmed 1 time										
001	VCOM has been programmed 2 times										
000	VCOM has been programmed 3 times										
Restrictions	SETEXTC turn on to enable this command.										
Register Availability	<table border="1"> <thead> <tr> <th>Status</th><th>Availability</th></tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr> <tr> <td>Sleep In or Booster Off</td><td>Yes</td></tr> </tbody> </table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes		
Status	Availability										
Normal Mode On, Idle Mode Off, Sleep Out	Yes										
Normal Mode On, Idle Mode On, Sleep Out	Yes										
Sleep In or Booster Off	Yes										

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6.3.8 SETTE: Set internal TE function (B7h)

B7H	SETTE (Set internal TE function)																																																																														
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																					
Command	0	1	0	1	1	0	1	1	1	B7																																																																					
1 st parameter	1	-	-	TE_SEL[1:0]		TEI[3:0]				-																																																																					
2 nd parameter	1	TEL_SEL[1:0]		TER_SEL[1:0]		-	TEP[10:8]			-																																																																					
3 rd parameter	1			TEP[7:0]						-																																																																					
Description	<p>TEI[3:0]: Set the output interval of TE signal according to the display data rewrite cycle and data transfer rate.</p> <table border="1"> <thead> <tr> <th>TEI3</th> <th>TEI2</th> <th>TEI1</th> <th>TEI0</th> <th>Output Interval</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1 frame</td> </tr> <tr> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>2 frames</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>3 frames</td> </tr> <tr> <td>...</td> <td>...</td> <td>...</td> <td>...</td> <td>...</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>0</td> <td>15 frames</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>16 frames</td> </tr> </tbody> </table>  <p>TEP[10:0]: Set the output position of frame cycle signal. TE can be used as the trigger signal for frame synchronous write operation. Make sure the setting restriction $11'h000 \leq \text{TEP}[10:0] \leq \text{Numbers of Line-1}$.</p> <table border="1"> <thead> <tr> <th>TEP[10:0]</th> <th>Output position</th> </tr> </thead> <tbody> <tr> <td>000h</td> <td>0th line</td> </tr> <tr> <td>001h</td> <td>1st line</td> </tr> <tr> <td>002h</td> <td>2nd line</td> </tr> <tr> <td>003h</td> <td>3rd line</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>3FEh</td> <td>1022th line</td> </tr> <tr> <td>3FFh</td> <td>1023th line</td> </tr> <tr> <td>400h</td> <td>1024th line</td> </tr> </tbody> </table> <p>TEL_SEL / TER_SEL[1:0]: Set the TE_L/TE_R pins output signal type.</p> <table border="1"> <thead> <tr> <th>TEL_SEL1/ TER_SEL1</th> <th>TEL_SEL0/ TER_SEL0</th> <th>TE / TER</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Normal DCS case, combine with CMD R35h Set_tear_on</td> </tr> <tr> <td>0</td> <td>1</td> <td>TE_VSYNC only</td> </tr> <tr> <td>1</td> <td>0</td> <td>TE_HSYNC only</td> </tr> <tr> <td>1</td> <td>1</td> <td>Source driving period (for touch sensor controller use)</td> </tr> </tbody> </table> <p>Restrictions</p> <p>SETEXTC turn on to enable this command.</p>	TEI3	TEI2	TEI1	TEI0	Output Interval	0	0	0	0	1 frame	0	0	0	1	2 frames	0	0	1	0	3 frames	1	1	1	0	15 frames	1	1	1	1	16 frames	TEP[10:0]	Output position	000h	0th line	001h	1 st line	002h	2 nd line	003h	3 rd line	3FEh	1022 th line	3FFh	1023 th line	400h	1024 th line	TEL_SEL1/ TER_SEL1	TEL_SEL0/ TER_SEL0	TE / TER	0	0	Normal DCS case, combine with CMD R35h Set_tear_on	0	1	TE_VSYNC only	1	0	TE_HSYNC only	1	1	Source driving period (for touch sensor controller use)										
TEI3	TEI2	TEI1	TEI0	Output Interval																																																																											
0	0	0	0	1 frame																																																																											
0	0	0	1	2 frames																																																																											
0	0	1	0	3 frames																																																																											
...																																																																											
1	1	1	0	15 frames																																																																											
1	1	1	1	16 frames																																																																											
TEP[10:0]	Output position																																																																														
000h	0th line																																																																														
001h	1 st line																																																																														
002h	2 nd line																																																																														
003h	3 rd line																																																																														
...	...																																																																														
3FEh	1022 th line																																																																														
3FFh	1023 th line																																																																														
400h	1024 th line																																																																														
TEL_SEL1/ TER_SEL1	TEL_SEL0/ TER_SEL0	TE / TER																																																																													
0	0	Normal DCS case, combine with CMD R35h Set_tear_on																																																																													
0	1	TE_VSYNC only																																																																													
1	0	TE_HSYNC only																																																																													
1	1	Source driving period (for touch sensor controller use)																																																																													

Register Availability	Status	Availability
	Normal Mode On, Idle Mode Off, Sleep Out	Yes
	Normal Mode On, Idle Mode On, Sleep Out	Yes
	Sleep In or Booster Off	Yes

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6.3.9 SETGPO: Set GPO (B8h)

B8H	SETGPO (Set GPO output function)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	0	1	1	1	0	0	0	B8								
1 st parameter	1		GPO1SEL[3:0]			GPO0SEL[3:0]				-								
2 nd parameter	1		GPO3SEL[3:0]			GPO2SEL[3:0]				-								
Description	This command is used to set GPOn pin output. <table border="1"> <tr> <td>GPOnSEL[3:0]</td> <td>Output signal</td> </tr> <tr> <td>0000</td> <td>No output</td> </tr> <tr> <td>0001</td> <td>Source driving period (for touch sensor controller use)</td> </tr> <tr> <td>Others</td> <td>Inhibited.</td> </tr> </table>										GPOnSEL[3:0]	Output signal	0000	No output	0001	Source driving period (for touch sensor controller use)	Others	Inhibited.
GPOnSEL[3:0]	Output signal																	
0000	No output																	
0001	Source driving period (for touch sensor controller use)																	
Others	Inhibited.																	
Restrictions	SETEXTC turn on to enable this command.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	

6.3.10 SETEXTC: Set extension command (B9h)

B9H	SETEXTC (Set extended command set)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	0	1	1	1	0	0	1	B9								
1 st parameter	1					EXTC1[7:0]				-								
2 nd parameter	1					EXTC2[7:0]				-								
3 rd parameter	1					EXTC3[7:0]				-								
Description	This command is used to set extended command set access enable. <table border="1"> <tr> <td>Extend cmd</td> <td>Command description</td> </tr> <tr> <td>Enable</td> <td>After command (B9h), must write 3 parameters (FFh, 83h, 79h) by order</td> </tr> <tr> <td>Disable(default)</td> <td>After command(B9h), write 3 parameters (xxh,xxh,xxh) any value is all right, but can not be (FFh, 83h, 79h)</td> </tr> </table>										Extend cmd	Command description	Enable	After command (B9h), must write 3 parameters (FFh, 83h, 79h) by order	Disable(default)	After command(B9h), write 3 parameters (xxh,xxh,xxh) any value is all right, but can not be (FFh, 83h, 79h)		
Extend cmd	Command description																	
Enable	After command (B9h), must write 3 parameters (FFh, 83h, 79h) by order																	
Disable(default)	After command(B9h), write 3 parameters (xxh,xxh,xxh) any value is all right, but can not be (FFh, 83h, 79h)																	
Restrictions	-																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	

6.3.11 SETOTP: Set OTP (BBh)

BBH	SETOTP(Set OTP Related Setting)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	0	1	1	1	0	1	1	BB								
1 st parameter	1					OTP_MASK[7:0]				-								
2 nd parameter		-	-	-	-	-	-	-	OTP_IN DEX[8]	-								
3 rd parameter	1				OTP_INDEX[7:0]					-								
4 th parameter	1	OTP_ LOAD_ DISABLE	OTP_ TEST	OTP_ POR	OTP_ PWE	OTP_PTM[1:0]	VPP_SEL (OTP_P WR_SEL)	OTP_ PROG		-								
5 th parameter	1				OTP_DATA[7:0]					-								
Description	This command is used to set OTP Related Setting. OTP_MASK[7:0]: Bit programming mask, if 1, means this bit can't be programmed. OTP_INDEX[8:0]: Set index of OTP table for programming. OTP_PROG: When set to 1, the register content of OTP index is programmed. VPP_SEL(OTP_PWR_SEL): When written to 1, OTP_PWR voltage is fed to OTP OTP_PTM[1:0]: For test mode enabling. OTP_PWE: OTP program write enable, if 1, means OTP is able to be programmed. OTP_POR: Pulse for OTP data read operation. OTP_TEST: "0", setting OTP_PROG high will trig internal state machine. "1", setting OTP_PROG high will not trig internal state machine. OTP_LOAD_DISABLE: Normally the internal registers are auto-loaded from OTP when the SLOUT command is received. Nevertheless, if this bit is set to 1, it will disable the auto loading function when the SLOUT command was received. In general, this bit is used when OTP is not yet programmed. OTP_DATA[7:0]: Read back the OTP index data.																	
Restrictions	SETEXTC turn on to enable this command.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	

6.3.12 SETDGCLUT: Set DGC LUT (C1h)

C1H	SETDGCLUT (Set DGC LUT)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	0	0	0	1	C1
1 st parameter	1	-	-	-	-	-	-	DITH_OPT	DGC_EN	-
2 nd parameter	1					D1[7:0]				-
:	1					Dn[7:0]				-
127 th parameter	1					D126[7:0]				-
Description	This command is used to set Digital Gamma Curve Look-Up Table.									
	DGC_EN: Enable the DGC function									
	DITH_OPT: No function.									
	D1[7:0] ~ D126[7:0]:									
	LUT	D7	D6	D5	D4	D3	D2	D1	D0	Default
	1 st	R00_9	R00_8	R00_7	R00_6	R00_5	R00_4	R00_3	R00_2	00h
	2 nd	R01_9	R01_8	R01_7	R01_6	R01_5	R01_4	R01_3	R01_2	08h
	3 rd	R02_9	R02_8	R02_7	R02_6	R02_5	R02_4	R02_3	R02_2	10h
	:	:	:	:	:	:	:	:	:	:
	32 th	R31_9	R31_8	R31_7	R31_6	R31_5	R31_4	R31_3	R31_2	F8h
	33 th	R32_9	R32_8	R32_7	R32_6	R32_5	R32_4	R32_3	R32_2	FFh
	34 th	R00_1	R00_0	R01_1	R01_0	R02_1	R02_0	R03_1	R03_0	00h
	35 th	R04_1	R04_0	R05_1	R05_0	R06_1	R06_0	R07_1	R07_0	00h
	:	:	:	:	:	:	:	:	:	:
	41 th	R28_1	R28_0	R29_1	R29_0	R30_1	R30_0	R31_1	R31_0	00h
	42 th	R32_1	R32_0	0	0	0	0	0	0	00h
	43 th	G00_9	G00_8	G00_7	G00_6	G00_5	G00_4	G00_3	G00_2	00h
	44 th	G01_9	G01_8	G01_7	G01_6	G01_5	G01_4	G01_3	G01_2	08h
	45 th	G02_9	G02_8	G02_7	G02_6	G02_5	G02_4	G02_3	G02_2	10h
	:	:	:	:	:	:	:	:	:	:
	74 th	G31_9	G31_8	G31_7	G31_6	G31_5	G31_4	G31_3	G31_2	F8h
	75 th	G32_9	G32_8	G32_7	G32_6	G32_5	G32_4	G32_3	G32_2	FFh
	76 th	G00_1	G00_0	G01_1	G01_0	G02_1	G02_0	G03_1	G03_0	00h
	77 th	G04_1	G04_0	G05_1	G05_0	G06_1	G06_0	G07_1	G07_0	00h
	:	:	:	:	:	:	:	:	:	:
	83 th	G28_1	G28_0	G29_1	G29_0	G30_1	G30_0	G31_1	G31_0	00h
	84 th	G32_1	G32_0	0	0	0	0	0	0	00h
	85 th	B00_9	B00_8	B00_7	B00_6	B00_5	B00_4	B00_3	B00_2	00h
	86 th	B01_9	B01_8	B01_7	B01_6	B01_5	B01_4	B01_3	B01_2	08h
	87 th	B02_9	B02_8	B02_7	B02_6	B02_5	B02_4	B02_3	B02_2	10h
	:	:	:	:	:	:	:	:	:	:
	116 th	B31_9	B31_8	B31_7	B31_6	B31_5	B31_4	B31_3	B31_2	F8h
	117 th	B32_9	B32_8	B32_7	B32_6	B32_5	B32_4	B32_3	B32_2	FFh
	118 th	B00_1	B00_0	B01_1	B01_0	B02_1	B02_0	B03_1	B03_0	00h
	119 th	B04_1	B04_0	B05_1	B05_0	B06_1	B06_0	B07_1	B07_0	00h
	:	:	:	:	:	:	:	:	:	:
	125 th	B28_1	B28_0	B29_1	B29_0	B30_1	B30_0	B31_1	B31_0	00h
	126 th	B32_1	B32_0	0	0	0	0	0	0	00h
Restrictions	SETEXTC turn on to enable this command.									
Register Availability	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				

6.3.13 SETID: Set ID (C3h)

C3H	SETID (Set ID)																		
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	0	1	1	0	0	0	0	1	1	C3									
1 st parameter	1					ID1[7:0]				-									
2 nd parameter	1					ID2[7:0]				-									
3 rd parameter	1					ID3[7:0]				-									
4 th parameter	1					ID4[7:0]				-									
5 th parameter	1		ID_TIMES[2:0]		-	-	-	-	-	-									
Description	ID1[7:0] is used to set ID RDAh value.																		
	ID2[7:0] is used to set ID RDBh value.																		
	ID3[7:0] is used to set ID RDCh value.																		
	ID4[7:0] is used to set the fourth ID.																		
	ID_TIMES[2:0]: Read the ID OTP programmed times.																		
	<table border="1"> <tr> <td>ID_TIMES[2:0]</td> <td>ID OTP Programmed Times</td> </tr> <tr> <td>111</td> <td>No programmed</td> </tr> <tr> <td>011</td> <td>ID has been programmed 1 time</td> </tr> <tr> <td>001</td> <td>ID has been programmed 2 times</td> </tr> <tr> <td>000</td> <td>ID has been programmed 3 times</td> </tr> </table>										ID_TIMES[2:0]	ID OTP Programmed Times	111	No programmed	011	ID has been programmed 1 time	001	ID has been programmed 2 times	000
ID_TIMES[2:0]	ID OTP Programmed Times																		
111	No programmed																		
011	ID has been programmed 1 time																		
001	ID has been programmed 2 times																		
000	ID has been programmed 3 times																		
Restrictions	SETEXTC turn on to enable this command.																		
Register Availability	<table border="1"> <tr> <th>Status</th> <th>Availability</th> </tr> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes	
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In or Booster Off	Yes																		

6.3.14 SETDDB: Set DDB (C4h)

C4H	SETDDB (Set DDB)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	1	0	0	0	1	0	0	C4								
1 st parameter	1					DDB1[7:0]				-								
2 nd parameter	1					DDB2[7:0]				-								
3 rd parameter	1					DDB3[7:0]				-								
4 th parameter	1					DDB4[7:0]				-								
Description	This command is used to set CMD RA1h DDB1~4 value.																	
Restrictions	SETEXTC turn on to enable this command.																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	

6.3.15 SETCABC: Set CABC control (C9h)

C9H	SETCABC (Set CABC Control)																																						
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																													
Command	0	1	1	0	0	1	0	0	1	C9																													
1 st Parameter	1	-		SEL_PWMCLK[2:0]		SEL_GAIN[1:0]		INVPULS	SEL_BLDU TY	-																													
2 nd Parameter	1			PWM_PERIOD[7:0]						-																													
3 rd Parameter	1	CABC_FSY NC			DIM_FRAME[6:0]					-																													
4 th Parameter	1			CABC_STEP[7:0]						-																													
5 th Parameter	1			CABC_CLKEN[7:0]						-																													
6 th Parameter	1	CABC_DD		SAVEPOWER[6:0]						-																													
7 th Parameter	1			MEAN_OFFSET[7:0]						-																													
8 th Parameter	1	-	-	-	-	CABC_FLM[3:0]				-																													
9 th Parameter	1	-	-	EN_DIM_M IX	EN_COST _MEAN	EN_COST	EN_NLN GAIN	EN_JUDG E	EN_TEMP	-																													
Description	<p>This command is used to set CABC parameter.</p> <p>SEL_BLDUTY: Backlight pwm output duty on/off control when CABC operation. '0', The Backlight pwm output duty is 100%. '1', The Backlight pwm output duty is calculate from CABC operation..</p> <p>INVPULS: The backlight PWM output polarity select. '0', The backlight PWM output is low level active. '1', The backlight PWM output is high level active.</p> <p>SEL_GAIN[1:0]: CABC gain select. Fixed value as 2'b11 in HX8379-A project.</p> <table border="1"> <thead> <tr> <th>SEL_GAIN[1:0]</th><th>Gain</th></tr> </thead> <tbody> <tr> <td>00</td><td>Use 1.00 as CABC calculate gain</td></tr> <tr> <td>01</td><td>Use 0.5x CABC calculate gain</td></tr> <tr> <td>10</td><td>Use 0.75x as CABC calculate gain</td></tr> <tr> <td>11</td><td>Use CABC calculate gain</td></tr> </tbody> </table> <p>SEL_PWMCLK[2:0] : Internal PWM_CLK divider for CABC clock.</p> <table border="1"> <thead> <tr> <th>SEL_PWMCLK[2:0]</th><th>Brightness Control Clock</th></tr> </thead> <tbody> <tr> <td>0 0 0</td><td>PWM_CLK / 1</td></tr> <tr> <td>0 0 1</td><td>PWM_CLK / 2</td></tr> <tr> <td>0 1 0</td><td>PWM_CLK / 4</td></tr> <tr> <td>0 1 1</td><td>PWM_CLK / 8</td></tr> <tr> <td>1 0 0</td><td>PWM_CLK / 16</td></tr> <tr> <td>1 0 1</td><td>PWM_CLK / 32</td></tr> <tr> <td>1 1 0</td><td>PWM_CLK / 64</td></tr> <tr> <td>1 1 1</td><td>PWM_CLK / 128</td></tr> </tbody> </table> <p>PWM_PERIOD[7:0]: The backlight PWM output period setting. Backlight PWM output period $=1 / [(PWM_CLK / \text{clock divider (SEL_PWMCLK)}) \times (255 \times (\text{PWM_PERIOD[7:0]} + 1))]$</p> <p>DIM_FRAME[6:0] : Manual brightness setting dimming period.</p> <p>CABC_FSYNC: Reset CABC_PWM_OUT signal by each VSYNC.</p> <p>CABC_STEP[7:0]: CABC step numbers during dimming period.</p> <p>CABC_CLKEN[7:0]: No function.</p> <p>SAVEPOWER[6:0] : Minimum CABC gain / maximum CABC duty output select. Fixed value as 7'b000_0000 in HX8379-A project.</p>											SEL_GAIN[1:0]	Gain	00	Use 1.00 as CABC calculate gain	01	Use 0.5x CABC calculate gain	10	Use 0.75x as CABC calculate gain	11	Use CABC calculate gain	SEL_PWMCLK[2:0]	Brightness Control Clock	0 0 0	PWM_CLK / 1	0 0 1	PWM_CLK / 2	0 1 0	PWM_CLK / 4	0 1 1	PWM_CLK / 8	1 0 0	PWM_CLK / 16	1 0 1	PWM_CLK / 32	1 1 0	PWM_CLK / 64	1 1 1	PWM_CLK / 128
SEL_GAIN[1:0]	Gain																																						
00	Use 1.00 as CABC calculate gain																																						
01	Use 0.5x CABC calculate gain																																						
10	Use 0.75x as CABC calculate gain																																						
11	Use CABC calculate gain																																						
SEL_PWMCLK[2:0]	Brightness Control Clock																																						
0 0 0	PWM_CLK / 1																																						
0 0 1	PWM_CLK / 2																																						
0 1 0	PWM_CLK / 4																																						
0 1 1	PWM_CLK / 8																																						
1 0 0	PWM_CLK / 16																																						
1 0 1	PWM_CLK / 32																																						
1 1 0	PWM_CLK / 64																																						
1 1 1	PWM_CLK / 128																																						

SAVEPOWER [6:0]							Min. Gain	Max. Duty
0	0	x	x	x	x	x	Reserve	
0	1	0	0	0	0	0	1+0/32	100%
0	1	0	0	0	0	1	1+1/32	96.97%
0	1	0	0	0	1	0	1+2/32	94.12%
0	1	0	0	0	1	1	1+3/32	91.43%
0	1	0	0	1	0	0	1+4/32	88.89%
0	1	0	0	1	0	1	1+5/32	86.49%
0	1	0	0	1	1	0	1+6/32	84.21%
0	1	0	0	1	1	1	1+7/32	82.05%
0	1	0	1	0	0	0	1+8/32	80%
0	1	0	1	0	0	1	1+9/32	78.05%
0	1	0	1	0	1	0	1+10/32	76.19%
0	1	0	1	0	1	1	1+11/32	74.42%
0	1	0	1	1	0	0	1+12/32	72.73%
0	1	0	1	1	0	1	1+13/32	71.11%
0	1	0	1	1	1	0	1+14/32	69.57%
0	1	0	1	1	1	1	1+15/32	68.09%
0	1	1	0	0	0	0	1+16/32	66.67%
0	1	1	0	0	0	1	1+17/32	65.31%
0	1	1	0	0	1	0	1+18/32	64%
0	1	1	0	0	1	1	1+19/32	62.75%
0	1	1	0	1	0	0	1+20/32	61.54%
0	1	1	0	1	0	1	1+21/32	60.38%
0	1	1	0	1	1	0	1+22/32	59.26%
0	1	1	0	1	1	1	1+23/32	58.18%
0	1	1	1	0	0	0	1+24/32	57.14%
0	1	1	1	0	0	1	1+25/32	56.14%
0	1	1	1	0	1	0	1+26/32	55.17%
0	1	1	1	0	1	1	1+27/32	54.24%
0	1	1	1	1	0	0	1+28/32	53.33%
0	1	1	1	1	0	1	1+29/32	52.46%
0	1	1	1	1	1	0	1+30/32	51.61%
0	1	1	1	1	1	1	1+31/32	50.79%
1	0	0	0	0	0	0	1+32/32	50%

For details, please refer to chapter "5.13.2 CABC Block".

CABC_DD: CABC dimming function enable bit.

'0', Disable CABC dimming.

'1', Enable CABC dimming.

MEAN_OFFSET[7:0]: Increase calculated frame mean. Fixed value as 8b'0000_0000 in HX8379-A project.

CABC_FLM[3:0]: CABC dimming frame number for each step. Fixed value as 4'b0001 in HX8379-A project.

EN_TEMP: Temporal weighting enable bit.

EN_JUDGE:

'0', Fix key value 35% to analysis image.

'1', Do not fix key value 35% to analysis image.

EN_NLN_GAIN: Non-linear gain enable bit.

EN_COST: Cost adjust enable bit.

EN_COST_MEAN: Histogram analysis mode (LR Ratio)

'0', mode 0.

	'1', mode 1. EN_DIX_MIX: No function.								
Restriction	SETEXTC turn on to enable this command.								
Register Availability	<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Booster Off</td><td>Yes</td></tr></tbody></table>	Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability								
Normal Mode On, Idle Mode Off, Sleep Out	Yes								
Normal Mode On, Idle Mode On, Sleep Out	Yes								
Sleep In or Booster Off	Yes								

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6.3.16 SETCABCGAIN (CAh)

CAH	SETCABCGAIN									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	1	0	1	0	CA
1 st Parameter	1	-				DBG0[6:0]				-
2 nd parameter	1	-				DBG1[6:0]				-
3 rd parameter	1	-				DBG2[6:0]				-
4 th parameter	1	-				DBG3[6:0]				-
5 th parameter	1	-				DBG4[6:0]				-
6 th parameter	1	-				DBG5[6:0]				-
7 th parameter	1	-				DBG6[6:0]				-
8 th parameter	1	-				DBG7[6:0]				-
9 th parameter	1	-				DBG8[6:0]				-
Description	DBG0~8[6:0] : Gain select register 0~8.									
	DBG0~8[6:0]							CABC Gain	CABC Duty	
	0	0	x	x	x	x	x	Reserve		
	0	1	0	0	0	0	0	1+0/32	100%	
	0	1	0	0	0	0	1	1+1/32	96.97%	
	0	1	0	0	0	1	0	1+2/32	94.12%	
	0	1	0	0	0	1	1	1+3/32	91.43%	
	0	1	0	0	1	0	0	1+4/32	88.89%	
	0	1	0	0	1	0	1	1+5/32	86.49%	
	0	1	0	0	1	1	0	1+6/32	84.21%	
	0	1	0	0	1	1	1	1+7/32	82.05%	
	0	1	0	1	0	0	0	1+8/32	80%	
	0	1	0	1	0	0	1	1+9/32	78.05%	
	0	1	0	1	0	1	0	1+10/32	76.19%	
	0	1	0	1	0	1	1	1+11/32	74.42%	
	0	1	0	1	1	0	0	1+12/32	72.73%	
	0	1	0	1	1	0	1	1+13/32	71.11%	
	0	1	0	1	1	1	0	1+14/32	69.57%	
	0	1	0	1	1	1	1	1+15/32	68.09%	
	0	1	1	0	0	0	0	1+16/32	66.67%	
	0	1	1	0	0	0	1	1+17/32	65.31%	
	0	1	1	0	0	1	0	1+18/32	64%	
	0	1	1	0	0	1	1	1+19/32	62.75%	
	0	1	1	0	1	0	0	1+20/32	61.54%	
	0	1	1	0	1	0	1	1+21/32	60.38%	
	0	1	1	0	1	1	0	1+22/32	59.26%	
	0	1	1	0	1	1	1	1+23/32	58.18%	
	0	1	1	1	0	0	0	1+24/32	57.14%	
	0	1	1	1	0	0	1	1+25/32	56.14%	
	0	1	1	1	0	1	0	1+26/32	55.17%	
	0	1	1	1	0	1	1	1+27/32	54.24%	
	0	1	1	1	1	0	0	1+28/32	53.33%	
	0	1	1	1	1	0	1	1+29/32	52.46%	
	0	1	1	1	1	1	0	1+30/32	51.61%	
	0	1	1	1	1	1	1	1+31/32	50.79%	
	1	0	0	0	0	0	0	1+32/32	50%	
Restrictions	For details, please refer to chapter "5.13.2 CABC Block".									
Register Availability	SETEXTC turn on to enable this command.									
	Status					Availability				
	Normal Mode On, Idle Mode Off, Sleep Out					Yes				
	Normal Mode On, Idle Mode On, Sleep Out					Yes				
	Sleep In or Booster Off					Yes				

6.3.17 SETCLOCK (CBh)

CBH	SETCLOCK									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	0	1	0	1	1	CB
1 st Parameter	1	-	-	-	-				UADJ[3:0]	-
2 nd parameter	1	-	-	-	-				UADJ_PE[3:0]	
Description	UADJ[3:0]: For user to adjust OSC frequency, default is 15 MHz. UADJ_PE[3:0]: For user to adjust OSC frequency in Idle mode, default is 15 MHz.									
	UADJ[3:0]/UADJ_PE[3:0]				Internal oscillator frequency					
	0	0	0	0						61.49%
	0	0	0	1						67.29%
	0	0	1	0						72.69%
	0	0	1	1						78.26%
	0	1	0	0						83.20%
	0	1	0	1						89.14%
	0	1	1	0						94.51%
	0	1	1	1						100.00%
	1	0	0	0						103.95%
	1	0	0	1						109.72%
	1	0	1	0						114.55%
	1	0	1	1						120.56%
	1	1	0	0						124.70%
	1	1	0	1						130.56%
	1	1	1	0						135.40%
	1	1	1	1						140.93%
Restrictions	SETEXTC turn on to enable this command									
Register Availability	Status				Availability					
	Normal Mode On, Idle Mode Off, Sleep Out				Yes					
	Normal Mode On, Idle Mode On, Sleep Out				Yes					
	Sleep In or Booster Off				Yes					

6.3.18 SETPANEL (CCh)

CCH	SETPANEL(Set panel related register)																		
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	0	1	1	0	0	1	1	0	0	CC									
1 st parameter	1	-	-	-	-	SS_ PANEL	GS_ PANEL	REV_ PANEL	BGR_ PANEL	-									
Description0	<p>This command is used to set setting of panel related register and make panel module meets below spec from viewpoint of user</p> <p>BGR_PANEL: The order of <R><G> dot color for module supplier, default value is stored in OTP. If color filter of panel is <G><R> type, setting BGR_PANEL = 1, if color filter of panel is <R><G> type, setting BGR_PANEL = 0. This bit is to make panel module look like a <R><G> type panel form the user viewpoint.</p> <p>REV_PANEL: The REV_PANEL setting is combined with HW_Pin NBWSEL to select the inversion of the display of all characters and graphics. This setting allows the display of the same data on both normally-white and normally-black panels.</p> <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td></td> <td>NBWSEL=1</td> <td>NBWSEL=0</td> </tr> <tr> <td>REV_PANEL = 0</td> <td>Normally-white panel</td> <td>Normally-black panel</td> </tr> <tr> <td>REV_PANEL = 1</td> <td>Normally-black panel</td> <td>Normally-white panel</td> </tr> </table> <p>GS_PANEL: Specify the shift direction of gate driver output. When GS_PANEL = 0, the panel control signal is normal scan. When GS_PANEL = 1, the panel control signal is reverse scan.</p> <p>SS_PANEL: Specify the shift direction of source driver output. When SS_PANEL = 0, the shift direction from S1 to S1440. When SS_PANEL = 1, the shift direction from S1440 to S1.</p>											NBWSEL=1	NBWSEL=0	REV_PANEL = 0	Normally-white panel	Normally-black panel	REV_PANEL = 1	Normally-black panel	Normally-white panel
	NBWSEL=1	NBWSEL=0																	
REV_PANEL = 0	Normally-white panel	Normally-black panel																	
REV_PANEL = 1	Normally-black panel	Normally-white panel																	
Restrictions	SETEXTC turn on to enable this command																		
Register Availability	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Status</th> <th style="text-align: center;">Availability</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode Off, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Normal Mode On, Idle Mode On, Sleep Out</td> <td style="text-align: center;">Yes</td> </tr> <tr> <td style="text-align: center;">Sleep In or Booster Off</td> <td style="text-align: center;">Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes	
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In or Booster Off	Yes																		

6.3.19 SETGIP (D5h)

D5H	SETGIP									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	0	1	0	1	0	1	D5
1 st parameter	1	-	-	-	-	PANEL_SEL[3:0]				
2 nd parameter	1	-	GIP_VS_EL	VGLO_SEL	LVGL_SEL	GIP_TYPE	-	GIP_MODE[1:0]		
3 rd parameter	1					Not Open				
4 th parameter	1					Not Open				
5 th parameter	1					Not Open				
6 th parameter	1					EQ_DELAY[7:0]				
7 th parameter	1	-	-	-	-		EQ_DELAY_HSYNC[3:0]			
8 th parameter	1					CGTS[15:8]				
9 th parameter	1					CGTS[7:0]				
10 th parameter	1		COS0_L[3:0] (CGOUT0_L)			COS0_R[3:0] (CGOUT0_R)				
11 th parameter	1		COS1_L[3:0] (CGOUT1_L)			COS1_R[3:0] (CGOUT1_R)				
12 th parameter	1		COS2_L[3:0] (CGOUT2_L)			COS2_R[3:0] (CGOUT2_R)				
13 th parameter	1		COS3_L[3:0] (CGOUT3_L)			COS3_R[3:0] (CGOUT3_R)				
14 th parameter	1		COS4_L[3:0] (CGOUT4_L)			COS4_R[3:0] (CGOUT4_R)				
15 th parameter	1		COS5_L[3:0] (CGOUT5_L)			COS5_R[3:0] (CGOUT5_R)				
16 th parameter	1		COS6_L[3:0] (CGOUT6_L)			COS6_R[3:0] (CGOUT6_R)				
17 th parameter	1		COS7_L[3:0] (CGOUT7_L)			COS7_R[3:0] (CGOUT7_R)				
18 th parameter	1		COS8_L[3:0] (CGOUT8_L)			COS8_R[3:0] (CGOUT8_R)				
19 th parameter	1		COS9_L[3:0] (CGOUT9_L)			COS9_R[3:0] (CGOUT9_R)				
20 th parameter	1		COS10_L[3:0] (CGOUT10_L)			COS10_R[3:0] (CGOUT10_R)				
21 st parameter	1		COS11_L[3:0] (CGOUT11_L)			COS11_R[3:0] (CGOUT11_R)				
22 nd parameter	1		COS12_L[3:0] (CGOUT12_L)			COS12_R[3:0] (CGOUT12_R)				
23 rd parameter	1		COS13_L[3:0] (CGOUT13_L)			COS13_R[3:0] (CGOUT13_R)				
24 th parameter	1		COS14_L[3:0] (CGOUT14_L)			COS14_R[3:0] (CGOUT14_R)				
25 th parameter	1		COS15_L[3:0] (CGOUT15_L)			COS15_R[3:0] (CGOUT15_R)				
26 th parameter	1		COS0_L_GS[3:0] (CGOUT0_L)			COS0_R_GS[3:0] (CGOUT0_R)				
27 th parameter	1		COS1_L_GS[3:0] (CGOUT1_L)			COS1_R_GS[3:0] (CGOUT1_R)				
28 th parameter	1		COS2_L_GS[3:0] (CGOUT2_L)			COS2_R_GS[3:0] (CGOUT2_R)				
29 th parameter	1		COS3_L_GS[3:0] (CGOUT3_L)			COS3_R_GS[3:0] (CGOUT3_R)				
30 th parameter	1		COS4_L_GS[3:0] (CGOUT4_L)			COS4_R_GS[3:0] (CGOUT4_R)				
31 th parameter	1		COS5_L_GS[3:0] (CGOUT5_L)			COS5_R_GS[3:0] (CGOUT5_R)				
32 th parameter	1		COS6_L_GS[3:0] (CGOUT6_L)			COS6_R_GS[3:0] (CGOUT6_R)				
33 th parameter	1		COS7_L_GS[3:0] (CGOUT7_L)			COS7_R_GS[3:0] (CGOUT7_R)				
34 th parameter	1		COS8_L_GS[3:0] (CGOUT8_L)			COS8_R_GS[3:0] (CGOUT8_R)				
35 th parameter	1		COS9_L_GS[3:0] (CGOUT9_L)			COS9_R_GS[3:0] (CGOUT9_R)				
36 th parameter	1		COS10_L_GS[3:0] (CGOUT10_L)			COS10_R_GS[3:0] (CGOUT10_R)				
37 th parameter	1		COS11_L_GS[3:0] (CGOUT11_L)			COS11_R_GS[3:0] (CGOUT11_R)				
38 th parameter	1		COS12_L_GS[3:0] (CGOUT12_L)			COS12_R_GS[3:0] (CGOUT12_R)				
39 th parameter	1		COS13_L_GS[3:0] (CGOUT13_L)			COS13_R_GS[3:0] (CGOUT13_R)				
40 th parameter	1		COS14_L_GS[3:0] (CGOUT14_L)			COS14_R_GS[3:0] (CGOUT14_R)				
41 th parameter	1		COS15_L_GS[3:0] (CGOUT15_L)			COS15_R_GS[3:0] (CGOUT15_R)				
42 th parameter	1				Not Open					
43 th parameter	1				Not Open					
44 th parameter	1				CGTS_INV[15:8]					
45 th parameter	1				CGTS_INV[7:0]					
46 th parameter	1				Not Open					
47 th parameter	1				Not Open					
Description	This command is used for the internal setting of GIP control signal output selection. PANEL_SEL[3:0]: Dummy register. GIP_MODE[1:0]: GIP EQ (pre-charge) type selection									

0	0	Both rising / falling EQ
0	1	Only rising edge EQ
1	0	Only falling edge EQ
1	1	EQ Off

GIP_TYPE: GIP EQ sequence selection.

GIP_TYPE	GIP EQ Sequence
0	VGL --> VSSA --> VGH --> VDD3/VSP/VSSA --> VGL
1	VGL --> VDD3/VSP/VSSA --> VGH --> VSSA --> VGL

Note. EQ voltage level VDD3 / VSP / VSSA is decided by GIP_VSEL[1:0]

LVGL_SEL: LVGL voltage selection.

LVGL_SEL	LVGL Voltage Selection
0	VGL
1	VGL_REG

VGLO_SEL: VGLO voltage selection.

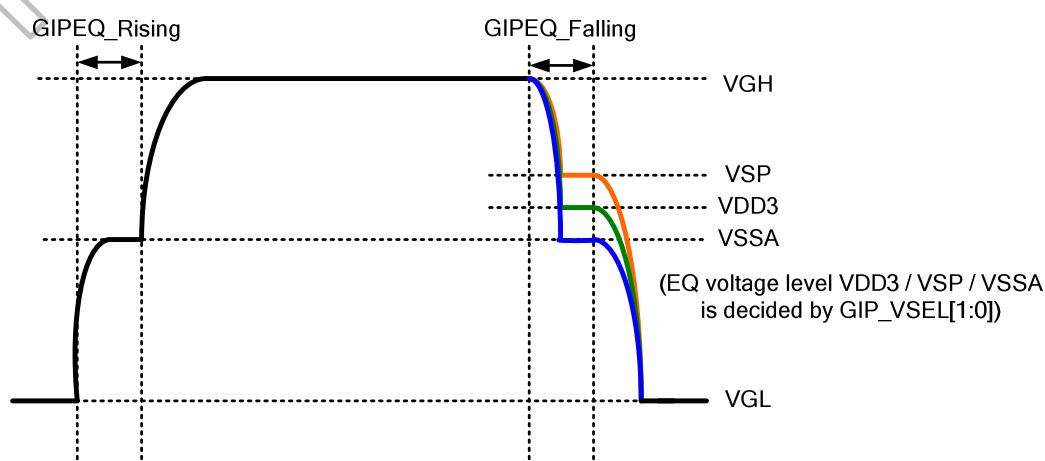
VGLO_SEL	VGLO Voltage Selection
0	VGL
1	VGL_REG

GIP_VSEL: GIP EQ Voltage Selection

GIP_VSEL[1]	GIP_VSEL[0]	GIP EQ Voltage Selection
0	0	EQ to VDD3
0	1	EQ to VSP
1	0	EQ to VSSA
1	1	Inhibited (Hi-Z)

EQ_DELAY[7:0]: Set GIP control signal EQ period

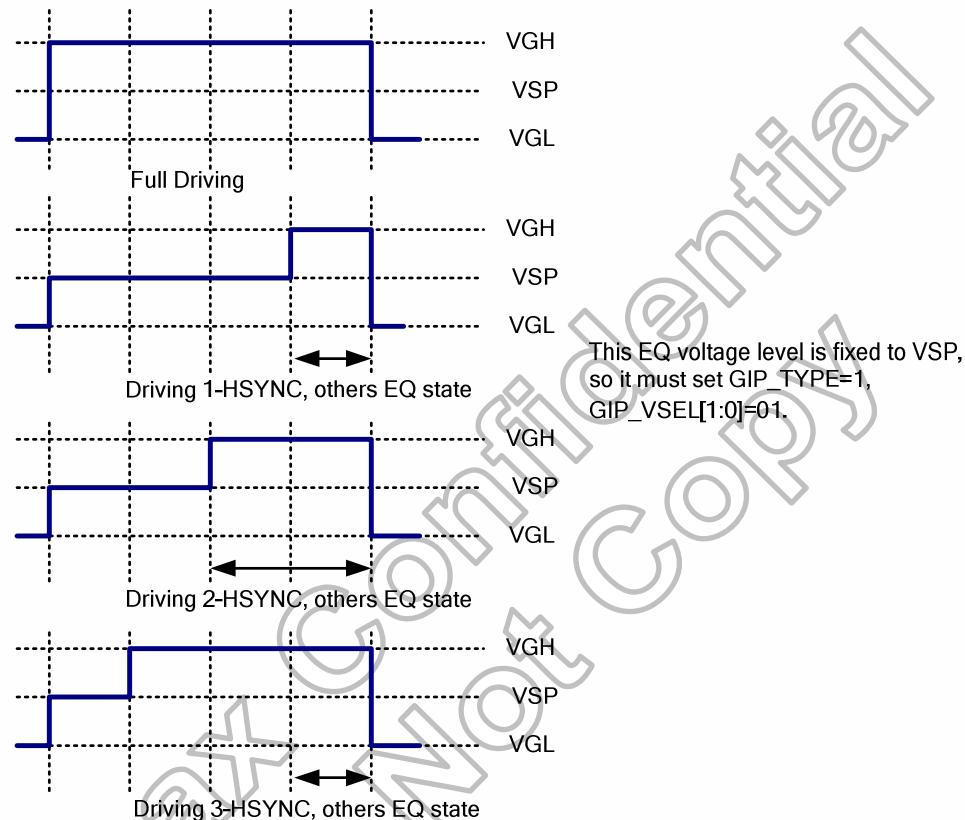
EQ_DELAY [7:0]								GIP EQ Period
0	0	0	0	0	0	0	0	0 OSC clock cycle
0	0	0	0	0	0	0	1	4 OSC clock cycle
0	0	0	0	0	0	1	0	8 OSC clock cycle
0	0	0	0	0	0	1	1	12 OSC clock cycle
0	0	0	0	0	1	0	0	16 OSC clock cycle
.....							
1	1	1	1	1	1	0	0	1008 OSC clock cycle
1	1	1	1	1	1	0	1	1012 OSC clock cycle
1	1	1	1	1	1	1	0	1016 OSC clock cycle
1	1	1	1	1	1	1	1	1020 OSC clock cycle



EQ_DELAY_HSYNC[3:0]: Set the EQ period in HSYNC width.

EQ_DELAY	EQ_DELAY	EQ_DELAY	EQ_DELAY	EQ Period in

HSYNC3	HSYNC2	HSYNC1	HSYNC0	HSYNC width
0	0	0	0	Normal Driving
0	0	0	1	1 x Hsync
0	0	1	0	2 x Hsync
0	0	1	1	3 x Hsync
.				
1	1	1	0	14 x Hsync
1	1	1	1	15 x Hsync



CGTS[15:0]: Select CGOUTn_L / R output, n=0~15

COSn_L[3:0]: Select CGOUTn_L output, n=0~15

COSn_R[3:0]: Select CGOUTn_R output, n=0~15

COSn_L GS[3:0]: When GS_Panel=1, select CGOUTn_L output, n=0~15

COSn_R GS[3:0]: When GS_Panel=1, select CGOUTn_R output, n=0~15

CGTS[n]	COSn_L[3:0]	Output Signal	Description
	COSn_R[3:0]		
	COSn_L GS[3:0]		
	COSn_R GS[3:0]		
0	0000	CK[0]	--
0	0001	CK[1]	--
0	0010	CK[2]	--
0	0011	CK[3]	--
0	0100	CK[4]	--
0	0101	CK[5]	--
0	0110	CK[6]	--
0	0111	CK[7]	--
0	1000	1'b0	--
0	1001	1'b1	--
1	0000	STV[0]	GROUP-0 SHR0[11:0]
1	0001	STV[1]	SHR0[11:0]+SHR0_1[3:0]
1	0010	STV[2]	SHR0[11:0]+SHR0_2[3:0]
1	0011	STV[3]	SHR0[11:0]+SHR0_3[3:0]

	1	0100	STV[4]	GROUP-1 SHR1[11:0]								
	1	0101	STV[5]	SHR1[11:0]+SHR1_1[3:0]								
	1	0110	STV[6]	SHR1[11:0]+SHR1_2[3:0]								
	1	0111	STV[7]	SHR1[11:0]+SHR1_3[3:0]								
	1	1000	1'b0	--								
	1	1001	STV[8]	GROUP-2 SHR2[11:0]								
	1	1010	STV[9]	SHR2[11:0]+SHR2_1[3:0]								
	1	1011	STV[10]	SHR2[11:0]+SHR2_2[3:0]								
	1	1100	STV[11]	SHR2[11:0]+SHR2_3[3:0]								
	Others		Reserved									
CGTS_INV[15:0]: CGTS_INV[n] set the corresponding signal CGOUTn_L / R output polarity, 0: Normal output 1: Invert output signal												
Restrictions	SETEXTC turn on to enable this command											
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>				Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability											
Normal Mode On, Idle Mode Off, Sleep Out	Yes											
Normal Mode On, Idle Mode On, Sleep Out	Yes											
Sleep In or Booster Off	Yes											

6.3.20 SETGAMMA: Set gamma curve related setting (E0h)

E0H	SETGAMMA (Set Gamma Curve Related Setting)									
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	1	1	0	0	0	0	0	E0
1 st Parameter	1					SETGAMMA_PASSWD[7:0]				
2 nd parameter	1	-	-			G1_VRP0[5:0]				-
3 rd parameter	1	-	-			G1_VRP1[5:0]				-
4 th parameter	1	-	-			G1_VRP2[5:0]				-
5 th parameter	1	-	-			G1_VRP3[5:0]				-
6 th parameter	1	-	-			G1_VRP4[5:0]				-
7 th parameter	1	-	-			G1_VRP5[5:0]				-
8 th parameter	1	-				G1_PRP0[6:0]				-
9 th parameter	1	-				G1_PRP1[6:0]				-
10 th parameter	1	-	-	-		G1_PKP0[4:0]				-
11 th parameter	1	-	-	-		G1_PKP1[4:0]				-
12 th parameter	1	-	-	-		G1_PKP2[4:0]				-
13 th parameter	1	-	-	-		G1_PKP3[4:0]				-
14 th parameter	1	-	-	-		G1_PKP4[4:0]				-
15 th parameter	1	-	-	-		G1_PKP5[4:0]				-
16 th parameter	1	-	-	-		G1_PKP6[4:0]				-
17 th parameter	1	-	-	-		G1_PKP7[4:0]				-
18 th parameter	1	-	-	-		G1_PKP8[4:0]				-
19 th parameter	1	-	-			G1_VRN0[5:0]				-
20 th parameter	1	-	-			G1_VRN1[5:0]				-
21 st parameter	1	-	-			G1_VRN2[5:0]				-
22 nd parameter	1	-	-			G1_VRN3[5:0]				-
23 rd parameter	1	-	-			G1_VRN4[5:0]				-
24 th parameter	1	-				G1_VRN5[5:0]				-
25 th parameter	1	-				G1_PRN0[6:0]				-
26 th parameter	1	-				G1_PRN1[6:0]				-
27 th parameter	1	-	-	-		G1_PKN0[4:0]				-
28 th parameter	1	-	-	-		G1_PKN1[4:0]				-
29 th parameter	1	-	-	-		G1_PKN2[4:0]				-
30 th parameter	1	-	-	-		G1_PKN3[4:0]				-
31 st parameter	1	-	-	-		G1_PKN4[4:0]				-
32 nd parameter	1	-	-	-		G1_PKN5[4:0]				-
33 rd parameter	1	-	-	-		G1_PKN6[4:0]				-
34 th parameter	1	-	-	-		G1_PKN7[4:0]				-
35 th parameter	1	-	-	-		G1_PKN8[4:0]				-
SETGAMMA_PASSWD[7:0]: Set as 79h to enable write Gamma register.										
Description	Register Groups	Positive Polarity	Negative Polarity	Description						
	Center Adjustment	PRP0 6-0	PRN0 6-0	Variable resistor (PRP/N0) for center adjustment						
		PRP1 6-0	PRN1 6-0	Variable resistor (PRP/N1)for center adjustment						
	Macro Adjustment	PKP0 4-0	PKN0 4-0	32-to-1 selector (voltage level of grayscale 3)						
		PKP1 4-0	PKN1 4-0	32-to-1 selector (voltage level of grayscale 7)						
		PKP2 4-0	PKN2 4-0	32-to-1 selector (voltage level of grayscale 19)						
		PKP3 4-0	PKN3 4-0	32-to-1 selector (voltage level of grayscale 25)						
		PKP4 4-0	PKN4 4-0	32-to-1 selector (voltage level of grayscale 32 for positive polarity and grayscale 31 for negative polarity)						
		PKP5 4-0	PKN5 4-0	32-to-1 selector (voltage level of grayscale 38)						
		PKP6 4-0	PKN6 4-0	32-to-1 selector (voltage level of grayscale 44)						
		PKP7 4-0	PKN7 4-0	32-to-1 selector (voltage level of grayscale 56)						
		PKP8 4-0	PKN8 4-0	32-to-1 selector (voltage level of grayscale 60)						

	Offset Adjustment	VRP0 5-0	VRN0 5-0	Variable resistor (VRP/N0)for offset adjustment								
		VRP1 5-0	VRN1 5-0	Variable resistor (VRP/N1)for offset adjustment								
		VRP2 5-0	VRN2 5-0	Variable resistor (VRP/N2)for offset adjustment								
		VRP3 5-0	VRN3 5-0	Variable resistor (VRP/N3)for offset adjustment								
		VRP4 5-0	VRN4 5-0	Variable resistor (VRP/N4)for offset adjustment								
		VRP5 5-0	VRN5 5-0	Variable resistor (VRP/N5)for offset adjustment								
Restriction	SETEXTC turn on to enable this command.											
Register Availability	<table border="1"><thead><tr><th>Status</th><th>Availability</th></tr></thead><tbody><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In or Booster Off</td><td>Yes</td></tr></tbody></table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes		
Status	Availability											
Normal Mode On, Idle Mode Off, Sleep Out	Yes											
Normal Mode On, Idle Mode On, Sleep Out	Yes											
Sleep In or Booster Off	Yes											

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6.3.21 SETCHEMODE_DYN (E4h)

E4H	SETCHEMODE_DYN (Set color enhancement mode, dynamic)																														
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX																					
Command	0	1	1	1	0	0	1	0	0	E4																					
1 st parameter	1	HUE_MODE [1:0]		SE_MODE [1:0]		BE_MODE [1:0]		CE_MODE[1:0]		-																					
2 nd parameter	1	-	-	-	-	-	-	-	DYN_CE_H_EN	-																					
Description	<p>This command is to set color enhancement in dynamic mode.</p> <p>CE_MODE [1:0]: Set image (saturation) enhancement in dynamic mode. BE_MODE [1:0]: Set brightness enhancement in dynamic mode. SE_MODE [1:0]: Set sharpness enhancement in dynamic mode. HUE_MODE[1:0]: Set image (hue) enhancement mode.</p> <p>Enhance effort selection. When HUE/SE/BE/CE turn on, their setting depend on register setting. It has three levels to select.</p> <table border="1"> <tr> <th>SE1/BE1/CE1/HUE1</th> <th>SE0/BE0/CE0/HUE0</th> <th>Enhance mode</th> </tr> <tr> <td>0</td> <td>0</td> <td>Off</td> </tr> <tr> <td>0</td> <td>1</td> <td>Low</td> </tr> <tr> <td>1</td> <td>0</td> <td>Medium</td> </tr> <tr> <td>1</td> <td>1</td> <td>High</td> </tr> </table> <p>DYN_CEH_EN: Select the color enhancement reload mode.</p> <table border="1"> <tr> <th>DYN_CEH_EN</th> <th>Color Enhancement Reload Mode</th> </tr> <tr> <td>0</td> <td>STA Mode</td> </tr> <tr> <td>1</td> <td>DYN Mode,</td> </tr> </table>										SE1/BE1/CE1/HUE1	SE0/BE0/CE0/HUE0	Enhance mode	0	0	Off	0	1	Low	1	0	Medium	1	1	High	DYN_CEH_EN	Color Enhancement Reload Mode	0	STA Mode	1	DYN Mode,
SE1/BE1/CE1/HUE1	SE0/BE0/CE0/HUE0	Enhance mode																													
0	0	Off																													
0	1	Low																													
1	0	Medium																													
1	1	High																													
DYN_CEH_EN	Color Enhancement Reload Mode																														
0	STA Mode																														
1	DYN Mode,																														
Restrictions	SETEXTC turn on to enable this command.																														
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes													
Status	Availability																														
Normal Mode On, Idle Mode Off, Sleep Out	Yes																														
Normal Mode On, Idle Mode On, Sleep Out	Yes																														
Sleep In or Booster Off	Yes																														

6.3.22 SETOTPKEY (E9h)

E9H	SETOTPKEY															
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX						
Command	0	1	1	1	0	1	0	0	1	E9						
1 st parameter	1				OTP_KEY0[7:0]					-						
2 nd parameter	1				OTP_KEY1[7:0]					-						
Description	This command is used to set OTP key to enter or leave OTP program mode.															
	OTP_KEY0[7:0], OTP_KEY1[7:0]	Description			Note											
	OTP_KEY0[7:0] = 0xAAh OTP_KEY1[7:0] = 0x55h	Enter OTP program mode			-											
	OTP_KEY0[7:0] = 0x00h OTP_KEY1[7:0] = 0x00h	Leave OTP program mode			-											
		Other value			Invalid											
Restrictions	SETEXTC turn on to enable this command.															
Register Availability	Status			Availability												
				Normal Mode On, Idle Mode Off, Sleep Out												
				Normal Mode On, Idle Mode On, Sleep Out												
				Sleep In or Booster Off												

6.3.23 SETCNCD/GETCNCD (FDh)

FDH	SETCNCD/GETCNCD (Set/Get Continue Command)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	1	1	1	1	1	0	1	FD								
1 st parameter	1	WR_CMD_CN[7:0]								-								
Description	This function is use to instead of Register-Content interface mode. The parameter for SETCNCD will continue to write or read from the last command address automatically.																	
Restrictions	SETEXTC turn on to enable this command																	
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>										Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes	Sleep In or Booster Off	Yes
Status	Availability																	
Normal Mode On, Idle Mode Off, Sleep Out	Yes																	
Normal Mode On, Idle Mode On, Sleep Out	Yes																	
Sleep In or Booster Off	Yes																	

6.3.24 SETREADINDEX: Set SPI Read Index (FEh)

FEH	SET SPI READ INDEX (Set SPI READ Command Address)																	
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX								
Command	0	1	1	1	1	1	1	1	0	FE								
1 st parameter	1	CMD_ADD[7:0]								-								
Description	SET SPI Read Command Address for User Define Command.																	
Restrictions	SETEXTC turn on to enable this command																	
Register Availability	Status	Availability																
	Normal Mode On, Idle Mode Off, Sleep Out	Yes																
	Normal Mode On, Idle Mode On, Sleep Out	Yes																
	Sleep In or Booster Off	Yes																

6.3.25 GETSPIREAD: SPI Read Command Data (FFh)

FFH	GETSPIREAD (Read Command Data)																		
	DCX	D7	D6	D5	D4	D3	D2	D1	D0	HEX									
Command	0	1	1	1	1	1	1	1	1	FF									
1 st parameter	1	CMD_DATA1[7:0]							-										
:	1	:							-										
n th parameter	1	CMD_DATA{n}[7:0]							-										
Description	Read SPI Command Data for User Define Command.																		
Restrictions	SETEXTC turn on to enable this command.																		
Register Availability	<table border="1"> <thead> <tr> <th>Status</th> <th>Availability</th> </tr> </thead> <tbody> <tr> <td>Normal Mode On, Idle Mode Off, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Normal Mode On, Idle Mode On, Sleep Out</td> <td>Yes</td> </tr> <tr> <td>Sleep In or Booster Off</td> <td>Yes</td> </tr> </tbody> </table>		Status	Availability	Normal Mode On, Idle Mode Off, Sleep Out	Yes	Normal Mode On, Idle Mode On, Sleep Out	Yes			Sleep In or Booster Off	Yes							
Status	Availability																		
Normal Mode On, Idle Mode Off, Sleep Out	Yes																		
Normal Mode On, Idle Mode On, Sleep Out	Yes																		
Sleep In or Booster Off	Yes																		

7. Layout Recommendation

7.1 Layout recommendation

7.1.1 Architecture 1 – internal charge pump

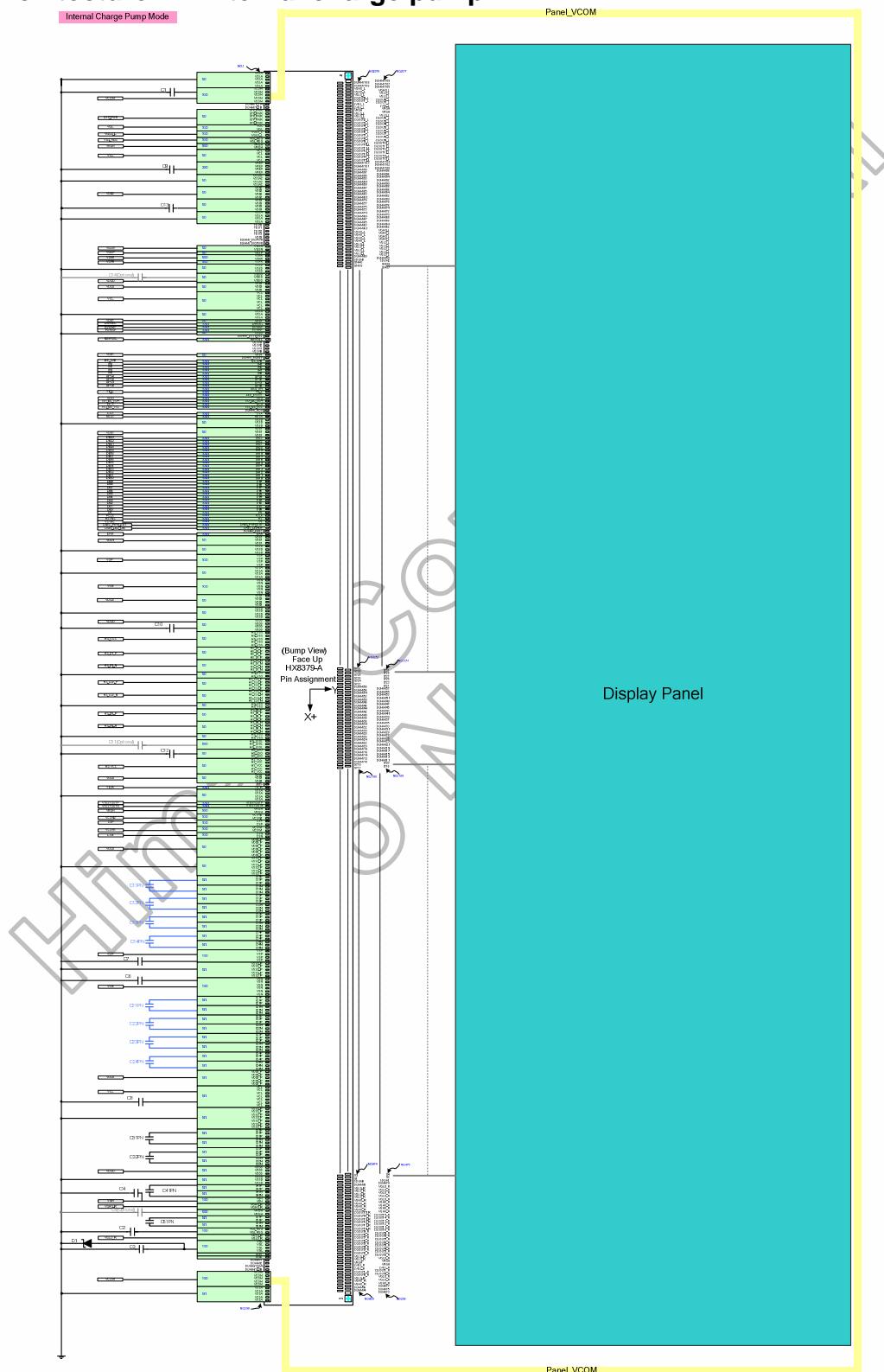


Figure 7.1: Power supply with internal charge pump

7.1.2 Architecture 2 – HX5186-A/B

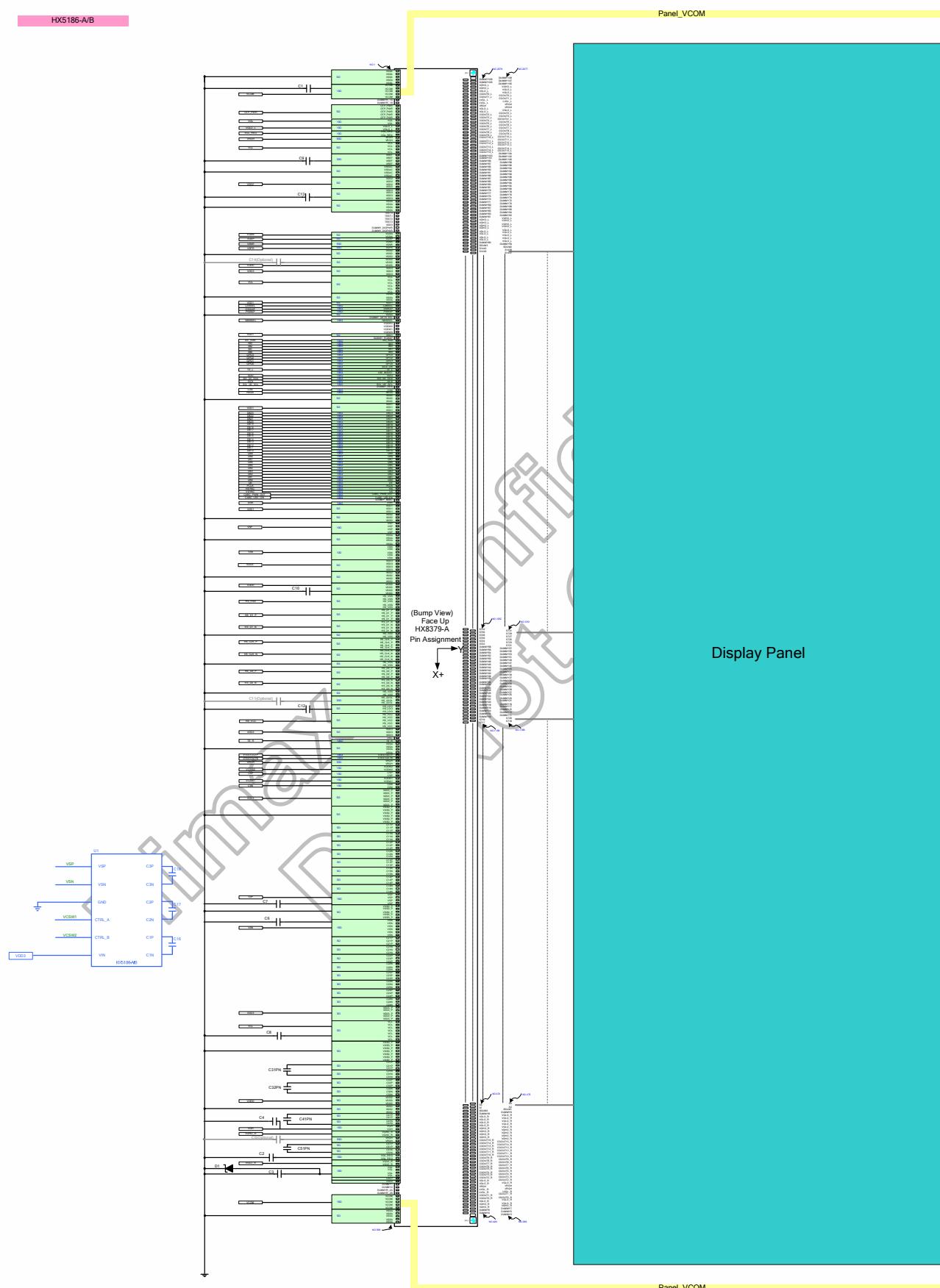


Figure 7.2: Power supply with HX5186-A/B

7.1.3 Architecture 3 – with PFM (Type C)

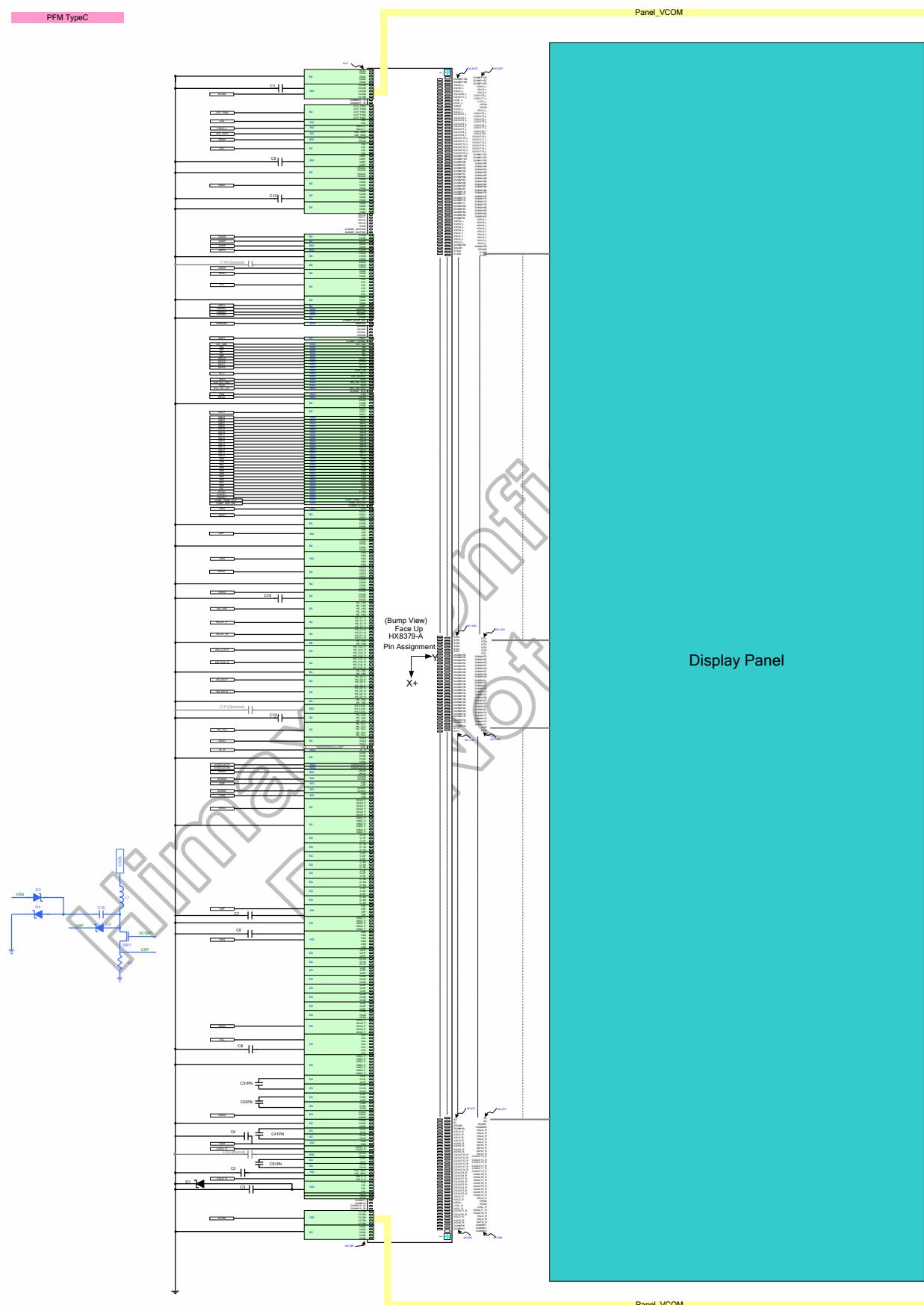


Figure 7.3: Power supply with PFM (Type C)

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7.1.4 Architecture 4 – VSN and VSP from external charge pump

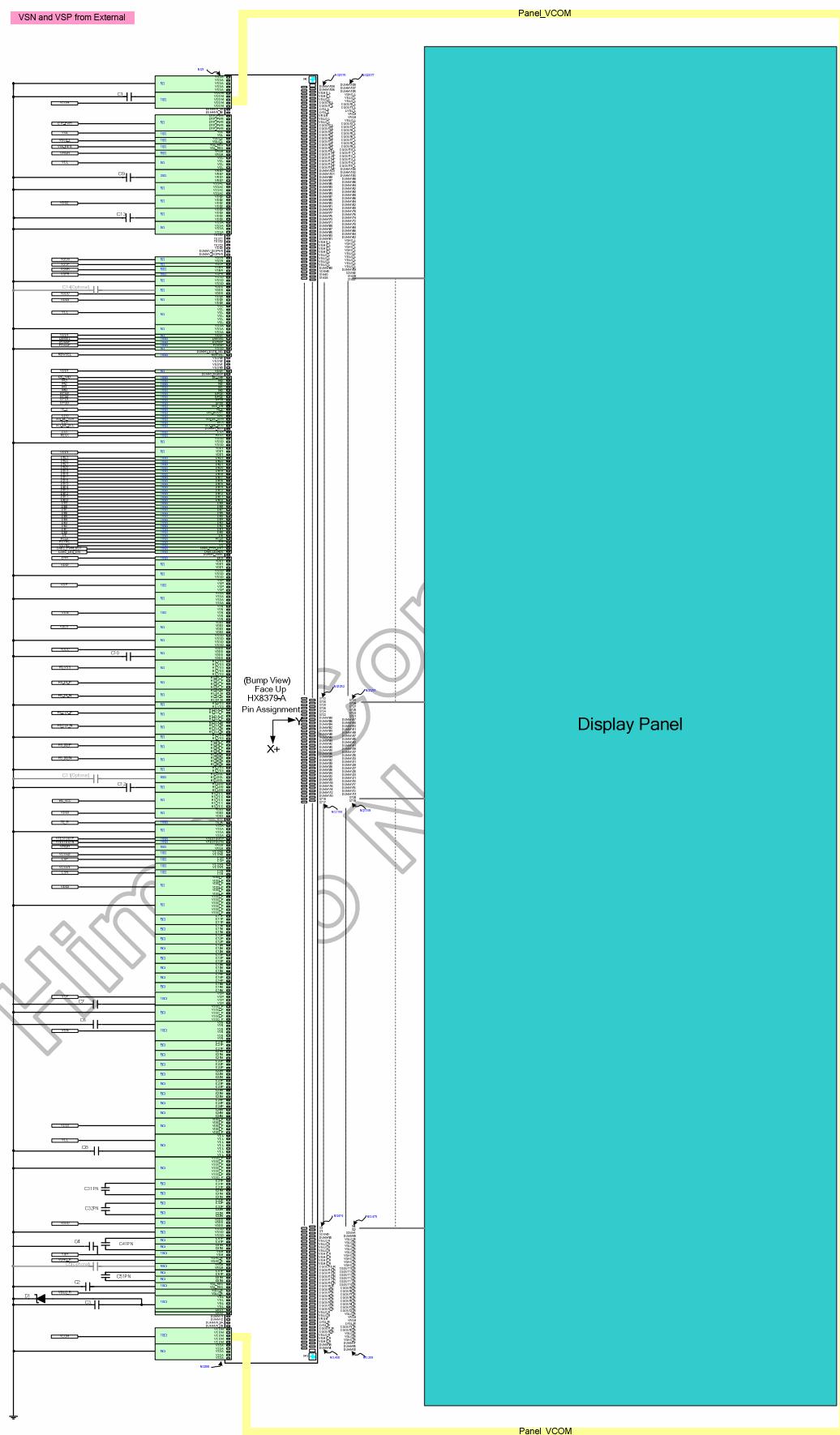


Figure 7.4: Power supply with VSN and VSP from external charge pump

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7.2 Maximum layout resistance

Name	Type	Maximum series resistance	Unit
VDD1	Power supply	5	Ω
VDD2	Power supply	5	Ω
VDD3, VDD3_P	Power supply	5	Ω
HS_VCC	Power supply	5	Ω
HS_VSS	Power supply	5	Ω
OTP_PWR	Power supply	5	Ω
VSSD, VSSD_P	Power supply	5	Ω
VSSA	Power supply	5	Ω
VSSAC	Power supply	20	Ω
IM[3:0]	Input	100	Ω
CSX, DCX, RESX, SCL_I2C_SCL	Input	100	Ω
HS, DE, VS, PCLK	Input	100	Ω
SDI_I2C_SDA	Input	100	Ω
SDO	Output	100	Ω
DB[23:0]	Input	100	Ω
NBWSEL	Input	100	Ω
GPO[3:0]	Output	100	Ω
CABC_PWM_OUT, CABC_LED_EN, TE_L, TE_R, IDLE_ON, LED_BOOST	Output	100	Ω
LED1,LED2	Output	10	Ω
VCOM	Output	10	Ω
HS_CLK_P, HS_CLK_N	Input	5	Ω
HS_D0P, HS_D0N	Input / Output	5	Ω
HS_D1P, HS_D1N,	Input	5	Ω
ERR	Output	100	Ω
DSWAP, PSWAP, LANSEL	Input	100	Ω
VDDD	Capacitor Connection	5	Ω
VCL	Capacitor Connection	10	Ω
VSP, VSN	Capacitor Connection	10	Ω
CSP,CSN	Input	10	Ω
VSPR, VSNR	Output	50	Ω
VGSP, VGSN	Output	50	Ω
VREF	Capacitor Connection	20	Ω
VGH, VGL, VGL_REG	Capacitor Connection	10	Ω
VRGH	Capacitor Connection	50	Ω
VGHO_L/R, VGLO_L/R, LVGL_L/R	Output	10	Ω
HS_LDO	Capacitor Connection	5	Ω
HS_LDOL	Output	50	Ω
OSC	Input	100	Ω
C11P, C11N, C12P, C12N, C13P, C13N, C14P, C14N, C21P, C21N, C22P, C22N, C23P, C23N, C24P, C24N, C31P, C31N, C32P, C32N, C41P, C41N, C51P, C51N	Capacitor Connection	5	Ω
VCSW1, VCSW2	Output	10	Ω
CGOUT0_L/R~CGOUT15_L/R	Output	10	Ω
TEST[3:0]	Input	100	Ω
VTESTOUTP, VTESTOUTN	Output	100	Ω

Table 7.1: Maximum layout resistance

7.3 External components connection

Internal charge pump mode:

Pad Name	Symbol	Connection	Typical Component Value
VCOM	C1	Connect to Capacitor (Max 6V): VCOM ---(-)--- --- (+)---- VSSA	2.2 μ F
VGL_REG	C2	Connect to Capacitor (Max 25V): VGL_REG ---(+)--- --- (-)---- VSSA (Optional)	1.0 μ F
VGL	D1	Connect to Schottky Diode(VR \geq 30V): VSSA ---(-)--- ◀--- (+)---- VGL (Optional)	VF < 0.4V / 20mA @ 25°C, VR \geq 30V (Recommended diode: RB521S-30)
	C3	Connect to Capacitor (Max 25V): VGL ---(+)--- --- (-)---- VSSA	2.2 μ F
VGH	C4	Connect to Capacitor (Max 25V): VGH ---(+)--- --- (-)---- VSSA	2.2 μ F
VRGH	C5	Connect to Capacitor (Max 25V): VRGH ---(+)--- --- (-)---- VSSA (Optional)	1.0 μ F
C11P – C11N	C11PN	Connect to Capacitor (Max 10V): C11P ---(+)--- --- (-)----C11N	1.0 μ F
C12P – C12N	C12PN	Connect to Capacitor (Max 10V): C12P ---(+)--- --- (-)----C12N	1.0 μ F
C13P – C13N	C13PN	Connect to Capacitor (Max 10V): C13P ---(+)--- --- (-)----C13N	1.0 μ F
C14P – C14N	C14PN	Connect to Capacitor (Max 10V): C14P ---(+)--- --- (-)----C14N	1.0 μ F
C21P – C21N	C21PN	Connect to Capacitor (Max 10V): C21P ---(+)--- --- (-)----C21N	1.0 μ F
C22P – C22N	C22PN	Connect to Capacitor (Max 10V): C22P ---(+)--- --- (-)----C22N	1.0 μ F
C23P – C23N	C23PN	Connect to Capacitor (Max 10V): C23P ---(+)--- --- (-)----C23N	1.0 μ F
C24P – C24N	C243PN	Connect to Capacitor (Max 10V): C24P ---(+)--- --- (-)----C24N	1.0 μ F
C31P – C31N	C31PN	Connect to Capacitor (Max 6V): C31P ---(+)--- --- (-)----C31N	1.0 μ F
C32P – C32N	C32PN	Connect to Capacitor (Max 6V): C32P ---(+)--- --- (-)----C32N	1.0 μ F
C41P – C41N	C41PN	Connect to Capacitor (Max 16V): C41P ---(+)--- --- (-)----C41N	1.0 μ F
C51P – C51N	C51PN	Connect to Capacitor (Max 16V): C51P ---(+)--- --- (-)----C51N	1.0 μ F
VSN	C6	Connect to Capacitor (Max 10V): VSN ---(+)--- --- (-)----VSSA	4.7 μ F
VSP	C7	Connect to Capacitor (Max 10V): VSP ---(+)--- --- (-)----VSSA	4.7 μ F
VCL	C8	Connect to Capacitor (Max 6V): VCL ---(-)--- --- (+)---- VSSA	2.2 μ F
VREF	C9	Connect to Capacitor (Max 6V): VREF ---(-)--- --- (+)---- VSSA	1.0 μ F
VDDD	C10	Connect to Capacitor (Max 6V): VDDD ---(+)--- --- (-)----VSSA	1.0 μ F
	C14	Connect to Capacitor (Max 6V): VDDD ---(+)--- --- (-)----VSSA (Option)	1.0 μ F
HS_LDOL	C11	Connect to Capacitor (Max 6V): HS_LDOL ---(+)--- --- (-)----HS_VSS (For MIPI DSI I/F, Optional)	1.0 μ F
HS_LDO	C12	Connect to Capacitor (Max 6V): HS_LDO ---(+)--- --- (-)----HS_VSS (For MIPI DSI I/F)	1.0 μ F
VDD3	C13	Connect to Capacitor (Max 6V): VDD3 ---(+)--- --- (-)----VSSA	1.0 μ F

Table 7.2: Adoptability of components (internal charge pump)

HX5186-A/B mode:

Pad Name	Symbol	Connection	Typical Component Value
VCOM	C1	Connect to Capacitor (Max 6V): VCOM ---(-)--- --- (+)--- VSSA	2.2 μ F
VGL_REG	C2	Connect to Capacitor (Max 25V): VGL_REG ---(+)- --- (-)--- VSSA (Optional)	1.0 μ F
VGL	D1	Connect to Schottky Diode(VR \geq 30V): VSSA ---(-)--- ◀--- (+)--- VGL (Optional)	VF < 0.4V / 20mA @ 25°C, VR \geq 30V (Recommended diode: RB521S-30)
	C3	Connect to Capacitor (Max 25V): VGL ---(+)- --- (-)--- VSSA	
VGH	C4	Connect to Capacitor (Max 25V): VGH ---(+)- --- (-)--- VSSA	2.4 μ F
VRGH	C5	Connect to Capacitor (Max 25V): VRGH ---(+)- --- (-)--- VSSA (Optional)	1.0 μ F
C31P – C31N	C31PN	Connect to Capacitor (Max 6V): C31P ---(+)- --- (-)--- C31N	1.0 μ F
C32P – C32N	C32PN	Connect to Capacitor (Max 6V): C32P ---(+)- --- (-)--- C32N	1.0 μ F
C41P – C41N	C41PN	Connect to Capacitor (Max 16V): C41P ---(+)- --- (-)--- C41N	1.0 μ F
C51P – C51N	C51PN	Connect to Capacitor (Max 16V): C51P ---(+)- --- (-)--- C51N	1.0 μ F
VSN	C6	Connect to Capacitor (Max 10V): VSN ---(+)- --- (-)--- VSSA	4.7 μ F
VSP	C7	Connect to Capacitor (Max 10V): VSP ---(+)- --- (-)--- VSSA	4.7 μ F
VCL	C8	Connect to Capacitor (Max 6V): VCL ---(-)--- --- (+)--- VSSA	2.2 μ F
VREF	C9	Connect to Capacitor (Max 6V): VREF ---(-)--- --- (+)--- VSSA	1.0 μ F
VDDD	C10	Connect to Capacitor (Max 6V): VDDD ---(+)- --- (-)--- VSSA	1.0 μ F
	C14	Connect to Capacitor (Max 6V): VDDD ---(+)- --- (-)--- VSSA (Option)	1.0 μ F
HS_LDOL	C11	Connect to Capacitor (Max 6V): HS_LDOL ---(+)- --- (-)--- HS_VSS (For MIPI DSI I/F, Optional)	1.0 μ F
HS_LDO	C12	Connect to Capacitor (Max 6V): HS_LDO ---(+)- --- (-)--- HS_VSS (For MIPI DSI I/F)	1.0 μ F
VDD3	C13	Connect to Capacitor (Max 6V): VDD3 ---(+)- --- (-)--- VSSA	1.0 μ F
HX5186-A/B	U1	Please refer HX5186-A/B datasheet	-
HX5186-A/B	C16	Please refer HX5186-A/B datasheet	1.0uF
HX5186-A/B	C17	Please refer HX5186-A/B datasheet	1.0uF
HX5186-A/B	C18	Please refer HX5186-A/B datasheet	1.0uF

Table 7.3: Adoptability of components (HX5186-A/B)

PFM Type C mode:

Pad Name	Symbol	Connection	Typical Component Value
VCOM	C1	Connect to Capacitor (Max 6V): VCOM ---(-)--- --- (+)--- VSSA	2.2 μ F
VGL_REG	C2	Connect to Capacitor (Max 25V): VGL_REG ---(+)--- --- (-)--- VSSA (Optional)	1.0 μ F
VGL	D1	Connect to Schottky Diode(VR \geq 30V): VSSA ---(-)--- \blacktriangleleft --- (+)--- VGL (Optional)	VF < 0.4V / 20mA @ 25°C, VR \geq 30V (Recommended diode: RB521S-30)
	C3	Connect to Capacitor (Max 25V): VGL ---(+)--- --- (-)--- VSSA	
VGH	C4	Connect to Capacitor (Max 25V): VGH ---(+)--- --- (-)--- VSSA	2.2 μ F
VRGH	C5	Connect to Capacitor (Max 25V): VRGH ---(+)--- --- (-)--- VSSA (Optional)	1.0 μ F
C31P – C31N	C31PN	Connect to Capacitor (Max 6V): C31P ---(+)--- --- (-)--- C31N	1.0 μ F
C32P – C32N	C32PN	Connect to Capacitor (Max 6V): C32P ---(+)--- --- (-)--- C32N	1.0 μ F
C41P – C41N	C41PN	Connect to Capacitor (Max 16V): C41P ---(+)--- --- (-)--- C41N	1.0 μ F
C51P – C51N	C51PN	Connect to Capacitor (Max 16V): C51P ---(+)--- --- (-)--- C51N	1.0 μ F
VSN	C6	Connect to Capacitor (Max 10V): VSN ---(+)--- --- (-)--- VSSA	4.7 μ F
VSP	C7	Connect to Capacitor (Max 10V): VSP ---(+)--- --- (-)--- VSSA	4.7 μ F
VCL	C8	Connect to Capacitor (Max 6V): VCL ---(-)--- --- (+)--- VSSA	2.2 μ F
VREF	C9	Connect to Capacitor (Max 6V): VREF ---(-)--- --- (+)--- VSSA	1.0 μ F
VDDD	C10	Connect to Capacitor (Max 6V): VDDD ---(+)--- --- (-)--- VSSA	1.0 μ F
	C14	Connect to Capacitor (Max 6V): VDDD ---(+)--- --- (-)--- VSSA (Option)	1.0 μ F
HS_LDOL	C11	Connect to Capacitor (Max 6V): HS_LDOL ---(+)--- --- (-)--- HS_VSS (For MIPI DSI I/F, Optional)	1.0 μ F
HS_LDO	C12	Connect to Capacitor (Max 6V): HS_LDO ---(+)--- --- (-)--- HS_VSS (For MIPI DSI I/F)	1.0 μ F
VDD3	C13	Connect to Capacitor (Max 6V): VDD3 ---(+)--- --- (-)--- VSSA	1.0 μ F
PFM	C16	Connect to Capacitor (Max 10V): L1 ---(+)--- --- (-)--- D2	1.0 μ F
PFM	D2	Connect to Schottky Diode(VR \geq 30V): VSP ---(-)--- \blacktriangleleft --- (+)--- L1/SW1	VF < 0.4V / 20mA @ 25°C, VR \geq 30V (Recommended diode: RB521S-30)
PFM	D3	Connect to Schottky Diode(VR \geq 30V): C16/D4 ---(-)--- \blacktriangleleft --- (+)--- VSN	
PFM	D4	Connect to Schottky Diode(VR \geq 30V): VSSA ---(-)--- \blacktriangleleft --- (+)--- C16/D3	
PFM	SW1	Connect to NMOS Switcher: VCSW1, D2/L1 and CSP	-
PFM	L1	Connect to inductor: VDD3/C13 and SW1/D2/C16	4.7 μ H
PFM	R1	Connect to resistor : CSP and VSSA	1 Ω

Table 7.4: Adoptability of components (PFM Type C)

VSN and VSP from External Charge Pump mode:

Pad Name	Symbol	Connection	Typical Component Value
VCOM	C1	Connect to Capacitor (Max 6V): VCOM ---(-)--- --- (+)--- VSSA	2.2 μ F
VGL_REG	C2	Connect to Capacitor (Max 25V): VGL_REG ---(+)--- --- (-)--- VSSA (Optional)	1.0 μ F
VGL	D1	Connect to Schottky Diode(VR \geq 30V): VSSA ---(-)--- \blacktriangleleft --- (+)--- VGL (Optional)	VF < 0.4V / 20mA @ 25°C, VR \geq 30V (Recommended diode: RB521S-30)
	C3	Connect to Capacitor (Max 25V): VGL ---(+)--- --- (-)--- VSSA	2.2 μ F
VGH	C4	Connect to Capacitor (Max 25V): VGH ---(+--- --- (-)--- VSSA	2.2 μ F
VRGH	C5	Connect to Capacitor (Max 25V): VRGH ---(+)--- --- (-)---VSSA (Optional)	1.0 μ F
C31P – C31N	C31PN	Connect to Capacitor (Max 6V): C31P ---(+)--- --- (-)---C31N	1.0 μ F
C32P – C32N	C32PN	Connect to Capacitor (Max 6V): C32P ---(+)--- --- (-)---C32N	1.0 μ F
C41P – C41N	C41PN	Connect to Capacitor (Max 16V): C41P ---(+)--- --- (-)---C41N	1.0 μ F
C51P – C51N	C51PN	Connect to Capacitor (Max 16V): C51P ---(+)--- --- (-)---C51N	1.0 μ F
VSN	C6	Connect to Capacitor (Max 10V): VSN ---(+)--- --- (-)---VSSA	4.7 μ F
VSP	C7	Connect to Capacitor (Max 10V): VSP ---(+)--- --- (-)---VSSA	4.7 μ F
VCL	C8	Connect to Capacitor (Max 6V): VCL ---(-)--- --- (+)--- VSSA	2.2 μ F
VREF	C9	Connect to Capacitor (Max 6V): VREF ---(-)--- --- (+)--- VSSA	1.0 μ F
VDDD	C10	Connect to Capacitor (Max 6V): VDDD ---(+)--- --- (-)---VSSA	1.0 μ F
	C14	Connect to Capacitor (Max 6V): VDDD ---(+)--- --- (-)---VSSA (Option)	1.0 μ F
HS_LDOL	C11	Connect to Capacitor (Max 6V): HS_LDOL ---(+)--- --- (-)---HS_VSS (For MIPI DSI I/F, Optional)	1.0 μ F
HS_LDO	C12	Connect to Capacitor (Max 6V): HS_LDO ---(+)--- --- (-)---HS_VSS (For MIPI DSI I/F)	1.0 μ F
VDD3	C13	Connect to Capacitor (Max 6V): VDD3 ---(+)--- --- (-)---VSSA	1.0 μ F

Table 7.5: Adoptability of components (VSN and VSP from external charge pump)

8. Electrical Characteristics

8.1 Absolute maximum ratings

The absolute maximum ratings are listed on Table 8.1. When used out of the absolute maximum ratings, the LSI may be permanently damaged. Using the LSI within the following electrical characteristics limit is strongly recommended for normal operation. If these electrical characteristic conditions are exceeded during normal operation, the LSI will malfunction and cause poor reliability.

Item	Symbol	Unit	Value	Note
Power Supply Voltage 1	VDD1~VSSD	V	-0.3 to +4.4	Note ^{(1),(2)}
Power Supply Voltage 2	VDD2~VSSA	V	-0.3 to +6.0	Note ^{(1),(3)}
Power Supply Voltage 3	VDD3~VSSA	V	-0.3 to +6.0	Note ^{(1),(4)}
Power Supply Voltage 4	HS_VCC ~ HS_VSS	V	-0.3 to +6.0	Note ^{(1),(5)}
Power Supply Voltage 5	VSP~VSSA	V	-0.3 to +6.6	Note ⁽⁶⁾
Power Supply Voltage 6	VSSA~VSN	V	0 to -6.6	Note ⁽⁷⁾
Power Supply Voltage 7	VGH~VSSA	V	-0.3 to +25	Note ⁽⁸⁾
Power Supply Voltage 8	VSSA~VGL	V	0 to -18	Note ⁽⁹⁾
Operating Temperature	Topr	°C	-40 to +85	Note ⁽¹⁰⁾
Storage Temperature	Tstg	°C	-55 to +110	Note ⁽¹¹⁾
Input Voltage	V _{IN}	V	-0.3 to VDD1+0.3	Note ⁽¹²⁾
HS Input Voltage	V _{HSIN}	V	-0.3 to +2	Note ⁽¹³⁾

Note: (1) VDD1, VSSD must be maintained.

(2) To make sure $VDD1 \geq VSSD$.

(3) To make sure $VDD2 \geq VSSA$.

(4) To make sure $VDD3 \geq VSSA$.

(5) To make sure $HS_VCC \geq HS_VSS$.

(6) To make sure $VSP \geq VSSA$.

(7) To make sure $VSSA \geq VSN$.

(8) To make sure $VGH \geq VSSA$.

(9) To make sure $VSSA \geq VGL$, $VGH + |VGL| < 30V$

(10) For die and wafer products, specified up to +85°C.

(11) This temperature specifications apply to the TCP package.

(12) This specifications include input signals but without following: HS_CLK_P, HS_CLK_N, HS_D0P, HS_D0N, HS_D1P, HS_D1N.

(13) This specifications include following signals: HS_CLK_P, HS_CLK_N, HS_D0P, HS_D0N, HS_D1P, HS_D1N.

Table 8.1: Absolute maximum rating

8.2 DC characteristics

(VDD2=2.3 ~ 5.5V, VDD3=2.3 ~ 5.5V, VDD1=1.65~3.6V, TA=-40 ~ 85 °C)

Item	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input high voltage	V _{IH}	VDD1= 1.65 ~ 3.6V VDD2= 2.3 ~ 5.5V VDD3= 2.3 ~ 5.5V	0.7 V _{DD1}	-	VDD1	V
Input low voltage	V _{IL}		0	-	0.3 V _{DD1}	V
OTP_PWR	V _{IH}	OTP_PWR	7.25V	7.5V	7.75V	V
	V _{IL}					
Output high voltage (SDO, CABC_PWM_OUT, CABA_LED_EN, IDLE_ON, LED_BOOST)	V _{OH1}	I _{OH} = -1.0 mA	0.8 V _{DD1}	-	VDD1	V
Output low voltage (SDO, CABC_PWM_OUT, CABC_LED_EN, IDLE_ON, LED_BOOST)	V _{OL1}	VDD1= 1.65 ~ 3.6V I _{OL} = 1.0 mA	0	-	0.2 V _{DD1}	V
Logic High level input current	I _{IH}	VSYNC, HSYNC	-	-	1	μF
		RESX, DCX, CSX, SCL	-	-	1	μF
	I _{IHD}	DB[23:0], SDI, DCX	-	-	1	μF
		DB[23:0]	-	-	1	μF
Logic Low level input current	I _{IL}	VSYNC, HSYNC	-1	-		μF
		RESX, DCX, CSX, SCL	-1	-		μF
	I _{ILD}	DB[23:0], SDI, DCX	-1	-		μF
		DB[23:0]	-1	-		μF
Current consumption standby mode (VDD2/VDD3-VSSD)	I _{ST(VDD)}	VDD2/VDD3=2.8V, VDD1=1.8V TA=25°C	-	TBD		μF
Current consumption standby mode (VDD1-VSSD)	I _{ST(VDD1)}		-	TBD	-	μF

Note: The VPP pin is open on normal mode and in used while OTP programming condition.

Table 8.2: DC characteristic

8.3 AC characteristics

8.3.1 DBI Type C interface characteristics

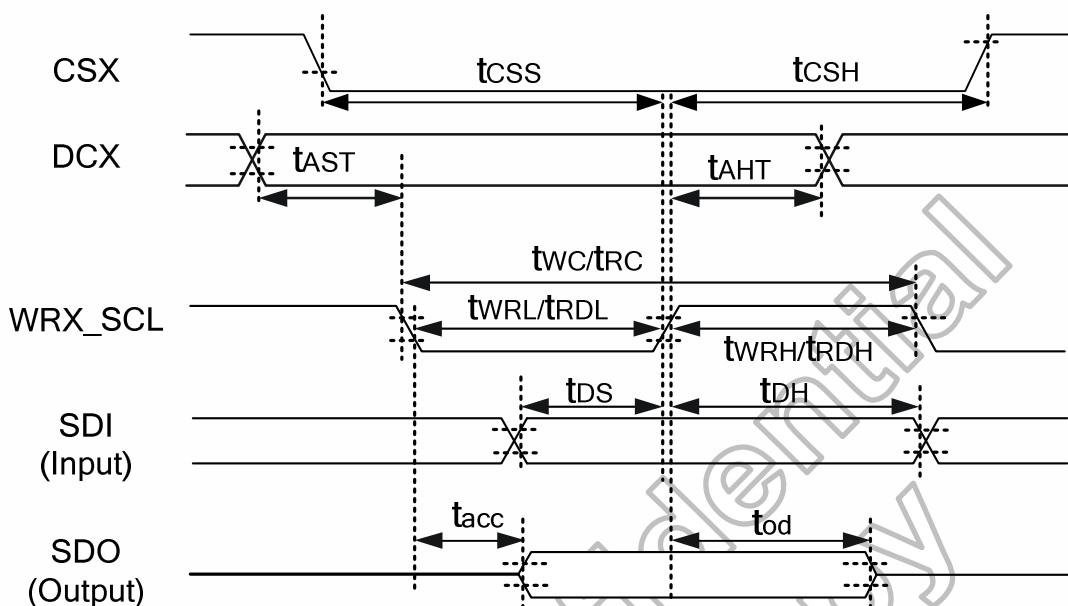


Figure 8.1: DBI Type C interface characteristics

(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, $T_A = 25^\circ\text{C}$)

Signal	Symbol	Parameter	Min.	Max.	Unit	Description
CSX	t_{CSS}	Chip select setup time (Write)	40	-	ns	-
	t_{CSH}	Chip select setup time (Read)	40	-	ns	
DCX	t_{AST}	Address setup time	10	-	ns	-
	t_{AHT}	Address hold time (Write/Read)	10	-	ns	
WRX_SCL (Write)	t_{WC}	Write cycle	100	-	ns	-
	t_{WRH}	Control pulse "H" duration	40	-	ns	
	t_{WRL}	Control pulse "L" duration	40	-	ns	
WRX_SCL (Read)	t_{RC}	Read cycle	150	-	ns	-
	t_{RDH}	Control pulse "H" duration	60	-	ns	
	t_{RDH}	Control pulse "L" duration	60	-	ns	
SDI (Input)	t_{DS}	Data setup time	30	-	ns	For maximum $C_L=30\text{pF}$
	t_{DH}	Data hold time	30	-	ns	
SDO (Output)	t_{acc}	Read access time	10	-	ns	For minimum $C_L=8\text{pF}$
	t_{od}	Output disable time	10	50	ns	

Note: The input signal rise time and fall time (t_r, t_f) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of VDD1 for Input signals.

Table 8.3: DBI Type C interface characteristics

8.3.2 DPI interface characteristics

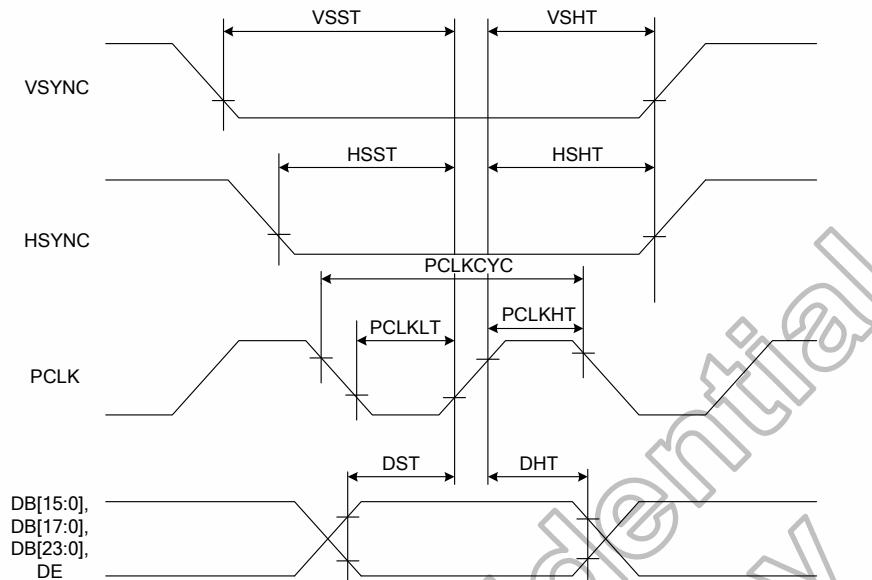


Figure 8.2: DPI interface characteristics

Resolution=480x854 (VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical sync. setup time	VSST	-	10	-	-	ns
Vertical sync. hold time	VSHT	-	10	-	-	ns
Horizontal sync. setup time	HSST	-	10	-	-	ns
Horizontal sync. hold time	HSHT	-	10	-	-	ns
Pixel clock cycle when DPI I/F is running	PCLKCYC	VRR = Min . 50 Hz Max. 70 Hz	29.1 ⁽³⁾	-	46.2 ⁽⁴⁾	ns
Pixel clock low time	PCLKLT	-	10	-	-	ns
Pixel clock high time	PCLKHT	-	10	-	-	ns
Data setup time DB[23:0]	DST	-	10	-	-	ns
Data hold time DB[23:0]	DHT	-	10	-	-	ns

Resolution=480x800 (VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical sync. setup time	VSST	-	10	-	-	ns
Vertical sync. hold time	VSHT	-	10	-	-	ns
Horizontal sync. setup time	HSST	-	10	-	-	ns
Horizontal sync. hold time	HSHT	-	10	-	-	ns
Pixel clock cycle when DPI I/F is running	PCLKCYC	VRR = Min . 50 Hz Max. 70 Hz	31 ⁽³⁾	-	49.2 ⁽⁴⁾	ns
Pixel clock low time	PCLKLT	-	10	-	-	ns
Pixel clock high time	PCLKHT	-	10	-	-	ns
Data setup time DB[23:0]	DST	-	10	-	-	ns
Data hold time DB[23:0]	DHT	-	10	-	-	ns

Note: (1) Signal rise and fall times are equal to or less than 10 ns.

(2) Input signals are measured by 0.30 x VDD1 for low state and 0.70 x VDD1 for high state.

(3) 30 MHz

(4) 27 MHz

(5) 26.7 MHz

(6) VRR : Vertical Refresh Rate, equal to VSYNC frequency.

Table 8.4: DPI interface characteristics

Vertical timings for DPI I/F

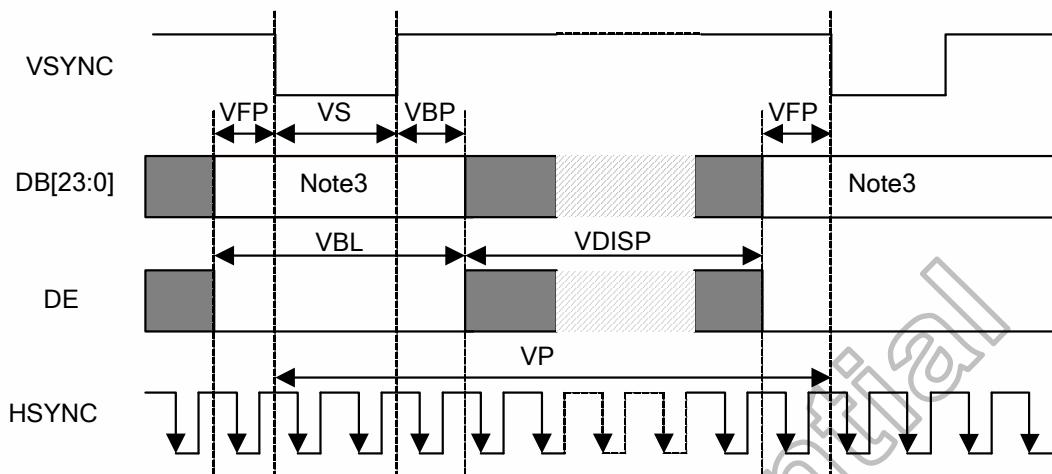


Figure 8.3: Vertical timings for DPI I/F

Resolution=480x854(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, TA=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	860	-	-	Line
Vertical low pulse width	VS	-	2	-	Note(4)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(4)	Line
Vertical data start point	-	VS+VBP	4	-	Note(4)	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	854	-	Line
Vertical Refresh rate	VRR	-	50	-	70	Hz

Resolution=480x800(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, TA=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	806	-	-	Line
Vertical low pulse width	VS	-	2	-	Note(4)	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	Note(4)	Line
Vertical data start point	-	VS+VBP	4	-	Note(4)	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	800	-	Line
Vertical Refresh rate	VRR	-	50	-	70	Hz

Note: (1) Signal rise and fall times are equal to or less than 10 ns.

(2) Input signals are measured by $0.30 \times VDD1$ for low state and $0.70 \times VDD1$ for highstate.

(3) Data lines can be set to "High" or "Low" during blanking time – Don't care.

(4) The VS and VBP pulse width are related to GSP and GCK timing. The GSP and GCK must be set at corresponding position for LCD normal display.

Table 8.5: Vertical timings for DPI I/F

Horizontal timings for DPI I/F

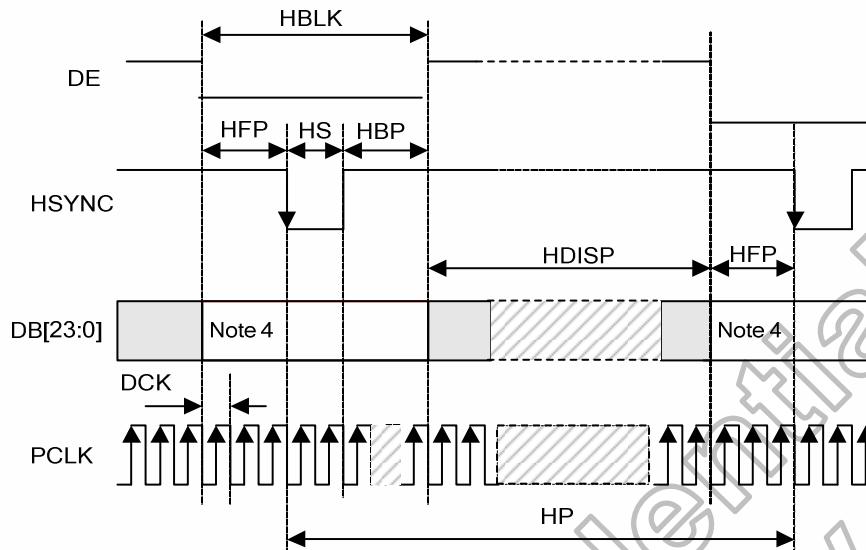


Figure 8.4: Horizontal Timing for DPI I/F

Resolution=480x854 (VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, TA=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS cycle	HP	Note(3)	504	-	568	PCLK
HS low pulse width	HS	-	5	-	78	PCLK
Horizontal back porch	HBP	-	5	-	78	PCLK
Horizontal front porch	HFP	-	5	-	78	PCLK
Horizontal data start point	-	HS+HBP	19	-	83	PCLK
Horizontal blanking period	HBLK	HS+HBP+HFP	24	-	88	PCLK
Horizontal active area	HDISP	-	-	480	-	PCLK
Pixel clock frequency When DPI I/F is running	PCLK	VRR = Min. 50Hz Max. 70Hz	21.6	-	34.3	MHz

Resolution=480x800 (VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, TA=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS cycle	HP	Note(3)	504	-	568	PCLK
HS low pulse width	HS	-	5	-	78	PCLK
Horizontal back porch	HBP	-	5	-	78	PCLK
Horizontal front porch	HFP	-	5	-	78	PCLK
Horizontal data start point	-	HS+HBP	19	-	83	PCLK
Horizontal blanking period	HBLK	HS+HBP+HFP	24	-	88	PCLK
Horizontal active area	HDISP	-	-	480	-	PCLK
Pixel clock frequency When DPI I/F is running	PCLK	VRR = Min. 50Hz Max. 70Hz	20.3	-	32.2	MHz

Note: (1) Signal rise and fall times are equal to or less than 20 ns.

(2) Input signals are measured by $0.30 \times VDD1$ for low state and $0.70 \times VDD1$ for high state.

(3) HP is multiples of eight PCLK.

(4) Data lines can be set to "High" or "Low" during blanking time – Don't care.

(5) HS+HBP must large than 1us.

Table 8.6: Horizontal Timings for DPI I/F

8.3.3 Reset input timing

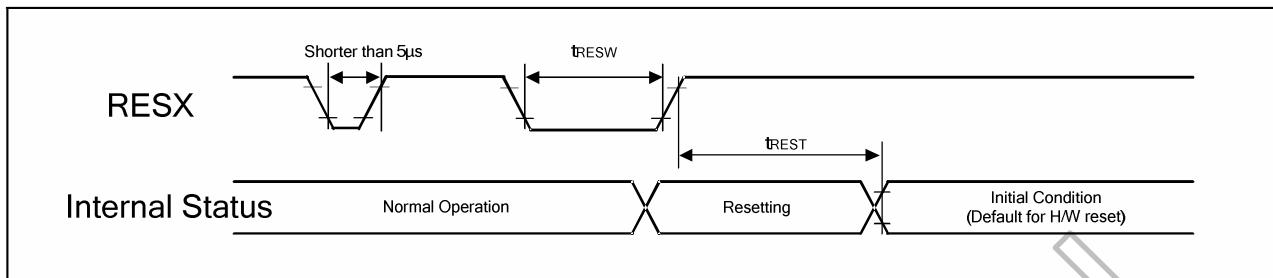


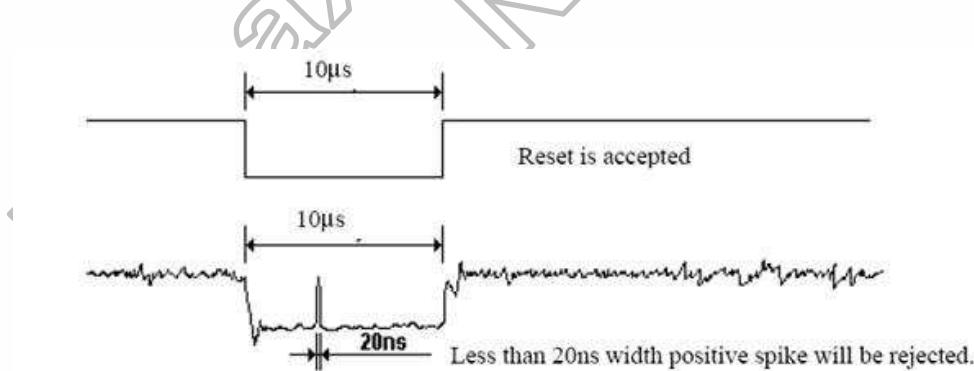
Figure 8.5: Reset input timing

Symbol	Parameter	Related pins	Min.	Typ.	Max.	Note	Unit
t_{RESW}	Reset low pulse width ⁽¹⁾	RESX	10	-	-	-	µs
t_{REST}	Reset complete time ⁽²⁾	-	5	-	-	When reset is applied during Sleep In mode	ms
		-	120	-	-	When reset is applied during Sleep Out mode	ms

Note: (1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 µs	Reset Rejected
Longer than 10 µs	Reset
Between 5 µs and 10 µs	Reset Start

- (2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out -mode. The display remains the blank state in Sleep In -mode) and then returns to Default condition for H/W reset.
- (3) During Reset Complete Time, ID2 value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.
- (4) Spike Rejection also applies during a valid reset pulse as shown below:



- (5) When Reset is applied during Sleep In Mode.
- (6) When Reset is applied during Sleep Out Mode.
- (7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

Table 8.7: Reset timing

8.3.4 DSI D-PHY electrical characteristics

8.3.4.1 The Electrical Characteristics of D-PHY Layer

In general, the DSI D-PHY may contain the following electrical functions: High-Speed Receiver (HS-RX), Low Power Transmitter (LP-TX), a Low-Power Receiver (LP-RX), and the Low-Power Contention Detector (LP-CD). Figure 8.6 shows the complete set of electrical functions required for a fully featured PHY transceiver.

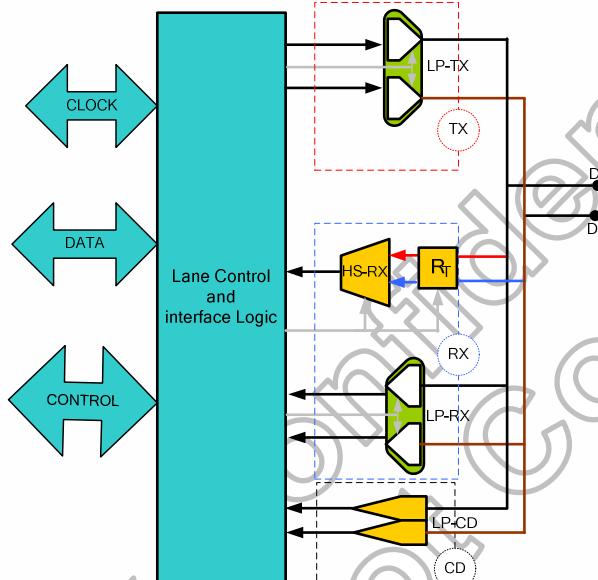


Figure 8.6: Electrical functions of a fully D-PHY transceiver

Where, the HS receiver utilize low-voltage swing differential signaling for signal transmission. The LP transmitter and LP receiver serve as a low power signaling mechanism. Figure 8.7 shows both the HS and LP signal levels on the left and right sides, respectively.

Because the HS signaling levels are below the LP low-level input threshold, Lane switches between Low-Power and High-Speed mode during normal operation.

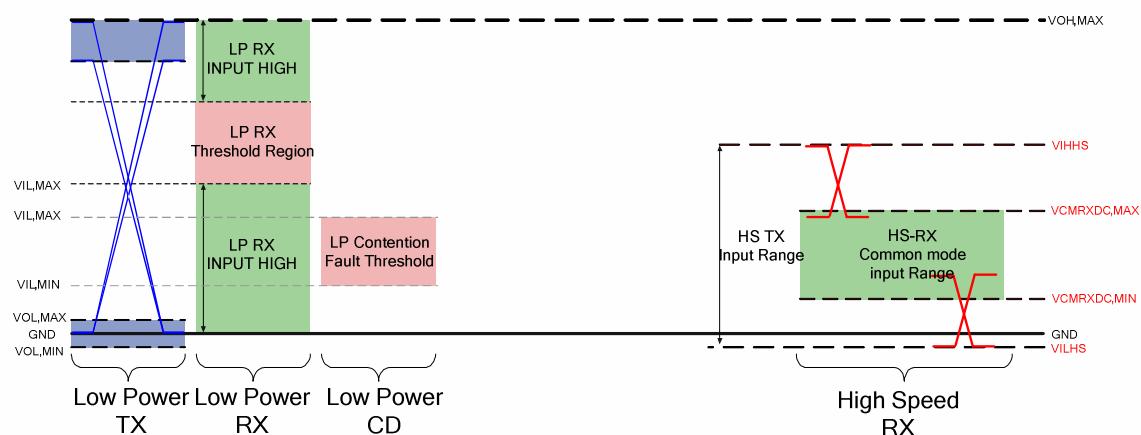


Figure 8.7: Shows both the HS and LP signal levels

8.3.4.2 Electrical characteristics of low-power transmitter

The Low-Power transmitter shall be a slew-rate controlled push-pull driver. It is used for driving the Lines in all Low-Power operating modes. It is therefore important that the static power consumption of a LP transmitter be as low as possible. Under tables list DC and AC characteristic for LP-TX

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{OL}	Thevenin output low level	-50	-	50	mV	-
V_{OH}	Thevenin output high level	1.1	1.2	1.3	V	-
Z_{OLP}	Output impedance of LP-TX	110	-	-	Ω	(1)

Note: (1) Though no maximum value for Z_{OLP} is specified, the LP transmitter output impedance shall ensure the t_{RLP}/t_{FLP} specification is met.

Table 8.8: LP transmitter DC specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
t_{RLP}/t_{FLP}	15%-85% rise time and fall time	-	-	25	ns	(1)
T_{LPX}	Transmitted length of any Low-Power state period	50	-	-	ns	TX_OSC=0 (10)
		100	-	-	ns	TX_OSC=1 (10)
$\frac{\Delta V}{\Delta t_{SR}}$	Slew rate @ $C_{LOAD} = 0\text{pF}$	-	-	500	mV/ns	(1),(3),(5),(6)
	Slew rate @ $C_{LOAD} = 5\text{pF}$	-	-	300	mV/ns	(1),(3),(5),(6)
	Slew rate @ $C_{LOAD} = 20\text{pF}$	-	-	250	mV/ns	(1),(3),(5),(6)
	Slew rate @ $C_{LOAD} = 70\text{pF}$	-	-	150	mV/ns	(1),(3),(5),(6)
	Slew rate @ $C_{LOAD} = 0$ to 70pF (Falling Edge Only)	30	-	-	mV/ns	(1),(2),(3)
	Slew rate @ $C_{LOAD} = 0$ to 70pF (Rising Edge Only)	30	-	-	mV/ns	(1),(3),(7)
	Slew rate @ $C_{LOAD} = 0$ to 70pF (Rising Edge Only)	30 – 0.075 * ($V_{O,INST}$ – 700)	-	-	mV/ns	(1),(8),(9)
C_{LOAD}	Load capacitance	0	-	70	pF	-

Note: (1) C_{LOAD} includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be $<10\text{pF}$. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

- (2) When the output voltage is between 400 mV and 930 mV.
- (3) Measured as average across any 50 mV segment of the output signal transition.
- (4) This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters.
- (5) This value represents a corner point in a piecewise linear curve.
- (6) When the output voltage is in the range specified by VPIN(absmax).
- (7) When the output voltage is between 400 mV and 700 mV.
- (8) Where $V_{O,INST}$ is the instantaneous output voltage, VDP or VDN, in millivolts.
- (9) When the output voltage is between 700 mV and 930 mV.
- (10) TX_OSC is internal register setting.

Table 8.9: LP Transmitter AC Specifications

8.3.4.3 Electrical characteristics of receiver

This part will contain two parts which High-Speed Receiver and Low-Power Receiver. Because their have differential DC and AC characteristic, describe HS-RX first then describe LP-RX.

8.3.4.4 High-speed receiver

The HS receiver is a differential line receiver. It contains a switch-able parallel input termination, Z_{ID} , between the positive input pin D_p and the negative input pin D_n. Under Tables list DC and AC characteristic for HS-RX.

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IDTH}	Differential input high threshold	-	-	70	mV	-
V_{IDL}	Differential input low threshold	-70	-	-	mV	-
V_{ILHS}	Single-ended input low voltage	-40	-	-	mV	(1)
V_{IHHS}	Single-ended input high voltage	-	-	460	mV	(1)
V_{CMRXDC}	Common-mode voltage HS receive mode	70	-	330	mV	(1),(2)
Z_{ID}	Differential input impedance	80	100	125	Ω	-

Note: (1) Excluding possible additional RF interference of 100mV peak sine wave beyond 450MHz.

(2) This table value includes a ground difference of 50mV between the transmitter and the receiver, the static common-mode level tolerance and variations below 450MHz

Table 8.10: HS receiver DC specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$\Delta V_{CMRX(HF)}$	Common mode interference beyond 450 MHz	-	-	100	mV _{PP}	(1)
C_{CM}	Common mode termination	-	-	60	pF	(2)

Note: (1) $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.

(2) For higher bit rates a 14pF capacitor will be needed to meet the common-mode return loss specification.

Table 8.11: HS receiver AC specifications

8.3.4.5 Low-power receiver

The low power receiver is an un-terminated, single-ended receiver circuit. The LP receiver is used to detect the Low-Power state on each pin. For high robustness, the LP receiver shall filter out noise pulses and RF interference. It is recommended the implementer optimize the LP receiver design for low power. The LP receiver shall reject any input glitch when the glitch is smaller than eSpike. The filter shall allow pulses wider than TMIN to propagate through the LP receiver. The related diagram shows as Figure 8.8 Input Glitch Rejection of Low-Power Receivers. Besides, under tables list DC and AC characteristic for LP-RX.

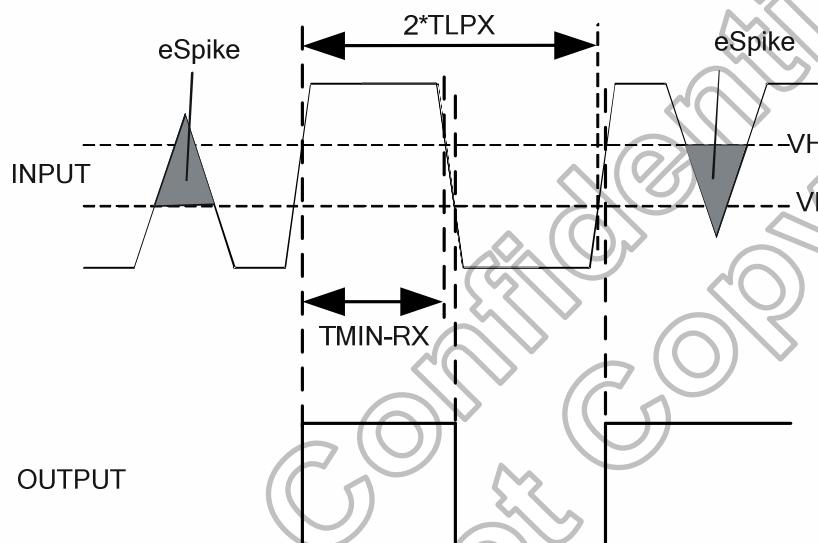


Figure 8.8: Input glitch rejections of low-power receivers

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IL}	Logic 0 input threshold	-	-	550	mV	-
V_{IH}	Logic 1 input threshold	880	-	-	mV	-

Table 8.12: LP receiver DC specifications

Parameter	Description	Min.	Typ.	Max.	Unit	Note
e_{SPIKE}	Input pulse rejection	-	-	300	V.ps	(1),(2), (3)
T_{MIN-RX}	Minimum pulse width response	20	-	-	ns	(4)
V_{INT}	Peak-to-peak interference voltage	-	-	200	mV	-
f_{INT}	Interference frequency	450	-	-	MHz	-

Note: (1) Time-voltage integration of a spike above VIL when being in LP-0 state or below VIH when being in LP-1 state

(2) An impulse less than this will not change the receiver state.

(3) In addition to the required glitch rejection, implementers shall ensure rejection of known RF-interferers.

(4) An input pulse greater than this shall toggle the output.

Table 8.13: LP receiver AC specifications

8.3.4.6 Line contention detection

Contention can be inferred from any of the following conditions:

- A. An LP high fault shall be detected when the LP transmitter is driving high and the pin voltage is less than V_{IL} .
- B. An LP low fault shall be detected when the LP transmitter is driving low and the pad pin voltage is greater than V_{IL} .

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IHCD}	Logic 1 contention threshold	450	-	-	mV	-
V_{ILCD}	Logic 0 contention threshold	-	-	200	mV	-

Table 8.14: Contention detector DC specifications

8.3.4.7 High-speed data-clock timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term “rising edge” means “rising edge of the differential signal, i.e. CP – CN, and similarly for “falling edge”. Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure 8.9.

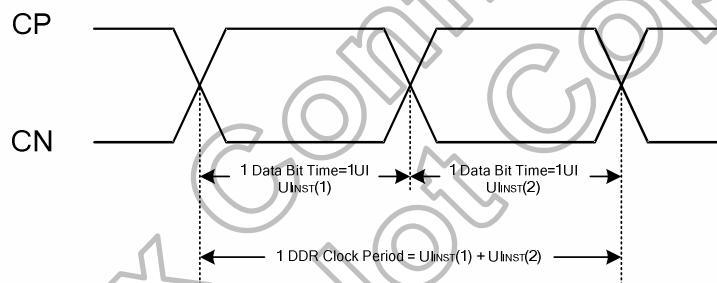


Figure 8.9: DDR clock definition

The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UI_{INST} specifications for the Clock signal are summarized in Table 8.15.

DSI Mode	Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
550Mbps @ 2-lane	UI instantaneous	UI_{INST}	1.82	-	12.5	ns	(1)

Note: (1) This value 1.82ns corresponds to a maximum 550 Mbps data rate, 12.5ns corresponds to a minimum 80 Mbps data rate

Table 8.15: Reverse HS data transmission timing parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.10. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

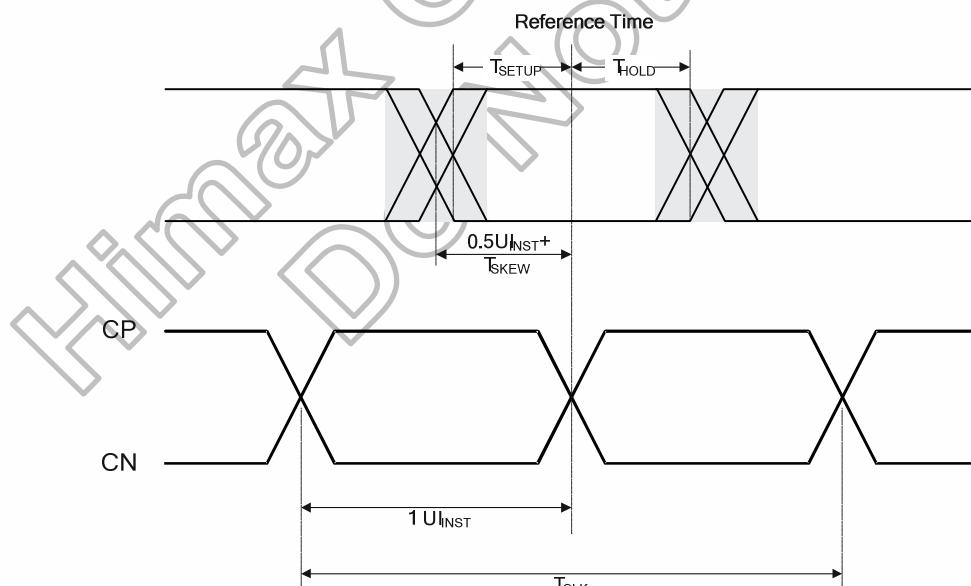


Figure 8.10: Data to clock timing definitions

8.3.4.8 Data-clock timing specifications

The Data-Clock timing specifications are shown in Table 8.16. Implementers shall specify a value $UI_{INST,MIN}$ that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 8.16 are specified as a part of this value. The skew specification, $T_{SKEW[TX]}$, is the allowed deviation of the data launch time to the ideal $\frac{1}{2}UI_{INST}$ displaced quadrature clock edge. The setup and hold times, $T_{SETUP[RX]}$ and $T_{HOLD[RX]}$, respectively, describe the timing relationships between the data and clock signals. $T_{SETUP[RX]}$ is the minimum time that data shall be present before a rising or falling clock edge and $T_{HOLD[RX]}$ is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave $0.4*UI_{INST}$, i.e. $\pm 0.2*UI_{INST}$ for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [Receiver]	$T_{SETUP[RX]}$	0.15	-	-	UI_{INST}	1
Clock to Data Hold Time [Receiver]	$T_{HOLD[RX]}$	0.15	-	-	UI_{INST}	1

Note: (1) Total setup and hold window for receiver of $0.3*UI_{INST}$.

Table 8.16: Data to Clock Timing Specifications

8.3.5 Timings for DSI video mode

8.3.5.1 Vertical timings

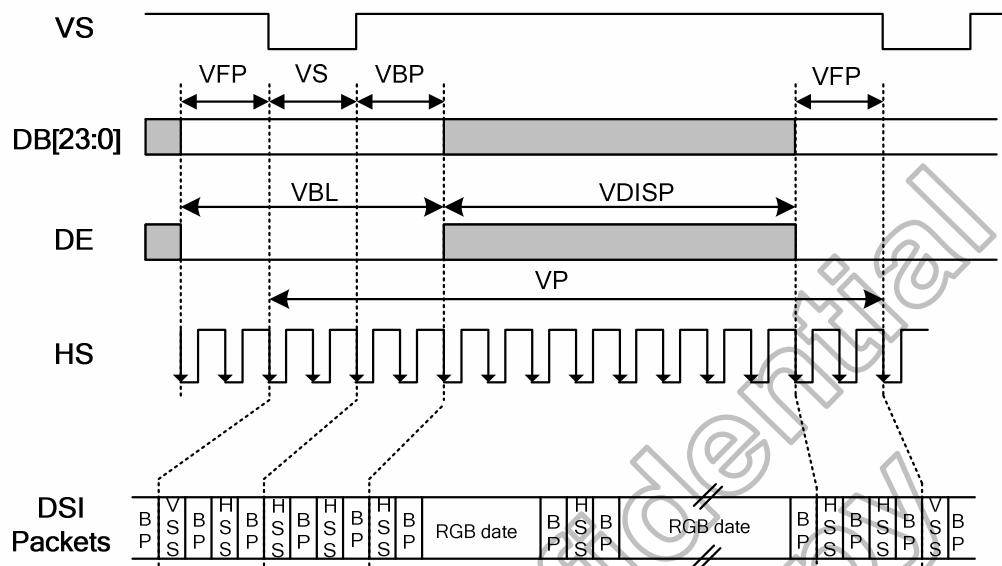


Figure 8.11: Vertical timings for DPI I/F

Resolution=480x854(VSSA=0V, VDD1=1.8V, VDD2=2.8V, VDD3=2.8V, T_A=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Vertical cycle	VP	-	860	-	-	Line
Vertical low pulse width	VS	-	2	-	255 ⁽¹⁾	Line
Vertical front porch	VFP	-	2	-	-	Line
Vertical back porch	VBP	-	2	-	255 ⁽¹⁾	Line
Vertical data start point	-	VS+VBP	4	-	255 ⁽¹⁾	Line
Vertical blanking period	VBL	VS+VBP+VFP	6	-	-	Line
Vertical active area	-	VDISP	-	854	-	Line
Vertical Refresh rate	VRR	-	-	60	-	Hz

Note: (1) The VS and VBP pulse width are related to GSP and GCK timing. The GSP and GCK must be set at corresponding position for LCD normal display.

Table 8.17: Vertical timings for DPI I/F

8.3.5.2 Horizontal timings

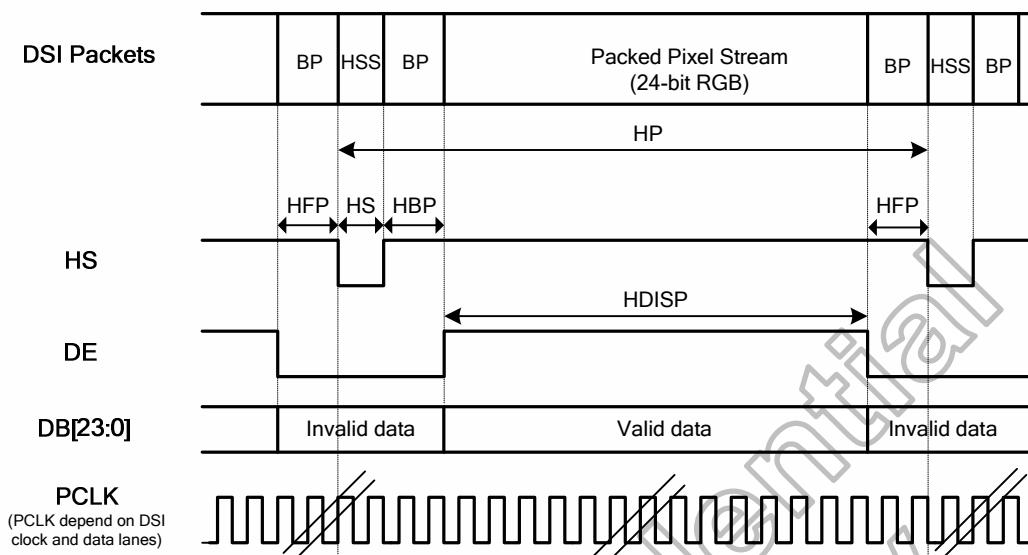


Figure 8.12: Horizontal timing for DSI video mode I/F

Resolution=480x854 (VSSA=0V, VDD1=1.8V, VDD2=VDD3=HS_VCC=2.8V, TA=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
HS cycle	HP	-	495	-	1725	DCK
HS low pulse width	HS	-	5	-	255	DCK
Horizontal back porch	HBP	-	5	-	255	DCK
Horizontal front porch	HFP	-	5	-	255	DCK
Horizontal data start point	-	HS+HBP	10	-	510	DCK
Horizontal blanking period	HBLK	HS+HBP+HFP	15	-	765	DCK
Horizontal active area	HDISP	-	-	480	-	DCK

Table 8.18: Horizontal timings for DSI video mode I/F

8.3.6 I2C AC characteristics

Characteristics of SDA and SCL bus lines for I2C-bus devices

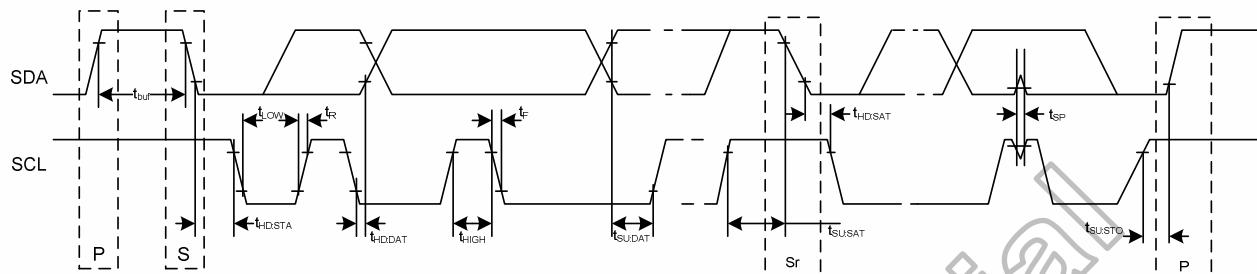


Figure 8.13 I2C timing

Parameter	Symbol	Standard-Mode I2C-BUS		Fast-Mode I2C-BUS		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f_{SCL}	0	100	0	400	KHz
Bus free time between STOP and START condition	t_{BUF}	4.7	-	1.3	-	μs
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD:STA}$	4.0	-	0.6	-	μs
LOW period of the SCL clock	t_{LOW}	4.7	-	1.3	-	μs
HIGH period of the SCL clock	t_{HIGH}	4.0	-	0.6	-	μs
Set-up time for a repeated START condition	$t_{SU:STA}$	4.7	-	0.6	-	μs
Data hold time	$t_{HD:DAT}$	0	-	0	0.9	μs
Data set-up time	$t_{SU:DAT}$	250	-	100	-	ns
Rise time of both SDA and SCL signals	t_R	-	1000	$20+0.1 C_b$	300	ns
Fall time of both SDA and SCL signals	t_F	-	300	$20+0.1 C_b$	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	4.0	-	0.6	-	μs
Capacitive load for each bus line.	C_b	-	400	-	400	pF

Note: (1) All values are referred to VIH (0.7xVCCIO) and VIL (0.3xVCCIO) level.

(2) A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the VIH of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

(3) The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal.

(4) A fast-mode I2C-bus device can be used in a standard-mode I2C-bus system, but the requirement $t_{SU:DAT} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{R_{max}} + t_{SU:DAT} = 1000+250=1250$ ns (according to the standard-mode I2C-bus specification) before the SCL line is released.

(5) C_b = total capacitance of one bus line in pF.

Table 8.19 I2C timing spec.

9. Ordering Information

Part No.	Package
HX8379-A000 <u>PDxxx</u>	PD: mean COG xxx: mean chip thickness (μm), (default: 200 μm)

10. Revision History

Version	Date	Description of Changes
01	2012/05/29	New setup.
	2012/06/04	<ol style="list-style-type: none"> 1. Remove TE mode2 description(page 52). 2. Modify capacitance value (page 246-249)
	2012/06/13	<ol style="list-style-type: none"> 1. Modify CSX pin description. Connect to VDD1 when not used. 2. Modify HS_VSS pin description. Connect to VSSD on FPC.
	2012/06/15	<ol style="list-style-type: none"> 1. Update some table format. 2. Remove partial mode. 3. Modify pin layout recommendation circuit, (some VSSA → VSSD_P). (page 241-244) 4. Modify pad name(CGOUT0~15L → CGOUT 15~0L). (page 241-244).
	2012/06/25	<ol style="list-style-type: none"> 1. Modify Layout recommendation circuit. Add CSP, CSN maxR. Modify Typo. (page 243-246) 2. Modify RB1h, FS0, FS1, FS2 description and setting table. (page 187-199). 3. Modify RB1h register description, OTP, default value. (page 120, 129, 187~201) 4. Add RD5h register description. (page 232-235)