# SPECIFICATION
# FOR
# LCM+CTP Module

| | |
|---|---|
| MODULE No: | KD050HDFIA020-06-C020E |
| CUSTOMER: | |

| STARTEK | INITIAL | DATE |
|---|---|---|
| PREPARED BY | | |
| CHECKED BY | | |
| APPROVED BY | | |

| CUSTOMER | INITIAL | DATE |
|---|---|---|
| APPROVED BY | | |

## Revision History

| Date | Rev. No. | Page | Summary |
|---|---|---|---|
| 2022.03.30 | V1.0 | ALL | FIRST ISSUE |
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# Contents

## * Description

This is a color active matrix TFT (Thin Film Transistor) LCD (liquid crystal display) that uses amorpho us silicon TFT as a switching device. This model is composed of a Transmissive type TFT-LCD Panel, driver circuit,back-light unit. The resolution of a 5.0'TFT-LCD contains 720x1280 pixels, and can displ ay up to 65K/262K/16.7M colors.

## * Features

| General Information Items | Specification | Unit | Note |
|---|---|---|---|
| | Main Panel | | |
| Display area(AA) | 62.10(H)*110.40(V) (5.0inch) | mm | - |
| Driver element | TFT active matrix | - | - |
| Display colors | 65K/262K/16.7M | colors | - |
| Number of pixels | 720(RGB)*1280 | dots | - |
| TFT Pixel arrangement | RGB vertical stripe | - | - |
| Pixel pitch | 0.08625(H)*0.08625(V) | mm | - |
| Viewing angle | ALL | o'clock | - |
| TFT Controller IC | ILI9881C | - | - |
| Display mode | Transmissive/Normally Black | - | - |
| LCM Interface | 4 Lane MIPI | - | |
| Operating temperature | -20～+70 | ℃ | - |
| Storage temperature | -30～+80 | ℃ | - |
| Module bonding technology | Use Tape bonding between LCM and CTP | - | |

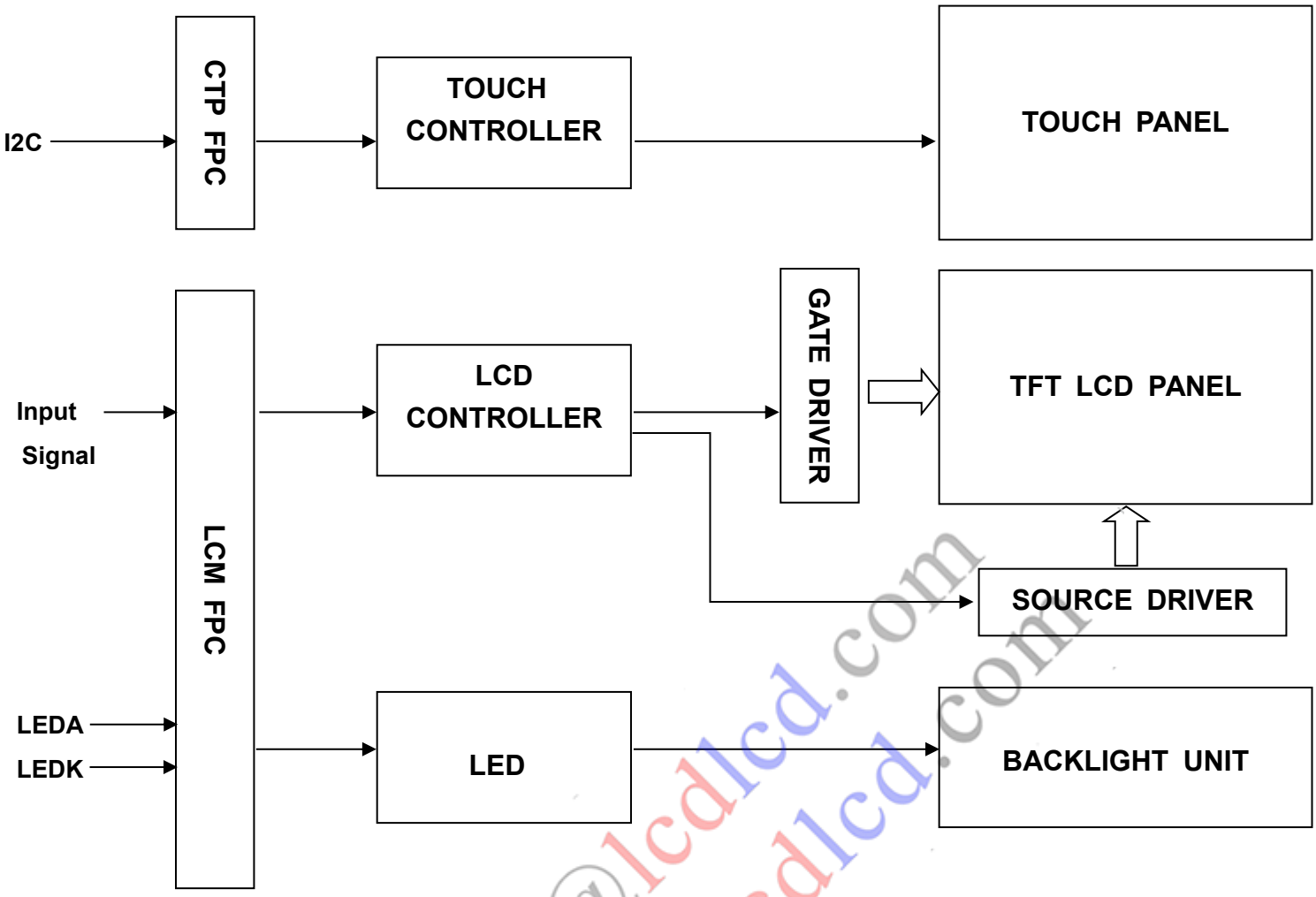
## * CTP Features

| General Information Items | Specification | Unit | Note |
|---|---|---|---|
| | Main Panel | | |
| Resolution | 720(H)*1280(V) | - | |
| Structure | G+G | - | |
| Controller IC | GT911 | - | |
| Interface | I2C | - | |
| Slave Adress | 0x5D(7bit) or 0x14(7bit) | - | Note1 |
| Touch mode | Five points | - | - |
| Logic level | 3.3 | V | |

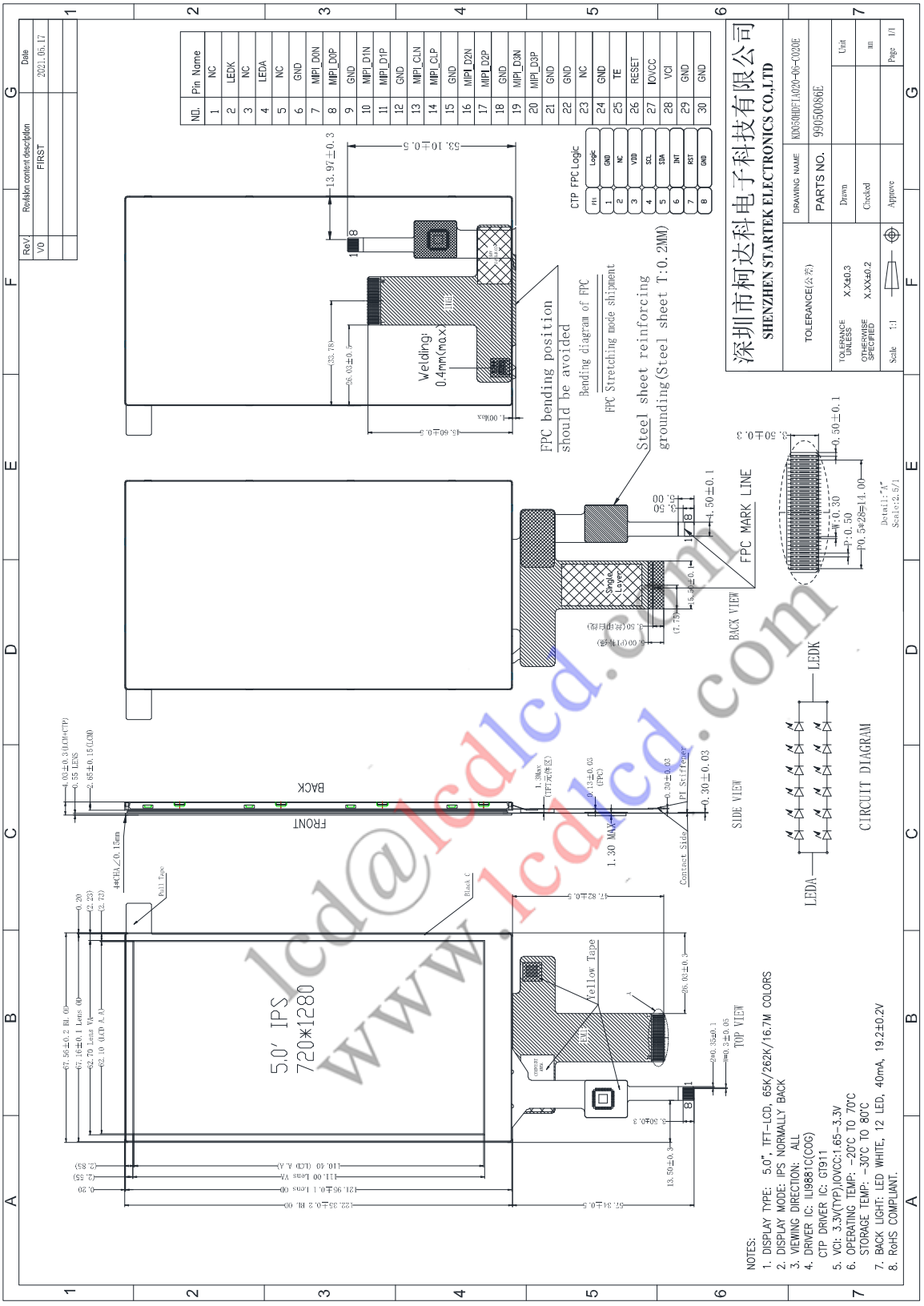
*** Mechanical Information**

| Item | | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Module size | Horizontal(H) | | 67.56 | | mm | - |
| | Vertical(V) | | 122.35 | | mm | - |
| | Depth(D) | | 4.03 | | mm | - |
| Weight | | | TBD | | g | - |

## 1. Block Diagram



## 2. Outline dimension



# 3. Input terminal Pin Assignment

## 3.1 TFT

| NO. | SYMBOL | DISCRIPTION | I/O |
|---|---|---|---|
| 1 | NC | | |
| 2 | LEDK | Cathode pin of backlight. | P |
| 3 | NC | | |
| 4 | LEDA | Anode pin of backlight. | P |
| 5 | NC | | |
| 6 | GND | Ground. | P |
| 7 | MIPI_D0N | - MIPI DSI differential data pair. (Data lane 0) | I |
| 8 | MIPI_D0P | | I |
| 9 | GND | Ground. | P |
| 10 | MIPI_D1N | - MIPI DSI differential data pair. (Data lane 1) | I |
| 11 | MIPI_D1P | | I |
| 12 | GND | Ground. | P |
| 13 | MIPI_CLN | - MIPI DSI differential clock pair. | I |
| 14 | MIPI_CLP | | I |
| 15 | GND | Ground. | P |
| 16 | MIPI_D2N | - MIPI DSI differential data pair. (Data lane 2)<br>Leave it open or fix to GND level when not in use. | I |
| 17 | MIPI_D2P | | I |
| 18 | GND | Ground. | P |
| 19 | MIPI_D3N | - MIPI DSI differential data pair. (Data lane 3)<br>Leave it open or fix to GND level when not in use. | I |
| 20 | MIPI_D3P | | I |
| 21 | GND | Ground. | P |
| 22 | GND | Ground. | P |
| 23 | NC | | |
| 24 | GND | Ground. | P |

| | | | |
|---|---|---|---|
| 25 | TE | - Tearing effect output pin.<br>Leave the pin open when not in use. | O |
| 26 | RESET | - The external reset input<br>Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power. | I |
| 27 | IOVCC | - Power supply for internal logic regulator. Connect to an external power supply of 1.65V to 3.3V | P |
| 28 | VCI | - Power supply for analog circuits. Connect to an external power supply of 2.5V to 3.3V | P |
| 29 | GND | Ground. | P |
| 30 | GND | Ground. | P |

**3.2 CTP**

| NO. | SYMBOL | DISCRIPTION | I/O |
|---|---|---|---|
| 1 | GND | Ground. | P |
| 2 | NC | | |
| 3 | VDD | Supply voltage. | P |
| 4 | SCL | I2C clock input. | I |
| 5 | SDA | I2C data input and output | I/O |
| 6 | INT | External interrupt to the host. | I |
| 7 | RST | External Reset, Low is active. | I |
| 8 | GND | Ground. | P |

# 4. LCD Optical Characteristics

## 4.1 Optical specification

| Item | | Symbol | Condition | Min. | Typ. | Max. | Unit. | Note |
|---|---|---|---|---|---|---|---|---|
| Contrast Ratio | | CR | Θ=0 Normal viewing angle | 640 | 800 | -- | | (1)(2) |
| Response time | Rising | $T_{R+}T_F$ | | -- | 20 | 25 | msec | |
| | Falling | | | -- | | | | (1)(3) |
| Color Gamut | | S(%) | | 65 | 70 | -- | % | |
| Color Filter Chromacicity | White | $W_X$ | | -0.04 | 0.316 | +0.04 | | (1)(4) CF glass |
| | | $W_Y$ | | | 0.336 | | | |
| | Red | $R_X$ | | | 0.631 | | | |
| | | $R_Y$ | | | 0.339 | | | |
| | Green | $G_X$ | | | 0.320 | | | |
| | | $G_Y$ | | | 0.607 | | | |
| | Blue | $B_X$ | | | 0.151 | | | |
| | | $B_Y$ | | | 0.045 | | | |
| Viewing angle | Hor. | ΘL | CR>10 | -- | 80 | -- | | (1)(4) |
| | | ΘR | | -- | 80 | -- | | |
| | Ver. | ΘU | | -- | 80 | -- | | |
| | | ΘD | | -- | 80 | -- | | |
| Option View Direction | | ALL | | | | | | |

*The data comes from the LCD specification.

**Measuring Condition**

Measuring surrounding : dark room

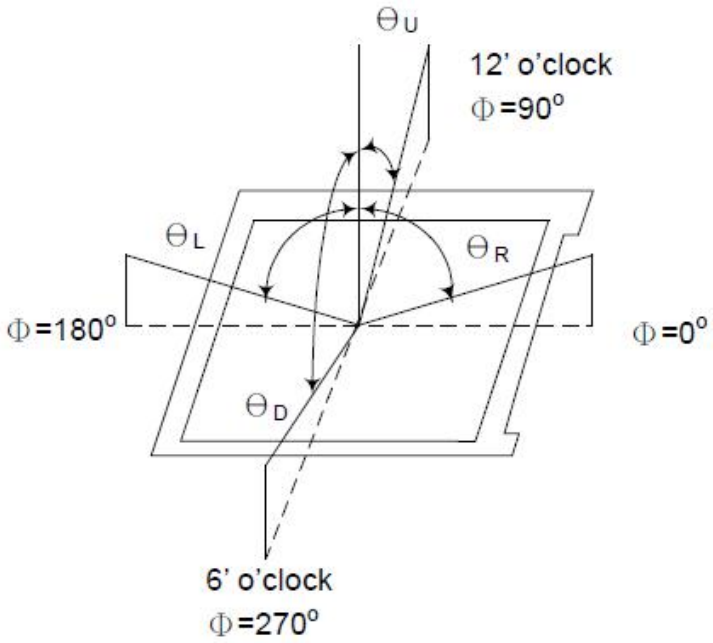
Ambient temperature : 25±2oC

15min. warm-up time.

**Measuring Equipment**

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.

**Note (1):** Definition of Viewing Angle :

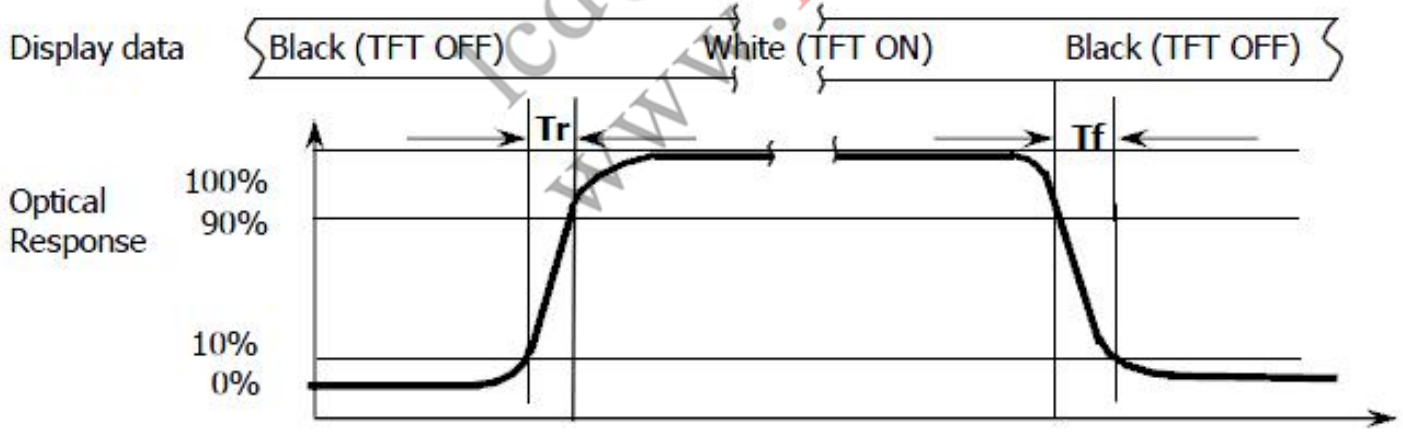



**Note (2):** Definition of Contrast Ratio(CR) :measured at the center point of panel

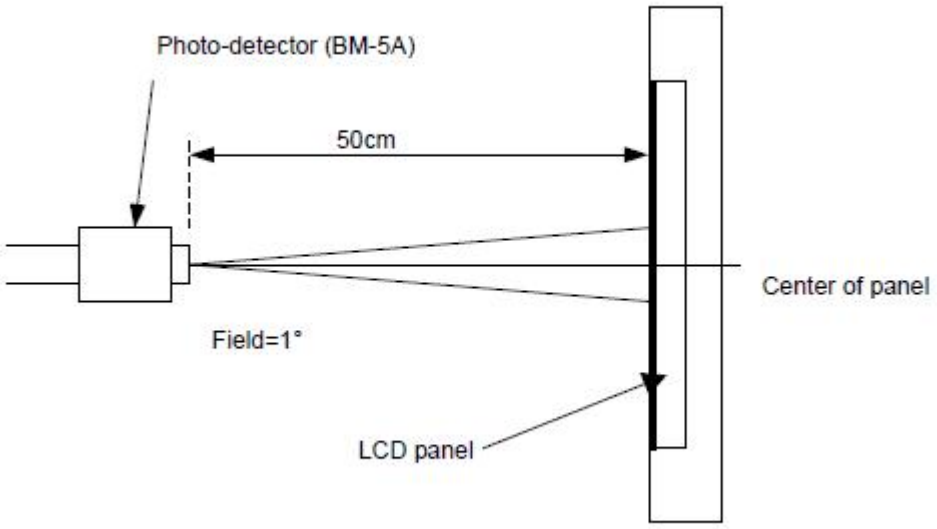
$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$



**Note (3):** Response Time



**Note (4):** Definition of optical measurement setup



# 5. TFT Electrical Characteristics

## 5.1 Absolute Maximum Rating (Ta=25 VSS=0V)

| Characteristics | Symbol | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Digital Supply Voltage | VCI | -0.3 | 6.5 | V | Note1 |
| Digital interface supple Voltage | IOVCC | -0.3 | 3.3 | V | |
| Operating temperature | $T_{OP}$ | -20 | +70 | ℃ | |
| Storage temperature | $T_{ST}$ | -30 | +80 | ℃ | |

NOTE1: If the absolute maximum rating of even is one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product within the range of the absolute maximum ratings.

## 5.2 DC Electrical Characteristics

| Characteristics | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Digital Supply Voltage | VCI | 2.5 | 3.3 | 6.0 | V | |
| Digital interface supple Voltage | IOVCC | 1.65 | 1.8 | 3.3 | V | |
| Normal mode Current | IDD | -- | 40 | 80 | mA | |
| Level input voltage | $V_{IH}$ | 0.7IOVCC | | IOVCC | V | |
| | $V_{IL}$ | GND | | 0.3 IOVCC | V | |
| Level output voltage | $V_{OH}$ | IOVCC- | | -- | V | |
| | $V_{OL}$ | GND | | GND+0.4 | V | |

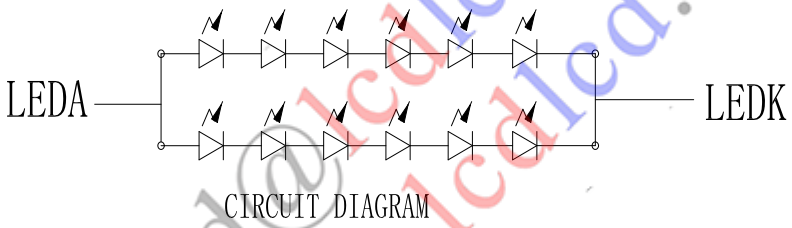
## 5.3 LED Backlight Characteristics

The back-light system is edge-lighting type with 12 chips White LED

| Item | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Forward Current | $I_F$ | 30 | 40 | -- | mA | -- |
| Forward Voltage | $V_F$ | -- | 19.2 | -- | V | -- |
| LCM Luminance | $L_V$ | 380 | 420 | -- | cd/m2 | Note3 |
| LED life time | Hr | 50000 | | | Hour | Note1,2 |
| Uniformity | AVg | 80 | -- | -- | % | Note3 |

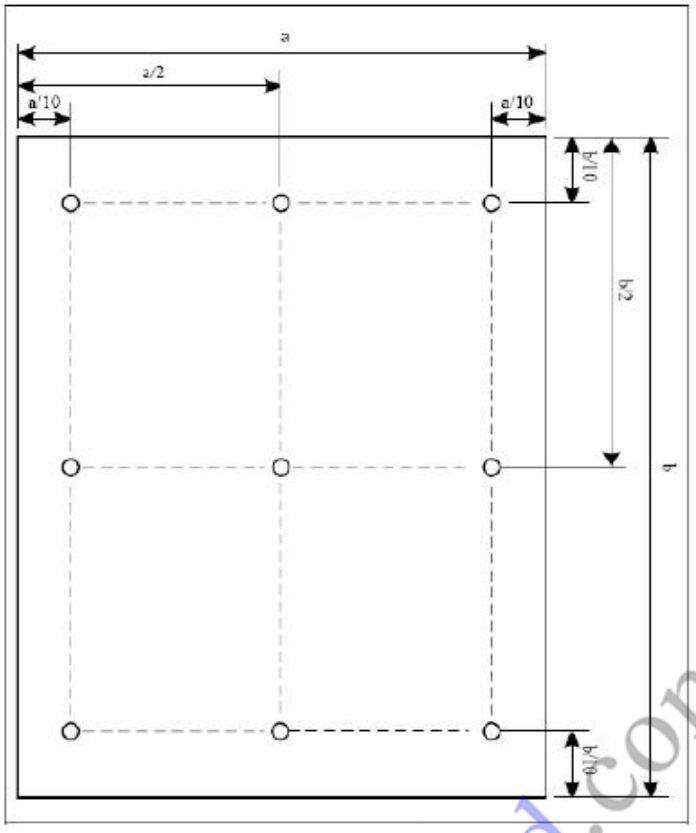
Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The “LED life time” is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=40mA. The LED lifetime could be decreased if operating IL is larger than 40mA. The constant current driving method is suggested.




CIRCUIT DIAGRAM

NOTE 3：Luminance Uniformity of these 9 points is defined as below:




$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points (1-9)}}{\text{maximum luminance in 9 points (1-9)}}$$

$$\text{Luminance} = \frac{\text{Total Luminance of 9 points}}{9}$$

# 6. MIPI Interface Characteristics

## 6.1 High Speed Mode – Clock Channel Timing

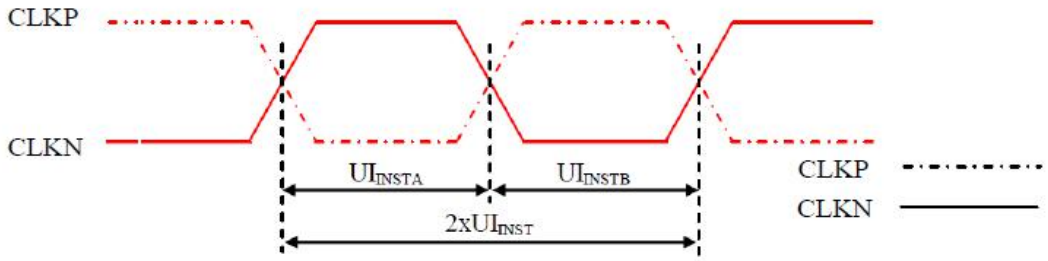



**Figure 118: DSI Clock Channel Timing**

**Table 38: DSI Clock Channel Timing**

| Signal | Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|
| CLKP/N | $2xUI_{INST}$ | Double UI instantaneous | 4 | 25 | ns |
| CLKP/N | $UI_{INSTA}$, $UI_{INSTB}$ (Note 1) | UI instantaneous Half | 2 (Note 2) | 12.5 | ns |

***Notes:***

*1. UI = UIINSTA = UIINSTB*

*2. Define the minimum value of 24 UI per Pixel, see Table 39.*

**Table 39: Limited Clock Channel Speed**

| Data type | Two Lanes speed | Three Lanes speed | Four Lanes speed |
|---|---|---|---|
| Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel | 566 Mbps | 433 Mbps | 366 Mbps |
| Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel | 637 Mbps | 487 Mbps | 412 Mbps |
| Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel | 850 Mbps | 650 Mbps | 550 Mbps |
| Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel | 850 Mbps | 650 Mbps | 550 Mbps |

## 6.2 High Speed Mode – Data Clock Channel Timing

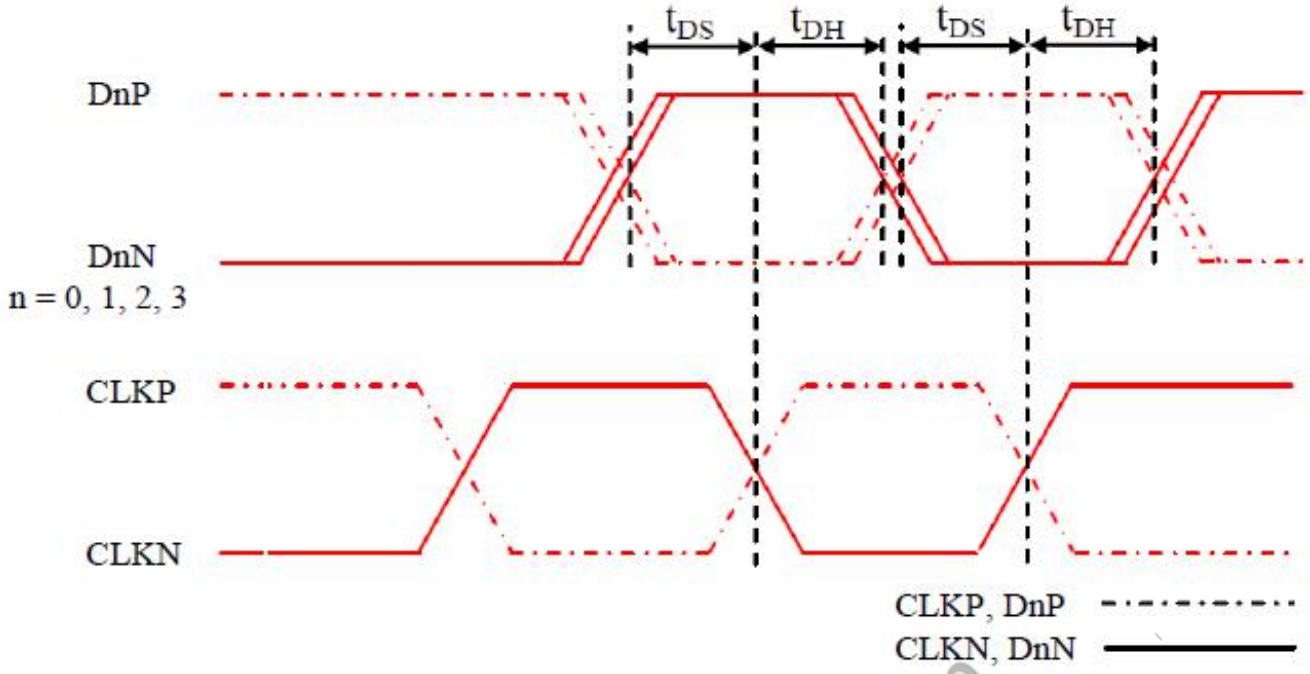



**Figure 119: DSI Data to Clock Channel Timings**

**Table 40: DSI Data to Clock Channel Timings**

| Signal | Symbol | Parameter | Min | Max |
|---|---|---|---|---|
| DnP/N , n=0 and 1 | $t_{DS}$ | Data to Clock Setup time | 0.15xUI | - |
| | $t_{DH}$ | Clock to Data Hold Time | 0.15xUI | - |

## 6.3 High Speed Mode – Rising and Fall Timings

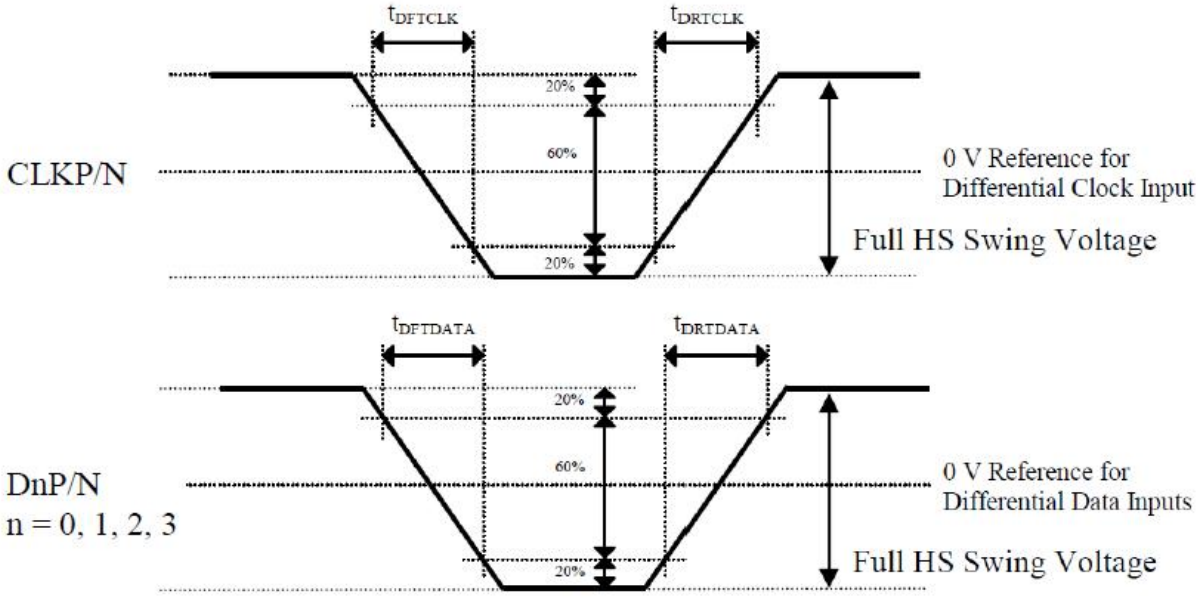



**Figure 120: Rising and Falling Timings on Clock and Data Channels**

**Table 41: Rise and Fall Timings on Clock and Data Channels**

| Parameter | Symbol | Condition | Specification | | |
|---|---|---|---|---|---|
| | | | Min | Typ | Max |
| Differential Rise Time for Clock | $t_{DRTCLK}$ | CLKP/N | 150 ps | - | 0.3UI (Note) |
| Differential Rise Time for Data | $t_{DRTDATA}$ | DnP/N n=0 and 1 | 150 ps | - | 0.3UI (Note) |
| Differential Fall Time for Clock | $t_{DFTCLK}$ | CLKP/N | 150 ps | - | 0.3UI (Note) |
| Differential Fall Time for Data | $t_{DFTDATA}$ | DnP/N n=0 and 1 | 150 ps | - | 0.3UI (Note) |

***Note:*** *The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard.*

## 6.4 Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the MCU to the Display Module (ILI9881C) are illustrated for reference purposes below.

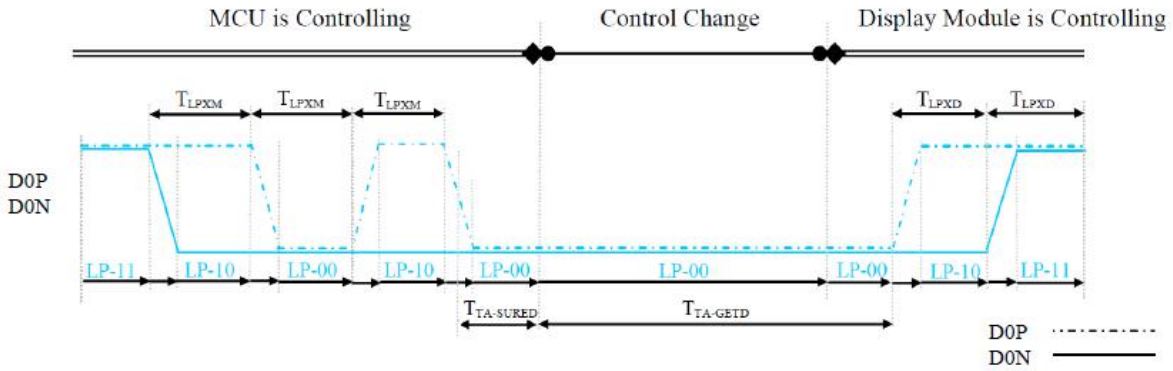



**Figure 121: BTA from the MCU to the Display Module**

Lower Power Mode and its State Periods on the Bus Turnaround (BTA) from the Display Module (ILI9881C) to the MCU are illustrated for reference purposes below.

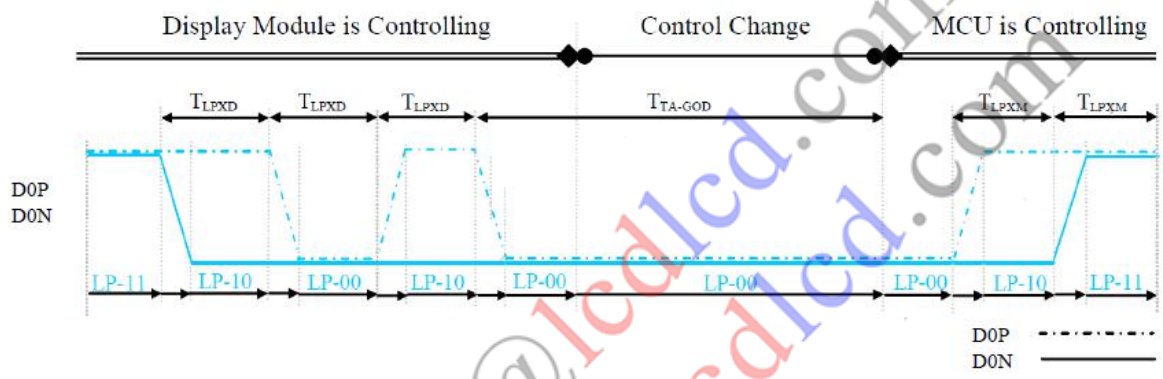



**Figure 122: BTA from the Display Module to the MCU**



**Table 42: Low Power State Period Timings – A**

| Signal | Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|---|
| D0P/N | $T_{LPXM}$ | Length of LP-00, LP-01, LP-10 or LP-11 periods<br>MCU ➔ Display Module (ILI9881C) | 50 | 75 | ns |
| D0P/N | $T_{LPXD}$ | Length of LP-00, LP-01, LP-10 or LP-11 periods<br>Display Module (ILI9881C) ➔ MCU | 50 | 75 | ns |
| D0P/N | $T_{TA-SURED}$ | Time-out before the Display Module (ILI9881C) starts driving | $T_{LPXD}$ | $2xT_{LPXD}$ | ns |

**Table 43: Low Power State Period Timings – B**

| Signal | Symbol | Description | Time | Unit |
|---|---|---|---|---|
| D0P/N | $T_{TA-GETD}$ | Time to drive LP-00 by Display Module (ILI9881C) | $5xT_{LPXD}$ | ns |
| D0P/N | $T_{TA-GOD}$ | Time to drive LP-00 after turnaround request - MCU | $4xT_{LPXD}$ | ns |

## 6.5 Data Lanes from Low Power Mode to High Speed Mode

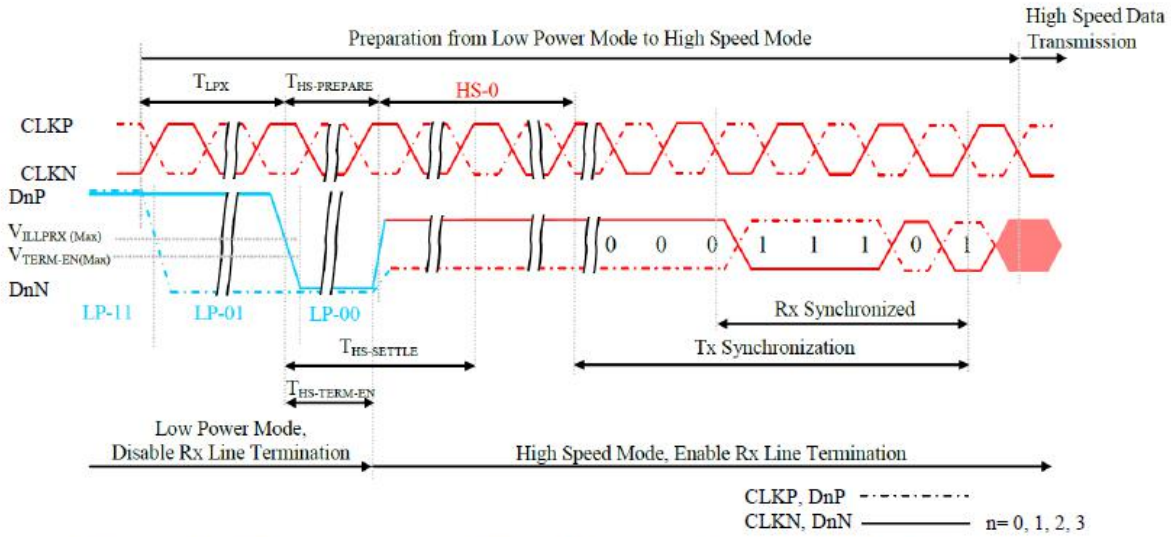
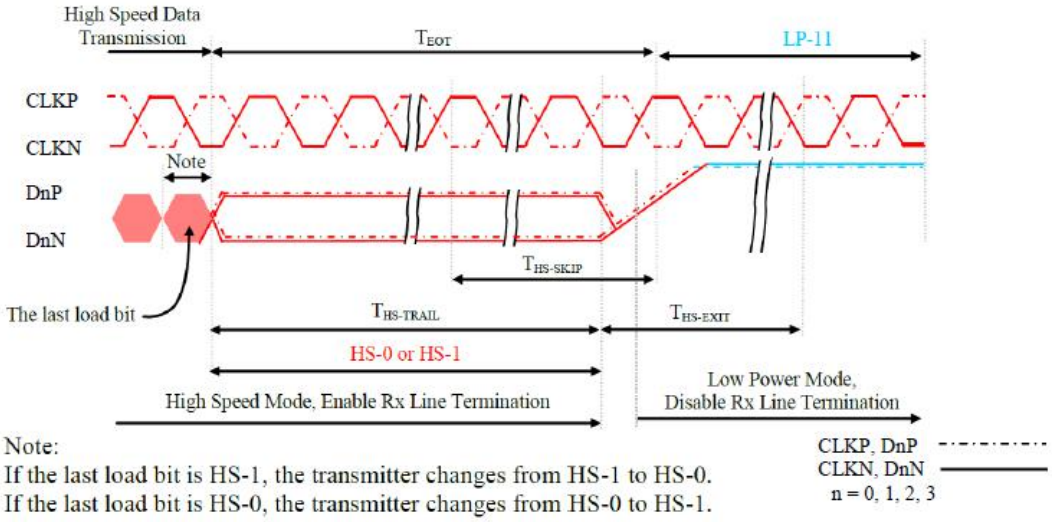



**Figure 123: Data Lanes - Low Power Mode to High Speed Mode Timings**

**Table 44: Data Lanes - Low Power Mode to High Speed Mode Timings**

| Signal | Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|---|
| DnP/N, n = 0 and 1 | $T_{LPX}$ | Length of any Low Power State Period | 50 | - | ns |
| DnP/N, n = 0 and 1 | $T_{HS-PREPARE}$ | Time to drive LP-00 to prepare for HS Transmission | 40+4xUI | 85+6xUI | ns |
| DnP/N, n = 0 and 1 | $T_{HS-TERM-EN}$ | Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX | - | 35+4xUI | ns |

## 6.6 Data Lanes from High Power Mode to High Speed Mode




Note:
If the last load bit is HS-1, the transmitter changes from HS-1 to HS-0.
If the last load bit is HS-0, the transmitter changes from HS-0 to HS-1.

**Figure 124: Data Lanes - High Speed Mode to Low Power Mode Timings**

**Table 45: Data Lanes - High Speed Mode to Low Power Mode Timings**

| Signal | Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|---|
| DnP/N, n = 0 and 1 | $T_{HS-SKIP}$ | Time-Out at Display Module (ILI9881C) to ignore transition period of EoT | 40 | 55+4xUI | ns |
| DnP/N, n = 0 and 1 | $T_{HS-EXIT}$ | Time to driver LP-11 after HS burst | 100 | - | ns |

## 6.7 DSI Clock Burst – High Speed Mode to/from Low Power Mode

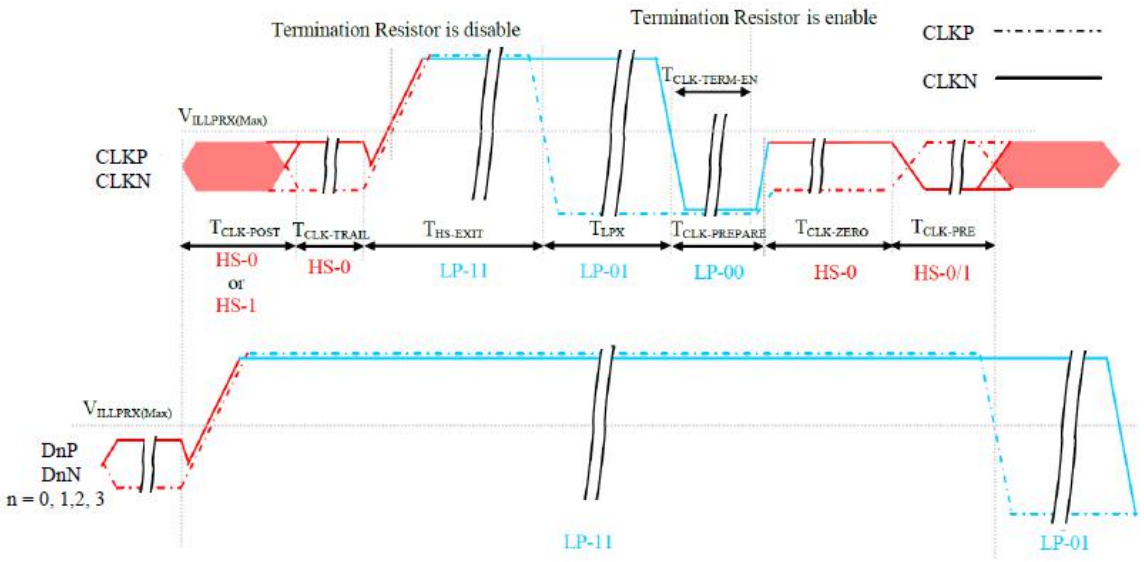


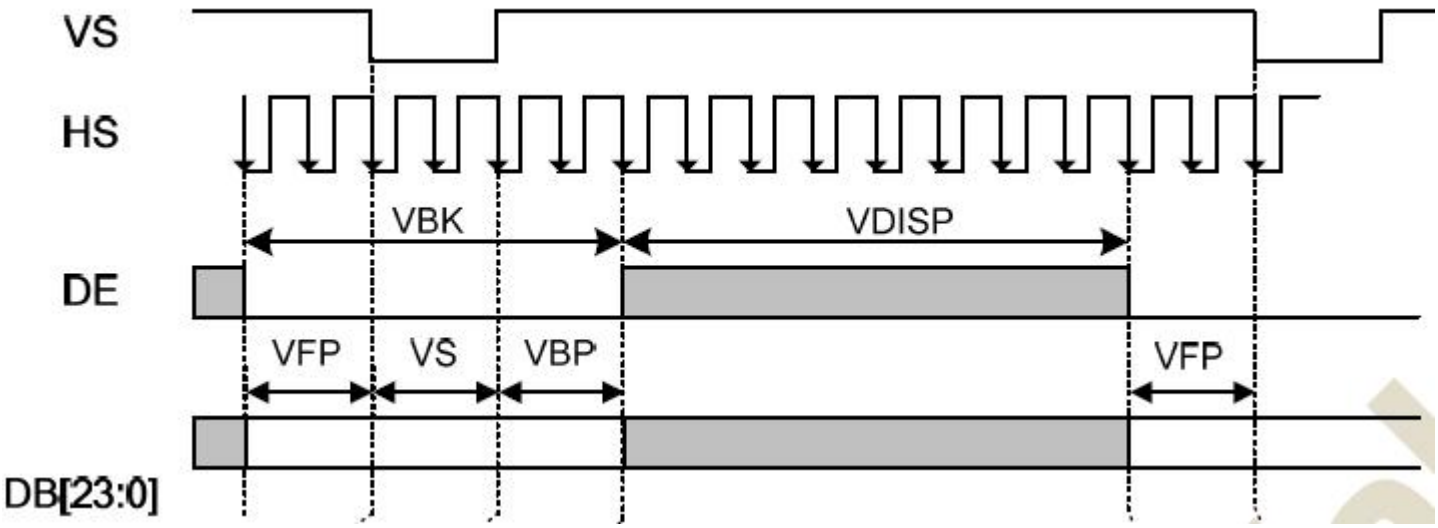

**Figure 125: Clock Lanes - High Speed Mode to/from Low Power Mode Timings**

**Table 46: Clock Lanes - High Speed Mode to/from Low Power Mode Timings**

| Signal | Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|---|
| CLKP/N | $T_{CLK-POST}$ | Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode | 60+52xUI | - | ns |
| CLKP/N | $T_{CLK-TRAIL}$ | Time to drive HS differential state after last payload clock bit of a HS transmission burst | 60 | - | ns |
| CLKP/N | $T_{HS-EXIT}$ | Time to drive LP-11 after HS burst | 100 | - | ns |
| CLKP/N | $T_{CLK-PREPARE}$ | Time to drive LP-00 to prepare for HS transmission | 38 | 95 | ns |
| CLKP/N | $T_{CLK-TERM-EN}$ | Time-out at Clock Lane to enable HS termination | - | 38 | ns |
| CLKP/N | $T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$ | Minimum lead HS-0 drive period before starting Clock | 300 | - | ns |
| CLKP/N | $T_{CLK-PRE}$ | Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode | 8xUI | - | ns |

## 6.8 Timing for DSI video mode

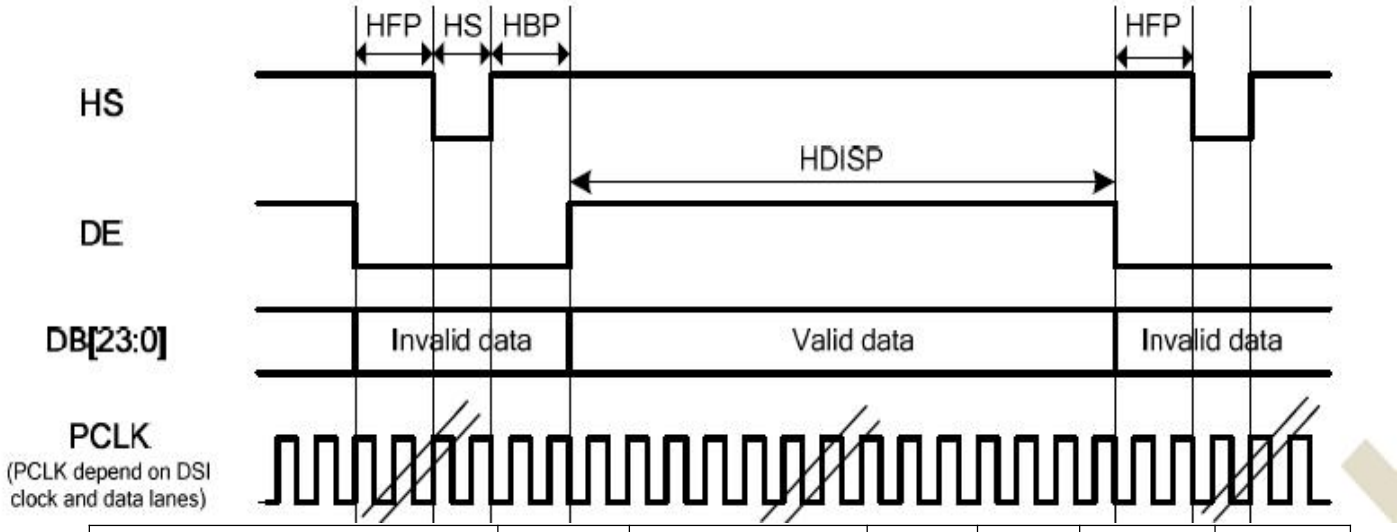
### 6.8.1 Vertical Timings




| Item | Symbol | Condition | Min | Typ | Max. | Unit |
|---|---|---|---|---|---|---|
| Vertical low pulse width | VS | -- | 2 | (4) | Note(1) | Line |
| Vertical front porch | VFP | -- | 2 | (10) | -- | Line |
| Vertical back porch | VBP | -- | 6 | (20) | Note(1) | Line |
| Vertical blanking period | VBK | VS+VBP+VFP | -- | (34) | -- | Line |
| Vertical active area | - | VDISP | -- | 1280 | -- | Line |
| Vertical Refresh rate | VRR | -- | -- | 60 | -- | HZ |

**Note:** (1) The VS and VBP pulse width are related to GIP start pulse and GIP clock pulse timing. The GIP start pulse and GIP clock pulse must be set at corresponding position for LCD normal display.

### 6.8.2 Horizontal Timings




| Item | Symbol | Condition | Min | Typ | Max. | Unit |
|---|---|---|---|---|---|---|
| HS low pulse width | HS | -- | 6 | (6) | 78 | DCK |
| Horizontal front porch | HFP | -- | 5 | (10) | 78 | DCK |
| Horizontal back porch | HBP | -- | 5 | (20) | 78 | DCK |
| Horizontal blanking period | HBK | HS+HBP+HFP | -- | (36) | 88 | DCK |
| Horizontal active area | - | HDISP | -- | 720 | -- | DCK |

## 6.9 Reset input timing

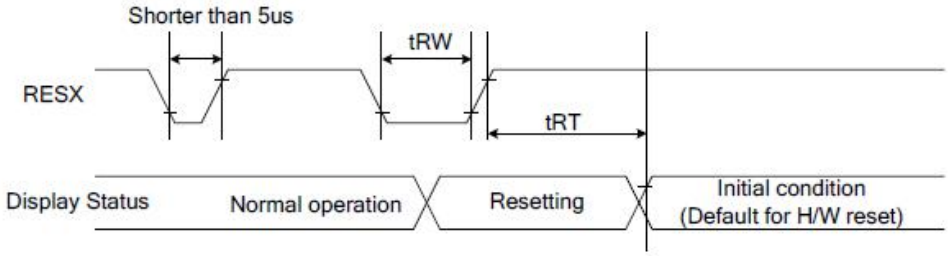



**Figure 126: Reset Timing**

**Table 47: Reset Timing**

| Signal | Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|
| RESX | tRW | Reset pulse duration | 10 | | uS |
| | tRT | Reset cancel | | 5 (note 1,5) | mS |
| | | | | 120 (note 1,6,7) | mS |

***Notes:***

1. *The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.*
2. *Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 48.*

**Table 48: Reset Descript**

| RESX Pulse | Action |
|---|---|
| Shorter than 5us | Reset Rejected |
| Longer than 10us | Reset |
| Between 5us and 10us | Reset starts |

3. During the Resetting period, the display will be blanked (The display enters the blanking sequence, which maximum time is 120 ms, when Reset Starts in the Sleep Out mode. The display remains the blank state in the Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection can also be applied during a valid reset pulse, as shown below:

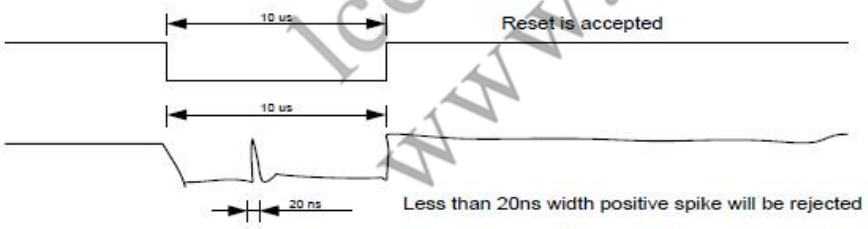



**Figure 127: Positive Noise Pulse during Reset Low**

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

# 7. CTP Specification

## 7.1 Electrical Characteristics

### 7.1.1 Absolute Maximum Rating

| Item | Symbol | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Power Supply Voltage | VDD | 2.66 | 3.47 | V | -- |
| Operating temperature | $T_{OP}$ | -20 | +70 | ℃ | -- |
| Storage temperature | $T_{ST}$ | -30 | +80 | ℃ | -- |

### 7.1.2 DC Electrical Characteristics (Ta=25℃)

(Ambient temperature:25℃, AVDD=2.8V, VDDIO=1.8V or VDDIO=AVDD)

| Item | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Normal mode operating current | -- | 8 | 14.5 | mA | |
| Green mode operating current | -- | 3.3 | -- | mA | |
| Sleep mode operating current | 70 | -- | 120 | uA | |
| Doze mode operating current | -- | 0.78 | -- | mA | |
| Digital Input low voltage/VIL | -0.3 | -- | 0.25*VDD | V | |
| Digital Input high voltage/VIH | 0.75*VDD | -- | VDD+0.3 | V | |
| Digital Output low voltage/VOL | -- | | 0.15*VDD | V | |
| Digital Output high voltage/VOH | 0.85*VDD | | | V | |

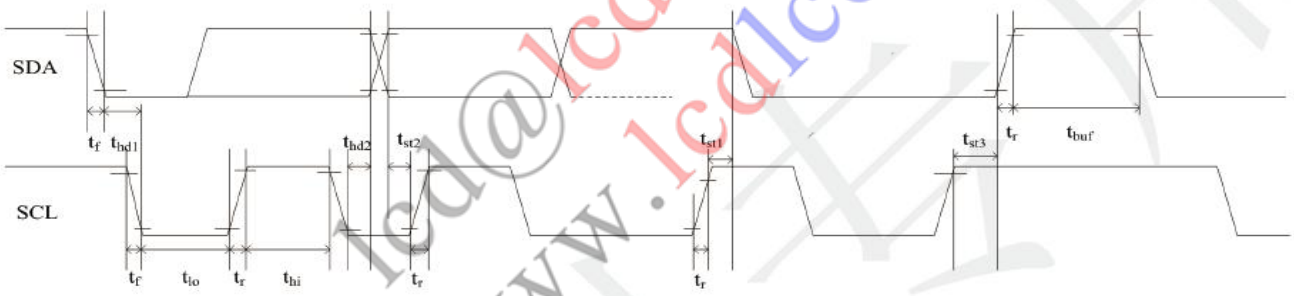
### 7.1.3 AC Characteristics

(Ambient temperature:25℃, AVDD=2.8V, VDDIO=1.8V)

| Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|
| OSC oscillation frequency | 59 | 60 | 61 | MHZ |
| I/O output rise time,low to high | - | 14 | - | ns |
| I/O output rfall time,high to low | - | 14 | - | ns |

### 7.2 I2C Timing

GT911 provides a standard I2C interface for SCL and SDA to communicate with the host. GT911 always serves as slave device in the system with all communication being initialized by the host. It is strongly recommended that transmission rate be kept at or below 400Kbps. The I2C timing is shown below:



**Test condition 1: 1.8V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor**

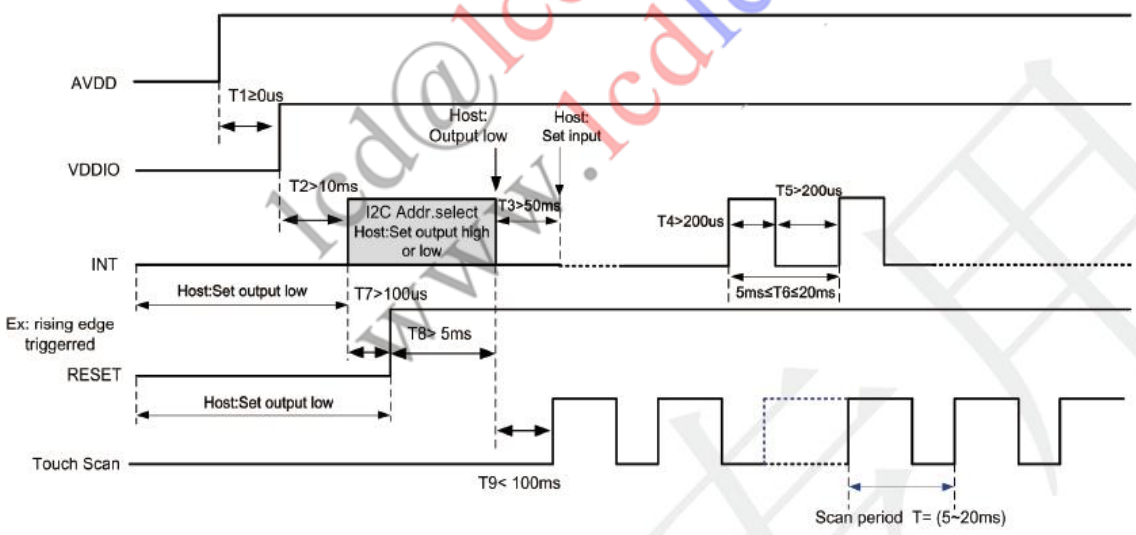
| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| SCL low period | $t_{lo}$ | 1.3 | - | us |
| SCL high period | $t_{hi}$ | 0.6 | - | us |
| SCL setup time for Start condition | $t_{st1}$ | 0.6 | - | us |
| SCL setup time for Stop condition | $t_{st3}$ | 0.6 | - | us |
| SCL hold time for Start condition | $t_{hd1}$ | 0.6 | - | us |
| SDA setup time | $t_{st2}$ | 0.1 | - | us |
| SDA hold time | $t_{hd2}$ | 0 | - | us |

**Test condition 2: 3.3V host interface voltage, 400Kbps transmission rate, 2K pull-up resistor**

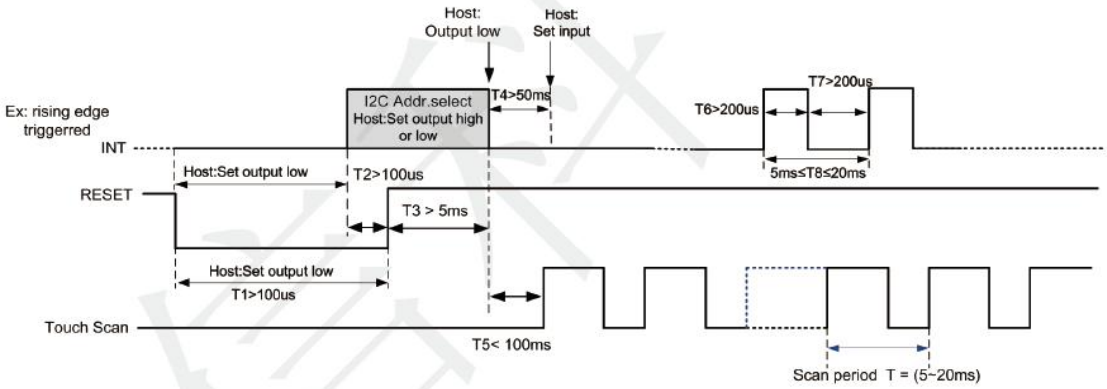
| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| SCL low period | $t_{lo}$ | 1.3 | - | us |
| SCL high period | $t_{hi}$ | 0.6 | - | us |
| SCL setup time for Start condition | $t_{st1}$ | 0.6 | - | us |
| SCL setup time for Stop condition | $t_{st3}$ | 0.6 | - | us |
| SCL hold time for Start condition | $t_{hd1}$ | 0.6 | - | us |
| SDA setup time | $t_{st2}$ | 0.1 | - | us |
| SDA hold time | $t_{hd2}$ | 0 | - | us |

GT911 supports two I2C slave addresses: 0xBA/0xBB and 0x28/0x29. The host can select the address by changing the status of Reset and INT pins during the power-on initialization phase. See the diagram below for configuration methods and timings:

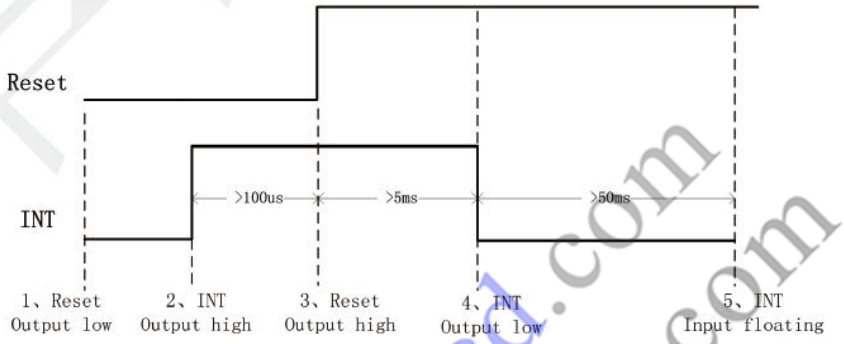
**Power-on Timing:**



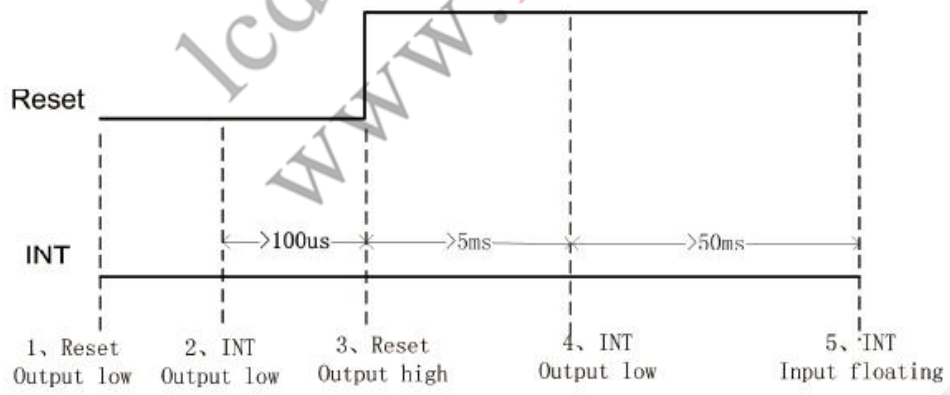
**Timing for host resetting GT911:**




**Timing for setting slave address to 0x28/0x29:**




**Timing for setting slave address to 0xBA/0xBB:**



**a) Data Transmission**

(For example：device address is 0xBA/0xBB)

Communication is always initiated by the host. Valid Start condition is signaled by pulling SDA line from "high" to "low" when SCL line is "high". Data flow or address is transmitted after the Start condition.

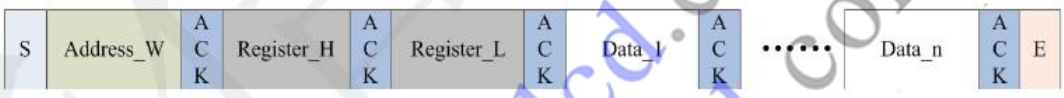
All slave devices connected to $I^2C$ bus should detect the 8-bit address issued after Start condition and send the correct ACK. After receiving matching address, GT911 acknowledges by configuring SDA line as output port and pulling SDA line low during the ninth SCL cycle. When receiving unmatched address, namely, not 0XBA or 0XBB, GT911 will stay in an idle state.

For data bytes on SDA, each of 9 serial bits will be sent on nine SCL cycles. Each data byte consists of 8 valid data bits and one ACK or NACK bit sent by the recipient. The data transmission is valid when SCL line is "high".

When communication is completed, the host will issue the STOP condition. Stop condition implies the transition of SDA line from "low" to "high" when SCL line is "high".

**b) Writing Data to GT911**

(For example：device address is 0xBA/0xBB)




**Timing for Write Operation**

The diagram above displays the timing sequence of the host writing data onto GT911. First, the host issues a Start condition. Then, the host sends 0XBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where writing starts) and the 8-bit data bytes (to be written onto the register).

The location of the register address pointer will automatically add 1 after every Write Operation. Therefore, when the host needs to perform Write Operations on a group of registers of continuous addresses, it is able to write continuously. The Write Operation is terminated when the host issues the Stop condition.

**c) Reading Data from GT911**

(For example：device address is 0xBA/0xBB)


**Timing for Read Operation**

The diagram above is the timing sequence of the host reading data from GT911. First, the host issues a Start condition and sends 0XBA (address bits and R/W bit; R/W bit as 0 indicates Write operation) to the slave device.

After receiving ACK, the host sends the 16-bit register address (where reading starts) to the slave device. Then the host sets register addresses which need to be read.

Also after receiving ACK, the host issues the Start condition once again and sends 0XBB (Read Operation). After receiving ACK, the host starts to read data.

GT911 also supports continuous Read Operation and, by default, reads data continuously. Whenever receiving a byte of data, the host sends an ACK signal indicating successful reception. After receiving the last byte of data, the host sends a NACK signal followed by a STOP condition which terminates communication.

# 8. LCD Module Out-Going Quality Level

## 8.1 VISUAL & FUNCTION INSPECTION STANDARD

### 8.1.1 Inspection conditions

Inspection performed under the following conditions is recommended.

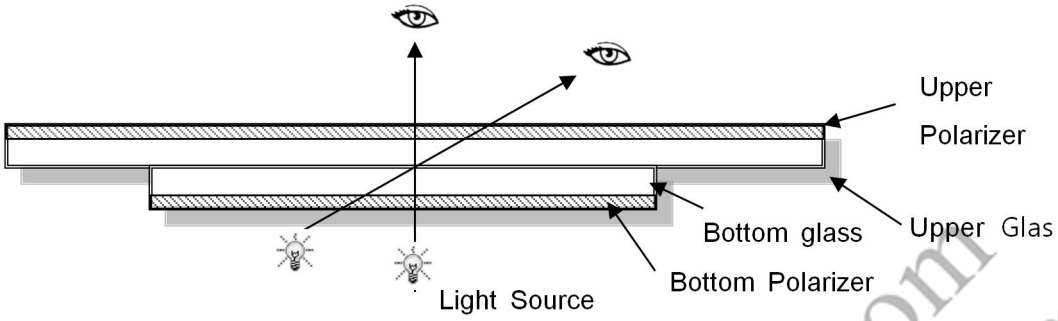
Temperature : 25±5℃

Humidity : 65%±10%RH

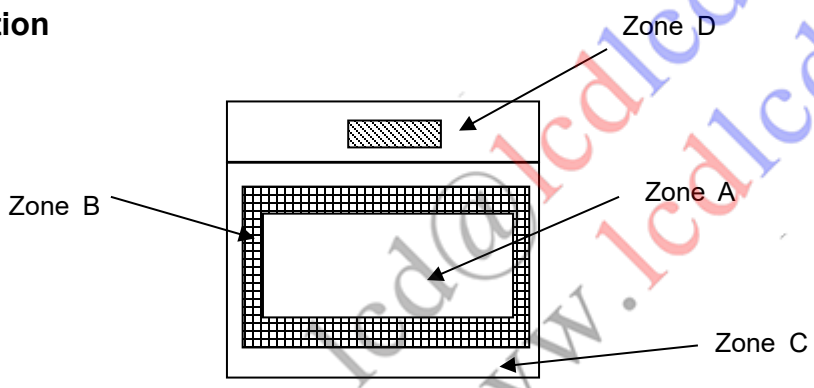
Viewing Angle : Normal viewing Angle.

Illumination: Single fluorescent lamp (300 to 700Lux)

Viewing distance:30-50cm




### 8.1.2 Definition




Zone A : Effective Viewing Area(Character or Digit can be seen)

Zone B : Viewing Area except Zone A

Zone C Cover (Zone A+Zone B) which can not be seen after assembly by customer .)

Zone D : IC Bonding Area

Note:As a general rule ,visual defects in Zone C can be ignored when it doesn't effect product function or appearance after assembly by customer

### 8.1.3 Sampling Plan

According to GB/T 2828-2003 ; , normal inspection, Class Ⅱ

AQL:

| Major defect | Minor defect |
|---|---|
| 0.65 | 1.5 |

LCD: Liquid Crystal Display , LCM: Liquid Crystal Module, CTP: Capacitive Touch Panel

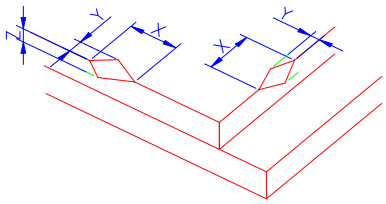
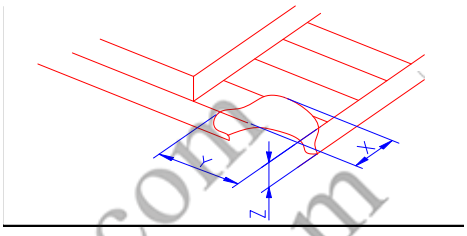
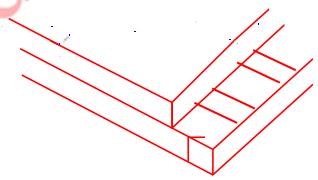
| No | Items to be inspected | Criteria | Classification of defects |
|---|---|---|---|
| 1 | Functional defects | 1) No display, Open or miss line<br>2) Display abnormally, Short<br>3) Backlight no lighting, abnormal lighting. etc | Major |
| 2 | Missing | Missing components and etc | |
| 3 | Outline dimension | Overall outline dimension beyond the drawing is not allowed,deformation and etc | |
| 4 | Color tone | Color unevenness, refer to limited sample | Minor |
| 5 | Spot/Line defect | Light dot,Dim spot,(Note1)<br>Polarizer Air Bubble,<br>Polarizer accidented spot and etc | |
| 6 | Soldering appearance | Good soldering , Peeling off is not allowed and etc | |
| 7 | LCD/Polarizer/CTP | Black/White spot/line, scratch, crack, etc. | |



**Note1:** a) Light dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

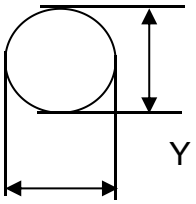
b) Dim dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

### 8.1.4 Criteria (Visual)

<table>
<tr><th>Number</th><th>Items</th><th>Criteria(mm)</th></tr>
<tr><td rowspan="3">1.0 LCD Crack/Broken<br>NOTE:<br>X: Length<br>Y: Width<br>Z: Height<br>L: Length of ITO,<br>T: Height of LCD</td><td>(1) The edge of LCD broken</td><td>  <br><table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td><Inner border line of the seal</td><td>≤T</td></tr></table></td></tr>
<tr><td>(2)LCD corner broken</td><td>  <br><table><tr><th>X</th><th>Y</th><th>Z</th></tr><tr><td>≤3.0mm</td><td>≤L</td><td>≤T</td></tr></table></td></tr>
<tr><td>(3) LCD crack</td><td>  <br>Crack<br>Not allowed</td></tr>
</table>

2.0

Spot defect




Φ=(X+Y)/2

① light dot ( black/white spot , pinhole, stain, etc. )

| Zone / Size (mm) | Acceptable Qty | | |
|---|---|---|---|
| | A | B | C |
| Φ≤0.15 | Ignore | Ignore | |
| 0.15<Φ≤0.25 | 3(distance≧10mm) | | |
| 0.25<Φ≤0.4 | 2(distance≧10mm) | | |
| Φ>0.4 | 0 | | |

② Dim spot ( light leakage、dent、dark spot, etc )

| Zone / Size (mm) | Acceptable Qty | | |
|---|---|---|---|
| | A | B | C |
| Φ≤0.15 | Ignore | Ignore | |
| 0.15<Φ≤0.25 | 3( distance≧10mm) | | |
| 0.25<Φ≤0.4 | 2( distance≧10mm) | | |
| Φ>0.4 | 0 | | |

③ Polarizer accidented spot

| Zone / Size (mm) | Acceptable Qty | | |
|---|---|---|---|
| | A | B | C |
| Φ≤0.2 | Ignore | | Ignore |
| 0.2<Φ≤0.5 | 2( distance≧10mm) | | |
| Φ>0.5 | 0 | | |

④Polarizer Bubble

| Zone / Size (mm) | Acceptable Qty | | |
|---|---|---|---|
| | A | B | C |
| Φ≤0.2 | Ignore | | Ignore |
| 0.2<Φ≤0.4 | 2(distance≧10mm) | | |
| Φ>0.4 | 0 | | |

3.0 LCD Pixel defect

Pixel bad points

| Item | Zone A | Acceptable Qt |
|---|---|---|
| Bright dot | Random | N≤2 |
| | 2 dots adjacent | N≤0 |
| | 3 dots adjacent | N≤0 |
| Dark dot | Random | N≤3 |
| | 2 dots adjacent | N≤0 |
| | 3 dots adjacent | N≤0 |
| Distance | 1. Minimum Distance Between Bright dots.<br>2. Minimum Distance Between dark dots<br>3. Minimum Distance Between dark and bright dot. | 5mm |
| Total bright and dark dot | | N≤4 |

Note:

A) Bright dot：Dots appear bright and unchanged in size in which LCD panel is displaying under black pattern.

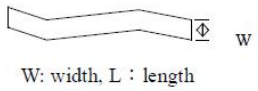
B) Dark dot: Dots appear dark and unchanged in size in which LCD panel is displaying under pure red, green, blue picture.

C) 2 dot adjacent = 1 pair = 2 dots

Picture:

2 dot adjacent　　2 dot adjacent

2 dot adjacent (vertical)　　2 dot adjacent (slant)

<table>
<tr>
<td>4.0</td>
<td>Line defect (LCD /Polarizer backlight black/white line, scratch, stain)<br>  <br><br>N：Count</td>
<td>
<table>
<tr><th rowspan="2">Width(mm)</th><th rowspan="2">Length(mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.05</td><td>Ignore</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.05<W≤0.06</td><td>L≤5.0</td><td colspan="2">N≤3</td></tr>
<tr><td>0.06<W≤0.08</td><td>L≤4.0</td><td colspan="2">N≤2</td></tr>
<tr><td>W>0.08</td><td colspan="4">Define as spot defect</td></tr>
</table>
</td>
</tr>
<tr>
<td>5.0</td>
<td>Electronic Components SMT.</td>
<td>Not allow missing parts，solderless connection，cold solder joint，mismatch，The positive and negative polarity opposite</td>
</tr>
<tr>
<td>6.0</td>
<td>Display color& Brightness.</td>
<td>1. Color：Measuring the color coordinates, The measurement standard according to the datasheet or samples.<br>2. Brightness：Measuring the brightness of White screen, The measurement standard according to the datasheet or Samples.</td>
</tr>
<tr>
<td>7.0</td>
<td>LCD Mura/Waving/ Hot spot</td>
<td>Not visible through 5% ND filter in 50% gray or judge by limit sample if necessary.</td>
</tr>
<tr>
<td>8.0</td>
<td>CTP Related</td>
<td>CTP Cover sensor accidented black/white spot</td>
<td>
<table>
<tr><th rowspan="2">Size Φ(mm)</th><th colspan="3">Acceptable Qty</th></tr>
<tr><th>A</th><th>B</th><th>C</th></tr>
<tr><td>Φ≤0.15</td><td colspan="2">Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td>0.15<Φ≤0.25</td><td colspan="2">1 ( distance ≥ 10mm )</td></tr>
<tr><td>0.25<Φ≤0.35</td><td colspan="2">2 ( distance ≥ 10mm )</td></tr>
<tr><td>Φ>0.35</td><td colspan="2">0</td><td></td></tr>
</table>
</td>
</tr>
</table>

**CTP Cover scratch**

| Width(mm) | Ignore (mm) | Acceptable Qty | | |
|---|---|---|---|---|
| | | A | B | C |
| Φ≤0.05 | Ignore | Ignore | | |
| 0.05<W≤0.06 | L≤4.0 | N≤3 | | |
| 0.06<W≤0.08 | L≤3.0 | N≤2 | | |
| 0.08<W | Define as spot defect | | | |

**CTP Cover Pinhole/ Lack of ink**

| Zone / Size (mm) | Acceptable Qty |
|---|---|
| | C |
| Φ≤0.2 | Ignore |
| 0.2<Φ≤0.3 | 4(distance≧10mm) |
| 0.3<Φ≤0.4 | 2(distance≧10mm) |
| Φ>0.4 | 0 |

**CTP Bonding bubble/ accidented spot**

| Size Φ(mm) | Acceptable Qty | |
|---|---|---|
| | A | B |
| Φ≤0.1 | Ignore | |
| 0.1<Φ≤0.2 | [illegible] | |
| 0.2<Φ≤0.3 | [illegible] | |
| Φ>0.3 | 0 | |

**Assembly deflection**

beyond the edge of backlight ≤0.2mm

**CTP cover broken**

X : length

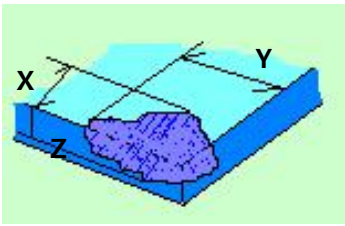
Y : width

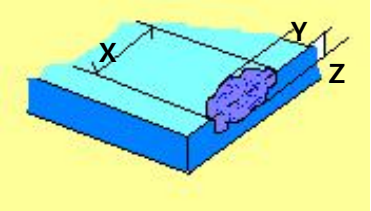
Z : height

| X | Y | Z |
|---|---|---|
| X≤0.5mm | Y≤0.5mm | Z<cover thickness |

*

Circuitry broken is not allowed.



| | | | | |
|---|---|---|---|---|
| | | CTP cover broken<br>X : length<br>Y : width<br>Z : height | X: X≤0.3mm; Y: Y≤0.3mm; Z: Z<cover thickness<br>* Circuitry broken is not allowed. |  |

Criteria ( functional items)

| Number | Items | Criteria (mm) |
|---|---|---|
| 1 | No display | Not allowed |
| 2 | Missing segment | Not allowed |
| 3 | Short | Not allowed |
| 4 | Backlight no lighting | Not allowed |
| 5 | CTP no function | Not allowed |

## 9. Reliability Test Result

| Item | Condition | Inspection after test |
|---|---|---|
| High Temperature Operating | 70℃,96H | Inspection after 2~4hours storage at room temperature, the sample shall be free from defects:<br>1.Air bubble in the LCD;<br>2.Non-display;<br>3.Missing segments/line;<br>4.Glass crack;<br>5.Current IDD is twice higher than initial value. |
| Low Temperature Operating | -20℃, 96HR | |
| High Temperature Storage | 80℃, 96HR | |
| Low Temperature Storage | -30℃, 96HR | |
| High Temperature & High Humidity Operating | +60℃, 90% RH ,96 hours. | |
| Thermal Shock (Non-operation) | -30℃,30 min ↔ +80℃,30 min,<br>Change time:5min 20CYC. | |
| ESD test | C=150pF, R=330,5points/panel<br>Air:±8KV, 5times; Contact:±6KV, 5 times; | |
| Vibration (Non-operation) | Frequency range:10~55Hz, Stroke:1.5mm<br>Sweep:10Hz~55Hz~10Hz 2 hours for each direction of | |
| Box Drop Test | 1 Corner 3 Edges 6 faces,80㎝(MEDIUM BOX) | |

Remark:

1.The test samples should be applied to only one test item.

2.Sample size for each test item is 5~10pcs.

3.For Damp Proof Test, Pure water(Resistance > 10MΩ) should be used.

4.In case of malfunction defect caused by ESD damage, if it would be recovered to normal state after resetting, it would be judged as a good part.

5.Failure Judgment Criterion: Basic Specification, Electrical Characteristic, Mechanical Characteristic, Optical Characteristic.

6. The color fading mura of polarizing filter should not care.

# 10. Cautions and Handling Precautions

## 10.1 Handling and Operating the Module

(1) When the module is assembled, it should be attached to the system firmly.
Do not warp or twist the module during assembly work.
(2) Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
(3) Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
(4) Do not allow drops of water or chemicals to remain on the display surface.
If you have the droplets for a long time, staining and discoloration may occur.
(5) If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
(6) The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane.
Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
(8) Protect the module from static; it may cause damage to the CMOS ICs.
(9) Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
(10) Do not disassemble the module.
(11) Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
(12) Pins of I/F connector shall not be touched directly with bare hands.
(13) Do not connect, disconnect the module in the “Power ON” condition.
(14) Power supply should always be turned on/off by the item 6.1 Power On Sequence &6.2 Power Off Sequence

## 10.2 Storage and Transportation.

(1) Do not leave the panel in high temperature, and high humidity for a long time.
It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
(2) Do not store the TFT-LCD module in direct sunlight.
(3) The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
(4) It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module.
In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
(5) This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.

## 11. Packing

----TBD----------