Hex Inverter

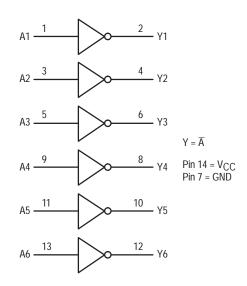
With LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

The MC74HCT04A may be used as a level converter for interfacing TTL or NMOS outputs to High–Speed CMOS inputs.

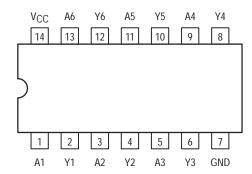
The HCT04A is identical in pinout to the LS04.

- Output Drive Capability: 10 LSTTL Loads
- TTL/NMOS-Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5V
- Low Input Current: 1µA
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 48 FETs or 12 Equivalent Gates

LOGIC DIAGRAM

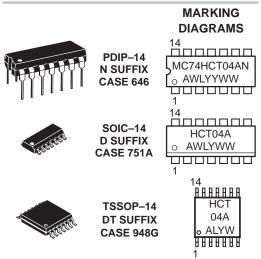


Pinout: 14-Lead Packages (Top View)





http://onsemi.com



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year

WW or W = Work Week

FUNCTION TABLE

Inputs	Outputs
Α	Υ
L	Н
Н	L

ORDERING INFORMATION

	_	_
Device	Package	Shipping
MC74HCT04AN	PDIP-14	2000 / Box
MC74HCT04AD	SOIC-14	55 / Rail
MC74HCT04ADR2	SOIC-14	2500 / Reel
MC74HCT04ADT	TSSOP-14	96 / Rail
MC74HCT04ADTR2	TSSOP-14	2500 / Reel

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
VCC	DC Supply Voltage (Referenced to GND)	- 0.5 to + 7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	- 0.5 to V _{CC} + 0.5	V
lin	DC Input Current, per Pin	± 20	mA
l _{out}	DC Output Current, per Pin	± 25	mA
ICC	DC Supply Current, V _{CC} and GND Pins	± 50	mA
PD	Power Dissipation in Still Air Plastic DIP† SOIC Package† TSSOP Package†	750 500 450	mW
T _{stg}	Storage Temperature Range	- 65 to + 150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds Plastic DIP, SOIC or TSSOP Package	260	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND \leq (V_{in} or V_{out}) \leq V_{CC} .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

 $\label{problem} \mbox{Functional operation should be restricted to the Recommended Operating Conditions}.$

SOIC Package: - 7 mW/°C from 65° to 125°C

TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
VCC	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	Vcc	V
TA	Operating Temperature Range, All Package Types	- 55	+ 125	°C
t _r , t _f	Input Rise/Fall Time (Figure 1)	0	500	ns

^{*}Maximum Ratings are those values beyond which damage to the device may occur.

[†]Derating — Plastic DIP: – 10 mW/°C from 65° to 125°C

DC CHARACTERISTICS (Voltages Referenced to GND)

	l v		vcc	Guara	nteed Lin		
Symbol	Parameter	Condition	V	–55 to 25°C	≤85°C	≤125°C	Unit
VIH	Minimum High–Level Input Voltage	$V_{Out} = 0.1V$ $ I_{Out} \le 20\mu A$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V _{IL}	Maximum Low–Level Input Voltage	$V_{Out} = V_{CC} - 0.1V$ $ I_{Out} \le 20\mu A$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
VOH	Minimum High-Level Output Voltage	$V_{in} = V_{IL}$ $ I_{out} \le 20\mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{in} = V_{IL}$ $ I_{out} \le 4.0 \text{mA}$	4.5	3.98	3.84	3.70	
VOL	Maximum Low–Level Output Voltage	$V_{in} = V_{iH}$ $ I_{out} \le 20\mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{in} = V_{IH}$ $ I_{out} \le 4.0 \text{mA}$	4.5	0.26	0.33	0.40	
l _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	5.5	±0.1	±1.0	±1.0	μΑ
lcc	Maximum Quiescent Supply Current (per Package)	V _{in} = V _{CC} or GND l _{out} = 0μA	5.5	1	10	40	μА
ΔlCC	Additional Quiescent Supply Current	V _{in} = 2.4V, Any One Input		≥ –55 °C	25 to 1	25°C	
	Current	$V_{in} = V_{CC}$ or GND, Other Inputs $I_{out} = 0\mu A$	5.5	2.9	2.	4	mA

^{1.} Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

AC CHARACTERISTICS ($V_{CC} = 5.0V \pm 10\%$, $C_L = 50pF$, Input $t_f = t_f = 6ns$)

		Guaranteed Limit			
Symbol	Parameter	–55 to 25°C	≤85°C	≤125°C	Unit
tPLH, tPHL	Maximum Propagation Delay, Input A to Output Y (Figures 1 and 2)	15 17	19 21	22 26	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 2)	15	19	22	ns
C _{in}	Maximum Input Capacitance	10	10	10	pF

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

		Typical @ 25°C, V _{CC} = 5.0 V		l
C_{PD}	Power Dissipation Capacitance (Per Inverter)*	22	pF	

^{*} Used to determine the no–load dynamic power consumption: $P_D = C_{PD} \ V_{CC}^2 f + I_{CC} \ V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High–Speed CMOS Data Book (DL129/D).

^{2.} Total Supply Current = $I_{CC} + \Sigma \Delta I_{CC}$.

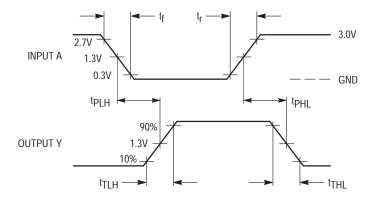
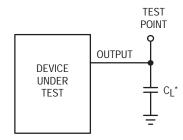


Figure 1. Switching Waveforms



*Includes all probe and jig capacitance

Figure 2. Test Circuit

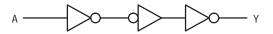
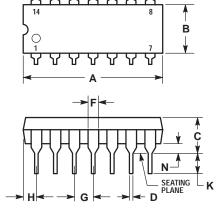


Figure 3. Expanded Logic Diagram (1/6 of the Device Shown)

PACKAGE DIMENSIONS

PDIP-14 **N SUFFIX** CASE 646-06 ISSUE L



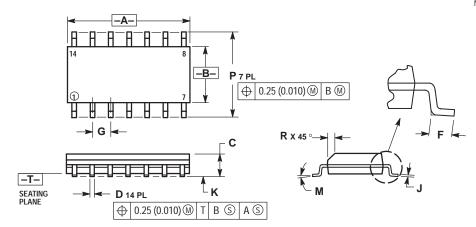


- NOTES:
 1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE
 POSITION AT SEATING PLANE AT MAXIMUM
 MATERIAL CONDITION.
 2. DIMENSION L TO CENTER OF LEADS WHEN
 FORMED PARALLEL.
 3. DIMENSION B DOES NOT INCLUDE MOLD

 - FLASH.
 4. ROUNDED CORNERS OPTIONAL

	INC	HES	MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	0.715	0.770	18.16	19.56	
В	0.240	0.260	6.10	6.60	
С	0.145	0.185	3.69	4.69	
D	0.015	0.021	0.38	0.53	
F	0.040	0.070	1.02	1.78	
G	0.100	BSC	2.54 BSC		
Н	0.052	0.095	1.32	2.41	
J	0.008	0.015	0.20	0.38	
K	0.115	0.135	2.92	3.43	
L	0.300	BSC	7.62 BSC		
M	0°	10°	0°	10°	
N	0.015	0.039	0.39	1 01	

SOIC-14 **D SUFFIX** CASE 751A-03 ISSUE F



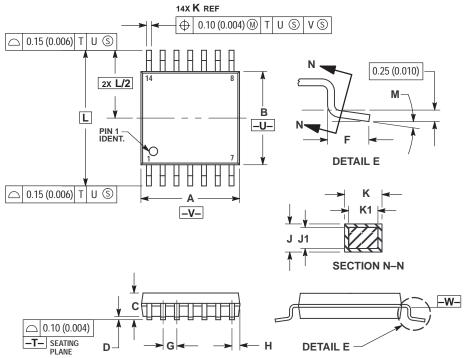
- NOTES:
 1. DIMENSIONING AND TOLERANCING PER ANSI 1. DIMENSIONING AND TOLERANCING PER ANS Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION ALLOWARD F. DAMBAR.

- PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIN	METERS	INCHES		
DIM	MIN	MAX	MIN	MAX	
Α	8.55	8.75	0.337	0.344	
В	3.80	4.00	0.150	0.157	
С	1.35	1.75	0.054	0.068	
D	0.35	0.49	0.014	0.019	
F	0.40	1.25	0.016	0.049	
G	1.27	BSC	0.050 BSC		
J	0.19	0.25	0.008	0.009	
K	0.10	0.25	0.004	0.009	
M	0 °	7°	0 °	7°	
Р	5.80	6.20	0.228	0.244	
R	0.25	0.50	0.010	0.019	

PACKAGE DIMENSIONS

TSSOP-14 **DT SUFFIX** CASE 948G-01 **ISSUE O**



- IES:
 DIMENSIONING AND TOLERANCING PER ANSI
 Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
 DIMENSION A DOES NOT INCLUDE MOLD FLASH,
 PROTRUSIONS OR GATE BURRS. MOLD FLASH
 OR GATE BURRS SHALL NOT EXCEED 0.15
- OR GATE BURRS SHALL NOT EXCEED 0.15
 (0.006) PER SIDE.
 DIMENSION B DOES NOT INCLUDE INTERLEAD
 FLASH OR PROTRUSION. INTERLEAD FLASH OR
 PROTRUSION SHALL NOT EXCEED
 0.25 (0.010) PER SIDE.
 DIMENSION K DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN
 EXCESS OF THE K DIMENSION AT MAXIMUM
 MATERIAL CONDITION. MATERIAL CONDITION.
 TERMINAL NUMBERS ARE SHOWN FOR
- REFERENCE ONLY.
 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	4.90	5.10	0.193	0.200	
В	4.30	4.50	0.169	0.177	
С		1.20		0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026 BSC		
Н	0.50	0.60	0.020	0.024	
J	0.09	0.20	0.004	0.008	
J1	0.09	0.16	0.004	0.006	
Κ	0.19	0.30	0.007	0.012	
K1	0.19	0.25	0.007	0.010	
L	6.40		0.252 BSC		
M	0°	8°	0°	8°	

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Device MC74HCT04A

Hex Inverter with LSTTL Compliant Input

With LSTTL-Compatible Inputs High-Performance Silicon-Gate CMOS

The MC74HCT04A may be used as a level converter for interfacing TTL or NMOS outputs to High-Speed CMOS inputs.

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Features:

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- Outputs Directly Interface to CMOS, NMOS and TTL
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- Low Input Current: 1μA
- In Compliance With the JEDEC Standard No. 7A Requirements
- Chip Complexity: 48 FETs or 12 Equivalent Gates

Orderable Parts

Action	Orderable Part	Short Desc.	Package Desc.	Pin Count	Case Outline	<u>Status</u>	Price/Unit	Pack Qty
N/A	MC74HCT04AD	Hex Inverter with TTL	SOIC	14	751A-03	Active	\$0.160	55

		Compilant Input						
N/A	MC74HCT04ADR2	Tape and Reel	SOIC	14	<u>751A-03</u>	Active	\$0.160	2500
N/A	MC74HCT04AFEL	Tape and Reel	SOIC EIAJ	14	940A-03	Active	\$0.160	2000
N/A	MC74HCT04AFL1	Tape and Reel	SOIC EIAJ	14	940A-03	LifeTime		
N/A	MC74HCT04ADT	Hex Inverter with TTL Compliant Input	TSSOP	14	948G-01	Active	\$0.200	96
N/A	MC74HCT04ADTR2	Tape and Reel	TSSOP	14	948G-01	Active	\$0.200	2500
N/A	MC74HCT04AF	Hex Inverter with TTL Compliant Input	SOIC EIAJ	14	<u>940A-03</u>	Active	\$0.160	50
N/A	MC74HCT04AN	Hex Inverter with TTL Compliant Input	PDIP	14	646-06	Active	\$0.160	500

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