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**Cannonlake** (formerly **Skymont**) is [Intel's codename](/wiki/List_of_Intel_codenames) for the [10-nanometer](/wiki/10_nanometer) die shrink of the [Kaby Lake](/wiki/Kaby_Lake) [microarchitecture](/wiki/Microarchitecture), expected to be released in the second half of 2017.[[1]](#cite_note-1)[[2]](#cite_note-2) As a die shrink, Cannonlake is a new process in Intel's "[Process-Architecture-Optimization](/wiki/Intel_Tick-Tock)" execution plan as the next step in semiconductor fabrication.[[3]](#cite_note-3) Cannonlake will be used in conjunction with Intel *200 Series* chipsets, also known as *Union Point*. The platform as a whole will be named *Union Bay*.[[3]](#cite_note-3) It has been speculated for a long time that reaching smaller [process nodes](/wiki/Process_node) would become impractical, leading to the end of [Moore's Law](/wiki/Moore's_Law). Intel however believes that it will be possible to reach at least 7 nm, though it will perhaps require use of materials other than silicon,[[4]](#cite_note-4) such as [indium gallium arsenide](/wiki/Indium_gallium_arsenide) (InGaAs).

The successors of the Cannonlake microarchitecture will be [Icelake](/wiki/Icelake) (2018) and [Tigerlake](/wiki/Tigerlake) (2019), which will represent Architecture and Optimization of the [Intel Process-Architecture-Optimization Model](/wiki/Intel_Tick-Tock).[[5]](#cite_note-5)[[6]](#cite_note-6)

## Features[[edit](/index.php?title=(none)&action=edit&section=1)]

* 200 Series chipset (Union Point)
* [Thermal design power](/wiki/Thermal_design_power) (TDP) up to 95 W (LGA 1151)

## See also[[edit](/index.php?title=(none)&action=edit&section=2)]

* [List of Intel CPU microarchitectures](/wiki/List_of_Intel_CPU_microarchitectures)

## References[[edit](/index.php?title=(none)&action=edit&section=3)]

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