Advanced VLSI Project – stage 5

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1. Reminder

So far, we have covered four stages:

- Synthesis stage – converting our RTL into logical cells
- STA stage – analyzing the timing constraints of our design.
- Floorplan – planning how we would want our chip to be constructed in a general view.
- Placement – place all the cells in a specific location (and some timing analysis practice).

In the current stage (CTS – Clock Tree Synthesis) we want to connect to every sequential cell the relevant clock specified by the RTL.

2. Setup

As we explained in previous stages of the project, we would like to copy the files for stage 5 from Elad's directory using the command:

```
cp -r /project/advvlsi/users/eladsimanian/ws/bitcoin/stage5 .
```

As explained in stage 3's document, you will work with a given NDM directories in this section too. For additional instruction on how to work with NDM directories please revisit the previous stage.

Reminder: in the previous assignment (Bitcoin_Intro_Stage1.pdf) we introduce these instructions in more detail.

3. Stage 5: CTS (Clock Tree Synthesis)

The Clock Tree Synthesis (CTS) stage is a critical step in the physical design process of a chip, particularly in synchronous digital designs. Once we have completed the Placement stage, the CTS stage involves synthesizing a network of clock distribution paths that connect the clock source to all the clocked elements in the design. This stage determines the skew and delay of the clock signal as it travels through the chip and ensures that each sequential element receives a clock signal at the correct time.

In our project, we have already completed the Placement stage for our bitcoin block, and now we need to perform the CTS stage to optimize the clock distribution network. The objective is to minimize clock skew and delay, which can negatively affect the timing and performance of the design. We also need to ensure that the clock tree meets the specified timing and power constraints while minimizing the area and power consumption of the chip.

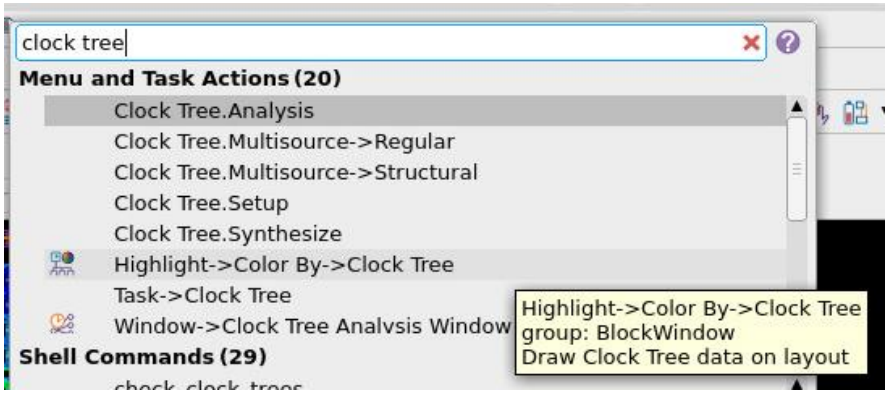
For your comfortable we marked all tasks needed for submission with:
[#P<Part_ID>_Q<Q_ID>] such as **[#P3.1_Q1]**

3.1 Warmup Questions

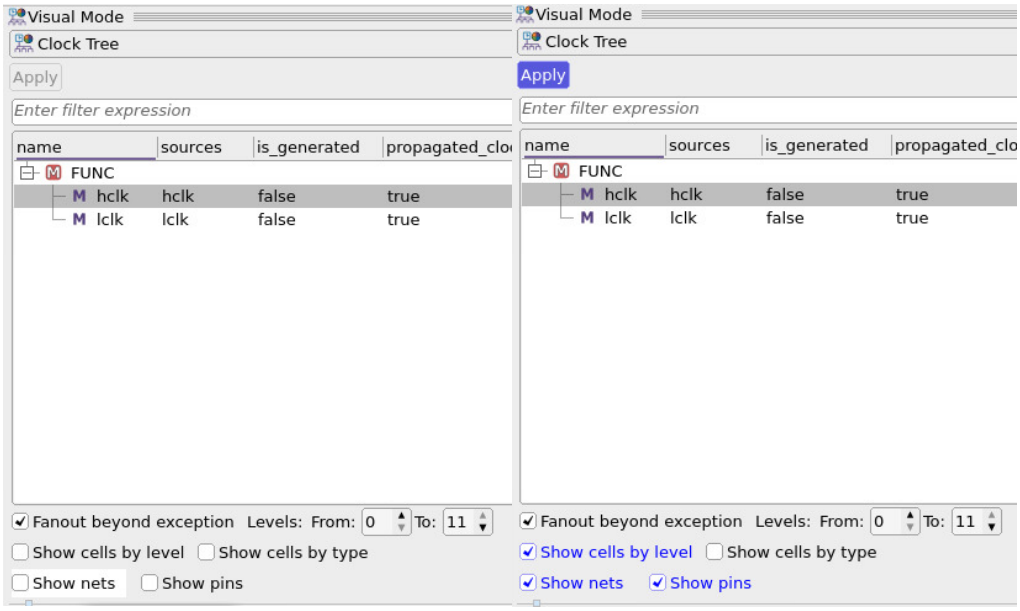
1. **[#P3.1_Q1]** What is the main goal of CTS? in your answer also discuss classic CTS and CCD.
2. **[#P3.1_Q2]** What is the role of clock buffers in the CTS stage, and how are they optimized to meet design constraints?
3. **[#P3.1_Q3]** Explain the following concepts:
   3.1. Skew – global and local
   3.2. Jitter
   3.3. PLL
4. **[#P3.1_Q4]** We discussed during the lecture about several approaches for clock trees. Choose one, describe it and explain its pros and cons (like mesh …)
5. **[#P3.1_Q5]** What are shielding and spacing techniques regarding the CTS stage?

3.2 CTS implementation

1. Open the NDM lib “bitcoin_stage_5” (see section “Working with NDM libraries” in previous project document for details).
2. This lib contains a similar snapshot of our design from the placement stage.
3. Run the commands one by one in the given script.
4. Export clock tree implementation:
   4.1. Search for “Clock tree” and selection the “Highlight -> Color By -> Clock Tree”

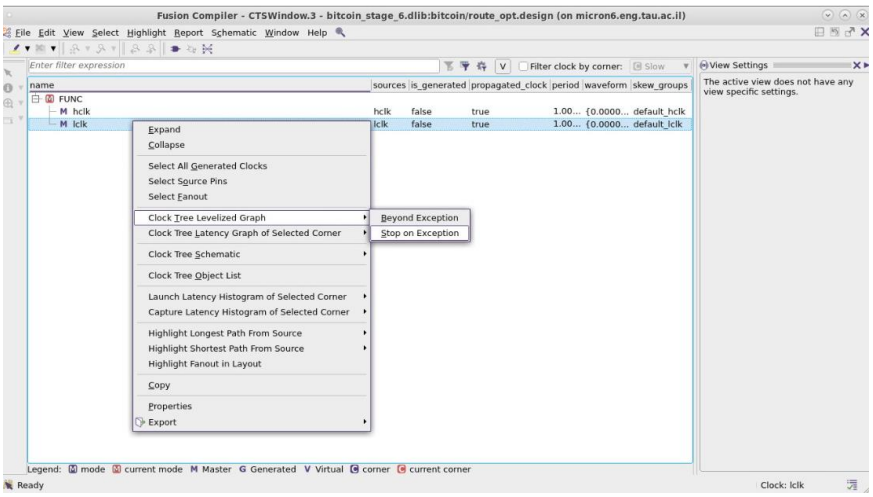


   4.2. In the “Visual Mode” / “Clock Tree” opened on the right side choose to show the cells, nets and pins, and press “Apply”:



   4.3. **[#P3.2_Q1]** Attach a print screen of the clock tree distribution
   4.4. **[#P3.2_Q2]** What is the skew of lclk and hclk? Is it high or low in your opinion?
   Hint: What is the clock period of the design?

4.5. Search for “Clock browser” and select the “View->clock browser”. Then, right click on each clock and select the “Clock Tree Levelized Graph -> Stop on Exception”



4.6. **[#P3.2_Q3]** Attach a print screen of each clock (lclk and hclk).

4. Submission

1. If the team approves the design functionality, the team lead, which has the updated work area with all the teams' files working, should submit the assignment as follows.
2. Submit to Moodle a zip:
   Let's say you are group advvlsi_15 then:
   bitcoin_stage5_advvlsi_15.zip

   The zip must include a PDF file:
   bitcoin_stage5_advvlsi_15.pdf

   the pdf should include the following:
   2.1. The stage name and number (Stage 5 – CTS)
   2.2. Workarea path, such as: /project/advvlsi/users/$user/ws/bitcoin_project
   2.3. Team's info: members name, id, usernames (in micron servers), tau emails
   2.4. Answers for all questions and tasks marked with "[#P<>Q<>]"

Good Luck.

P.S the next stage will deal with Routing!

Questions only

[#P3.1_Q1] What is the main goal of CTS? in your answer also discuss classic CTS and CCD.

[#P3.1_Q2] What is the role of clock buffers in the CTS stage, and how are they optimized to meet design constraints?

[#P3.1_Q3] Explain the following concepts:

- Skew – global and local
- Jitter
- PLL

[#P3.1_Q4] We discussed during the lecture about several approaches for clock trees. Choose one, describe it and explain its pros and cons (like mesh …)

[#P3.1_Q5] What are shielding and spacing techniques regarding the CTS stage?

[#P3.2_Q1] Attach a print screen of the clock tree distribution

[#P3.2_Q2] What is the clock period and clock skew of lclk and hclk?

Search `report_clock` and `report_clock_timing` in the Fusion Compiler program and find the commands to extract the skew and the clock period to answer those questions.

[#P3.2_Q3] Attach a print screen of each clock (lclk and hclk).