

# VLSI- FINAL PROJECT

## 4 BIT ALU DESIGN

### תקציר

בפרויקט זה התבקשנו לתקן ALU של 4 ביטים הנשלט על ידי OPCODE מהמשתמש ומבצע פעולות אריתמטיות שונות.

# תוכן עניינים

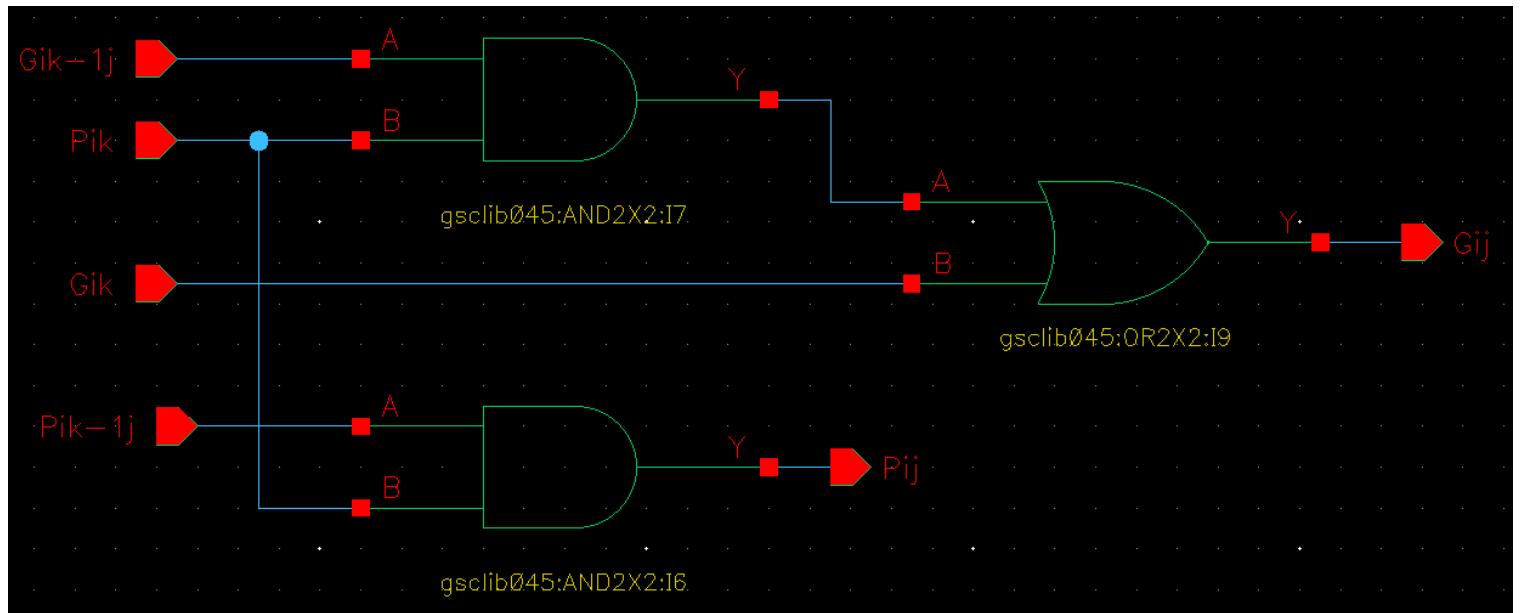
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We had created the following cells:

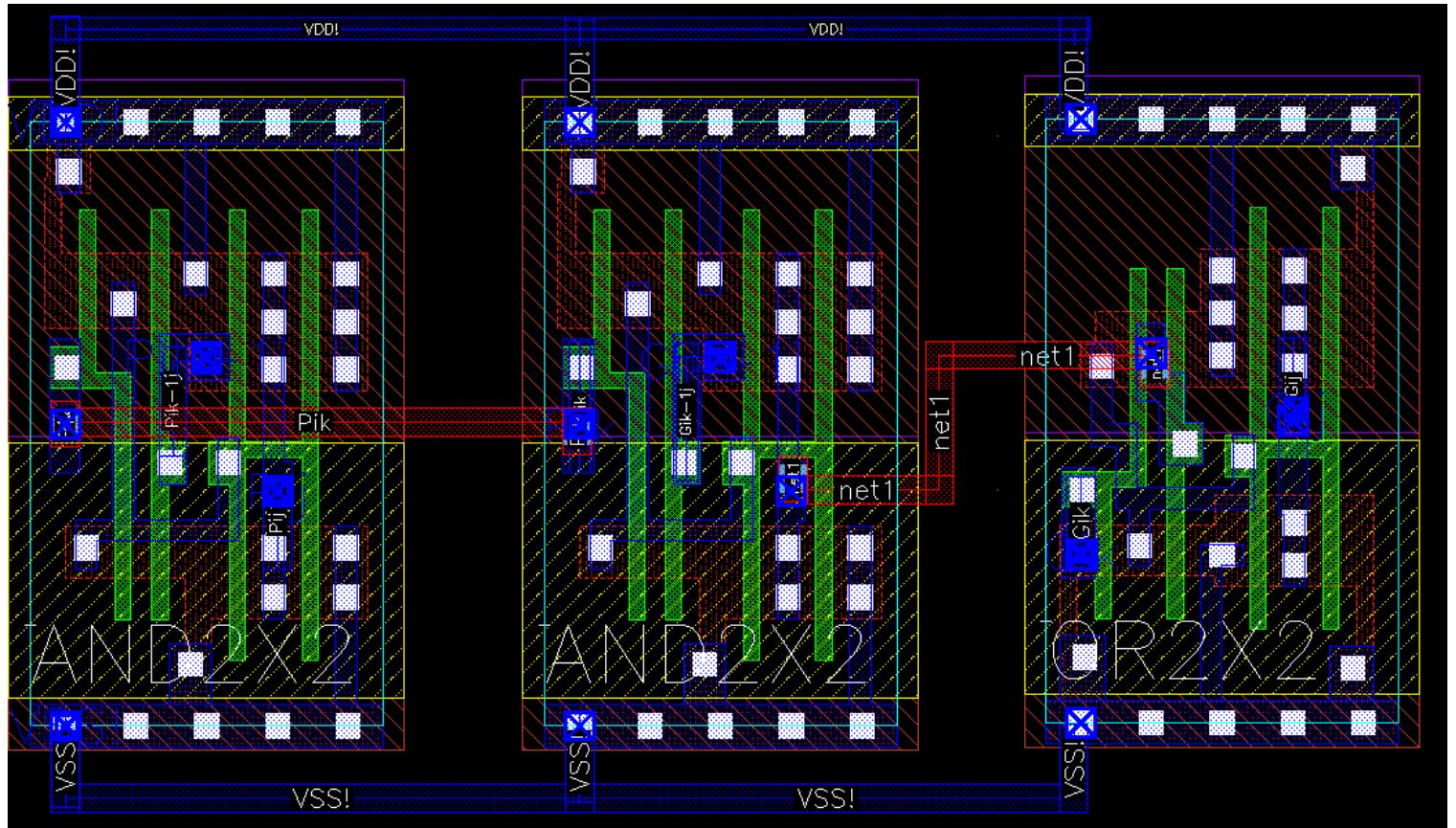
- Bitwise\_XOR.
- Bitwise\_PG.
- Gray\_cell.
- Black\_cell.
- Adder
- Register\_4bit
- OPCODE\_Register
- MUX2X1
- Demux4X16
- BSR
- Mux4\_1
- ALU

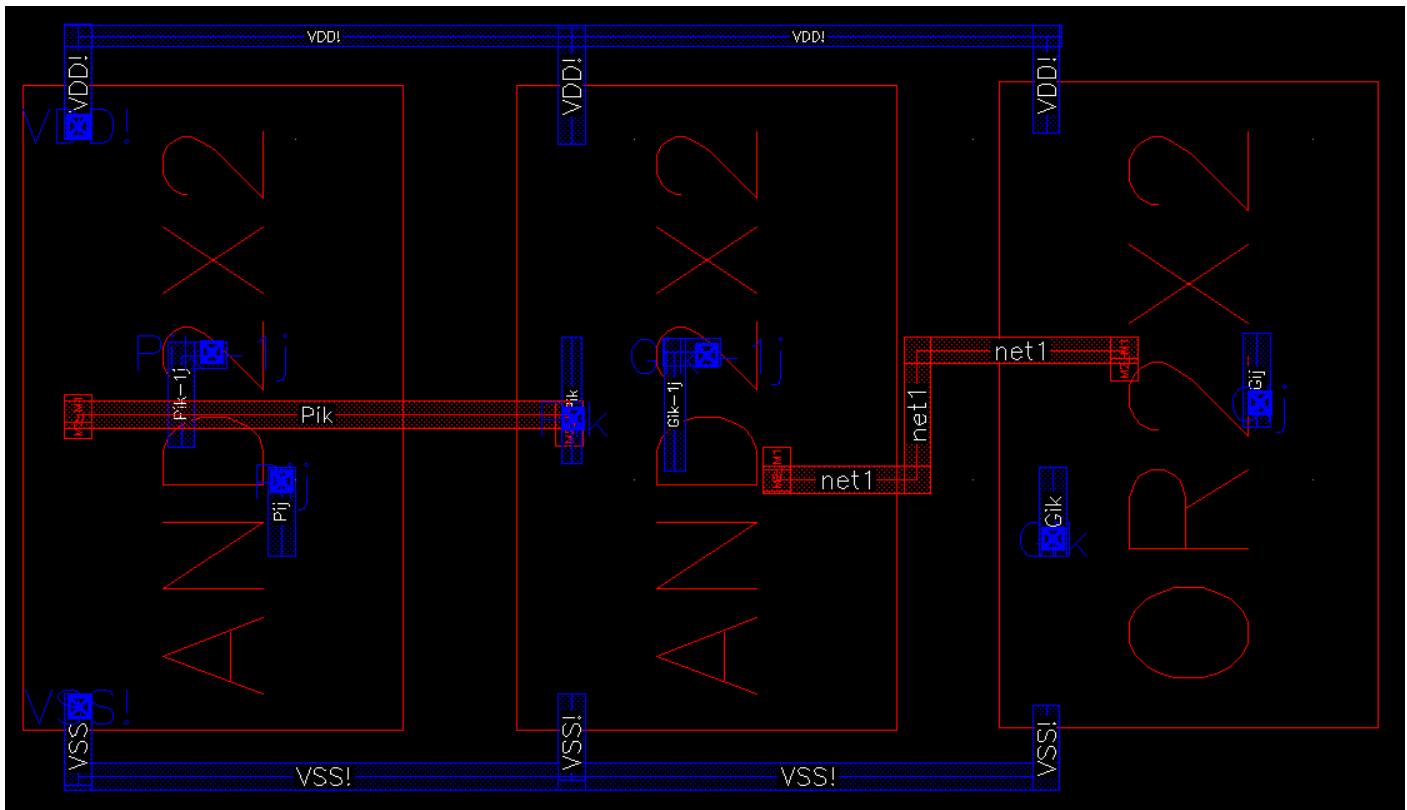
## Black cell

schematic:



layout:





## DRC:

```

PVS 22.21-64b Reports: Done [DRC] Black_cell... (on micron2.eng.tau.ac.il)

[DRC] Black_cell x

Total CPU Time : 2 (s)
Total Real Time : 3 (s)
Peak Memory Used : 19 (M)
Total Original Geometry : 135 (219)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file Black_cell.sum
ASCII report database is /project/gpdk45/users/orshaul/ws/PVS_RESULTS/DRC/Black_cell/Black_cell.ascii
Checking in all SoftShare licenses.

Design Rule Check Finished Normally. Sun Apr 14 22:45:30 2024

```

## LVS:

```

PVS 22.21-64b Reports: Done [LVS] Black_cell... (on micron2.eng.tau.ac.il)

[DRC] Black_cell x [LVS] Black_cell x

#####
# PVS Comparison Finished. Sun Apr 14 22:51:42 2024

Creating cross reference ...
*****
pvs_RCXref 22.21-s031 64 bit (Thu Apr 20 20:17:00 PDT 2023)
Build Ref No.: 031 Production (04-20-2023) {pvs_2221}

Copyright 2023 Cadence Design Systems, Inc.
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Build O/S: Linux x86_64 3.10.0-693.e17.x86_64
Executed on: micron2.eng.tau.ac.il (Linux x86_64 3.10.0-1160.92.1.e17.x86_64)
Process Id: 32015
Starting Time: Sun Apr 14 22:51:42 2024 (Sun Apr 14 19:51:42 2024 GMT)
With parameters: -format C -nxlf /project/gpdk45/users/orshaul/ws/PVS_RESULTS/LVS/Black_cell/svdb/Black_cell Black_cell.rep
****

Total CPU Time : 0 (s)
Total Real Time : 0 (s)
Memory Used : 88.11 (M)

pvs_RCXref Done
Checking in all SoftShare licenses.

```

PVS 22.21-64b LVS Run Stat...

ERC Results: Empty

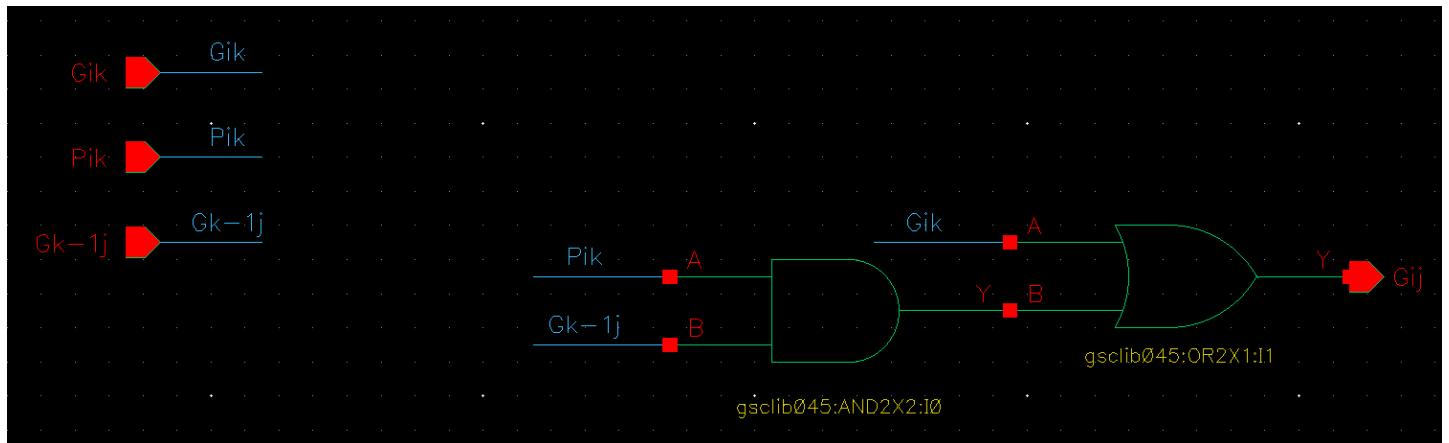
Extraction Results: Clean

Comparison Results: Match

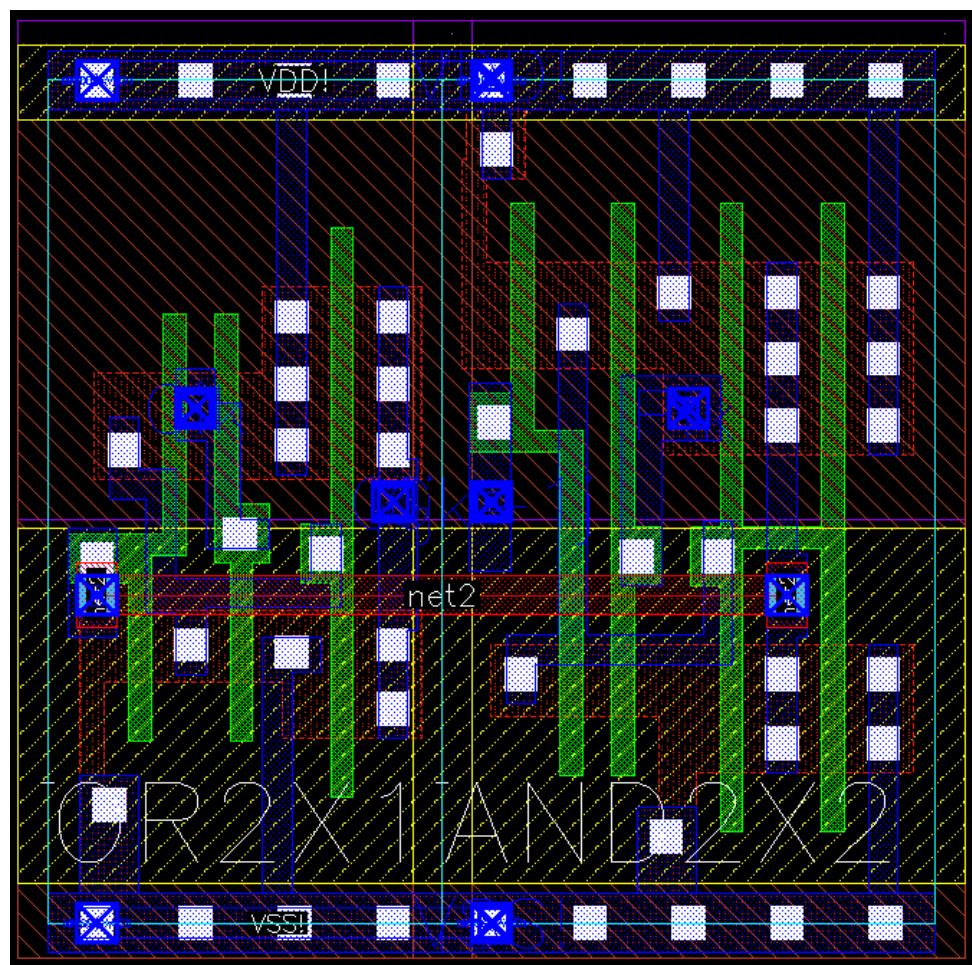
Do you want to start the LVS DE?

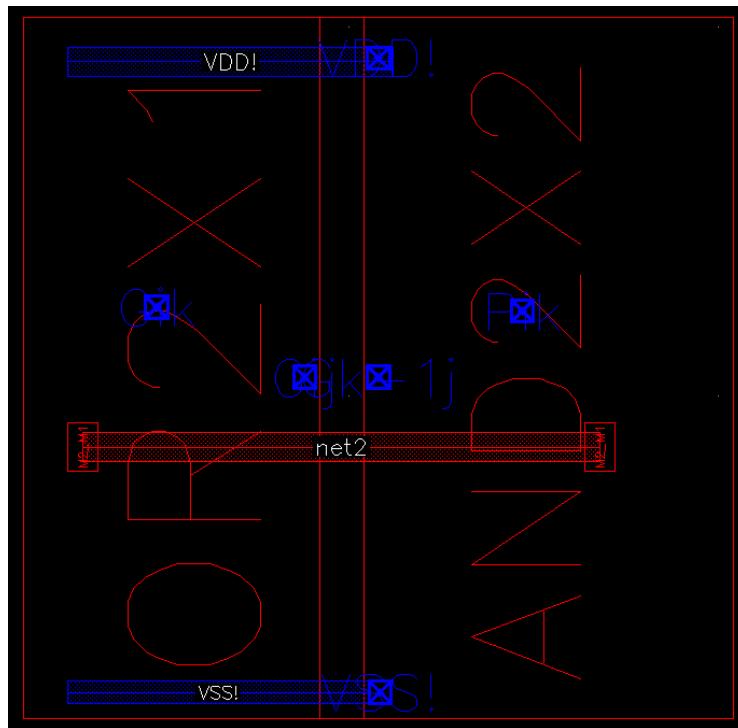
## Gray cell

### schematic:



### Layout:





### DRC:

```
PVS 22.21-64b Reports: Done [DRC] gray_cell... (on micron2.eng.tau.ac.il)
[DRC] gray_cell x

Total CPU Time          : 2 (s)
Total Real Time         : 2 (s)
Peak Memory Used       : 19 (M)
Total Original Geometry: 117 (120)
Total DRC RuleChecks   : 562
Total DRC Results      : 0 (0)
Summary can be found in file gray_cell.sum
ASCII report database is /project/gpdk45/users/orshaul/ws/PVS_RESULTS/DRC/gray_cell/gray_cell.ascii
Checking in all SoftShare licenses.

Design Rule Check Finished Normally. Sun Apr 14 23:13:32 2024
```

LVS:

[LVS]gray\_cell x

```
#
#####
#
PVS Comparison Finished. Sun Apr 14 23:20:36 2024

Creating cross reference ...
*****
pvs_RCXxref 22.21-s031 64 bit (Thu Apr 20 20:17:00 PDT 2023)
Build Ref No.: 031 Production (04-20-2023) [pvs_2221]

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Build O/S:      Linux x86_64 3.10.0-693.el7.x86_64
Executed on:    micron2.eng.tau.ac.il (Linux x86_64 3.10.0-1160.92.1.el7.x86_64)
Process Id:    22129
Starting Time: Sun Apr 14 23:20:36 2024 (Sun Apr 14 20:20:36 2024 GMT)
With parameters: -format C -nxf -ixf /project/gpdk45/users/orshaul/ws/PVS_RESULTS/LVS/gray_cell/svdb/gray_cell gray_cell.rep
*****
```

Total CPU Time : 0(s)  
Total Real Time : 0(s)  
Memory Used : 86.18(M)

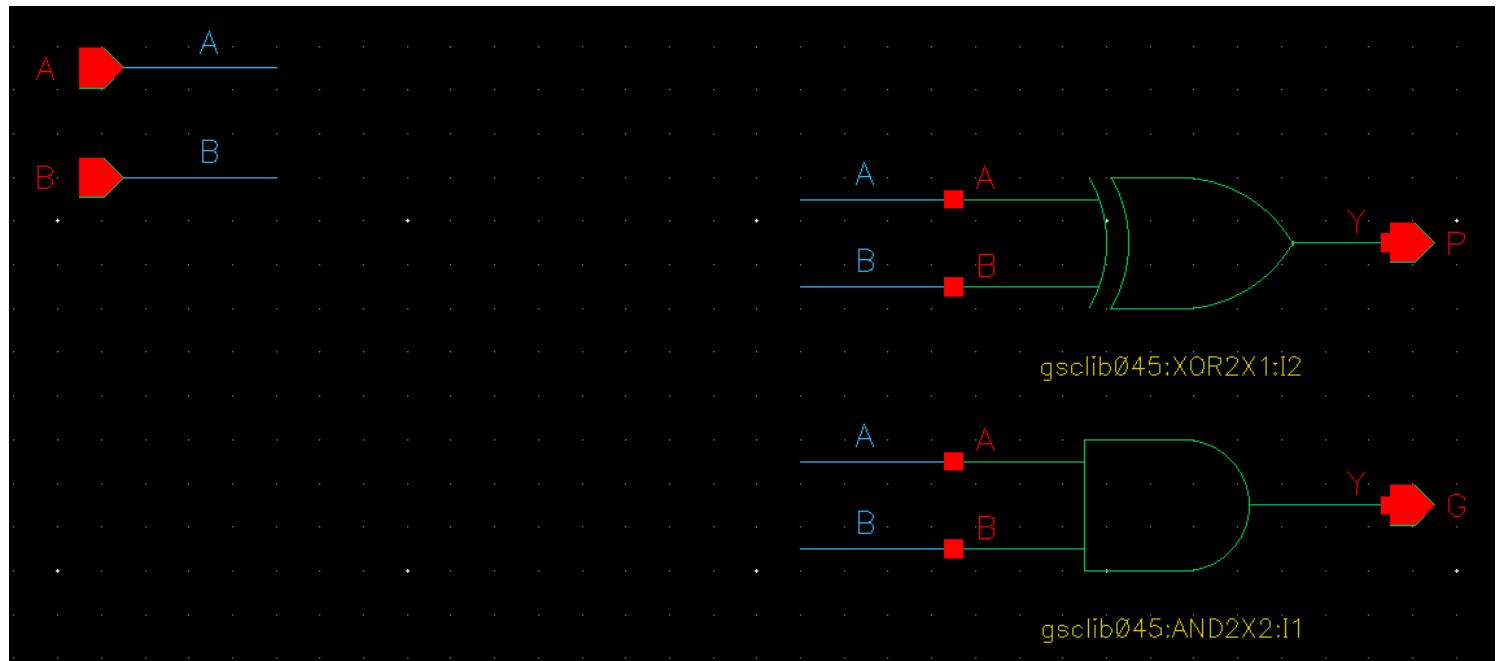
pvs\_RCXxref Done  
Checking in all SoftShare licenses.



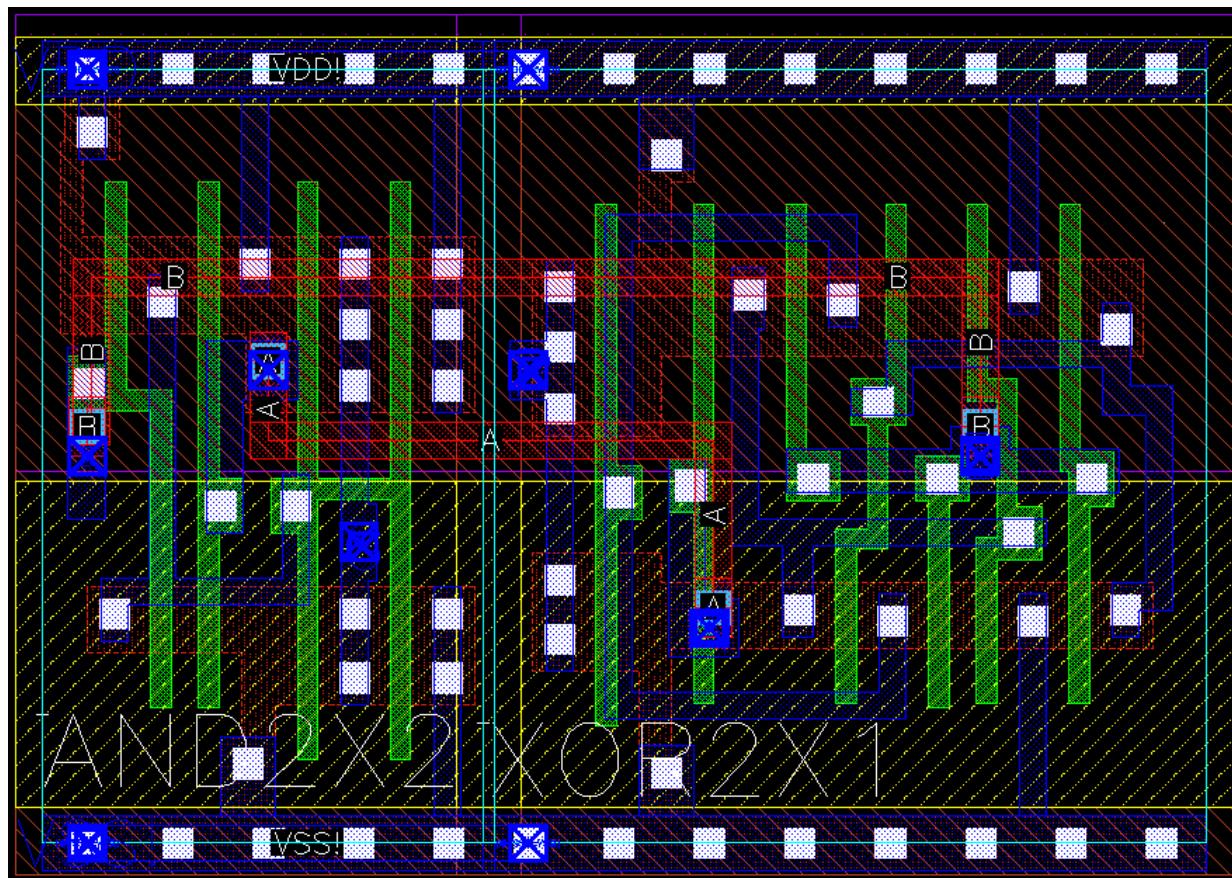
The dialog box shows the following results:  
ERC Results: Empty  
Extraction Results: Clean  
Comparison Results: Match  
A message at the bottom asks: Do you want to start the LVS DE? with Yes and No buttons.

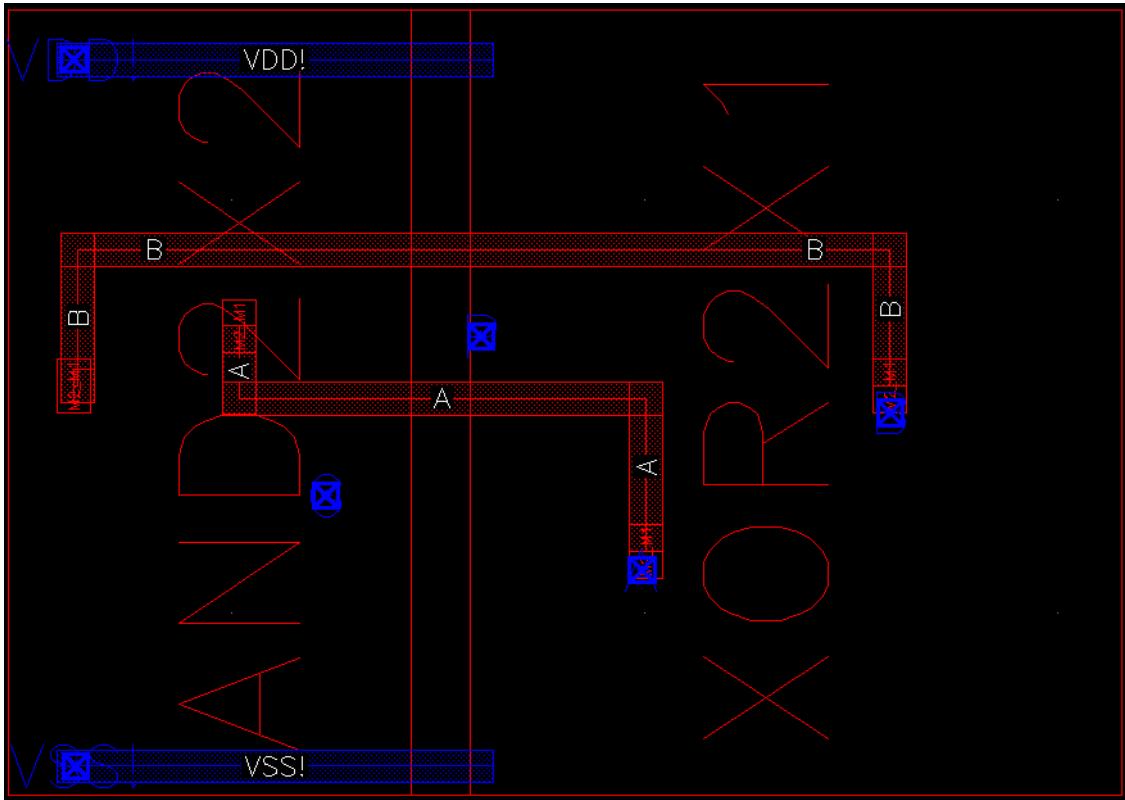
## Bitwise PG Unit

schematic:



Layout:





## DRC:

```

PVS 22.21-64b Reports: Done [DRC] Bitwise_PG_U... (on micron2.eng.tau.ac.il)

[DRC] Bitwise_PG_U... x

Total CPU Time : 2 (s)
Total Real Time : 3 (s)
Peak Memory Used : 19 (M)
Total Original Geometry : 145 (154)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file Bitwise_PG_Unit.sum
ASCII report database is /project/gpdk45/users/orshaul/ws/PVS_RESULTS/DRC/Bitwise_PG_Unit/Bitwise_PG_Unit.ascii
Checking in all SoftShare licenses.

Design Rule Check Finished Normally. Mon Apr 15 14:04:38 2024

```

## LVS:

```

PVS 22.21-64b Reports: Done [LVS] Bitwise_PG_U... (on micron2.eng.tau.ac.il)

[LVS] Bitwise_PG_U... x

# ****#
PVS Comparison Finished. Mon Apr 15 14:00:19 2024

Creating cross reference ...
*****+
pvs_RCXref 22.21-s031 64 bit (Thu Apr 20 20:17:00 PDT 2023)
Build Ref No.: 031 Production (04-20-2023) [pvs_2221]

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Build O/S: Linux x86_64 3.10.0-693.117.x86_64
Executed on: micron2.eng.tau.ac.il (Linux x86_64 3.10.0-1160.92.1.e17.x86_64)
Process Id: 11980
Starting Time: Mon Apr 15 14:00:19 2024 (Mon Apr 15 11:00:19 2024 GMT)
With parameters: format C -nxp -ixf /project/gpdk45/users/orshaul/ws/PVS_RESULTS/LVS/Bitwise_PG_Unit/svdb/Bitwise_PG_Unit Bitwise_PG_Unit.rep
*****+
Total CPU Time : 0 (s)
Total Real Time : 0 (s)
Memory Used : 88.68 (M)

pvs_RCXref Done
Checking in all SoftShare licenses.


```

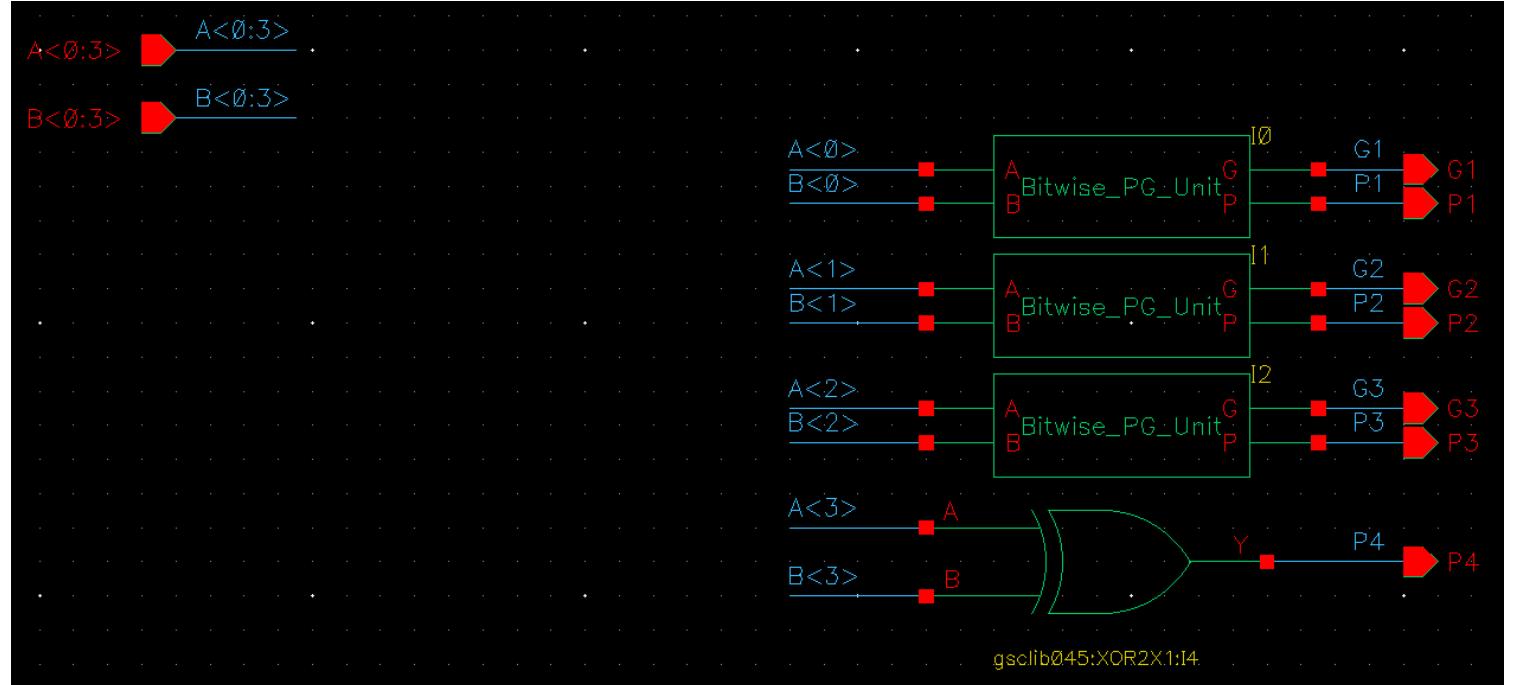
PVS 22.21-64b LVS Run Stat...

	✓
ERC Results	Empty
Extraction Results:	Clean
Comparison Results:	Match

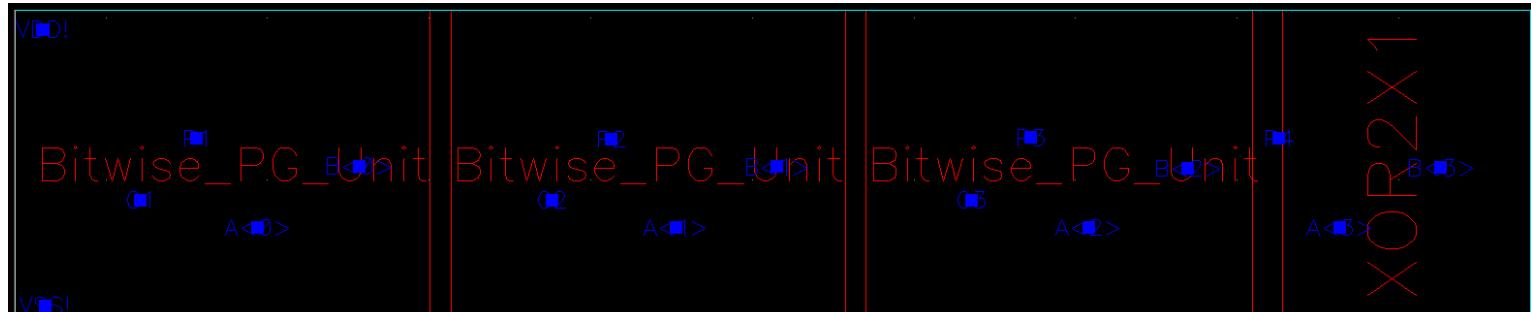
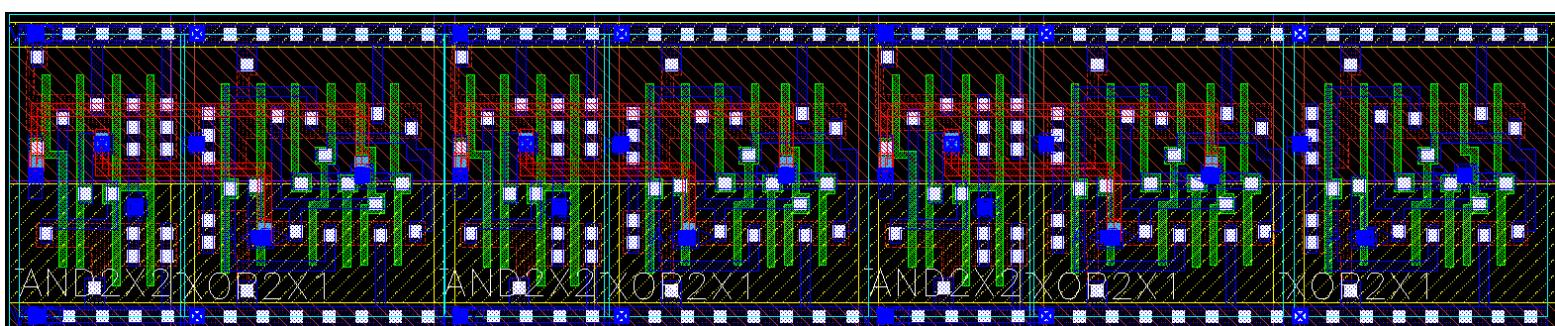
Do you want to start the LVS DE?

# Bitwise PG

## Schematic:



## Layout:



## DRC:

PVS 22.21-64b Reports: Done [DRC] Bitwise\_P... (on micron2.eng.tau.ac.il)  
[DRC] Bitwise\_PG X

---

```
Total CPU Time          : 2(s)
Total Real Time         : 3(s)
Peak Memory Used        : 23(M)
Total Original Geometry : 162(550)
Total DRC RuleChecks    : 562
Total DRC Results       : 0 (0)
Summary can be found in file Bitwise_PG.sum
ASCII report database is /project/gpdk45/users/orshaul/ws/PVS_RESULTS/DRC/Bitwise_PG/Bitwise_PG.ascii
Checking in all SoftShare licenses.

Design Rule Check Finished Normally. Mon Apr 15 15:23:11 2024
```

## LVS:

PVS Comparison Finished. Mon Apr 15 15:25:12 2024

Creating cross reference ...

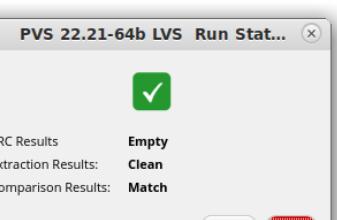
\*\*\*\*\*  
pvs\_RCXref 22.21-s031 64 bit (Thu Apr 20 20:17:00 PDT 2023)  
Build Ref No.: 031 Production (04-20-2023) [pvs\_2221]

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Build O/S: Linux x86\_64 3.10.0-693.el7.x86\_64  
Executed on: micron2.eng.tau.ac.il (Linux x86\_64 3.10.0-1160.92.1.el7.x86\_64)  
Process Id: 3655  
Starting Time: Mon Apr 15 15:25:12 2024 (Mon Apr 15 12:25:12 2024 GMT)  
With parameters: -format C -nxvf -ixf /project/gpdk45/users/orshaul/ws/PVS\_RESULTS/LVS/Bitwise\_PG/svdb/Bitwise\_PG Bitwise\_PG.rep  
\*\*\*\*\*

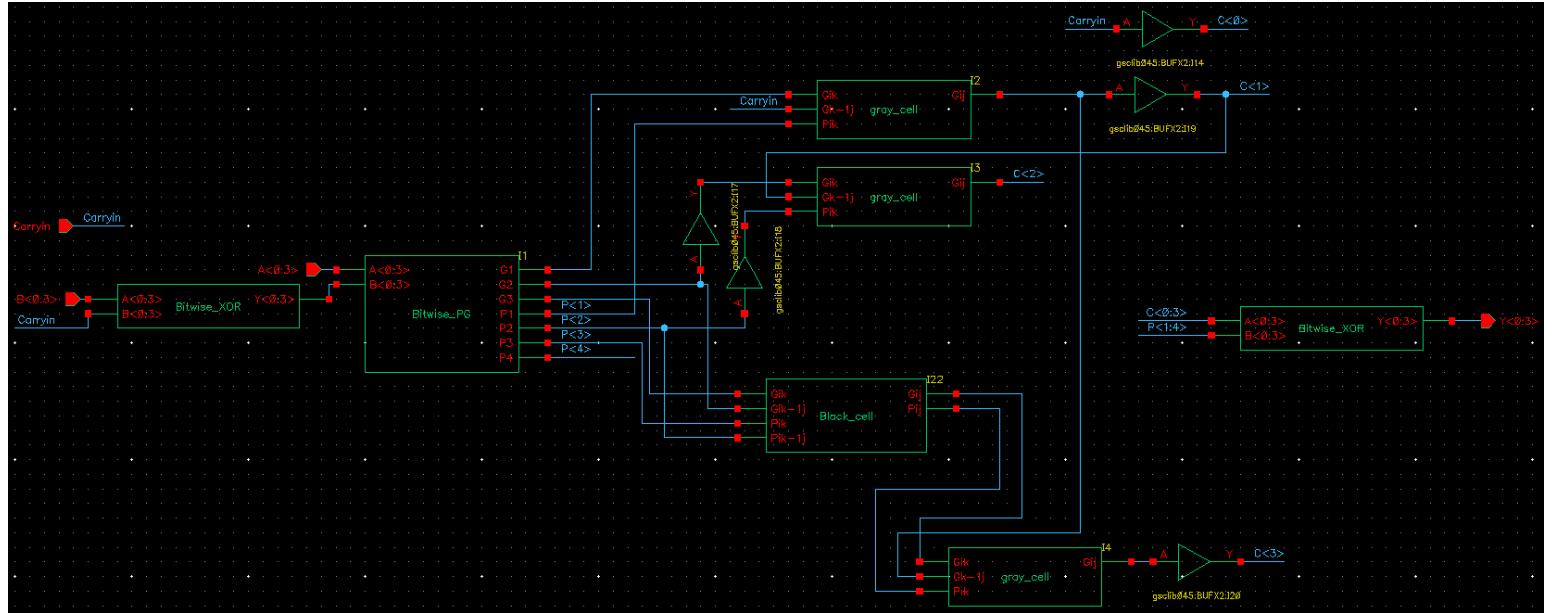
Total CPU Time : 0 (s)  
Total Real Time : 0 (s)  
Memory Used : 88.43 (M)

pvs\_RCXref Done  
Checking in all SoftShare licenses.

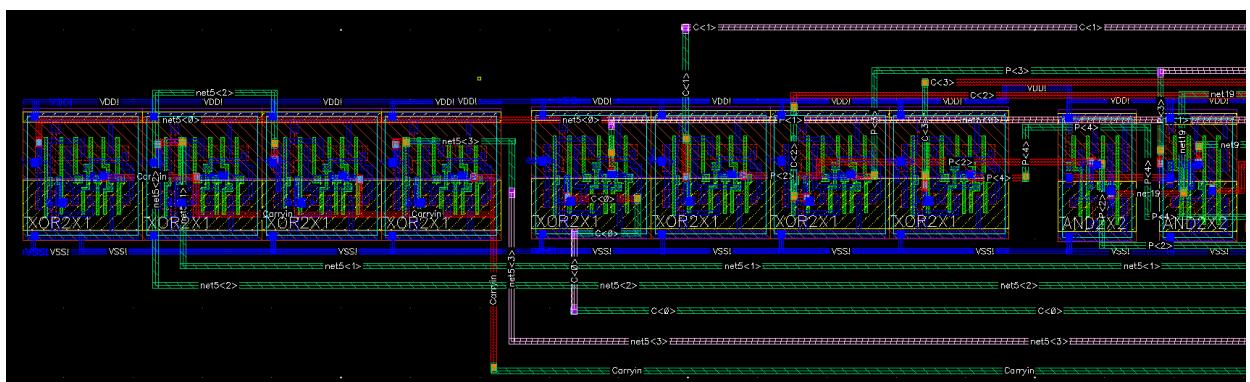
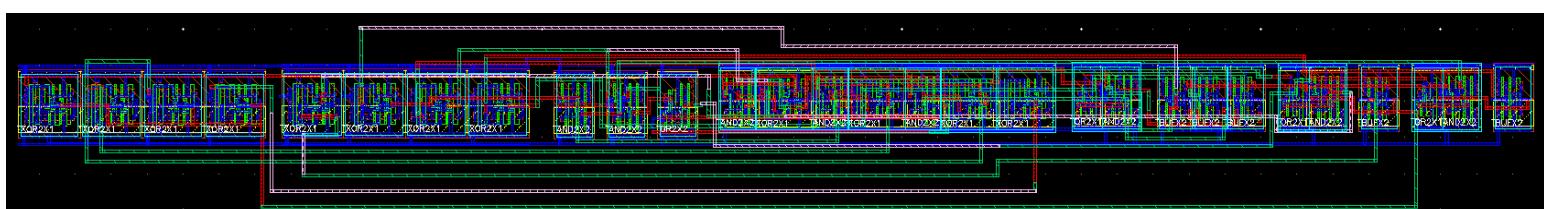
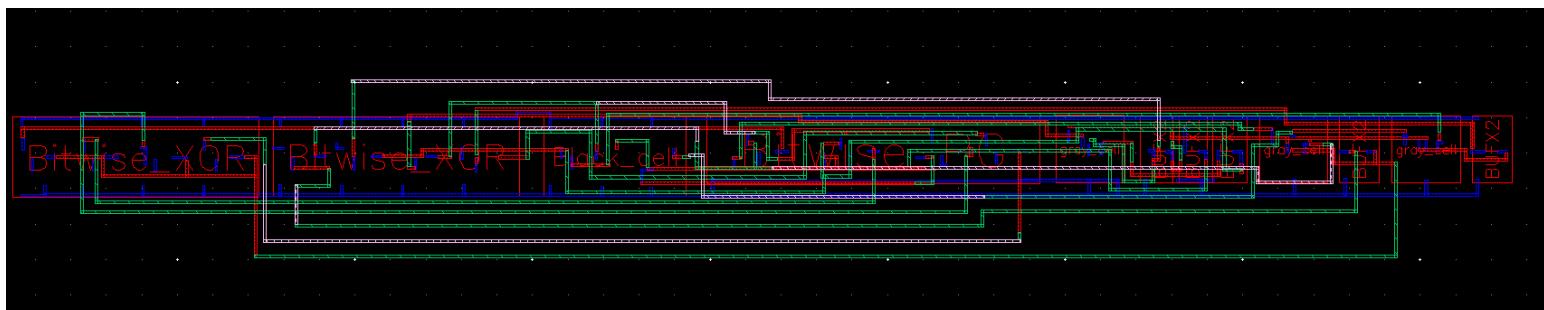


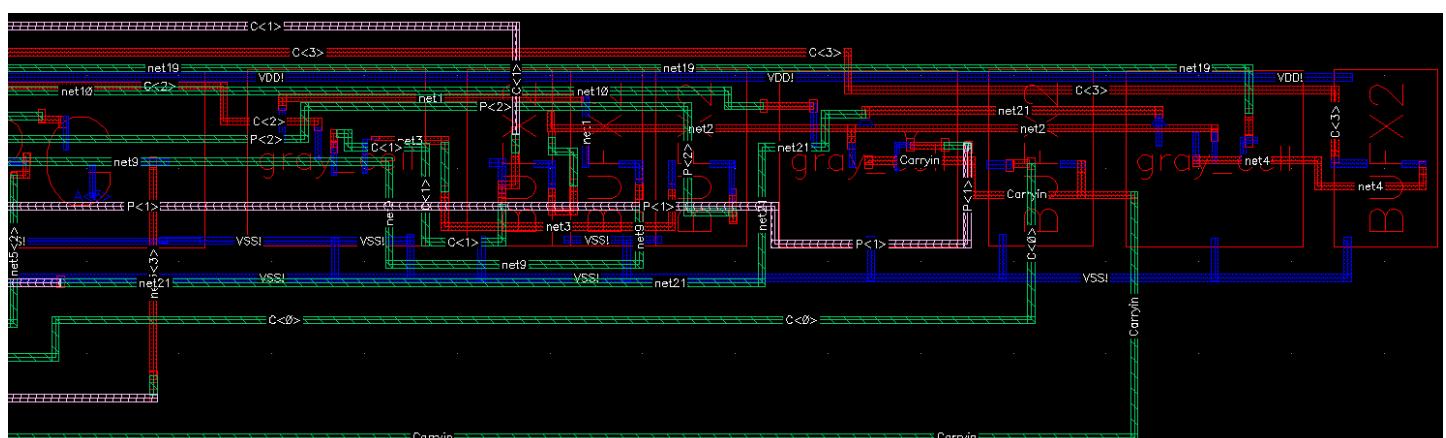
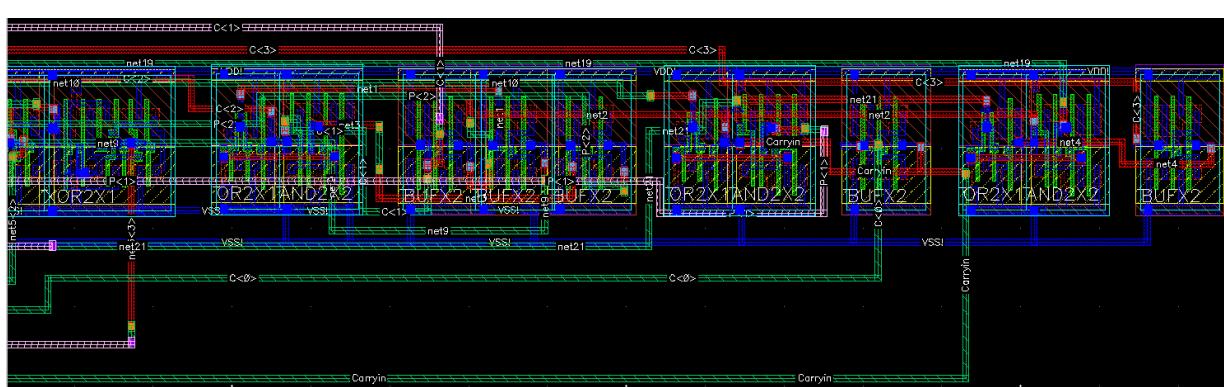
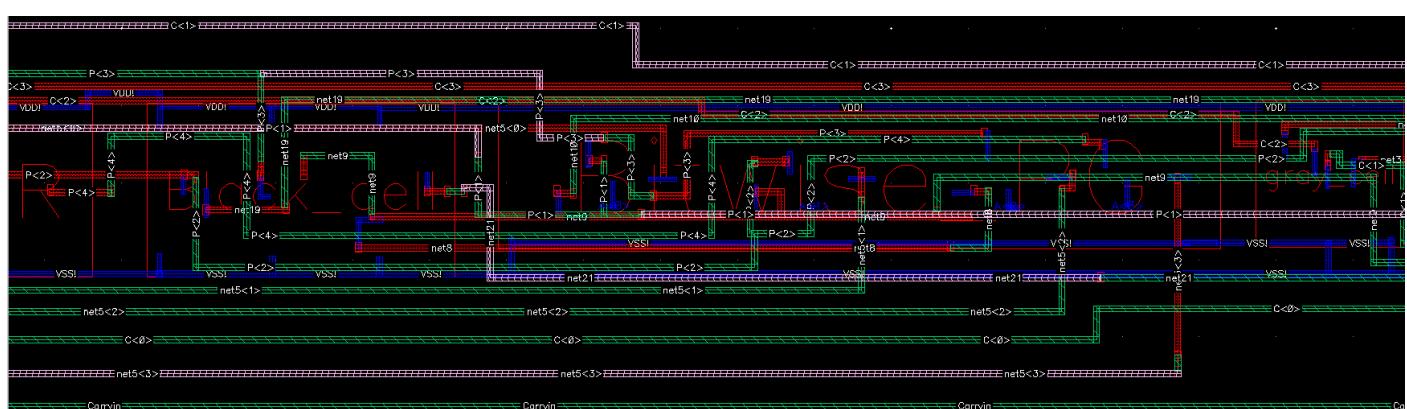
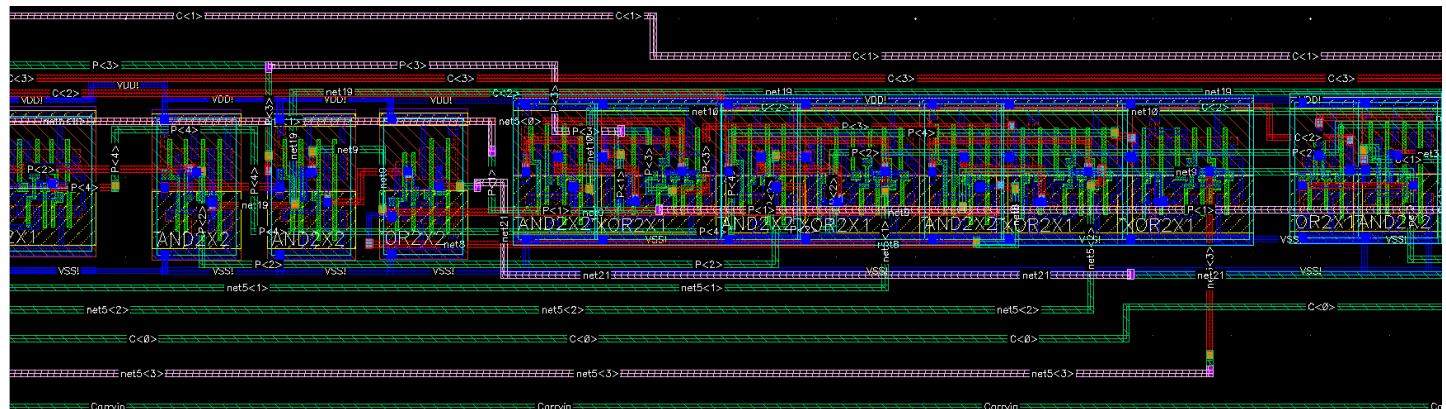
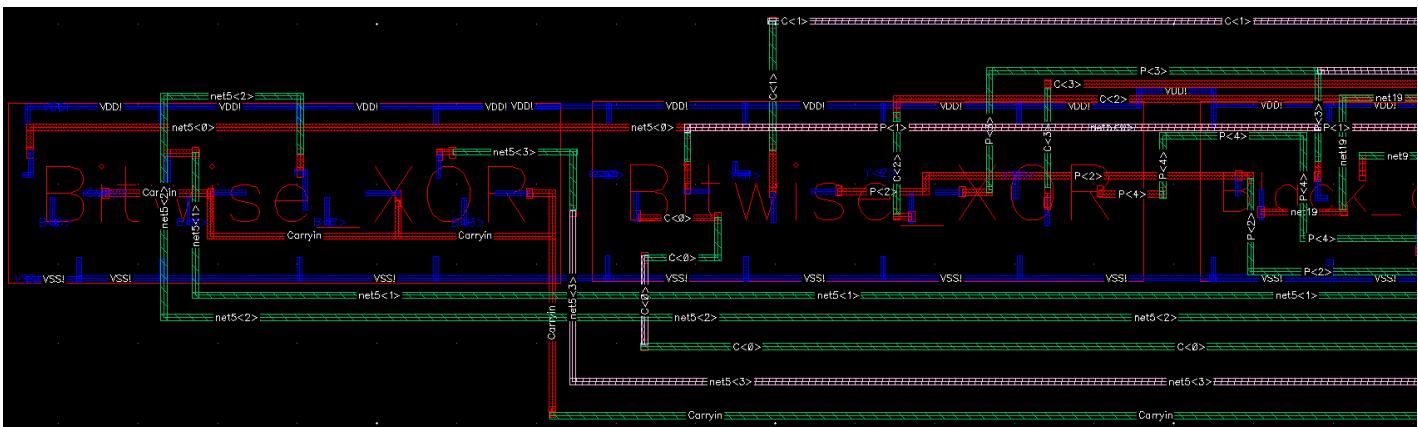
# Adder

schematic:



Layout:





## DRC:

PVS 22.21-64b Reports: Done [DRC] Adder... (on micron2.eng.tau.ac.il)

[DRC] Adder X

---

```
Total CPU Time          : 2 (s)
Total Real Time         : 3 (s)
Peak Memory Used        : 23 (M)
Total Original Geometry : 785 (2777)
Total DRC RuleChecks    : 562
Total DRC Results       : 0 (0)
Summary can be found in file Adder.sum
ASCII report database is /project/gpdk45/users/orshaul/ws/PVS_RESULTS/DRC/Adder/Adder.ascii
Checking in all SoftShare licenses.

Design Rule Check Finished Normally. Mon Apr 15 14:33:41 2024
```

LVS:

PVS Comparison Finished. Mon Apr 15 14:36:47 2024

Creating cross reference ...

\*\*\*\*\*

pvs\_RCXxref 22.21-s031 64 bit (Thu Apr 20 20:17:00 PDT 2023)  
Build Ref No.: 031 Production (04-20-2023) [pvs\_2221]

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Build O/S: Linux x86\_64 3.10.0-693.el7.x86\_64  
Executed on: micron2.eng.tau.ac.il (Linux x86\_64 3.10.0-1160.92.1.el7.x86\_64)  
Process Id: 25979  
Starting Time: Mon Apr 15 14:36:47 2024 (Mon Apr 15 11:36:47 2024 GMT)  
With parameters: -format C -nxfs -ixf /project/gpdk45/users/orshaul/ws/PVS\_RESULTS/LVS/Adder/svdb/Adder.Adder.rep  
\*\*\*\*\*

Total CPU Time : 0(s)  
Total Real Time : 0(s)  
Memory Used : 90.70 (M)

pvs\_RCXxref Done  
Checking in all SoftShare licenses.

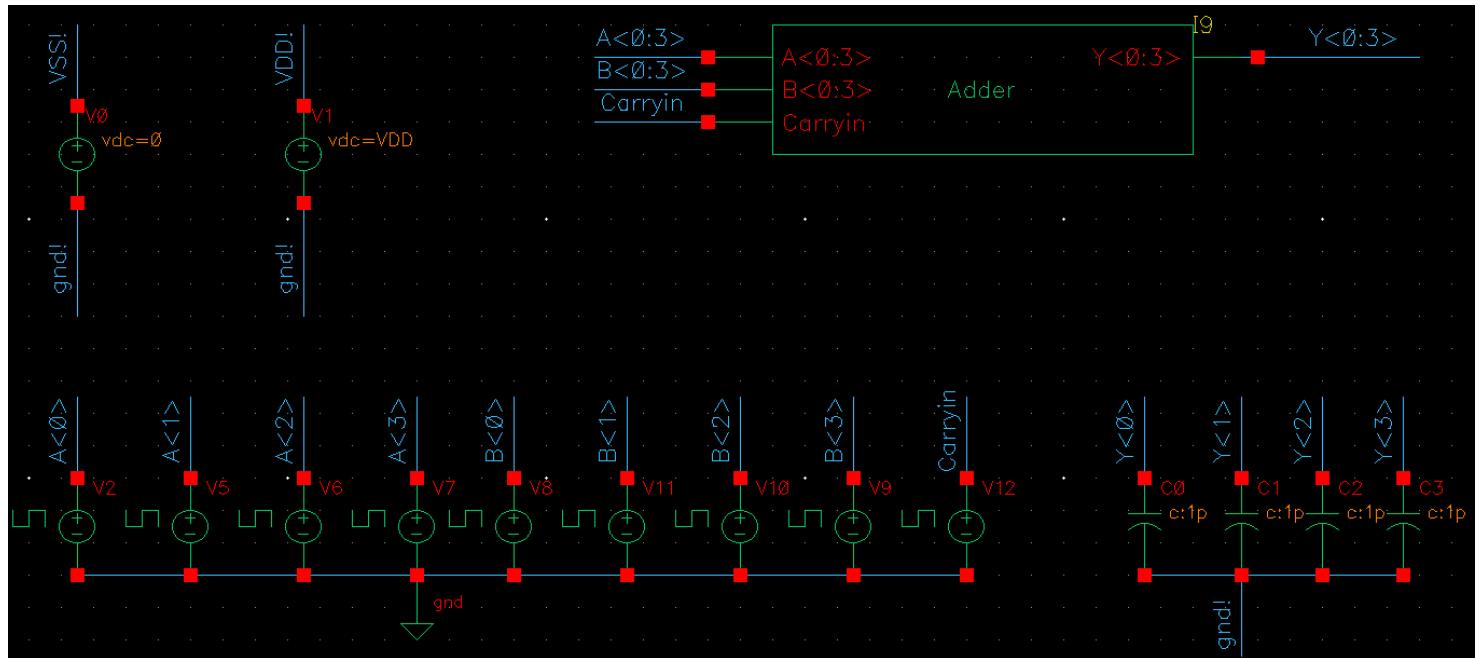
**PVS 22.21-64b LVS Run Stat...**

ERC Results: **Empty**  
Extraction Results: **Clean**  
Comparison Results: **Match**

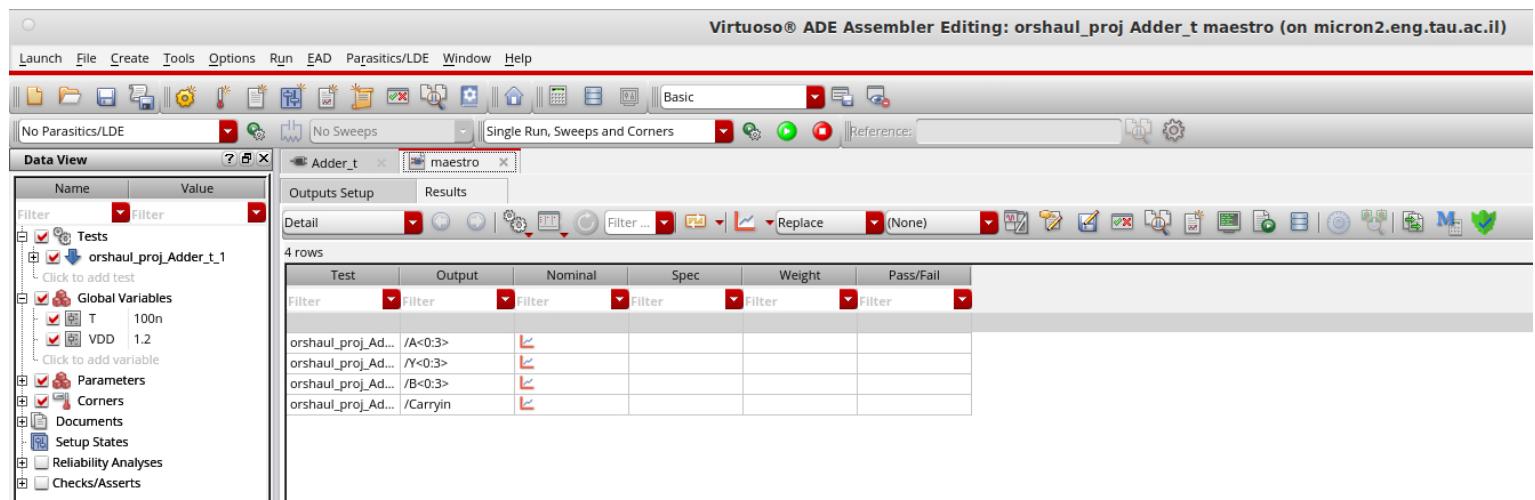
Do you want to start the LVS DE?

## Adder testbench

### Schematic:



### Maestro:



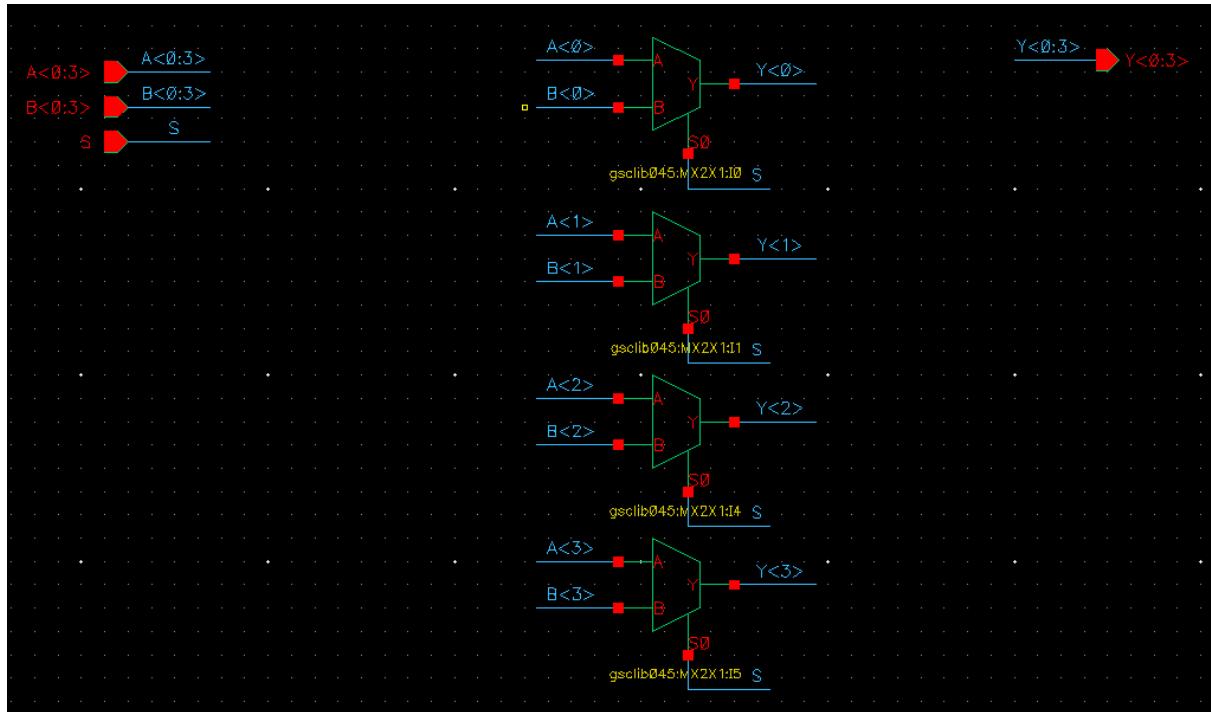
## Graphs:

סימולציה של ה-ADDER – כאשר  $\text{Carryin} = 1$  למשהו אנחנו ביחסור. ולכן בגרפים היקן שנראה  $\text{Yout} = 1$ . נבדוק שהתבצע חישור תקין ולא חיבור. בסימולציה של ה-ALU הוסף בהמשך, נבדוק את תקינות פעולות החישור רק כאשר נראה בגרף של opcode את האופקוד שקבענו לפעולות החישור.

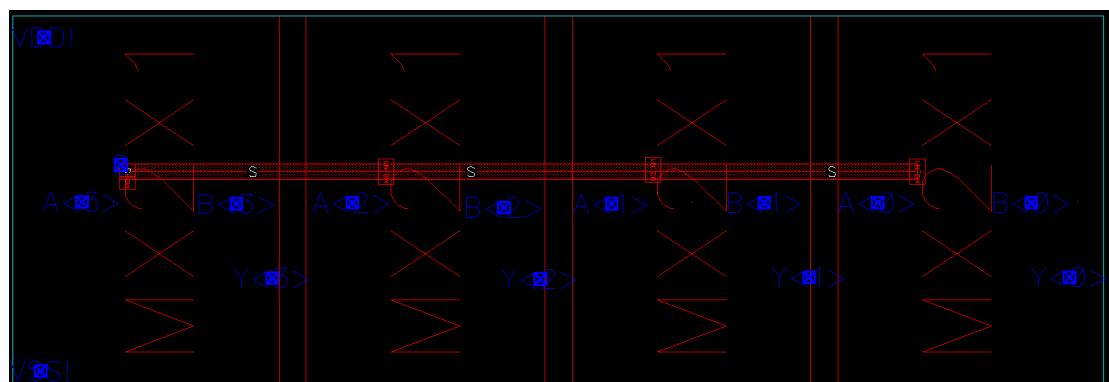
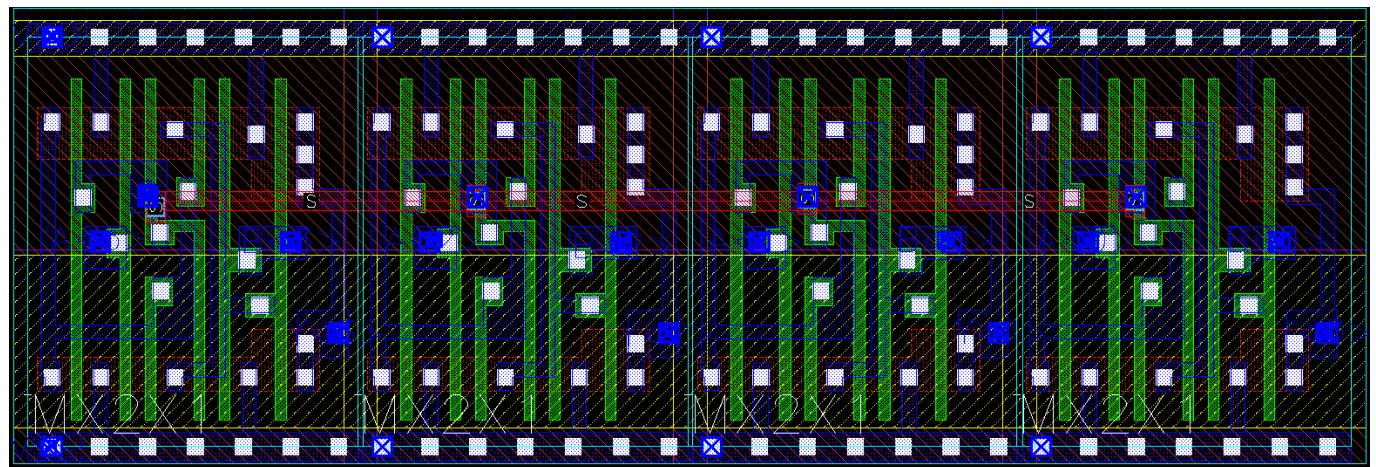


# MUX 2X1

## Schematic



## Layout



DRC

PVS 22.21-64b Reports: Done [DRC] MUX2X... (on micron2.eng.tau.ac.il)  
[DRC] MUX2X1 x

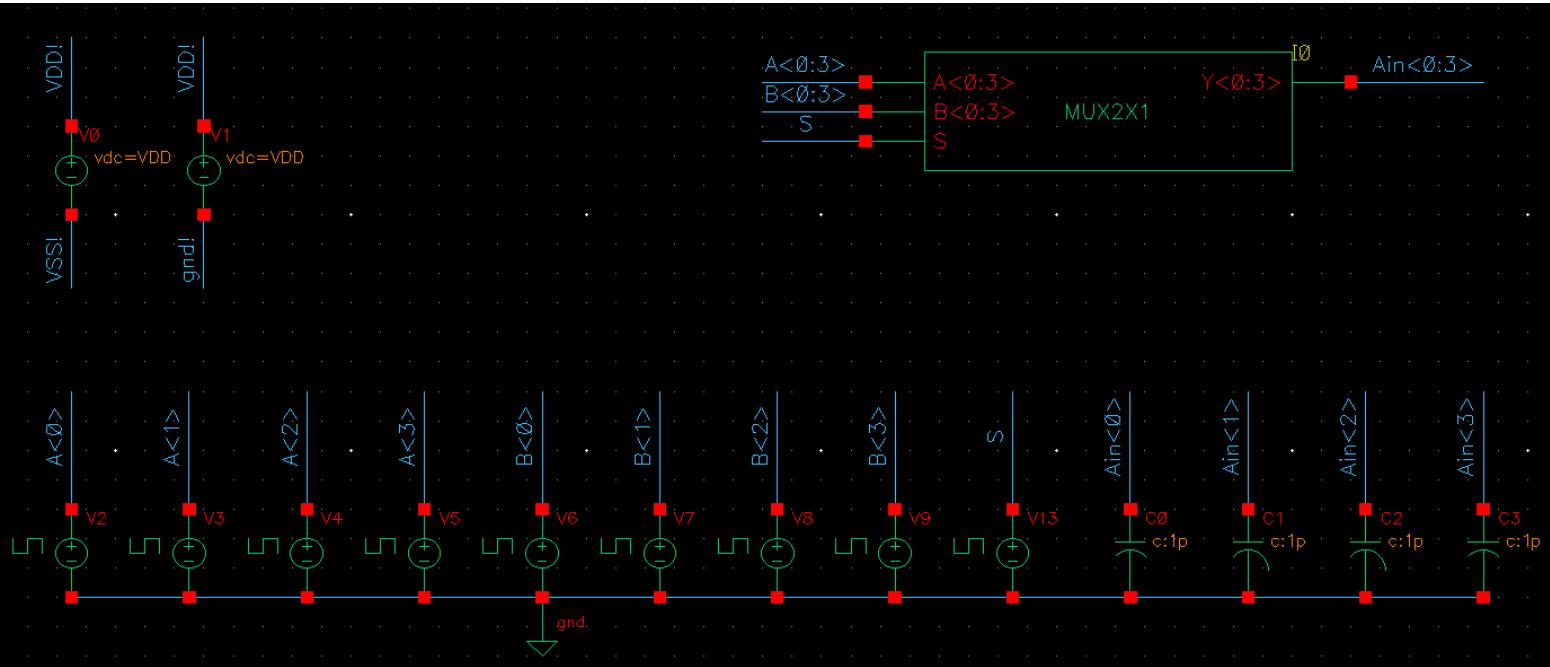
DFM FILL: Cumulative Time CPU =		0 (s)	REAL =	0 (s)
Total CPU Time	:	2 (s)		
Total Real Time	:	2 (s)		
Peak Memory Used	:	19 (M)		
Total Original Geometry	:	89 (302)		
Total DRC RuleChecks	:	562		
Total DRC Results	:	0 (0)		
Summary can be found in file MUX2X1.sum				
ASCII report database is /project/gpdk45/users/orshaul/ws/PVS_RESULTS/DRC/MUX2X1/MUX2X1.ascii				
Checking in all SoftShare licenses.				

Design Rule Check Finished Normally. Mon Apr 22 19:19:41 2024

LVS

## Mux 2X1 Test Bench

### Schematic

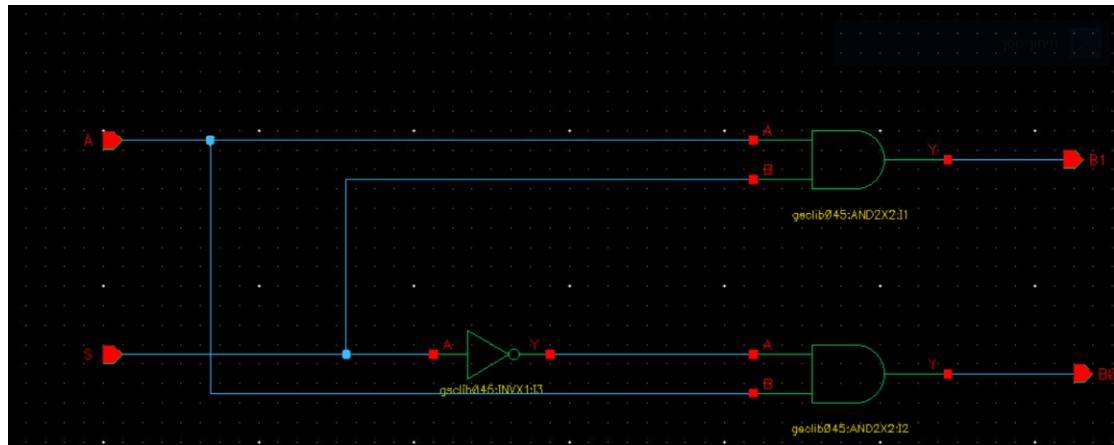


### Graphs

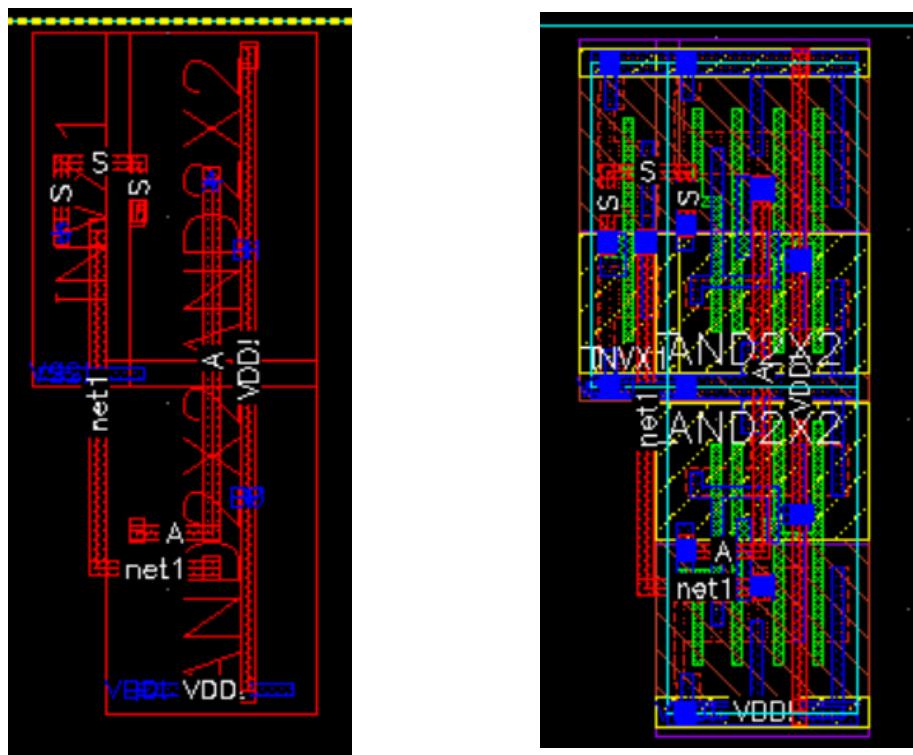


## Demux 2X1

### schematic



### Layout



## LVS

```
PVS 22.21-64b Reports: Done [LVS] Dmux... (on micron7.eng.tau.ac.il)
[DRC] Dmux_0804... [LVS] Dmux

Build O/S:      Linux x86_64 3.10.0-693.el7.x86_64
Executed on:   micron7.eng.tau.ac.il (Linux x86_64 3.10.0-1160.92.1.el7.x86_64)
Process Id:    41429
Starting Time: Mon Apr  8 14:18:27 2024 (Mon Apr  8 11:18:27 2024 GMT)
With parameters: -format C -nxf /project/gpdk45/users/idanlevy3/ws/PVS_RESULTS
*****
Total CPU Time    : 0(s)
Total Real Time   : 0(s)
Memory Used       : 84.86(M)

pvs_RCXxref Done
Checking in all SoftShare licenses.

PVS 22.21-64b LVS Run Status (x)

ERC Results      Empty
Extraction Results: Clean
Comparison Results: Match

Do you want to start the LVS DE?   Highlight
```

## DRC

```
PVS 22.21-64b Reports: Done [DRC] Dmux_0804... (on micron7.eng.tau.ac.il)
[DRC] Dmux_0804...

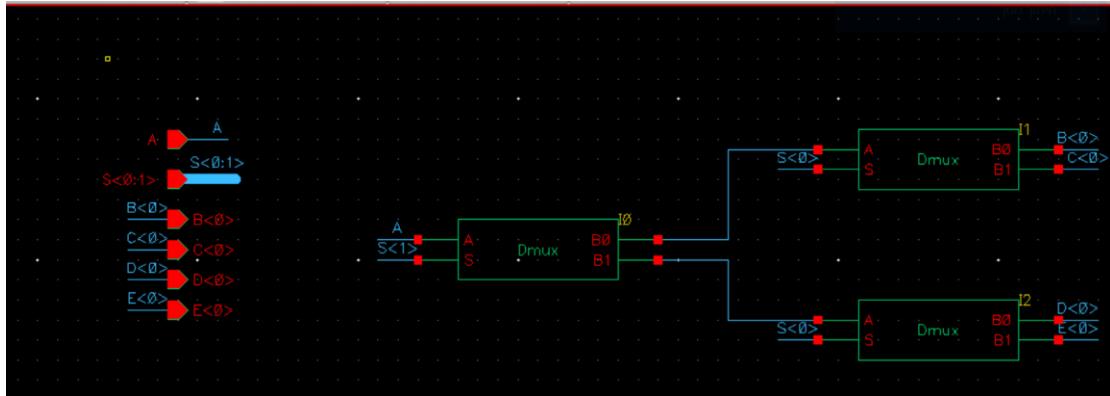
Total CPU Time          : 1(s)
Total Real Time         : 2(s)
Peak Memory Used       : 19(M)
Total Original Geometry: 111(188)
Total DRC RuleChecks   : 562
Total DRC Results      : 0 (0)
Summary can be found in file Dmux.sum
ASCII report database is /project/gpdk45/users/idanlevy3/ws/PVS_RESULTS/DRC/Dmux.a
Checking in all SoftShare licenses.

Design Rule Check Finished Normally. Mon Apr  8 14:08:59 2024

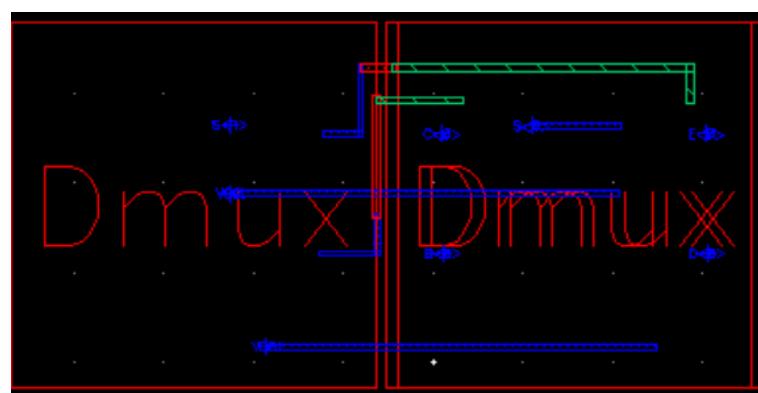
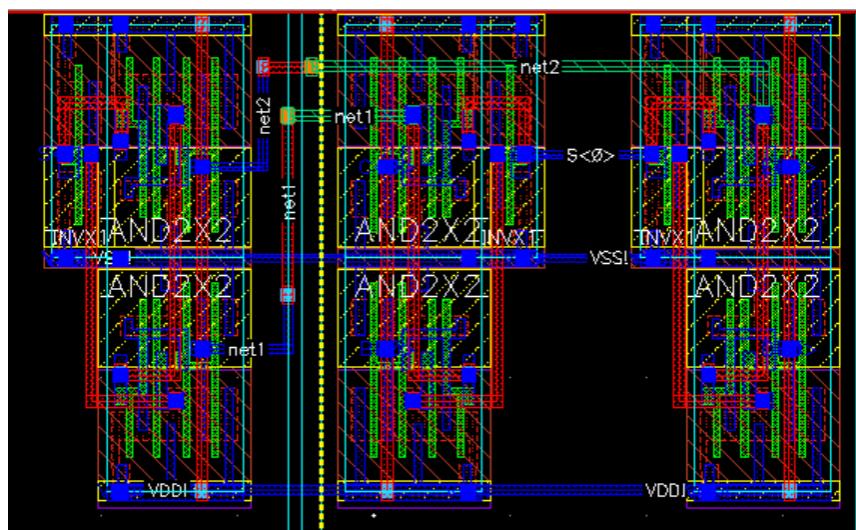
Find  Prey  Next  Match case  Whole word  Use RegExp  Highlight
```

## Demux 1X4

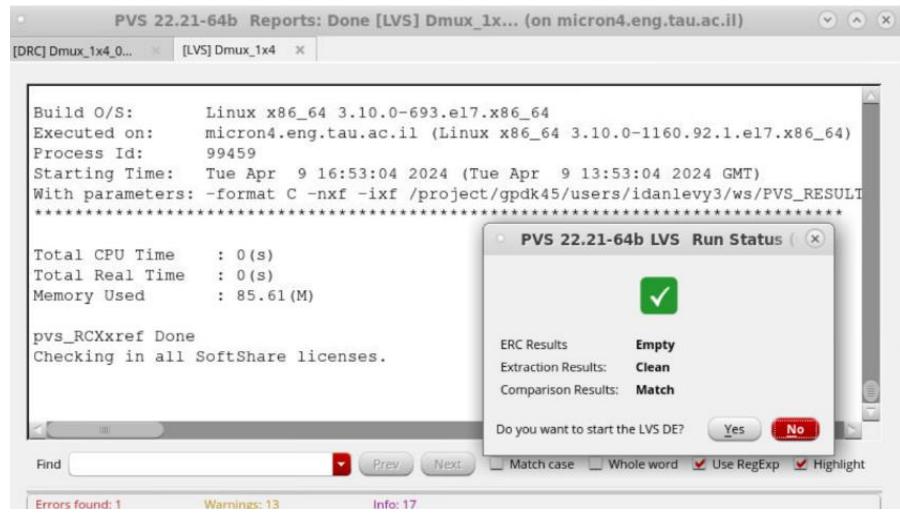
### Schematic



### Layout



## LVS



PVS 22.21-64b Reports: Done [LVS] Dmux\_1x4\_0... (on micron4.eng.tau.ac.il)

[DRC] Dmux\_1x4\_0... [LVS] Dmux\_1x4

```
Build O/S: Linux x86_64 3.10.0-693.el7.x86_64
Executed on: micron4.eng.tau.ac.il (Linux x86_64 3.10.0-1160.92.1.el7.x86_64)
Process Id: 99459
Starting Time: Tue Apr 9 16:53:04 2024 (Tue Apr 9 13:53:04 2024 GMT)
With parameters: -format C -nxf -ixf /project/gpdk45/users/idanlevy3/ws/PVS_RESULT
*****
Total CPU Time : 0(s)
Total Real Time : 0(s)
Memory Used : 85.61(M)

pvs_RCXxref Done
Checking in all SoftShare licenses.
```

**PVS 22.21-64b LVS Run Status**

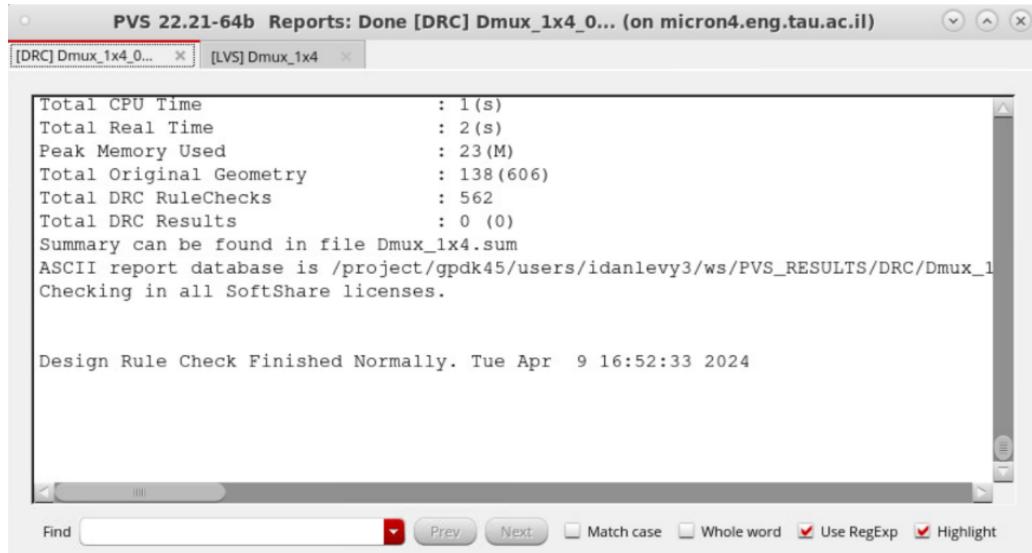
ERC Results	Empty
Extraction Results:	Clean
Comparison Results:	Match

Do you want to start the LVS DE?  Yes  No

Match case  Whole word  Use RegExp  Highlight

Find Errors found: 1 Warnings: 13 Info: 17

## DRC



PVS 22.21-64b Reports: Done [DRC] Dmux\_1x4\_0... (on micron4.eng.tau.ac.il)

[DRC] Dmux\_1x4\_0... [LVS] Dmux\_1x4

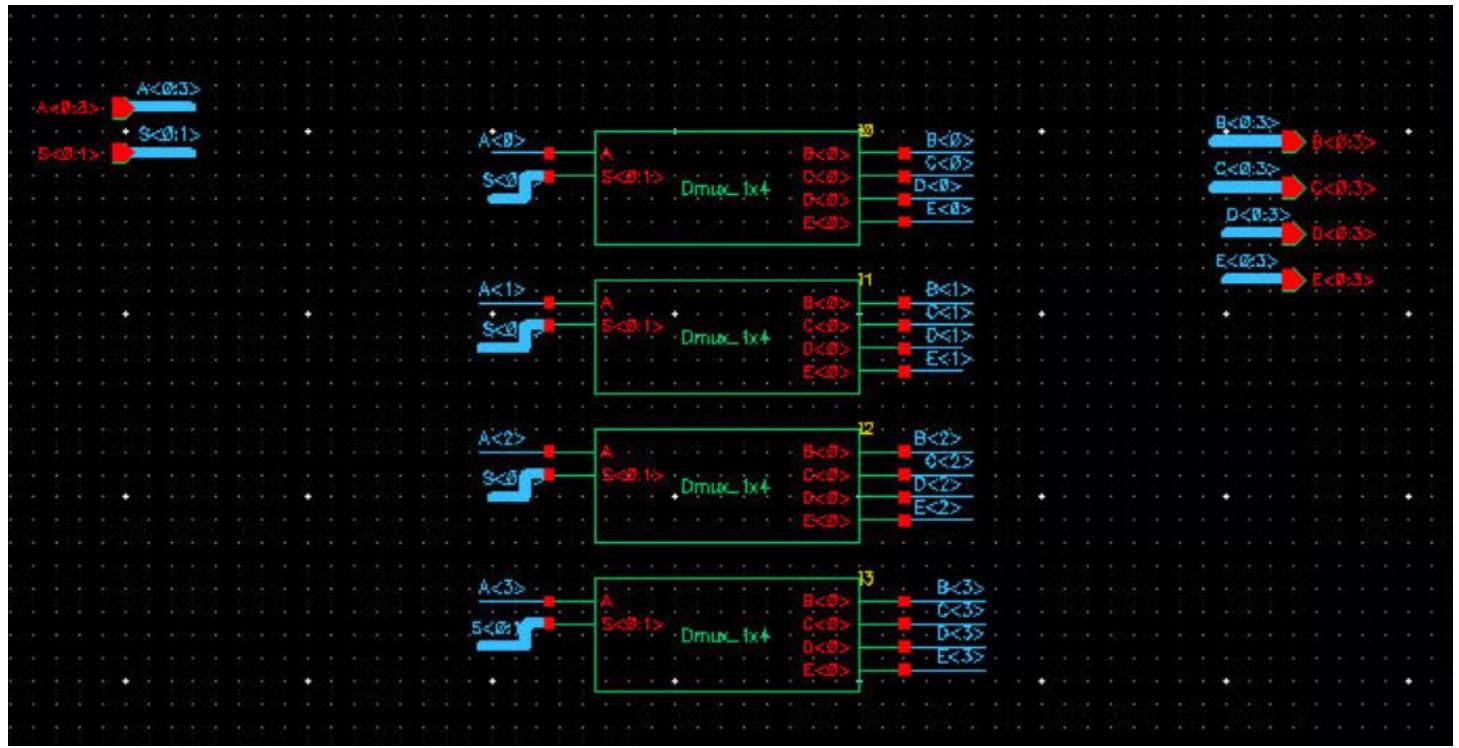
```
Total CPU Time : 1(s)
Total Real Time : 2(s)
Peak Memory Used : 23(M)
Total Original Geometry : 138(606)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file Dmux_1x4.sum
ASCII report database is /project/gpdk45/users/idanlevy3/ws/PVS_RESULTS/DRC/Dmux_1
Checking in all SoftShare licenses.

Design Rule Check Finished Normally. Tue Apr 9 16:52:33 2024
```

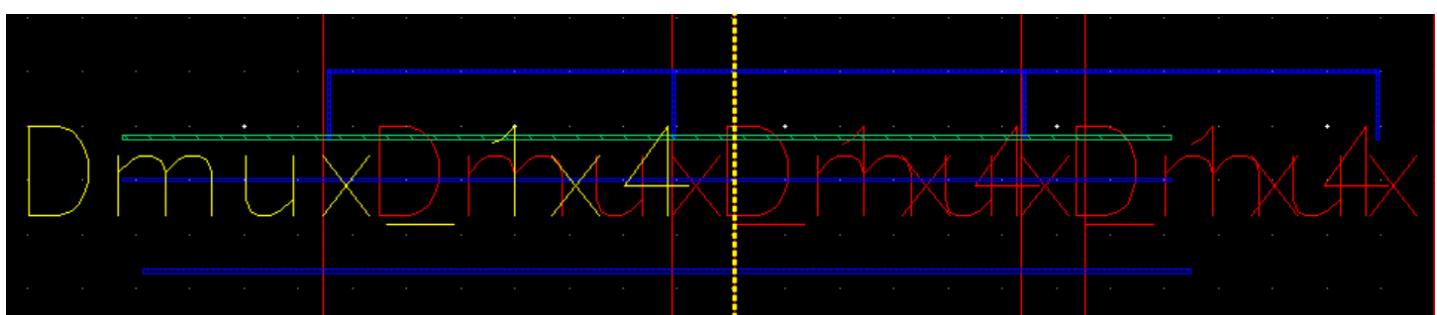
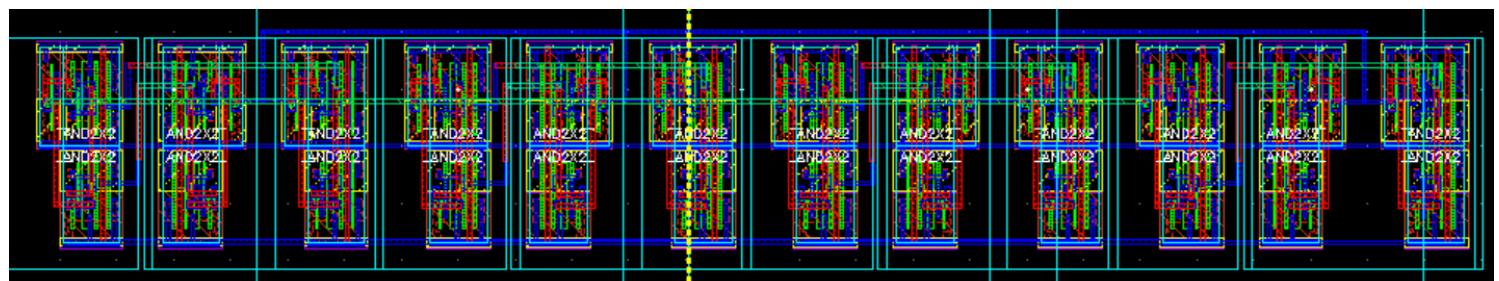
Match case  Whole word  Use RegExp  Highlight

## Demux 4X16

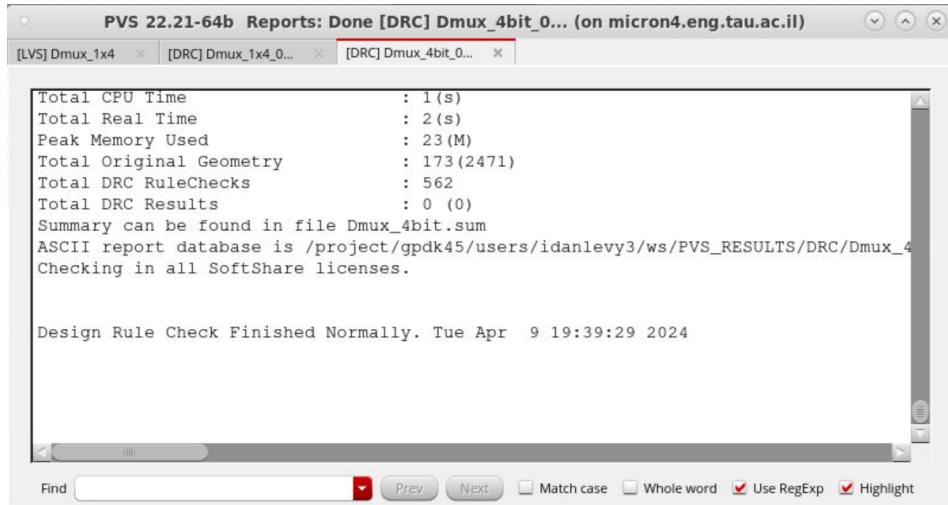
### Schematic



### Layout



## DRC



PVS 22.21-64b Reports: Done [DRC] Dmux\_4bit\_0... (on micron4.eng.tau.ac.il)

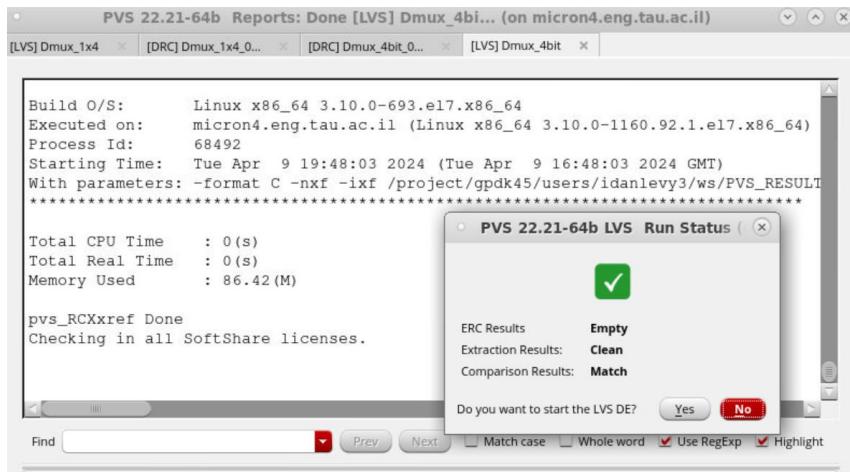
[LVS] Dmux\_1x4 [DRC] Dmux\_1x4\_0... [DRC] Dmux\_4bit\_0... [ ]

```
Total CPU Time : 1 (s)
Total Real Time : 2 (s)
Peak Memory Used : 23 (M)
Total Original Geometry : 173 (2471)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file Dmux_4bit.sum
ASCII report database is /project/gpdk45/users/idanlevy3/ws/PVS_RESULTS/DRC/Dmux_4bit
Checking in all SoftShare licenses.

Design Rule Check Finished Normally. Tue Apr 9 19:39:29 2024
```

Find   Prey  Next  Match case  Whole word  Use RegExp  Highlight

## LVS



PVS 22.21-64b Reports: Done [LVS] Dmux\_4bit\_0... (on micron4.eng.tau.ac.il)

[LVS] Dmux\_1x4 [DRC] Dmux\_1x4\_0... [DRC] Dmux\_4bit\_0... [LVS] Dmux\_4bit [ ]

```
Build O/S: Linux x86_64 3.10.0-693.el7.x86_64
Executed on: micron4.eng.tau.ac.il (Linux x86_64 3.10.0-1160.92.1.el7.x86_64)
Process Id: 68492
Starting Time: Tue Apr 9 19:48:03 2024 (Tue Apr 9 16:48:03 2024 GMT)
With parameters: -format C -nxf -ixf /project/gpdk45/users/idanlevy3/ws/PVS_RESULTS/DRC/Dmux_4bit
*****
Total CPU Time : 0 (s)
Total Real Time : 0 (s)
Memory Used : 86.42 (M)

pvs_RCXxref Done
Checking in all SoftShare licenses.
```

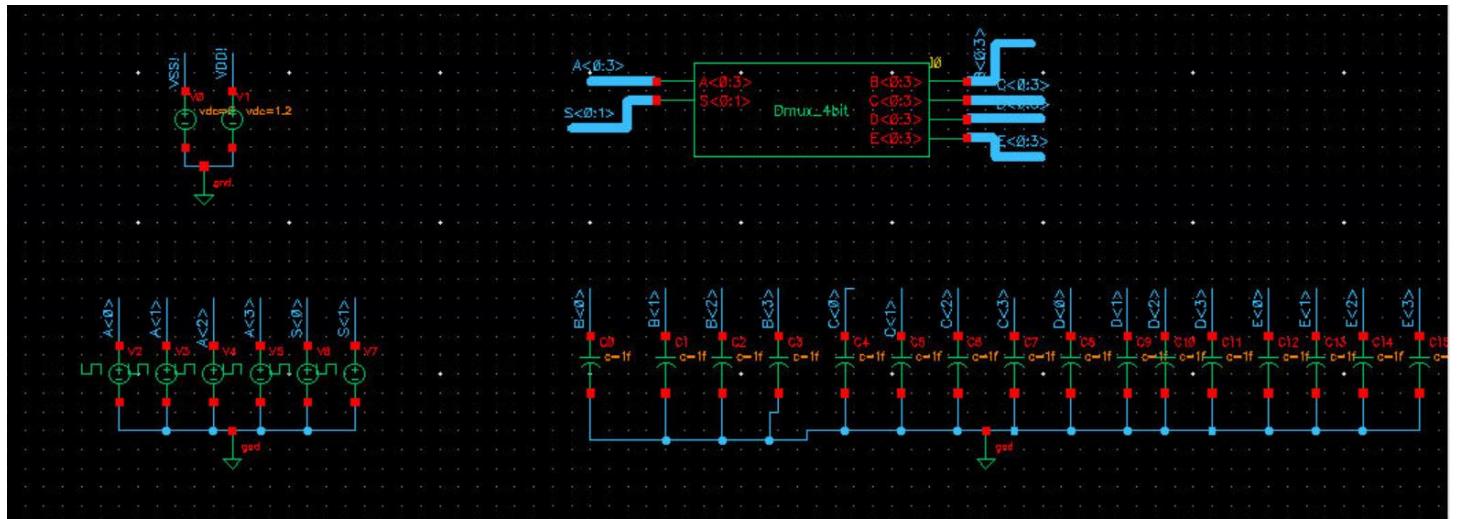
**PVS 22.21-64b LVS Run Status ( )**

ERC Results: **Empty**  
Extraction Results: **Clean**  
Comparison Results: **Match**

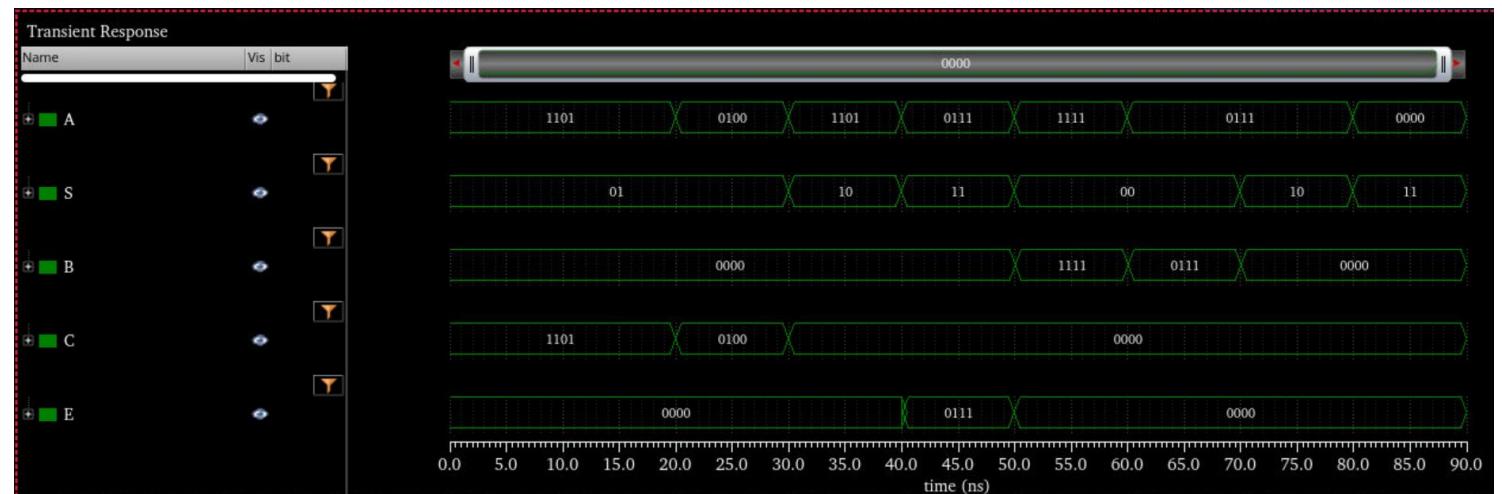
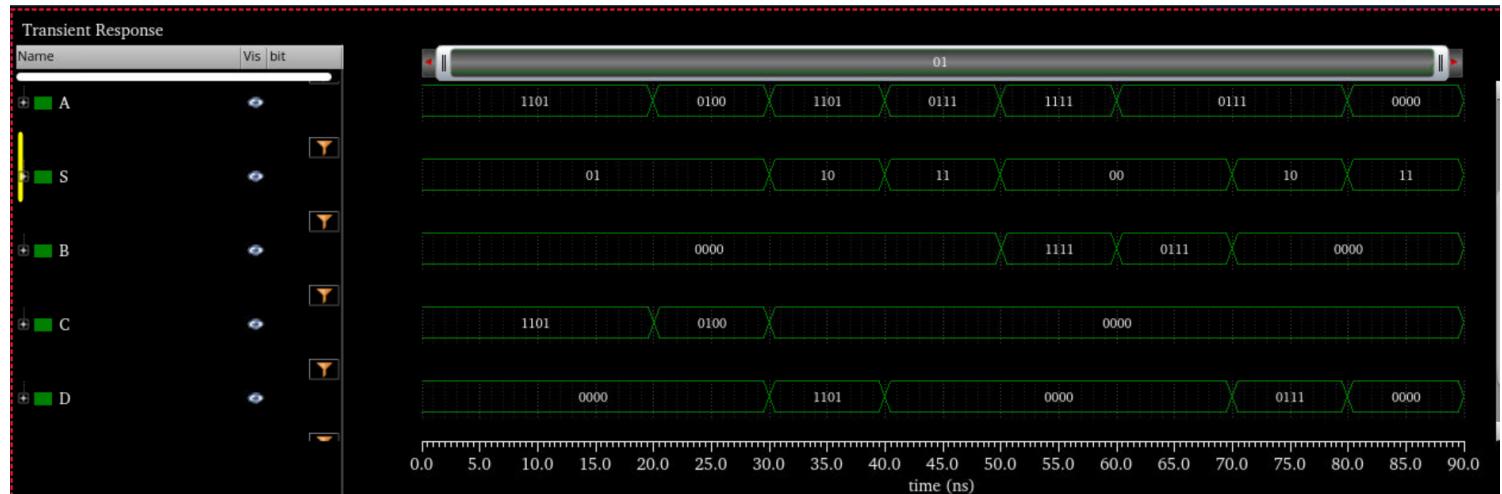
Do you want to start the LVS DE?  Yes  No

Find   Prey  Next  Match case  Whole word  Use RegExp  Highlight

# Demux 4X16 Test bench

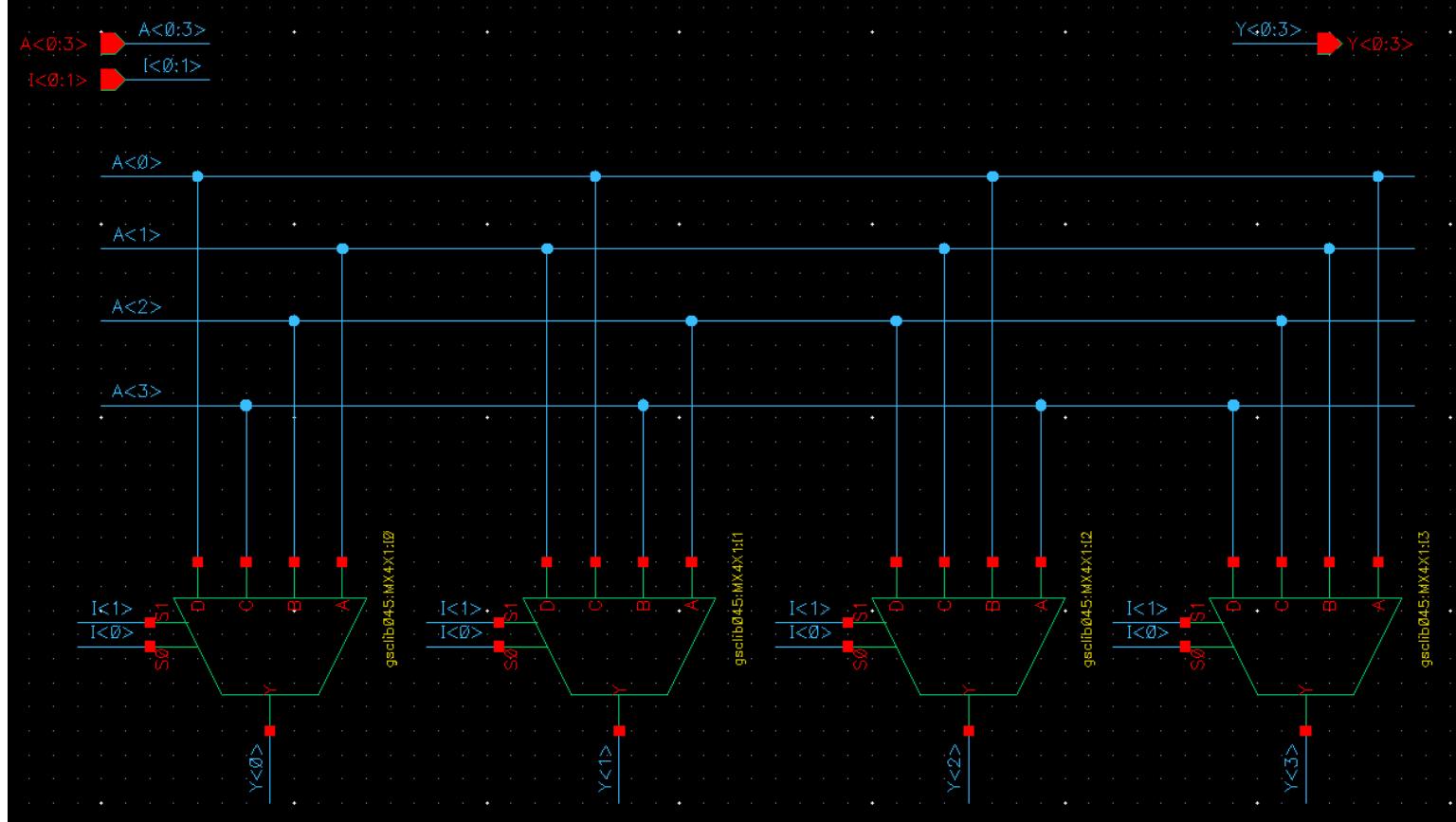


## Graphs

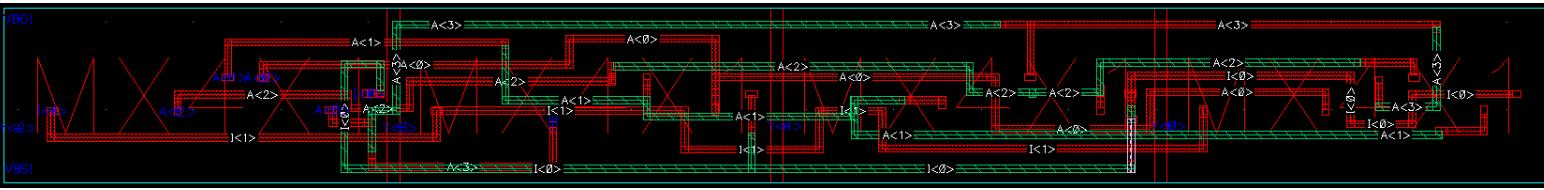
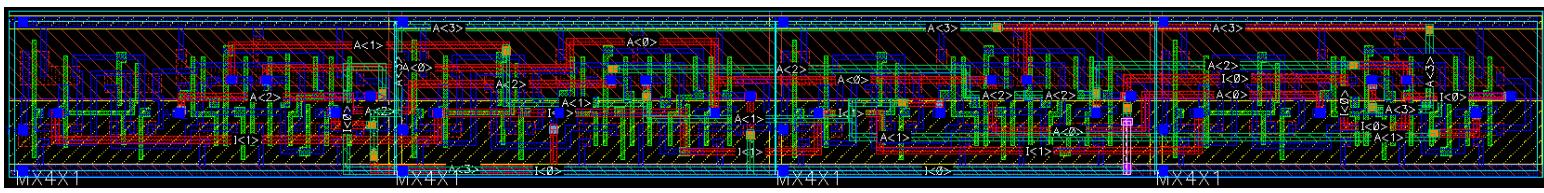


# BSR(shifter)

## Schematic



## Layout



LVS

PVS Comparison Finished. Thu Apr 25 01:30:24 2024

Creating cross reference ...

\*\*\*\*\*  
pvs\_RCXref 22.21-s031 64 bit (Thu Apr 20 20:17:00 PDT 2023)  
Build Ref No.: 031 Production (04-20-2023) [pvs\_2221]  
  
Copyright 2023 Cadence Design Systems, Inc.  
All rights reserved worldwide.  
  
Build O/S: Linux x86\_64 3.10.0-693.el7.x86\_64  
Executed on: micron2.eng.tau.ac.il (Linux x86\_64 3.10.0-1160.92.1.el7.x86\_64)  
Process Id: 14668  
Starting Time: Thu Apr 25 01:30:24 2024 (Wed Apr 24 22:30:24 2024 GMT)  
With parameters: -format C -nxp -ixf /project/gpdk45/users/orshaul/ws/PVS\_RESULTS/LVS/BSR/svdb/BSR.BSR.rep  
\*\*\*\*\*  
  
Total CPU Time : 0(s)  
Total Real Time : 0(s)  
Memory Used : 84.29(M)  
  
pvs\_RCXref Done  
Checking in all SoftShare licenses.

**PVS 22.21-64b LVS Run Stat...**

ERC Results: **Empty**  
Extraction Results: **Clean**  
Comparison Results: **Match**

Do you want to start the LVS DE? **Yes** **No**

DRC

PVS 22.21-64b Reports: Done [DRC] BS... (on micron2.eng.tau.ac.il)  
[DRC] BSR X

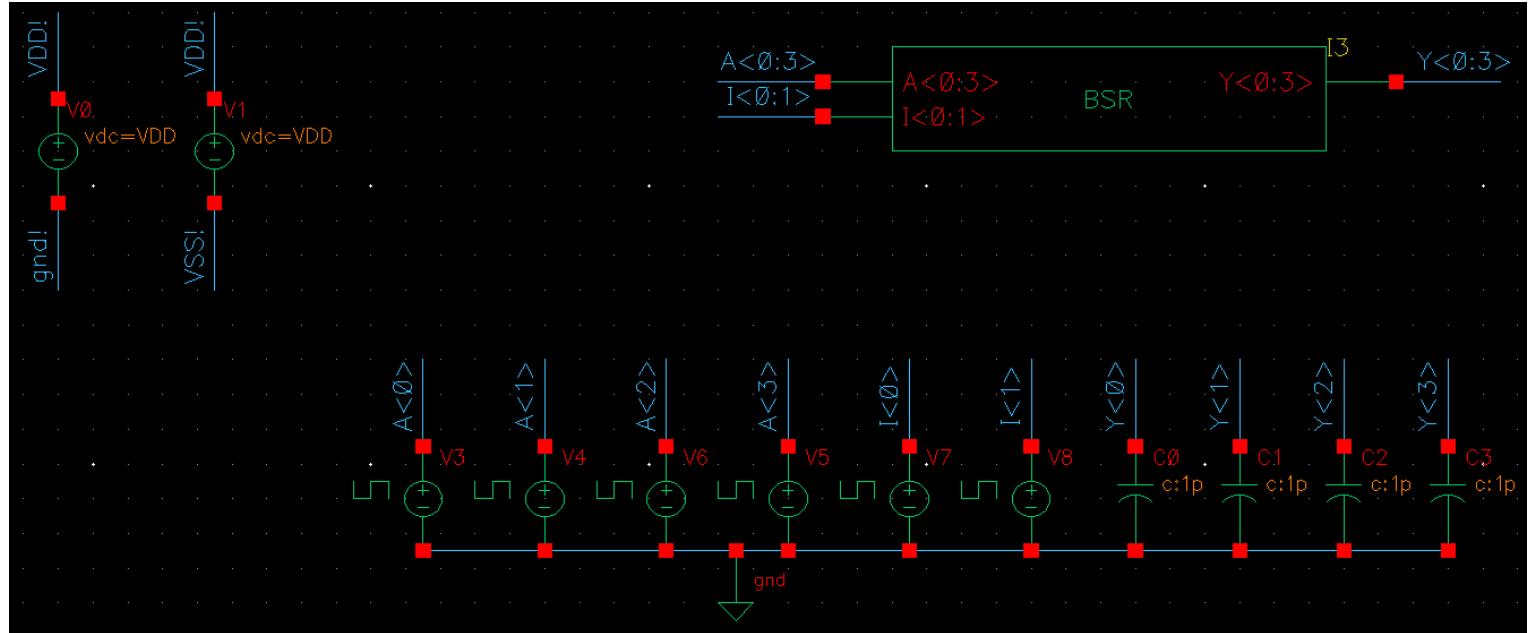
---

```
Total CPU Time           : 2(s)
Total Real Time          : 3(s)
Peak Memory Used         : 19(M)
Total Original Geometry  : 264(813)
Total DRC RuleChecks     : 562
Total DRC Results        : 0 (0)
Summary can be found in file BSR.sum
ASCII report database is /project/gpdk45/users/orshaul/ws/PVS_RESULTS/DRC/BSR/BSR.ascii
Checking in all SoftShare licenses.

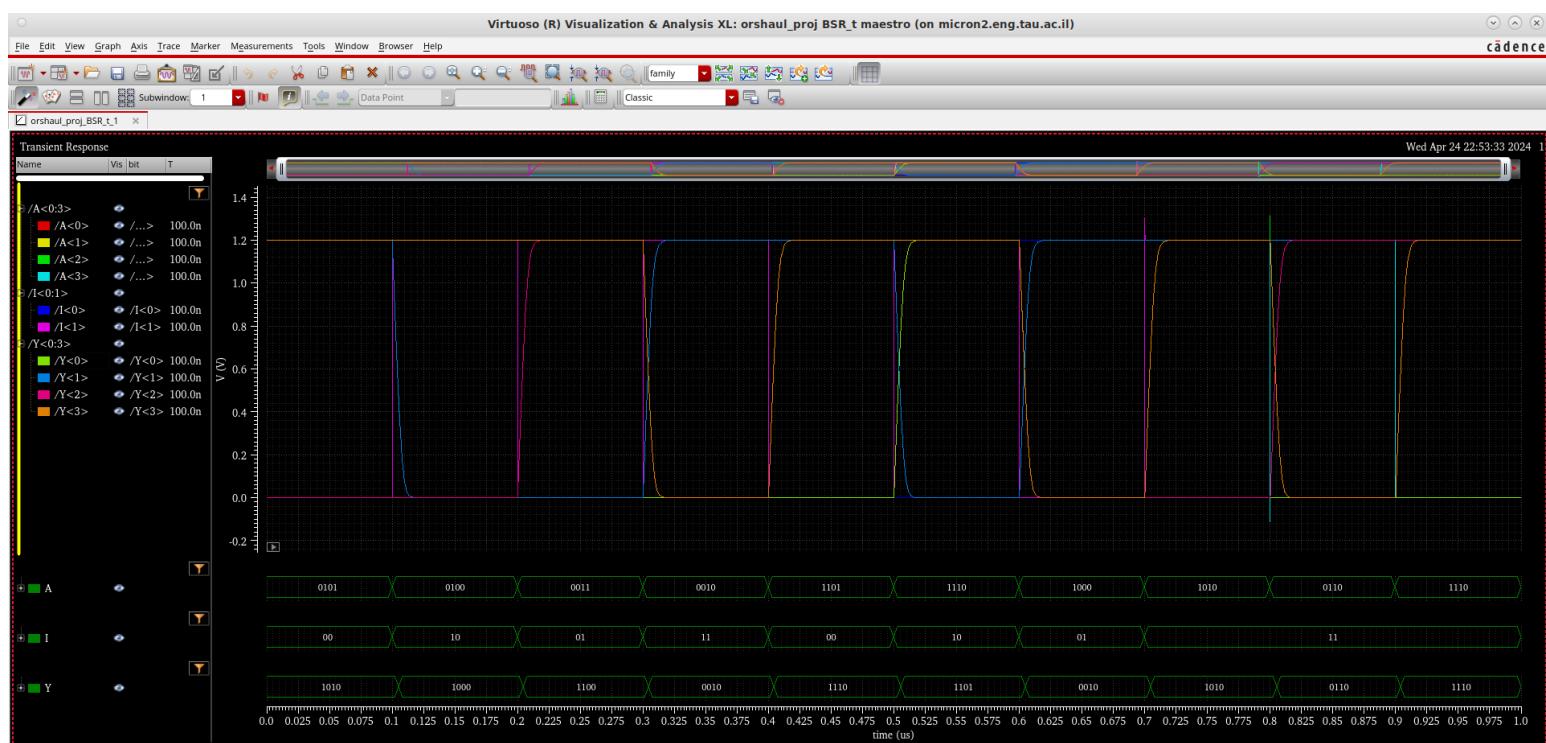
Design Rule Check Finished Normally. Thu Apr 25 01:27:22 2024
```

## BSR(shifter) Testbench

### Schematic



### Graphs



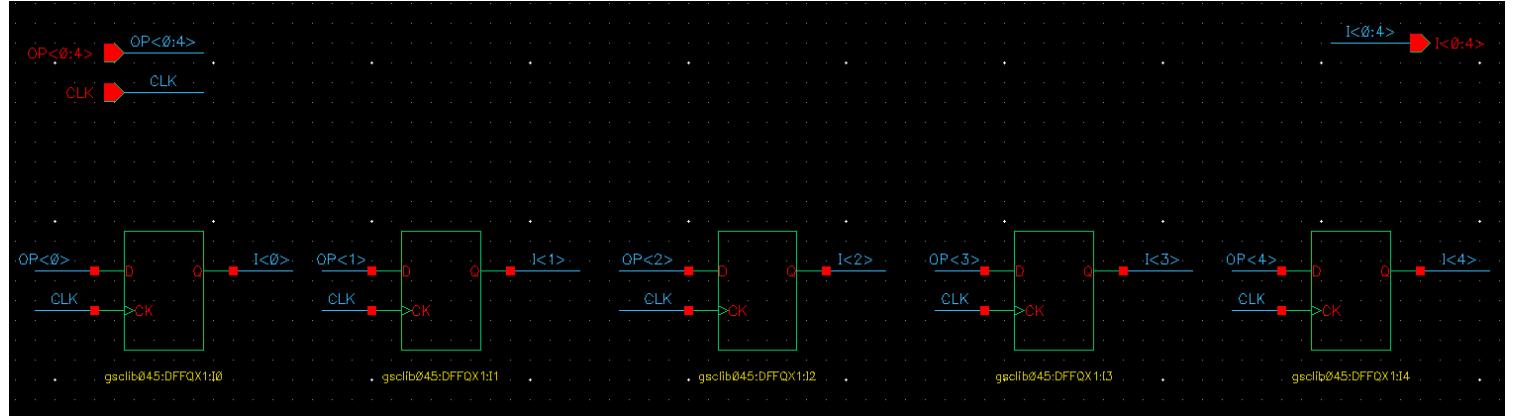
ניתן לראות מהגרפים שקיבלנוbove ציקלית ימינה של המחרוזת A לפי המחרוזת I בהתאם לחוקיות שקבענו בשלב התכנון :

- $\text{Opcode}[2:1]$  - represents the number of shifts the BSR should do:

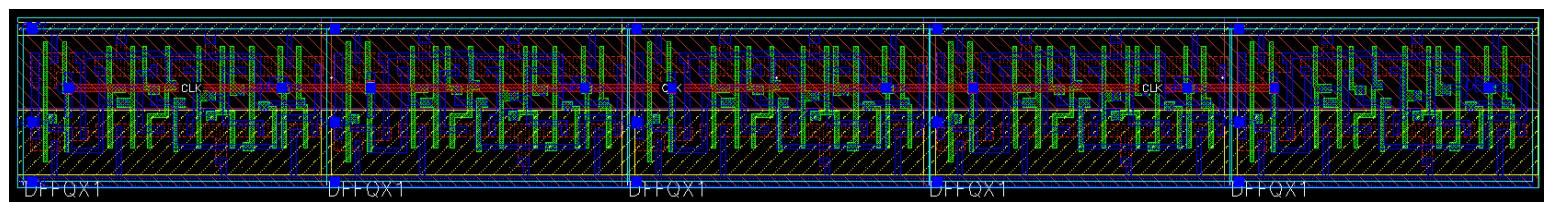
- $\text{Opcode}[2:1] = 00 \Rightarrow$  Shift by 1
- $\text{Opcode}[2:1] = 01 \Rightarrow$  Shift by 2
- $\text{Opcode}[2:1] = 10 \Rightarrow$  Shift by 3
- $\text{Opcode}[2:1] = 11 \Rightarrow$  Shift by 4 (no shifting)

# OPCODE Register

## Schematic



## Layout



## LVS

PVS 22.21-64b Reports: Done [LVS] OPCODE\_Reg... (on micron2.eng.tau.ac.il)

[LVS] OPCODE\_Reg... x

```
# #####
```

PVS Comparison Finished. Thu Apr 25 17:01:07 2024

Creating cross reference ...

```
*****
```

pvs\_RCXref 22.21-s031 64 bit (Thu Apr 20 20:17:00 PDT 2023)  
Build Ref No.: 031 Production (04-20-2023) [pvs\_2221]

Copyright 2023 Cadence Design Systems, Inc.  
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Build O/S: Linux x86\_64 3.10.0-693.el7.x86\_64  
Executed on: micron2.eng.tau.ac.il (Linux x86\_64 3.10.0-1160.92.1.el7.x86\_64)  
Process Id: 12471  
Starting Time: Thu Apr 25 17:01:08 2024 (Thu Apr 25 14:01:08 2024 GMT)  
With parameters: -format C -nxlf -ixf /project/gpdk45/users/orshaul/ws/PVS\_RESULTS/LVS/OPCODE\_Register/svdb/OPCODE\_Register OPCODE\_Register.rep

```
*****
```

Total CPU Time : 0(s)  
Total Real Time : 0(s)  
Memory Used : 88.55 (M)

pvs\_RCXref Done  
Checking in all SoftShare licenses.

**PVS 22.21-64b LVS Run Stat...**

ERC Results: **Empty**  
Extraction Results: **Clean**  
Comparison Results: **Match**

Do you want to start the LVS DE? **Yes** **No**

## DRC

PVS 22.21-64b Reports: Done [DRC] OPCODE\_Reg... (on micron2.eng.tau.ac.il)

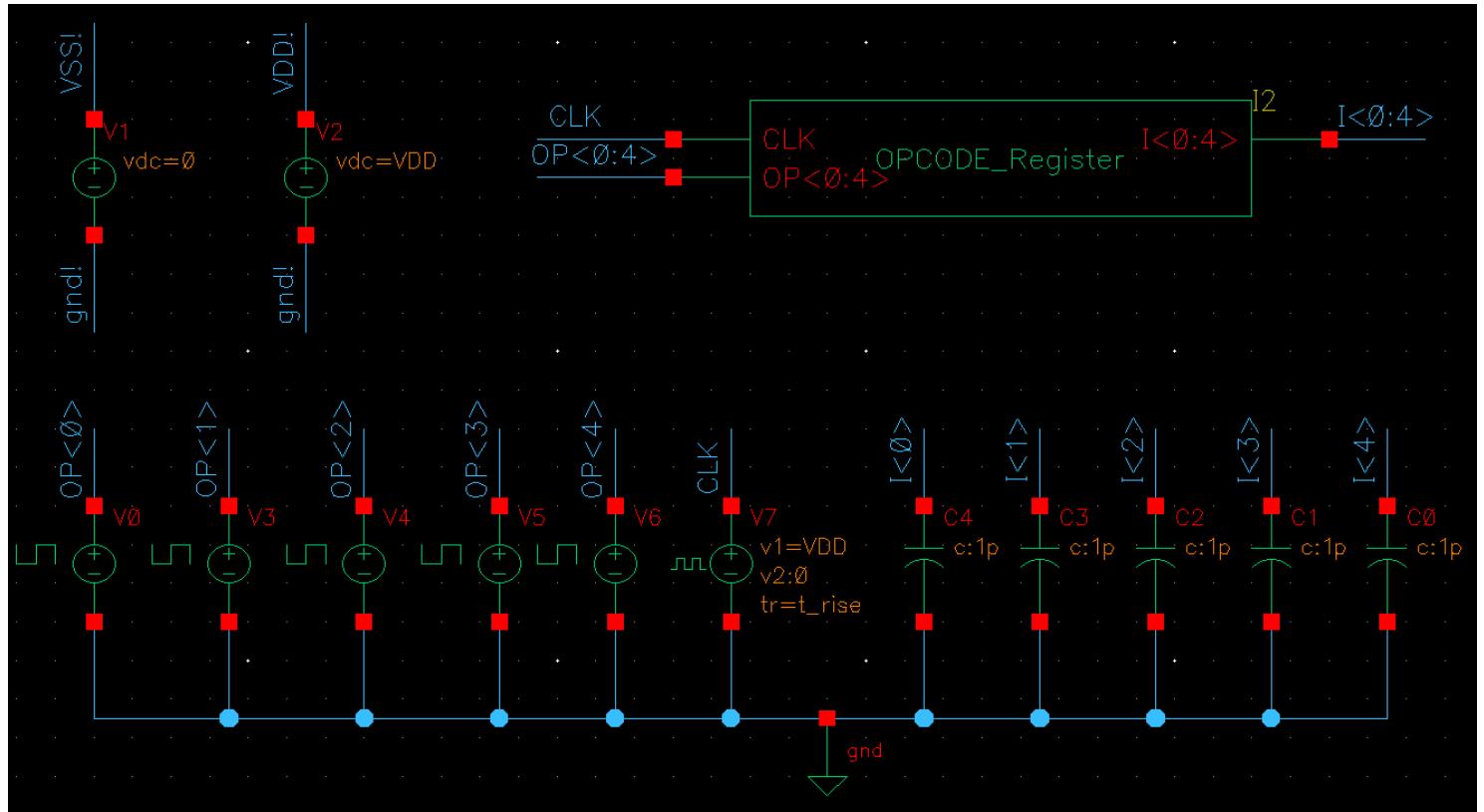
[DRC] OPCODE\_Reg... x

```
Total CPU Time : 2(s)
Total Real Time : 3(s)
Peak Memory Used : 19(M)
Total Original Geometry : 138(634)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file OPCODE_Register.sum
ASCII report database is /project/gpdk45/users/orshaul/ws/PVS_RESULTS/DRC/OPCODE_Register/OPCODE_Register.ascii
Checking in all SoftShare licenses.
```

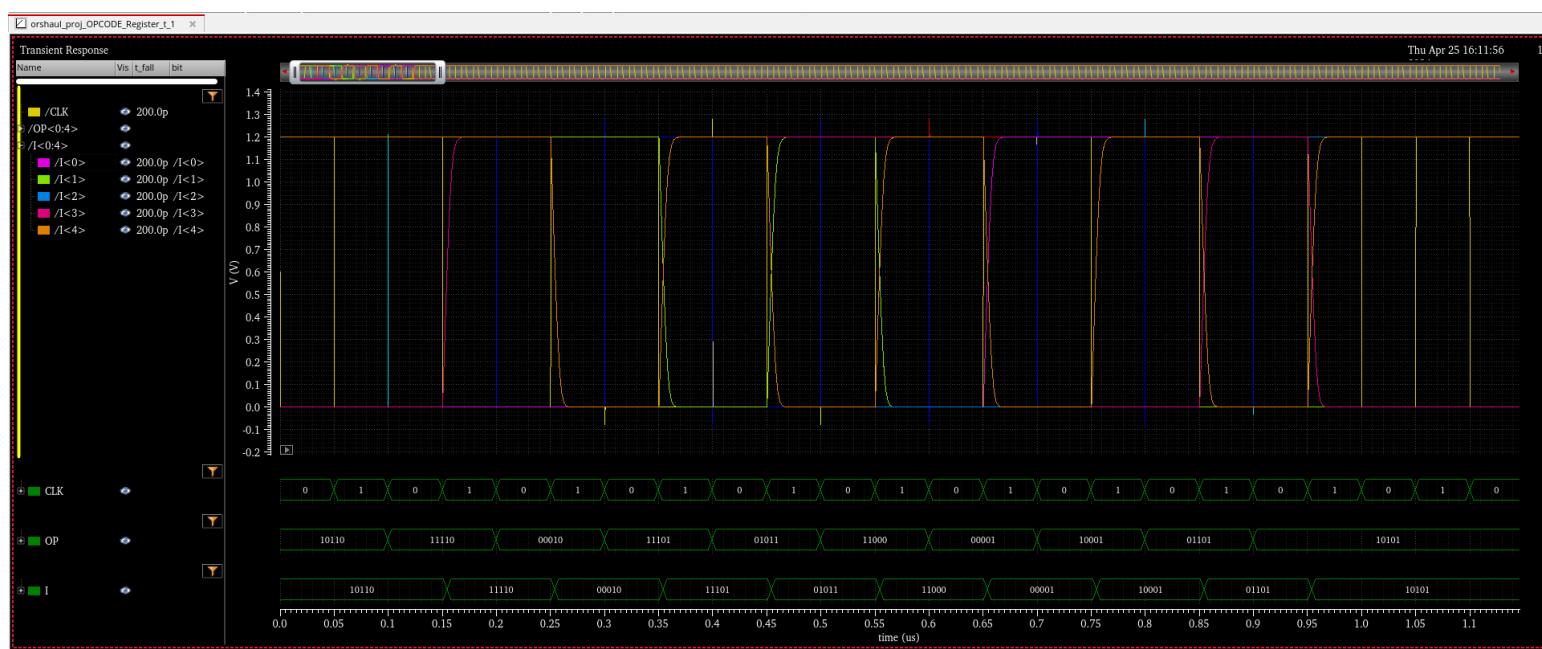
Design Rule Check Finished Normally. Thu Apr 25 17:02:35 2024

# OPCODE Register Testbench

## Schematic



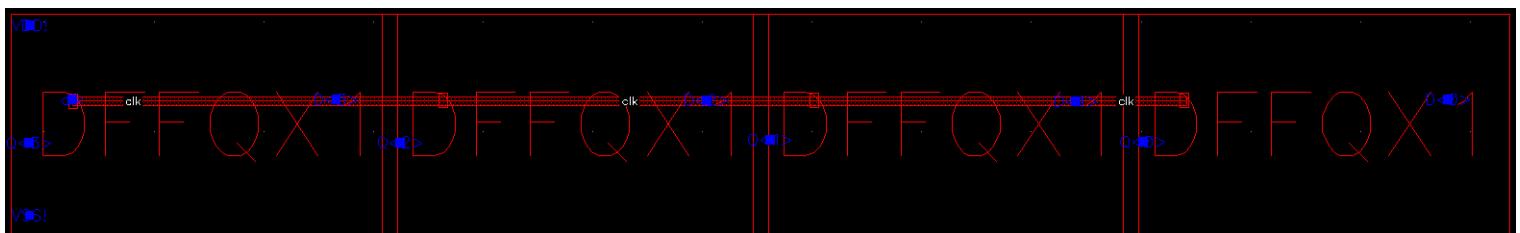
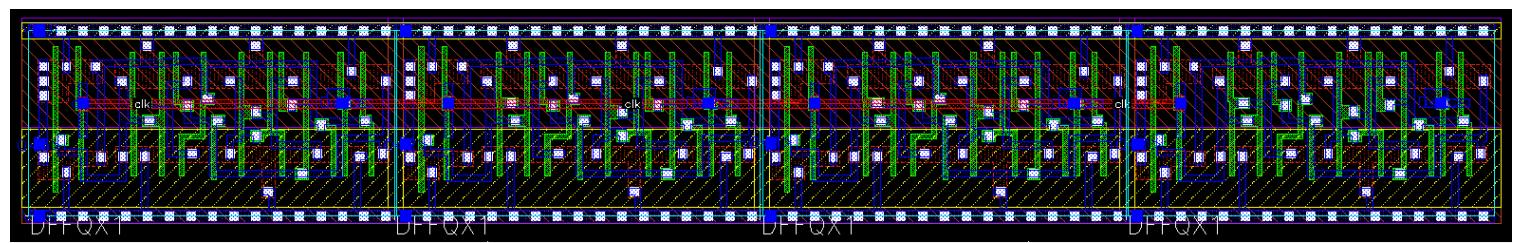
## Graphs



# Register\_4bit



## Layout



LVS

PVS Comparison Finished. Thu Apr 25 17:16:10 2024

Creating cross reference ...

\*\*\*\*\*  
pvs\_RCXref 22.21-s031 64 bit (Thu Apr 20 2017:00 PDT 2023)  
Build Ref No.: 031 Production (04-20-2023) [pvs\_2221]

Copyright 2023 Cadence Design Systems, Inc.  
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Build O/S: Linux x86\_64 3.10.0-693.el7.x86\_64  
Executed on: micron2.eng.tau.ac.il (Linux x86\_64 3.10.0-1160.92.1.el7.x86\_64)  
Process Id: 31555  
Starting Time: Thu Apr 25 17:16:10 2024 (Thu Apr 25 14:16:10 2024 GMT)  
With parameters: -format C -nxF -ixF /project/gpdk45/users/orshaul/ws/PVS\_RESULTS/LVS/Register\_4bit/svdb/Register\_4bit\_Register\_4bit.rep  
\*\*\*\*\*

Total CPU Time : 0(s)  
Total Real Time : 0(s)  
Memory Used : 87.05(M)

pvs\_RCXref Done  
Checking in all SoftShare licenses.

**PVS 22.21-64b LVS Run Stat...**

<input checked="" type="checkbox"/>	ERC Results	Empty
<input type="checkbox"/>	Extraction Results:	Clean
<input type="checkbox"/>	Comparison Results:	Match

Do you want to start the LVS DE?

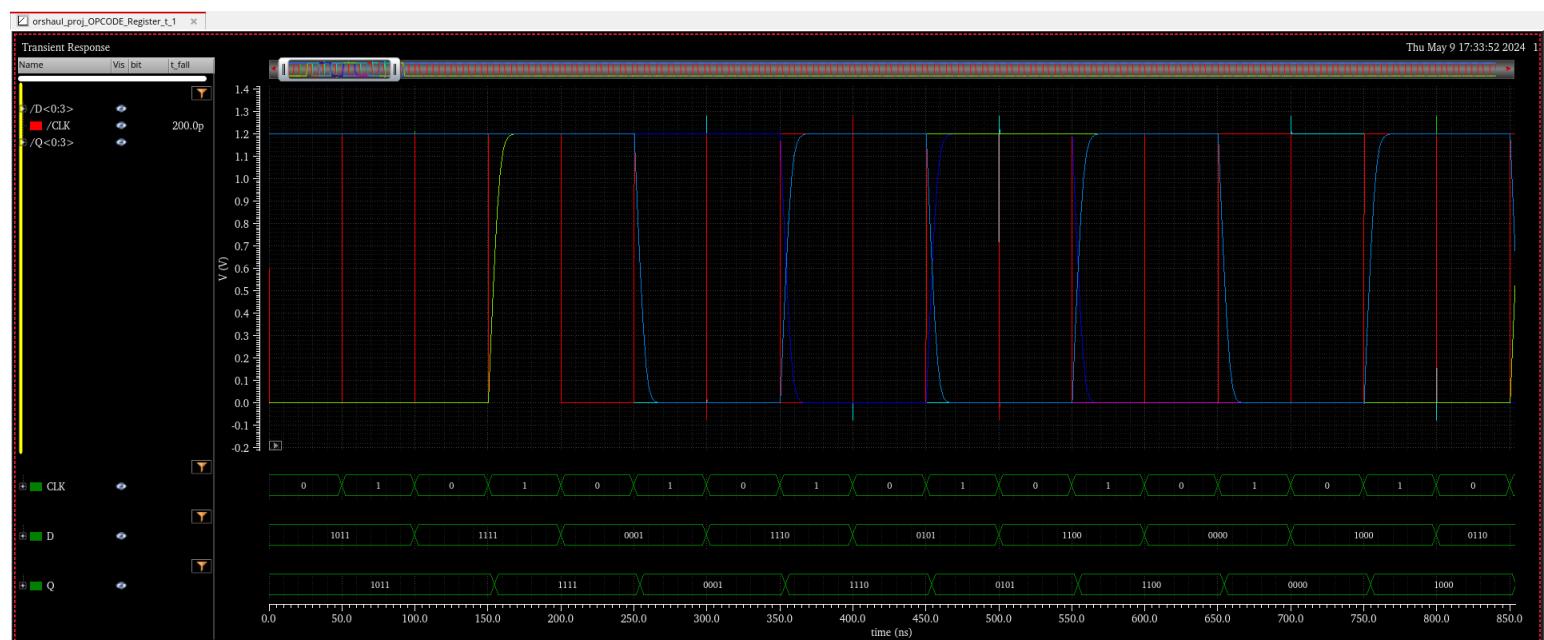
## DRC

```
PVS 22.21-64b Reports: Done [DRC] Register_4bit... (on micron2.eng.tau.ac.il)
[DRC] Register_4bit x

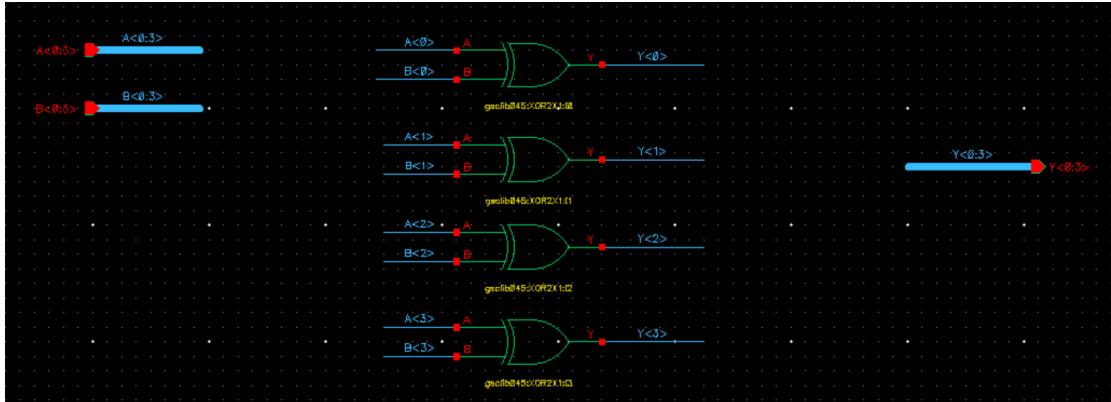
Total CPU Time : 2 (s)
Total Real Time : 3 (s)
Peak Memory Used : 19 (M)
Total Original Geometry : 136 (508)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file Register_4bit.sum
ASCII report database is /project/gpdk45/users/orshaul/ws/PVS_RESULTS/DRC/Register_4bit/Register_4bit.ascii
Checking in all SoftShare licenses.

Design Rule Check Finished Normally. Thu Apr 25 17:18:09 2024
```

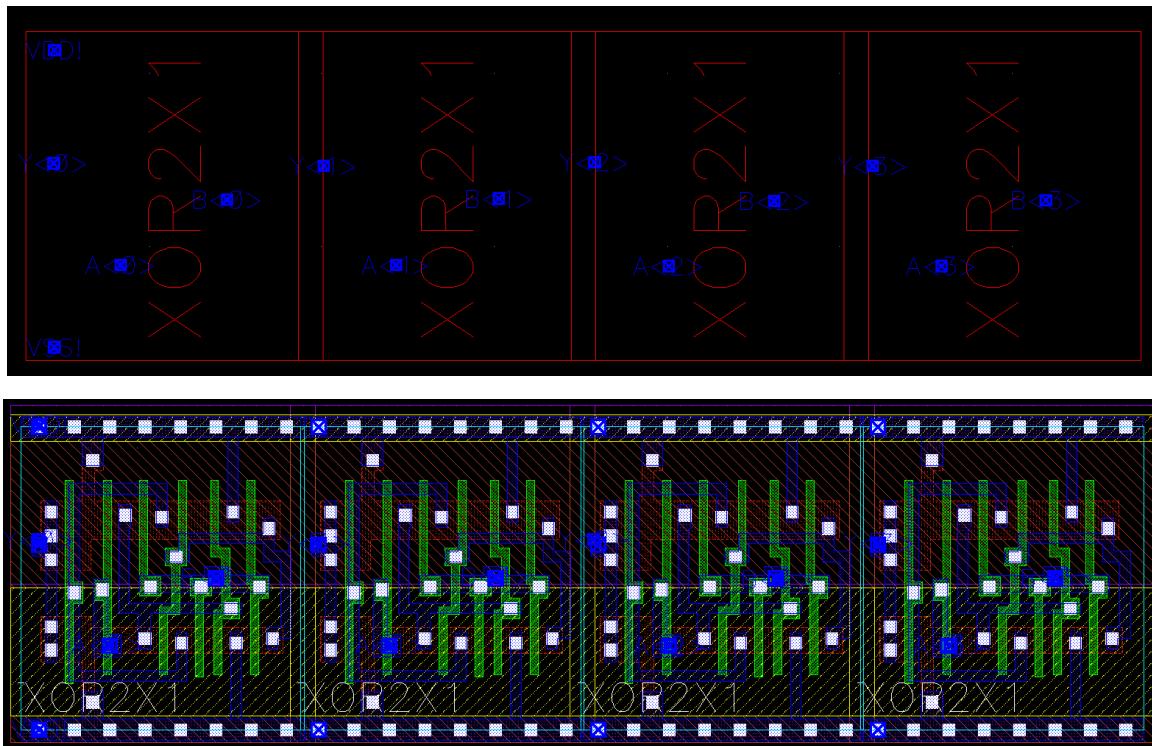
## Graphs



## Bitwise XOR Schematic



## Layout



## LVS

The LVS Comparison Results window displays the comparison between the schematic and layout. The window is divided into two main sections: a terminal window on the left and a status window on the right.

**Terminal Window Output:**

```

[LVS] Bitwise_XOR
=====
Creating cross reference ...
=====
pvs_RCXref 22.21-8031 64 bit (Thu Apr 20 20:17:00 PDT 2023)
Build Ref No.: 031 Production (04-20-2023) [pvs_2221]

Copyright 2023 Cadence Design Systems, Inc.
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Build O/S: Linux x86_64 3.10.0-693.11.1.x86_64
Executed on: micron2.eng.tau.ac.il (Linux x86_64 3.10.0-1160.92.1.e17.x86_64)
Process Id: 15904
Starting Time: Thu Apr 25 17:46:52 2024 (Thu Apr 25 14:46:52 2024 GMT)
With parameters: -format C -nxf -ifx /project/gpdk45/users/orshaul/ws/PVS_RESULTS/LVS/Bitwise_XOR/svdb/Bitwise_XOR.Bitwise_XOR.rep
=====

Total CPU Time : 0(s)
Total Real Time : 0(s)
Memory Used : 84.66(M)

pvs_RCXref Done
Checking in all SoftShare licenses.

```

**Status Window:**

PVS 22.21-64b Reports: Done [LVS] Bitwise\_XO... (on micron2.eng.tau.ac.il)

PVS Comparison Finished. Thu Apr 25 17:46:52 2024

=====
Creating cross reference ...
=====
pvs\_RCXref 22.21-8031 64 bit (Thu Apr 20 20:17:00 PDT 2023)
Build Ref No.: 031 Production (04-20-2023) [pvs\_2221]

Copyright 2023 Cadence Design Systems, Inc.
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Build O/S: Linux x86\_64 3.10.0-693.11.1.x86\_64
Executed on: micron2.eng.tau.ac.il (Linux x86\_64 3.10.0-1160.92.1.e17.x86\_64)
Process Id: 15904
Starting Time: Thu Apr 25 17:46:52 2024 (Thu Apr 25 14:46:52 2024 GMT)
With parameters: -format C -nxf -ifx /project/gpdk45/users/orshaul/ws/PVS\_RESULTS/LVS/Bitwise\_XOR/svdb/Bitwise\_XOR.Bitwise\_XOR.rep
=====

Total CPU Time : 0(s)
Total Real Time : 0(s)
Memory Used : 84.66(M)

pvs\_RCXref Done
Checking in all SoftShare licenses.

**Run Status:**

ERC Results: Empty  
Extraction Results: Clean  
Comparison Results: Match

Do you want to start the LVS DE?

## DRC

```

PVS 22.21-64b Reports: Done [DRC] Bitwise_XO... (on micron2.eng.tau.ac.il)

[DRC] Bitwise_XOR x

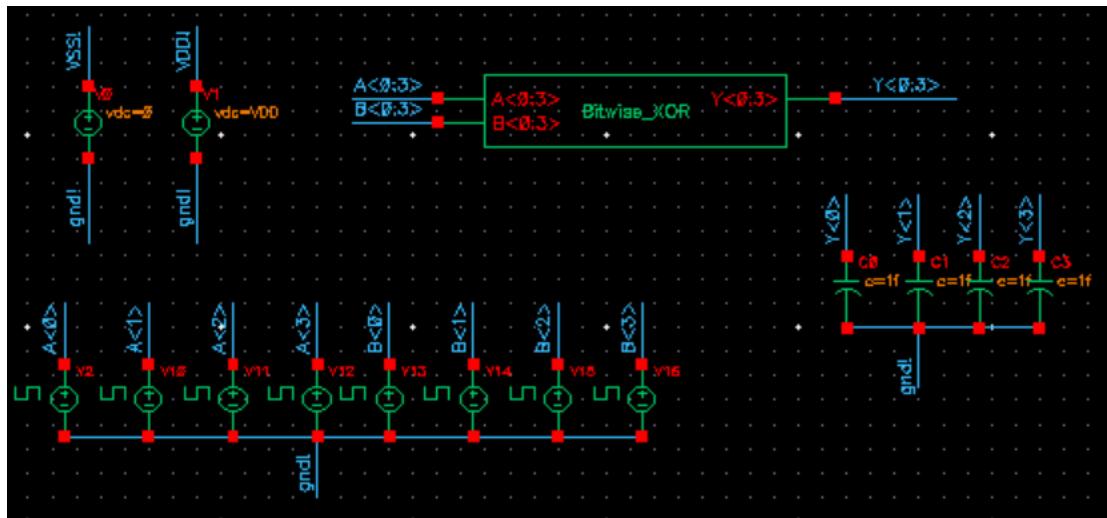
Total CPU Time : 2 (s)
Total Real Time : 3 (s)
Peak Memory Used : 19 (M)
Total Original Geometry : 85 (298)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file Bitwise_XOR.sum
ASCII report database is /project/gpdk45/users/orshaul/ws/PVS_RESULTS/DRC/Bitwise_XOR/Bitwise_XOR.ascii
Checking in all SoftShare licenses.

Design Rule Check Finished Normally. Thu Apr 25 17:40:26 2024

```

## **Bitwise XOR Test bench**

### Schematic

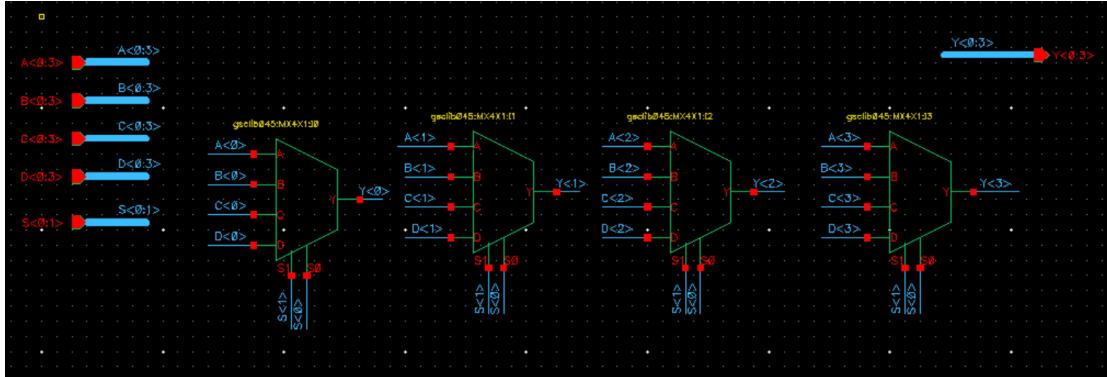


### Graphs

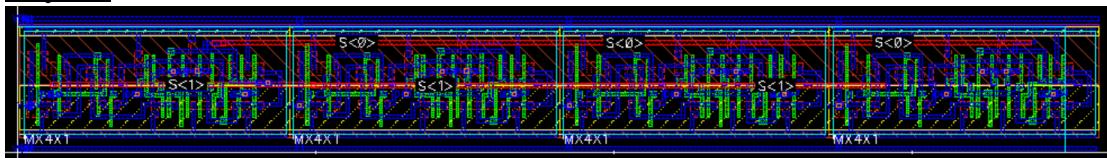
WE TESTED TWO SIGNALS A: 0110 AND B: 1101 WE GOT THE RESULT WE WERE EXPECTING DUE TO THE XOR TRUTH TABLE Y: 1011



## Output Mux 4:1 Schematic



## Layout



## DRC

```

PVS 22.21-64b Reports: Done [DRC] mux4_... (on micron2.eng.tau.ac.il)
[DRC] mux4_1 x

PATTERN_MATCH: Cumulative Time CPU = 0 (s) REAL = 0 (s)
DFM FILL: Cumulative Time CPU = 0 (s) REAL = 0 (s)

Total CPU Time : 2 (s)
Total Real Time : 2 (s)
Peak Memory Used : 19 (M)
Total Original Geometry : 213 (669)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file mux4_1.sum
ASCII report database is /project/gpdk45/users/orshaul/ws/PVS_RESULTS/DRC/mux4_1/mux4_1.ascii
Checking in all SoftShare licenses.

Design Rule Check Finished Normally. Tue May 7 12:30:15 2024

```

## LVS

```

PVS 22.21-64b Reports: Done [LVS] mux4_... (on micron1.eng.tau.ac.il)
[DRC] Bitwise_XOR... x [DRC] Bitwise_XOR x [LVS] Bitwise_XOR x [DRC] output_mux x [DRC] mux4_1 x [LVS] mux4_1 x

Build O/S: Linux x86_64 3.10.0-693.el7.x86_64
Executed on: micron1.eng.tau.ac.il (Linux x86_64 3.10.0-1160.92.1.el7.x86_64)
Process Id: 55402
Starting Time: Wed Apr 24 16:53:47 2024 (W
With parameters: -format C -nxm -ixf /projec
*****
Total CPU Time : 0 (s)
Total Real Time : 0 (s)
Memory Used : 85.36 (M)

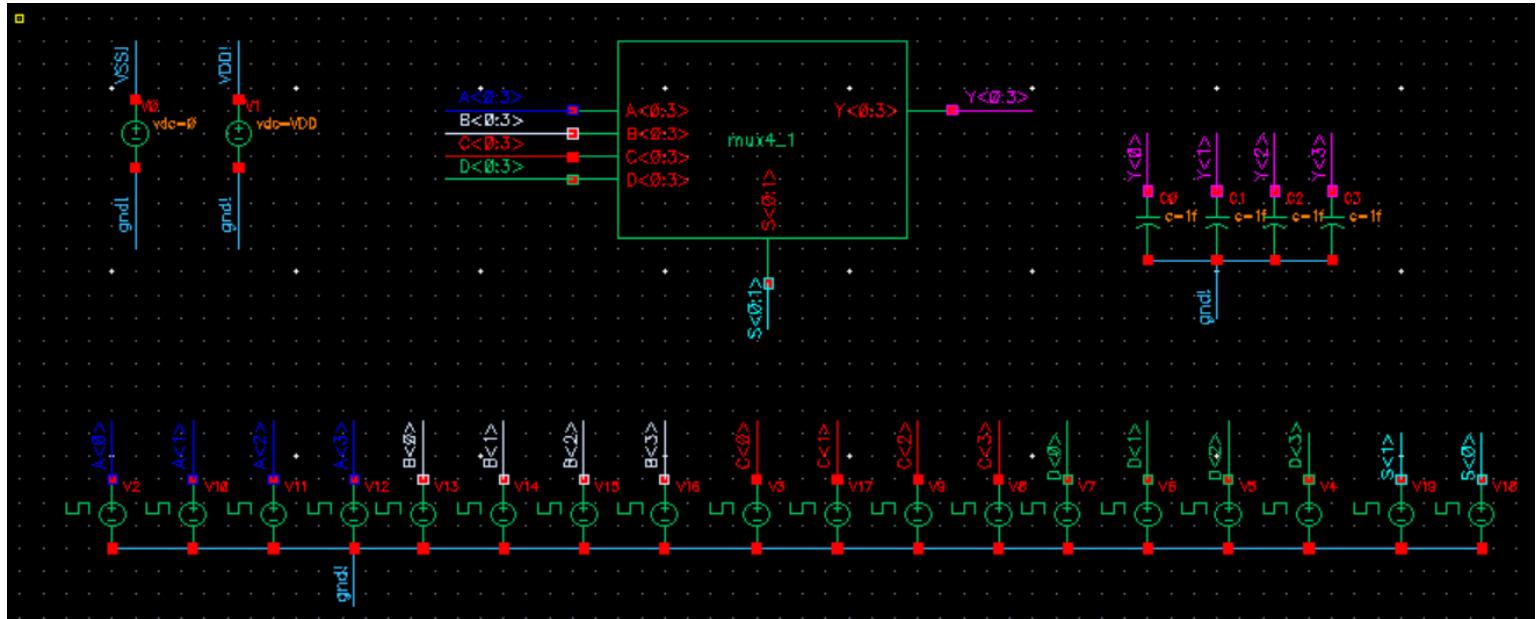
pvs_RCXref Done
Checking in all SoftShare licenses.

PVS 22.21-64b LVS Run Stat...
RESU
*****
ERC Results Empty
Extraction Results: Clean
Comparison Results: Match
Do you want to start the LVS DE? Yes No

```

# Output MUX 4:1 Test bench

## Schematic

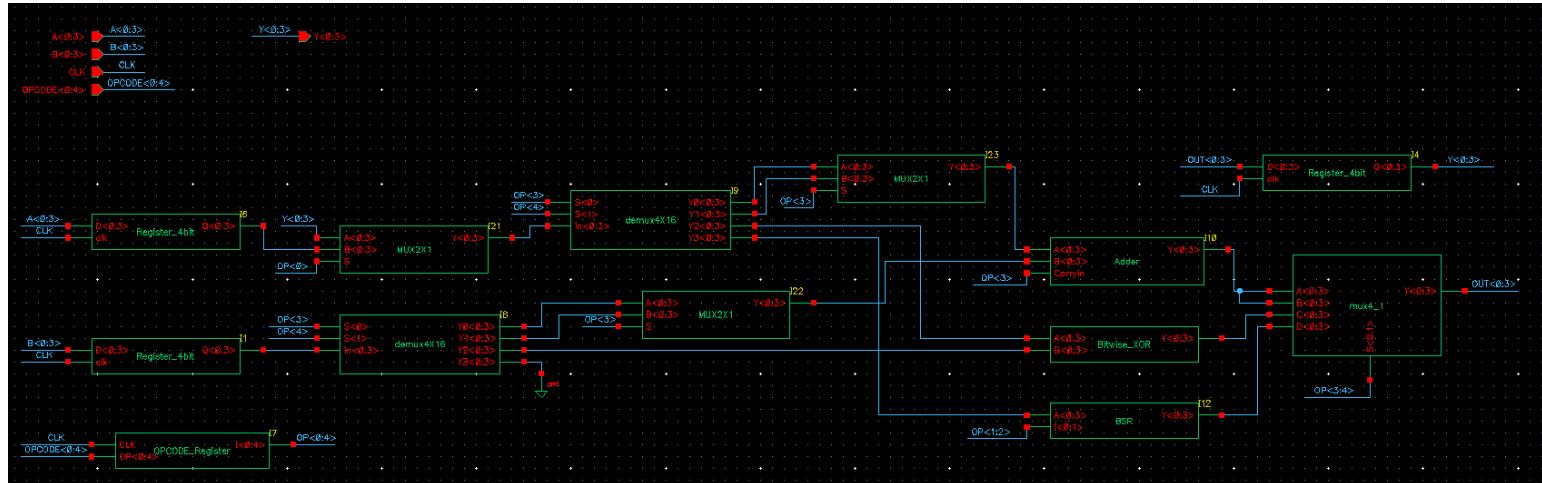


## Graphs



# ALU

## Schematic



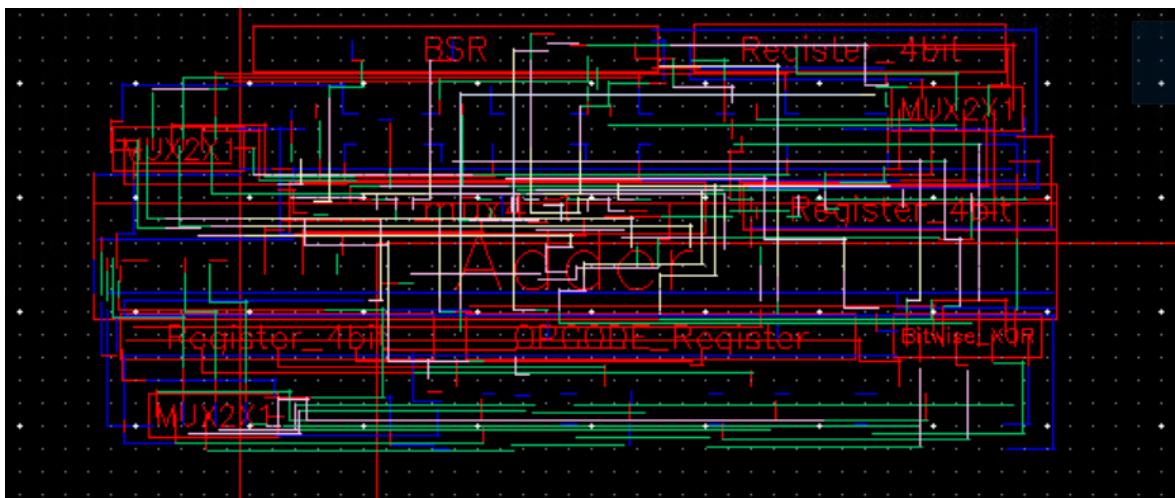
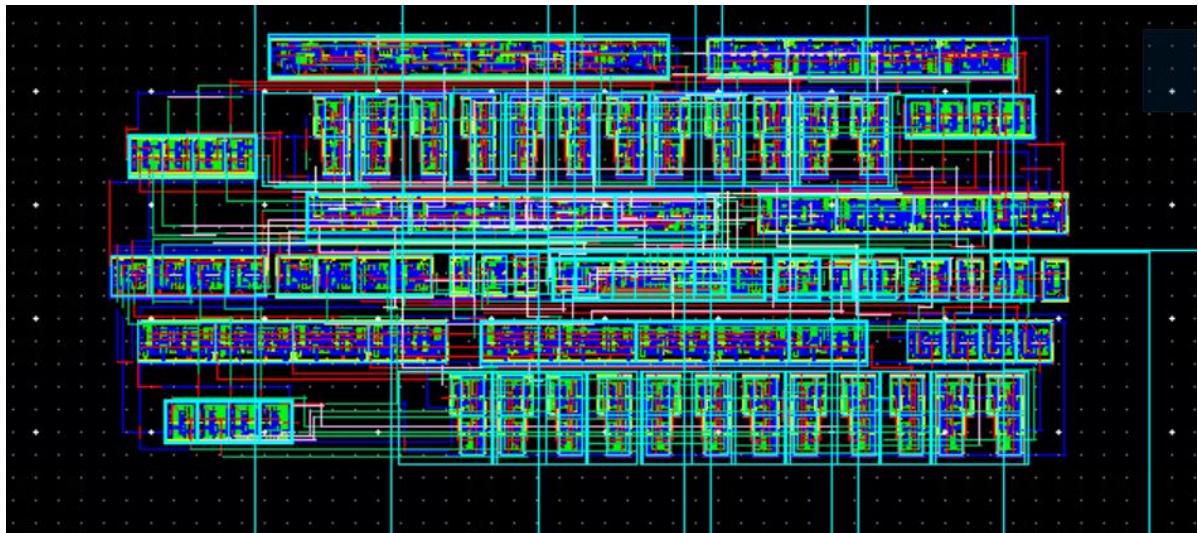
## Opcode Table – L

במהלך המימוש של מעגל ה-ALU שינו משלב התוכנון כחלק מאופטימיזציה לمعالג. נציג כאן את טבלת ה-OPCODE החדשה, לפיה נציג את תוכנות הסימולציות בפרויקט.

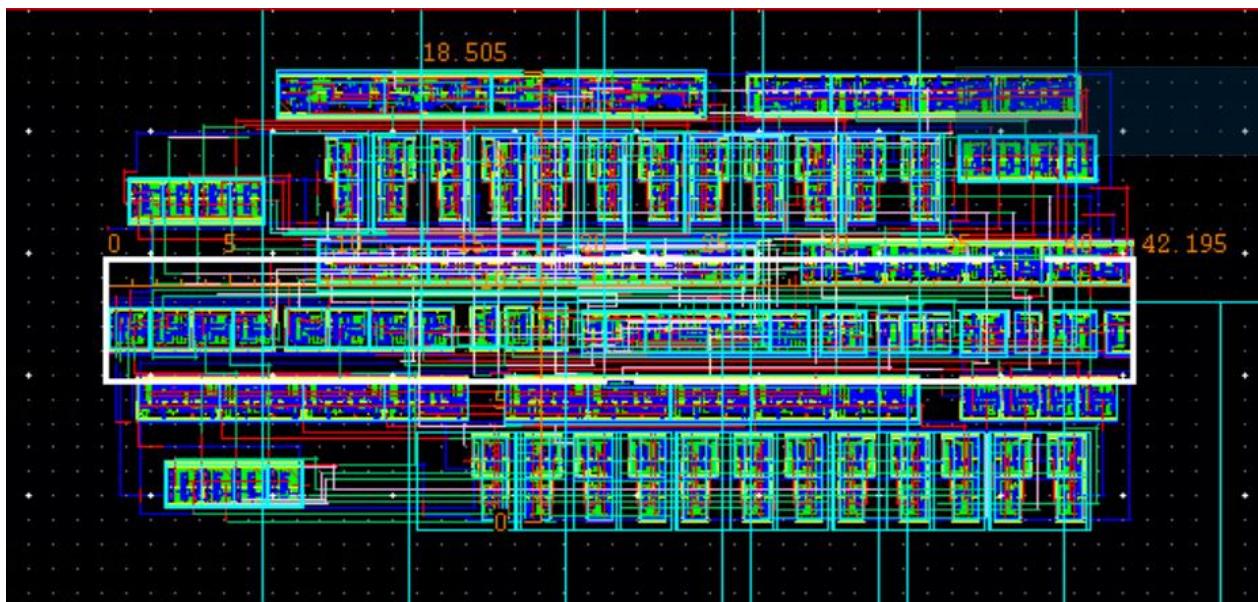
Operation	Opcode[4]	Opcode[3]
ADD	0	0
SUB	0	1
XOR	1	0
BSR	1	1

- Opcode[2:1] - represents the number of shifts the BSR should do:
  - Opcode[2:1] = 00 => Shift by 1
  - Opcode[2:1] = 01 => Shift by 2
  - Opcode[2:1] = 10 => Shift by 3
  - Opcode[2:1] = 11 => Shift by 4 (no shifting actually)

## Layout



### Realization Area:



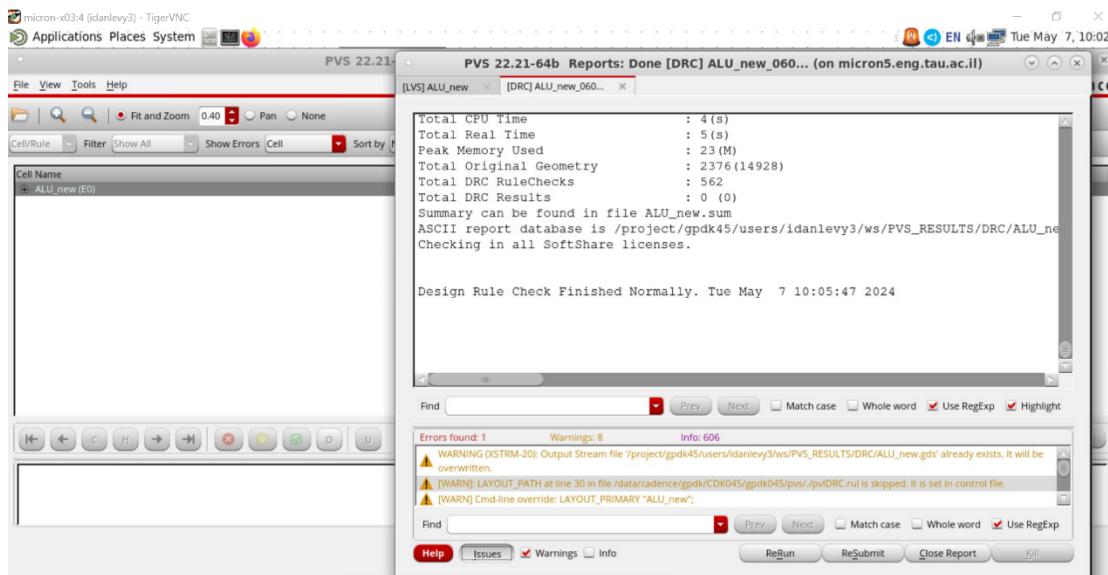
במהלך העבודה ביצענו תיקון לחישוב השטח הכלול של המימוש וקיבלנו שטח סך כל הרכיבים בمعالג ה – ALU :

$524.096\mu\text{m}^2$

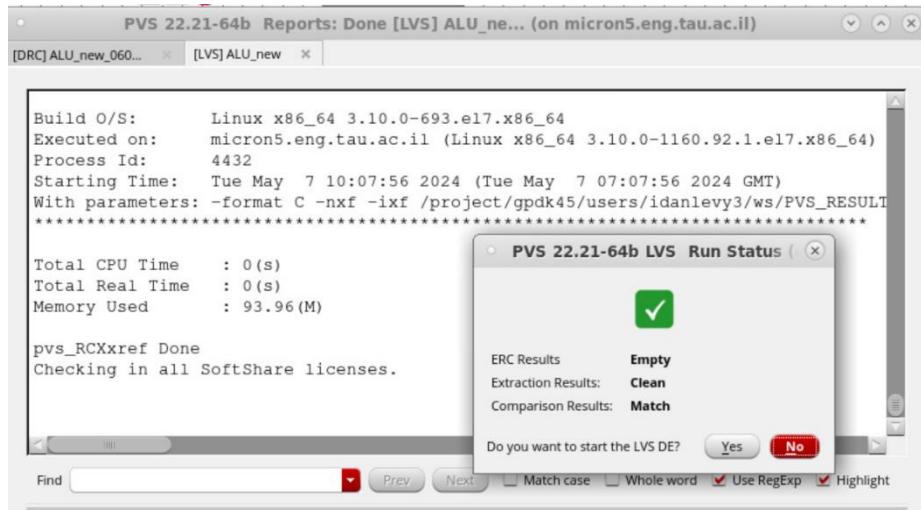
ניתן לראות שחברנו והצבנו את הבלוקים בצורה אופטימלית ולא חריגנו מ 150% מהתוכנו המקורי וקיבלנו שטח של :

$780.82\mu\text{m}^2$

## DRC

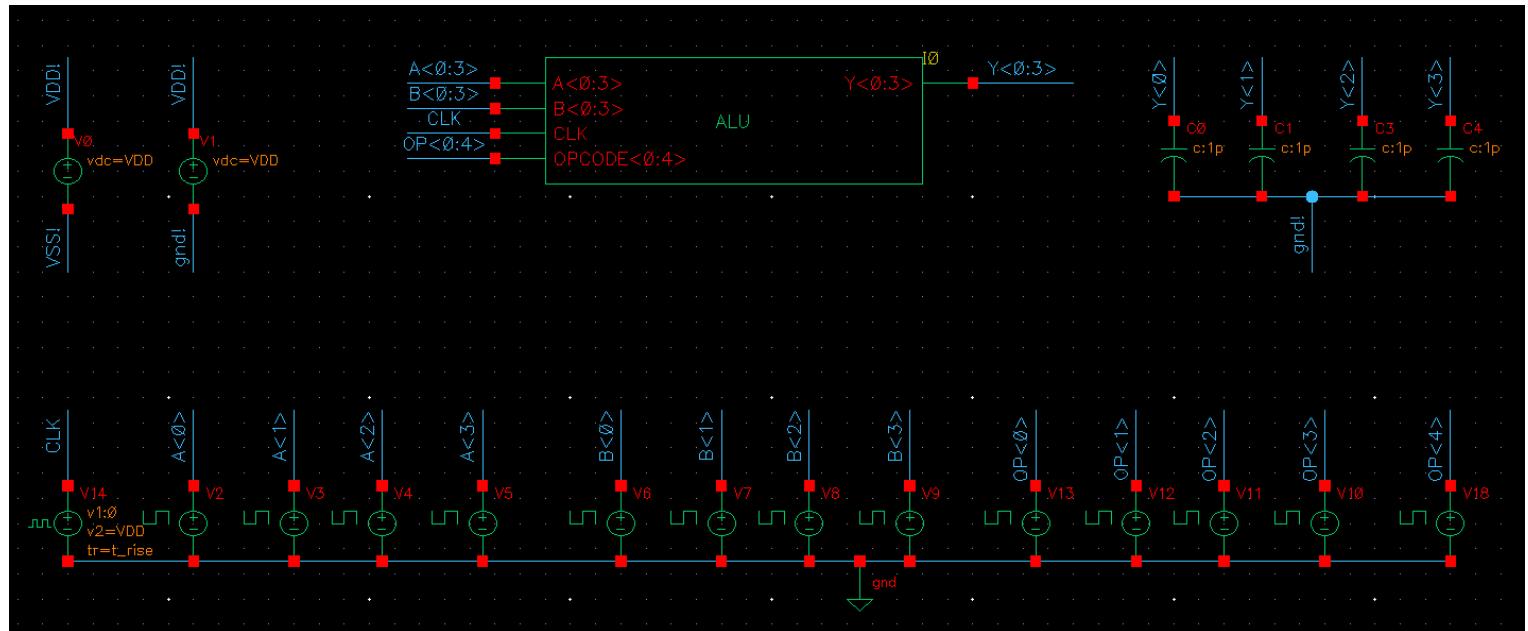


## LVS



## ALU\_t TESTBENCH

### Schematics

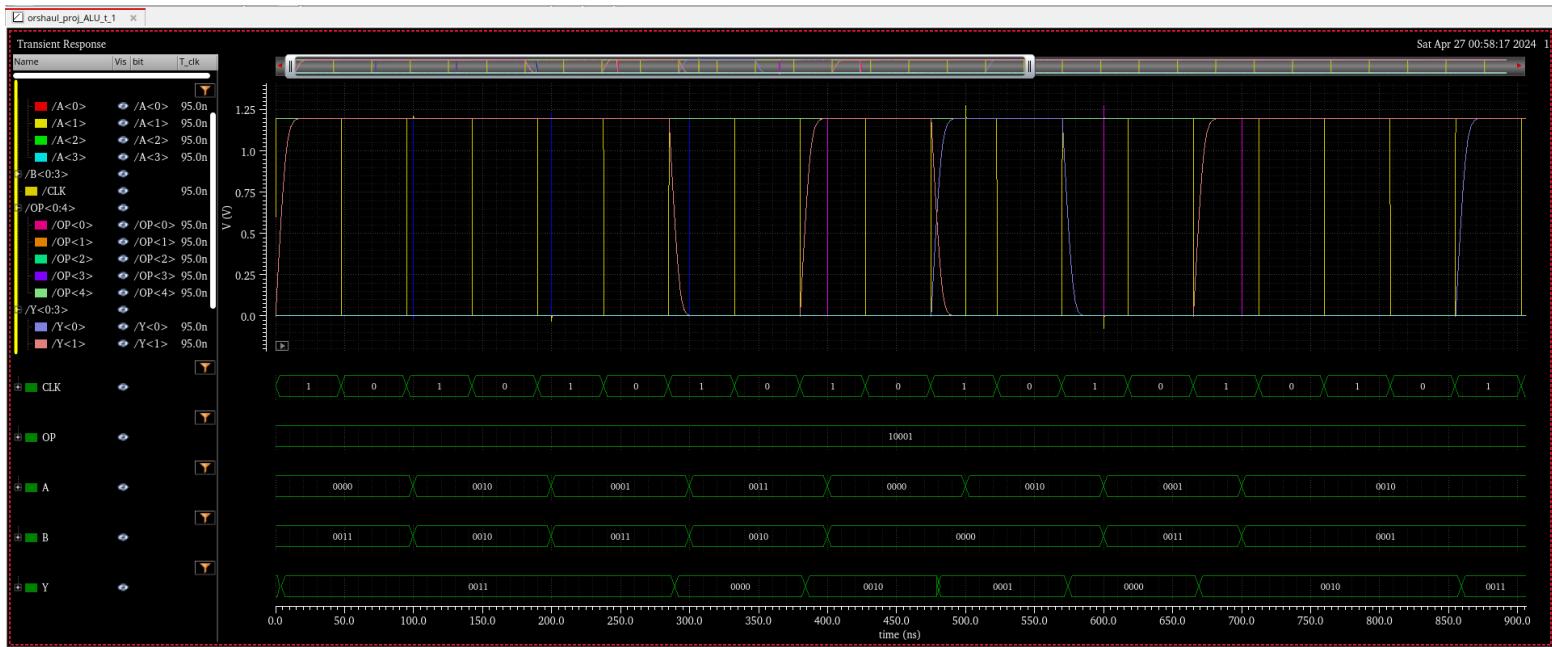


### סימולציות לתקינות ה- ALU עם וללא פידבק (OP[0]=1/0)

בחרנו את  $bits$  באופן כזה שיהיה אפשר לראות חלוקה ברורה בין מקרה בו אנו לוקחים את מחרוזת A לבין מחרוזת כניסה חדשה מהמשתמש לבין המקרה השני בו ניקח את A להיות המוצא Y במחזור שערן הקודם. ככלומר נבחן עבור כל אחד מה- OPCODES את שני המקרים כאשר יש/אין פידבק, ככלומר כאשר OP[0]=0/1 ונשים לב כי התוצאה הרצויה מגיעה במחזור שעון הבא.

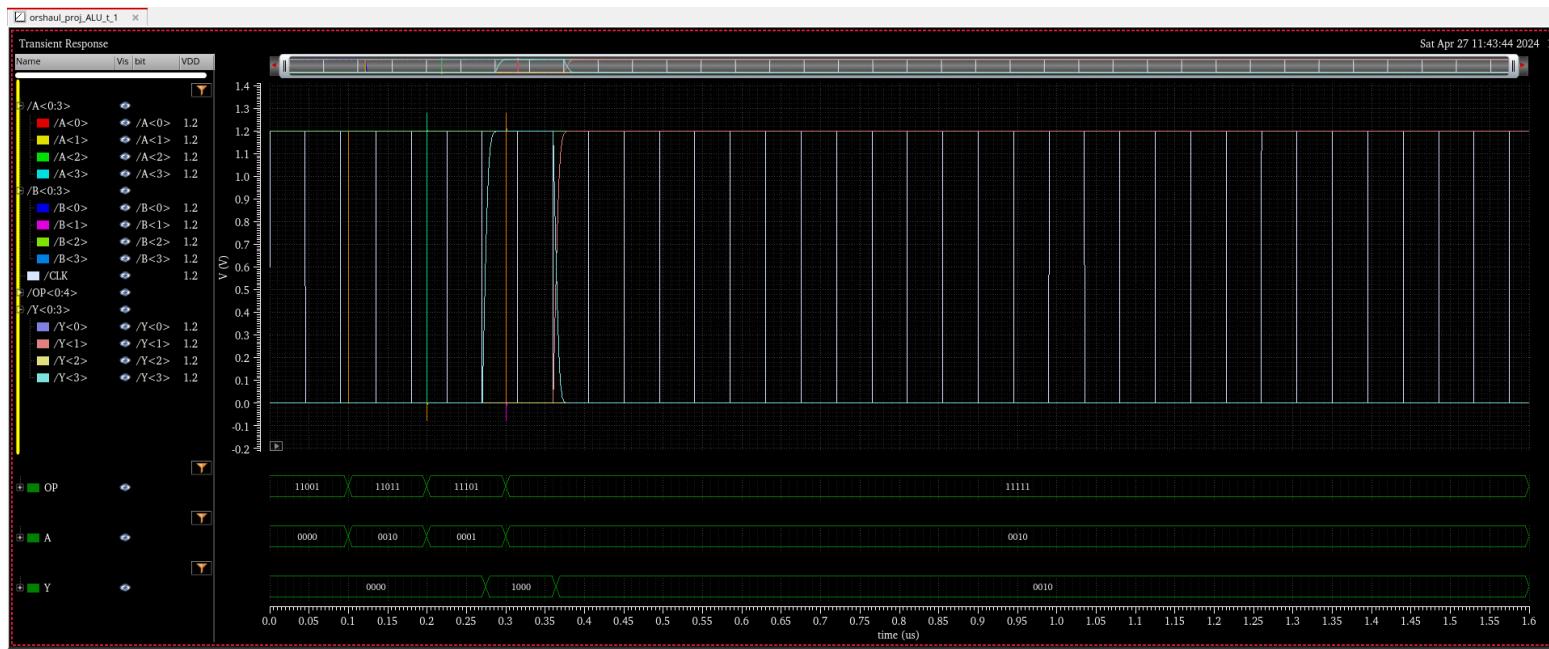
## Graphs

נבצע סימולציה לתקינות פועלות **XOR** (OP=10000/10001).  
 נבחן את המקרה בו אין פידבק מהМОץא כלומר כאשר  $OP[0]=1$ .



## נבע סימולציה לתקינות פועלות BSR

נבחן את המקרה בו אין פידבק מהמושג כלומר כאשר  $OP[0]=0$



### נבע סימולציה לתקינות פועלות SUB

נבחן את המקרה בו אין פידבק מה מוצר כלומר כאשר  $OP=0$



נבצע סימולציה לתקינות פועלות ADD  
נבחן את המקרה בו אין פידבק מהМОץא קלומר כאשר  $OP[0]=1$ .



- נבצע סימולציה של כל הפעולות יחד.  
נבחן את המקרה בו אין פידבק מהМОץא קלומר כאשר  $OP[0]=1$ . נחלק את הפירוט לשלבים:  
שלב 1 : מבוצעת פעולה XOR בין A ל-B,  
שלב 2 : מבוצעת פעולה חיבור  $1110_{14} + 1011_{11} = 11001_{28}$ , נשים לב כי ה-MSB חסר מכיוון שמדובר ב-Overflow.  
שלב 3 : מבוצעת פעולה חיסור  $1110_{14} - 1011_{11} = 0011_3$ .  
שלב 4 : מבוצעת פעולה BSR ב-1,2,3,4.



**נבחן את המקרה בו יש פידבק מהמושג כולם כאשר  $0 = [0]$  OP.**

## XOR

נשים לב שברכף ניתן לראות שהנתוצאות בגרפים Y יוצאות בדילאי של מחזור שעו בגל רגיסטר היציאה לכן צירפנו גם את הכניסה לרגיסטר המוצא (OUT).



BSR

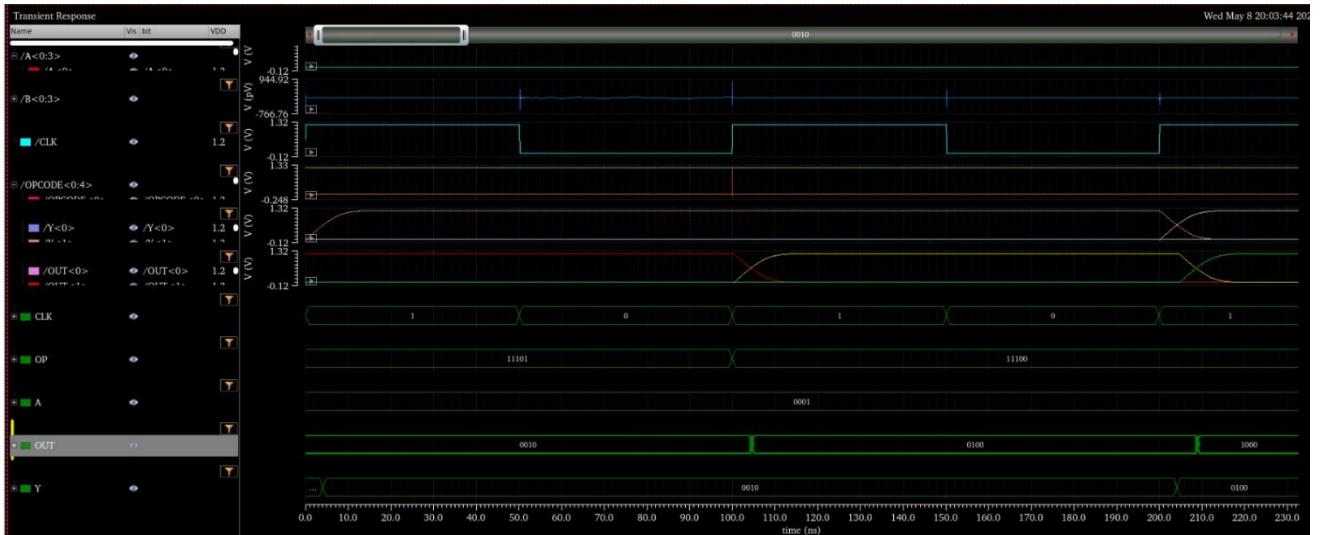
$$X = OPCODE[2:1] = 00 \Rightarrow Shift\ by\ 1$$



$$X = \text{OPCODE}[2:1] = 01 \Rightarrow \text{Shift by 2}$$



$$X = \text{OPCODE}[2:1] = 10 \Rightarrow \text{Shift by 3}$$



$$X = \text{OPCODE}[2:1] = 11 \Rightarrow \text{Shift by 4 (no shifting actually)}$$



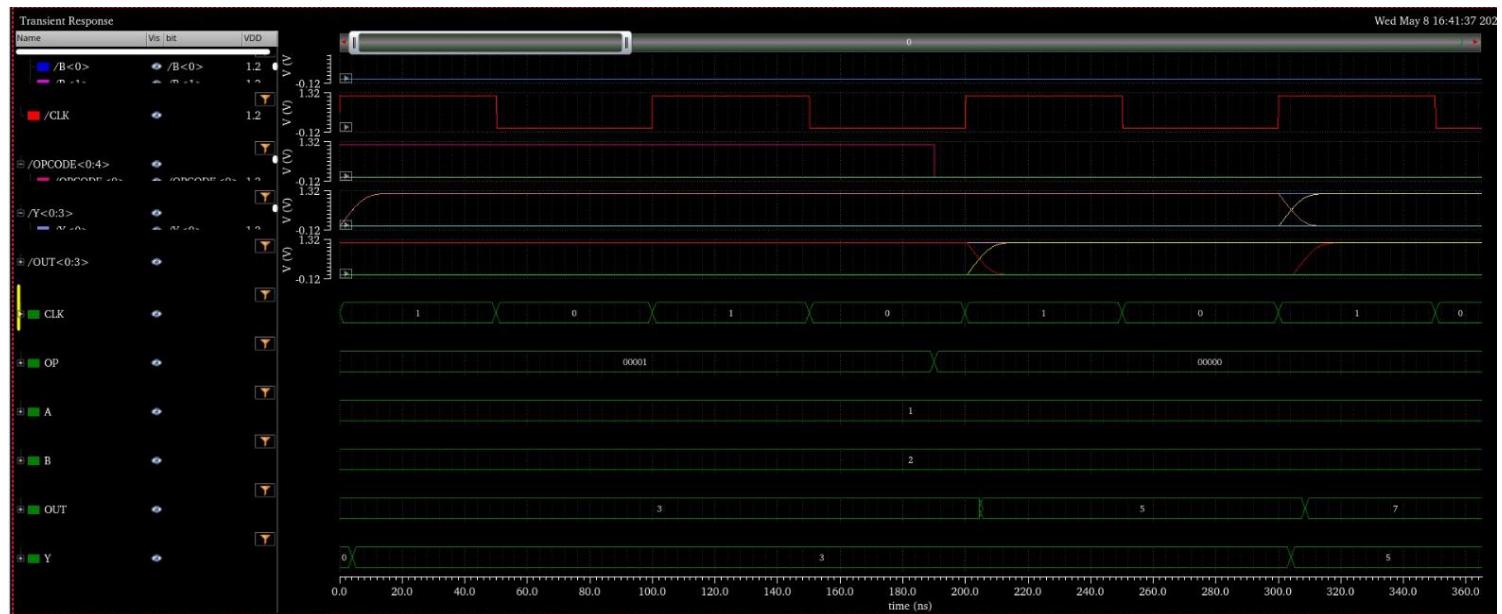
## SUB

ניתן לראות שהחילה מבוצעת פועלות SUB בין A ל-B ולאחר מכן מבוצעת פעולה SUB בין המוצא ל-B.

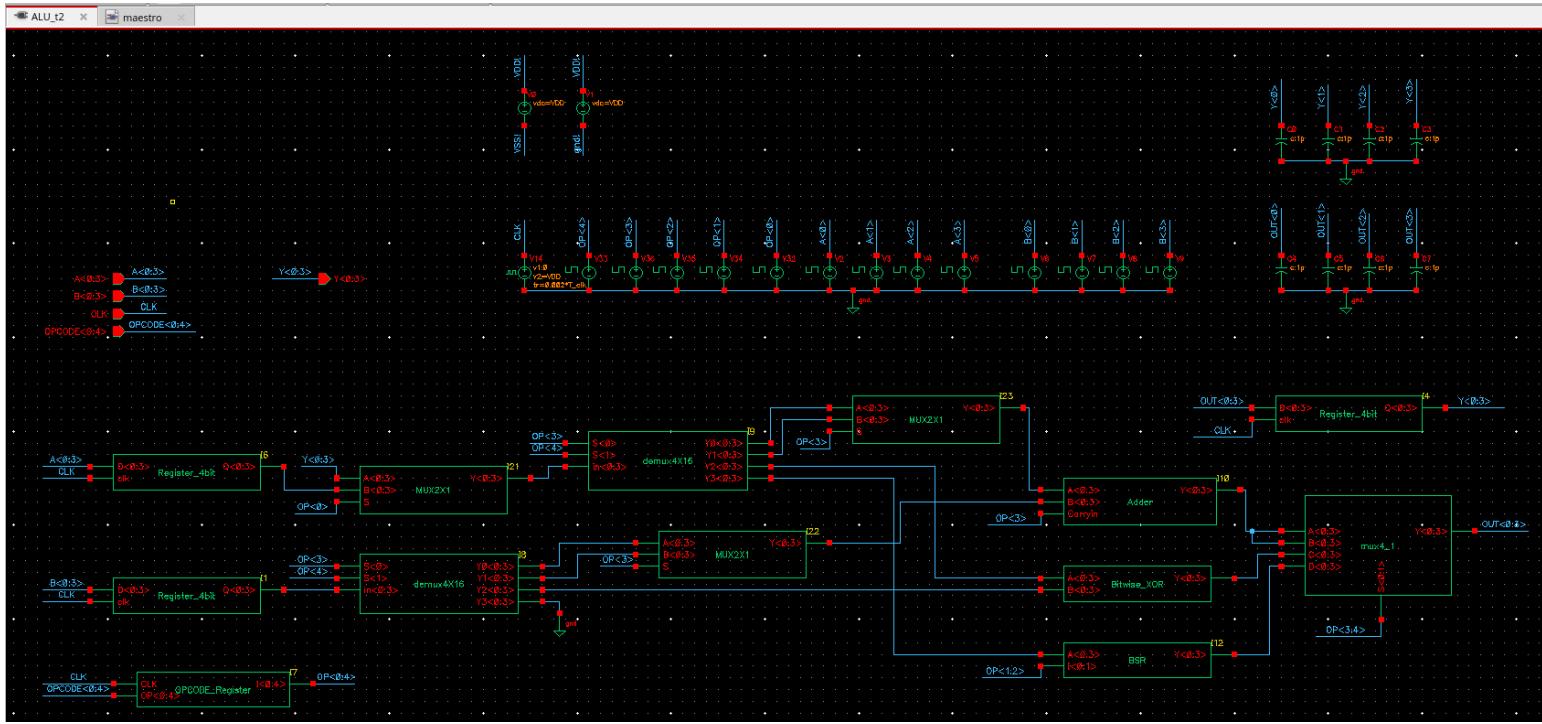


## ADD

ניתן לראות שתחילה מבוצעת פעולה ADD בין A ל-B ולאחר מכן מבוצעת פעולה ADD בין המוצא ל-B.



## Testbench ALU\_T\_2 (Critical path, $t_{setup}$ , $T_{min}$ , $f_{max}$ )

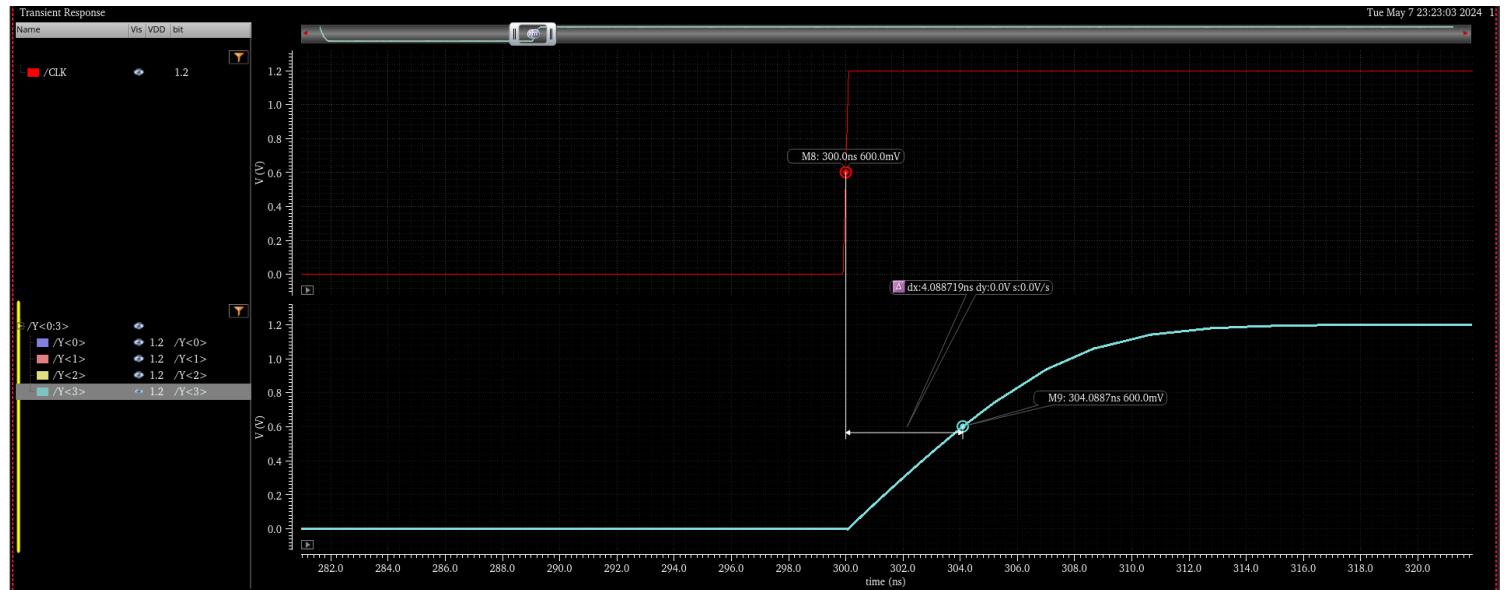


המסלול הקritisטי מתקיים על ידי פעולה החישור בה סיגנלי הכניסה עוברים דרך ה-  
adder והינו היחידה הגדולה ביותר עם  $t_{pd}$  הגדול ביותר.

עבור מתחי ההזנה  $V_{DD}=1.2V$ ,  $0.7V$  נחשב את ההפרש בין עלית השעון CLK לבין המוצא  $y$ . זהו למעשה  $t_{logic} + t_{cq} + t_{setup}$ . זמן זה נדרש להוסיף את ה- $t_{setup}$ . הינו הזמן בו הסיגנל צריך להיות קבוע וכייב בכניסה לרגיסטר אליו נכנסת מחרוזת הכניסה A (או B) על מנת שהרגיסטר ידגם את סיגנל זה באופן תקין. שני הרגיסטרים עברו מחרוזות הכניסה A ו B זהים. לכן, חישוב זמן זה הוא זהה עבור שני הרגיסטרים. את המוצא אינו תואם לכינסה ונמצאים את טווח הקפע עד שנתקבע על זמן ה-  $t_{setup}$  הרצוי לתקינות המעל. נציין שזמן זה חושב על Register\_4bit ולא עבור ה-  
OPCODE\_Register מכיוון שני הרגיסטרים בנויים באותו אופן (מרכיבי D-FF) ושניהם פועלים במקביל כך שנכפה לקבל את אותן התוצאות. לאחר מכן, על מנת למצוא את זמן המחזור המינימלי נחבר בין שני הערכים שקיבלו בהתחלת זה ואת התדר

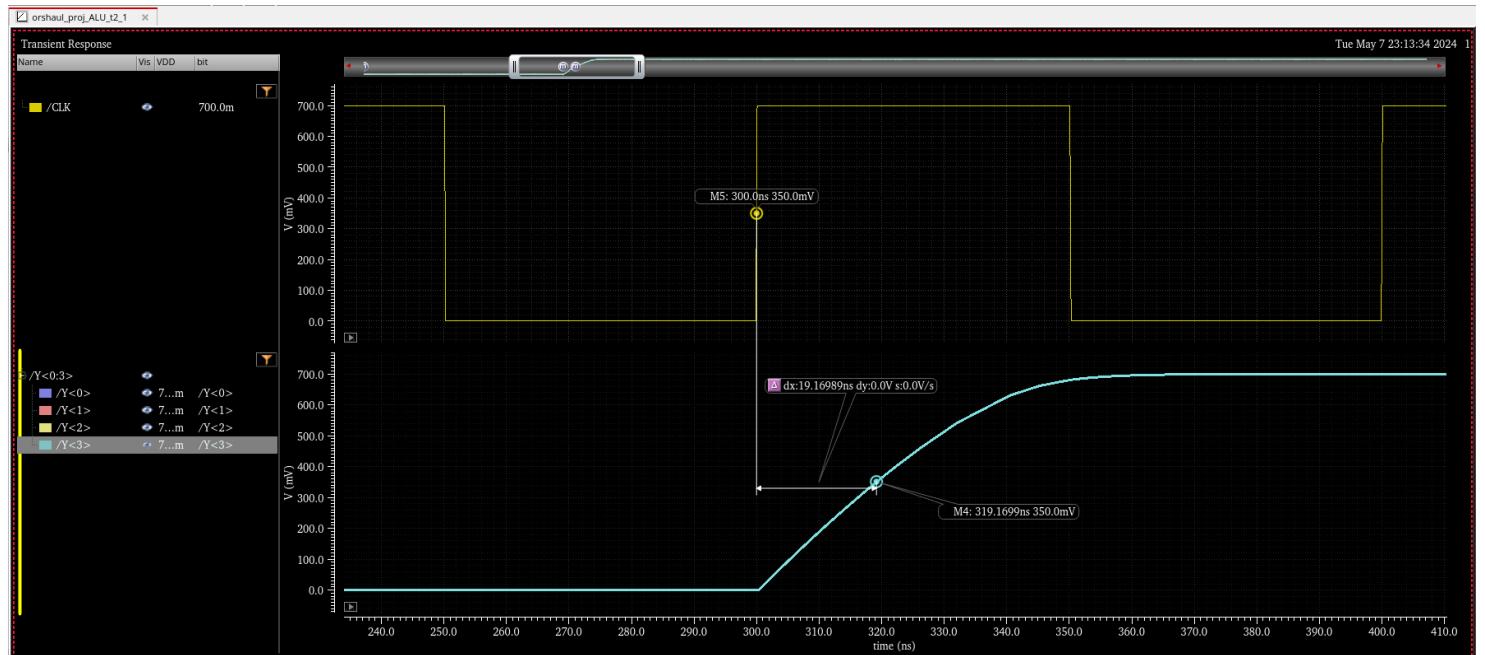
$$\text{המקסימלי נחשב על ידי הנוסחה: } f_{max} = \frac{1}{T_{min}}$$

עבור :  $VDD=1.2V$



годל הדלטא : 4.0887n [sec]

עבור :  $VDD=0.7V$



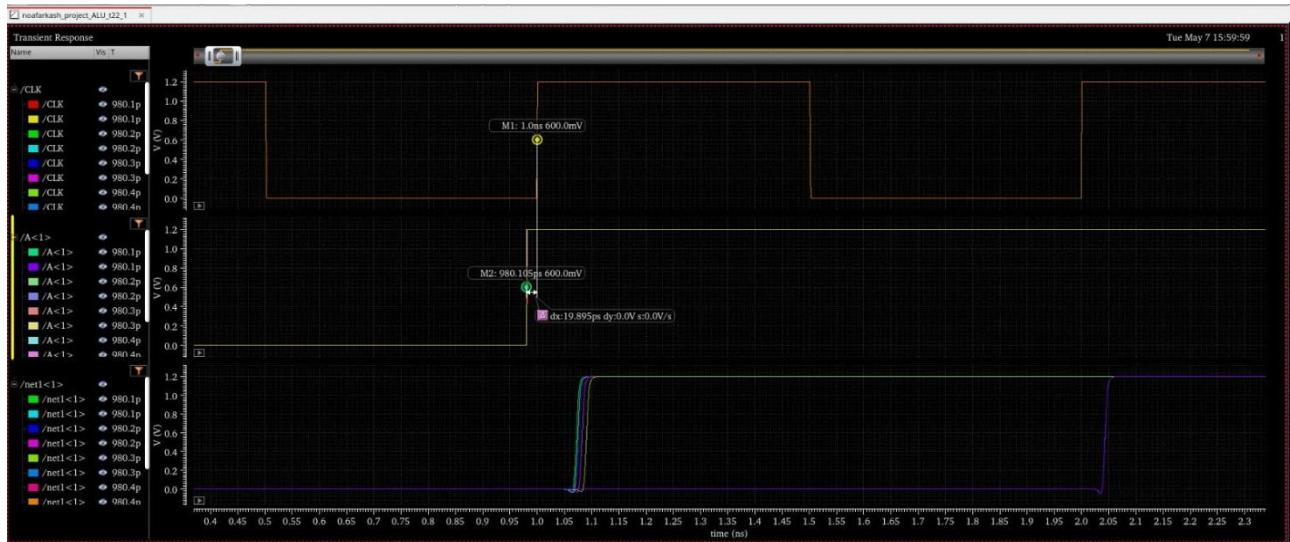
ניתן לראות שכעת הדלטא גדול כתוצאה מההפחפת מתח ההזנה וערךו בעת הוא : 19.16989n [sec]

זה נובע מכך שדחיפת הזרם במעגל ירידה כתוצאה מההפחפת מתח ההזנה.

נחשב את  $t_{setup}$

ערך זה חושב לפי רגיסטר של 4 ביטים מכיוון שהרגיסטרים (4/5 ביטים בנויים בצורה זהה ועובדים במקביל לכן נצפה לקבל ערך זהה לשני הרכיבים)

עבור  $VDD=1.2V$



годל הדלטה :  $19.895p [sec]$

עבור  $VDD=0.7V$



годל הדלטה :  $151.995p [sec]$

נסכם בטבלה:

$f_{max} [Hz]$	$T_{min} [sec]$	V[volt]
243.42 Mega	$4.088179n + 19.895p = 4.108074n$	<b>1.2V</b>
51.75 Mega	$19.16989n + 151.995p = 19.3221885n$	<b>0.7V</b>

## Critical path after QRC

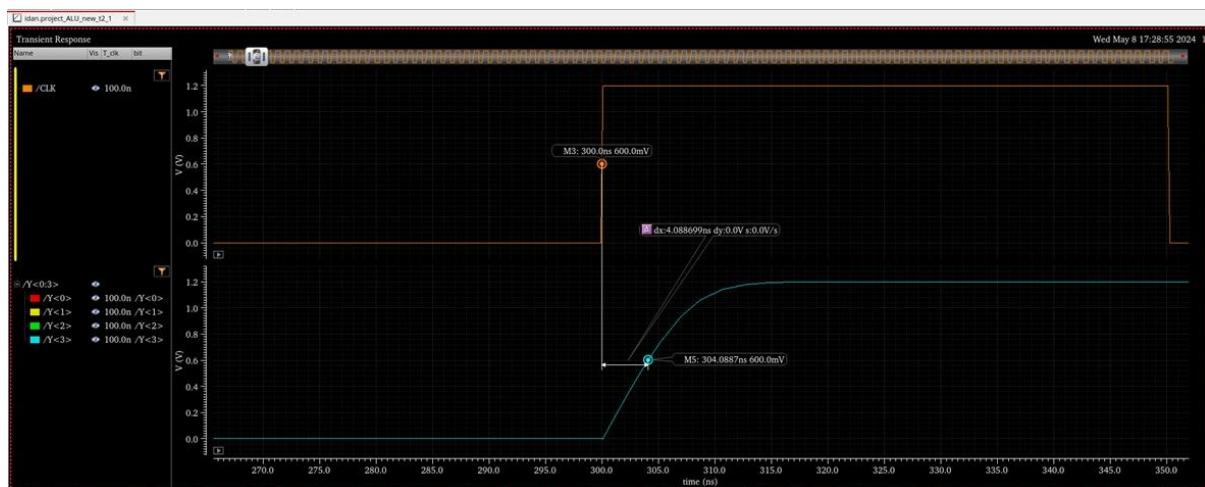
נציג כעת את הסימולציות לחישוב זמני ה- Critical Path  $t_{setup}$  והוא לאחר חילוץ הקיבולים הפרזיטיטים מהמעגל שמתבצע על ידי הרצת QRC ל- layout של מעגל ה- ALU

:QRC



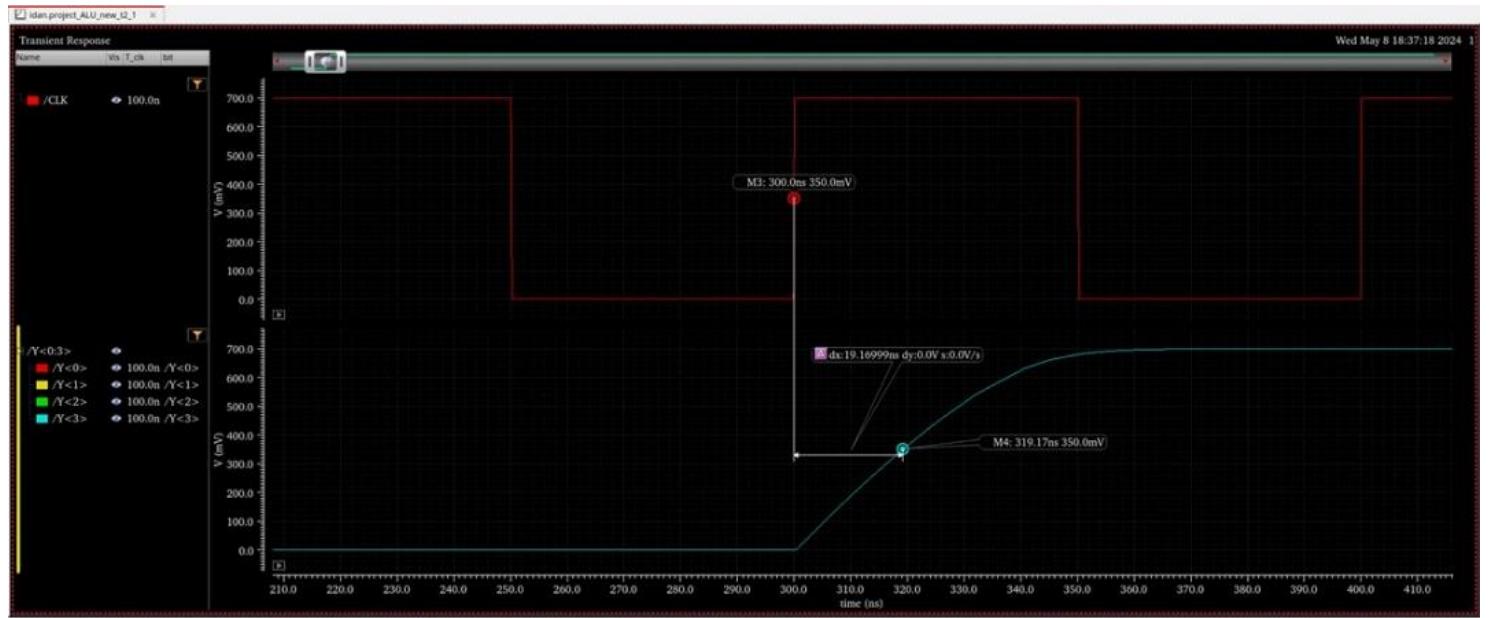
תחילת נחשב את האופן החישבונו לפני ה- QRC  $t_{cq} + t_{logic}$

: VDD=1.2V



גודל הדלטה : 4.0886n [sec]

עבור  $VDD=0.7V$



נימן לראות שבעת הדלתא גדל כתוצאה מהפחמת מתח ההזנה וערכו כעת הוא : 19.16999n [sec]

## נחשב את `t_setup`

עבור  $V_{DD} = 1.2V$



גודל הדلتא : 19.66167 p [sec]

עבור  $V_{DD}=0.7V$



גודל הדלטה:  $852.338 \text{ p [sec]}$

### נסכם בטבלה:

$f_{max} [\text{Hz}]$	$T_{min} [\text{sec}]$	V [volt]
243.411 Mega	$4.0886n+19.66167p=4.10826n$	<b>1.2V</b>
49.94 Mega	$19.16999n + 852.338p=20.02n$	<b>0.7V</b>

ניתן לראות שקיבלנו כי הזמןנים נשארו זהים לאחר ה-QRC בנויגוד למה שציפינו. ביצוע ה-QRC layout של המוגול ALU, מחלץ וモציא את הקיבולים הפרזיטיטים מהמוגול וכפי שלמדנו בקורס זה ומקורות מוגולים ספורתיים אלו יודעים שדבר זה אמרור להביא לירידה בזמןנים. הסיבה שהזמןנים אצלו נותרו זהים עד כדי שינוי זנitch קשורה לכל הנראה בתוכנה עצמה, אך חשוב לנו היה לפחות לציין זאת על מנת להראות לנו מבינים את משמעותות ה-QRC.