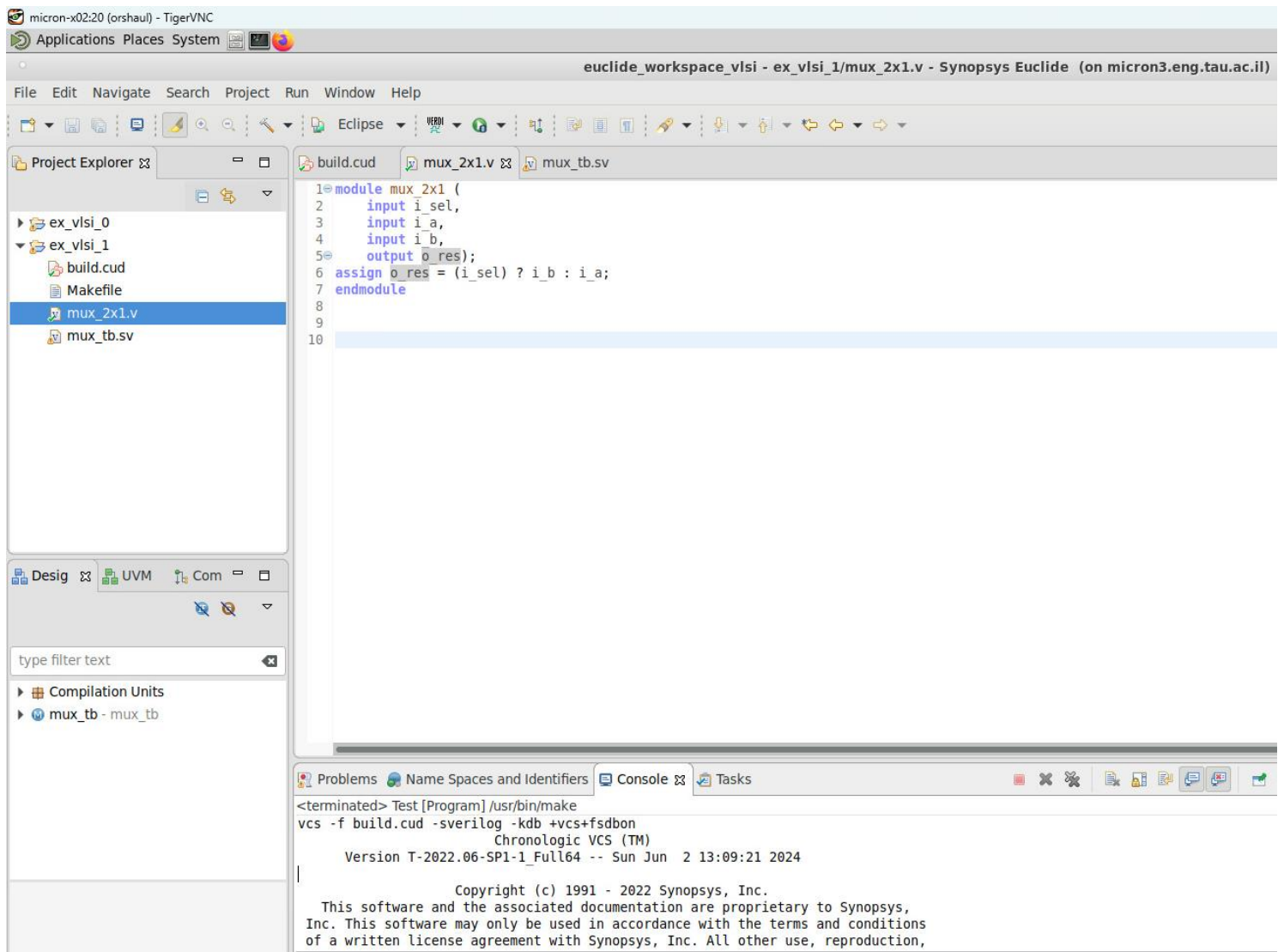


נחלק ל-8 מקרים של mux_2x1 ונוודא שקיבלנו ב-console ובגרפים (waveforms) את התוצאה הרצויה עבור o_res:

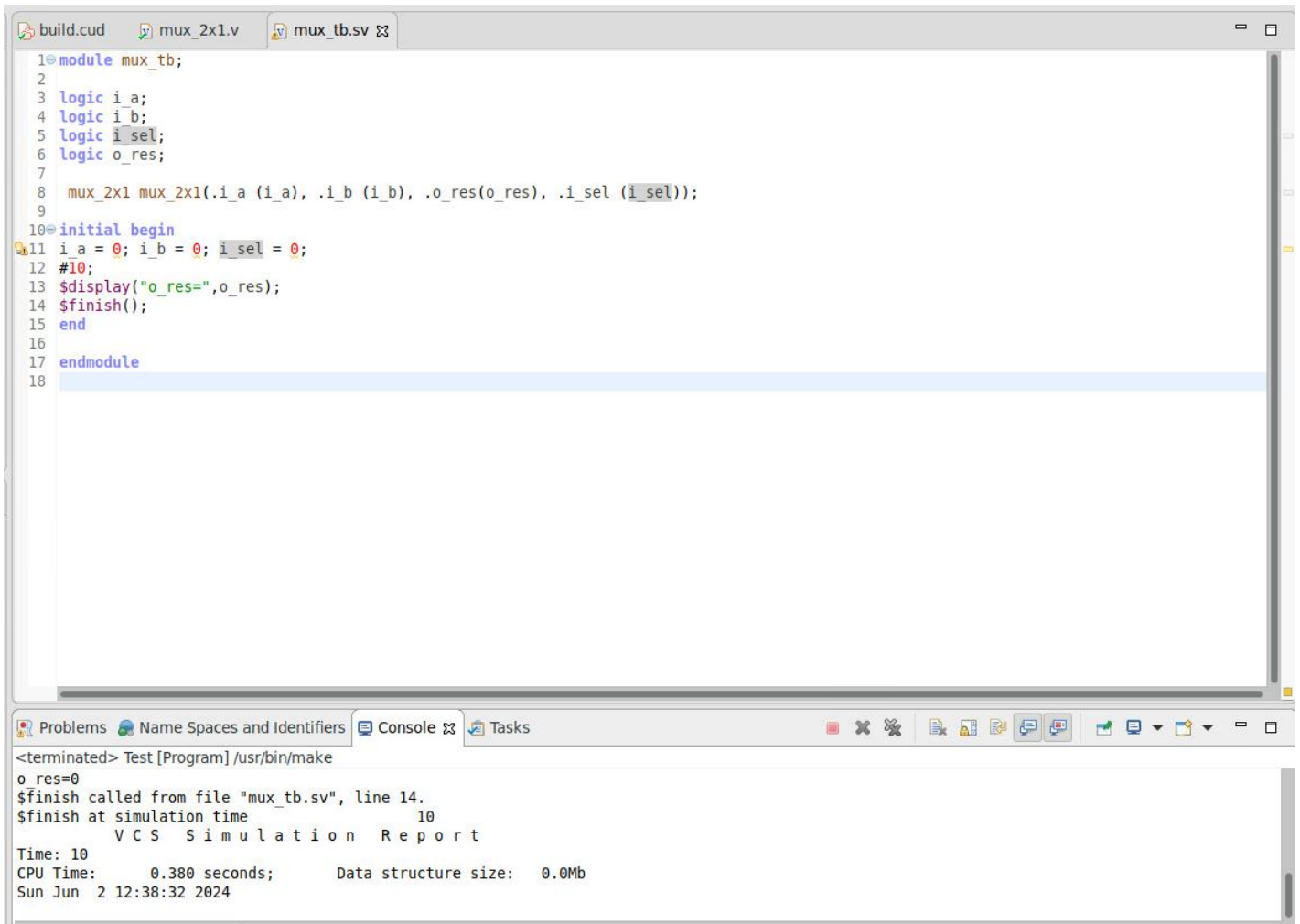
i_a	i_b	i_sel	o_res
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

הקוד עבור קובץ mux_2x1:



כעת נציג צילומי מסך של ה-testbench ונציג את תוצאות הסימולציה ואת הגרפים עבור 8 המקרים. ניתן לראות שעבור כל המקרים קיבלנו תוצאה רצויה ב-console עבור o_res, והגרפים מתקבלים כמצופה.

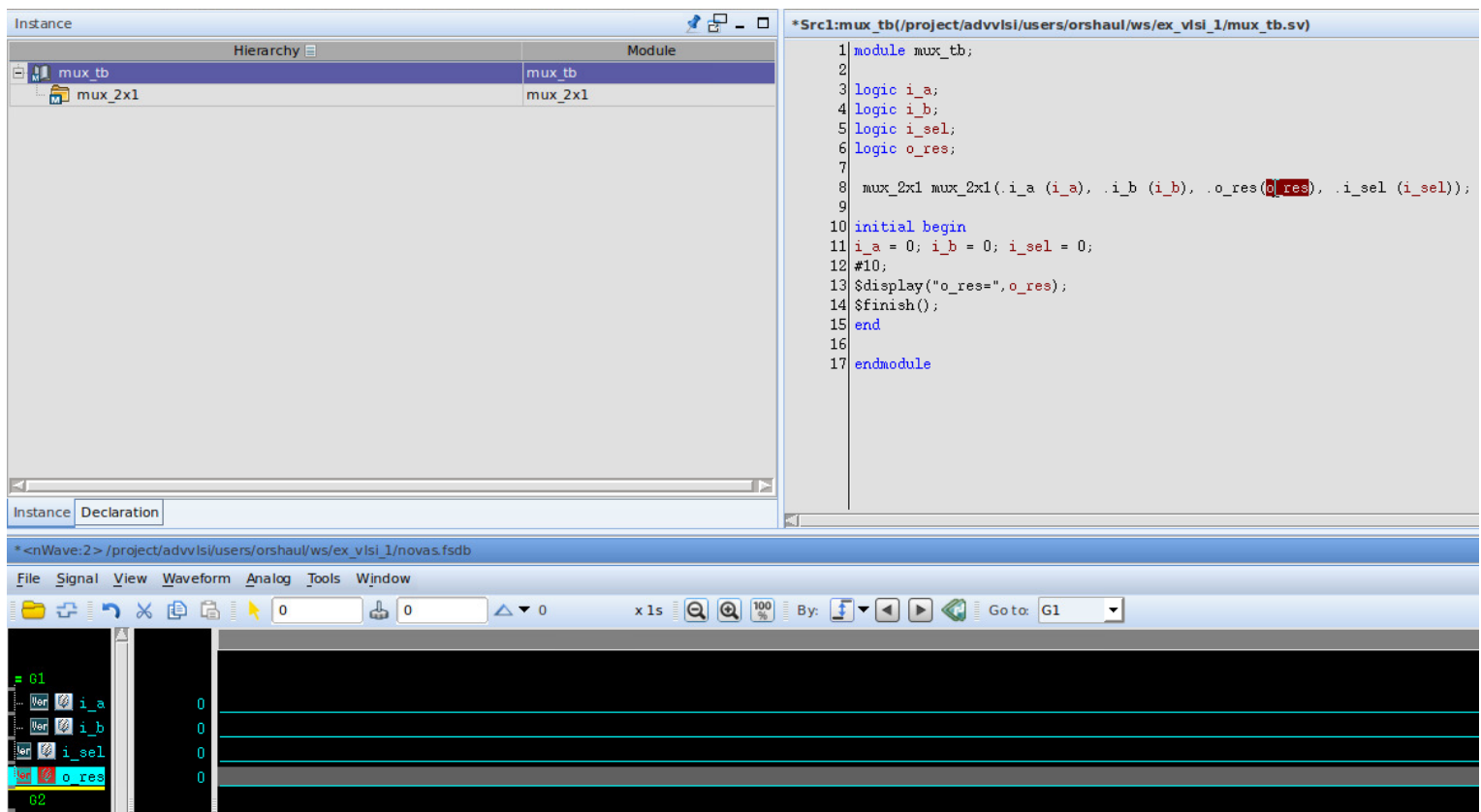
מקרה 1: $i_a=0, i_b=0, i_{sel}=0$



```
1 module mux_tb;
2
3   logic i_a;
4   logic i_b;
5   logic i_sel;
6   logic o_res;
7
8   mux_2x1 mux_2x1(.i_a(i_a), .i_b(i_b), .o_res(o_res), .i_sel(i_sel));
9
10 initial begin
11   i_a = 0; i_b = 0; i_sel = 0;
12   #10;
13   $display("o_res=", o_res);
14   $finish();
15 end
16
17 endmodule
18
```

Problems Name Spaces and Identifiers Console Tasks

<terminated> Test [Program] /usr/bin/make
o_res=0
\$finish called from file "mux_tb.v", line 14.
\$finish at simulation time 10
VCS Simulation Report
Time: 10
CPU Time: 0.380 seconds; Data structure size: 0.0Mb
Sun Jun 2 12:38:32 2024



Instance Hierarchy Module

Instance	Module
mux_tb	mux_tb
mux_2x1	mux_2x1

*Src1:mux_tb(/project/advvlsi/users/orshaul/ws/ex_vlsi_1/mux_tb.v)

```
1 module mux_tb;
2
3   logic i_a;
4   logic i_b;
5   logic i_sel;
6   logic o_res;
7
8   mux_2x1 mux_2x1(.i_a(i_a), .i_b(i_b), .o_res(o_res), .i_sel(i_sel));
9
10 initial begin
11   i_a = 0; i_b = 0; i_sel = 0;
12   #10;
13   $display("o_res=", o_res);
14   $finish();
15 end
16
17 endmodule
```

*<nWave:2> /project/advvlsi/users/orshaul/ws/ex_vlsi_1/novas.fsd

File Signal View Waveform Analog Tools Window

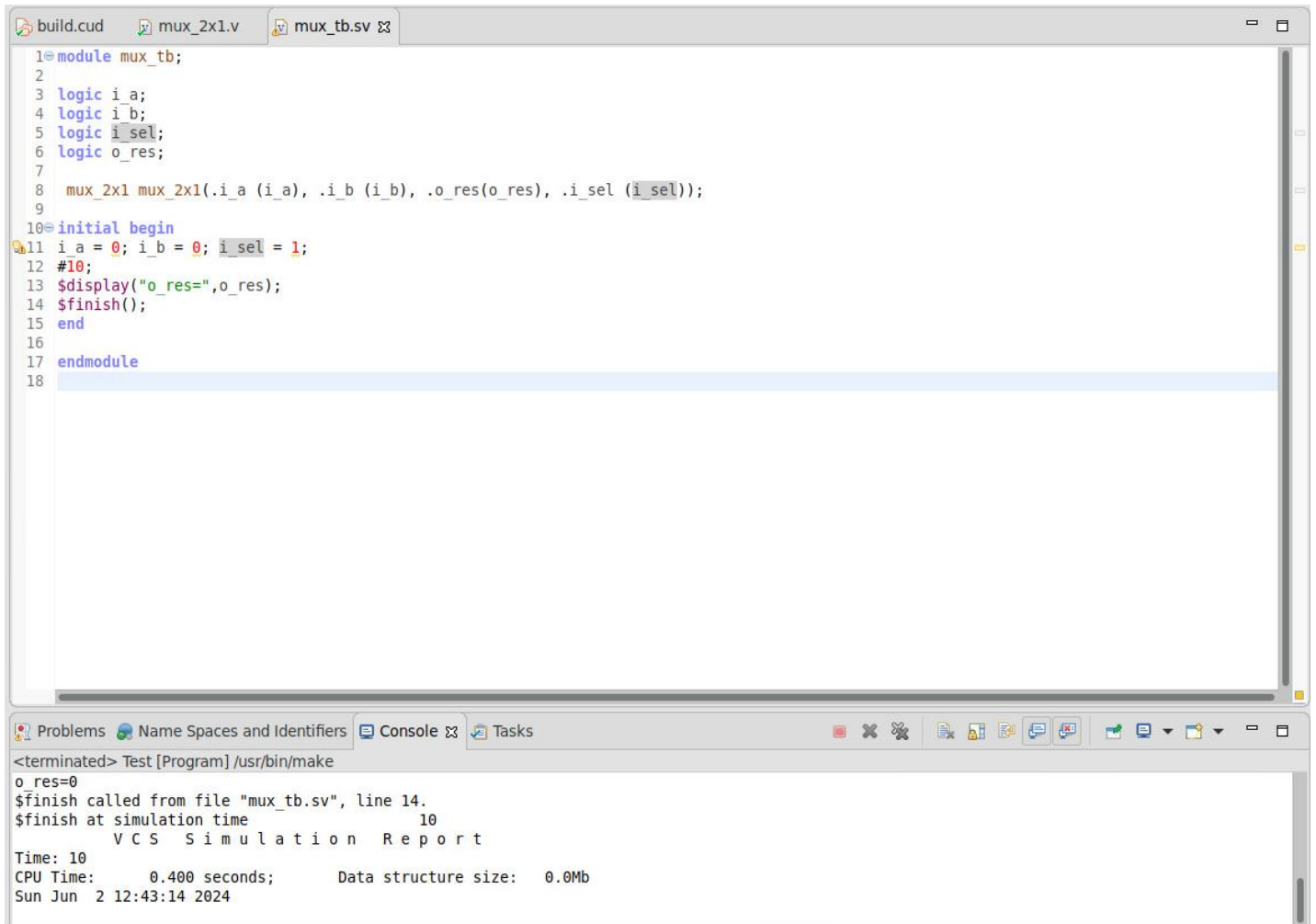
0 0 0 x 1s 100% By: f Go to: G1

01

Signal	Value
i_a	0
i_b	0
i_sel	0
o_res	0

02

מקרה 2: $i_a=0, i_b=0, i_{sel}=1$

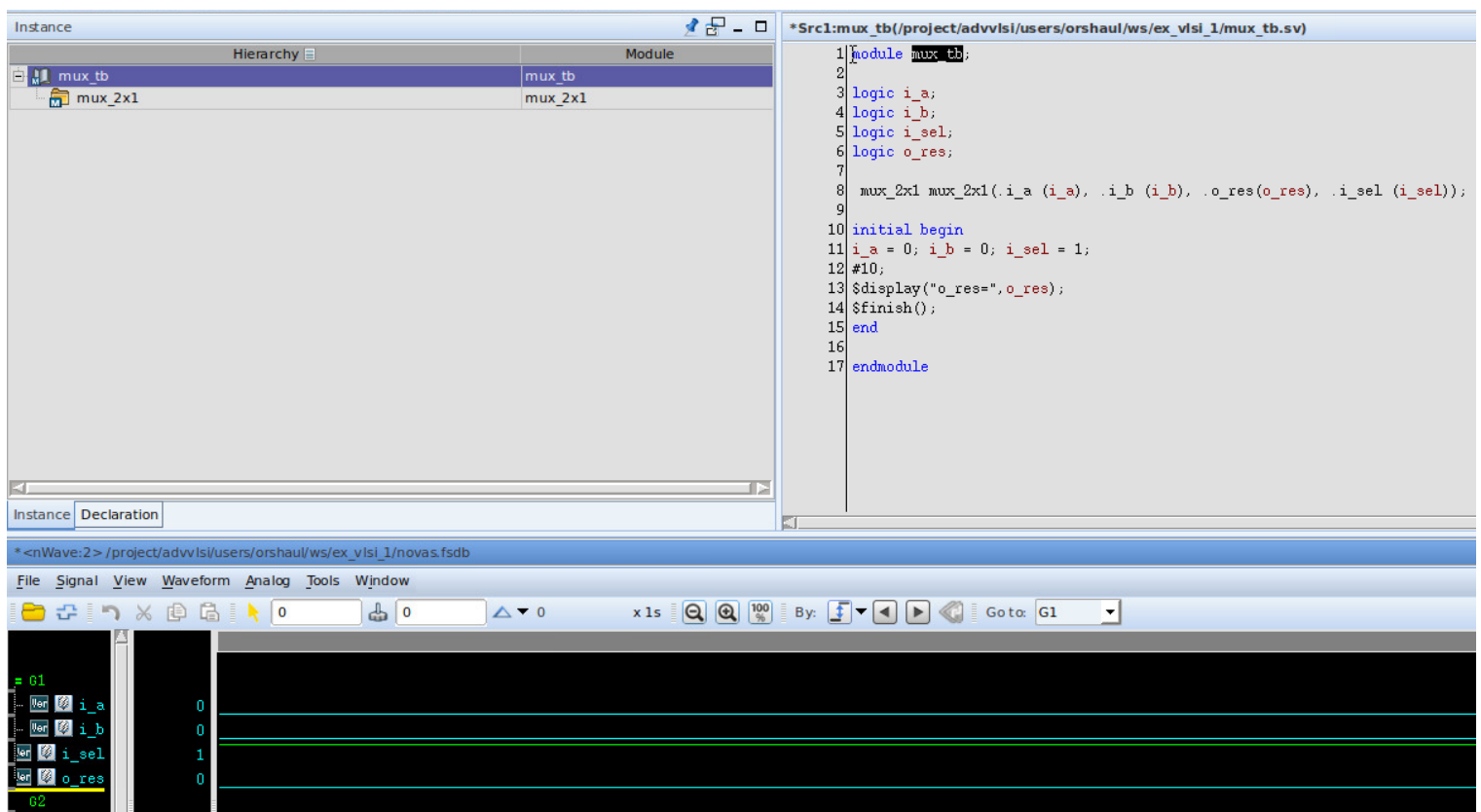


The screenshot shows a Verilog IDE with two tabs: `build.cud` and `mux_2x1.v`. The main editor displays the testbench code for `mux_tb`. Below the code, the `Console` window shows the simulation output, indicating that the simulation completed successfully at 10 time units.

```
1 module mux_tb;
2
3 logic i_a;
4 logic i_b;
5 logic i_sel;
6 logic o_res;
7
8 mux_2x1 mux_2x1(.i_a(i_a), .i_b(i_b), .o_res(o_res), .i_sel(i_sel));
9
10 initial begin
11 i_a = 0; i_b = 0; i_sel = 1;
12 #10;
13 $display("o_res=", o_res);
14 $finish();
15 end
16
17 endmodule
18
```

Console Output:

```
<terminated> Test [Program] /usr/bin/make
o_res=0
$finish called from file "mux_tb.sv", line 14.
$finish at simulation time 10
VCS Simulation Report
Time: 10
CPU Time: 0.400 seconds; Data structure size: 0.0Mb
Sun Jun 2 12:43:14 2024
```



The screenshot shows a logic analyzer interface. The `Hierarchy` window displays the module structure, with `mux_tb` and `mux_2x1` listed. The `Waveform` window shows the signals `i_a`, `i_b`, `i_sel`, and `o_res` over time. The `Signal` window shows the values of these signals at the current time step.

Hierarchy:

Instance	Module
mux_tb	mux_tb
mux_2x1	mux_2x1

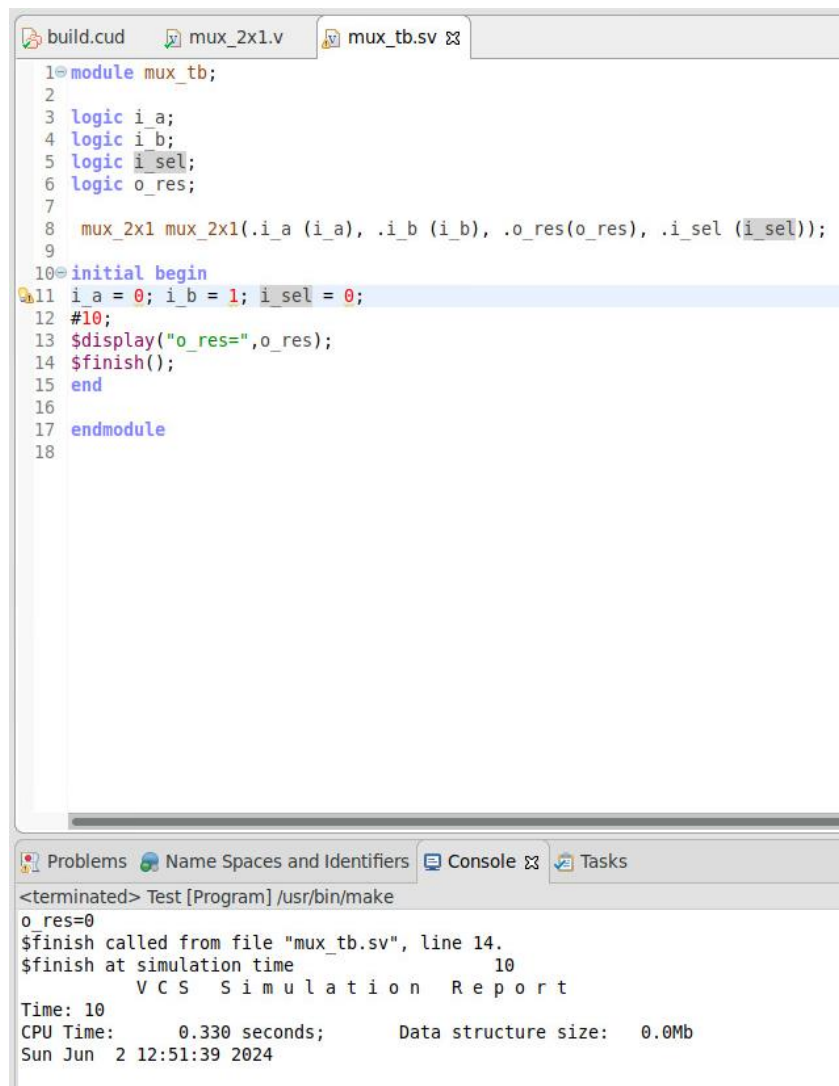
Waveform:

Signal	Value
i_a	0
i_b	0
i_sel	1
o_res	0

Signal Values:

Signal	Value
i_a	0
i_b	0
i_sel	1
o_res	0

מקרה 3: $i_a=0, i_b=1, i_{sel}=0$

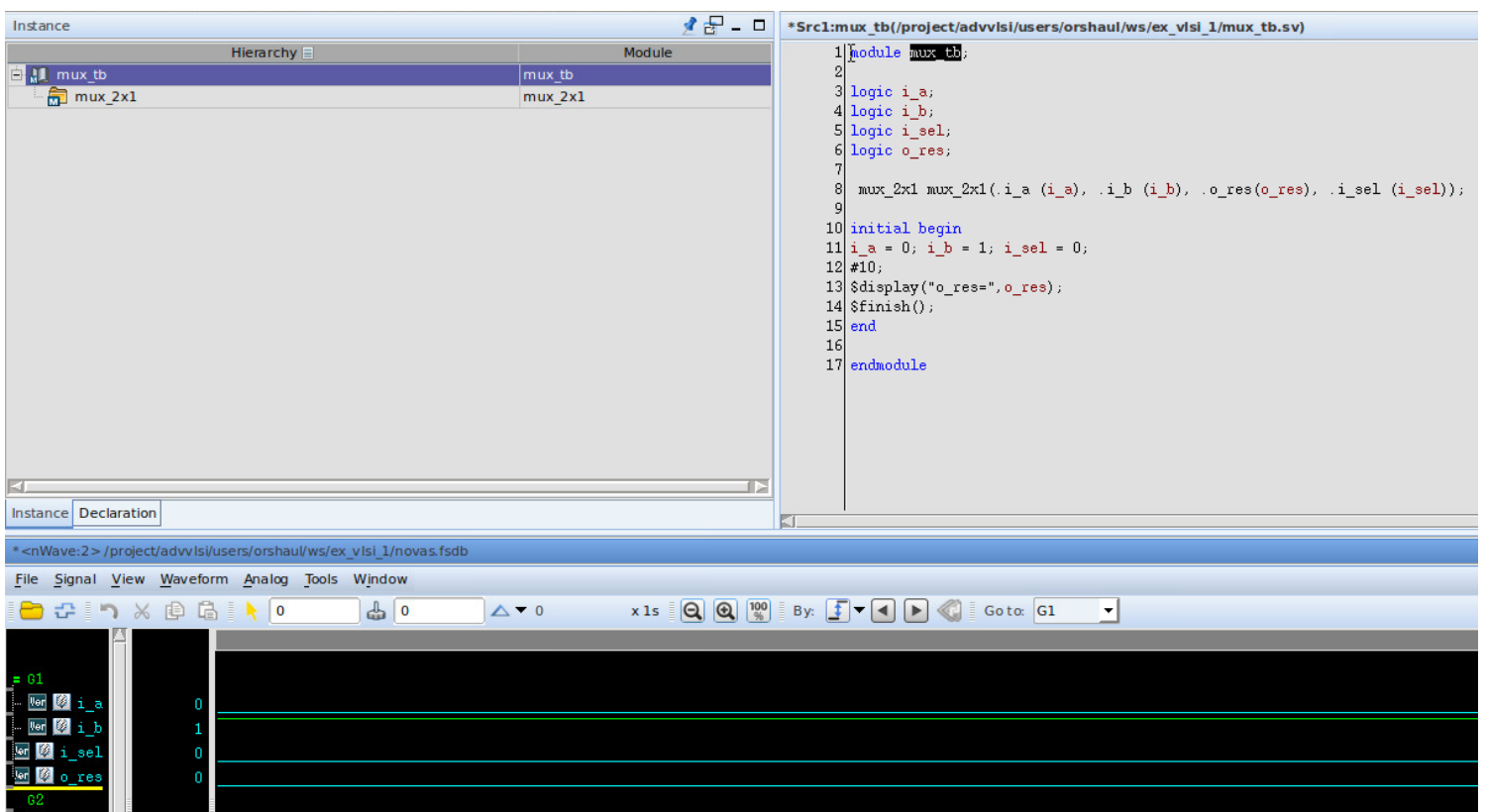


The screenshot shows a Verilog code editor with three tabs: `build.cud`, `mux_2x1.v`, and `mux_tb.v`. The `mux_tb.v` tab is active, displaying the following code:

```
1 module mux_tb;
2
3 logic i_a;
4 logic i_b;
5 logic i_sel;
6 logic o_res;
7
8 mux_2x1 mux_2x1(.i_a(i_a), .i_b(i_b), .o_res(o_res), .i_sel(i_sel));
9
10 initial begin
11 i_a = 0; i_b = 1; i_sel = 0;
12 #10;
13 $display("o_res=", o_res);
14 $finish();
15 end
16
17 endmodule
18
```

Below the code editor, the `Console` tab is active, showing the output of the simulation:

```
<terminated> Test [Program] /usr/bin/make
o_res=0
$finish called from file "mux_tb.v", line 14.
$finish at simulation time 10
VCS Simulation Report
Time: 10
CPU Time: 0.330 seconds; Data structure size: 0.0Mb
Sun Jun 2 12:51:39 2024
```



מקרה 4: $i_a=0, i_b=1, i_{sel}=1$

```
build.cud  mux_2x1.v  mux_tb.sv 3
1 module mux_tb;
2
3 logic i_a;
4 logic i_b;
5 logic i_sel;
6 logic o_res;
7
8 mux_2x1 mux_2x1(.i_a(i_a), .i_b(i_b), .o_res(o_res), .i_sel(i_sel));
9
10 initial begin
11 i_a = 0; i_b = 1; i_sel = 1;
12 #10;
13 $display("o_res=", o_res);
14 $finish();
15 end
16
17 endmodule
18
```

Problems Name Spaces and Identifiers Console Tasks

<terminated> Test [Program] /usr/bin/make
o_res=1
\$finish called from file "mux_tb.sv", line 14.
\$finish at simulation time 10
VCS Simulation Report
Time: 10
CPU Time: 0.340 seconds; Data structure size: 0.0Mb
Sun Jun 2 12:56:47 2024

Instance

Hierarchy	Module
mux_tb	mux_tb
mux_2x1	mux_2x1

*Src1:mux_tb(/project/advvlsi/users/orshaul/ws/ex_vlsi_1/mux_tb.sv)

```
1 module mux_tb;
2
3 logic i_a;
4 logic i_b;
5 logic i_sel;
6 logic o_res;
7
8 mux_2x1 mux_2x1(.i_a(i_a), .i_b(i_b), .o_res(o_res), .i_sel(i_sel));
9
10 initial begin
11 i_a = 0; i_b = 1; i_sel = 1;
12 #10;
13 $display("o_res=", o_res);
14 $finish();
15 end
16
17 endmodule
```

*<nWave:2> /project/advvlsi/users/orshaul/ws/ex_vlsi_1/novas.fsdb

File Signal View Waveform Analog Tools Window

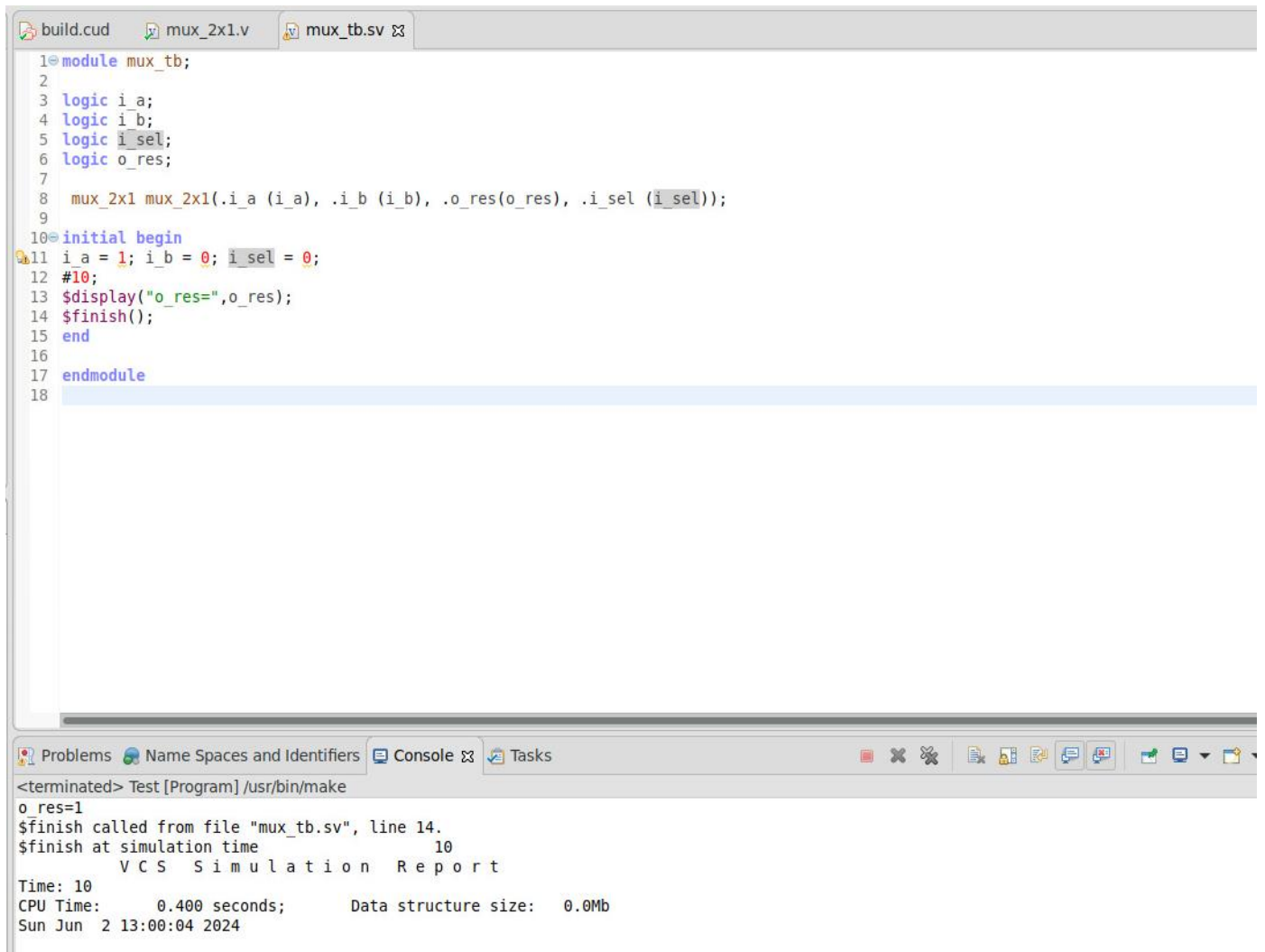
x1s 0 0 0 100% By: Goto: G1

01

Ver	0
i_a	0
i_b	1
i_sel	1
o_res	1

02

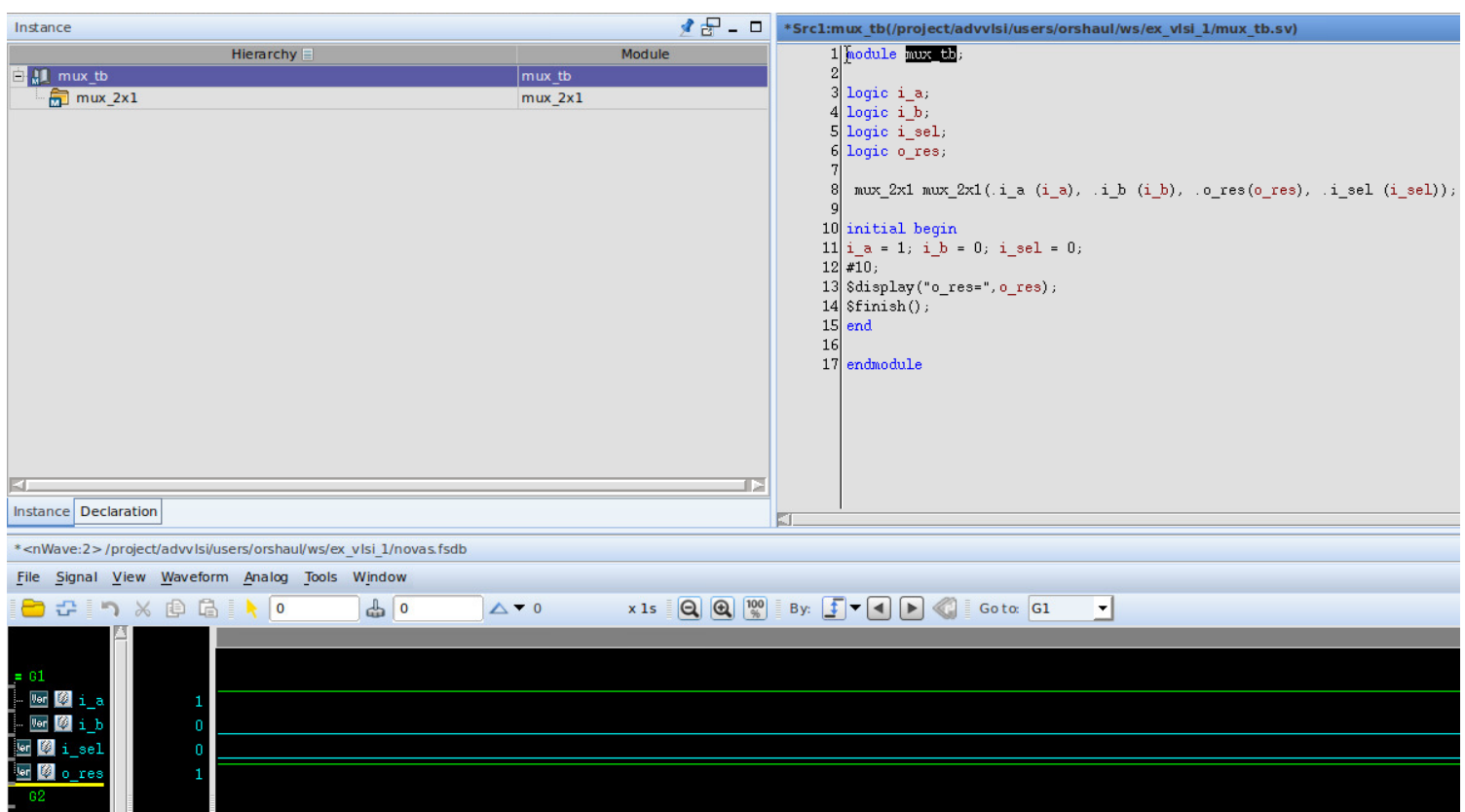
מקרה 5: $i_a=1, i_b=0, i_{sel}=0$



```
1 module mux_tb;
2
3 logic i_a;
4 logic i_b;
5 logic i_sel;
6 logic o_res;
7
8 mux_2x1 mux_2x1(.i_a(i_a), .i_b(i_b), .o_res(o_res), .i_sel(i_sel));
9
10 initial begin
11 i_a = 1; i_b = 0; i_sel = 0;
12 #10;
13 $display("o_res=", o_res);
14 $finish();
15 end
16
17 endmodule
18
```

Problems Name Spaces and Identifiers Console Tasks

<terminated> Test [Program] /usr/bin/make
o_res=1
\$finish called from file "mux_tb.v", line 14.
\$finish at simulation time 10
VCS Simulation Report
Time: 10
CPU Time: 0.400 seconds; Data structure size: 0.0Mb
Sun Jun 2 13:00:04 2024



מקרה 6: $i_a=1, i_b=0, i_{sel}=1$

```
build.cud mux_2x1.v mux_tb.sv
1 module mux_tb;
2
3 logic i_a;
4 logic i_b;
5 logic i_sel;
6 logic o_res;
7
8 mux_2x1 mux_2x1(.i_a(i_a), .i_b(i_b), .o_res(o_res), .i_sel(i_sel));
9
10 initial begin
11 i_a = 1; i_b = 0; i_sel = 1;
12 #10;
13 $display("o_res=", o_res);
14 $finish();
15 end
16
17 endmodule
18
```

Problems Name Spaces and Identifiers Console Tasks

<terminated> Test [Program] /usr/bin/make
o_res=0
\$finish called from file "mux_tb.sv", line 14.
\$finish at simulation time 10
VCS Simulation Report
Time: 10
CPU Time: 0.370 seconds; Data structure size: 0.0Mb
Sun Jun 2 13:02:39 2024

Instance Hierarchy Module

Instance	Module
mux_tb	mux_tb
mux_2x1	mux_2x1

*Src1: mux_tb(/project/advvlsi/users/orshaul/ws/ex_vlsi_1/mux_tb.sv)

```
1 module mux_tb;
2
3 logic i_a;
4 logic i_b;
5 logic i_sel;
6 logic o_res;
7
8 mux_2x1 mux_2x1(.i_a(i_a), .i_b(i_b), .o_res(o_res), .i_sel(i_sel));
9
10 initial begin
11 i_a = 1; i_b = 0; i_sel = 1;
12 #10;
13 $display("o_res=", o_res);
14 $finish();
15 end
16
17 endmodule
```

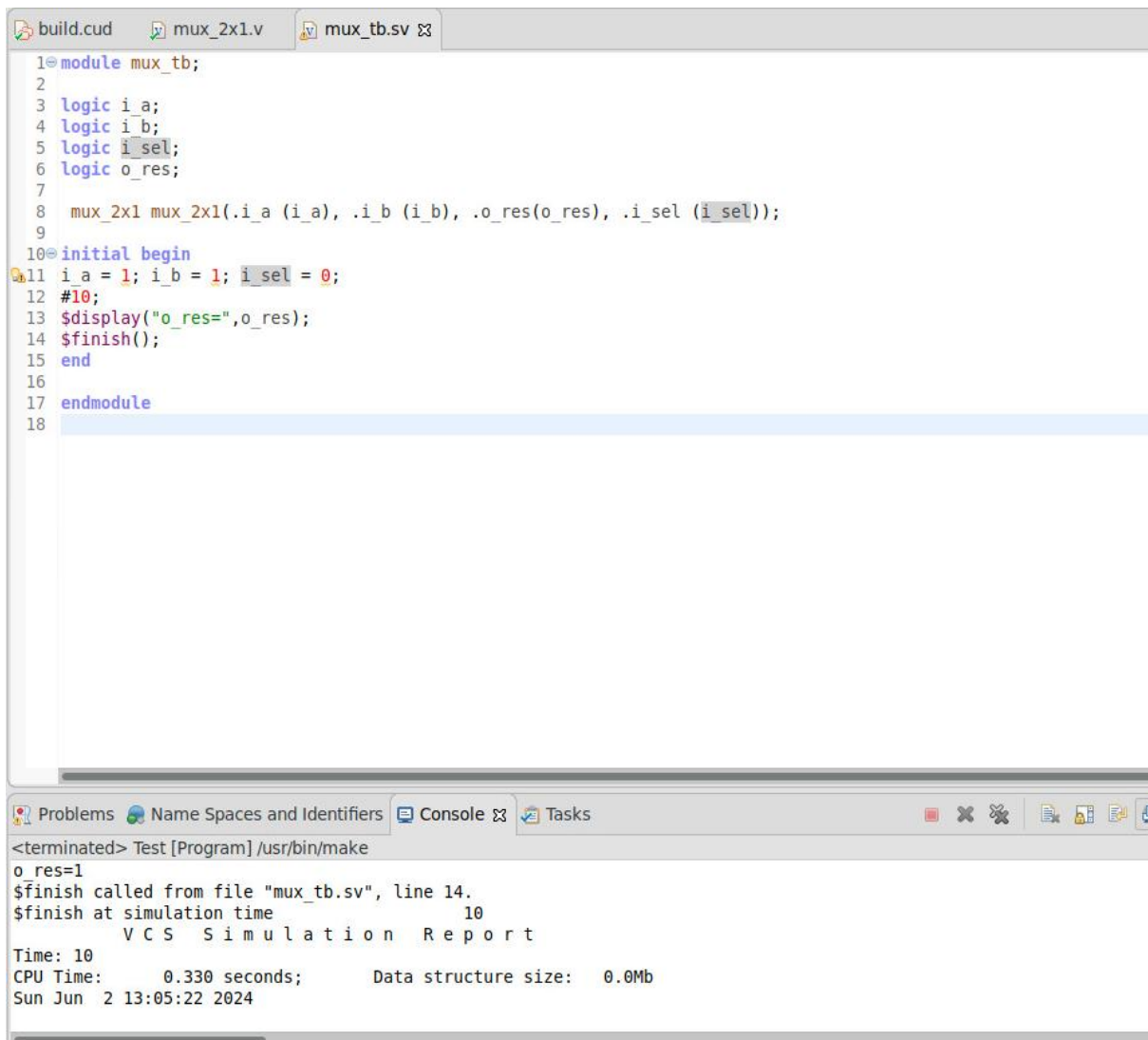
*<nWave:2> /project/advvlsi/users/orshaul/ws/ex_vlsi_1/novas.fsd

File Signal View Waveform Analog Tools Window

0 0 x 1s 100% By: f Goto: G1

01 i_a 1
01 i_b 0
01 i_sel 1
01 o_res 0

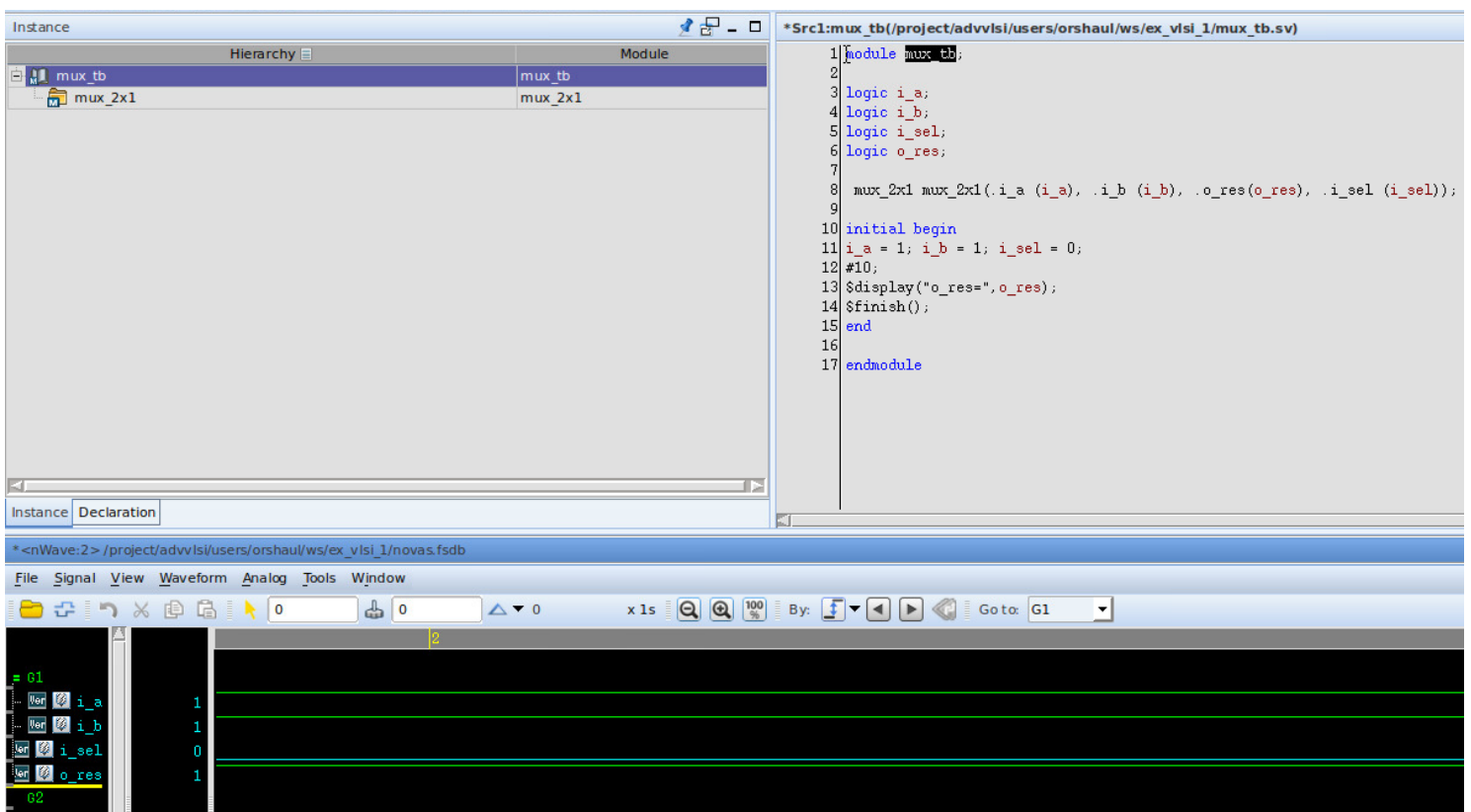
מקרה 7: $i_a=1, i_b=1, i_{sel}=0$



```
1 module mux_tb;
2
3 logic i_a;
4 logic i_b;
5 logic i_sel;
6 logic o_res;
7
8 mux_2x1 mux_2x1(.i_a(i_a), .i_b(i_b), .o_res(o_res), .i_sel(i_sel));
9
10 initial begin
11 i_a = 1; i_b = 1; i_sel = 0;
12 #10;
13 $display("o_res=", o_res);
14 $finish();
15 end
16
17 endmodule
18
```

Problems Name Spaces and Identifiers Console Tasks

<terminated> Test [Program] /usr/bin/make
o_res=1
\$finish called from file "mux_tb.sv", line 14.
\$finish at simulation time 10
VCS Simulation Report
Time: 10
CPU Time: 0.330 seconds; Data structure size: 0.0Mb
Sun Jun 2 13:05:22 2024



Instance Hierarchy Module

Instance	Module
mux_tb	mux_tb
mux_2x1	mux_2x1

*Src1:mux_tb(/project/advvlsi/users/orshaul/ws/ex_vlsi_1/mux_tb.sv)

```
1 module mux_tb;
2
3 logic i_a;
4 logic i_b;
5 logic i_sel;
6 logic o_res;
7
8 mux_2x1 mux_2x1(.i_a(i_a), .i_b(i_b), .o_res(o_res), .i_sel(i_sel));
9
10 initial begin
11 i_a = 1; i_b = 1; i_sel = 0;
12 #10;
13 $display("o_res=", o_res);
14 $finish();
15 end
16
17 endmodule
```

*<nWave:2> /project/advvlsi/users/orshaul/ws/ex_vlsi_1/novas.fsdb

File Signal View Waveform Analog Tools Window

0 0 0 x 1s 100% By: G1

Waveform:

Signal	Value
i_a	1
i_b	1
i_sel	0
o_res	1

מקרה 8: $i_a=1, i_b=1, i_{sel}=1$

```
build.cud  mux_2x1.v  mux_tb.sv 3
1 module mux_tb;
2
3 logic i_a;
4 logic i_b;
5 logic i_sel;
6 logic o_res;
7
8 mux_2x1 mux_2x1(.i_a (i_a), .i_b (i_b), .o_res(o_res), .i_sel (i_sel));
9
10 initial begin
11 i_a = 1; i_b = 1; i_sel = 1;
12 #10;
13 $display("o_res=", o_res);
14 $finish();
15 end
16
17 endmodule
18
```

Problems Name Spaces and Identifiers Console Tasks

<terminated> Test [Program] /usr/bin/make
o_res=1
\$finish called from file "mux_tb.sv", line 14.
\$finish at simulation time 10
VCS Simulation Report
Time: 10
CPU Time: 0.340 seconds; Data structure size: 0.0Mb
Sun Jun 2 13:09:22 2024

Instance

Hierarchy	Module
mux_tb	mux_tb
mux_2x1	mux_2x1

Instance Declaration

```
*Src1: mux_tb(/project/advvlsi/users/orshaul/ws/ex_vlsi_1/mux_tb.sv)
1 module mux_tb;
2
3 logic i_a;
4 logic i_b;
5 logic i_sel;
6 logic o_res;
7
8 mux_2x1 mux_2x1(.i_a (i_a), .i_b (i_b), .o_res(o_res), .i_sel (i_sel));
9
10 initial begin
11 i_a = 1; i_b = 1; i_sel = 1;
12 #10;
13 $display("o_res=", o_res);
14 $finish();
15 end
16
17 endmodule
```

*<nWave:2> /project/advvlsi/users/orshaul/ws/ex_vlsi_1/novas.fsdb

File Signal View Waveform Analog Tools Window

0 0 0 x 1s 100% By: Go to: G1

G1

Signal	Value
i_a	1
i_b	1
i_sel	1
o_res	1

G2