Name: Thasin abedin

ID : 160021139

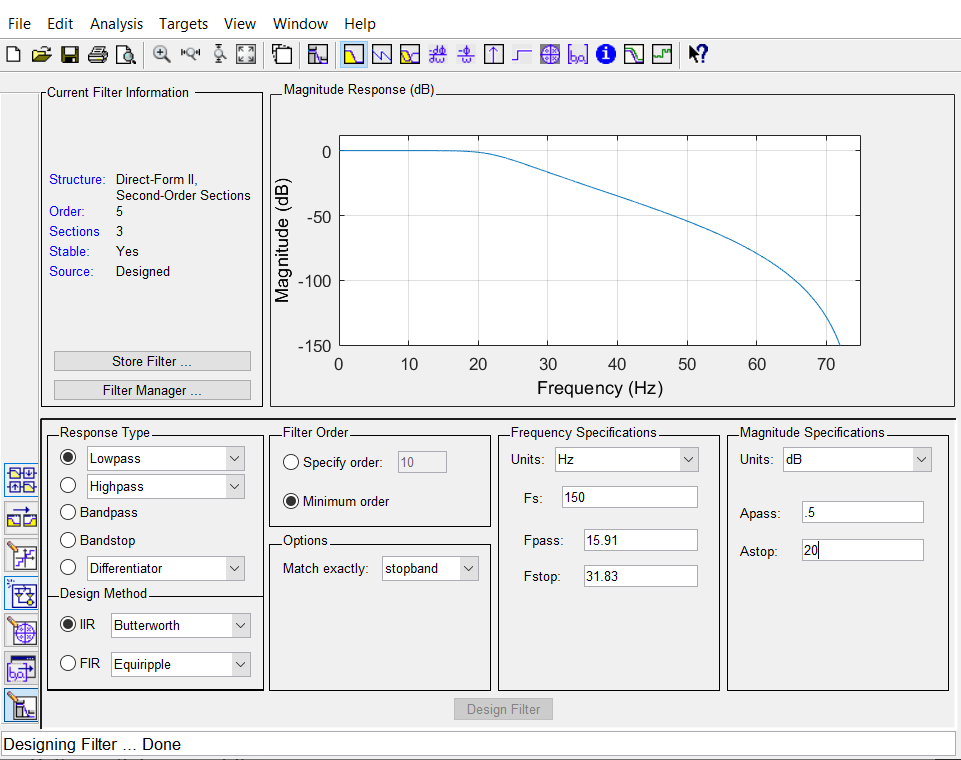
Section : c

Group: c2

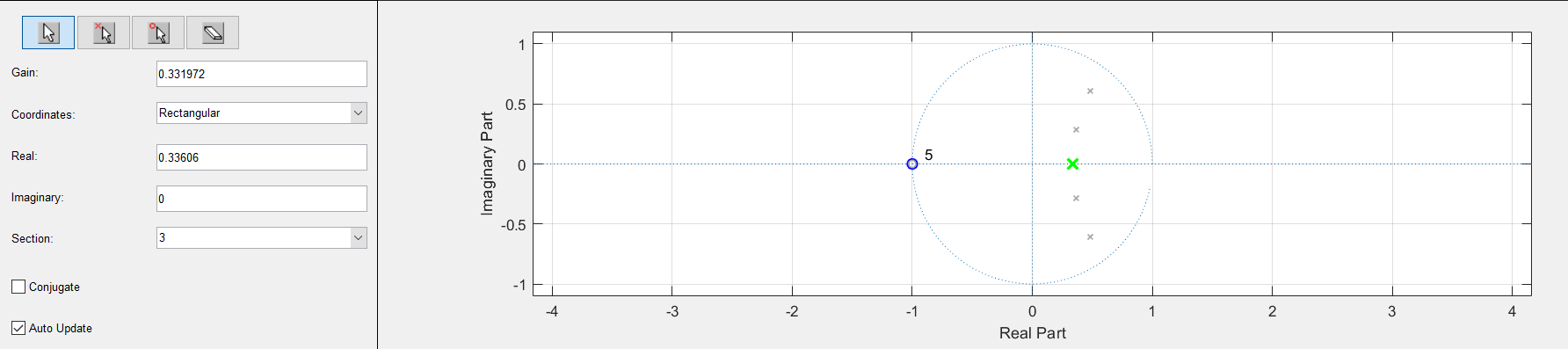
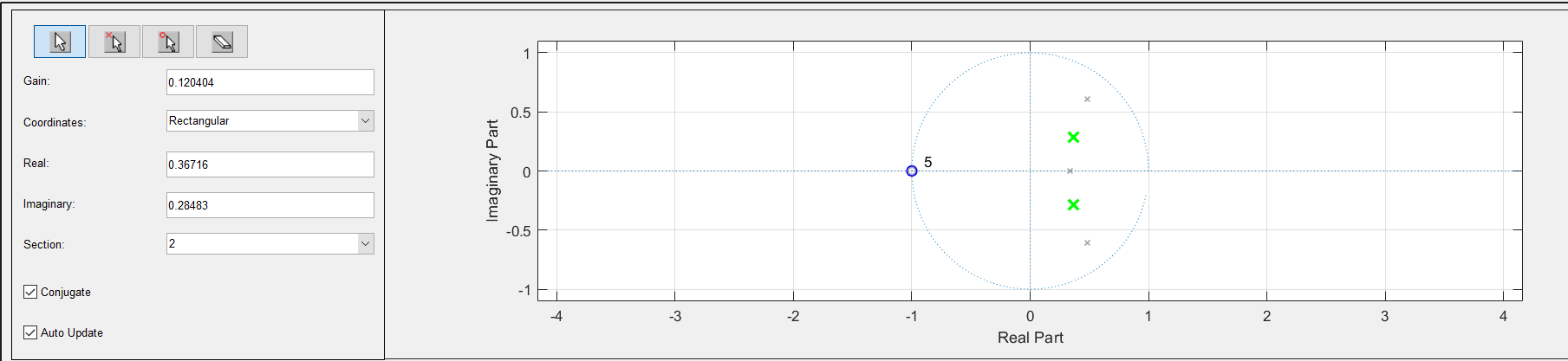
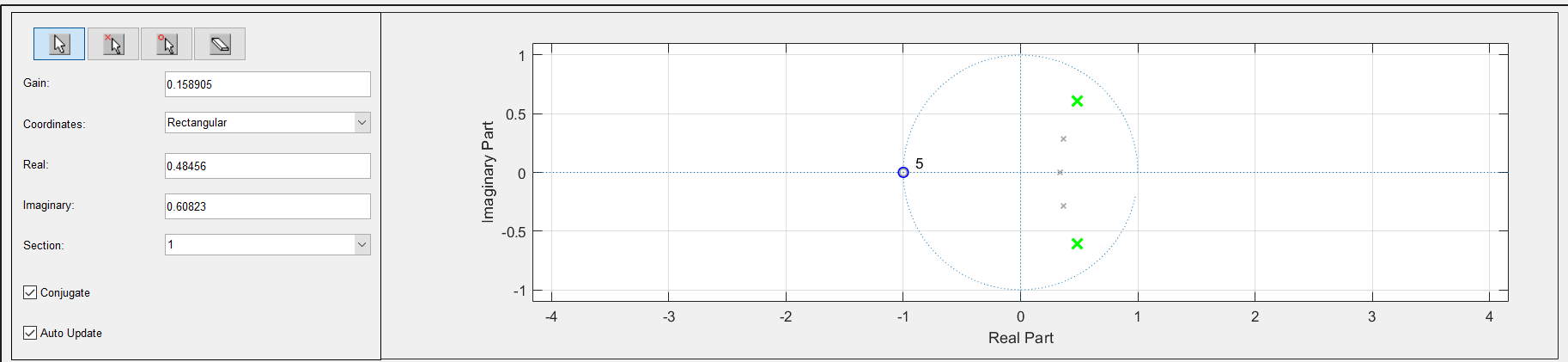
DIGITAL FILTER DESIGN LAB

EXP NO. : 2

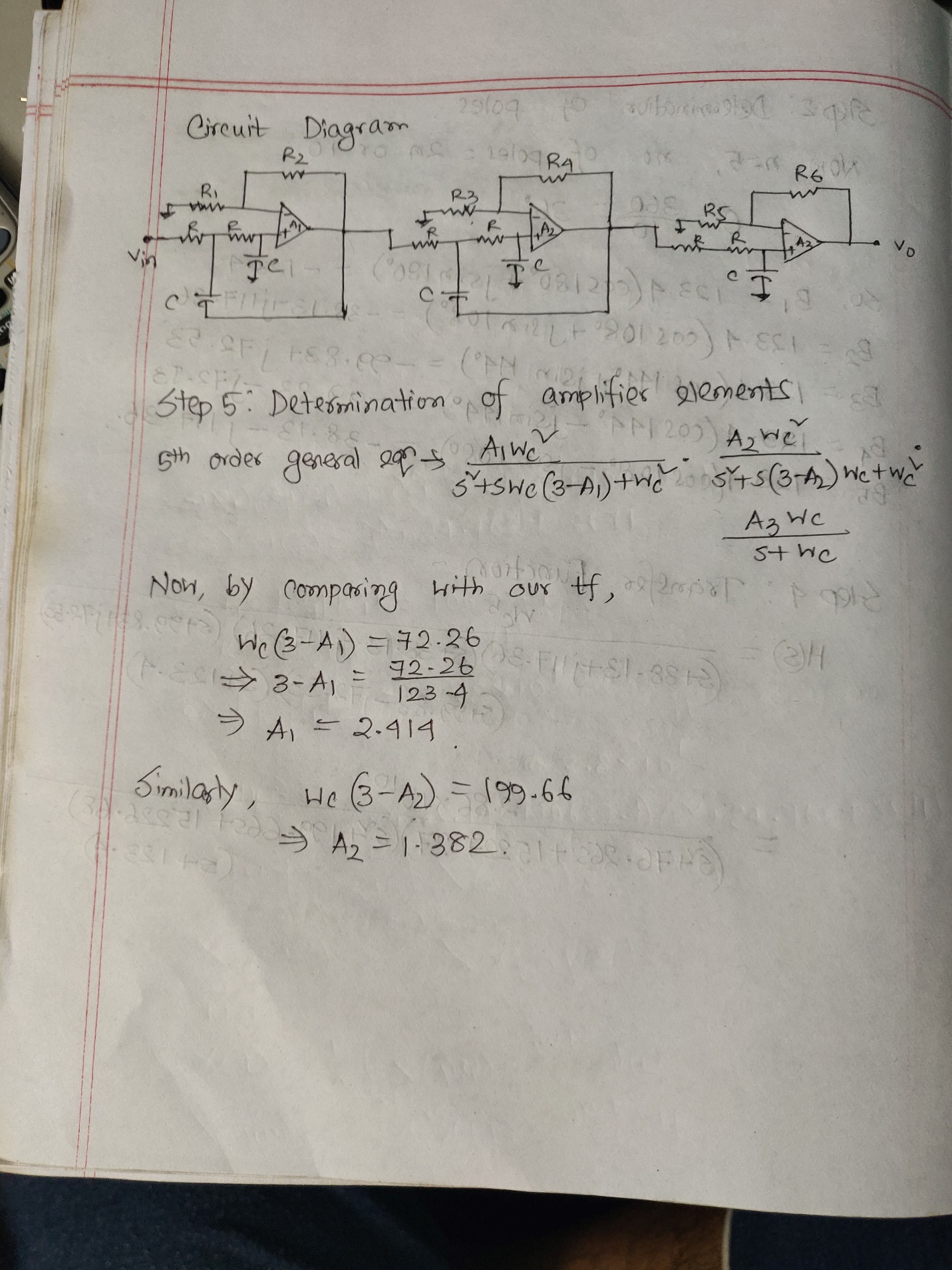
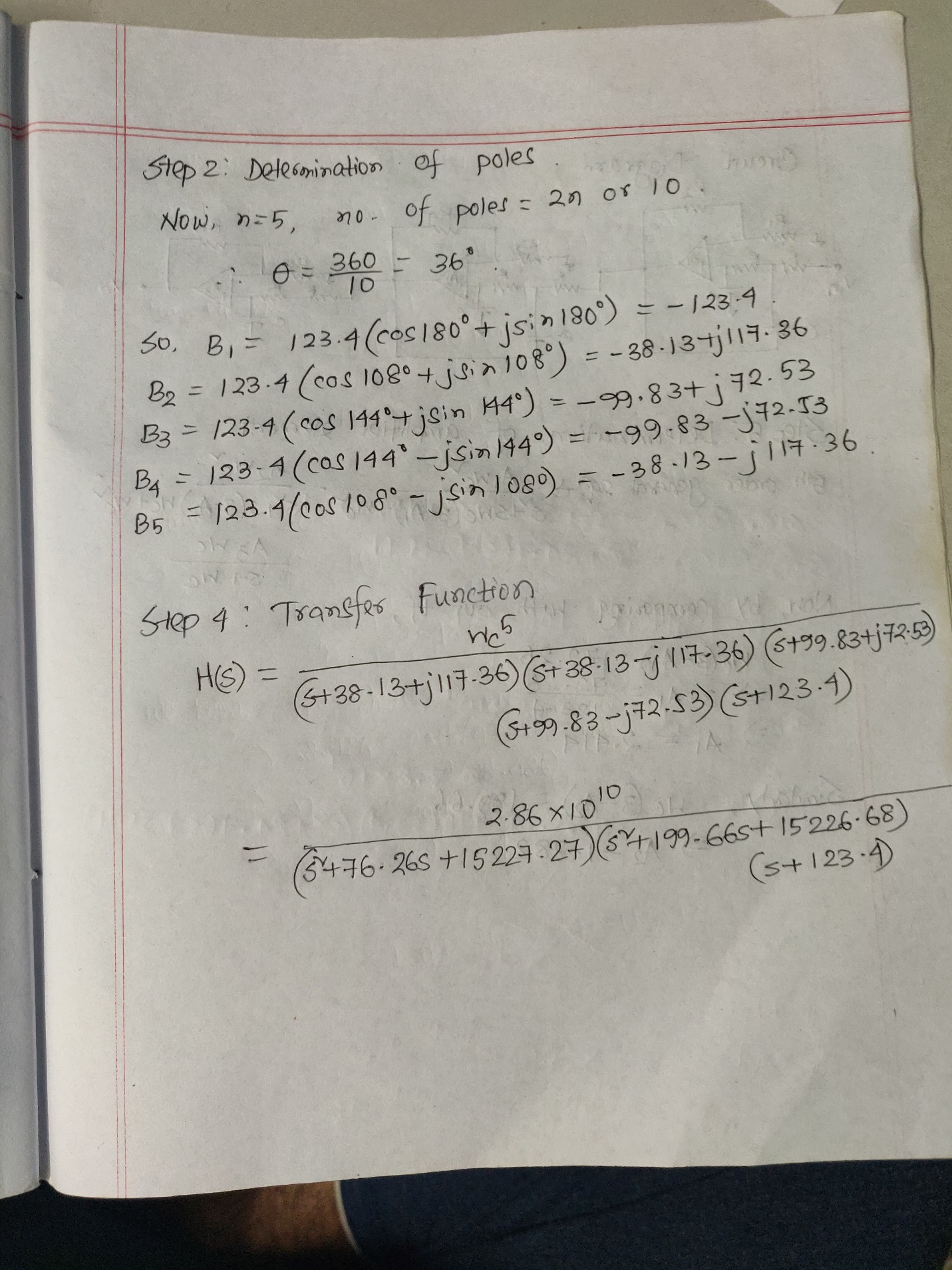
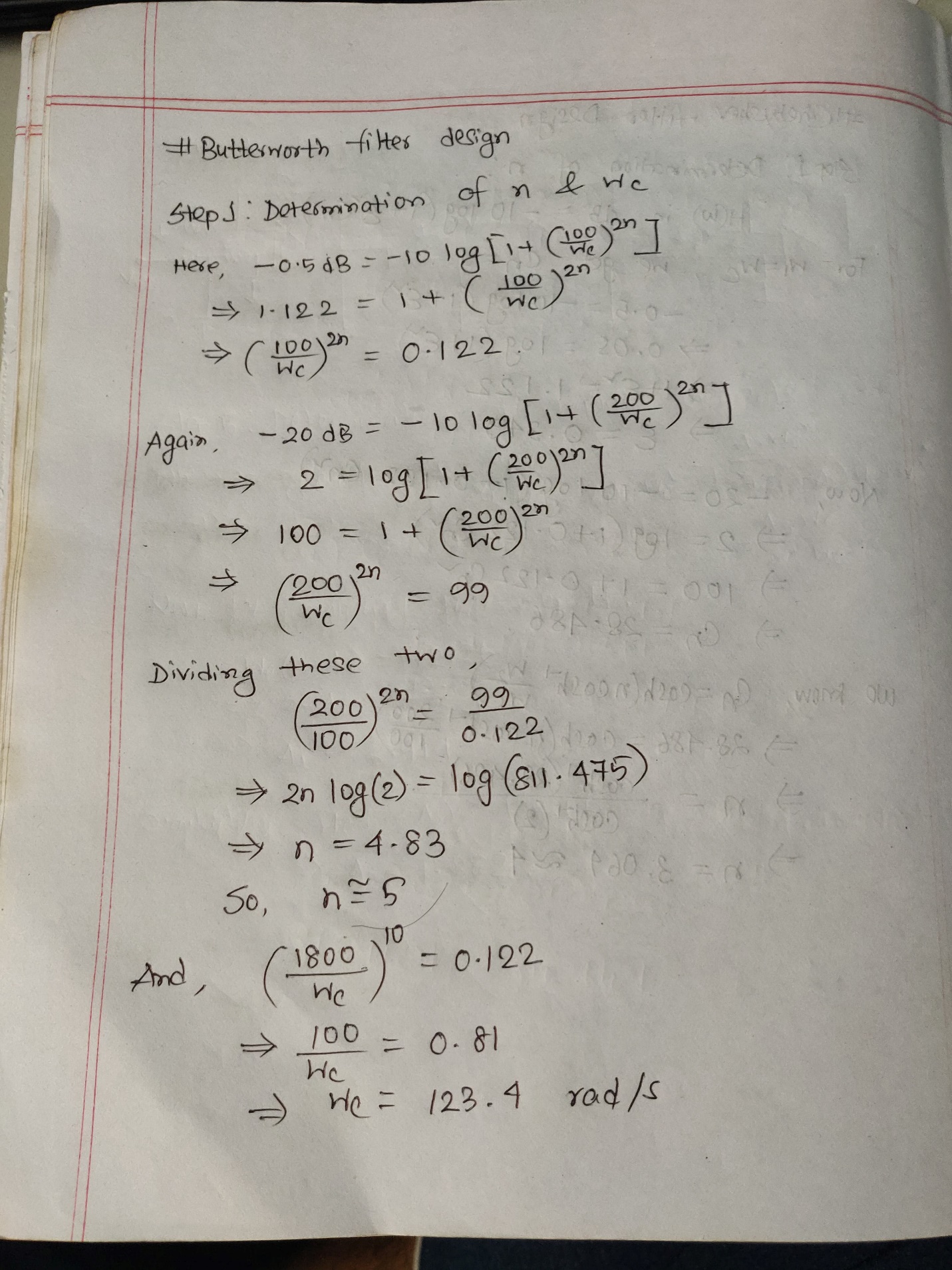
**TASK 1:**

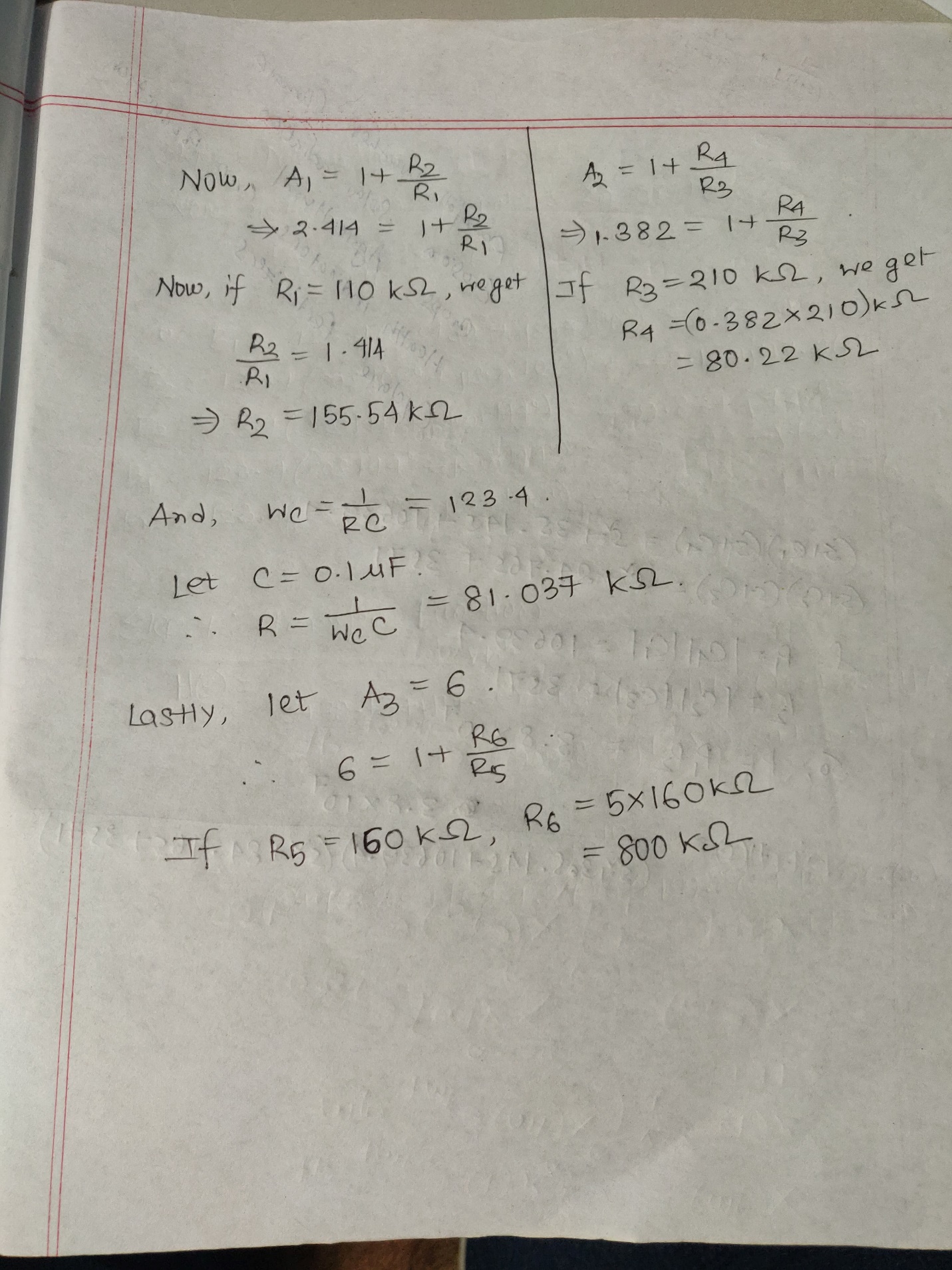


A)Pole-Zero Location

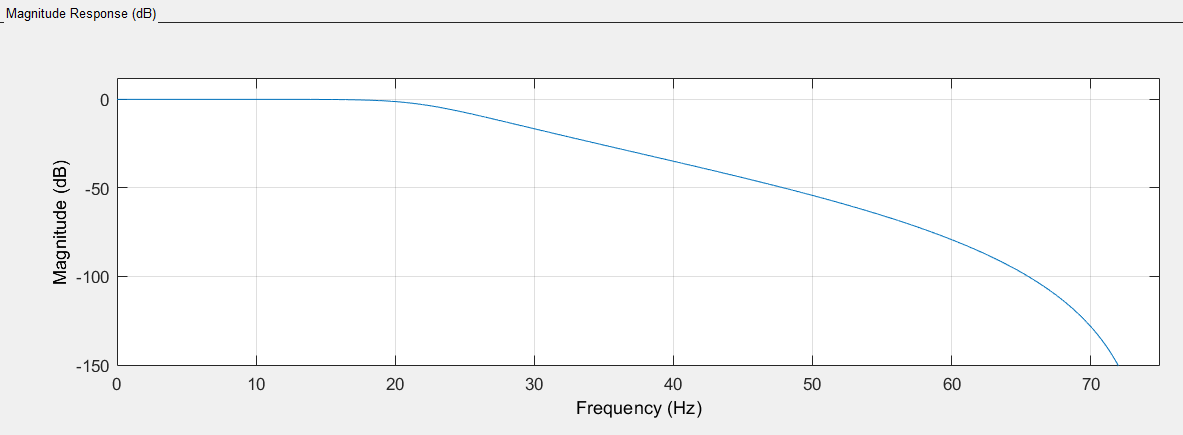


B & C) Calculated pole-zero & Circuit derivation:

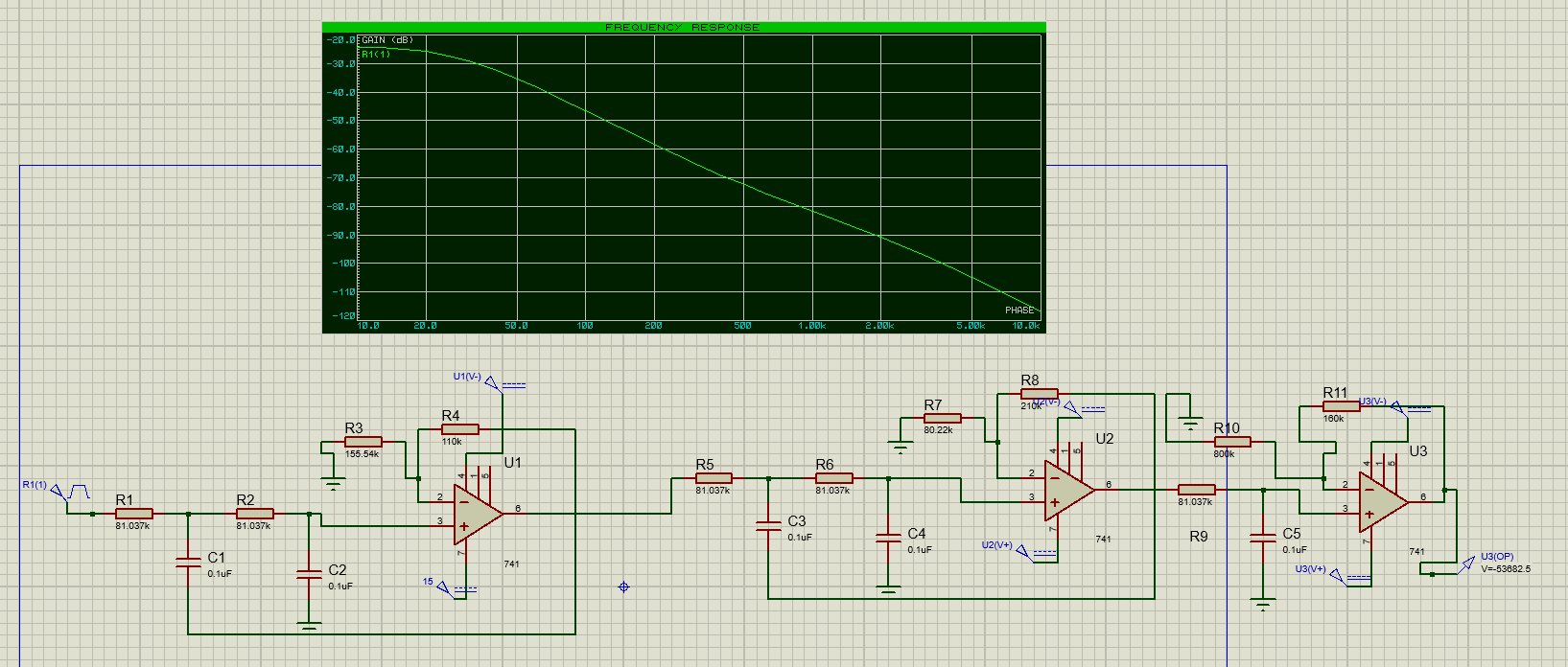




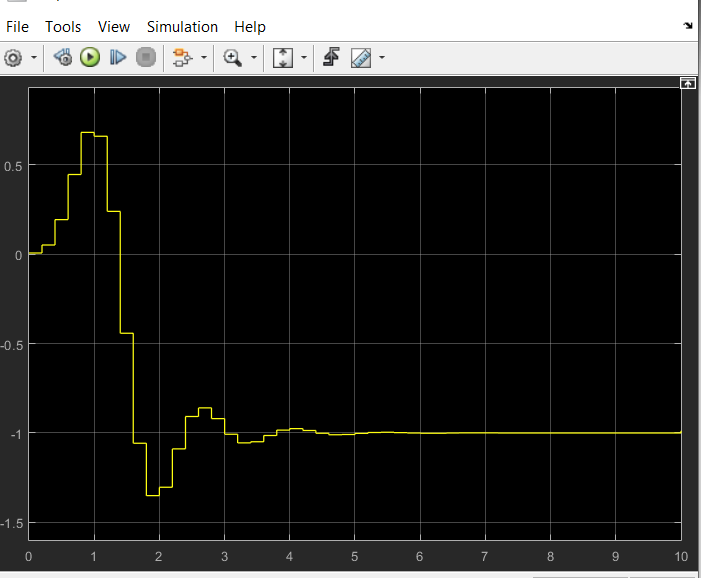
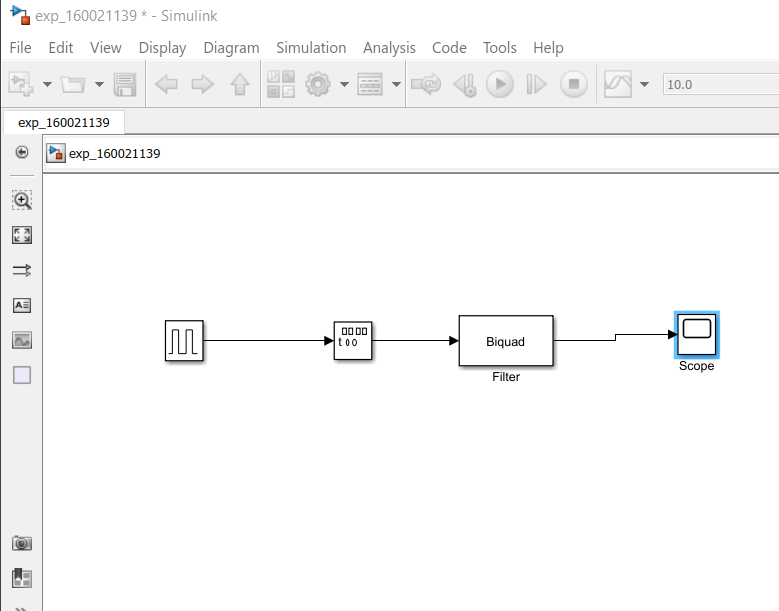
D) Frequency Response:



E) Generating given pulse using Proteus:



E) Generating given pulse using Simulink:



G) To improve the quality of filter:

To improve the quality of the filter, we can increase the order of the filter. The more we increase the order of the filter, the more the quality of the filter increases. However, increasing the order makes the filter more complex and costly. So, quality and cost must be balanced according to our need.