

DTU



Open-Source Chip Design

An 'experimental' special course at DTU

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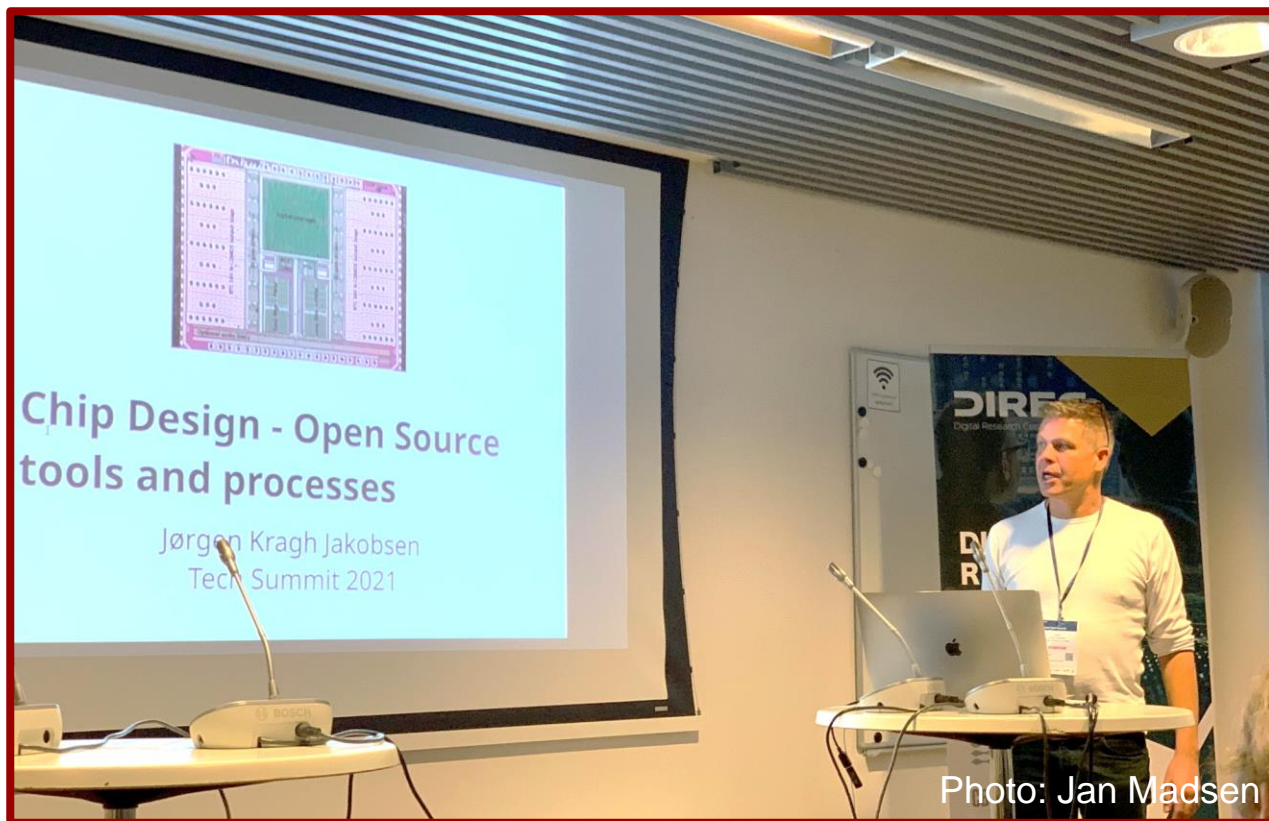
Tjark Petersen

Nicolai Dyre Bülow Jespersen

BSc Students in Electro Technology

Motivation

Digital Tech Summit 2021



Jørgen Kragh Jakobsen
IC Works



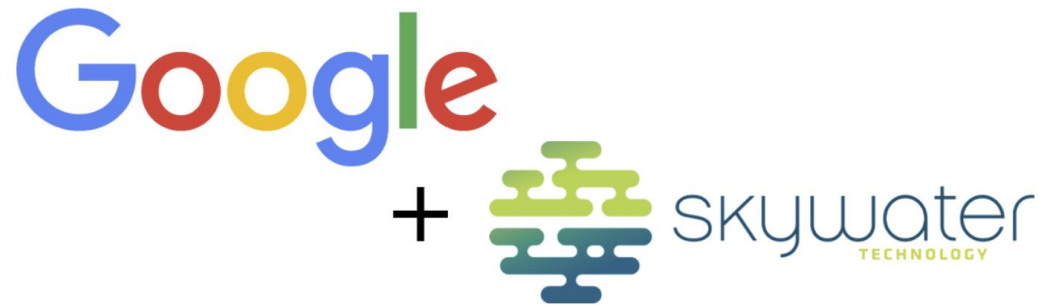
Martin Schoeberl
Professor
DTU Compute



Luca Pezzarossa
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Motivation

Open source 130nm Skywater PDK



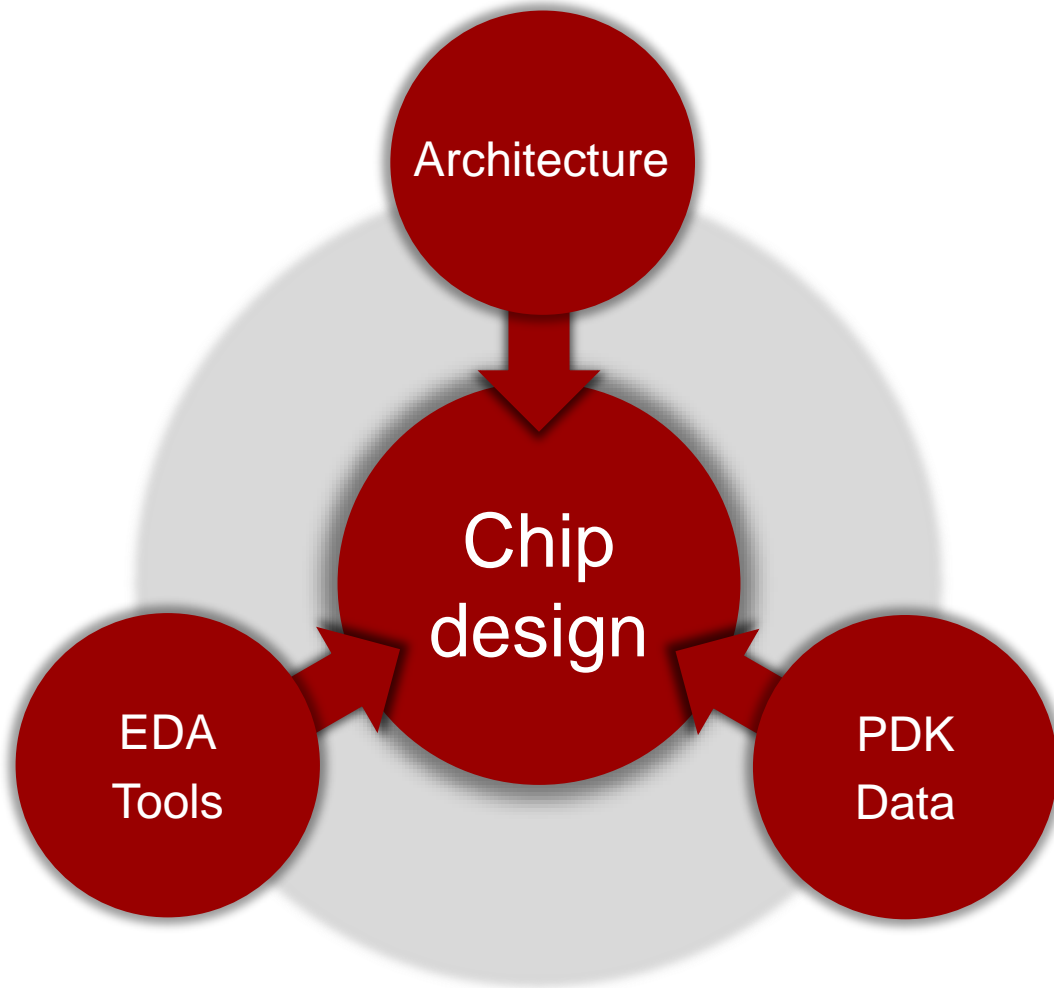
- Full open source toolchain
- From RTL down to the GDS

Open source shuttle program



- Free chip fabrication
- Design has to be open source

The *Open-Source Chip Design* special course



- 13 weeks course - 5 ECTS
- Learning objectives
 - Define precise specifications of a computing system
 - Develop (in Chisel) and test the hardware architecture
 - Use EDA tools and solve related challenges
- 12 students signed up for the course

The group



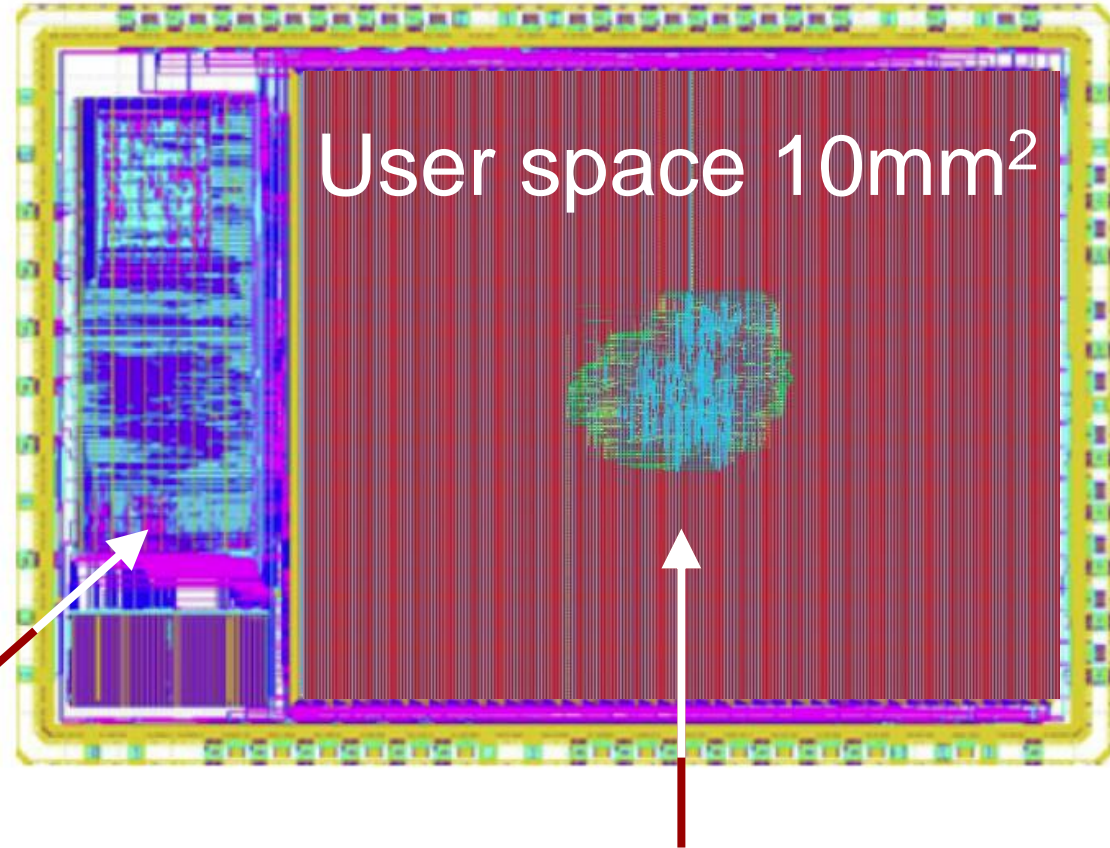
Tjark, Andreas, Simon, Niels, Nicolai, Anas, Karl, Jakob, Mads, Jonas, Jørgen.

Missing: Christa, Ulrik.

Our architecture

- Based on **caravel**
 - **Pre-made harness**
 - **I/O management**
- Heterogeneous dual core processor

Harness



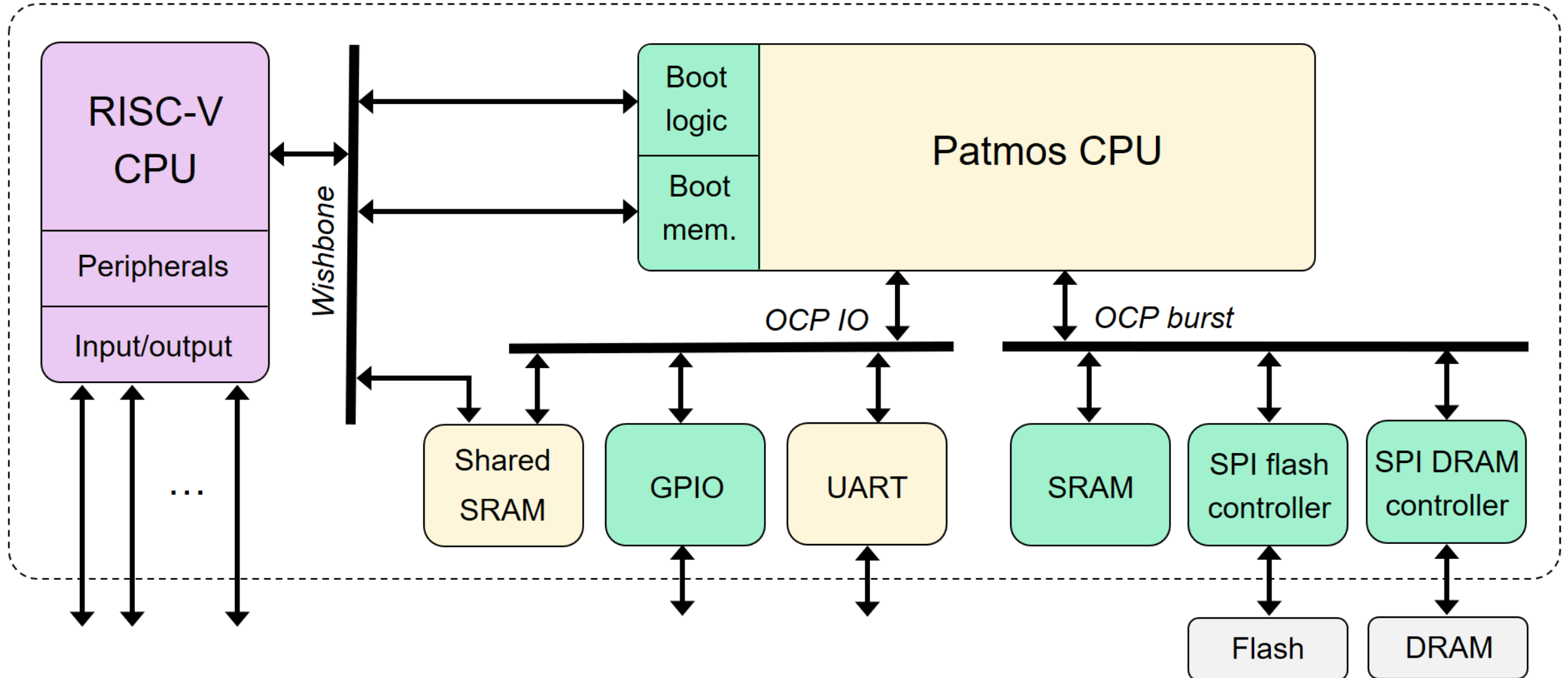
User space 10mm²

Small RISC-V CPU

Patmos time predictable CPU

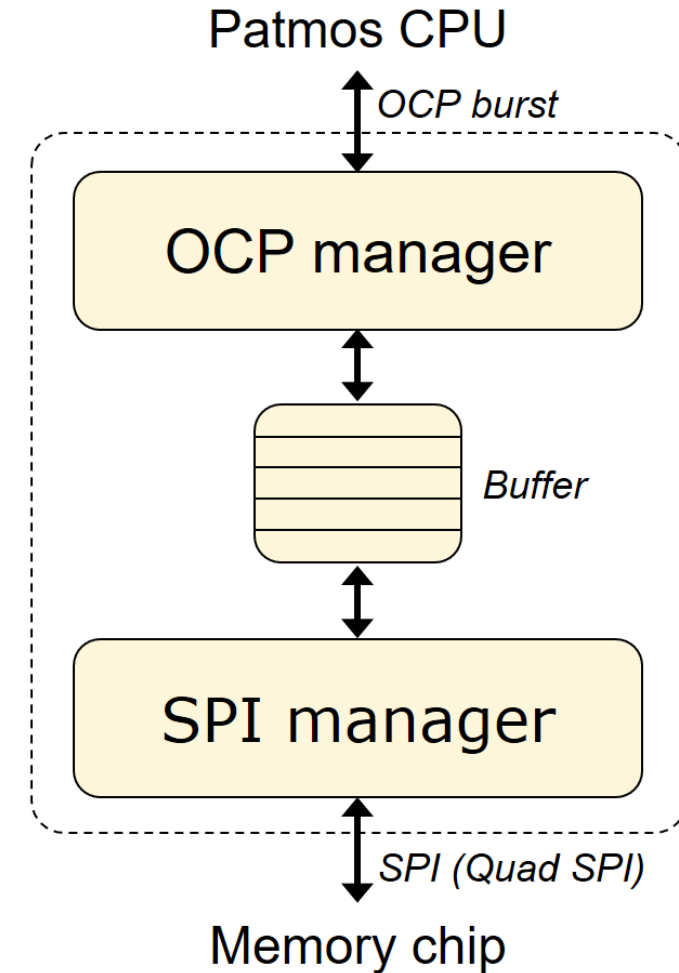
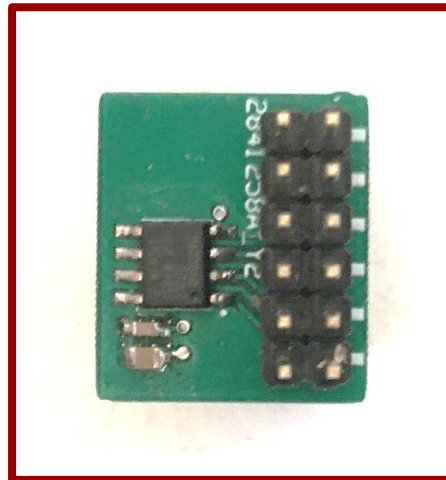
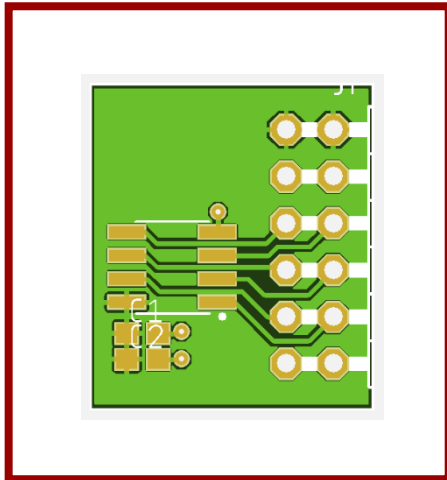
Our architecture

Silicon chip



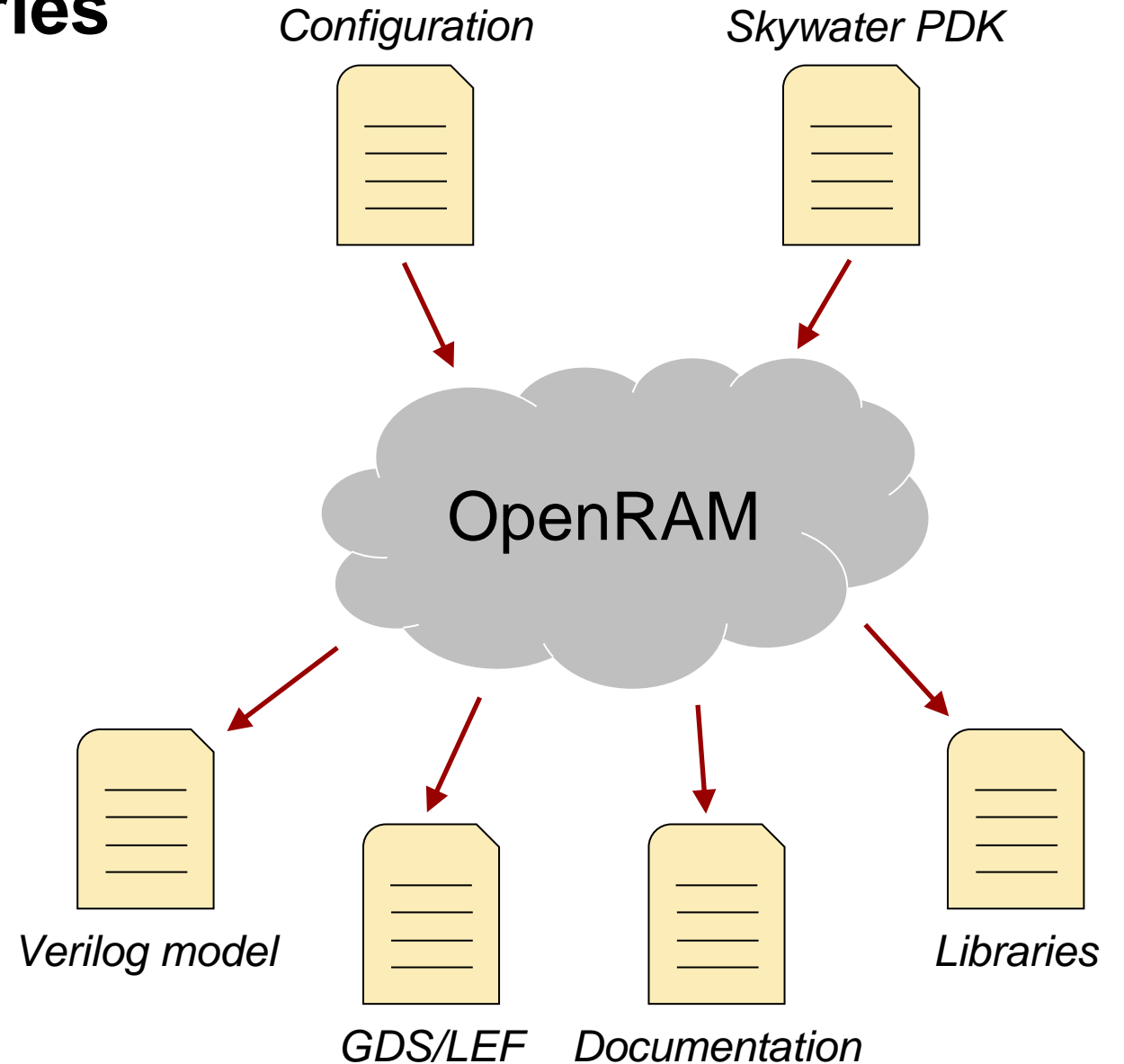
External memories

- 10mm² cannot fit large memories
- Off chip DRAM and Flash
- We developed a **memory controller**
- We tested on the real chips



Internal (on-chip) memories

- Memories need to be generated
- We use OpenRAM
 - Precompiled macros
 - Custom memories

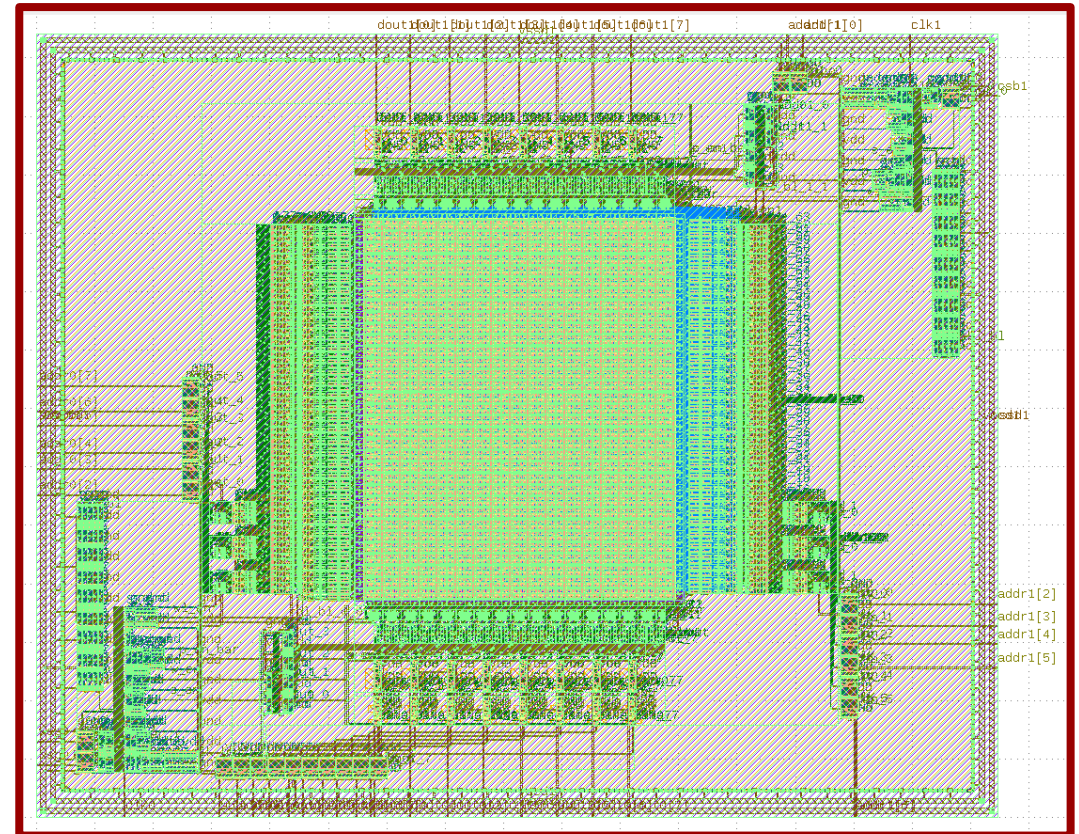


Internal (on-chip) memories

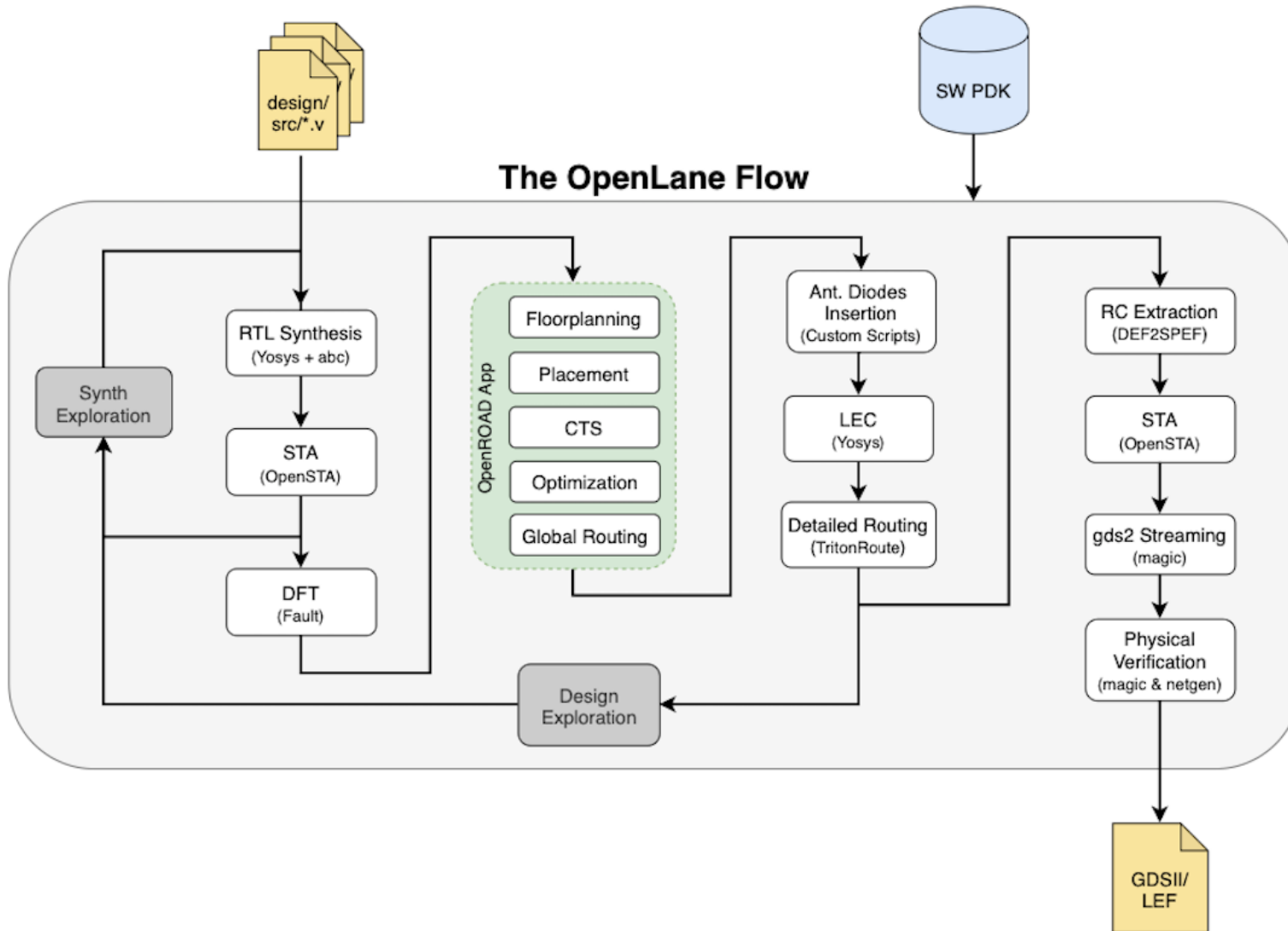
- Memories need to be generated
- We use OpenRAM
 - Precompiled macros
 - Custom memories



SRAM - sky130 - 1k x 8bit



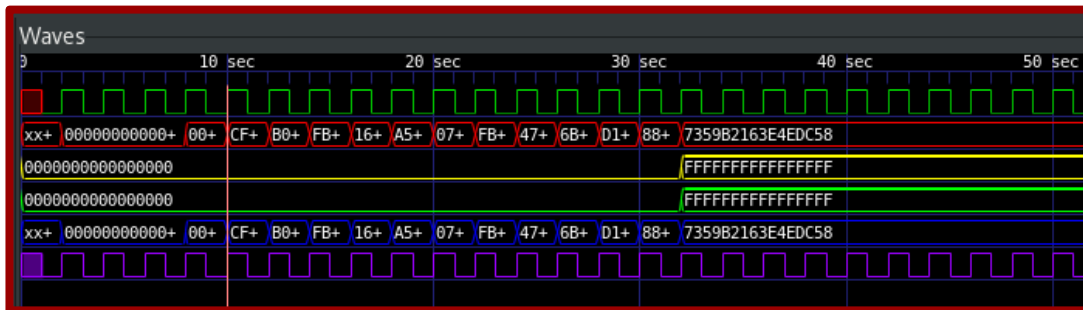
Open source tools and processes



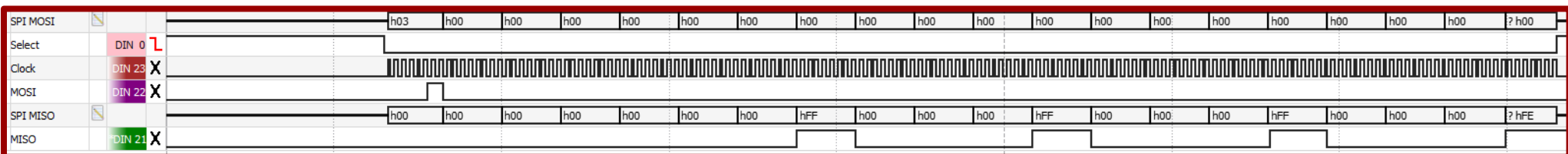
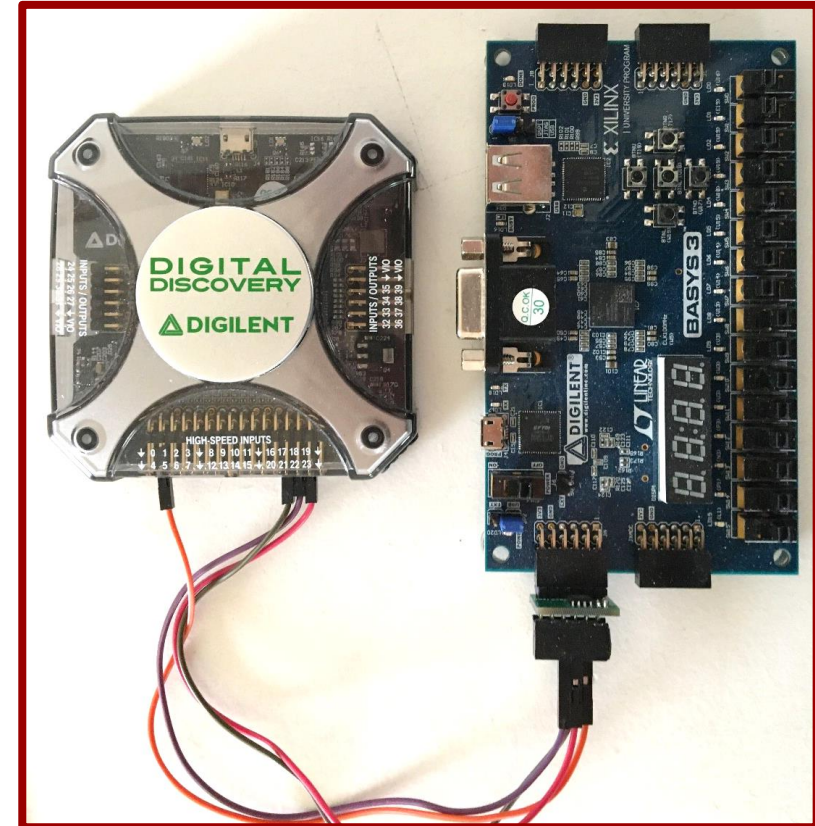
- Series of different tools
 - Yosys for synthesis
 - OpenROAD
 - Others
- Start from our Verilog design
- Finish with the GDS layout files
- Intermediate simulations

Testing

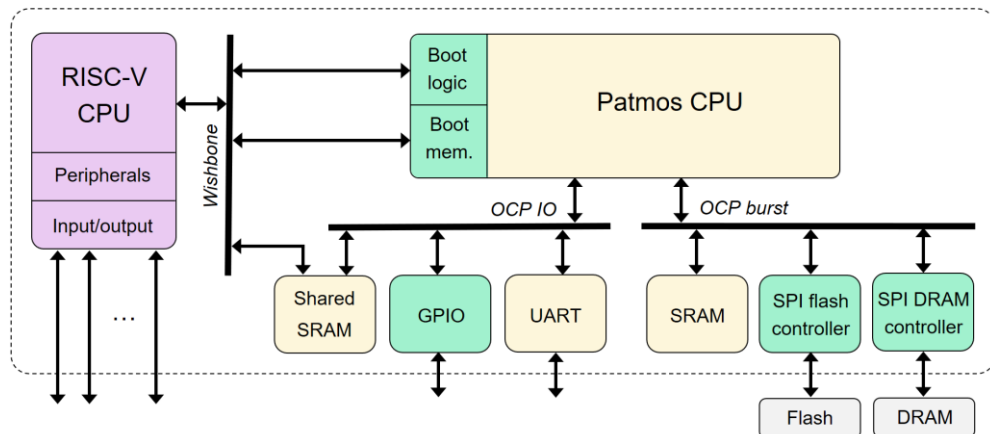
- Simulation with test-benches
- Simulation running programs



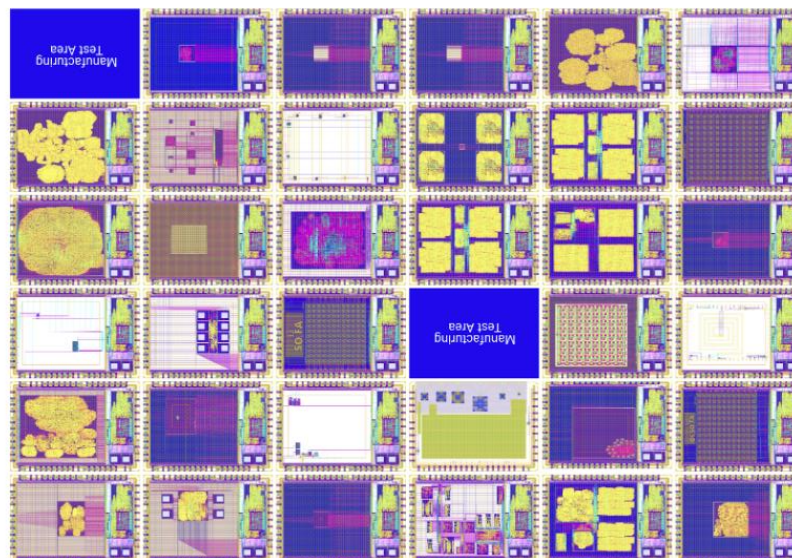
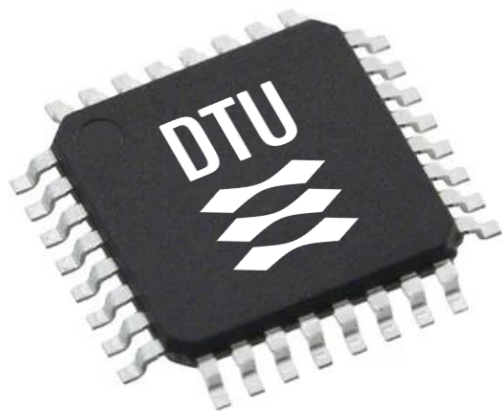
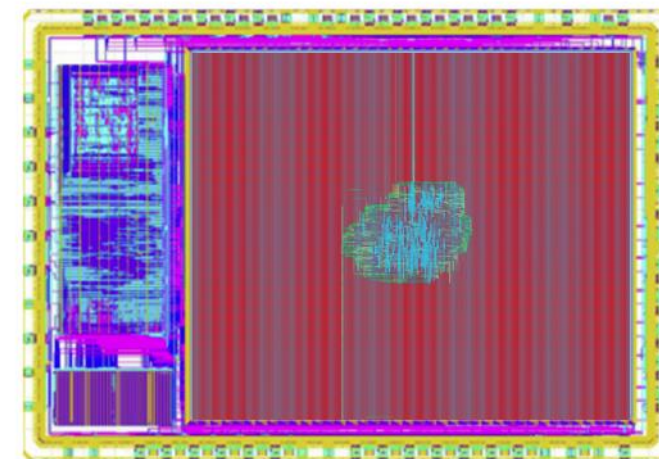
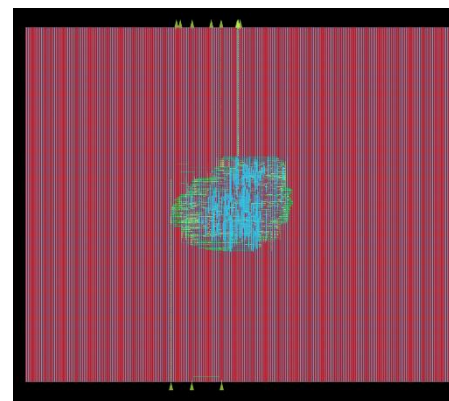
- Test on FPGA + logic analyzer



Summary



Patmos without memories



Open-Source Chip Design

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The first open source chip developed at DTU!

<https://github.com/os-chip-design>

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