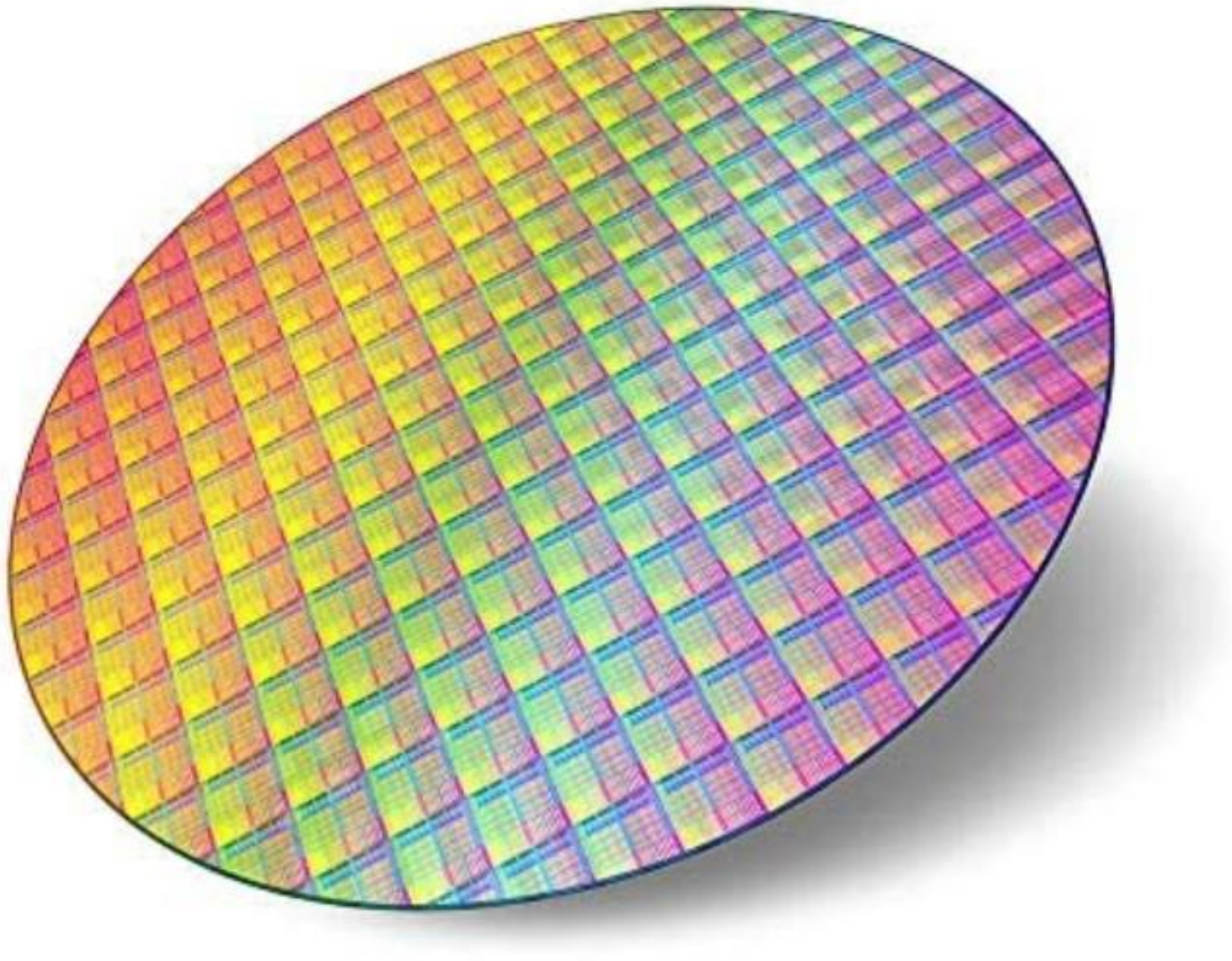
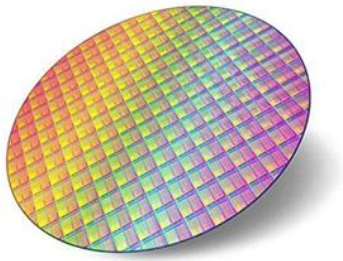
Chip verification is a growing and challenging task!



Peter Jensen, SyoSil
Martine Chegaray, Synopsys

DTU Chip Day
April 19th 2022

Who are we?



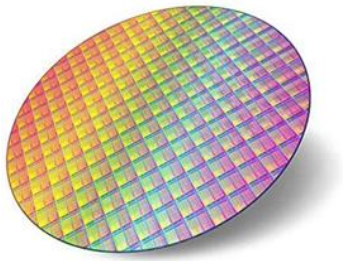
- Synopsys

  Global leader in EDA software for ASIC development
  “Powering the New Era of Smart Everything—from Silicon to Software”

- SyoSil

  Leading Danish consulting company with international projects building chips for: 5G telecom, hearing aids, AI for sensors – and more!

Agenda

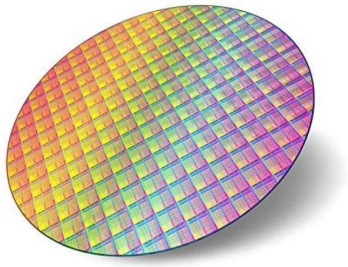


- Chip Verification :

  *Ensuring your chip design is free of bugs ****before**** you send it to the fab*

  - Why is it necessary ?
  - How do we do it ?
  - What DTU technical sciences and courses are background ?

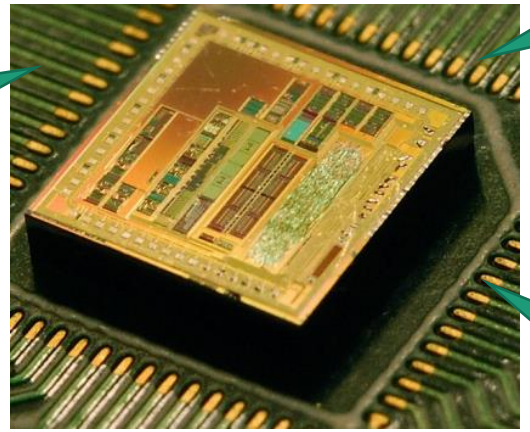
Why digital chip verification?



- What is the risk?
- What is the cost of failure?

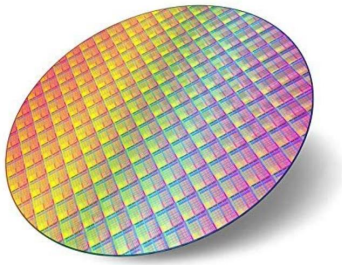
FPGA Field Failures Costly: Telecom, Security, Finance, Automotive/Aero...

ASIC Silicon Respin @sub 10nm: EUR 1mio or more (+ 3 months dev)

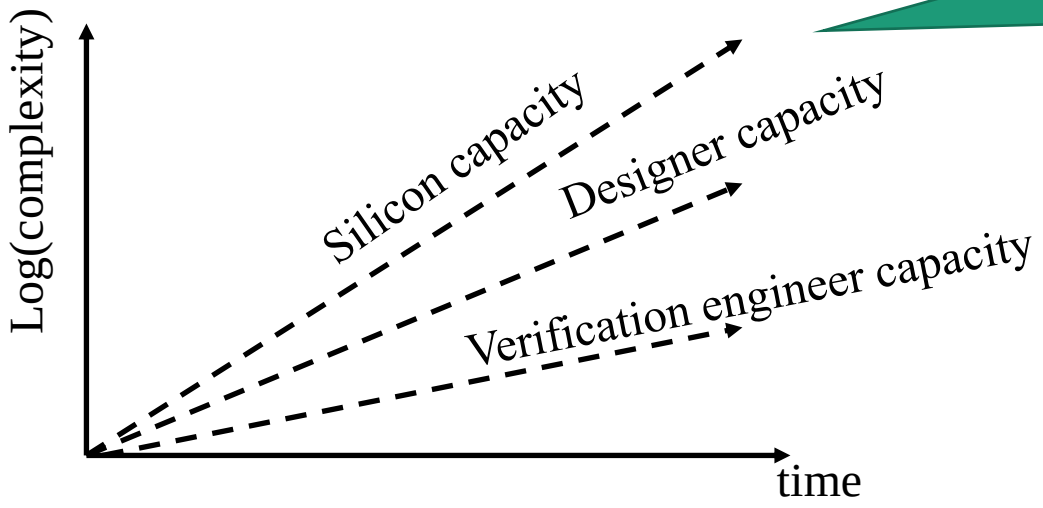


Do it 1st time right or loose your money and your market window !

Why digital chip verification?



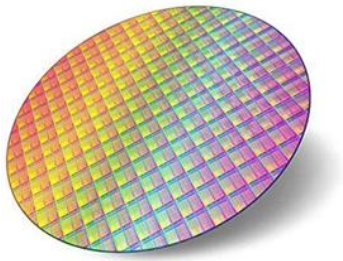
- Digital Verification Becomes Bottleneck
  - Silicon capacity is constantly increasing
  - Design gap: Designers cannot keep up
  - Verification gap: Verification engineers can’t even keep up with designers.
  - Majority of chip re-spins is due to functional bugs!

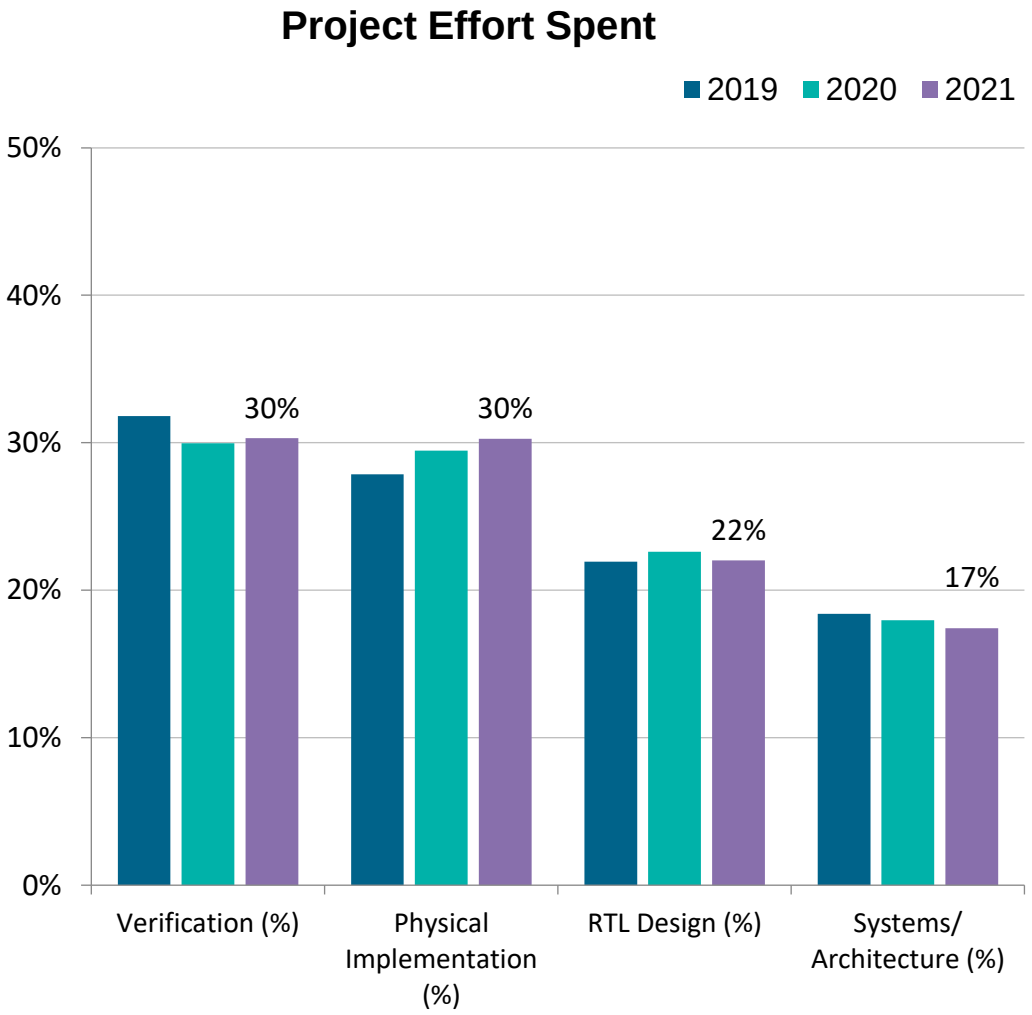


Intel 2021 AI Chip ”Ponte Vecchio” has 100*10^9 transistors !

Breakdown of total ASIC development efforts

GLOBAL 2021

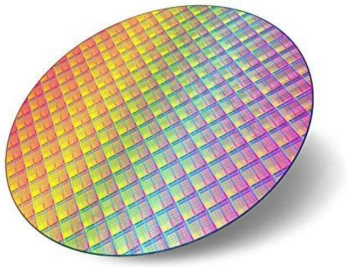


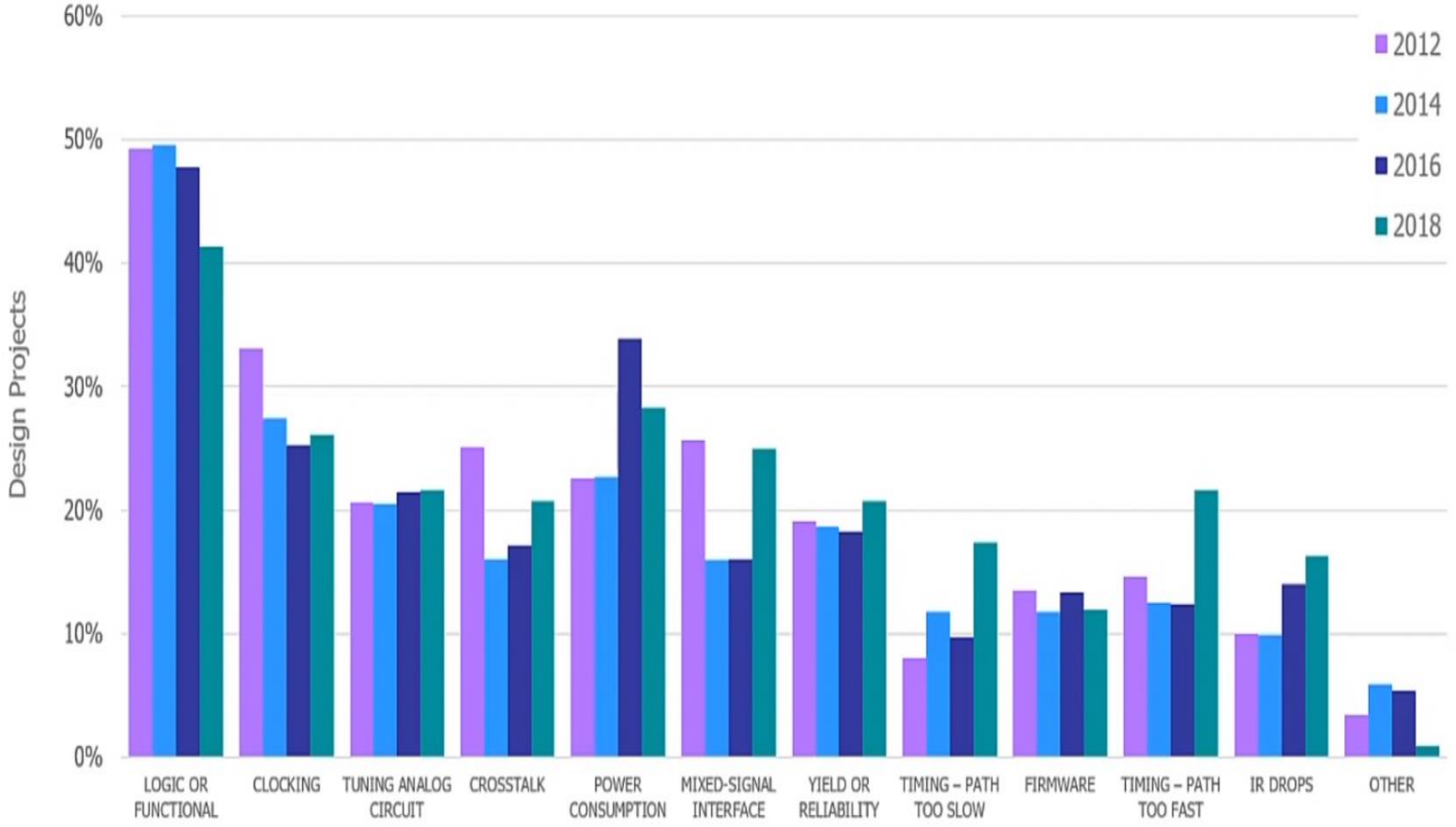


3,434 respondents WW

Source: Synopsys Global User Survey 2021 – used with Synopsys' permission.

What are the bugs?

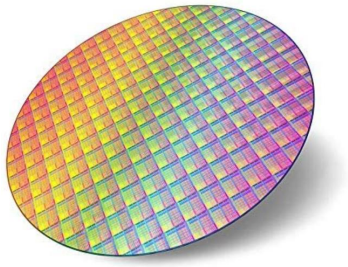




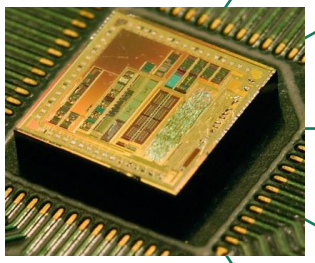
Type of CHIP flaws contributing to re-spin.

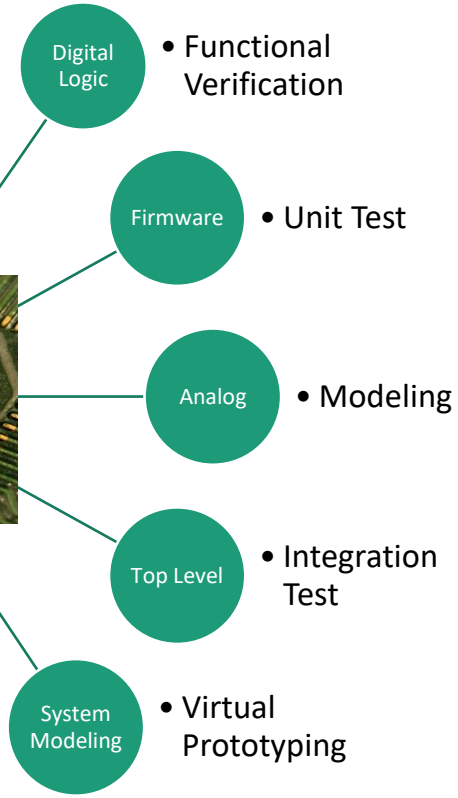
Source: https://semiengineering.com/why-chips-die

Chip Abstractions & Disciplines

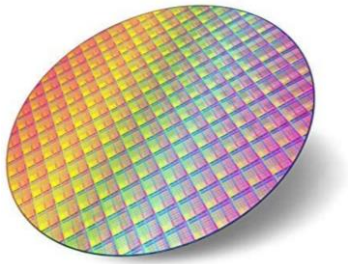


- Verification has to be done on several models of the chip
  - System level
  - RTL
  - Gate Level
  - Analog

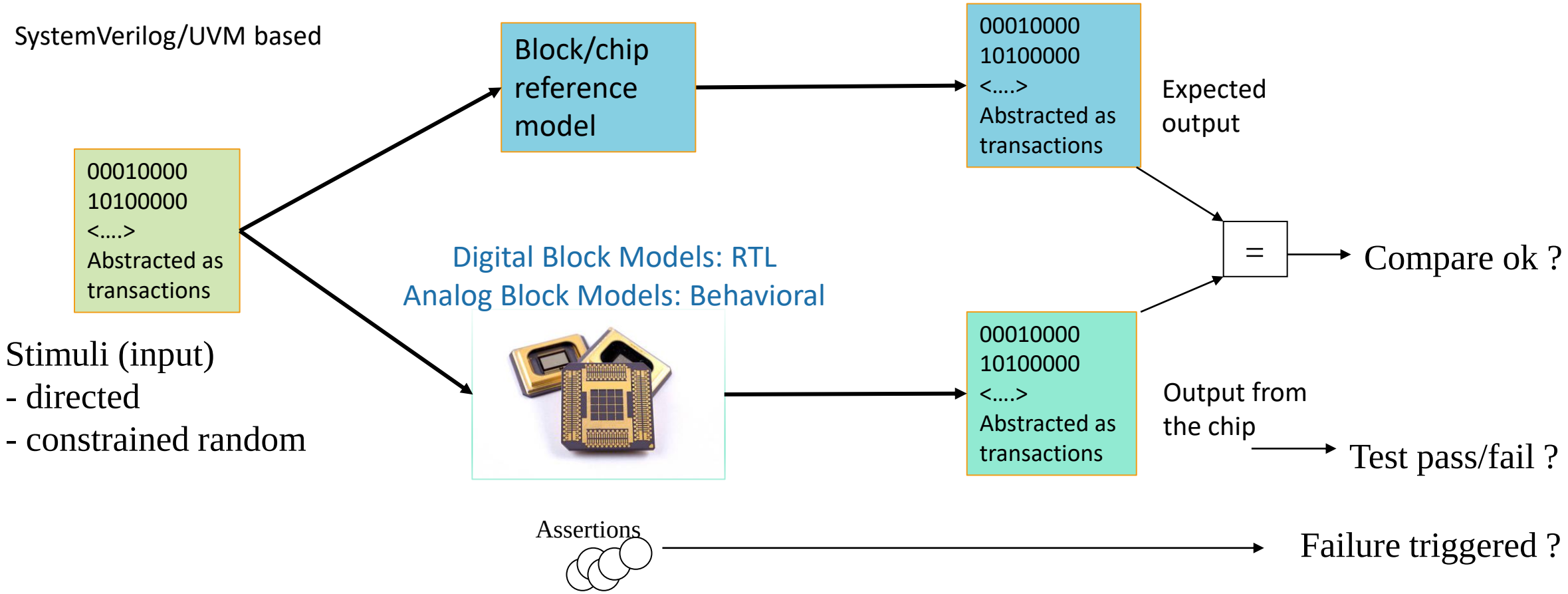




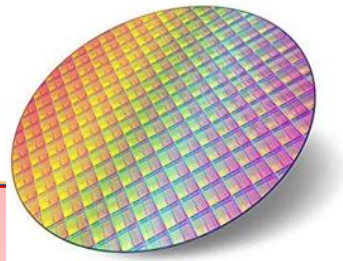
Simulation Based Verification



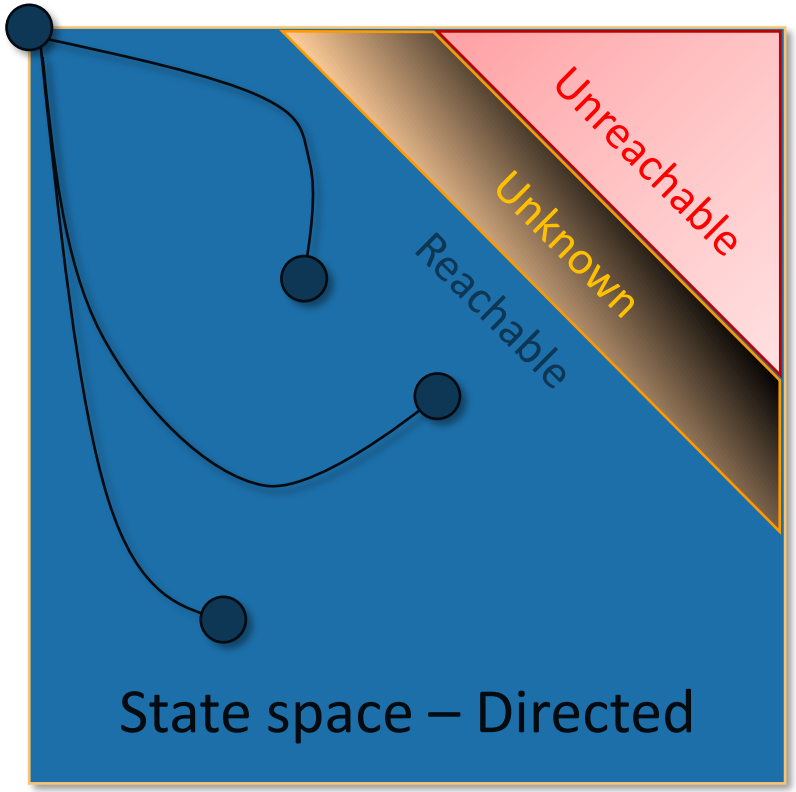
- Does the block/chip behave as intended?
- SystemVerilog/UVM based



Directed Stimuli vs. Constrained Random

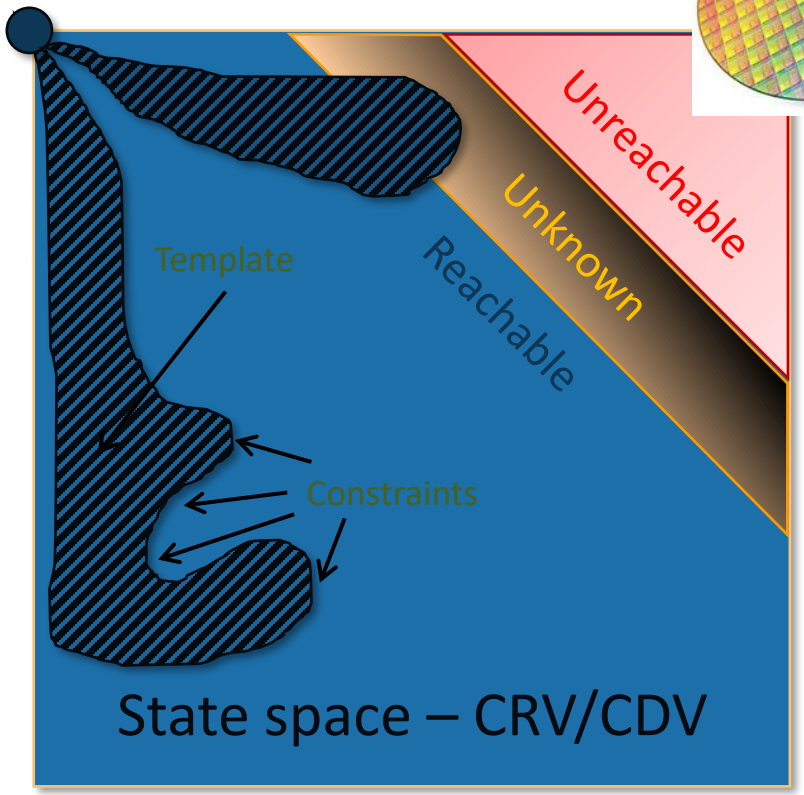


Initial state



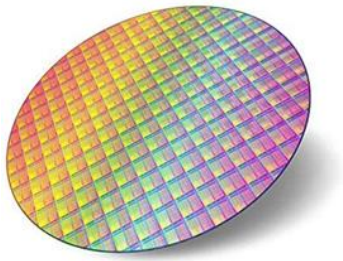
- How to reach all the states?
- How to reach unknown parts of the state space?

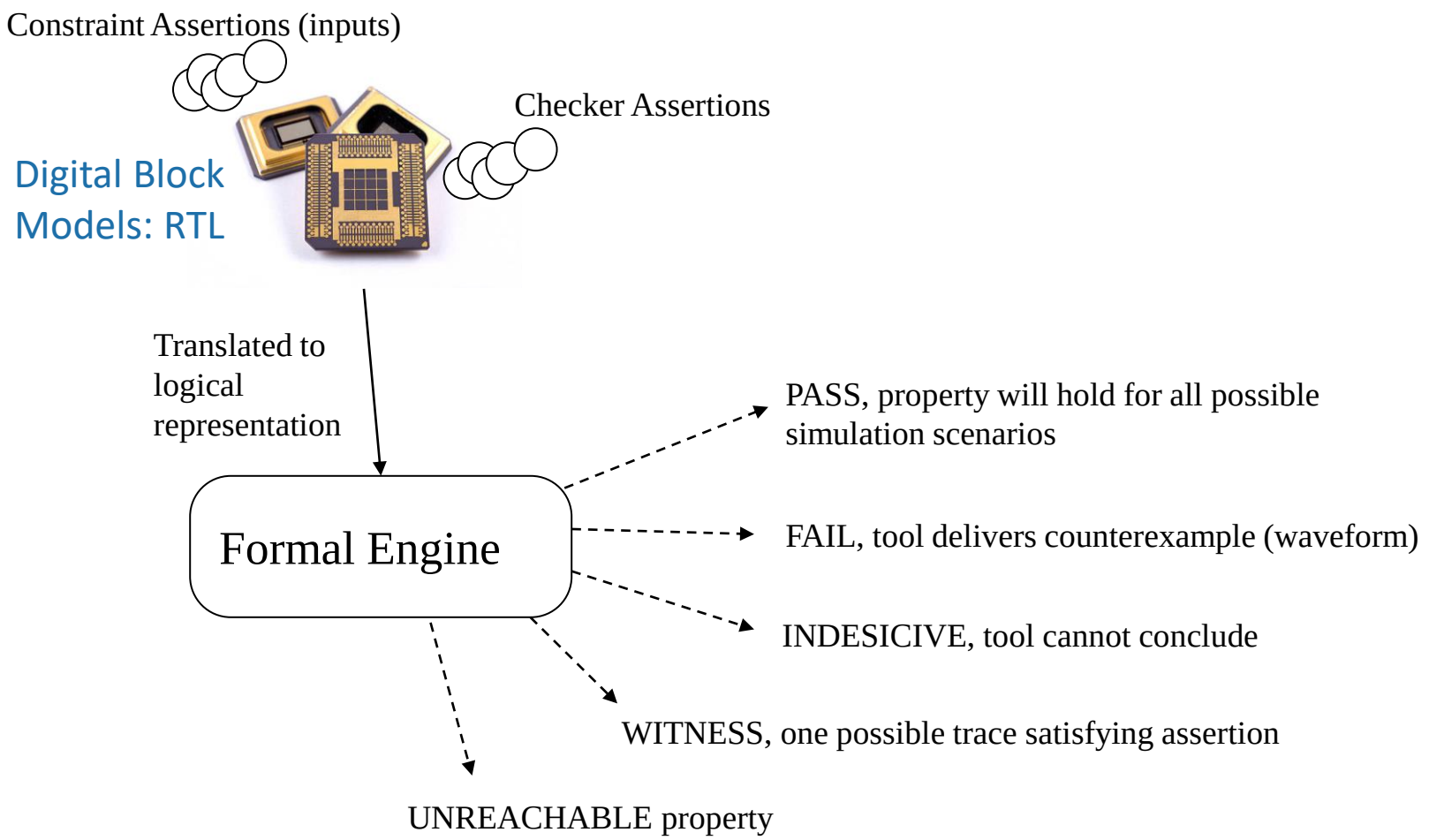
Initial state



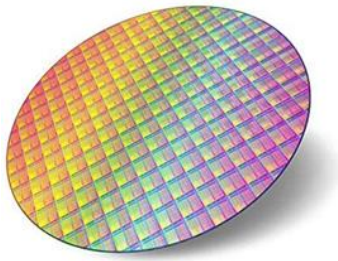
- Testcase templating
- Random stimuli + constraints
- Functional coverage

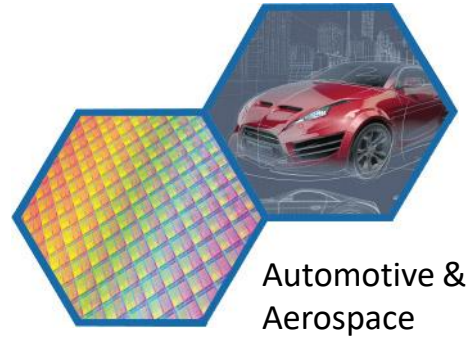
Formal Property Checking





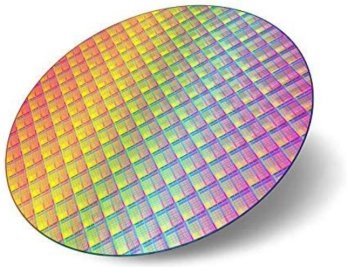
Modern ASIC/FPGA Digital Verification Process using simulation and formal verification





Automotive & Aerospace

How big are the (Scandinavian) projects ?



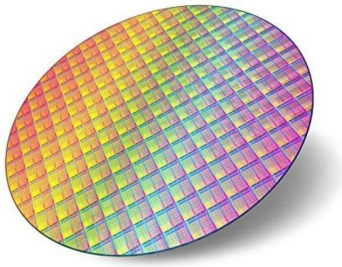
- Video Chip
  - People:
    - 30 ASIC engineers
    - 60 Algorithm/Electronics engineers
    - 300 SW engineers (FW, Drivers etc.)
  - Costs: ~10 MEUR
  - Time: 2+ years

- Verification efforts:
  - 45 git repos
  - 167 test benches
  - DV Languages:

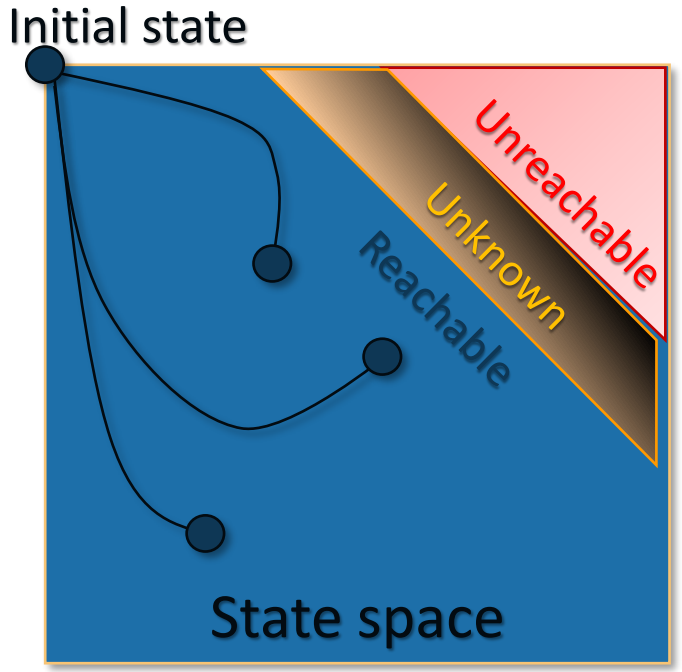
    SystemC TLM
    UVM
    SystemVerilog
    C/C++
    Python .... and more ...

Source: SyoSil

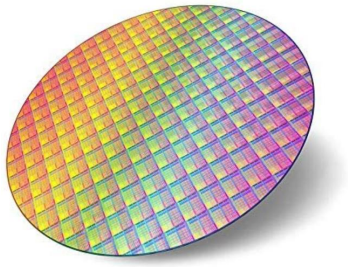
Required Technologies



- DV languages & methodologies
  - SystemVerilog/UVM, SystemC/TLM, Python, ...
- EDA tools
  - Simulators, FV tools, linters, …
- Deep knowledge of
  - Electronics (digital, analog, …)
  - Computer science
  - Algorithms; HW implementation
  - CPUs & Embedded software

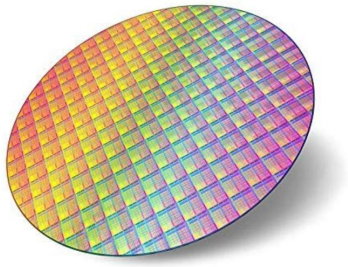


Required Technologies



- To overcome the complexity of the 100 billion transistors…
  - REUSE
    - of verification components & environments
    - at different system levels and abstraction levels
  - EMPLOY
    - OOP SW frameworks & design patterns
    - Constraint solvers
    - Model Driven SW Development (Code Generation)
    - Formal techniques using temporal logic
    - Big data (coverage, regressions)
    - AI/ML is emerging in verification

What DTU courses are relevant?



- Some examples:
  - 01227 - Graph Theory
  - 02110 - Algorithms and Data Structures 2
  - 02132 - Computer Systems
  - 02139 - Digital Electronics 2
  - 02141 - Computer Science Modelling
  - 02155 - Computer Architecture and Engineering
  - 02158 - Concurrent Programming
  - 02203 - Design of Digital Systems
  - 02205 - VLSI Design
  - 02209 - Test of Digital Systems
  - 02211 - Advanced Computer Architecture
  - 02217 - Design of Arithmetic Processors
  - 02223 - Model-Based Systems Engineering
  - 02282 - Algorithms for Massive Data Sets
  - 34656 - Design and layout of integrated CMOS circuits
  - 34657 - System level integrated circuit design

  - And more ☺

Lot's of challenges

Lot's of fun 

Thank You