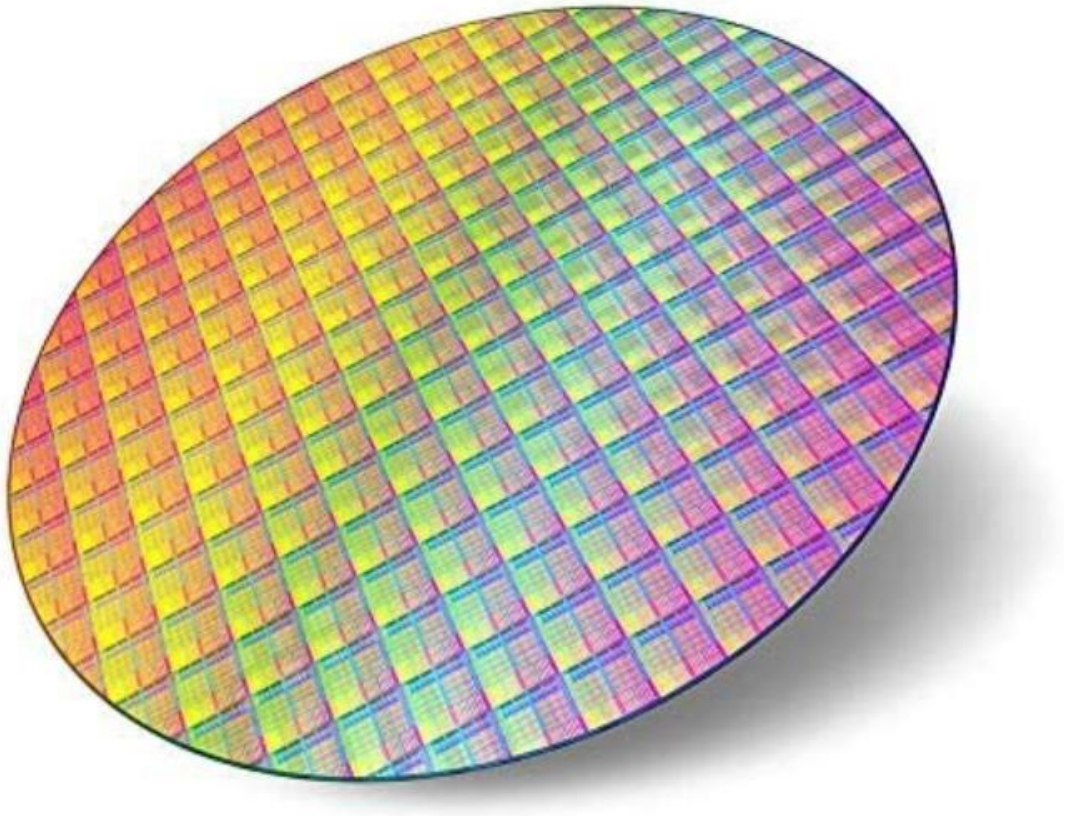
Chip Day, DTU, April 19th, 2022

ASIC prototyping in FPGA



Presented by:

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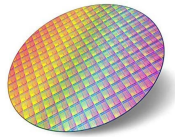
In collaboration with:

Ketil Julsgaard (WSAudiology)

Thomas Aakjer (MicroChip)

FPGA vs. ASIC products



Company	FPGA	ASIC	DK development
Demant		X	Hearing Instrument
GN Hearing		X	Hearing Instrument
Infineon		X	Speaker Amplifier IC
Knowles		X	MEM Microphones
Microchip		X	Networking
Napatech	X		Networking
Nvidia		X	Optical interconnect
Silicom Denmark	X		Networking
Skycore		X	Power converters
WSAudiology		X	Hearing Instrument
Xena networks	X		Networking
IP core vendors / Consultants			
Comcores	X	X	Networking
Zeuxion	X	X	Misc.

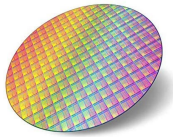
ASIC drivers:

- Small physical dimension
- Low power
- High volumen

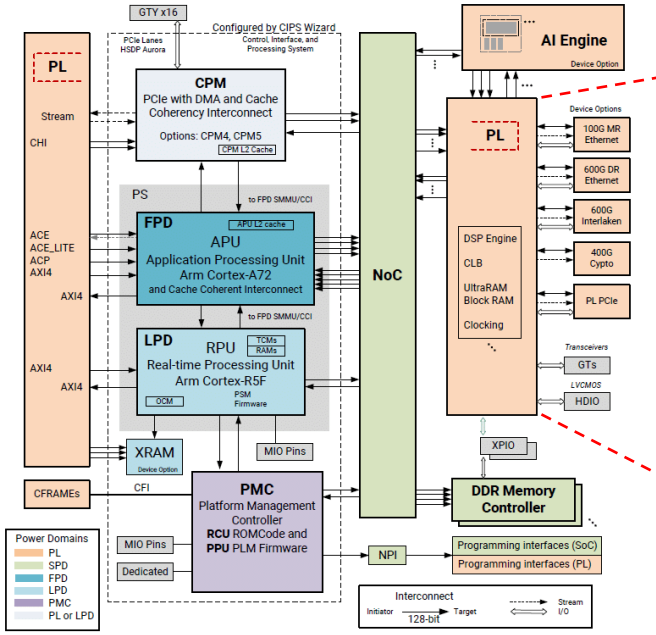
FPGA drivers:

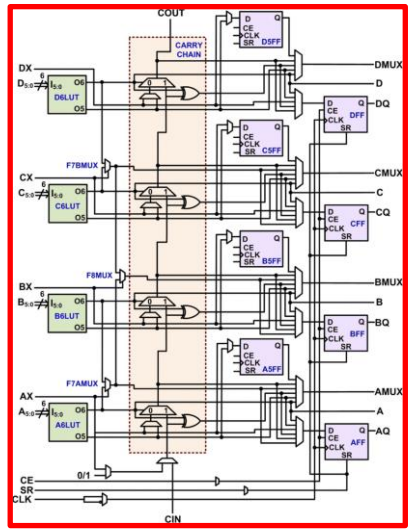
- Frequent updates
- Early technology adaption
- Low volumen

FPGA vs. ASIC technology

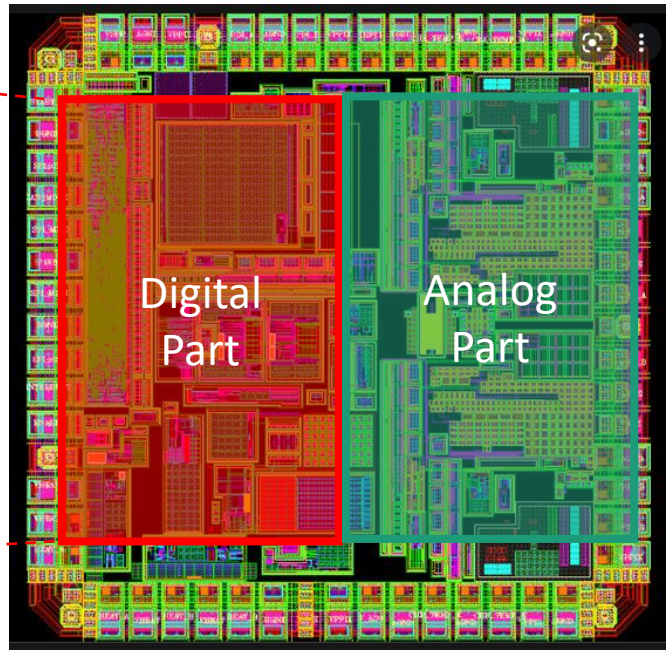


FPGA (Pure digital)



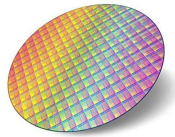


Custom ASIC (Analog + digital)

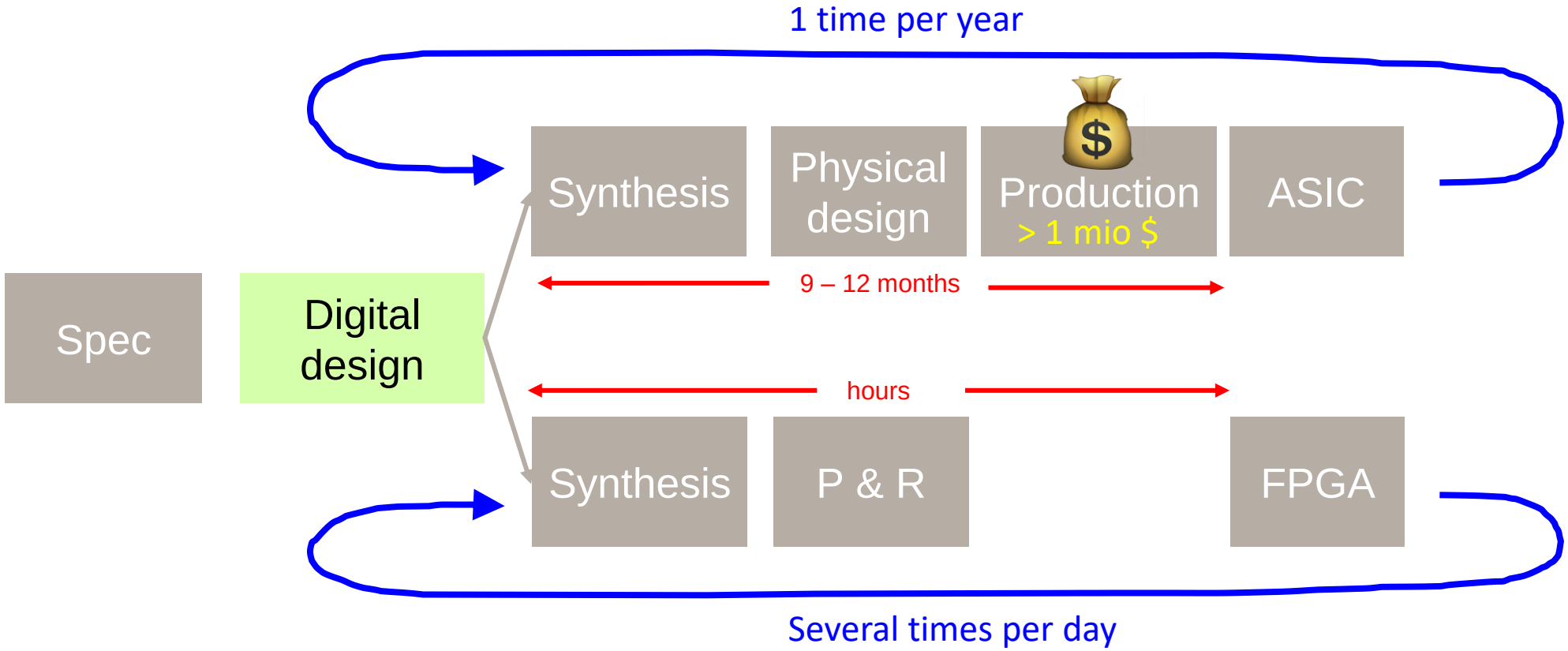


	FPGA	ASIC
Size	~cm^2	~mm^2
Power	+100W	mW
NRE	0	$1 mio+
Price / unit	$ 5000+	< 50$
Upgrade	Yes	No

FPGA vs ASIC design flow.

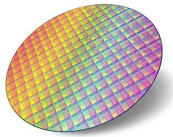


- Digital design is (largely) the same
- Rest of the flow is very different



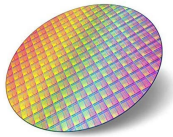
- FPGA emulation allows rapid prototyping of the digital design

FPGA emulation: Motivation



- Minimize risk of respin.
  - IC errors seriously impact ”time to market”
  - Tapeout of an IC is VERY EXPENSIVE
- Get SW started
  - Often SW development is the major part of a chip project
  - SW important for verification
- Simulation is slow
  - Testing interfaces with existing equipment in the lab is very convincing
  - Testing in the lab is much faster than simulating
- Improved debugging in FPGA
  - Debugging inside FPGA (e.g. ChipScope / Signal tap)

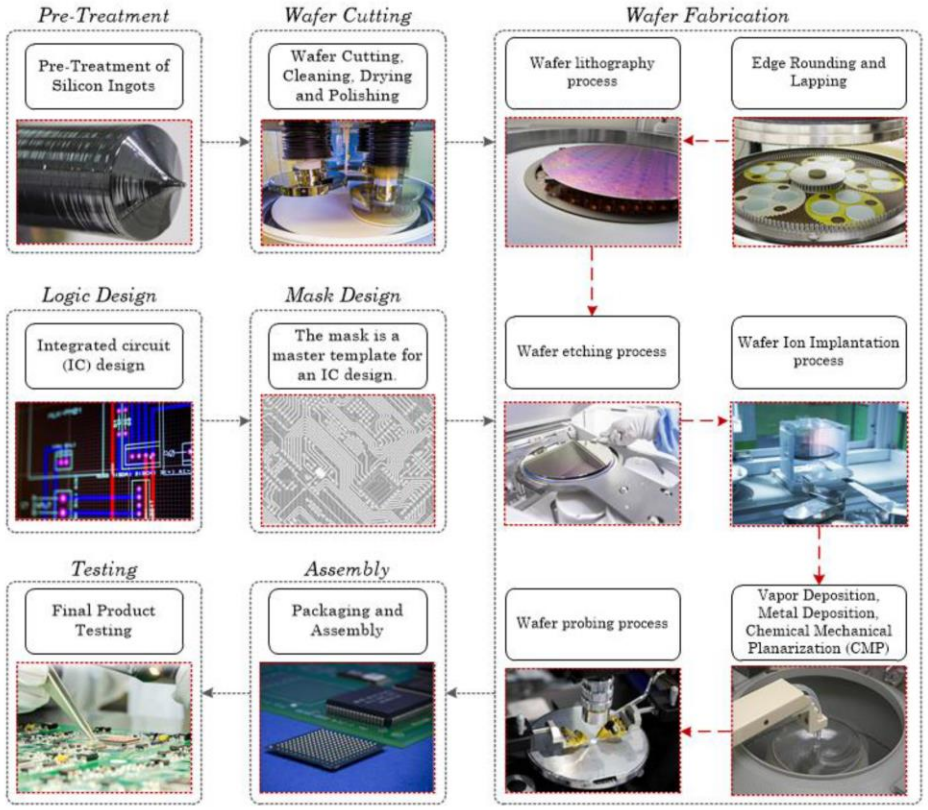
FPGA emulation: Limitation



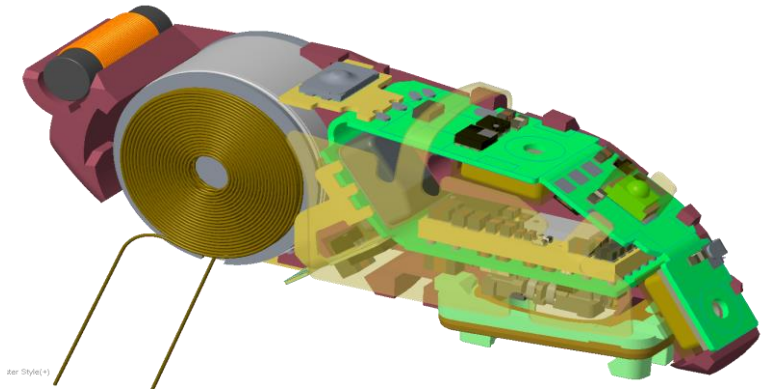
- Power gating (Low power designs)
- FPGA technology
  - Hard IP needs to be included into RTL (added risk)
- Interface to analog contents
  - External to the FPGA i.e partitioning the design.
- Design size – design could be too big to build prototype
  - Test selected blocks (Modify RTL i.e. add risk).
  - Reduced performance (e.g. High speed networking)
- Development of FPGA platform (HW + SW)
  - Added cost + resources

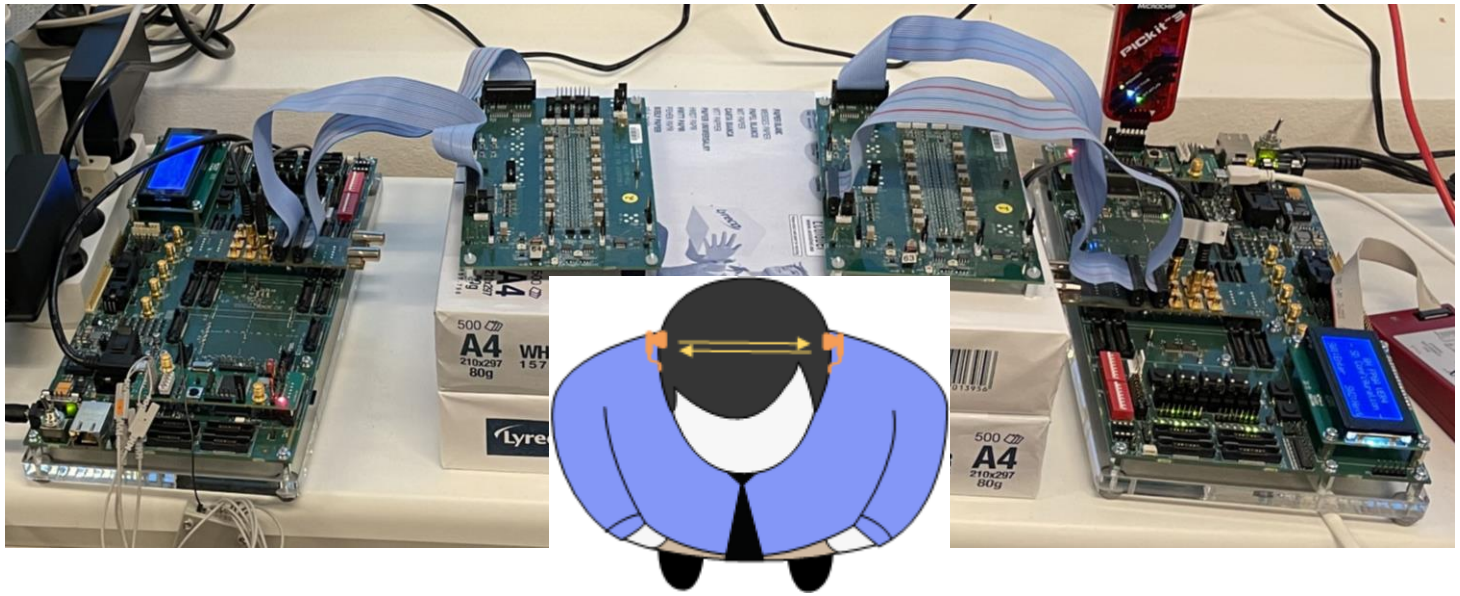
FPGA emulation: Other considerations

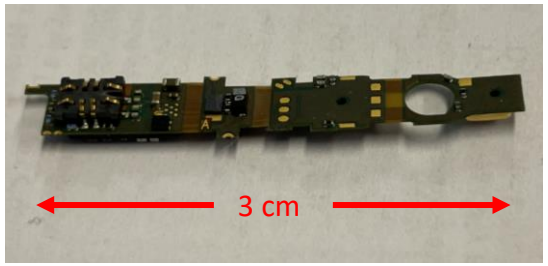
- Introducing extra tools
  - New tool chain means are added complexity / cost
  - Can cause RTL changes due to different support for RTL (added risk)
- ASIC production and production testing



Hearing aid prototyping in FPGA



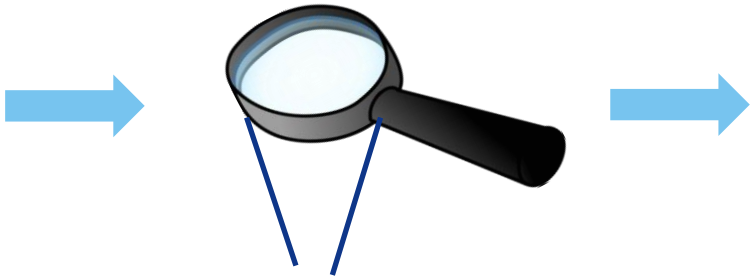




	FPGA	ASIC
Logic size	100%	100%
Power	~30W	~20 mW
Frequency	100%	100%
Price / unit	1,000 USD	~1$

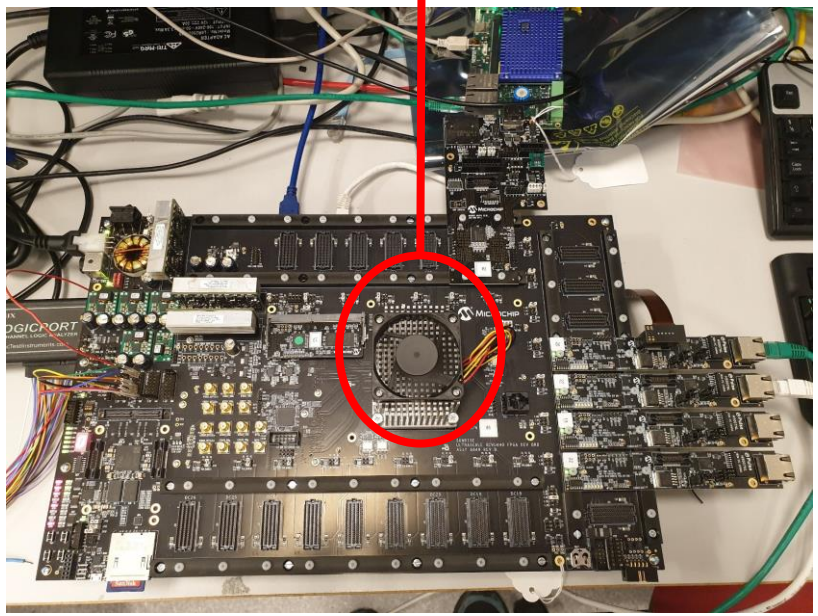
Ethernet switch ASIC prototyping in FPGA

ASIC layout



Shrinking tables, ports etc.
(port speeds the same)

$50k FPGA for pre-silicon validation



	FPGA	ASIC
Logic size	10-20%	100%
Power	~300W	~3W
Frequency	10-20%	100%
Price / unit	50,000 USD	~5$

Questions or comments ?

Thank You