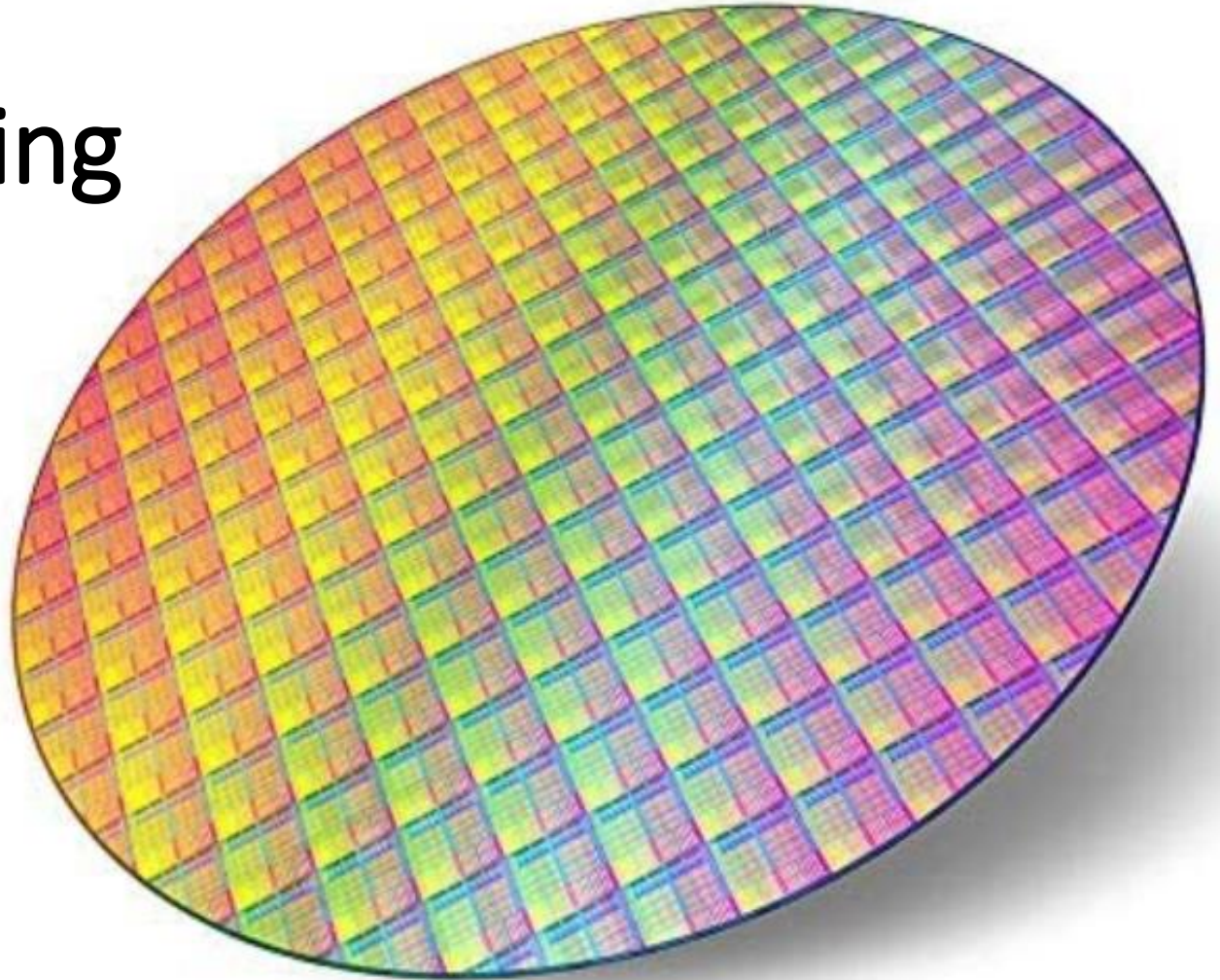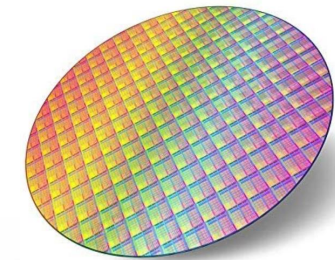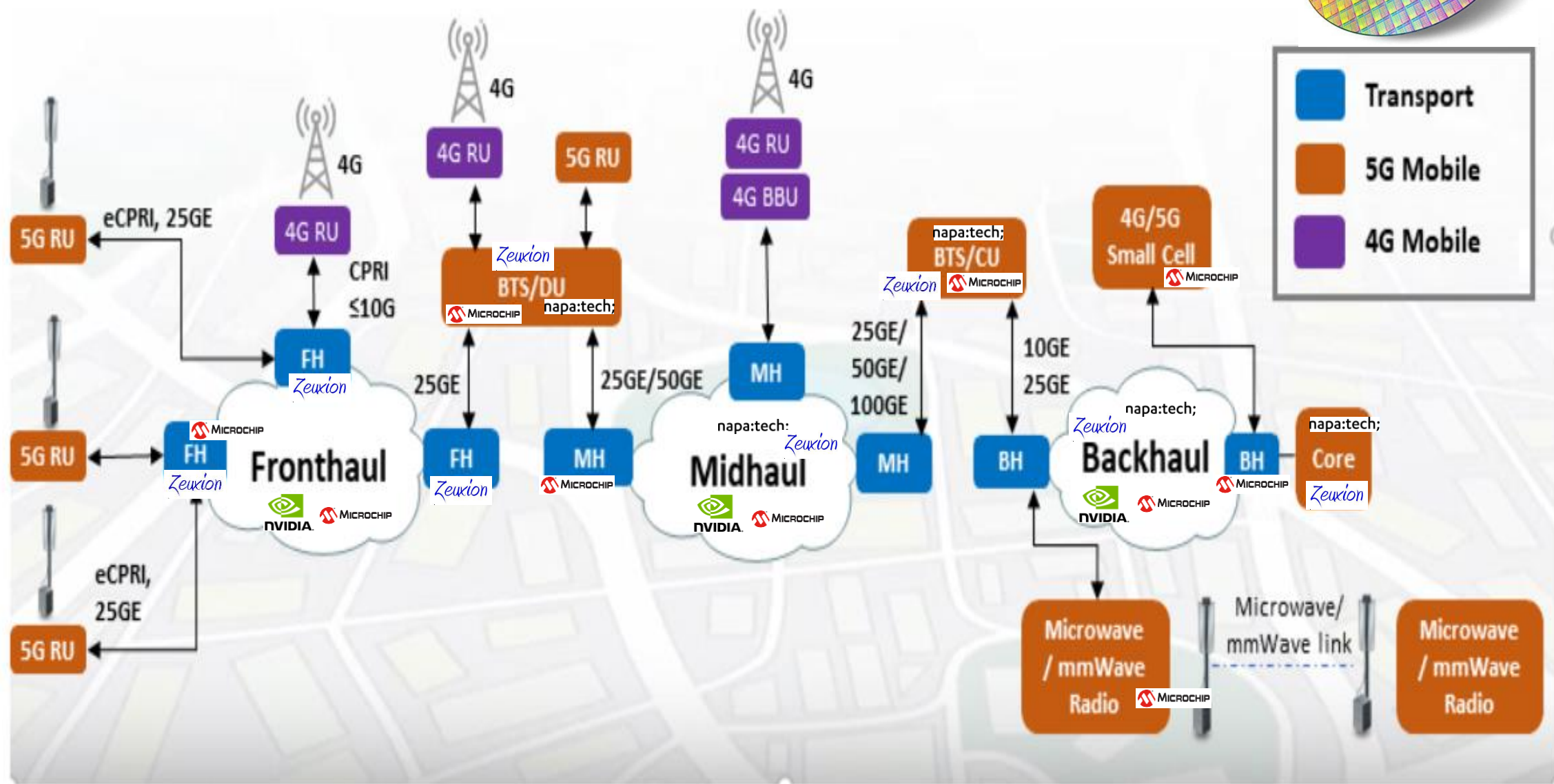# High Speed Networking

Zeuxion
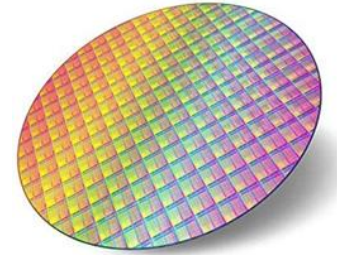## Microchip
Nvidia
Napatech

Chip Day,

DTU,
April 2022

High Speed Networking

High Speed Networking –
IP development & Design Services

IP & Projects in:

Wireless systems
Packet switching
Optical transport
Security

New technologies:

Internal chip vendor project development
Early programs – not always fun...

Working in the High-Speed Networking industry enables:

Newest roadmaps @ Tier-1 companies:

Tera bit
5G, 6G
Sub nano sec.
Virtualization

RTL Design, Verification,
Backend & project-lead opportunities
Working with teams all over the world ☺
Customer contact

Zeuxion

High Speed Networking – Ethernet/PCIe switches



Example: 200G Ethernet switch w. CPU

Denmark Design

- 28nm process
 - 100mm2 - 4.5M FlipFlops, ~1.3B transistors (> Intel Core i7 quad 2011)
    - Largest chips designed in Denmark
- 34 High speed serial interfaces – 10 Gbps/25 Gbps
- 625MHz switch core
- 1GHz Dual core ARM, DDR4 w. ECC, PCIe 3
  - Running Linux w. advanced switching application SW on top
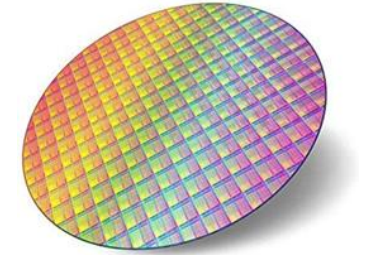- ~1000 physical SRAM inst. , all ECC protected
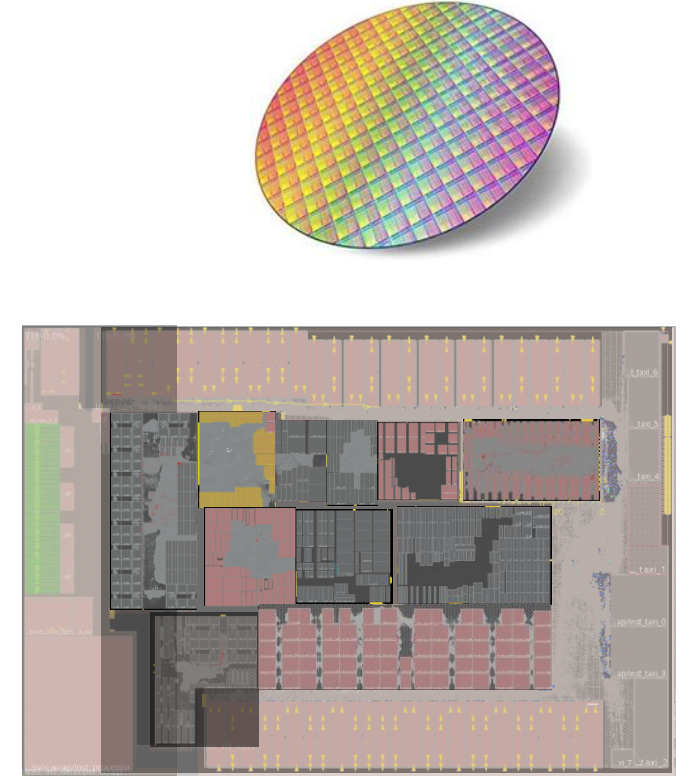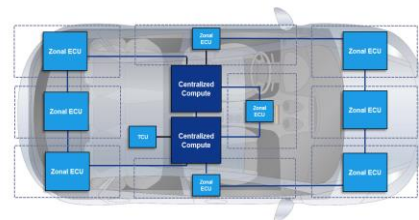
Why IC design?
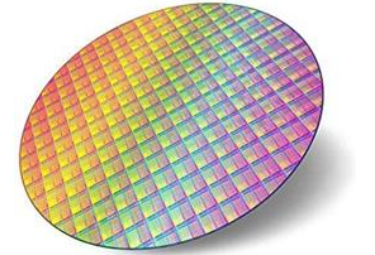
High Speed Networking –
High-speed analog chip design
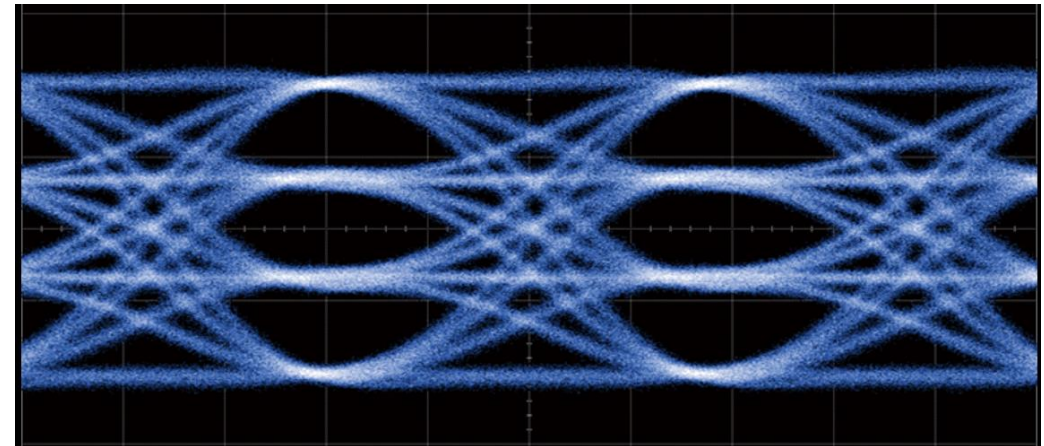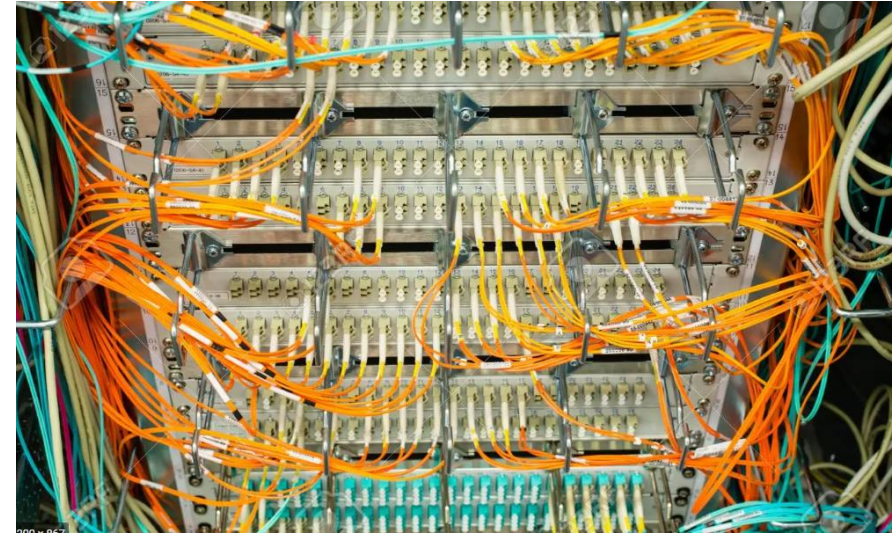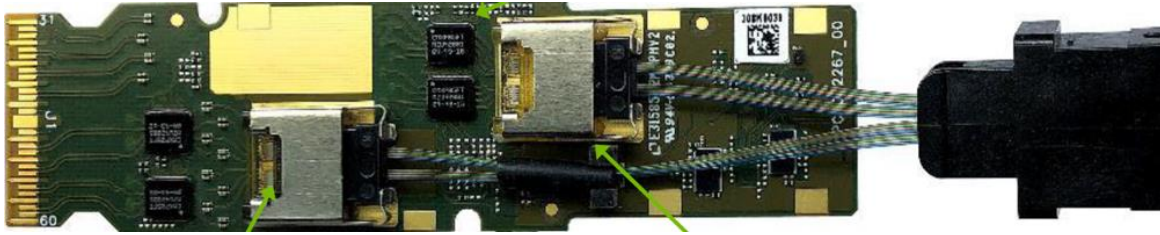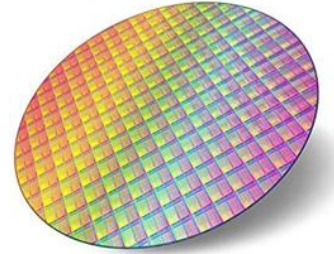
High Speed Networking: Advanced Packet Processing

Cybersecurity	Monitoring	Infrastructure	Cloud & Edge	Mobile	Financial Trading
Firewall	Application Performance	Stateful Load Balancer	Server Virtualization	vEPC, vBNG	Market Simulation
Next-Gen Firewall	Network Performance	Session Border Controller	vRouter	vBRAS, vFW	Low Latency Trading
Data Loss Prevention	Test & Measurement	Packet Broker	vSwitch	vGGSN, GTP FW	Market Data Capture
Intrusion Detection	Lawful Intercept	Virtualization and Slicing	Telemetry	vSGSN, vUPF	Latency Measurement
Intrusion Prevention	Network Recorder	Deep Packet Inspection		vRAN	
Threat Prevention	Forensics	SD-WAN		vIMS	
Web Application Firewall	Analytics			CORD	
Anti-virus, SIEM, VPN	Packet Capture			O-RAN / C-RAN	

Applications and Services that are accelerated by SmartNICs

napa:tech;
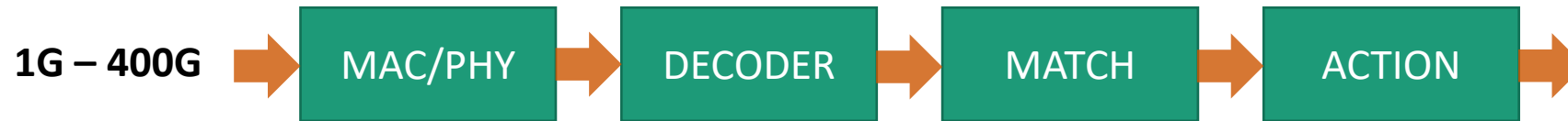RECONFIGURABLE COMPUTING

High Speed Networking:
Advanced Packet Processing
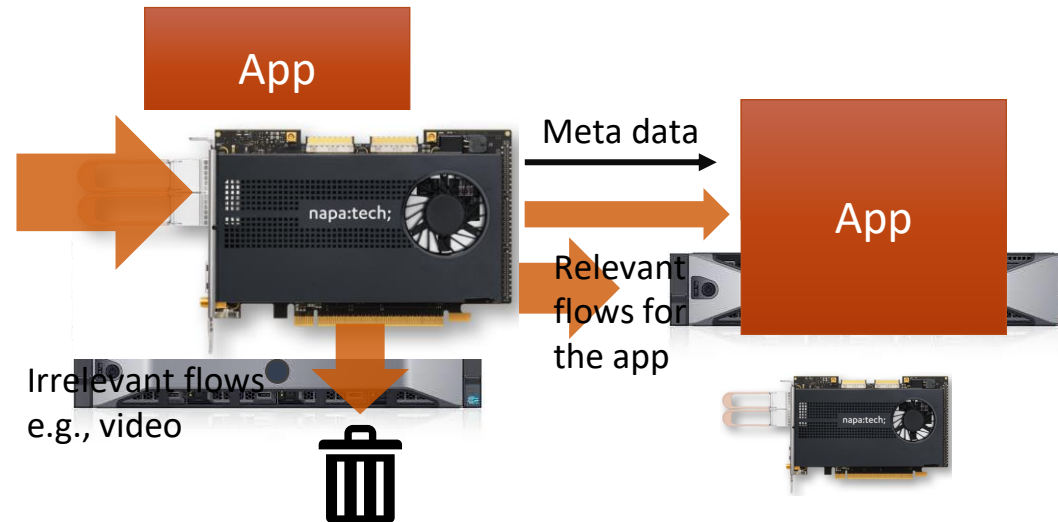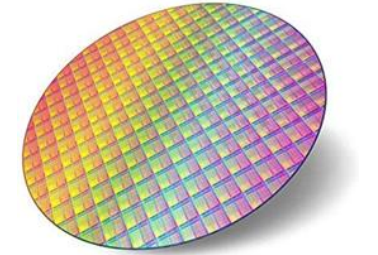
High Speed Networking: Advanced Packet Processing
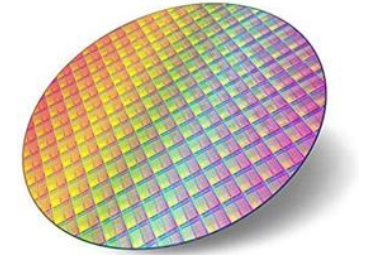
64B @ 400G -> ~600 M Packets per second!

1G – 400G → MAC/PHY → DECODER → MATCH → ACTION →

Network

Host/Application

| L2 | Tunnel header | Inner IP | Payload | CRC1 |

| L2 | Inner IP | Payload | CRC2 |

| L2 | Inner IP | Payload | CRC1 |

napa:tech;
RECONFIGURABLE COMPUTING

Thank You