Introduction to Chip Design 2025 - Group 1

GPIO controller, PWM & ~~Timers~~

Objectives

- Design and implement a GPIO module with configurable input/output functionality
- Design and implement a PWM timer for generating pulse-width-modulated signals
- Implement a bridge connecting to the selected bus architecture
- Integrate peripherals with the Wildcat CPU, memory-mapped interface
- Demonstrate functionality through simulation and verification

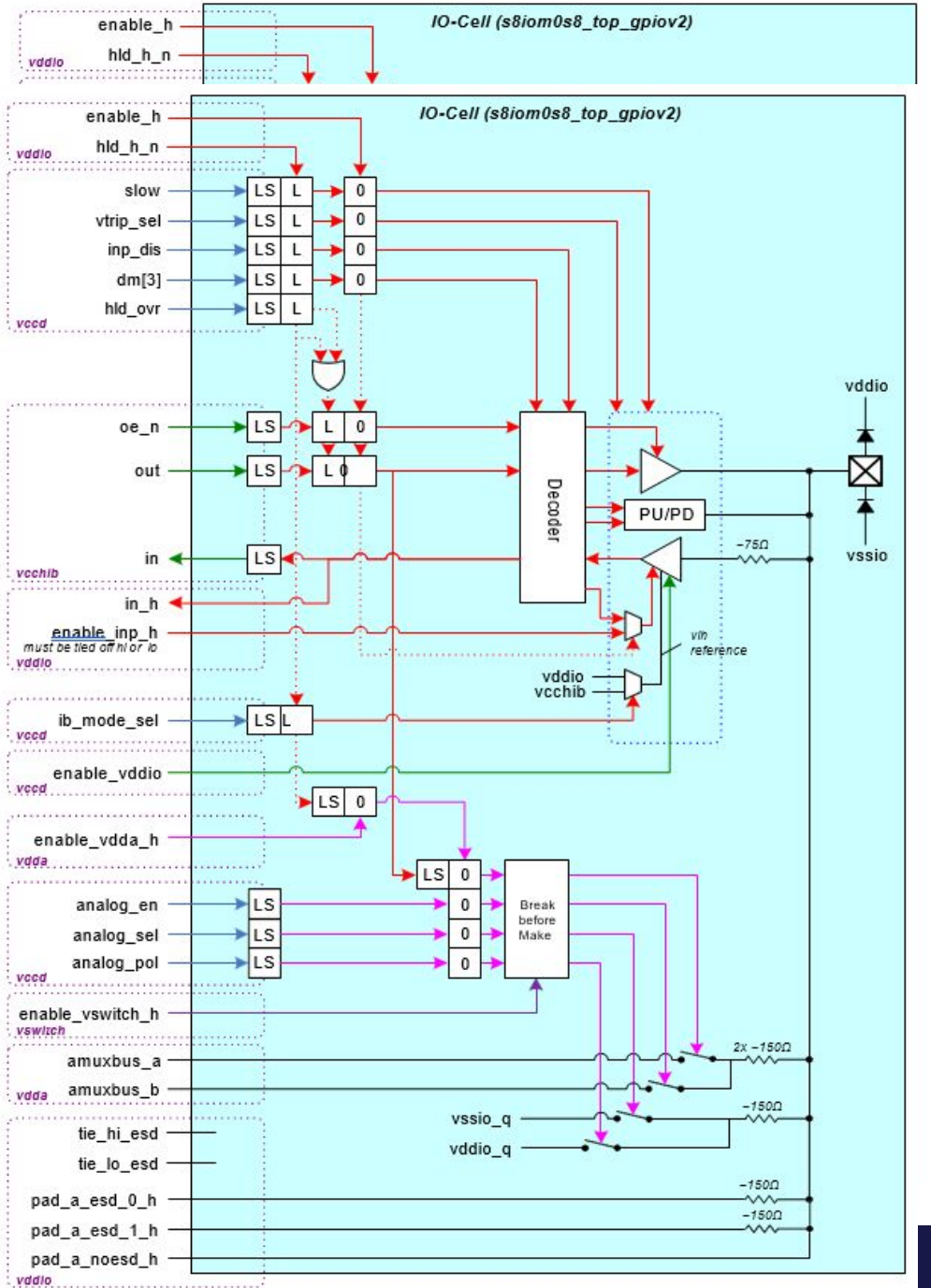
Current Actions

- Investigate the possibility of pull-up/pull-down resistors for the GPIO peripheral
- Investigating how the MUX-ing between input and output should be handled
- Investigate possibility output driver configuration (pushpull, open drain)
- Investigate ESD protection necessity

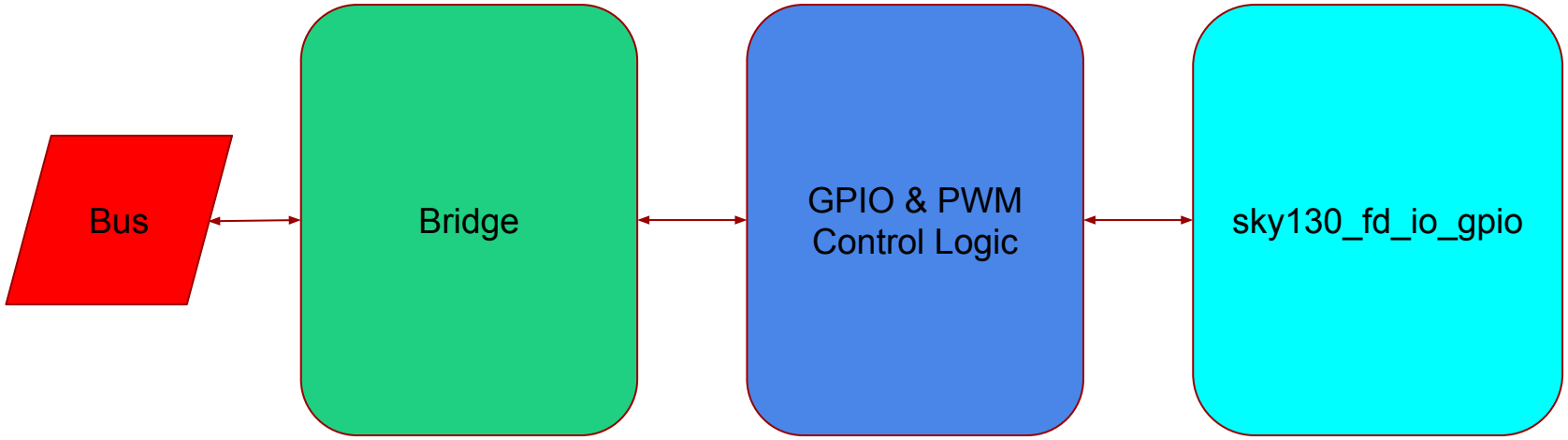
Preliminary Design - GPIO

- IO Cell for the analog front-end of the GPIO
  - sky130_fd_io__gpio
- The IO cell will be instantiated as a black box
- Main features:
  - Bidirectional operation
  - ESD protection
  - Configurable drive strength
  - Pull-up/Pull-down resistors

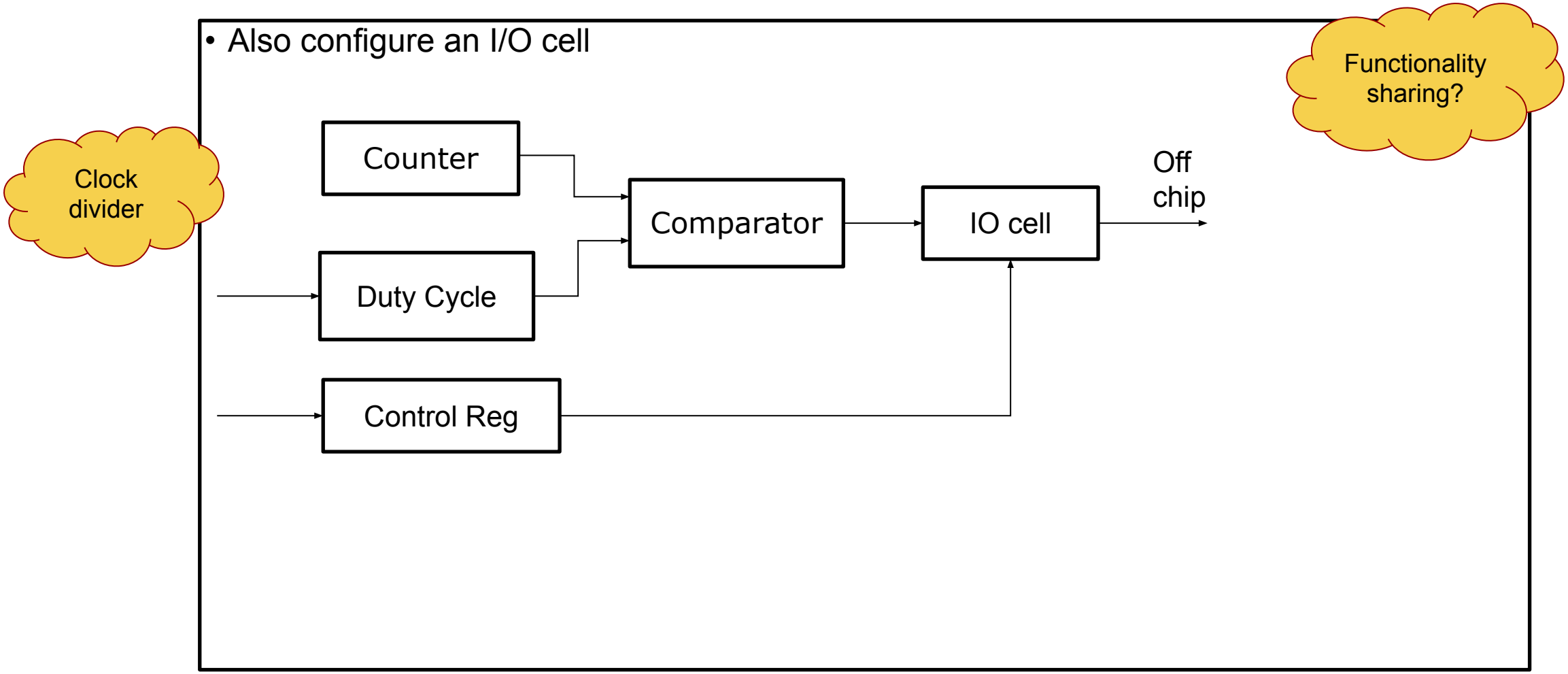
Maybe IHP PDK equivalent if exists.
Specifically we will create a wrapper that can handle one of those but easily be ported to the other.



Preliminary Design - to be finalized



Preliminary Design - PWM



Implementation & Verification Plan

- Chisel for RTL design
- Testbench in Chisel depending on whether we are testing at RTL or chip level (for chip level maybe cocotb similar to tiny tapeout)

Obstacles

- Getting familiar with the Wildcat CPU architecture and how the memory-mapped interface works
- Accurate PWM
- Figuring out getting the IOs placed optimally with Openlane
- Creating module to use for simulation of GPIO block for RTL level?