System integration

DTU SoC 2025 - Group 7

Primary objectives

System integration

- Outline (collaboratively) the overall project structure and design a single top level component that integrates with caravel.
- Automate caravel process (CI)
- Standardize pre-hardened or otherwise external components
    - Must provide mock component in code if we decide to go with a dual-repo setup
- Ensure no drift between simulation/verification benches between builds nor in module interfaces
- Handle breaking interface changes

CPU Integration

- Include CPU in project. [Completed]
- Provide testing primitives [Completed]
- Integrate with AX4-lite bus (group 20)
- Integrate with actual memory components (not mock)
- Create, automate and maintain test suite for CPU/hardware interaction

Design and implementation

- Proposed (project) structure
  - Every team provides an initial top level module API and potentially a mock implementation
  - We use this to create the top level module wrapper and start from there
- Proposed caravel workflow (1)
  - Fully integrated into the main repository, we produce the clean minimal template repository every time and invoke it directly from the main repository.
- Proposed caravel workflow (2)
  - We maintain both repositories and allow custom configuration / components directly in the caravel repository

- Create chisel top level module that adheres to `user_project_wrapper`
- Produce CPU-only test cases using simulated memories
- Produce CPU-only test cases using actual memories
- Integrate with each set of hardware
  - Produce test cases for each unique combination of CPU/Hardware etc.

Obstacles and open matters (blockers)

- Final decision on overall project structure, see 2 slides back point 1.
- Final decision on how to use soc-dtu-2025, see previous slide for suggestions.
- Awaiting integration with other hardware teams