

# On-Chip Logic Analyzer v1.0

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*IP User Guide*



January 10, 2023

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# IP Summary

## Introduction

The On Chip Logic Analyzer (OCLA) core is an AXI4-Lite compliant customizable logic analyzer that is designed to be used in applications that require verification or debugging by monitoring the internal signals of a design on FPGAs.

The OCLA core supports various features of a modern logic analyzer including trigger options like edge transition triggering, multi-triggers and other configurations options like number of probes and trace memory depth.

The OCLA has various modes of data capturing operation for debugging like continuous, pre-trigger, post-trigger and center-trigger options

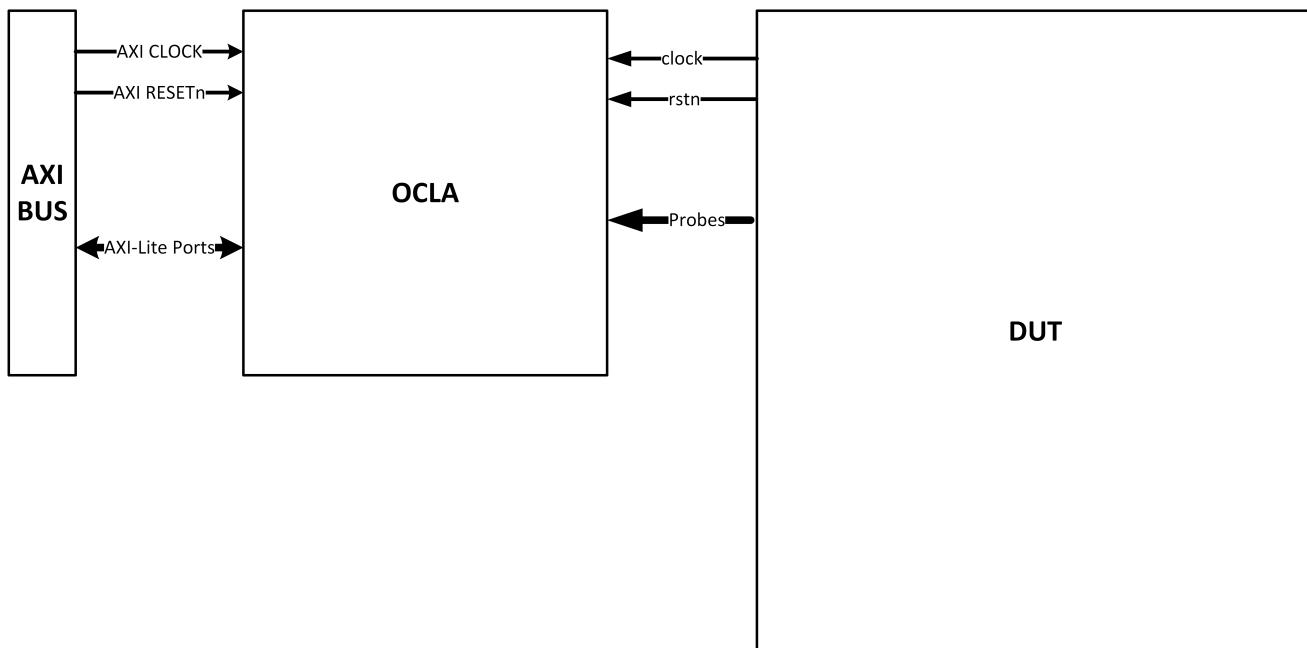
## Features

- Configurable number of probes
- Configurable trigger condition
- Configurable trigger mode
- Configurable number of input triggers
- Configurable data depth
- Configurable simple or advance trigger mode
- Configurable data sampling mode

# Overview

## On-Chip Logic Analyzer

OCLA is configured via its AXI-lite slave interface. It captures the signals' behavior that are connected to its probe port. It is synchronous to the design being monitored for data sampling operation. The figure 1 shows the OCLA IP core connection with a DUT on an FPGA.



**Figure 1.** OCLA Core Connected with a DUT

## Licensing

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# IP Specification

## Overview

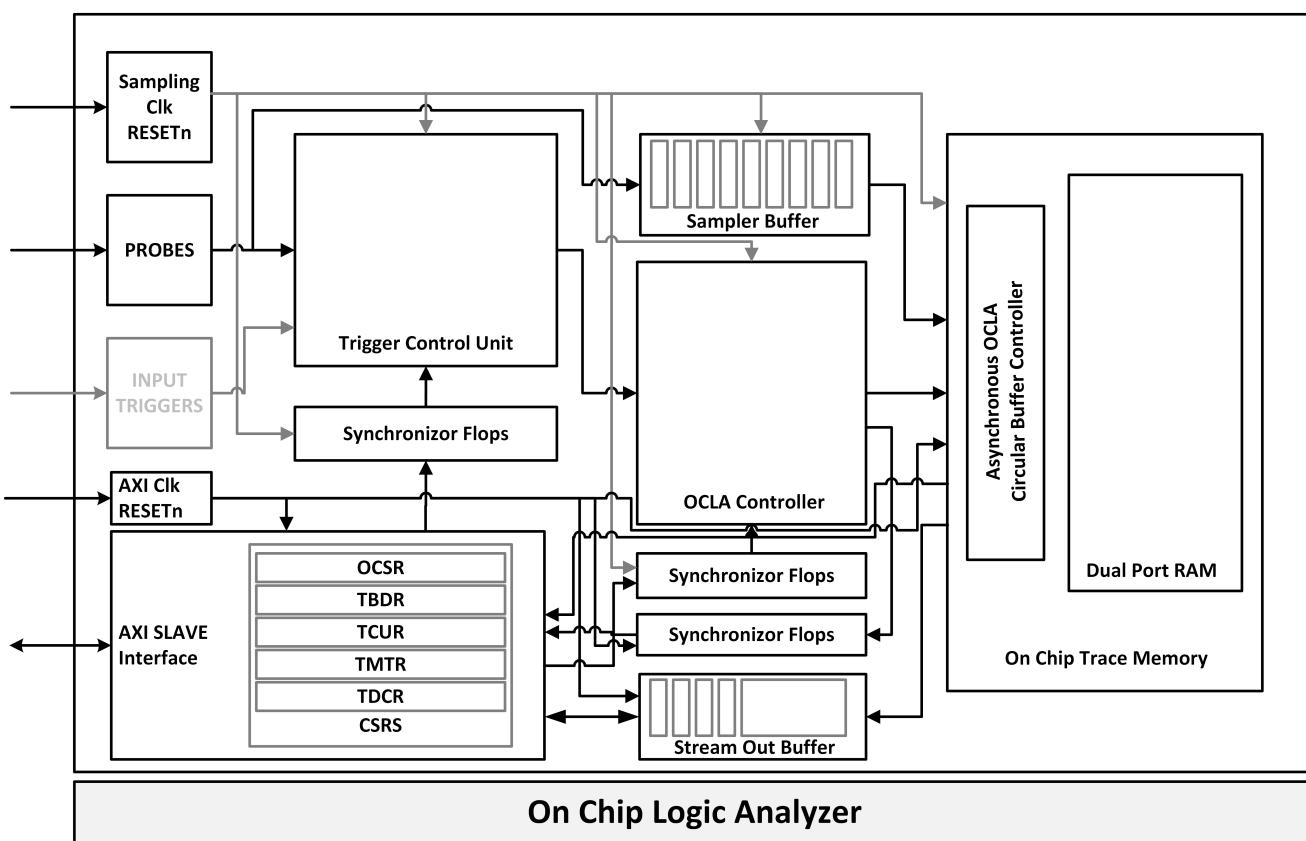
The figure 2 shows the internal block diagram of OCLA. It is a modular design consisting various modules like OCLA AXI-lite Slave interface, Trigger Control Unit, Sampler Buffer, OCLA Controller and OCLA On-Chip Trace Memory modules.

It is a multi-clock design and it has a sampling clock as well as the AXI bus clock. The sampling clock is the same clock as the clock of the System/Design under test (S/DUT).

Data is sampled on the rising edge of this sample clock based on the configured sampling mode of the OCLA. The OCLA is configured through the AXI interface on the rising edge of the AXI bus clock. The sampled data can be read via the AXI interface running on rising edge of the AXI clock.

The modules that controls the sampling operation of the OCLA operate on the sampling clock. For example the sampler buffer and the OCLA controller operates on sampling clock. On the other hand the AXI Slave and the Stream Out Buffer is modules operate on the AXI clock and these modules are used to configure or read the acquired data from the trace memory.

The On-Chip trace memory controller is a circular buffer based on a modified asynchronous FIFO that handles clock domain crossing of the trace memory data and configuration data .



**Figure 2.** Top Module

## Trigger

Triggers can be defined to configure the OCLA for capturing probe data samples. A probe input signal or a trigger input signal can be set as a trigger signal. A variety of trigger conditions can be configured on the trigger signal.

Data sampling begins when all of the trigger conditions in the active trigger pattern are satisfied. A Trigger Position setting (Trigger mode) allows the user to specify the amount of data captured by the OCLA that should be acquired before the trigger and the amount that should be acquired after the trigger. Acquired data is placed in a circular buffer.

OCLA supports simple and advance trigger options.

- In simple trigger option configuration the trigger condition can be applied on only a single probe channel.
- In advance triifer option configuration the trigger condition can be applied on two probe channels with boolean comparison applicable on their trigger conditions.

## Trigger Conditions

Multiple options for trigger conditions are available for probe and input triggers signals. Following lists the trigger conditions:

Trigger Condition	Description
Don't Care	Default trigger condition. The channel is not used to determine the trigger event.
Low level	OCLA triggers when the probe channel is low.
High level	OCLA triggers when the probe channel is high.
Falling Edge	OCLA triggers on the falling edge the probe channel.
Rising Egde	OCLA triggers on the falling edge the probe channel.
Either Edge	OCLA triggers on either edge of the probe channel.
Value Comparison	OCLA triggers when the value of a probe channel is equal /less than / greater than some user specified value.
Boolean Trigger equations	Advance Trigger Conditions AND, OR, <, >, == etc

**Table 1.** Trigger Conditions

## Trigger Modes

The common trigger modes are post trig, pre trig, center and countinous.

- In **pre triggered** the stored data set will consist of data sampled after the trigger.
- **Post triggered** is the opposite and in this mode the logic analyzer stops the sampling immediately when the trigger is raised thus only storing data from before the triggering event.
- **Center triggered** is a combination putting the triggering event in the middle of the sampled data set
- **Continous trigger** mode continounlly samples data.

## Fix number of samples

OCLA can be configured on run time to sample a specific number of probe samples other than the trace memory depth.

## Standards

The AXI4-Lite Slave interface is compliant with the AMBA® AXI Protocol Specification.

## IP Support Details

Compliance		IP Resources					Tool Flow		
Device	Interface	Source Files	Constraint File	Testbench	Simulation Model	Software Driver	Analyze and Elaboration	Simulation	Synthesis
GEMINI	AXI4-lite	Systemverilog	SDC	Systemverilog	-	-	Raptor	Raptor	Raptor

## Resource Utilization

Tool	Raptor Design Suite		
FPGA Device	GEMINI		
	Configuration		Resource Utilization
Minimum Resource	Options	Configuration	Resources
	Number of Probe	1	LUT
	Trace Memory Depth	32	DFFR
	Advance Trigger Mode	OFF	DFFRE
	Value Compare Feature	OFF	BRAM
	Input Triggers	0	DSP
Maximum Resource	Options	Configuration	Resources
	Number of Probe	1024	LUT
	Trace Memory Depth	1024	DFFR
	Advance Trigger Mode	ON	DFFRE
	Value Compare Feature	ON	BRAM
	Input Triggers	32	DSP

## Ports

Table 3 lists the top interface ports of the OCLA.

Signal Name	I/O	Description
<b>Sampling Clock and Reset</b>		
i_sample_clk	I	Clock to Sample the Probe Data. It must be same as the Design under test
i_rstn	I	Reset port of OCLA and it must be same as design under test
<b>AXI Clock and Reset</b>		
i_S_AXI_ACLK	I	AXI4-Lite Clock
i_S_AXI_ARESETN	I	AXI4-Lite RESET
<b>AXI WRITE ADDRESS CHANNEL</b>		
s_axil_awvalid	I	AXI4-Lite Write address valid
s_axil_awready	O	AXI4-Lite Write address ready
s_axil_awaddr	I	AXI4-Lite Write address
s_axil_awprot	I	AXI4-Lite Protection type
<b>AXI WRITE DATA CHANNEL</b>		
s_axil_wvalid	I	AXI4-Lite Write valid
s_axil_wready	O	AXI4-Lite Write ready.
s_axil_wdata	I	AXI4-Lite Write data
s_axil_wstrb	I	AXI4-Lite Write strobes
<b>AXI WRITE RESPONSE CHANNEL</b>		
s_axil_bvalid	O	AXI4-Lite Write response valid
s_axil_bready	I	AXI4-Lite Response ready
s_axil_bresp	O	AXI4-Lite Write response
<b>AXI READ ADDRESS CHANNEL</b>		
s_axil_arvalid	I	AXI4-Lite Read address valid
s_axil_arready	O	AXI4-Lite Read address ready
s_axil_araddr	I	AXI4-Lite Read address
s_axil_arprot	I	AXI4-Lite Protection type
<b>AXI READ DATA CHANNEL</b>		
s_axil_rvalid	I	AXI4-Lite Read valid
s_axil_rready	O	AXI4-Lite Read ready
s_axil_rresp	I	AXI4-Lite Read data
s_axil_rdata	O	AXI4-Lite Read response
<b>OCLA PORTS</b>		
i_probes	I	OCLA Probes port
i_trigger_input	I	OCLA Trigger input port. It is an optional port

## OCLA Interface

## Parameters

Table 4 lists the parameters of the OCLA.

Parameter	Values	Default Value	Description
NUMBER OF PROBES	1-1024	1	Number of OCLA probe ports.
MEMORY DEPTH	32, 64, 128, 256, 512,1024	32	Probe storage buffer depth. This number represents the maximum number of samples that can be stored at run time for each probe input.
NUMBER OF INPUT TRIGGERS	1-31	1	Number of trigger input ports.
PROBE WIDTH	1-31	1	Probe width in case of value compare mode

Parameters

## Optional Macros

Table 5 lists the Macros of the OCLA.

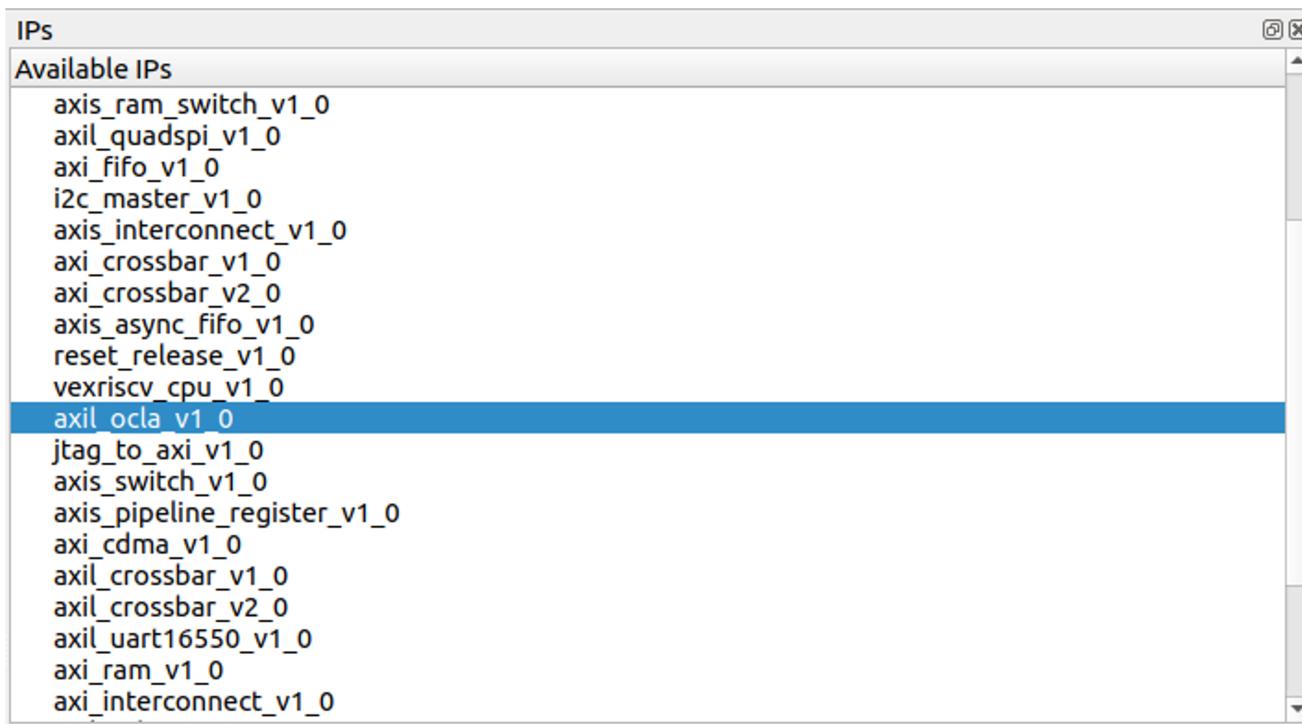
Feature	Macro	Description
Value Compare Feature	value_compare	To enable Value Compare feature
Advance Trigger Mode	advance_trigger	To enable Advance Trigger Mode
Enable Trigger Inputs	trigger_inputs_en	To enable Trigger inputs

Parameters

# Design Flow

## IP Customization and Generation

OCLA IP core is a part of the Raptor Design Suite Software. A customized ocla can be generated from the Raptor's IP configurator window.



IP list

**Parameters Customization:** From the IP configuration window, the parameters of the OCLA can be configured and OCLA features can be enabled for generating a customized OCLA IP core that suits the user application requirement.

Configure IP

Configuring axil\_ocla (v1.0) from rapidsilicon's ip library

Parameters

MEM_DEPTH	32
ADDR_WIDTH	32
DATA_WIDTH	32
NO_OF_PROBES [1, 1024]	1
NO_OF_TRIGGER_INPUTS [1, 31]	1
PROBE_WIDTH [1, 31]	1
VALUE_COMPARE	<input type="checkbox"/>
ADVANCE_TRIGGER	<input type="checkbox"/>
TRIGGER_INPUTS_EN	<input type="checkbox"/>

Output

Module Name	axil_ocla_wrapper
Output Dir	:cts/ocla_soft_ip/ocla_soft_ip.IPs/rapidsilicon/ip/axil_ocla/v1_0/axil_ocla_wrapper

IP Configuration

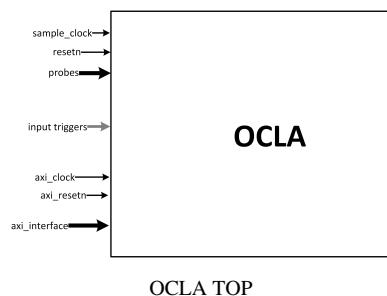
# OCLA Debug Subsystem

## The Generated OCLA IP Wrapper

After the IP customization and generation step, a top wrapper plus all source file are made available to the user. The generated top wrapper file for OCLA 5 has two different clocks i.e., the sample clock and the AXI clock. The sample clock of the OCLA is to be connected with the design being monitored and the AXI clock is to be connected to an AXI bus clock.

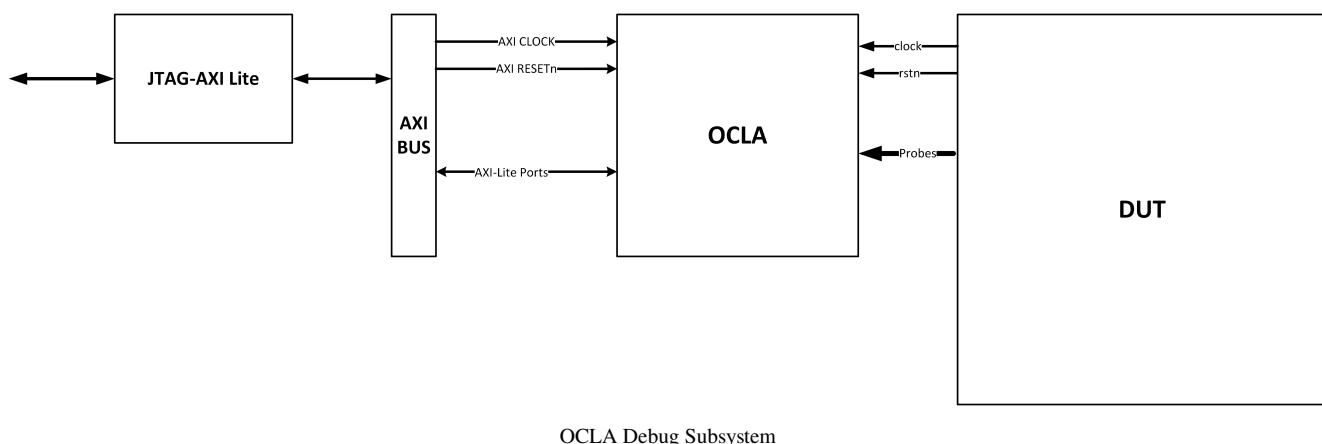
The signals of the design that are to be sampled are connected to the probes port of the OCLA and the user specified input triggers signals can be connected to the corresponding port in the top wrapper.

For the OCLA configuration and to read the sampled data from the OCLA the AXI-lite slave interface can be connected to an AXI bus.



## OCLA Debug Subsystem

The OCLA top wrapper can be instantiated in a subsystem like the one shown in the figure 6 for debugging purpose. In the debug subsystem the OCLA IP core is integrated in between the AXI bus and the design being monitored. All the runtime OCLA configurations are controlled though JTAG interface.



# Test Bench

There is no test bench for this IP

# Revision History

Date	Version	Revisions
January 10, 2023	0.01	Initial version OCLA User Guide Document