CPUGEN 2.00 (TM)

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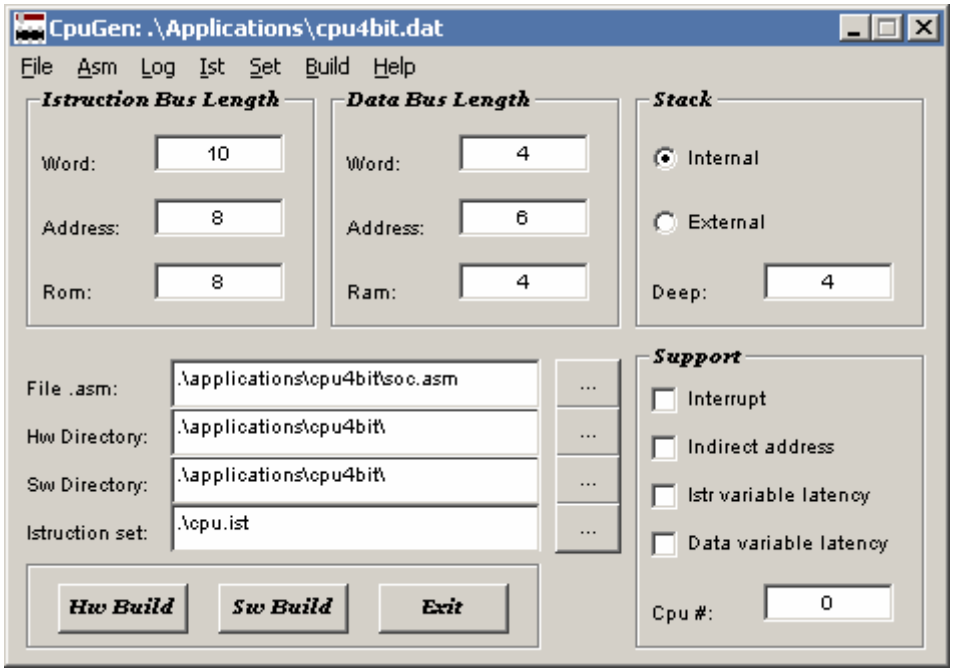
Overview



Cpugen (TM) is a graphical interface to **cpuasm** (TM) and **cpucore** (TM).
It allows creation of a configurable VHDL cpu and ram/rom code to be downloaded to a FPGA design.
The cpu and code parameters are stored inside a .dat file to be loaded via the **File/Open** menu.
Set/FileAsm menu allows to choose the assembler source code.
HwBuild generates the VHDL cpu code into the HW directory (**Set/HWDirectory**);
SwBuild generates the FPGA ram/rom files into the SW directory (**Set/SWDirectory**).
Asm opens the Assembler file whilst **Log** logs the cpuasm report after **SwBuild**.
Instruction set file permits to set a custom assembler istruction set encoding.
CPU# permits to generate HW/SW files with different prefixes.

The meaning for other dialog items in the above picture can be easily understood by reading the cpucore companion help file.

Istruction Bus Length

- Word = IWL = Instruction Word Length
- Address = IAL = Instruction Address Length
- Rom = IRL = Instruction ROM Length

Data Bus Length

- Word = DBL = Data Bus Length
- Address = DBAL = Data Bus Address Length
- Ram = DBRL = Data Bus RAM Length

Stack

- Internal/External = ST = Stack Type
- Deep = HSD = Hardware Stack Deep

Support

- Interrupt = I
- Indirect Address = IA
- Istruction Variable Latency = IVL
- Data Variable Latency = DVL