CPUGEN 2.00 (TM)

gferrante@opencores.org

Overview

CpuGen: .\Applications\cpu4bit.dat	_
File Asm Log Ist Set Build Help	
Istruction Bus Length — Data Bus Length	Stack
Word: 10 Word: 4	● Internal
Address: 8 Address: 6	C External
Rom: 8 Ram: 4	Deep: 4
File .asm:	Support
Hw Directory: \(\text{\Applications\cpu4bit\} \)	☐ Interrupt ☐ Indirect address
Sw Directory: \(\lambda applications\cpu4bit\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	Istr variable latency
Istruction set:	Data variable latency
Hw Build Sw Build Exit	Cpu#: 0

Cpugen (TM) is a graphical interface to ${\it cpuasm}$ (TM) and ${\it cpucore}$ (TM).

It allows creation of a configurable VHDL cpu and ram/rom code to be downloaded to a FPGA design.

The cpu and code parameters are stored inside a .dat file to be loaded via the ${\bf File/Open}$ menu.

 ${\bf Set/FileAsm}$ menu allows to choose the assembler source code.

HwBuild generates the VHDL cpu code into the HW directory (Set/HWDirectory); SwBuild generates the FPGA ram/rom files into the SW directory (Set/SWDirectory).

Asm opens the Assembler file whilst Log logs the cpuasm report after SwBuild. Instruction set file permits to set a custom assembler istruction set encoding. CPU# permits to generate HW/SW files with different prefixes.

The meaning for other dialog items in the above picture can be easily understood by reading the cpucore companion help file.

Istruction Bus Length

- Word = IWL = Instruction Word Length - Address = IAL = Instruction Address Length - Rom = IRL = Instruction ROM Length

Data Bus Length

- Word = DBL = Data Bus Length - Address = DBAL = Data Bus Address Length - Ram = DBRL = Data Bus RAM Length

Stack

- Internal/External = ST = Stack Type - Deep = HSD = Hardware Stack Deep

Support

- Interrupt = I - Indirect Address = IA - Indirect Address
- Istruction Variable Latency = IVL
Data Variable Latency = DVL - Data Variable Latency